# Online Condition Monitoring Methodology for Power Electronics Package Reliability Assessment

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# Online Condition Monitoring Methodology for Power Electronics Package Reliability Assessment

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***Abstract*—This article introduces an online condition monitoring strategy that utilizes a transient heat pulse to detect package thermal performance degradation. The metric employed is the temperature-dependent transient thermal impedance "$Z_{\text{th}}(t, T_{\text{amb}})$." The proposed methodology offers quantitative insights into package thermal performance degradation and effectively pinpoints the presence of multiple failure mechanisms. A thermal test chip assembled in a power quad flat no-lead package is used in this study to demonstrate the methodology. The packaged devices are first characterized to determine the transient pulse duration, a critical parameter to monitor a specific region of interest. Subsequently, package thermal performance degradation is continuously monitored online during thermomechanical cycling lifetime experiments. The validity of the measurement results is later confirmed through acoustic imaging and cross-sectional analysis. The changes observed in $Z_{\text{th}}(t, T_{\text{amb}})$ over thermal cycling correspond to the delamination of the active metal layers on the die and cohesive failure on the die attach. This article further includes a comparative summary, highlighting the distinctions between the proposed and industry-standard test methods. In conclusion, the importance of online condition monitoring to detect early signs of failure is emphasized, and the proposed methodology's practical applicability in real-life scenarios is briefly discussed.**

***Index Terms*—Application-driven reliability qualification, silver sintering, thermal cycling, thermal test chips (TTCs), transient thermal impedance.**

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## I. Introduction

IN TODAY'S rapidly evolving technological landscape, ensuring power electronics package reliability is crucial as the scaling of More than Moore and mission-profile-based applications is becoming significantly important [1]. Recent advancements in power electronics reliability research are provided in [2]. Surveys conducted across various highly demanding industrial applications indicate power semiconductor devices to be particularly susceptible to failures [3], [4], [5], [6], [7], [8]. Power devices in field-critical applications undergo various stresses, including electrical overstress, mechanical vibrations, environmental humidity, and temperature fluctuations. While electrical, mechanical, and chemical-related issues are essential considerations for package reliability, thermal breakdowns pose a particularly severe challenge [9], [10]. Thermal bottlenecks and thermomechanical challenges primarily arise from the packaging materials' inhomogeneities. The mismatch in thermal expansion coefficients between the semiconductor die and the package substrate creates residual stresses, ultimately leading to thermal performance degradation.

Power packages are commonly subjected to rigorous stress tests such as active power cycling [11] and temperature cycling [12] to ensure reliability and meet qualification standards [13], [14]. However, the "test-to-fail" approach mostly involves offline monitoring and necessitates destructive techniques to identify failures. Hence, there is a clear need for online condition monitoring strategies to detect early signs of failure and gain quantitative insights. Further references to condition monitoring methods, online measurements, and lifetime reliability models are provided in [15], [16], [17], [18], [19], [20], [21], [22], and [23].

In this research, we present a novel methodology for identifying the temperature-dependent transient thermal impedance, denoted as "$Z_{\text{th}}(t, T_{\text{amb}})$," by utilizing a transient pulse. Our methodology demonstrates the following in this article:

1) online monitoring of package thermal performance degradation during accelerated lifetime testing;
2) quantitative insights into the package degradation behavior and the ability to detect the presence of multiple failure mechanisms;
3) applicability of the proposed methodology on functional power devices [MOSFETs and insulated-gate bipolar transistors (IGBTs)] to facilitate application-driven qualification in real-life scenarios.

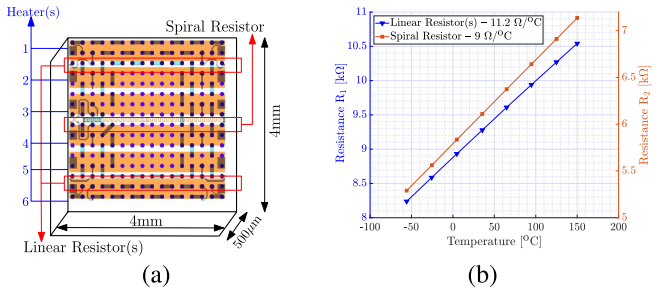


Fig. 1. (a) Layout of the TTC, depicting its geometry, in-built heaters, and resistors. (b) Resistance sensitivity of linear and spiral resistors evaluated at eight temperature points ranging from −55 to 150 °C, demonstrating a linear temperature dependence.

The following section covers the semiconductor device selection, packaging materials, and the experimental methodology. The experimental results and analysis are presented subsequently with a brief discussion on practical challenges. Finally, a comparison to the industry standard thermal characterization methods is summarized.

## II. Experimental Methods

### A. Sample Preparation

Silicon-based thermal test chips (TTCs) are specialized devices fabricated using the same process technology as semiconductor devices. These test chips feature lithographically defined heating and temperature sensing elements designed to optimize and evaluate package thermal performance. Several research efforts have been devoted to developing TTCs for interconnect material characterization and package reliability assessment [24], [25], [26], [27]. Since TTCs realistically represent thermal challenges that actual power components experience in operation, we chose them as a test vehicle in this study to demonstrate the online monitoring methodology. However, it is worth noting that the methodology can also be applied to functional power devices like MOSFETs and IGBTs by utilizing their temperature-sensitive electrical parameters for both heating and temperature sensing purposes.

The TTC chosen for this study contains six heaters and three resistance-based temperature detectors (RTDs) [see Fig. 1(a)]. The temperature dependence of the linear and spiral RTDs was measured at eight different temperatures ranging from −55 to 150 °C, revealing a linear relationship [see Fig. 1(b)]. The differences in resistance sensitivity between the linear and spiral RTDs arise from their geometrical variations. Normalizing the resistance sensitivity with the base resistance yields the resistor material's temperature coefficient resistance. In the rest of this article, Heater-3 was used for heating, and the spiral resistor was used for temperature sensing. Further details about the TTC are provided in [25] and [28].

The choice of interconnect material is a critical factor in package assembly. High-temperature Pb-rich solders have been favored in power electronics for their high melting point (≥ 300 °C) and low stiffness (∼45–60 GPa). However, their usage has been progressively reduced due to concerns about lead toxicity. An alternative technology for die attachment has emerged in the form of sintering metal particles (lead-free compositions). Metal precursors (Ag/Cu) in paste form are fused under heat and pressure. A review of die-attach materials for high-temperature applications, recent advancements in sintering materials, and lifetime modeling are provided in [29], [30], [31], [32], and [33].

The package assembly process involved in this study is further enumerated as follows.

1) A pressureless micro-Ag sinter material in the form of wet paste was screen printed onto a silver-metalized copper lead frame [see Fig. 2(a)].
2) The TTC was then wet mounted over the sintering paste and sintered in a nitrogen-filled oven at 150 °C for 60 min, followed by an additional 60 min at 200 °C. After sintering, electrical connections were established using 99.99% pure gold wire bonds with a bond wire diameter of 25 $\mu$m and a bond bump of 50 $\mu$m [see Fig. 2(b)].
3) Subsequently, the entire stack was transfer molded using an epoxy molding compound, and individual packages were then singulated [see Fig. 2(c)].
4) The integrity of the package was further assessed through X-ray inspection, which offers high contrast with low-density materials like silicon and polymers compared to heavy metals such as gold and silver. This enables the detection of inhomogeneities in wire bonds and die attachments. An X-ray image of an overmolded package is presented in Fig. 2(d), illustrating the absence of voids or wire bond failures.
5) The packages were soldered onto an especially designed test board with four-point Kelvin connections extending up to the device, as depicted in Fig. 2(e). The solder joint interface was assumed to remain stable during the lifetime test.

### B. Experimental Setup

A dedicated setup was developed for online monitoring of the package condition during thermomechanical cycling lifetime (TMCL) testing, as illustrated schematically in Fig. 3. The test boards, soldered with power quad flat no-lead (PQFN) packages [see Fig. 2(e)], were securely placed on a test socket inside a temperature cycling oven. The electrical connections from the test socket were extended to the sourcing and measuring equipment using a multiplexer (switch matrix), allowing for sequential measurements. The source unit has 40-V compliance at 1 A in continuous mode and 20 V at 10 A in pulsed mode. A trigger synchronization and communication protocol (TSP) was established between the instruments to ensure proper synchronization and communication. A dedicated control program exchanges data between the master computer and the TMCL oven. A user-defined MATLAB program manages all instrument communications.

The measurement conditions were fine-tuned to optimize the RTD sensitivity. Various input currents were applied to the test chips to determine the optimal measurement currents (≤0.3 mA)

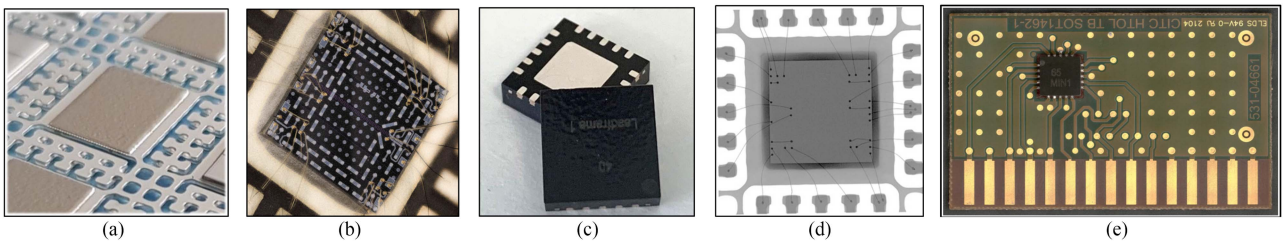


Fig. 2. Illustration of the steps involved in the package assembly process. (a) Micro-Ag sinter material screen printed on a lead frame. (b) Sintering of a test chip onto the lead frame with wire bonding. (c) Molded, singulated, and laser marked PQFN packages. (d) X-ray inspection of a molded package. (e) PQFN soldered to a test board for online measurements.

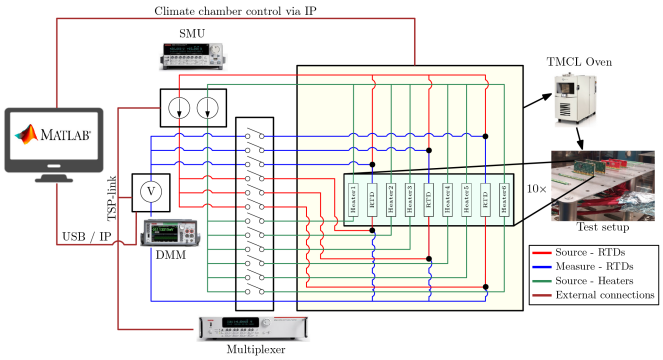


Fig. 3. Schematic of the experimental setup for online condition monitoring during accelerated lifetime testing. Packaged devices, soldered to the test boards, are placed in dedicated slots inside a temperature-cycling oven. Test boards are connected to a source measurement unit (SMU) and a digital multimeter (DMM) through a multiplexer for sequential measurements.

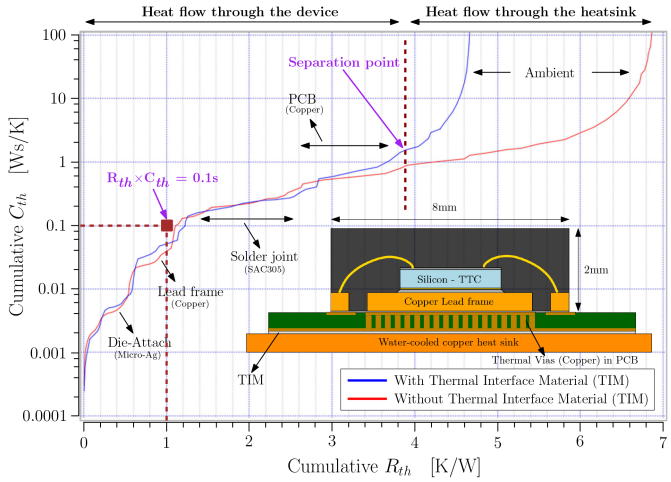


Fig. 4. Cumulative resistance ($R_{\text{th}}$)–capacitance ($C_{\text{th}}$) network graph from the measured data. The PQFN on a test board, mounted on a water-cooled heat sink, allows heat flow from the device toward the heat sink. Analysis with and without a TIM identifies the key heat dissipation information, notably at the die-attach interface, within a 0.1-s transit time window.

with minimal self-heating effects. The measuring equipment has a resolution of 1 $\mu$V for measurements in the 10-V range, and the accuracy was determined to be within $\pm$0.1 mV. Further information regarding measurement variation, repeatability, and reproducibility can be found in [28]. While the electrical layout depicted in Fig. 3 pertains to the test chip configuration, the test setup also features dedicated slots designed to measure up to 15 MOSFETs and/or IGBTs sequentially.

### C. Experimental Characterization

The thermal characterization methodology employed in this study is an adaptation of the JESD51-14 transient dual interface test method [34]. To analyze the package thermal performance, it is necessary to measure the transient thermal impedance $Z_{\text{th}}(t)$. This parameter represents the packaging materials' ability to dissipate heat, and it is a sum of individual layer resistances $R_{\text{th}}$. In this study, Heater-3 was used for heating, and the spiral resistor (RTD-2) was used to measure the change in electrical resistance due to heating, which further translates to device temperature. To ensure efficient heat dissipation, the test boards were clamped onto a water-cooled heat sink, and thermal characterization was conducted with and without a thermal interface material (TIM).

A continuous current of 100 mA (equivalent to approximately 0.7 W or 32 W/cm $^2$ at 25 °C ambient) was supplied to Heater-3 for a duration of 100 s. This current value was selected in consideration for online monitoring experiments during thermal cycling. The intention was to apply a brief localized heat pulse that would generate sufficient heat for package thermal performance analysis without deviating beyond the limits set for thermal cycling. The resulting changes in the resistance of RTD-2 were measured to determine the device temperature. During the 100-s heating period, the device and packaging materials reached a 1-D steady state, allowing the extraction of the resistance–capacitance network. This was achieved by computing the structure function, as described in [35], [36], and [37]. The TDIM-Master software provided by JEDEC [34] was used for time-constant spectrum deconvolution and Foster–Cauer transformation. The computed results of the structure function are depicted in Fig. 4, along with a schematic representation of the PQFN package on a printed circuit board (PCB) mounted to a heat sink.

Based on the thermal characterization measurements depicted in Fig. 4, the following conclusions and assumptions were drawn to support the online condition monitoring experiments.

1) Fig. 4 illustrates the separation point distinguishing the heat flow paths between the device (PQFN + PCB) and the heat sink. Regarding heat flow through the device, the

primary sources of resistance are the package solder joint interface and the PCB.

2) Given that the die-attach interface is the region of interest, a transient pulse duration of 0.1 s was chosen for localized heating and online condition monitoring, as highlighted in Fig. 4. The transient pulse duration of 0.1 s was chosen to limit the influence of the solder joint and the PCB materials.
3) The 0.1-s heating window defines a thermal resistance boundary of 1 K/W (see Fig. 4). Due to thermal aging, the packaging material's thermal resistance might shift, subsequently altering the boundary conditions for a 0.1-s heating interval. Since the region of interest is to monitor the die-attach interface, we assumed that the thermal resistance shift of the die-attach layer over the lifetime testing would not exceed the thermal resistance boundary.

### D. Online Condition Monitoring Methodology

Packaging materials undergo degradation over time, influenced by operational and environmental conditions. Package degradation may cause an increase in thermal resistance and impede heat dissipation, resulting in elevated device temperatures. Traditional thermal characterization methods, such as MIL-STD-883E, involve invasive means to measure the device junction and its case temperatures to determine the "steady-state" thermal impedance [38]. This method has been surpassed by transient thermal impedance measurements proposed by Székely [35], which has been adopted as the JEDEC standard JESD51-14 [34]. These approaches are suitable for offline monitoring and thermal characterization.

In this study, we introduce a novel "temperature-dependent transient-pulse test method" to obtain the temperature-dependent transient thermal impedance, denoted as $Z_{\text{th}}(t, T_{\text{amb}})$. The transient time is the transient pulse duration illustrated in Fig. 4, and the temperature dependence is established by measuring $Z_{\text{th}}(t)$ at different temperature ambients during TMCL testing. This approach allows for characterizing the package's thermal behavior under dynamic conditions.

The TMCL tests were in accordance with the guidelines outlined in the JESD22-A104 standard [12] and automotive norms AEC-Q101 [14]. The PQFNs with TTC soldered to the PCB underwent thermal cycling from $-55\,^{\circ}\text{C}$ (compression state) to $150\,^{\circ}\text{C}$ (expansion state), as illustrated in Fig. 5. The temperature cycling rate was maintained at approximately one to two cycles per hour, with a rise time ($t_{\text{rise}}$) and fall time ($t_{\text{fall}}$) of around 10 min. The dwell time ($t_{\text{dwell}}$) was dependent on the time required for the oven to reach a stable temperature. Although thermal cycling is a relatively slow process for power device aging, the transient pulse measurements for online monitoring take only a few second per device. Once the oven's temperature stabilized, a short transient heat pulse of 0.1 s was applied using Heater-3, and the device temperature was measured using RTD-2. It is important to be aware that the measurements were conducted without a water-cooled heat sink due to thermal cycling.

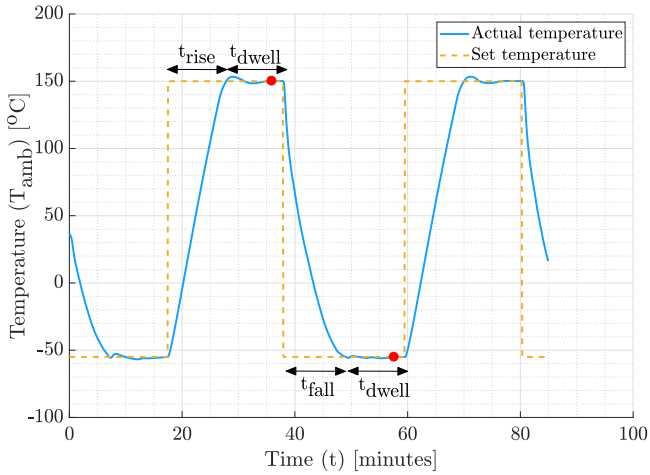


Fig. 5. Graph illustrating the temperature cycling profile adapted according to JEDEC standards for automotive-grade discrete semiconductor devices. The devices are cycled at one to two cycles per hour. $Z_{\text{th}}$ ($t = 0.1$ s) was measured during every cycle once the oven reached a stable temperature, as indicated by a red dot in the graph.

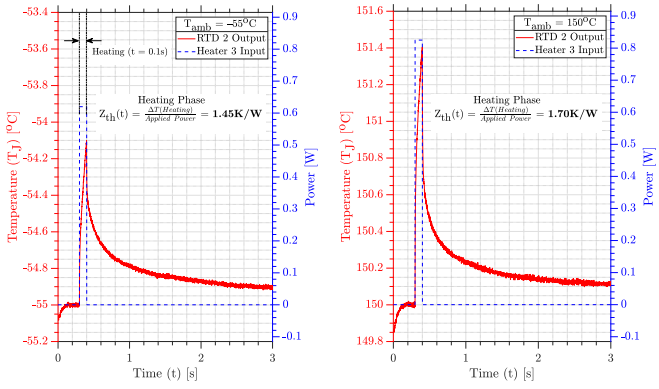


Fig. 6. (a) Measurements at $-55\,^{\circ}\text{C}$. (b) Measurements at $150\,^{\circ}\text{C}$. A 0.1-s 100-mA heat pulse applied to Heater-3, with junction temperature ($T_j$) measured using RTD-2 at different ambient temperatures ($T_{\text{amb}} = -55$ and $150\,^{\circ}\text{C}$). The applied power input varied with $T_{\text{amb}}$ due to the temperature sensitivity of the heater material. Differences observed in $Z_{\text{th}}(t)$ at different $T_{\text{amb}}$ result from the temperature-dependent thermal properties of packaging materials, where silicon plays a significant role.

The transient pulse response of RTD-2 measured at $-55$ and $150\,^{\circ}\text{C}$ is shown in Fig. 6, along with the applied input power for the heater. The initial fluctuations observed within the first 0.2 s are a measurement artifact resulting from the trigger range settings of the sourcing equipment. The differences in power input at $-55$ and $150\,^{\circ}\text{C}$ are due to the temperature sensitivity of the heater material. Hence, the temperature change $\Delta T$ was normalized with the applied input power to obtain the transient thermal impedance $Z_{\text{th}}(t)$. The $Z_{\text{th}}(t)$ parameter was determined during the heating phase since the heating time chosen was not long enough for the device to reach a steady state. Besides, the test chip has separate structures for heating and sensing, with heating power remaining relatively constant during the heating pulse time and no electrical crosstalk occurring to the sensing

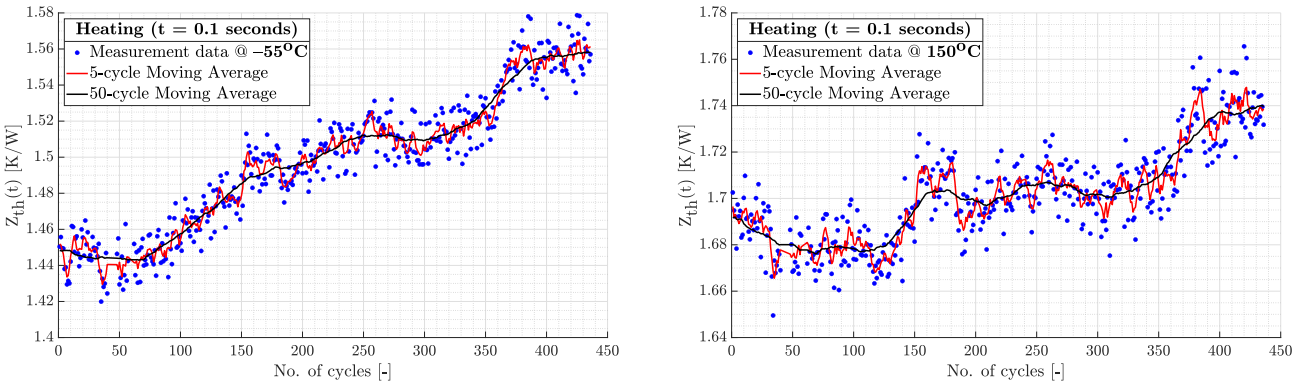


Fig. 7. (a) Measurement data at −55 °C. (b) Measurement data at 150 °C. The measurements were halted at 436 cycles, as the acquired data were deemed sufficient to demonstrate the methodology.

element. Hence, in accordance with JESD51-14 standards, it is acceptable to extract $Z_{\text{th}}(t)$ during the heating phase.

$Z_{\text{th}}(t)$ obtained from Fig. 6 exhibits strong temperature dependence, which can be attributed to the temperature-dependent thermal properties of the packaging materials. The micro-Ag sinter die attach and the copper lead frame exhibit minimal temperature dependence within the thermal cycling temperature range [39], [40]. However, the thermal properties of the semiconductor substrate (Silicon) undergo significant changes with temperature [41]. Therefore, the observed change in temperature $\Delta T$ between −55 and 150 °C (see Fig. 6) is influenced by the temperature-dependent properties of the silicon substrate. A theoretical explanation of the temperature-dependent properties of the packaging materials and their impact on the relative change in temperature $\Delta T$ is provided in [28]. The change in temperature-dependent transient thermal impedance "$Z_{\text{th}}(t, T_{\text{amb}})$" parameter over "$N$" thermal cycles indicating the package's health is demonstrated in the subsequent section.

It is important to be aware that an increment in $Z_{\text{th}}(t)$ would suggest degradation and the dissimilarities at different temperatures $Z_{\text{th}}(t, T_{\text{amb}})$ would signify the degradation behavior.

## III. Experimental Results and Discussion

### A. Online Condition Monitoring Results

The transient thermal impedance $Z_{\text{th}}(t)$ obtained from the transient pulse measurements (see Fig. 6) was continuously monitored during thermal cycling until a sufficient amount of data on package degradation were obtained to demonstrate the online monitoring methodology. Ideally, $Z_{\text{th}}(t)$ should remain constant (within the measurement variability) over time. However, due to continuous cyclic loading, the packaging materials tend to degrade, resulting in an increase in the $Z_{\text{th}}(t)$ value. Since the transient time is kept short ($t = 0.1$ s), the obtained time-transient $Z_{\text{th}}$ information reflects the behavior of the materials near the die, such as die attachment, as observed in experimental characterization (see Fig. 4). The measurement results of 436 thermal cycles at −55 and 150 °C are presented in Fig. 7.

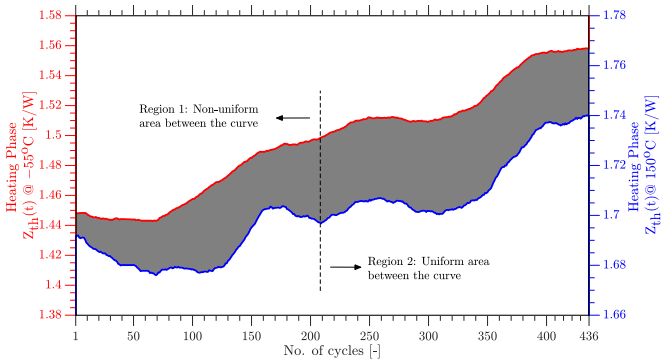


Fig. 8. Differences in the measurements at −55 and 150 °C are visualized by highlighting the area between the curves. Two distinct regions (Region-1 and Region-2) can be identified within the highlighted area. Region-1 indicates a nonuniform increase between the curves, and Region-2 indicates a relatively uniform increase.

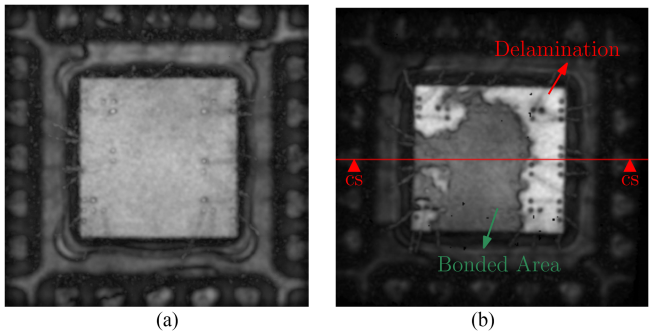


Fig. 9. (a) Reference PQFN sample at zero cycle. (b) Device under test after 436 thermal cycles. A sequential lateral scan (C-scan) analysis reveals signs of delamination near the overmold-die interface, clearly distinguishable from bonded areas in the thermally cycled sample. Further cross sectioning of the delaminated sample is highlighted in (b).

To facilitate the visual interpretation of the measurement data and identify the degradation trend, simple moving averages (SMAs) were calculated for the variable vector $Z^i_{\text{th}}(t)$ over $N$ observations. The five-cycle moving average highlights short-term fluctuations in the measurements, while the 50-cycle moving

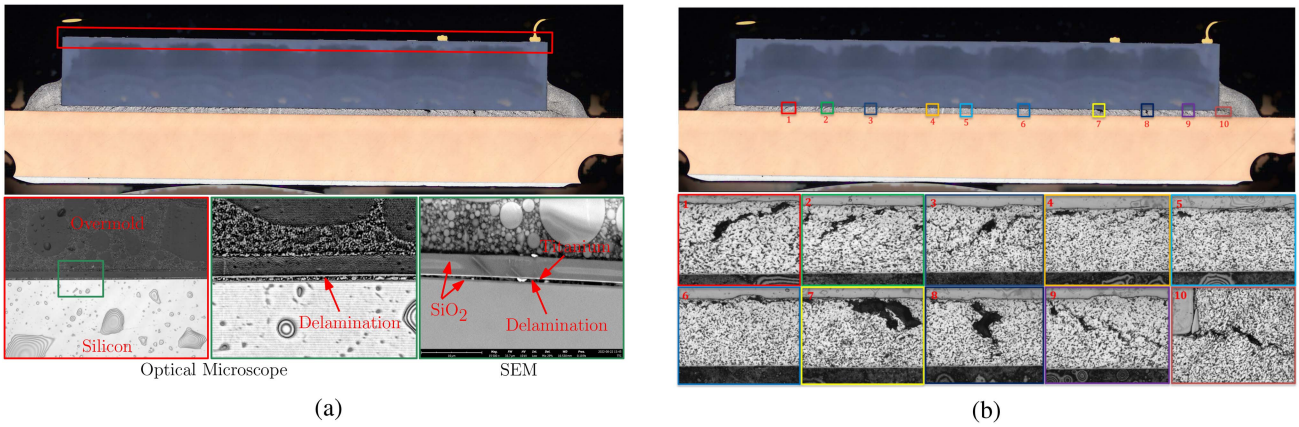


Fig. 10. (a) Cross-sectional micrographs focused near the overmold-die interface indicate delamination of titanium metal layers from the silicon dioxide passivation layer on the test chip. (b) Cross-sectional micrographs focused near the die-attach interface indicate a cohesive failure within the bulk of the micro-Ag sintered die-attach material. Notably, fractures align parallel to the die in the center and are inclined toward the bulk along the edges.

average smooths out variations and reveals long-term trends. The 50-cycle SMA data at −55 °C [see Fig. 7(a)] indicate a gradual increase in thermal impedance, signifying the degradation of packaging materials due to repeated thermal cycling-induced expansion and contraction. Similarly, the 50-cycle SMA data at 150 °C [see Fig. 7(b)] also suggest comparable indications of package degradation. However, comparing the measurement data at −55 and 150 °C indicates dissimilarities in the $Z_{th}(t)$ trend. Consequently, the 50-cycle SMA data from −55 and 150 °C were plotted together for further analysis, as depicted in Fig. 8.

Two distinct regions, namely, Region-1 and Region-2, can be observed by comparing the area between the curves. In Region-1, the area between the curves shows a nonuniform increasing trend, while in Region-2, the area remains relatively uniform with marginal variations. One possible explanation for such distinct regions can be due to the interplay of multiple failure mechanisms influencing the measurements of $Z_{th}(t)$. Under compression, defects such as delamination and/or in-plane fractures may grow, leading to larger thermal resistances. Conversely, the defects might close during expansion, resulting in lower thermal resistance. Such behavior can induce different thermal responses at −55 and 150 °C, as observed in Fig. 8. This reasoning aligns well with the nonuniform increasing trend observed in Region-1. However, beyond ∼210 cycles (Region-2), the thermal resistances increase uniformly at −55 and 150 °C. This suggests that the dominant failure mechanism in Region-1 may differ from that in Region-2. It is important to note that the interpretation provided here based on the experimental results represents one of several possible explanations. The device was subjected to acoustic imaging [confocal scanning acoustic microscopy (CSAM)] to further investigate and provide quantitative evidence, followed by cross sectioning to gather comprehensive insights.

### B. *Failure Analysis*

CSAM is a highly effective imaging technique used for non-destructive identification of delaminations occurring at buried interfaces within electronic packages [42], [43]. Fig. 9(a) illustrates CSAM imaging obtained from a reference zero-hour sample, where no indications of delaminations were detected. However, a notable contrast emerges when examining the device under test after 436 thermal cycles, as displayed in Fig. 9(b). Delaminations near the overmold-die interface are clearly visible in the image. Although the exact cause of these delaminations remains unknown, we consider them to be a significant contributing factor to the observed increase in thermal impedance during online monitoring. To conduct further analysis, the sample was cross sectioned, and the location of the cross section is indicated in Fig. 9(b).

The tested PQFN package was potted in an epoxy resin and meticulously cross sectioned by polishing at a step of 25 $\mu$m with 150 r/min and 5-N force. After the completion of the polishing procedure, a comprehensive analysis of the sample was conducted. The cross-sectioned sample was examined using an optical microscope and an electron microscope near the overmold-die interface. This analysis aimed to identify the root cause of the delamination observed during CSAM imaging. Upon the close inspection of the cross-sectional images taken in proximity to the overmold-die interface [see Fig. 10(a)], it became evident that the active-metal layers consisting of a 100-nm titanium film on the silicon substrate had experienced delamination from the silicon dioxide passivation layer. This delamination is most likely attributed to residual stresses originating from the manufacturing process or thermomechanical stresses encountered during testing.

Further analysis was conducted on the cross-sectional sample, focusing on the region near the die-attach interface. Fractures within the micro-Ag sinter die-attach material were observed [see Fig. 10(b)]. These fractures exhibited a distinct pattern. The fractures aligned parallel to the die interface at the center, while toward the edges, the fractures were inclined into the bulk of the silver sinter material. Repeated thermomechanical loading conditions caused the die-attach interface to endure cumulative stress damage from continuous expansion and contraction. The fracture behavior exhibited by the micro-Ag pressureless sinter material raises concerns regarding its reliability. Therefore,

TABLE I
ONLINE MONITORING METHODOLOGY PROPOSED IN THIS ARTICLE AGAINST THE INDUSTRY STANDARDS MIL-STD-883E AND JESD51-14

| | **MIL-STD-883E** Thermal Characteristics Testing Method | **JESD51-14** Transient Dual Interface Test Method | **Proposed Methodology** Temperature Dependent Transient-Pulse Test Method |
|---|---|---|---|
| **Purpose** | To determine the Junction-to-Case thermal impedance of a package. | To determine the packaging materials individual layer contribution towards Junction-to-Case thermal impedance. | To determine the package's thermal performance degradation based on temperature-dependent (ambient) transient thermal impedance. |
| **Application / Suitability** | 1. Thermal Characterization.<br>2. Offline monitoring during accelerated lifetime testing. | 1. Thermal Characterization.<br>2. Offline monitoring during accelerated lifetime testing. | 1. Thermal Characterization.<br>2. Online monitoring during accelerated lifetime testing. |
| **Methodology** | 1. Measure the device junction and case (package substrate) temperature at steady-state by external sensors (extrinsic) and/or temperature sensitive device parameters (intrinsic). | 1. Measure the change in the device junction temperature (extrinsic or intrinsic) to compute the resistance – capacitance network.<br>2. Requires a water-cooled heat sink to achieve one-dimensional conductive heat flow path. | 1. Pre-characterization is required based on JESD51-14 test method to identify the transient pulse duration.<br>2. Ambient conditions to be recorded.<br>3. Measure the change in the device junction temperature (intrinsic) by applying a transient heat pulse. |
| **Measurement parameters** | "Steady-state" thermal impedance — $\mathbf{Z_{th\text{-}JC}(t = \infty)}$ | "Transient-state" thermal impedance - $\mathbf{Z_{th\text{-}JC}(t)}$ | "Temperature-dependent transient-state" thermal impedance - $\mathbf{Z_{th}(t,T_{amb})}$ |
| **Advantages** | 1. Easy to implement.<br>2. Less computational effort.<br>3. Precise estimation of Junction-to-case package thermal impedance. | 1. Accurate thermal characterization.<br>2. Enables estimating the individual layer thermal resistance-capacitance network.<br>3. Non-destructive method. | 1. Fast and accurate measurements.<br>2. Online monitoring.<br>3. The presence of multiple failure mechanisms can be identified.<br>4. Advanced data analytics can improve identifying degradation trends.<br>5. Includes the advantages of JESD51-14 test method. |
| **Limitations** | 1. Invasive method.<br>2. Offline monitoring. | 1. Assumes one-dimensional heat flow.<br>2. High signal-to-noise ratio.<br>3. High computational effort.<br>4. Offline monitoring. | 1. Requires further tests and validation.<br>2. Additional refinements are needed for real-life applications.<br>3. Lifetime reliability models are needed to understand the aging mechanisms.<br>4. Includes the limitations of JESD51-14 test method. |

further research on sintering materials is crucial to identify an optimal replacement for high-Pb solders.

Based on the findings from CSAM and cross-sectional analysis, the following conclusions can be drawn, which align in line with the online monitoring measurement results shown in Fig. 8.

1) Two distinct failure mechanisms were identified: 1) delamination of active metal layers from the passivation layer, confirmed by CSAM and cross-sectional analysis; and b) die-attach failure. The micro-Ag pressureless sinter material experienced significant long-term fractures under repeated cyclic loading conditions.
2) The analysis quantifies the experimental results and confirms the presence of multiple failure mechanisms.

### C. Discussion

The online condition monitoring methodology proposed in this study has demonstrated its capability for real-time assessment of the package's health and performance, particularly during accelerated lifetime tests (thermal cycling). Nevertheless, it is essential to acknowledge the practical challenges that accompany this methodology and its applicability in real-life situations.

1) The proposed method has demonstrated its effectiveness in monitoring package thermal performance degradation. However, with a complex interplay of multiple failure mechanisms (see Fig. 8), it remains challenging to decouple the influence solely from the experimental results. Hence, the methodology requires further testing and validation.
2) The thermal resistance of the various packaging layers might shift over time due to aging. Based on the experimental results (see Fig. 7), the relative change in thermal resistance $\Delta Z_{\text{th}}(t, T_{\text{amb}})$ over 436 thermal cycles was $\sim$0.1 K/W, which remains within the thermal resistance boundary highlighted in Fig. 4. Hence, in this particular testing condition, the assumption to consider a 0.1-s heating interval was appropriate. However, this needs to be verified for different package geometries.
3) Temperature significantly affects the semiconductor material's conductivity and carrier mobility. By utilizing the temperature-sensitive parameters, the transient thermal impedance based on a transient pulse can be determined in functional power devices (MOSFETs and IGBTs). Hence, the methodology is not bound to TTCs as demonstrated in this study but can be applied to other temperature-sensitive devices.
4) Additional refinements are required for monitoring the devices online in real-life scenarios. The transient thermal impedance must be measured in real time at a predefined interval without disrupting the system operation. It is also necessary to capture the ambient conditions (temperature, humidity, etc.) while measuring the transient

thermal impedance. The objective is to create a continuous longitudinal dataset spanning the device's lifespan, analyzing its real-time thermal performance in correlation to environmental factors.

5) In this study, moving averages were used to reduce measurement variation and identify the degradation trend. Recent advances in machine learning techniques involving artificial neural networks and convolutional neural networks enhance prognostic monitoring and enable failure mode classification [44], [45].

## IV. Comparison of the Proposed Methodology Against the Industry Standard Test Methods

Despite the aforementioned practical challenges, the proposed methodology provides compelling reasons for its adaptation as an online condition monitoring tool for package reliability assessment. For decades, measuring the package thermal impedance has been a standard practice in the industry, serving as a pivotal metric for evaluating package thermal performance. Established standards, such as MIL-STD-883E [38] and JESD51-14 [34], have provided guidelines for determining the steady-state and transient-state thermal impedance. This research takes a step further in determining the temperature-dependent transient thermal impedance. This innovative approach leverages transient heat pulses to identify the changes in thermal resistance within a specific region of interest. Notably, the transient time is instrumental in delineating the boundary conditions for continuous monitoring. A comprehensive summary is presented herein, comparing the proposed methodology with established industry-standard test methods outlined in MIL-STD-883E and JESD51-14. This comparison spans various facets: purpose, suitability, measurement methodology, metric employed, advantages, and limitations (see Table I).

Besides, several research efforts have been devoted to establishing online condition monitoring based on diverse prognostic device health management measurement methodologies. These measurement methods can be broadly classified as follows: contact (probing) [15], [16] and contactless techniques, thermal and nonthermal (electrical, acoustic [43], [46], etc.) methods, extrinsic methods involving sensors [47], [48], [49], [50], and intrinsic methods (temperature-sensitive parameters [51]), and reliability modeling methods [22], [23]. Notably, most of these measurement techniques necessitate physical or visual access to the device and are intrusive to device operation, limiting their practical applicability in real-life scenarios. In contrast, the methodology proposed in this study monitors the package's thermal performance without requiring physical or visual access. This characteristic underscores its potential as a viable solution for online monitoring in real-life applications.

## V. Conclusion

In response to the increasing demand for reliable power semiconductor devices in field-critical applications, particularly in environments prone to thermal breakdown, an online condition monitoring methodology was introduced in this study. The methodology facilitated the real-time detection of thermal degradation within packaged devices. An accelerated lifetime test (thermal cycling) was conducted in this study to validate the methodology. Based on the changes monitored in the temperature-dependent transient thermal impedance $Z_{\text{th}}(t, T_{\text{amb}})$, we were able to understand the package degradation behavior and identify the presence of multiple failure mechanisms.

The proposed methodology was demonstrated using a TTC integrated into a PQFN package as a test platform. The transient dual-interface test method from JESD51-14 was adapted to determine the optimal transient pulse duration, a critical parameter for acquiring thermal performance data within the region of interest. During TMCL testing, an increase in $Z_{\text{th}}(t)$ was observed at different ambient temperatures ($T_{\text{amb}}$), indicating thermal degradation due to cyclic loading. Disparities in measurements at different temperature ambients hinted at multiple failure mechanisms, later confirmed through CSAM analysis and cross-sectional inspection.

The proposed methodology has proven effective for online monitoring and offers quantitative insights into the degradation behavior. In this article, we further discussed the practical challenges associated with the methodology and highlighted distinctions between the proposed and industry-standard methods. The applicability of the online monitoring methodology in real-life applications requires additional refinements, which were briefly discussed. The experiments were demonstrated with TTCs in a PQFN package subjected to thermal cycling. However, the methodology can also be applied to functional power semiconductor devices and other accelerated aging processes. The significance of the proposed method lies in the early detection of signs of failure or degradation, thereby preventing unexpected system downtime and additional costs.

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