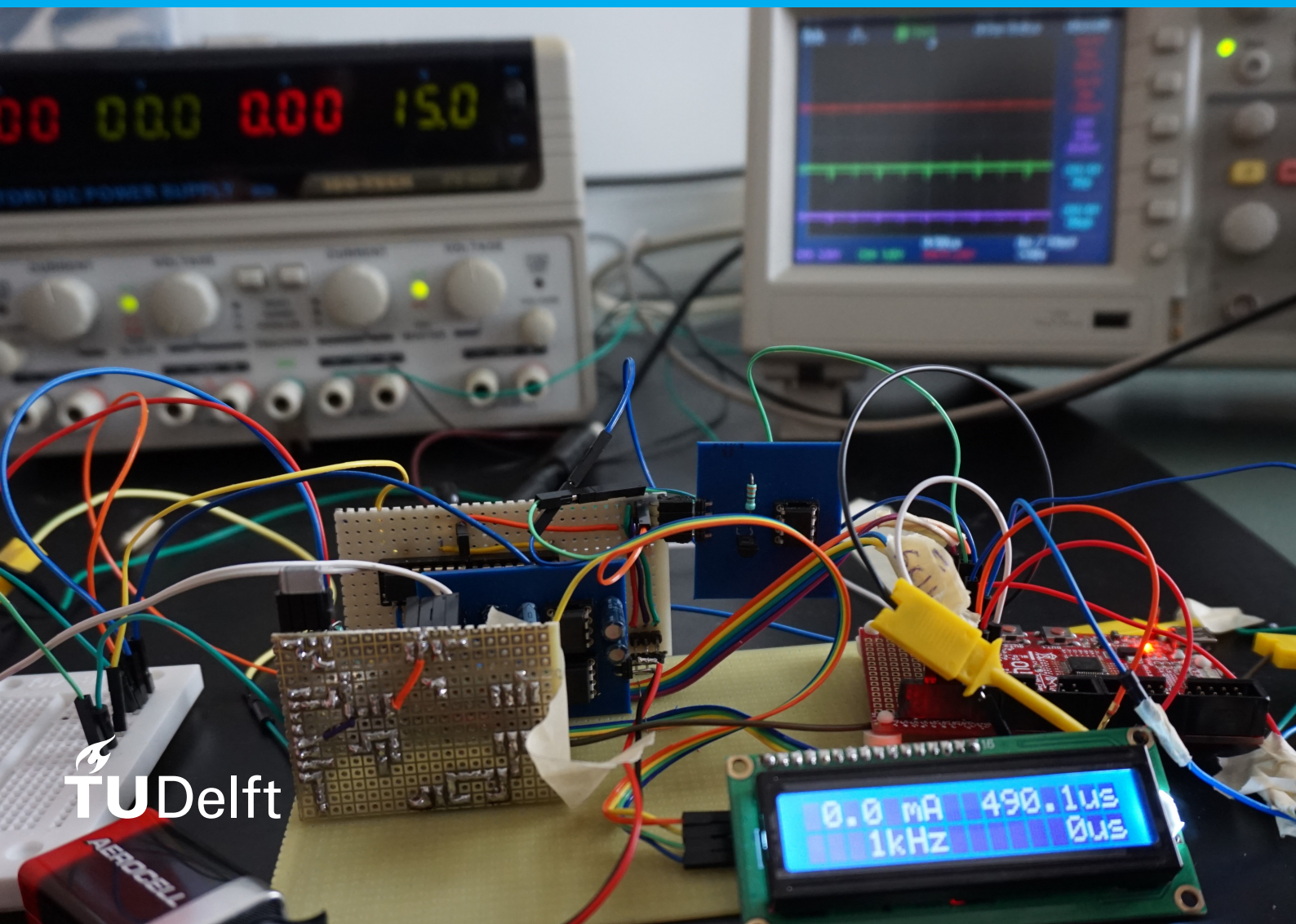
Bachelor Thesis

Control & Interface module

for a High Frequency Arbitrary Waveform Neural Stimulator

M.C.W. Engelen & P.C. van den Heuvel

REValUE Project



TU Delft

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Control & Interface module
for a High Frequency Arbitrary Waveform Neural Stimulator

by

M.C.W. Engelen & P.C. van den Heuvel

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FACULTY OF ELECTRICAL ENGINEERING, MATHEMATICS
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An electronic version of this thesis is available at `http://repository.tudelft.nl/`.

TU Delft

Abstract

In the REstore Voiding Urinary rEtention (REValUE) project, a high frequency stimulator is designed that should be able to determine the optimal parameters to block the urethral sphincter. In this report the design of the control, interface, current source and electrode switching circuit of the device is explained – the other parts are explained in the reports of the waveform and safety subgroup [1, 2]. The 2,304 cm^3 high frequency stimulator has an adjustable frequency (0-15 kHz with 1 kHz step-size), amplitude (0-10 mA with 0.1 mA step-size), pulse width (0-500 μs with 1 μs step-size) and interphase delay (0-1000 μs with 2 μs step-size). Two 4-electrode leads of can be connected in mono- and bipolar configuration. Integration of an Liquid-Crystal Display (LCD) screen with Inter-Integrated Circuit messaging bus (I^2C) on the NXP LPC1343 shows the user the settings of the stimulation parameters.The current source is designed based on a cascode current mirror, implemented with PNP transistors, using active feedback to control the current. The topology is based on a discrete component implementation.

Preface

A couple of months ago the project started by us walking up to professor Serdijn with the question if he had a project on which we could do our bachelor thesis. He proposed the REValUE project and all the team-members of the 3 subgroups were very enthusiastic for the project. From that point on, research was done on the problem in order to better understand it from both a medical as well as electrical point of view. More than a month before the project actually begun, we started by getting familiar with the problem and trying to understand how we can achieve the project goal.

In the preparations towards the project, but most of all during the project, we have had help from multiple people which we would like to thank.

First of all, we want to speak our gratitude towards professor Wouter Serdijn for being a very good supervisor. Wouter is a supervisor which is always concerned about the student perspective by asking questions like: is it instructive enough for the students? Do they have necessary facilities for doing the project? how should you deal with a client as a designer? Furthermore, Wouter has always been open to help us and think about solutions for the problems we have had.

We also want to thank Bertil Blok who came up with the project. As our client supervisor he was very actively involved and he freed up a lot of time to help us with the project. His passion to get a better solution for the patients has lead to this research and our project.

Furthermore, we want to thank Xavier van Rijnsoever for giving advice on which some of the design choices are based. He always helped us to think critically on what components we should choose for our design. We also want to thank Jan Groen for helping us understand the demands of the device from the hospital operator side. Jan Groen was also always willing to help us very quickly for questions such as feedback on our interface design.

We are also grateful for the help of and collaboration with Gerard Baquer, a master student which was working on a similar topic. He has helped us understand the project with the literature he had already found. His research on the biomedical aspect of neurostimulation at the bladder area has helped us with the electrical design.We also want to speak our gratitude to Ali Kaichouhi, technician at the bioelectronics department and Marion, the secretary of the department.

Lastly, we would like to thank the other subgroups for the collaboration and the team spirit of the whole group. Despite the fact that we are graded for the project in couples, we have never experienced the idea that people were doing the project with two group members. Everyone was always available to help the other subgroups on the problems they faced.

The project has been very interesting for all of us because we learned how we can design a device which is state-of-the-art in just a few weeks. Our technical knowledge combined with real life problems people face brings us perspective on what we can do with the knowledge from our bachelor in Electrical Engineering.

Max Engelen en Philip van den Heuvel
Delft, June 2018

Contents

1 | Introduction

This project is done in cooperation with two other groups [1, 2], all groups concern the same problem but work on different sub modules for this project. Therefore, the project introduction, problem definition and project objective found in the theses are the same.

1.1. Introduction to the REValUE Project

Millions of people have difficulty in emptying their urinary bladder [3]. Well-known causes are *spinal-cord injury* (SCI) and *multiple sclerosis* (MS), but many more non-neurological patients suffer from similar problems without an obvious cause. Normally, the urethral sphincter is continuously contracted and only a few times per day relaxed during voiding. This relaxation is controlled by a switch in the brainstem [4]. When the brainstem switch is not activated, there is no relaxation of the sphincter and, thus, no voiding and the sphincter remains contracted and closed. Patients in retention cannot void because they are unable to activate the brainstem switch.

1.1.1. Problem Definition

The most common treatment is to mechanically empty the bladder with intermittent self catheterization or an indwelling catheter as there is no treatment to restore the voiding function [5]. Using a catheter results in infections, pain and excessive healthcare costs [6]. Electrical stimulation to improve bladder function has been utilized with varying success [7]. The Bindley system has been implanted which uses sacral root stimulation where the roots are selectively cut. This method is irreversible and causes total absence of erections. The rhizotomy and implantation take more than five hours of surgery and both urologists and neurosurgeons are necessary for the operation.

Sacral nerve stimulation is an often used technique for bladder voiding in patients without SCI [8]. This method only needs percutaneous access to the nerves, significant reducing the surgery time. The downside of this method is that the urethra is still closed, resulting in a high bladder pressure and an increased chance that urine flows back into the kidneys.

1.1.2. Project Objective

In this project, a high frequency stimulator is developed. The high frequency signal cancels the blocking of the urethral sphincter. A study has shown effective emptying of the bladder of cats by blocking the pudendal nerves [9]. Besides high frequency stimulation, the project is aimed to develop a low frequency stimulator as well, to stimulate the ventral roots, causing bladder contraction.

For this goal, a Bachelor Graduation Project group from Electrical Engineering was formed. The objective of this group was to develop a high frequency, arbitrary-waveform, neural stimulation device that offers efficacious, yet safe, stimulation of the pudendal nerves. This can be used to focus on relaxing the urethral sphincter by reversible, bilateral, high frequency blocking of the pudendal nerves to enable voiding. After emptying the urinary bladder, the blockage is stopped and the sphincter resumes its normal closure function during continence.

This group of six people is divided in teams of two. The first team focuses on the interface and the control of the device. The second team develops the waveform generator circuit and a third team makes the safety system of the waveform generator [1, 2].

1.1.3. State-of-the-art Arbitrary Waveform Neural Stimulator Analysis

The state of the art neural stimulators are integrated circuits because they have restrictions on the power and the size of the device. Most arbitrary waveform generators are however made with discrete components [10]. Furthermore, most state-of-the-art neural stimulators have been made for testing and implementation

on small animals and not for humans [10, 11]. When there are no power and size limitations the arbitrary waveform generators are often implemented using a current controlled stimulation [10].

The choice between current or voltage controlled stimulation circuit schemes are however not necessarily trivial, often a trade-off is made for the specific design. In state-of-the-art technology solutions such as charge steered stimulators based on switched-capacitor techniques are also proposed. Charge steered stimulators combine the power efficiency of voltage-controlled simulators and safety and controllability of current-controlled stimulator in a simplified design to decrease the size and power requirements of the stimulator [12].

Most state-of-the-art stimulators are based on low frequency stimulation (1-100 Hz). Low frequency stimulation can produce neural response, while high frequency stimulation results the blockage of these neural responses [13]. High frequency stimulators do exist for other applications than the pudendal nerve stimulation which this project is focussed on [14]. The stimulator designed will stimulate at both high and low frequency, which does not exist currently.

Neurostimulators used in urology
At the start of the research, the Medtronic 3625 Test Stimulator has been used as arbitrary urinary neurostimulation in the hospital. The Test Stimulator is a voltage controlled device and has the following characteristics: it has an amplitude range 0-10 V with a ±0.5V accuracy, a frequency between 5 and 1400 Hz and a variable pulse width between 50-1000 μs [15]. The currently used stimulator is the Medtronic Synergy 7427 [16].

1.2. Thesis outline

After this section, a list of requirements for the interface and control module will be presented. The complete system overview of the device will be given to bring perspective of all the modules. The (inter)connection of the relevant modules will be explained.

From this overview, three chapters are dedicated to the process of design, simulation (if applicable), prototyping and a discussion for the interface (chapter 4), control (chapter 5) and current source (chapter 6). In the interface chapter the design of the electrode switches module will be discussed. In the control chapter an overview of the complete control integration on the LPC1343 microcontroller will be shown and our control submodules will be explained in-depth. The different designs leading to the final current source design are explained in chapter 6. The results will be discussed in every separate chapter. Lastly, in chapter 7 the project will be concluded and recommendations will be given for future research.

All the programming files and spice simulations used for this project are not included in this thesis report but are available on request. More information on this can be found in appendix A.1.

2 | Program of requirements

2.1. General requirements of the project

The goal of the REValUE project is to deliver a testing device which can determine the optimal parameters for urinary stimulation. The program of requirements is divided into two parts. First, the general requirements are presented, which hold for the entire testing device. Afterwards, in section 2.2, the requirements for the control and interface part are presented. The following general requirements have been set for the project:

- The device should have 2 identical connections for 2 extension cables which are connected to a lead. This lead has an array with 4 electrodes (the lead used is Medtronic Model 388928).
- The leads must be connected with an extension cable which should fit the connectors of the device.
- The device must be able to stimulate on all possible terminals of the lead.
- The device must support monopolar and bipolar stimulation.
- The device must operate outside the sterile field around the patient.
- The device must not cost more than €5.000,-.
- The device must not be larger than $0.5 \times 0.5 \times 0.3$ meters (length x width x height).
- The device must not weigh more than 10 kg.
- The components of the device must ensure a lifetime of at least 6 months.
- The device must be able to operate between 10° and 40° C.
- The internal temperature of the device must be kept in a range where the device is still fully functioning (so where the device meets all specified requirements).
- The device must not create sounds which exceed 40 dB [17].
- The device must be made from commercial off-the-shelf components.

Output Quantity
A current waveform has to be available at the output. This is done either by the waveform generator or converted from a voltage waveform by a separate section later in the design.

Primary requirement to apply injected charge
The generated waveform must be current driven. The device must independently control the current through two (implantable) leads with both four electrodes. The current through all electrodes must be controlled independently in two different channels.

Secondary requirement to apply injected charge
Besides a current driven waveform, the device must be able to generate a voltage driven waveform.

2.2. Requirements for control and interface

2.2.1. Functional Requirements

The functional requirements define the purpose of the control system and the connected interface. The requirements are split up into primary and secondary requirements. The primary requirements are the highest priority. When all primary goals are met, the secondary goals can be taken into account.

Primary functional requirements

Implementation of the hardware
The control of the system will be implemented using a microcontroller, Raspberry Pi or FPGA. The interface must be connected to the control system and show the main settings of the device.

Main settings changeable by user
The user must be able to turn the device on/off with a button. The interface must show the user the specified settings of the device. Furthermore, the user must be able to change the following settings – in order to select the desired type of stimulation:

- Adjustable frequency of the applied waveform.
- Adjustable pulse width of the waveform.
- Adjustable interphase delay of the waveform.
- Adjustable amplitude of the waveform.
- Selection between monopolar or bipolar stimulation.
- Selection between which (implantable) leads are stimulated with which frequency (high or low frequency) of the two channels for all four electrodes.

Secondary functional requirements

Additional settings changeable by user
Additional settings which the user should be able to change, if the settings will be implemented by the waveform subgroup, are:

- Selection between the possible types of waveforms.
- Selection between voltage or current driven stimulation.
- Selection between monophasic or biphasic stimulation.

Visual interface
The device needs to indicate settings to the user. The type of waveform needs to be indicated on the interface of the device and the actual values of the adjustable parameters should be visible to the user. The user friendliness needs to be considered during the development of the device.

2.2.2. System requirements

System requirements are specific technical requirements that describe the functioning and performance of the control system and connected interface. The requirements are split up into primary and secondary requirements. The primary requirements are the highest priority. When all primary goals are met, the secondary goals can be taken into account.

Primary system requirements

Frequency requirements
The output frequency range is between 1 kHz and 15 kHz and it should be possible to adjust this frequency with steps of 1 kHz.

Amplitude requirements
The amplitude requirements are based on current driven stimulation, where the amplitude of the current should be adjustable between 0 to 10 mA. The user has to be able to sweep through this amplitude range.

Safety requirements
The feedback of the safety module should be graphically shown to the user, by the use of for example a LED.

Secondary system requirements

Low frequency stimulation requirements
The user must be able to select on which electrodes a low frequency simulation between 5 and 20 Hz with increments of 1 Hz, is applied. The user also should be able to change the duty cycle and the inter-pulse delay of the waveform.

Voltage driven stimulation
Changing from current to voltage driven stimulation must be possible on the device. The amplitude of the voltage should be adjustable between 0 to 10 V.

3 | System overview

In the design process of the arbitrary waveform generator, the complete system has been divided in many different modules which were designed by different subgroups. In Figure 3.1 the complete system overview is shown with all the different modules. The orange modules are the ones which are covered in this report, the blue and green modules are described in the reports of the waveform and safety subgroup respectively [1, 2]. The white module is, namely the electrodes module, is not covered in the report since they have not designed by us, but are provided through an external party.

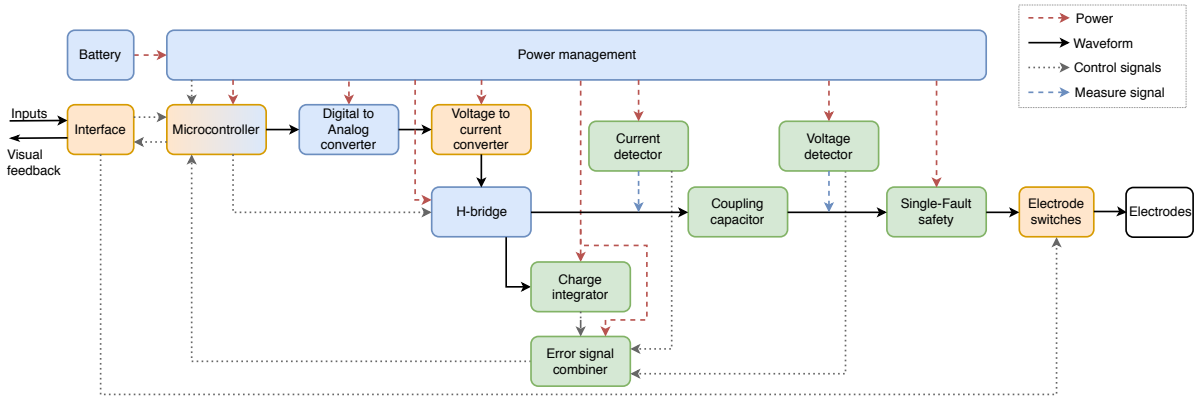


Figure 3.1: The complete system overview of the arbitrary waveform generator. The orange modules are designed by the Interface & Control subgroup, the blue modules are designed by the Waveform subgroup and the green modules are designed by the Safety subgroup and the white module (electrodes) are provided via a external party. The inputs are the user inputs on the interface and the visual feedback the feedback given to the user. Four type of connections can be seen in the system overview: delivering power, generation of the stimulated waveform, control signals to communicate and measurements on the waveform signal.

In chapter 4 the design and implementation of the Interface and Electrode switches modules are described. In chapter 5 the design and implementation of the microcontroller module are described. In chapter 6 the design, stimulations and results of the DC-DC converter and regulator and the voltage to current converter modules – also named the current source – are described.

3.1. Interfaces between the relevant modules

The relevant modules – namely the modules which are connected to the Interface & Control modules – have a signal, power or control signal which is important for the Interface & Control modules. The type of interface with the relevant modules is shortly elaborated:

Most of the the modules need a direct power supply to function, this is done by the power management module. The design of the power management module is discussed in the waveform groups report [1]. The microcontroller module requires a 3.3 V supply and the voltage to current converter requires a 15 V supply. The control signal connection from interface to microcontroller is the users input on the waveform parameters on the interface. The control signal back from microcontroller to interface are the graphically showed feedback and parameter settings to the user, implemented using four Light-Emitting Diodes (LEDs) and a LCD screen. The error signal combiner module gives the microcontroller a logic control signal to pass on the status of the device. The connection from the microcontroller to the Digital-to-Analog Converter (DAC) is the generated 10-bit signal for the waveform parameters obtained from the user input. The voltage to current converter, or often named the current source, receives a voltage signal from the DAC, and converts this into a current. The current signal is then send to the H-Bridge. The H-Bridge is a switching circuit that can redirect the current through a load, how this is done can be found in the report of the waveform group [1]. Lastly, the electrode switches connect the stimulated signal to the correct electrodes according to the users input.

4 | Interface

In this chapter the design and implementation of the interface and switching circuit is described. The design steps for the interface are described in section 4.1 and for the switching circuit in section 4.2.

In the interface design phase of the arbitrary waveform generator, a design with both a high and low frequency stimulation was considered. During the prototype phase, the choice was made to solely implement the high frequency part of the arbitrary waveform generator and not the low frequency part – which was a secondary requirement as described in the program of requirements in chapter 2. This choice was made because of the limited time available in the bachelor thesis project. Especially for the Control & Interface module, a lot of the systems can be implemented in a very similar way with some minor changes for the low frequency part, such as changing the units from Hz to KHz.

4.1. Design of the interface module

Demands on the design

The interface is a very important aspect of the arbitrary waveform generator. It should both indicate which parameters are used as well as letting the user adjust the waveform using these parameters. There should however be limitations on the settings such that the user is only able to adjust the parameters to the extent that we can ensure safe stimulation. In order to achieve a well-designed interface, the demands can be summarized by the following guidelines [18]:

- consistency, standards and universal usability
- visibility of system status
- informative feedback
- flexibility and efficiency of use
- make users feel in control
- recognition rather than recall
- prevent errors
- help users recognize, diagnose, and recover from errors

Road to the confirmation of the demands

In the user-discovery phase users can confirm if the design has the characteristics described by these guidelines. This phase is very important for the design of the interface and the following tools can be used to find the demands of the user: direct observation, case studies, surveys and personas [19]. Direct observation – namely interviewing the user(s) and observing the response of the user(s) to the design – was done with the users (the doctors that operates it) of our device in order to create a device which suits the users' demands and is considered intuitively.

Furthermore, case studies using personas – a detailed study into extreme user situations and conditions with fictional personas and asking questions like: "What would X do?" – were conducted in order to make sure our interface is also secure for operators who are not familiar with what the arbitrary waveform generator does. Survey's were not considered because of the limited amount of people who will use our device.

Creating improved consistency for the user

Inspiration for the interface was taken from a frequently used external arbitrary waveform generator in the hospital in order to improve intuitivity and consistency for the user. The Medtronic 3625 Test Stimulator described in subsection 1.1.3 and also shown in Figure 4.1 was a frequently used device in the hospital for testing neurostimulation parameters [15]. The Medtronic 3625 Test Stimulator interface is divided into external and

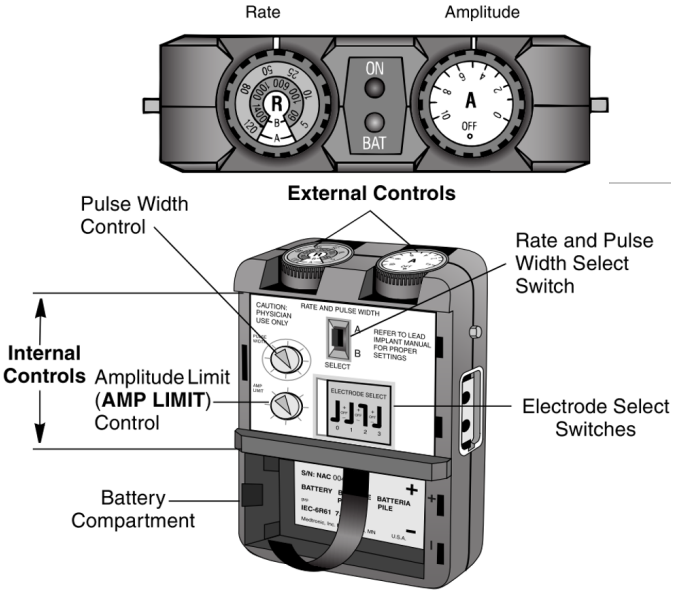


Figure 4.1: Image obtain from the manual [15]. The internal and external controls and the battery component of the Medtronic 3625 Test Stimulator [15]. The device has a LED light for when the battery is low and when the device is turned on. The external controls consist of the rate and pulse width control and the amplitude control. The internal controls may only be adjusted when the stimulator is turned off using the amplitude control. The internal controls consist of the amplitude limit control, the rate and pulse width select switch and the electrode select switches. The cable connected to the electrodes can be connected to the side of the device.

internal controls. The external controls can be adjusted during stimulation and the internal controls should only be adjusted when the stimulation is turned off [15].

According to operators, the Medtronic 3625 Test Stimulator had a very intuitive and simple design. But, the operator has to have knowledge on what settings are safe and which are not, because unsafe or undesired settings can be selected. In our design the extreme user situations will also be taken into account, in order to reach the highest possible safety for the patient.

Implementing the other design demands
An accurate readout of the settings – with direct feedback on the adjustment of the parameters – is important for our device since the device will be used to determine the optimal parameters for stimulation. Therefore, a LCD screen has been integrated to show the settings accurately to the user. The device will not only show the user when the device is turned on and when the battery is low, but also when a safety problem occurs. This has been done in order to let the user understand when certain settings will not be supported. Our waveform will not only be adjustable in amplitude and pulse width but also frequency and interphase delay. Therefore, there are more parameters which can be controlled during stimulation or when the device is turned on.

Compared to the Medtronic 3625, the design for the interface integration of the switching array was done with rotary switches to select the electrode for the stimulation (+ electrode) and the return of signal (- electrode). The electrode selection switching system is different than the Medtronic 3625 Test Stimulator for reasons explained in section 4.2. In the first design of the interface – which met all the primary and secondary requirements – the electrode lead selection also needed to be extended with buttons to select either high or low frequency on every electrode. This design did not achieve the goals of a well-designed interface.

The final design of the interface

In the first design, seen in Figure 4.2, all the primary and the secondary requirements were also incorporated.

For high frequencies, no switch to monophasic stimulation was integrated. This choice was made because monophasic monopolar stimulation was found to lead to serious damage [20].

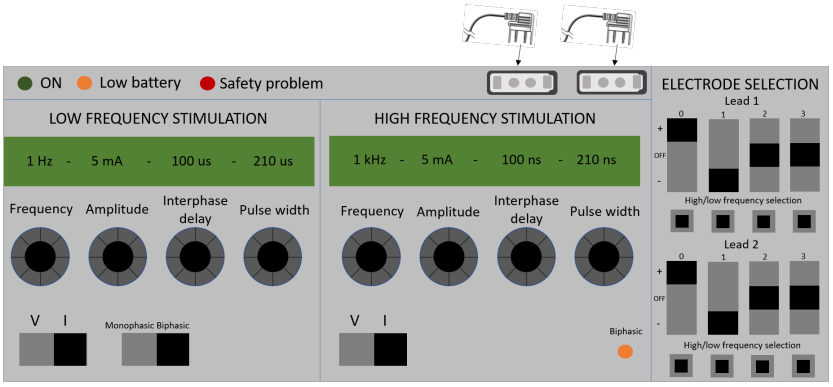


Figure 4.2: The first design of the interface which was able to meet all the primary and secondary requirements. The interface is separated in a low frequency and high frequency stimulation interface where the settings are visualized and can be adjusted. A separate electrode selection part for 2 leads where both high and low frequency can be selected were integrated.

In the final interface design, seen in Figure 4.3, the LCD screen shows the parameters on two rows because a reasonable sized implementation can show only 16 characters on one row. The electrode high or low frequency signal can be put on both or either one of the leads, using the buttons. Solely current driven and biphasic waveforms could be selected in this interface. These were primary requirements and are incorporated in the final waveform [1]. Lastly, the parameter limit LED was added, which was not a requirement but a logical implementation to give users informative feedback and help users recognize errors, while not limiting the control or flexibility of the user in the settings of the waveform. More explanation on the functionality of the modules of the design is given in the control implementation, described in section 5.2.

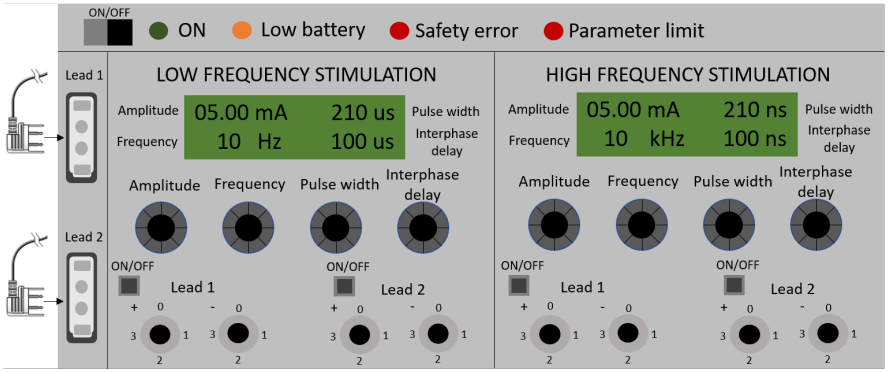


Figure 4.3: The final design of the interface when all options are integrated. The on/off switch will turn the device on. Four LEDs are added to show when the device is stimulating, the battery is low, a safety error has been detected and a stimulation parameter has been limited. The two LCDs show the stimulation parameters and the rotary meters let the user adjust the stimulation parameters. The electrode/lead selection is integrated by rotary switches and on-off buttons to connect to the right leads. Two leads can be plugged into the device for connecting electrodes.

4.2. Design of the electrode switches module

The electrode switches or switching array is the integration of the electrode selection part of the interface. Since the system has a multiple channel with a multiple electrode system, the user has more flexibility. But in order to prevent errors and unsafe situations, the switching circuit is designed such that undesired configurations are impossible. Therefore, as already described in section 4.1, the choice has been made to deviate from the Medtronic 3625 Test Stimulator switching circuit because the user should only be able to select one electrode for stimulation (+) and only one electrode as return electrode (-). Unused electrodes are left floating and not connected to ground, similar to the system proposed in figure 6.10 of *Design of efficient and safe neural stimulators* [11].

Monopolar stimulation
The switching circuit has to be able to make both monopolar and bipolar stimulation possible. Monopolar stimulation uses the ground pad as the return electrode, while bipolar uses one of the other electrodes on the lead as the return electrode. When switching to monopolar stimulation the switches need to be changed to position 0 and 3 and the return electrode (-) needs to be connected to the ground pad.

The Medtronic 3625 Test Stimulator can be connected to a bipolar cable (such as the Alligator Clip Screening Cable) or a quadripolar cable (such as the Twist-Lock Screening Cable). The bipolar connection cable requires a certain selection of the electrode selection switches (connection is made when position 0 and 3 are selected), where the quadripolar cable can select all the four electrodes as stimulating or returning electrodes. Thus a bipolar cable can be used for monopolar simulation when the electrode switches of a lead are placed in position 0 and 3. In general bipolar stimulation is more focused, on a specific area within the tissue, than monopolar stimulation and bipolar stimulation reduces the size of the artifact [21], but both stimulation types seem to be effective. For high frequencies, the bipolar configuration was much more efficacious in some cases [22].

High and low frequency stimulation
When low frequency stimulation was implemented, the switching circuit had to be able to select both high frequency and low frequency on the same lead (e.g. stimulating with low frequency on electrode 0 and 1 and high frequency on electrode 2 and 3). This was desired in order to block the urethral sphincter with high frequency as well as using contract the ventral roots with low frequency stimulation.
With the interface proposed in Figure 4.3, a circuit should be designed to check if the high and low frequency signals (+) or return signals (-) are connected to the same electrodes. Mainly because we do not know the effect of putting both signals on the same electrodes, this situation should be prevented.

4.3. Prototype implementation interface module

Since the implemented interface concerns a high frequency stimulator, the interface implementation shown in Figure 4.4 deviates from the final design of the interface, which is shown in Figure 4.3.

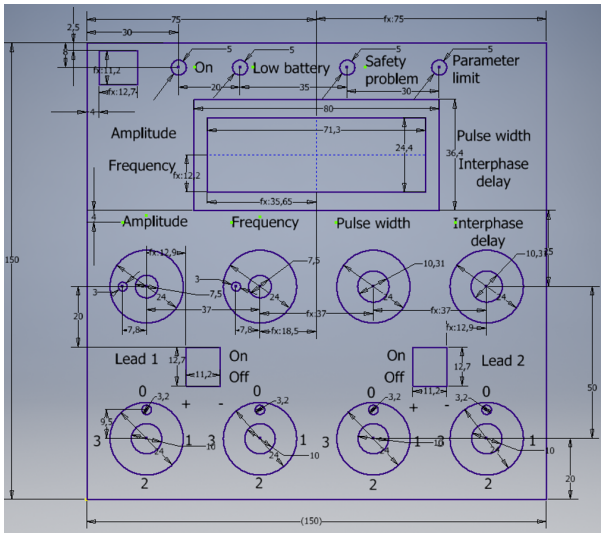


Figure 4.4: The front view of the implemented interface of the arbitrary waveform generator. The dimensions of the interface and the components are given in millimeters. The four LED lamps are the HLMP-1503 (green), HLMP-1401 (yellow) and HLMP-1503 (green) diffused LED lamps. The implemented On-Off switches are the 1201M2S3CQE2 On-On slide switch with double-pole double-throw. The implemented LCD screen is the 16 × 2 HD44780 LCD screen with I^2C module. The implemented potentiometers are two P160KNP-0EC15B25K 1 turn 25kΩ and two Bourns 3590S-2-203L 10 turns 20kΩ rotary potentiometers. The implemented rotary switches are the CK1031 3-pole 4-position rotary switch.

The four integrated LED lamps show the user when the stimulation is on, has a low battery voltage or a safety problem. The battery voltage light will start to burn when the battery is at 7.5 V and the device will turn off at 7 V [1]. The implementation of this is further discussed in section 5.2. The safety error light will indicate

to the user when the device was turned off due to a safety issue from the error signal combiner [2]. The parameter limit LED lamp will show the user when one or multiple waveform parameter values are limited, as further elaborated in the control implementation in section 5.2. The selected LCD screen is the 16 × 2 HD44780 LCD screen. It will turn on when the device is turned on, whereas the ON LED lamp is only turned on when the device is stimulating. More about how the LCD screen is integrated, can be found in section 5.2. The LCD screen will visualize the stimulation parameters and will give direct feedback – by changing the value on the screen – if the user adjusts the position of the potentiometers.

The implemented potentiometers for the amplitude, frequency are simple 1 turn rotary switches. The implemented potentiometers for the pulse width and interphase delay are 10 turn rotary potentiometers which were chosen because accuracy and high reliability are of major concern. Cheaper, less accurate and less reliable 1 turn potentiometers did not have a steady value which lead to a less accurate read-out and significant changing parameters of the waveform, which was considered undesired. The amplitude and frequency suffered less from this unstability. This is because the range of these parameters is smaller, with 0-15kHz with 1 kHz increment and the 0-10mA with 0.1mA increment.

The chosen 1201M2S3CQE2 On-On slide switches were selected because the switch was sturdy. The chosen CK1031 rotary switches were selected because they were able to switch between 4 different positions. The cable connectors of the device are not visible on the front view, since they are implemented on the side of the case. The Medtronic extension cable which will be connected to the electrodes, fits the connectors of our device. The selection of electrodes have been tested to work with the extension cable and the rotary switches. More on the implementation of the rotary switches is described in section 4.4.

The selected 1554SGY ABS plastic case of the device has rail mounting tabs and is well-suited for mounting printed circuit boards. The size of the case is 16 cm × 16 cm × 9 cm and the front design shown in Figure 4.4 is only 15 cm which gave a margin of 5 mm at the sides. The size of the device therefore easily meets the general requirement on the size of below 50 × 50 × 30 cm.

4.4. Prototype implementation electrode switches module

The electrode selection was, as explained in section 4.3, implemented with 4 positions rotary switches. The electrode switching scheme with the designed functionality is given for both monopolar and bipolar stimulation in Figure 4.5. As already explained in section 4.2, electrode 0 and 3 need to be selected for the stimulating (+) and returning electrode (-) when using monopolar stimulation. Either one of the options will lead to the circuit of Figure 4.5b. Selecting two the same electrodes as stimulating and returning electrode – by putting the two rotary switches in the same position – will just short the circuit and cause no stimulation.

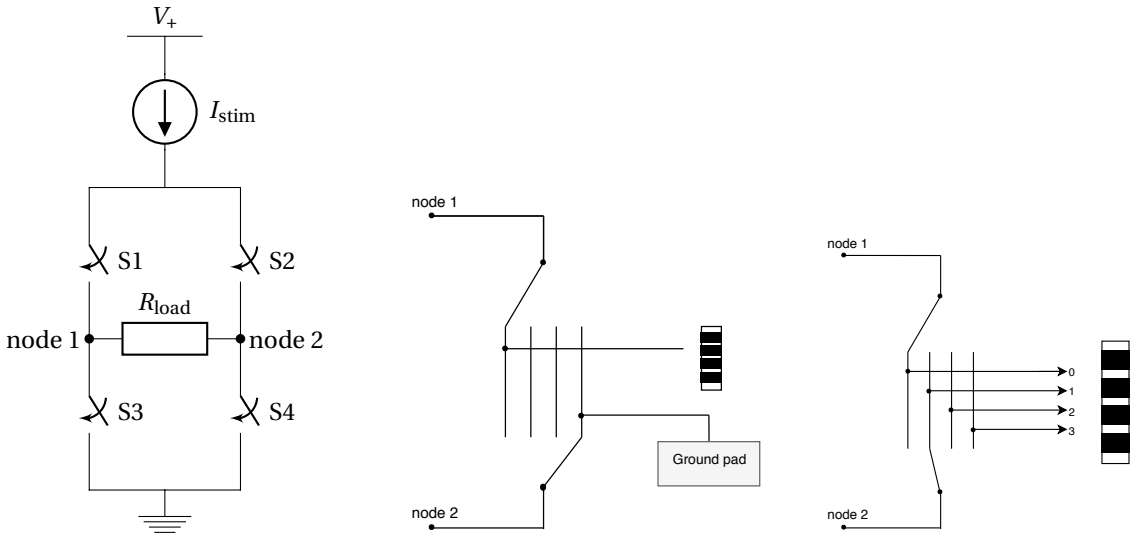
The operator should never adjust the selection of the electrodes while stimulating. Switching behaviour will become present in the stimulated waveform of which the effects on the tissue are not investigated.

4.5. Discussion on the interface implementation

The final interface was successfully integrated in the prototype and worked as designed. The design can be evaluated against the demands for a well designed interface of section 4.1. The best way to evaluate the design would be by interviewing the user. However, when reflecting on the design using the criteria for well-designed interfaces:

The design was based upon the standards of currently used test simulators in order to improve consistency. The visibility of the system status is done by implementing the LEDs like for on, low battery and safety error. Similarly, the informative feedback to the user is done with the LCD screen and LEDs. The safety status would be even more informative if the specific error can be shown to the user. The device was designed for flexibility with a lot of different possible types of stimulations. The device would be more flexible if both high and low frequency would have been implemented. The efficiency of use can be improved by having less turns for the potentiometers for the pulse width and interphase delay. Especially on 15 kHz, less than 10% of the range will be used for both the pulse width and interphase delay. The users are in control for all the settings unless these are not safe or possible, then they are informed accordingly using the LEDs. The interface is

always the same which makes the recognition very easy. The interface prevents errors from the users by limiting the options which are possible. Using the LEDs the user is also able to recognize, diagnose and recover from errors.



(a) Basic H-bridge design [1]

(b) The monopolar stimulation setup of the switching circuit.

(c) The bipolar stimulation setup of the switching circuit.

Figure 4.5: The switching circuit as direct load of the H-bridge of the waveform subgroup. The stimulating electrode is connected via the 4 position rotary switch at node 1 and the return electrode is connected via the 4 position rotary switch at node 2. The second figure shows the operation for monopolar stimulation and the third figure shows the operation for bipolar stimulation using electrode 0 and 1.

4.6. Discussion on the switching circuit implementation

The switching circuit is quite simple but works effective. In this design the user is able to switch the lead selection during stimulation, which could have been prevented if the switching circuit was implemented on a microcontroller. Therefore, the user is now able to possibly introduce errors if he changes the electrodes during stimulation.

The switching circuit for combining high and low frequency would have been more advanced. The switching circuit implemented on a microcontroller could have also prevented simulating with both high and low frequency on the same lead. If the low frequency part was also integrated and the switching circuit was not implemented on the microcontroller, there should have been some logic module implemented which prevents this – similar like the error signal combiner of the safety subgroup [2].

5 | Control

5.1. Design of the microcontroller module

The control system will be integrated on a microcontroller – not only for the internal control signals but also for the generation of the waveform. After analyzing and considering multiple options like Arduino, Raspberry Pi, FPGA, the NXP LPC1343 microcontroller was selected. The LPC1343 met the following selection criteria and specifications:

- It has good documentation [23].
- It has enough availability of communication protocols and timers for all control.
- It is able to control a DAC and had internally integrated components such as an Analog-to-Digital Converter (ADC) and an Inter-Integrated Circuit messaging bus (I^2C) adapter.

According to the system overview – shown in Figure 3.1 – the microcontroller gets control input from the error signal combiner, interface and battery. Similarly, the microcontroller gives output to the DAC, control output to the interface and the H-bridge switches. The voltage regulators will give a supply voltage of 3.3V from the 9V battery to the microcontroller. The inputs are the potentiometers which are transformed into a 10-bit value using the integrated analog-to-digital converters (ADCs) of the microcontroller. The visual feedback of the interface is given by the LEDs and the 16 × 2 LCD screen which is addressed using I^2C communication. The complete overview of the microcontroller module is shown in Figure 5.1.

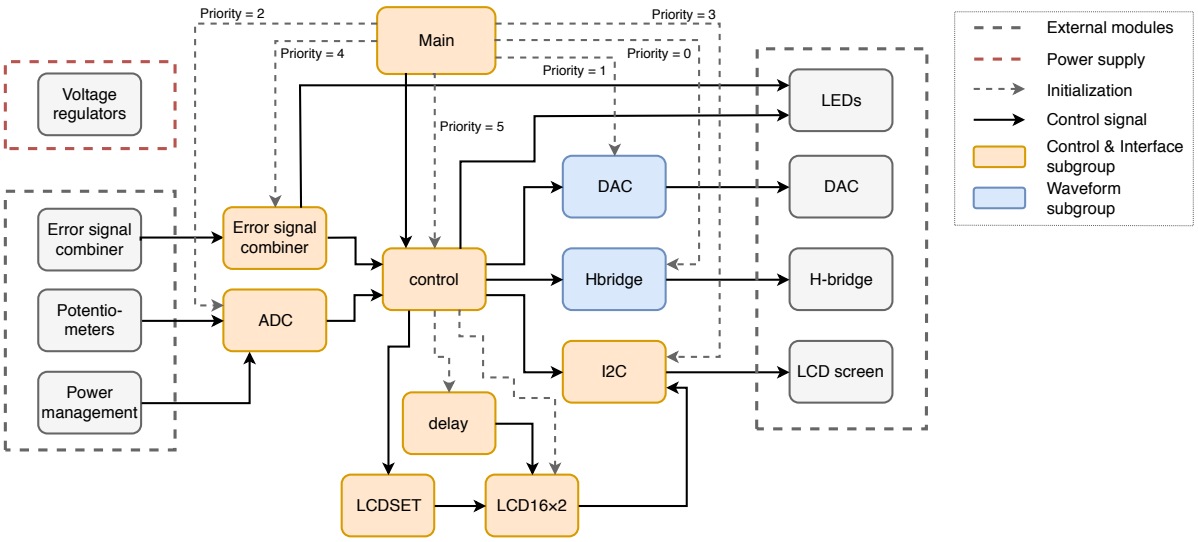


Figure 5.1: The microcontroller functionality divided into different submodules. The implementation of the Control & Interface subgroup modules are discussed in section 5.2 and the description of the Waveform subgroup modules implementation can be found in the Waveform report [1]. The gray modules are physical modules which are the inputs/outputs of the microcontroller module – which are in accordance with the system overview in Figure 3.1 – where the potentiometers, LEDs and LCD submodules represent the Interface module. The two types of signals are shown in the microcontroller functionality scheme are initialization signals and control signals. The voltage regulators give the 3.3V supply voltage to the microcontroller.

The main code will initialize and set priorities to the interrupts of the different modules. The H-bridge timer has the highest priority (priority = 0) because this submodule will create the timing of the actual waveform using a clock signal which should not be interrupted. Similarly, the DAC submodule is also dependent on a communication protocol that relies on a clock, this will not work properly if this clock is interrupted, and therefore gets the second highest priority (priority = 1).

The ADC submodule has the third highest priority (priority = 2) because the values from the ADC sub module are used to set the right parameters for the waveform. Hereafter, the I^2C timers have the highest priority (priority = 3) because this submodule will communicate the correct parameters of the waveform to the user and the H-bridge.

The error signal combiner timer has the second lowest priority (priority = 4) this submodule will internally communicate the safety error and set a LED. Because the actual error signal combiner will directly stop the stimulation at the H-bridge, the priority of the error signal combiner submodule can be quite low. The lowest priority (priority = 5) is for the control submodule timer because this timer will just change the values a little slower but does not effect the operation of the system.

5.2. Prototype implementation of the microcontroller module

The complete design overview of the microcontroller module, shown in Figure 5.1, is programmed in several C files corresponding with the submodules of the microcontroller and uploaded to the microcontroller. On request the different files can be shared, the contact info for this can be found in appendix A.1.

The main and intialization submodule

The main code will initialize all the different submodules in the right operating modes and set the interrupts with the right priority as explained in section 5.1. The low priority for the error combiner is not an issue because the error combiner will just change the values which are shown on the screen – and not stop the stimulation, this is done directly at the H-bridge module. The delay due to a low priority will be in the few micro seconds range – which is barely noticeable. By initializing the control submodule, the microcontroller module will start to run. In order to save power, the microcontroller is put in sleep mode when no interrupts are given. The timers of the control are such that the registers, which contains the settings, are updated 20 times per second and the LCD screen – if the values constantly change – are updated 10 times per second.

The ADC submodule

The ADC on the microcontroller has two operating modes: burst and non-burst mode. The implemented ADC submodule is initialized in burst mode. Burst mode is preferred because the value of all the 10-bit ADCs on the microcontroller can continuously be read. From the 8 ADCs available on the microcontroller, four are used for reading out the values of the four potentiometers. Used for changing the waveform parameters. One ADC is used for reading out the voltage level of the battery, how this is exacly done can be found in the waveform report [1]. The other 3 are not used and therefore disabled. The ADC module will continuously update the values of the 5 ADCs and put the result in the memory. The ADC module will give an interrupt if one or more of the values of the array change. If the battery voltage is below 7.5 V, the ADC module will turn the battery low LED lamp on. If the battery voltage is below 7 V, the ADC module will turn the complete system off.

The error signal combiner submodule

The error signal combiner submodule is the implementation of the communication between the microcontroller and the actual error signal combiner module. This submodule will turn on the safety error LED and stop the communication of stimulation parameters in the control submodule to the H-bridge and the DAC.

The control submodule

The control submodule initializes the LCD screen and puts the amplitude, frequency, pulse width and phase delay on the screen. The delay module is initialized by the control submodule. The control submodule will first discard the lowest bits or map the bits of the 10-bit ADC to the desired range of the specific parameter. Not using all the 1024 different levels (0-1023) detectable by the ADC, increases the stability of an accurate read-out. The mapping is done by a function which implements the following calculation and automatically discards the decimals because the use of integers:

$$(x - in_{min}) \times \frac{out_{max} - out_{min}}{in_{max} - in_{min}} + out_min \tag{5.1}$$

Where x is the value of the potentiometers value of that specific parameter and in_{min}, in_{max}, out_{min} and out_{max} the minimum and maximum values of the in- and output range for the mapping.

For the frequency the 6 lowest bits are discarded to get values between 0 and 15. For the amplitude, the 10-bit values are mapped to values between 0 and 100. For the pulse width and interphase delay, the 10-bit values are mapped between 0 and 1000 and are multiplied to get the desired range with 1 decimal accuracy. As already explained in section 4.3, these two parameters use more precise potentiometers integrated to obtain a more stable value from the ADC without the need to discard bits. The 10-bit ADC values for the pulse width and inter phase delay are checked to see if they can fit in the period of the pulse using the (in)equality of equation 5.2 before they are mapped.

$$\frac{1000}{\text{frequency}} \leq 2 \times \text{pulse width} + \text{interphase delay} \tag{5.2}$$

Here, the frequency is in kHz and the pulse width and interphase delay are in μs. When the interpulse delay or interval time is non-zero, Equation 5.2 becomes an inequality. If the inequality holds, the 10-bit values for the pulse width and interphase delay are mapped to values between 0 and 500.0 μs and 0 and 1000.0 μs respectively. The maximum values are chosen separately such that the pulse width and interphase delay can be set maximum at the highest period – which is at 1 kHz. However also at 1 kHz, the (in)equality check is still valid since the maximum value of the pulse width is only possible when the interphase delay is zero and vice versa. If the frequency increases, the values for the pulse width and interphase delay which were possible at the frequency before may however become too high for the new frequency. In order to better understand the definitions of the different stimulation parameters, the parameters are visualized in Figure 5.2.

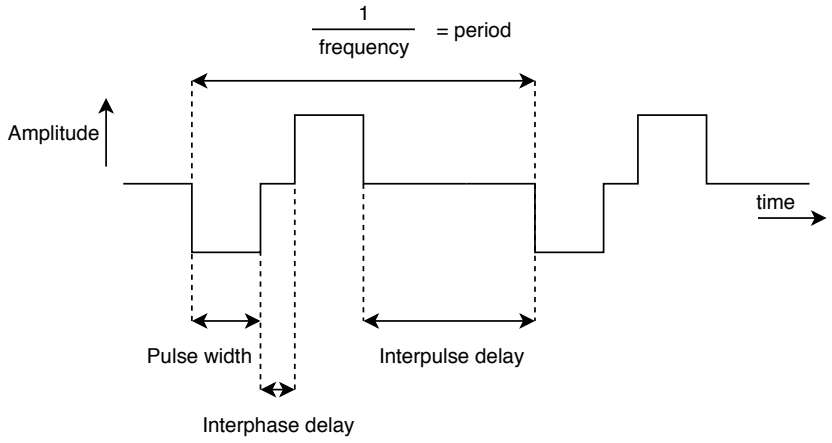


Figure 5.2: The implemented biphasic waveform and the definitions of the amplitude, frequency, period, pulse width, interphase delay and interpulse delay visualized.

Using the (in)equality check, the control submodule is able to limit the parameters to physically possible values. If the parameters are limited by the control submodule, it will also generate an error signal which will set the paramater limit LED on.

The mapped values for the amplitude, frequency, pulse width and interphase delay set by the potentiometers – and maybe limited by the control submodule – will then be saved in registers. After the first cycle the parameters are constantly checked if the new value is more than 1 higher/lower than the old value in the register, before being stored. This check was implemented in order too prevent bouncing behaviour between two values of the ADC.

The amplitude register will continuously be read after each waveform cycle by the DAC module and the frequency, pulse width and interphase delay registers will continuously be read after each waveform by the H-bridge module. Approximately at the same time as the values are being read by the DAC and H-bridge module, the control module will have sent the data to the LEDSET submodule to print the parameter values on the screen. Since the biggest latency for printing data and reading values is a few microseconds which is much less than the 50 ms and 100 ms at which the data and screen are being refreshed.

The LCDSET, LCD16×2, delay and I²C submodules

The LCDSET and LCD16×2 submodules handle all the functions for writing data and commands to the LCD screen. The delay submodule is necessary for the required delay when writing data and commands, which takes time to settle. The microcontroller uses the internally integrated I²C adapter of the microcontroller – which functionality is integrated in the I²C submodule of Figure 5.1 – to communicate to the I²C adapter on the back of the LCD screen. The I²C communication was used in order to save connection pins on the microcontroller. This can also be seen in the hardware implementation of the LCD screen with I²C adapter shown in Figure 5.3. The data for the 16 LCD pins, now needs to be send over the serial clock signal in I²C (SCL) and serial data signal in I²C (SDA). This made the control of the LCD screen much more difficult. Therefore, the LCD control was implemented by using multiple submodules.

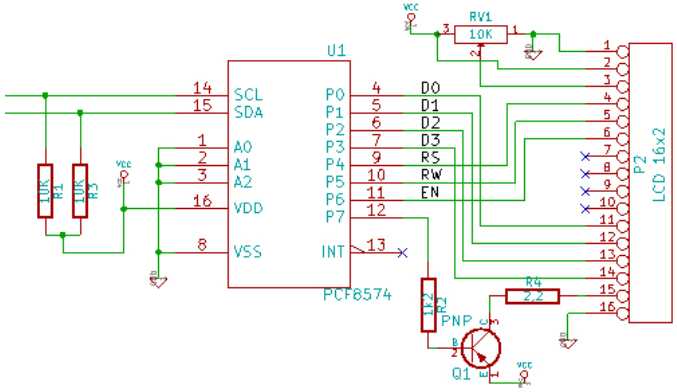


Figure 5.3: The LCD screen with I²C implementation [24]. The SCL and SDA signals are the clock and data signals of the I²C. The D0-D3 are the 4 data pins available using the I²C communication protocol, where without the I²C protocol the LCD has 8 data pins. The **RS** is the register select which selects the command register when low and data register when high. The **RW** is the read/write signal which when low writes to the register and when high to reads from the register. The **EN** sends data to data pins when a high to low pulse is given. The variable resistance **RV1** is to adjust the contrast of the screen. The signal from pin **P7** of the I²C module is to get the backlight on.

The LCDdata submodule

The LCDSET submodule uses functions which convert the integer values into individual numbers and commands in order to write data to the LCD screen. The individual numbers are also converted from integers into characters. The individual write data and command functions used in these functions, are specified in the LCD16×2 submodule. Different functions are made for the different amount of integer and fractional digits at which data is written for the different parameters.

The LCD16×2 submodule

The LCD16×2 submodule contains all the different functions which can be used with the LCD screen such as clearing the screen, setting the display, setting the cursor, setting the backlight, blinking, scrolling and writing data and commands. The LCD16×2 submodule is directly addressed by the control submodule when the LCD screen has to be initialized. The correct initialization is very important in order to be able to write data and commands correctly. The initialization will set the 2 rows and 16 columns and the font size of characters. Also the initialization will always clear the screen with no cursor or blinking, the default text direction and set up the mode where entry is possible.

The 7-bits data – this is the data for one individual character in American Standard Code for Information Interchange (ASCII) – or 7-bits for the command is divided into two 4 bits parts. This is done because the address space of the I²C protocol consist of 7-bits and more data needs to be send to the LCD, such as whether command or data is written. Depending on if a command or data must be written, 1-bit is used to determine whether data or a command is being written. The two other bits are used for a backlight value bit and a bit read/write bit – which is always high because the registers of the LCD screen are never read. Directly after sending the data, an enable signal is also send which makes sure the external I²C module is able to send the data to the data pins on the LCD screen.

The I^{2}C submodule
The I^{2}C submodule is the integration of the I^{2}C protocol on the microcontroller. The I^{2}C communication works with a clock signal line and a data signal line, where multiple devices can connect to. Since the microcontroller is the only device which can send data over the communication bus, the master transmitter mode is selected where one master sends signals to (multiple) slaves. The implemented protocol for the master transmitter can be found in the manual of the microcontroller [23]. The master transmitter mode operation also visualized in appendix Figure A.1. The I^{2}C clock data signal frequency is standard 100 kHz and it has been tested at higher frequencies, which Fast-mode (400 kHz) and Fast-mode Plus (1 MHz). However this difference was not change in the user experience, regarding the updates of the LCD.

5.3. Discussion on the microcontroller implementation

The LPC1343 microcontroller was a good choice, but had as downside compared to microcontrollers like Arduino or Raspberry Pi that a lot of functionalities had to be written by ourselves. Especially for theLCD with I^{2}C integration this took quite some effort, because little to no documentation was available.

Currently, the frequency, pulse width and interphase delay are dependent on each other in order to limit the parameters to physical possible settings. Literature suggests that for high frequency stimulation higher frequencies require linearly related higher amplitudes to block peripheral nerves [22]. Therefore, one could argue that the maximum amplitude is should be dependent on the selected frequency. Since this is not integrated, this could mean that the maximum amplitude is too high for 1 kHz, but too low for 15 kHz.

Saving data on the stimulation parameters, by a building a more advance graphical interface, is a feature which has been considered. Considering the implications of needing to sending the data or storing the data on a flash drive, this was not done. Especially for a research device, this could however still be a valuable feature. It makes it easier to handle and saving the relevant data obtained from the tests and create better documentation on the test results.

Lastly, the microprocessor is now integrated while being still implemented on a development board. In the future the microprocessor and oscillation crystal could be integrated into the complete PCB design. Similar to the idea of saving data, this features is not implemented because it is very time consuming and does not add much value to the main purpose of the device.

6 | Current source

The electrical stimulation of tissue, in order to activate or suppress neuron response, is dependent on the amount of charge applied. The stimulation can be differentiated on whether the signal is voltage controlled or current controlled. When there is no power limitation, the current controlled stimulator is preferred because current stimulation intensity is directly controllable [11] and the applied charge to the tissue is more precisely known [25, 26]. However, current controlled stimulation has a low power efficiency due to highly variable and dynamic range of the Electrode-Tissue Interface (ETI) [10]. The voltage controlled stimulation can achieve two to three times higher energy efficiency [27], but the injected charge and stimulation intensity will depend on the load [11].

Taking all in mind, a current controlled system is preferred since power efficiency is not a limiting factor for the arbitrary waveform generator and precisely knowing the injected charge is very important for safe stimulation. In a future iteration, voltage controlled can also be used since the difference between current and voltage controlled stimulation is not as big as the influence caused by changes in the medium conductivity and electrode distance [28].

6.1. Current source description

In the following chapter, an insight into the design process of a current source is given. This current source is being designed for Continuous Current Stimulation (CCS) and will result in the stimulation after a voltage signal is created by the DAC implemented by the waveform subgroup. The main consideration for choosing CCS is a stable output independent of a certain load-impedance range. Furthermore, the safety of the system is of great importance, while size, power and speed are of less importance for the design. In the simulation and prototype described in section 6.3, an in-depth analysis will be given of the selected current source.

6.1.1. The load-impedance range

The load impedance is dependent on three factors: the load internally added by the system, the impedance of the electrode and the ETI. The electrode impedance is given in the manual of the used electrode [29]. It has a typical value of 125 Ω. A value of 90 Ω was measured with one sample electrode. Only one electrode was measured due to the low availability of these devices. The conclusion can be drawn that the specified impedance is valid and can be used. The ETI is more problematic since this is not documented somewhere within reach. A paper [30] suggest some values for different kind of interfaces, but most interestingly that the impedance of tissue goes down when the frequency goes up.

In the manual of the Medtronic 3625 Test Stimulator [15] is suggested that the maximum voltage, that is safe to fall over the tissue, is 10.5 V. With a basic Ohm's law calculation: when a constant maximum current of 10 mA is determined, this leads to a maximum load impedance of 1.05 KΩ. This value can be seen as the ETI plus the electrode impedance and internal resistance of the device. Important to notice here is that this an assumption and is not necessarily true. Staying within the safety range of the Medtronic 3625 means that the device under design will stay in the same safety regions of maximum voltages and currents. The charge applied to the tissue is something else which needs to be considered separately. This will be discussed in the report of the safety group [2]. The safety ranges specified for the Medtronic 3625 implies that stimulation with 10 mA is safe up to a tissue impedance of 1.05 kΩ. This will be the maximum impedance at which the device will still be able to deliver 10 mA. An important thing to notice is that the safety module will add 200 Ω resistance in the stimulation path. In total, the device must be able to deliverer 10 mA up to 1.25 kΩ. More on safe stimulation can be found in the report of the safety subgroup [2].

6.1.2. Input signals

The battery which powers the device will be a 9 V battery. The subsystems under design need two different supply lines: a 15 V line and a reference voltage. The reference voltage for the current source is delivered

via a Digital-to-Analog Converter (DAC) by the microcontroller. The DAC is part of the waveform group and is extensively documented is their report. The 15 V is generated using a boost converter, more specific the *MAXIM INTEGRATED CMOS fixed/adjustable Output Step-Up Switching Regulators (MAX633)*. More on these choices can be found the report of the waveform group [1]. A simplistic module overview can be found in Figure 6.1.

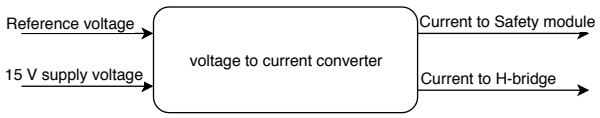


Figure 6.1: Description of the current source as a black box. At the left side of the black box the input a 15 V supply and a Reference voltage are displayed. At the right side of the black box the two current outputs to the safety module and H-bridge are displayed.

6.2. Design of the current source

The current source is responsible for delivering a stable output which is independent of the load that the human tissue can adopt. The amplitude of the current should be a fixed value which is programmed by a microcontroller based on the input from user on the interface of the device. In this way, the user has full control over the applied charge injected into the tissue. An ideal current source would be the perfect current source but, as perfect implies, this does not exist. The challenge is to design a current source that comes close to the ideal current source for the specific impedance region where it will be used.

The designed device is a test device which will not be implantable and only used for short time periods. Therefore, size and power not as important as the other constraints. The size is restrained by the fact the device is used in the operating room and must be easy to handle by the operator. The power used is not a problem as long it is within the safety constraints.

For the independence of the load impedance, different typologies will be reviewed in the upcoming sections and in the end, a discussion will be held to defend the choice of the final topology.

6.2.1. Single transistor source topology

A single transistor can be used to create a current source. The current source operates as a constant current source when the transistor is biased in the saturation region. Using a Metal-oxide-semiconductor field-effect transistor (MOSFET) gives us the power of a voltage controlled device. Instead of a current controlled device which holds for a bipolar transistor. Using a DAC as the reference voltage for the current source, a MOSFET is the preferred choice.

Using a very simple circuit as in Figure 6.2, allows for some calculations to be performed on the behaviour of the transistor. These calculation are all for the saturation mode of the transistor, thus it is important that the transistor is kept in this mode.

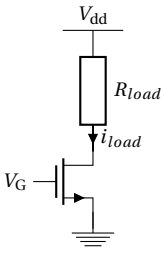


Figure 6.2: A single N-channel MOSFET (NMOS) as current source, used to explain the behaviour of MOS devices.

The current i_{load} is given by the MOSFET current in Equation 6.1. This equation only holds if the *Gate-source voltage (V_{GS})* is larger than the *Threshold voltage (V_{TH})* and the *drain-source voltage (V_{DS})* > V_{GS} - V_{TH}, or in other words that the MOSFET transistor is in saturation mode. There is an overhead voltage needed of $V_{ov} = V_{GS} - V_{TH}$. The K_p or K_n ($= \mu \times C_{ox} \frac{W}{L}$) is a constant that is dependent on the physical properties of

the transistor, which can be found in most data-sheets or simulations of the component. The channel length modulation of a transistor is given by λ. The drain-current expression is a first-order approximation, which is reasonably accurate for devices with a channel length greater than approximately 2 μm. More information on how this equation is formed can be on the following website [31].

$$I_D = \frac{K_p}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{6.1}$$

N-channel MOSFET (NMOS) vs P-channel MOSFET (PMOS)
Choosing between a NMOS or PMOS transistor is choosing between a current sink or source design. Both would do just fine in the suitable application. For the design requirements of the REValUE project, both would be able to deliver the right amount of current to the load.

Since the reference voltage used to set the current from the DAC only goes up to 3.3 V, the design choice was made to go with a NMOS transistor. This is because they need a lower reference voltage than a PMOS. There is also a need for safety measurements to have a second current output which is an exact copy of the current going to the load. Later the direction of the current will be adjusted and a copy is made using a current mirror.

Active feedback
The fact that the drain current is not linearly dependent on the gate voltage of the MOSFET transistor makes it difficult to determine. Since the DAC used in this project is linear, the changes in the voltage are preferably linearly proportional to the changes in current. This behaviour can be achieved using the topology as given in Figure 6.3. Since the Operational amplifier (op-amp) with negative feedback wants to have the same voltages on the non-inverting input as the inverting input of the amplifier and gives an output, this can be established with an op-amp. Therefore, if it is within the limits of the amplifier's source voltage, the voltage over R_{set} will be regulated to the same voltage as applied to the non-inverting input. Using this active feedback the current I_{set} will be well defined by Equation 6.2.

$$I_{set} = \frac{V_{ref}}{R_s} \tag{6.2}$$

The op-amp does not need to meet a lot of requirements, but the op-amp speed does not influence the accuracy of the stimulation while it only changes the amplitude. So the slew rate (how fast the op-amp can change the output voltage) is not an important parameter. The only parameter which has to meet the requirements is the required supply range to set the required gate voltage. The required supply range can be calculated from the V_G Equation 6.3.

$$\begin{aligned} V_{GS} &= \sqrt{\frac{I_d}{\frac{1}{2}K_n}} + V_{TH} \\ V_S &= R_{set} \times I_D \\ V_G = V_{GS} - V_S &= \sqrt{\frac{I_d}{\frac{1}{2}K_n}} + V_{TH} - R_{set} \times \left(\frac{K_p}{2}(V_{GS} - V_{TH})^2\right) \end{aligned} \tag{6.3}$$

In the calculated range of Equation 6.3 a simplified version of Equation 6.1 is taken and rearranged. Where the channel length modulation is left out, because it is only an indication of the needed supply voltage. The simulation will provide proof if this indication of the range was well enough.

6.2.2. The current mirror topology

A current mirror has a topology designed to copy a current through an active device by controlling the current flowing through another active device, thus keeping the output current constant. Conceptually, an ideal current mirror is an ideal inverting current amplifier that reverses the current direction as well. A current mirror can also be used to model a more realistic current source, since ideal current sources do not exist. It is not only able to create one copy but can easily be altered to create more than one copy. A example topology of a simple current mirror is given in Figure 6.4.

It is important to notice that it is crucial for transistor M3 to be in the saturation region, in order to stay independent from the load. The equation to calculate the maximum load is given in a simplified version in

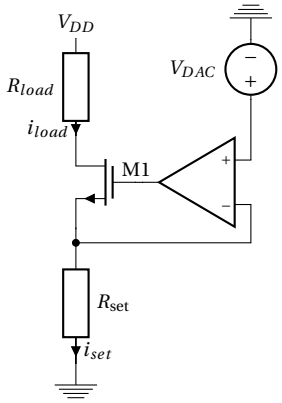


Figure 6.3: An NMOS topology with an actively regulated V_{gate} voltage circuit is given using an op-amp, as negative feedback loop. The topology regulates the voltage over R_{ref} to become equal to the voltages set by V_{DAC}. The I_{load} is therefore linearly dependent on V_{DAC} as long the transistor is in saturation mode. The current I_{set} will equal I_{load} because a NMOS does not require a gate current.

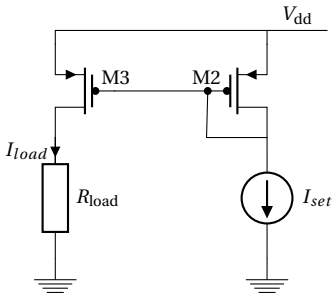


Figure 6.4: Topology to reach a copy of I_{set}, the copy will be I_{load}, Transistor M2 is the regulating active device, where M3 delivers the copy.

Equation 6.4. This equation gives a good indication of the parameters which are needed to reach the desired behaviour. For the real values, a detailed simulation will be done to obtain an even better indication.

$$R_{max} = \frac{V_{GS} - V_{TH}}{I_D} \tag{6.4}$$

Another really important aspect of the current mirror is that the transistors are well matched. If the K_p values match in Equation 6.5, the output-input ratio is given by Equation 6.6. With Equation 6.6 another problem occurs, namely the channel-length modulation. V_{SD2} equals $VSG2$ because of the topology, but this is not the case for V_{SD3}. The value of V_{SD3} is dependent on the voltage drop over the load. Equation 6.6 shows that even when using a perfect matching transistor couple, there can still be some significant differences between I_{ref} and I_{load}.

$$\begin{aligned} I_{ref} &= \frac{k_{p2}}{2}(V_{SG2} - V_{TH2})^2(1 + \lambda_1 V_{SD2}) \\ I_{load} &= \frac{k_{p3}}{2}(V_{SG3} - V_{TH3})^2(1 + \lambda_2 V_{SD3}) \end{aligned} \tag{6.5}$$

$$\frac{I_{load}}{I_{ref}} = \frac{(1 + \lambda_1 V_{SD2})}{(1 + \lambda_2 V_{SD3})} \tag{6.6}$$

To minimize the effects of the channel length modulation a cascoded mirror is used, like the circuit shown in Figure 6.5. Using a cascoded mirror minimizes the effect of the two top transistors M2 and M3. These transistors now have approximately the same V_{SD} which results into a ratio between the I_{load} and I_{ref} of one. This is, of course, in the ideal case which is based on a low-level approximation. The simulations will be performed to check whether or not this model holds.

The last requirement is to get another copy for the safety module. This is done by adding an additional stage to the design. The complete circuit is showed below Figure 6.6. This topology is based on six PMOS transistors, one NMOS transistor, one op-amp and one resistor.

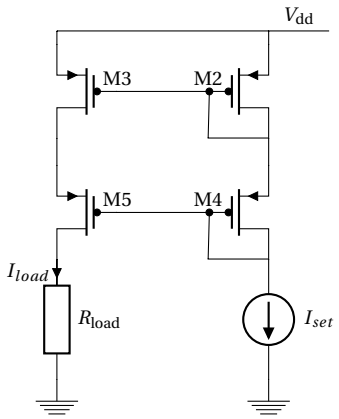


Figure 6.5: In this circuit, M2 and M3 form a current mirror in which both drains are held to the same voltage of V_{GS}. M2 and M3 therefore show a closely matched behaviour. Simultaneously, they serve as emitter impedance for the second current mirror build with M4 and M5. The transistors of each pair must be matched, but the different pairs do not necessarily need to be matched.

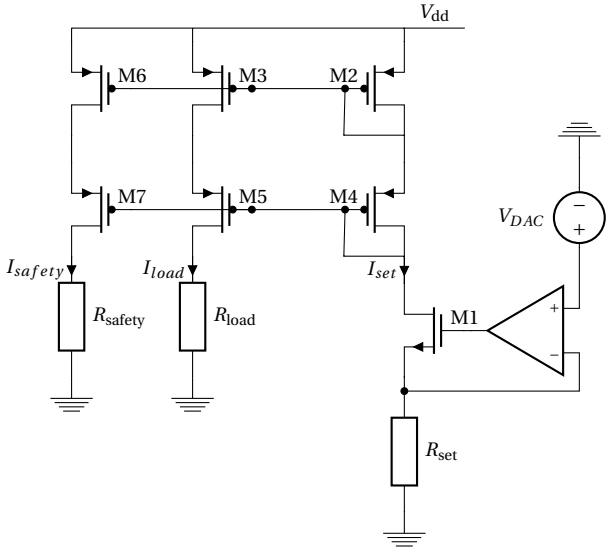


Figure 6.6: A combination of the circuits of Figure 6.3 and Figure 6.5, where the cascode mirror has an extra copy. Note: M6 is matched and part of the pair M3 and M2, where M7 is matched and part of the pair M5 and M4.

6.2.3. Topology decision

The chosen current source topology is a single NMOS transistor with active feedback. This topology is used in combination with a double current mirror to obtain two exact copies of the reference current. One copy will be used by the waveform group to generate the stimulated wave and the other copy is used for the current integrator of the safety subgroup [2]. The active feedback of the current source is necessary to make the system linear. Furthermore, using this method the system is able to control the amplitude with a reference voltage that can be generated using a DAC. The DAC of the microcontroller will be used for the reference voltage and will range between 0 and 3.3 volt. Using a 330 Ω resistance the system will be able to supply 10 mA for loads up to approximately 1.5 kΩ when using a 15 V source.

6.2.4. Component choices

In this section, the component choices will be justified. Regarding these components, there is a problem with the matched PMOS transistors. As research had already indicated, matched PMOS devices do exist, but are in reality most of the time not matched [10].

PNP instead of P-channel MOSFET (PMOS)

The downside of PNP (*Bipolar junction transisitor with a N-doped semiconductor layer between two layers of P-doped material (PNP)*) transistors is that they draw a certain gate current for which has to be compensated.

Because of this, the MOSFET transistors seems to be a better choice, but research suggests that it is really hard to match this MOSFET transistors using discrete components. As a result of this PNP arrays will be used for the discrete implementation of the systems.

As already mentioned PNP transistors are current controlled current sources, where PMOS devices are voltage controlled current sources. The switch to PNP simply means that the base of the transistor is not satisfied with a fixed voltage anymore, but will draw a certain current to stay biased. The saturation mode calculation however still applies using a PNP instead of a PMOS device, which is very important because the load impedance requirement will still be satisfied. However, the output amplitude is not satisfied anymore. The current which is needed to bias the PNP transistors has to be subtracted from the I_{set}. The current that is needed is dependent on the DC current gain β, by $I_B = \frac{I_C}{\beta}$. When applied to the topology, with some reordering, the current I_{out} is described by Equation 6.7. This system is linear and I_{out} can be expressed in a percentage of I_{ref} as long the PNP transistors are all biased in saturation region. The typical ratio for the THAT320 PNP transistor integrated into the topology is given by Equation 6.8.

$$I_{out} = (I_{set} - 3 \times \left(\frac{I_{set}}{\beta}\right) - \frac{3 \times (I_{set} - \frac{3I_{set}}{\beta})}{\beta} \tag{6.7}$$

$$I_{out} = I_{set} \times \frac{\beta - 6 + \frac{9}{\beta}}{\beta} = I_{set} \times 92.16\% \tag{6.8}$$

As can be concluded approximately 8% of the current is lost due to the base currents. For the project, this has not immediately significant impact. The most straightforward solution is to pick a new R_{set} value that is 7.84% lower than the 330 Ω. But this is all based on the fact it is exactly known what the DC current gain is. In practice this is not the case which makes this circuit very hard to tune, implementing a potentiometer would be a better solution instead of a fixed value resistor for R_{set}. But compensation is not the correct way to solve an issue, a feedback system that actively regulated this loss would be preferable.

Proposed new circuit
To create this feedback system the topology displayed in Figure 6.7 is proposed. The PMOS (M2) regulates that the current I_{safety} and I_{load} are equal to I_{set}. Because there is now a MOSFET transistor that regulates the base setting of the top array of transistors. The property of a voltage controlled current source is restored. The second line of transistor still needs to be biased to the saturation mode. This is done with the addition of 2 PNP transistors. The only function of Q8 and Q9 is to drop the voltage v_{dd} to the right base voltage for the lower transistor array. Resistor R_1 and R_2 are essential to protect the PNP transistor against damage. In the case, there is no load connected to the drain of transistor Q7 and/or Q5, in other words, the collector is floating. The transistor will push the current that comes out of transistors Q6 and Q3 through the base of transistors Q7 and Q5.

Component list
All components are chosen based on their availability and needed requirements. V_{dd} is chosen to be 15 V and therefore all transistor must be able to handle 15 V. The same goes for the op-amps positive power supply that will be supplied with V_{dd}. The negative power supply will be grounded. This combined with the fact that the slew-rate is not important, the *Texas Instruments LMx58-N Low-Power, Dual-Operational Amplifiers (LM358)* are a perfect choice, certainly knowing that these components are easily accessible. A benefit of this choice is the fact it is optimized for low noise, which is not that significant for the design, but a positive extra feature.

For the NMOS transistor there where not that many requirements due to the chosen topology, the NMOS will not see big loads and will never see more than 15 V over its terminals. Within the project, the *2N7000G Small Signal MOSFET 200 mAmps, 60 Volts (2N7000)* was already used and met all requirements. The resistor R_{set} is crucial to be as close as possible to the required value (of 330 Ω).

For the transistor array, there was little choice of what could be ordered. The most important parameter here is the DC gain of the PNP transistors. The highest DC gain was 75 [Hfe], the importance of this DC gain being as high as possible is discussed later in this chapter. Taking this into consideration the *THAT 300 series, Low-Noise Matched Transistor Array ICs (THAT320)* is selected. The bases of the transistor in the

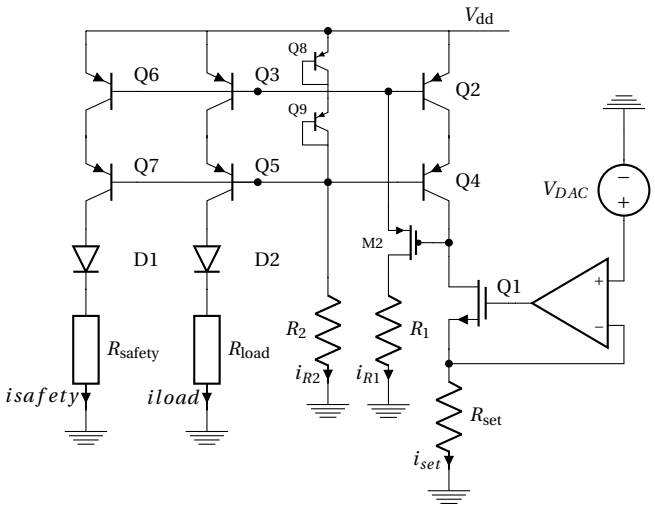
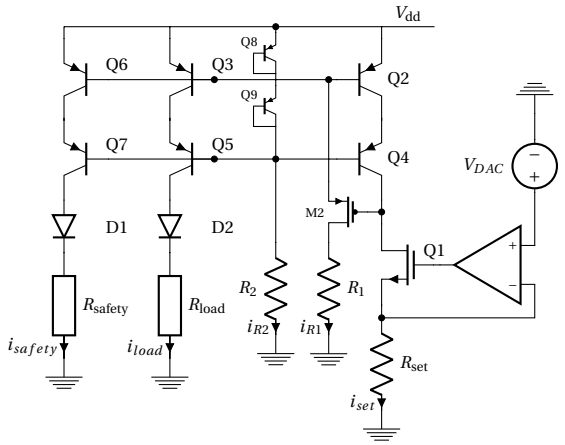


Figure 6.7: The circuit from Figure 6.6 implemented with PNP transistors. The gate lines are biased using 1 active feedback for the top line and 2 PNP transistors to drop the bottom line to the desired potential. Resistors R1 and R2 are implemented for protection and have a current limiting function. To this topology 2 diodes are added, D1 and D2, in order to separate all current lines. This way if a transistor breaks down, the system will never put unexpected currents on a specific line.

case of the THAT320 can only handle currents up to 1mA. To make sure this current will not exceed this current level 20KΩ resistor is added to each base path. The maximum current that can flow will never exceed $\frac{V_{dd}}{R} = \frac{15}{20} = 0.75$ mA. This still is enough to properly bias the transistors when maximum settings are selected ($I_b = 3 * \frac{10\text{mA}}{75[hFe]} = 0.4\text{mA}$).

For the PMOS the same goes as for the chosen NMOS, it just must be able to handle to voltages and currents that can occur. The FAIRCHILDFQD17P06 / FQU17P06 P-Channel QFET MOSFET (FQD17P06) was selected because it could handle the voltages and currents. Lastly, two diodes FAIRCHILD 1N4446 Small Signal Diode (1N4446), are added to the design. These play a key role when R_{load} becomes a source instead of a resistor. In this case, the current generated can never flow towards the rest of the system.



Component	Discrete implementation
M1	2N7000
M2	FQD17P06
Q2,Q3,Q6,Q8	THAT320, pack1
Q4,Q5,Q7,Q9	THAT320, pack2
Opamp	LM358
R_{set}	330 Ω
R_1,R_2	20 $k\Omega$
D1,D2	1N4446

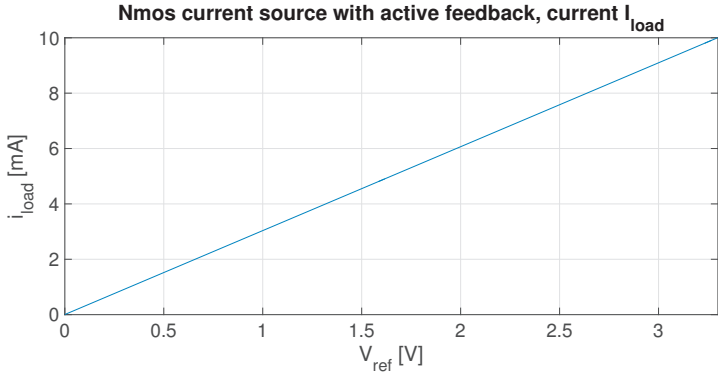
Figure 6.8: On the left the final proposed circuit is shown with on the right a table containing the selected components.

6.3. Simulation and prototyping results

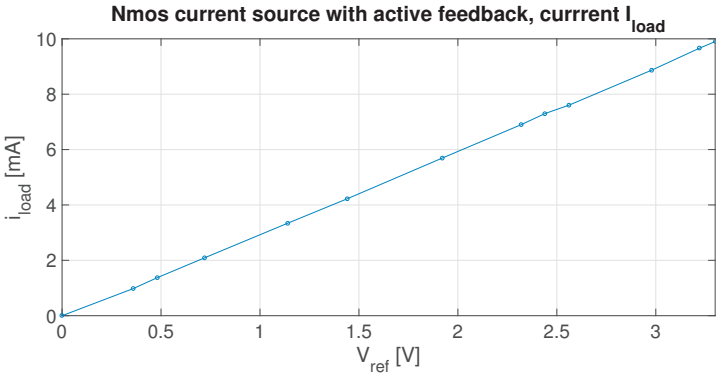
In this section, the simulations of the different version of the current source are executed and compared to a real implementation with the components as specified in Figure 6.8, the same components are used for all circuits. The simulation software used is LTspice [32]. The net-list and used libraries are available on request,

the contact info for this can be found in appendix A.1.

NMOS with active feedback
The circuit in Figure 6.3 will be the first submodule tested. This submodule has to set a certain current and regulate the voltages over R_{set} in a manner this circuit is controllable via the DAC. The DAC is able to deliver a voltage with more than 0.033 V precision on the non-inverting input of the op-amp. This corresponds with a precision in current amplitude of more then $\frac{\Delta V_{ref}}{R_{set}} = 0.1$ mA. So the requirement on the ability to set the current amplitude with a certain precision is met. In the LTspice simulations, this can be shown graphically when the reference voltage is stepped with 0.033 from 0 to 3.3 volts, the acquired results are shown in Figure 6.9a. When implemented in discrete components, the same result as in simulation where acquired with deviations that never exceed the requirements of the circuit, see Figure 6.9b. The prototype measurements were done with a multimeter and are just an indication.



(a) Simulation results done with LTspice to determine the V_{ref} vs i_{load} ratio.

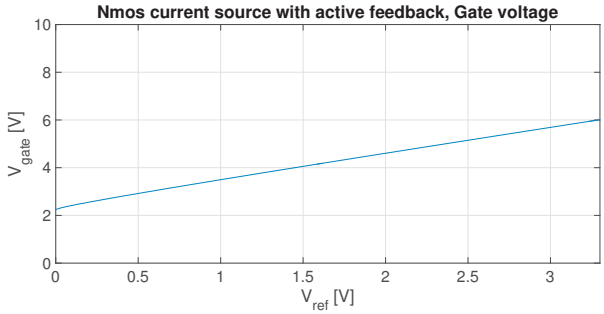


(b) Prototype measurements done with multimeter, to determine the V_{ref} vs i_{load} ratio.

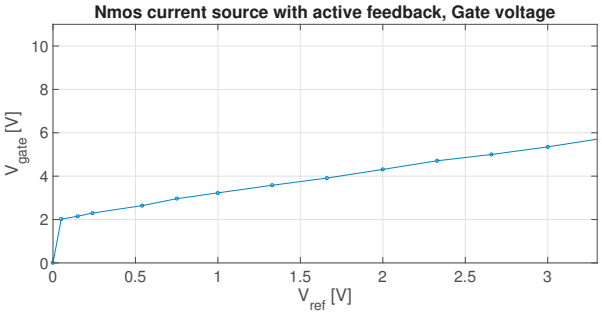
Figure 6.9: Simulation versus prototype measurements, to establish if the simulations done are matching reality, this is the case as can be abstracted from the figures.

The gate voltages that are needed to control the NMOS, are delivered by the output of the op-amp, a simulation and prototype test is done. This is to ensure that the op-amp is able to deliver the output voltages. The positive power supply of the op-amp is connected to the 15 V line. The negative power supply is grounded. When the results of the simulation, Figure 6.10a, are compared to the prototype results, we obtain Figure 6.10b. It is clear that the prototype behaves as expected and the op-amp with 15 V supply is well capable of delivering these voltages. Note that these measurements are done with a multimeter and are just an indication.

Current mirror
The current mirror must be able to copy a current up to 10 mA when connected to a load that can go up to 1 Ω. For simulation purposes the FDC5614P from Fairchild is used for the PMOS devices, this is a standard in LTspice (with parameters for channel length modulation and a well-documented library). Note that this is just



(a) Simulationone with LTspice, to determine the V_G necessary to set a certain V_{Rset} that equals V_{ref}



(b) Prototype measurements done with multimeter, to determine the V_G necessary to set a certain V_{Rset} that equals V_{ref}

Figure 6.10: Simulation versus prototype measurements, to establish if the simulations done are matching reality. Which as can be abstracted from the figures is the case.

a graphical explanation of the choices made. Of course, it can be improved by picking better components but fundamentally it still is not the perfect topology. Improving it in this manner is not the way to go. The PMOS transistors are replaced for PNP transistors in the same configuration, more specific the THAT320 transistors are used for simulation.

Immediately, the difference between the bipolar and MOSFET transistors can be seen from Figure 6.11. Bipolar loses a percentage of the current to the bases of the transistor and therefore is a constant factor lower than the MOSFET output current. When changing V_{ref} the same limits are acquired but shifted to lower amplitudes levels a detailed graph of this can be found in the appendix Figure A.2. For further simulations, V_{ref} is set to the fixed maximum value of 3.3 V.

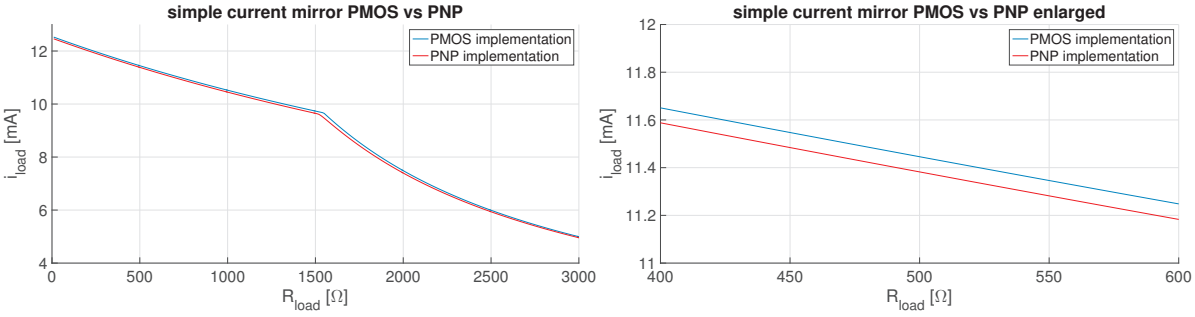


Figure 6.11: Simulated dependency of I_{load} on R_{load} in a simple current mirror circuit Figure 6.4 for PMOS and PNP implementation. The PNP implementation shows constantly a lower load current. At the left an overview of the complete run is given. At the right, a zoomed version to the region of interest of the same simulation results.

Cascode current mirror

To improve the topology a cascode current mirror is suggested, as already explained in the design phase subsection 6.2.2 this improves the characteristics of the circuit. The simulations do confirm the theory, see Figure 6.12. Again it is clear the PMOS behaves better and is able to deliver a stable 10 mA current to a load of approximately 1300 Ω. The PNP implementation does behave reasonably well when the 8% of losses are not taken into account, but does cope with some larger deviations in the 'flat-region'.

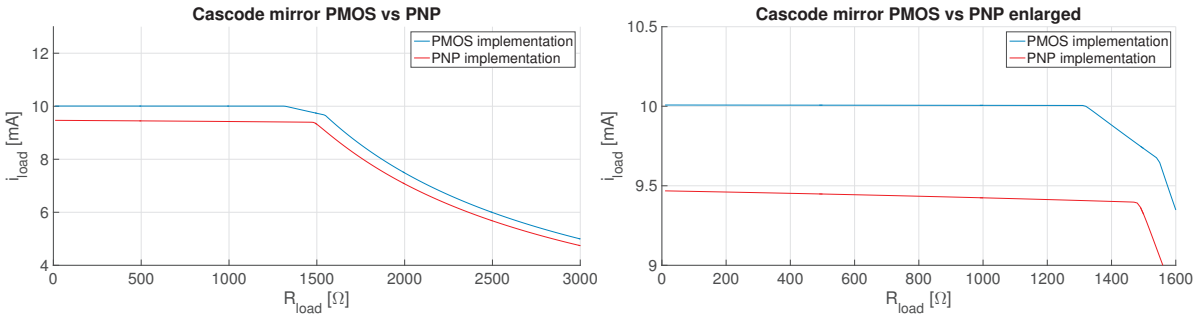


Figure 6.12: Simulated dependency of I_{load} on R_{load} in a cascode current mirror circuit Figure 6.5 for PMOS and PNP implementation. The PNP implementation shows constantly a lower load current. At the left an overview of the complete run is given. At the right, a zoomed version to the region of interest of the same simulation results.

6.3.1. First prototype

For the first version of the current source, which is based on the circuit from Figure 6.5, only one thing changes and that is the fact there needs to be a second copy. This makes the losses due to the base currents of the PNP transistors a little bigger. Approximately going from 5% up to 8% with the typical DC current gain of the THAT320 transistors (75hFE). As mentioned the PNP implementation, see Figure 6.13, is used for the implemented circuit. The fact that the PNP implementation is not as flat as the PMOS implementation is not that big of a deal because a precision of 0.1 mA is required.

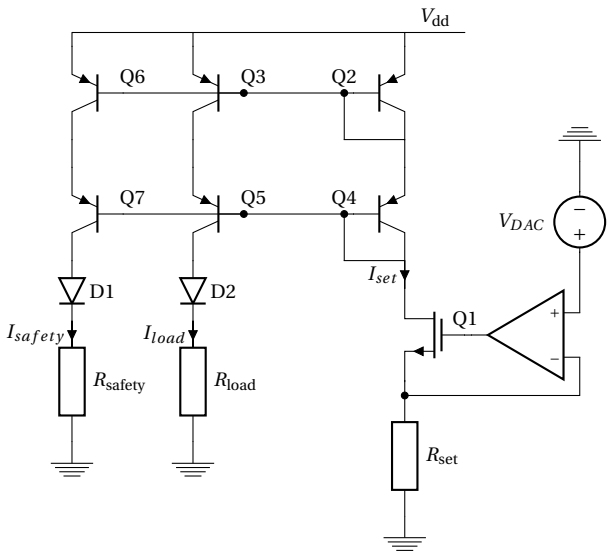


Figure 6.13: Circuit topology of the first version current source designed for the REValUE project

Simulation

This PNP implementation of the first version is simulated, the results can be found in Figure 6.14. Here a problem arises: The current to the safety module is not an exact copy of the current to the tissue. This due to the fact that the impedance of the safety system does not match the impedance of the tissue – the impedance of the safety system is kept at a constant value of 30 Ω where the value impedance value of the

tissue channel can be found on the x-axis – as a result of different V_{DS} voltages received by the transistors. The output current is not perfectly flat but with a deviation of 0.056 mA well within requirements. The fact that the i_{safety} does not precisely copy the current with a maximum deviation of 0.029 in simulation and how this differs for different frequencies and loads will be elaborated on in [2].

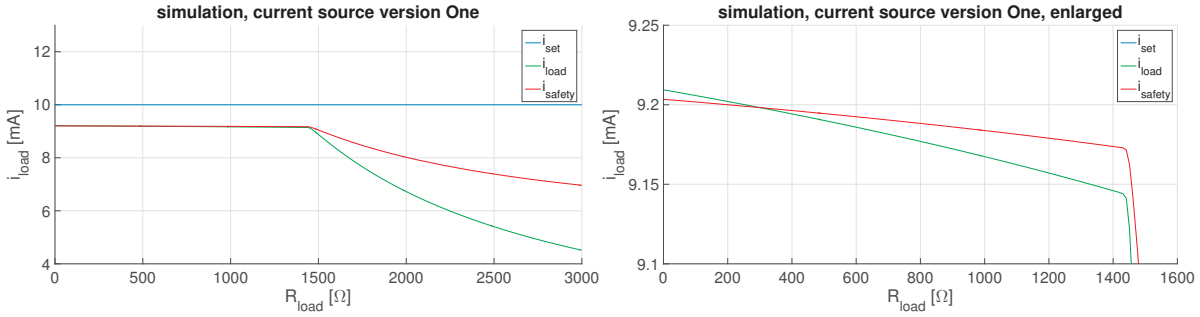


Figure 6.14: Simulated dependency of I_{load} on R_{load} in the version one current source circuit Figure 6.13. Left an overview of the complete run is given. At the right, a zoomed version to the region of interest of the same simulation results. Simulation is done to see if the 2 copies have the same behaviour, where R_{load} is the parameter that is stepped from 0 to 3000 Ω and the R_{safety} is kept at a constant 300 Ω which most likely will be the impedance of the safety system connected to this line. More on the system can be found in the safety group's report [2].

Prototype results

The circuit from Figure 6.13 is build using the components form Figure 6.8. The circuit is then tested and measured. Two voltages supplies are used to deliver the required voltages (in Dutch named: "voedingsapparaat D 030-1, from DELTA elektronika"). The current is measured by means of a multimeter, which does not have the highest accuracy. To determine if the requirements are met, only a 0.1 mA accuracy is needed. which means that (the accuracy of) a multimeter will be sufficient for these measurements.

The results are displayed in Figure 6.15. When these results are compared to the simulations it can be concluded the prototype works properly.

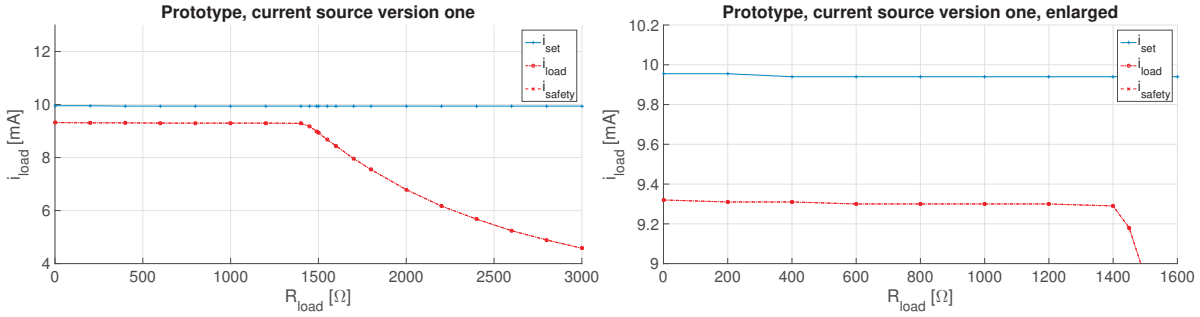


Figure 6.15: Prototype measurements results of I_{load} on R_{load} on the version one current source topology from Figure 6.13. At the left, an overview of the complete test results is given. At the right a zoomed version to the region of interest of the same results.

6.3.2. Proposed circuit

In this section the second version and also proposed topology for the device is discussed. This topology and a component list can be found in Figure 6.8. This topology should resolve the flaws that version one of the current source had.

Simulations

The simulations results can be found in Figure 6.16. At first sight, the simulation looks promising. The same load impedance is reached but now with the required 10 mA. Also, the output current for the load impedance region has a little less deviation then with version one. This all together gives a lot of potential to this circuit over the current source version one. In the simulation results i_{ideal} is added, this line is purely an indication

line, to see if how the circuit behaves in comparison to the ideal behaviour. In the Appendix a simulations that show the behaviour of this topology for different reference voltages in include, see Figure A.3.

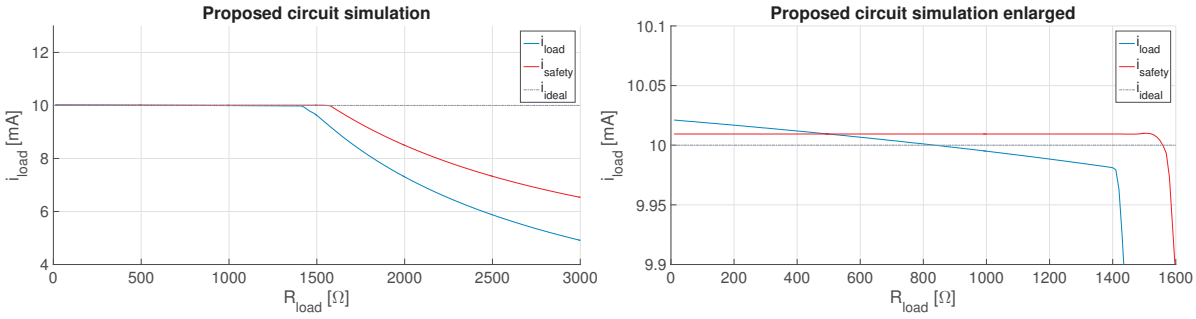


Figure 6.16: Simulated dependency of I_{load} on R_{load} in the proposed final current source topology from Figure 6.7, Left an overview of the complete run is given at the right a zoomed version to the region of interest of the same simulation results. Simulation is done to see if the 2 copies have the same behaviour, where R_{load} is the parameter that is stepped from 0 to 3000 Ω and the R_{safety} is kept at a constant 300 Ω for the same reason as before. i_{ideal} added for comparing the circuit to an ideal behaviour.

Prototype results

The circuit is assembled with the discrete components. The measurement setup is the same as in subsection 6.3.1, the measurements of the topology are done simultaneously with the measurements of the first version, to ensure the same conditions. When the results are compared, it is clear that this topology outperforms version 1. It behaves exactly as expected and perfectly met all requirements that are set for this module.

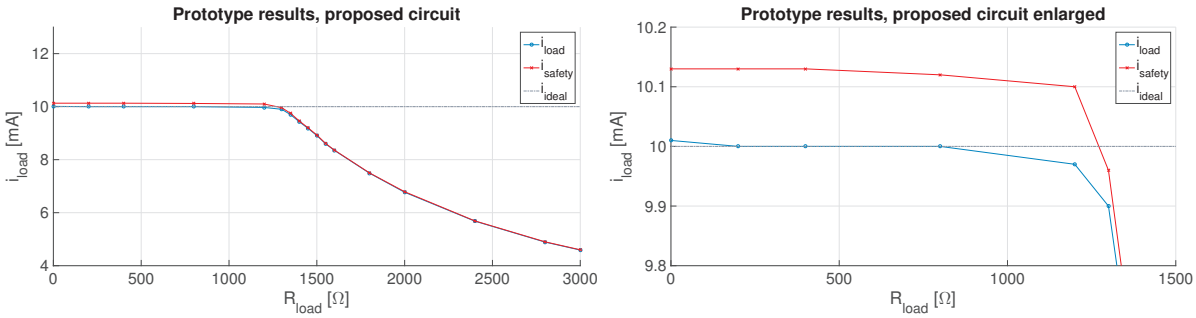


Figure 6.17: Prototype measurements results of I_{load} on R_{load} on the proposed final current source topology from Figure 6.7. At the left an overview of the complete test results is given. At the right a zoomed version to the region of interest of the same results. i_{ideal} added for comparing the circuit to an ideal behaviour.

6.4. Discussion

There was a lot of focus in the chapter on PNP vs PMOS transistors. The recommendation is straightforward here and that uses the topology in Figure 6.5 with a PMOS implementation. This will generate the best results using the least power and space. In the case of discrete components, there was not a PMOS transistor array available for this project that performed as a matched array. That is why that choice was made to go to PNP transistor arrays, which has its flaws. Implementing the topology from Figure 6.7 solves these flaws at the cost of area consumption and power consumption. For the device under design, there are no requirements that detain us from choosing this topology. To conclude, the circuit build with the components from Figure 6.8 behaves as expected in the design phase.

7 | Conclusion and recommendations

7.1. Conclusion

The previous chapters described the design process of a Control and interface module for an arbitrary waveform generator to be used as a neural stimulator. The Control & Interface module meets all primary system and functional requirements described in chapter 2. The Control & Interface module does not meet all the secondary system and functional requirements, namely only the visual interface showing the values of the adjustable parameters requirement has been integrated. The device is not able to generate a voltage driven waveform. This requirement was not given priority since the main advantage of voltage driven is the size and power efficiency, which were not critical for our design.

The device is only able to stimulate with an adjustable biphasic square waveform as displayed in Figure 5.2. Other types of waveforms are not implemented, since they are not significantly more efficacy or safety. The main advantage is to improve energy efficiency of the waveform [1]. Furthermore, low-frequency stimulation is not included in the delivered prototype, due to the limited time for this project. Lastly, the general requirement of having two connectors for the extension cables, which can be connected to our device and simulate on all possible terminals of the two leads, were also implemented by the Control & Interface module.

The three Control & Interface modules obtained a good final result which met the primary requirements. The interface is assembled and it works as it was designed. It has a great user response, in combination with the 16×2 LCD screen used to graphically show the settings the user can change. The control module has been integrated on the NXP LPC1343 microcontroller. The microcontroller overview given in Figure 5.1 shows all the submodules integrated on the microcontroller. All the submodules are implemented with interrupts and the microcontroller is in sleep mode when no interrupt is given which lead to an efficient integration and power saving.

The current source is implemented using a single NMOS with active feedback in combination with a cascode current mirror. This module is implemented using discrete components, which had its challenges, but functions as required by the program of requirements. The current source topology used for this project is not the one preferred. A well design PMOS system would outperform the current topology on the size and power consumption. Implemented on an Integrated Circuit this must be possible to develop.

7.2. Recommendations

From this project some topics for future research have been found. This section will briefly cover these and hopefully lead a path to future innovation and research.

7.2.1. Recommendations on improving the prototype

For the final prototype device which is under development, there are definitely some more, maybe a little less academic, challenges. The device has to be CE marked before it can be used on patients, which means a lot of testing has to be done with the prototype. The final PCB design of the complete system and integration in a case is done nicely, but can definitively be approved also by adding the microprocessor and oscillator from the microcontroller development board. The integration of the low frequency part is very valuable for the research with the device. This way the device is able to both block the urethral sphincter with high frequency as well as contract the ventral roots with low frequency stimulation.

To conclude, the most important improvements on our prototype are thus obtaining the CE marking for testing it on patients, which can/should be done in close contact with our client supervisor. Also, the integration of the low frequency part of the simulator such that the device can also contract the ventral roots.

Recommendations on for a new device

In case a new high frequency neurostimulator is made which will also be implanted, one should look into the possibilities to decrease the size limited and increase the power efficiency of our design. These were both no restrictions for our project but definitively points for improvement. For the size and power efficiency of the device an integration on an Intergrated Circuit (IC) should be considered on which many literature can be found. Also wireless charging can be considered to reduce the size of the battery. Lastly, for the interface a better looking and maybe even more advanced graphical interface is preferable. With a smaller device this has to be externally made such that it communicates with the device via wireless communication.

Clinical research on effectiveness

The effectiveness of high frequency stimulation for blocking the urethral sphincter is not yet proved. Because the high frequency arbitrary waveform neural stimulator is made, it is possible to perform research on patients for the effectiveness. The first tests should be on the pressure difference between the urethra and bladder and rest urethra. Hereafter, the technique should be proved to lead to an major improvement in the voiding function of patients. Especially for the clinical research the testing should be extended with a low-frequency stimulator in order to stimulate the ventral roots, causing bladder contraction. In this research it is specifically interesting to look at the different pressures in the urethra and bladder between men and woman for different frequencies in the high frequency range.

Load impedance of tissue

With high frequency stimulation the impedance of the tissue increases with the frequency [30]. By doing further research on the different impedances of the ETI with specific eletrodes that are used, better performing and more effective design of the device and for example the current source can be done. By integrating a module which measures the current which goes into the tissue and the voltage drop over the tissue at different frequencies the (frequency dependent) impedance of the ETI can be determined. If this data can also be saved or send to another device via wireless communication, the data can be very useful for future research and future applications.

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List of Symbols and Abbreviations

1N4446 FAIRCHILD 1N4446 Small Signal Diode. 25
2N7000 2N7000G Small Signal MOSFET 200 mAmps, 60 Volts. 24, 25

ADC Analog-to-Digital Converter. 13–15
ASCII American Standard Code for Information Interchange. 16

CCS Continuous Current Stimulation. 19

DAC Digital-to-Analog Converter. 5, 13–15, 19–21, 23

ETI Electrode-Tissue Interface. 19, 32

FQD17P06 FAIRCHILDFQD17P06 / FQU17P06 P-Channel QFET MOSFET. 25

I^2C Inter-Integrated Circuit messaging bus. iii, 10, 13, 14, 16, 17, 37
IC Intergrated Circuit. 32

LCD Liquid-Crystal Display. iii, 5, 9, 11, 13, 14, 16, 17
LED Light-Emitting Diode. 5, 8–11, 13–15
LM358 Texas Instruments LMx58-N Low-Power, Dual-Operational Amplifiers. 24, 25

MAX633 MAXIM INTEGRATED CMOS fixed/adjustable Output Step-Up Switching Regulators. 20
MOSFET Metal-oxide-semiconductor field-effect transistor. 20, 21, 24, 27

NMOS N-channel MOSFET. 20–22, 24–26

op-amp Operational amplifier. 21, 22, 24, 26

PMOS P-channel MOSFET. 21–28, 30
PNP Bipolar junction transisitor with a N-doped semiconductor layer between two layers of P-doped material. 23–25, 27, 28, 30

REValUE REstore Voiding Urinary rEtention. iii, v, 3, 21, 28

SCL serial clock signal in I^2C. 16
SDA serial data signal in I^2C. 16

THAT320 THAT 300 series, Low-Noise Matched Transistor Array ICs. 24, 25, 27, 28

V_{DS} drain-source voltage. 20
V_{GS} Gate-source voltage. 20
V_{TH} Threshold voltage. 20

A | Appendix

A.1. Contact information for SPICE and LPC programming files

Please contact: Prof. dr. ir. W.A. Serdijn, Chairman Bioelectronics (BE), Department of Microelectronics, TU Delft. It also possible to contact on of the authors of this report, but the availability of these persons is not guaranteed.

A.2. I2C protocol for master transmitter mode

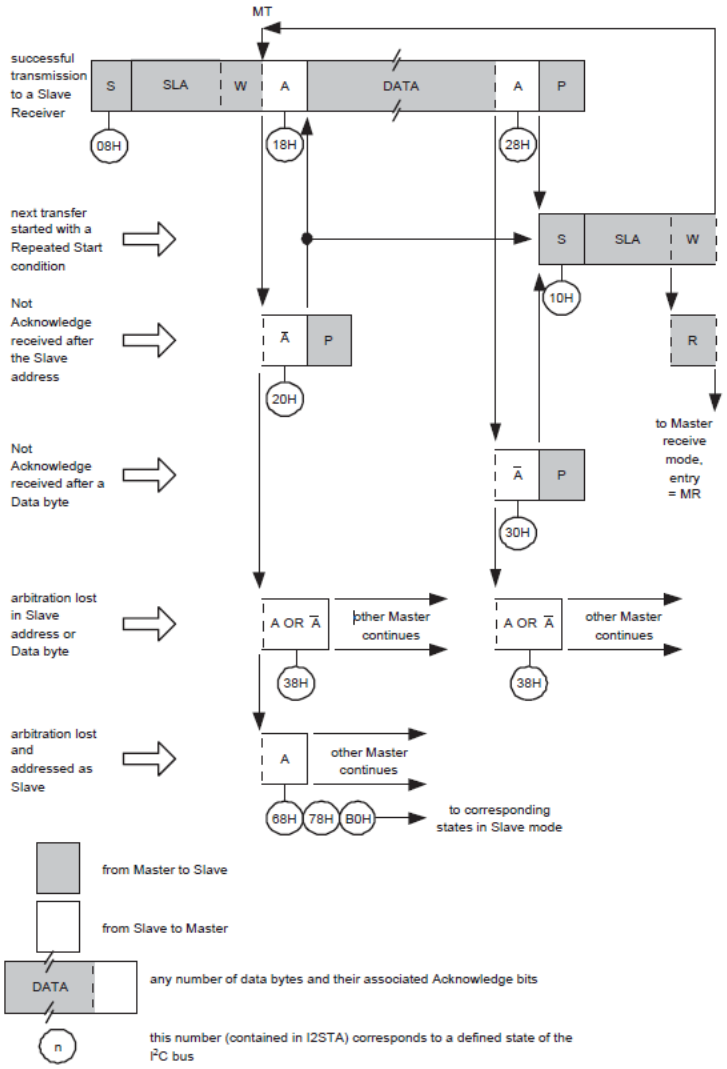

Figure A.1: Image obtain from the datasheet [23]. The implemented logic when the I^2C module is set-up in master transmitting mode. The logic has been obtained from the data sheet of the UM10375 from NXP the processor that drives the used LPC development board [23].

A.3. Detailed simulation for the current source

A detailed simulation is for the simple current mirror topology, Figure A.2, and the proposed topology, Figure A.3. An ideal indication line is added for each V_{ref}.

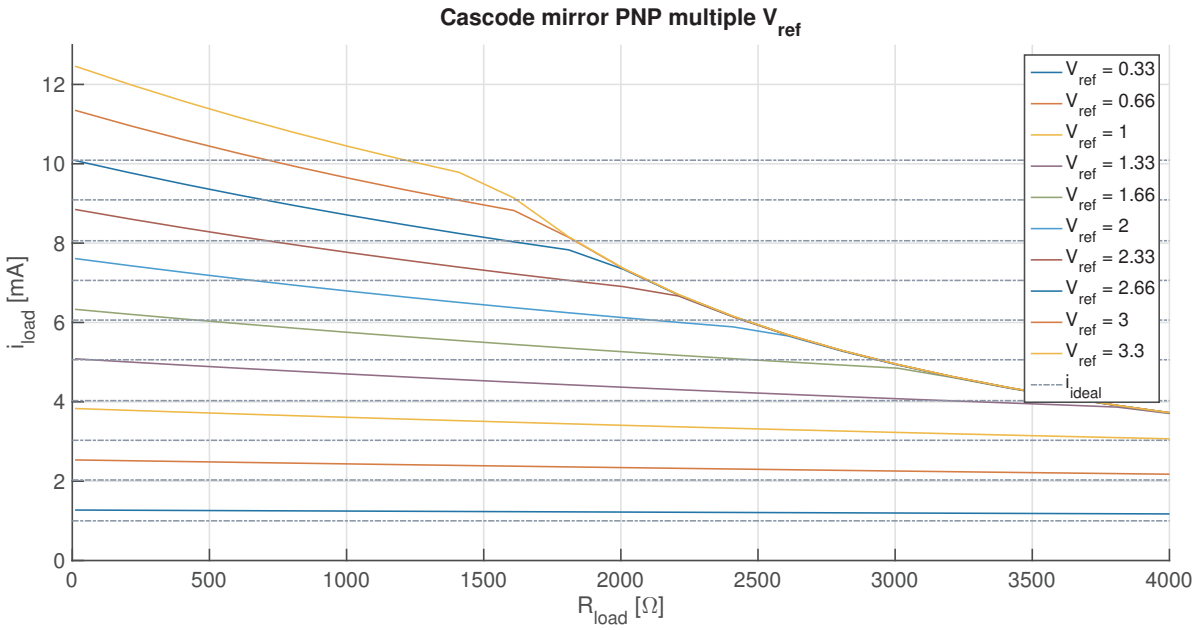

Figure A.2: Simulations done on the simple current mirror topology from Figure 6.4. The simulation is done to determine the effect of different reference voltages, the behaviour behaves as expected, it can be clearly seen that the transistors fall out of saturation mode when it stop behaving linearly. This happens when the line hits the V_{ref} = 3.3 V curve. The i_{ideal} lines are added for comparison to a 'ideal current source'.

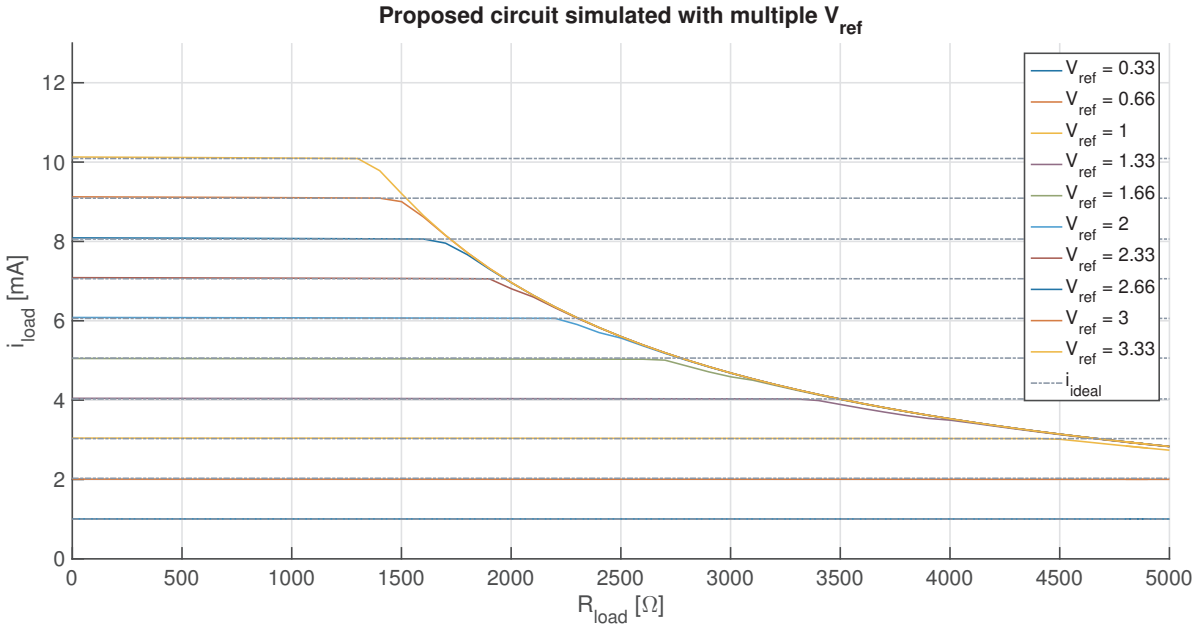

Figure A.3: Simulation done on the proposed current source topology from Figure 6.7. The simulation is done to determine the effect of different reference voltages, the behaviour behaves as expected, it can be clearly seen that the transistors fall out of saturation mode when it stop behaving linearly. This happens when the line hits the V_{ref} = 3.3 V curve. The i_{ideal} lines are added for comparison to a 'ideal current source'.

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