Integrated Circuits for Miniature 3–D Ultrasound Probes
Solutions for the Interconnection Bottleneck

Chen, Z.

DOI
10.4233/uuid:54597354-3ebd-4bee-b5de-4a87e22bceae

Publication date
2020

Document Version
Final published version

Citation (APA)
Chen, Z. (2020). *Integrated Circuits for Miniature 3–D Ultrasound Probes: Solutions for the Interconnection Bottleneck*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:54597354-3ebd-4bee-b5de-4a87e22bceae

Integrated Circuits for Miniature 3-D Ultrasound Probes

Solutions for the Interconnection Bottleneck

Dissertation

for the purpose of obtaining the degree of doctor

at Delft University of Technology

by the authority of the Rector Magnificus prof.dr.ir. T.H.J.J. van der Hagen

chair of the Board for Doctorates

to be defended publicly on

Monday, 21 December 2020 at

at 15:00 o'clock

by

Zhao CHEN

Master of Science in Electrical and Electronic Engineering,

Imperial College London, UK

born in Shandong, P.R. China

This dissertation has been approved by the promotors.

Composition of the doctoral committee:

Rector Magnificus,	chairman
Dr. ir. M.A.P. Pertijs	Delft University of Technology, promotor
Prof. dr. ir. N. de Jong	Delft University of Technology, promotor

Independent members:

Prof. dr. ir. R. Dekker	Delft University of Technology
Prof. dr. S. Cochran	University of Glasgow, United Kingdom
Prof. dr. P. Tortoli	Università degli Studi di Firenze, Italy
Dr. ir. P. Harpe	Eindhoven University of Technology
Dr. ir. M. Verweij	Delft University of Technology

This thesis work is supported by the Dutch Technology Foundation (STW), which is part of the Netherlands Organization for Scientific Research (NWO), and which is partly funded by the Dutch Ministry of Economic Affairs, in the framework of the project number 12405: “MICA: Miniature ultrasound probe for real-time three-dimensional imaging and monitoring of Cardiac interventions”.

To Anqi and my parents

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Echocardiography

Imaging of the cardiovascular system can be traced back to the early 20th century, with the discovery of X-rays [1]. With the arrival of echocardiographic imaging techniques, cardiovascular imaging started to be widely used in clinical practice for the diagnosis of various cardiovascular diseases (CVDs). In the past 20 years, the development of more advanced cardiovascular imaging techniques was significantly promoted by the increasing prevalence of CVDs worldwide [2]. The quality improvements in the visualization of the heart and its vasculature not only allow more accurate diagnosis, but also led to the development of surgical and percutaneous coronary revascularization and thrombolytic therapy, a better understanding in the pathophysiology of CVDs, and the development of better preventive strategies [3].

Among the imaging modalities that have been commonly used in clinical practice, including echocardiography, myocardial perfusion imaging via nuclear scintigraphy, magnetic resonance imaging (MRI) and computed tomography (CT) , echocardiography, which was firstly addressed in the literature in the 1950s, remains the most popular modality today [4]. In echography, ultrasound waves with a frequency of several MHz up to several tens of MHz propagate through the human body and are reflected and scattered by tissue boundaries and tissue inhomogeneities. The acoustic properties as well as the depth information of these reflectors can be derived from the echo signals. The amplitude of the echo signals indicates the difference in the acoustic impedance while the depth information is gained from the time of flight of the echo. Brightness-mode (B-mode) ultrasound images display the anatomical structures by means of brightness levels, based on the received echo strength. The velocities of blood flow and tissue motion can also be displayed in Doppler ultrasound images.

Imaging using ultrasound has several advantages compared to other imaging modalities:

- Safe: echocardiography has an excellent safety record in clinical use since exposure to ultrasound has little or no side effects on the human body. This is a great advantage compared to other imaging modalities like CT, where the exposure to harmful ionizing radiation is required [5], and MRI, which is hardly applicable for patients with iron-based metal implants due to the presence of a strong magnetic field [6];
- Low-cost: echocardiography is widely considered the most cost-effective imaging modality, which is crucial in its role in CVD diagnosis, since over three quarters of CVD-related deaths took place in low- and middle-income countries, according to the data from WHO in 2017 [7];
- Real-time: a frame of an ultrasound image can be generated by about one hundred transmit-receive cycles. A transmit-receive cycle lasts typically 50-200 microseconds, depending on the distance between the ultrasound transducer and the imaging structure [8]. The resulting frame rate is therefore 50-200 frames per second which makes it possible to produce images for real-time diagnosis and monitoring.

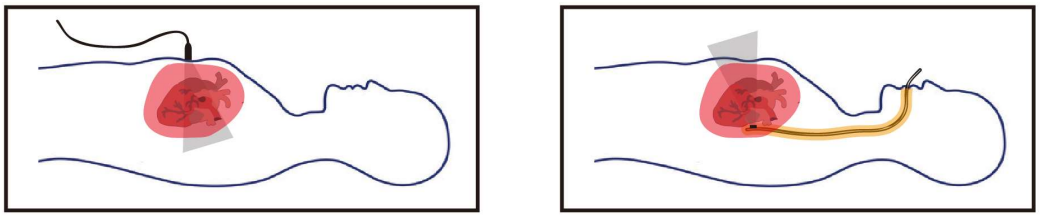


Figure 1. 1 Illustrations of TTE (left) and TEE (right) probes

Two main types of echocardiography are routinely used in clinical practice, characterized by the way they are performed (Fig. 1.1). One is called transthoracic echocardiography (TTE). In TTE, the heart is imaged by means of a hand-held probe placed on the chest of the patient [9]. This non-invasive operating procedure allows it to be used almost unlimitedly without any complications. An alternative approach is called transesophageal echocardiography (TEE), which is typically used when TTE cannot produce definitive images. In TEE, an ultrasound transducer is mounted on the tip of a gastroscopic tube and is guided through the throat of the patient and passed into the esophagus. The TEE probe tips are miniaturized (adult 3-D probes: ~17 × 13.5 × 38 mm) to allow safe insertion into the oropharynx with an acceptable level of discomfort [10]. Since

esophagus is only a few millimetres away from the heart, ultrasound waves are less obstructed by the chest wall, muscles, and ribs compared to TTE, allowing higher frequencies to be used (typically 5 MHz), thus leading to a better visualization of cardiac structures [9]. Images from TEE typically provide better image quality and spatial resolution of various cardiac structures. An obvious inconvenience of TEE is the difficulty of the procedure of guiding the probe into the patient's esophagus, for which often light sedation of the patient is required [11]. TEE outperforms TTE in clinical conditions such as the evaluation of native valvular diseases, the cardiac source of embolism and aortic dissection [12], and is also used as an imaging guidance tool for cardiac interventions [13].

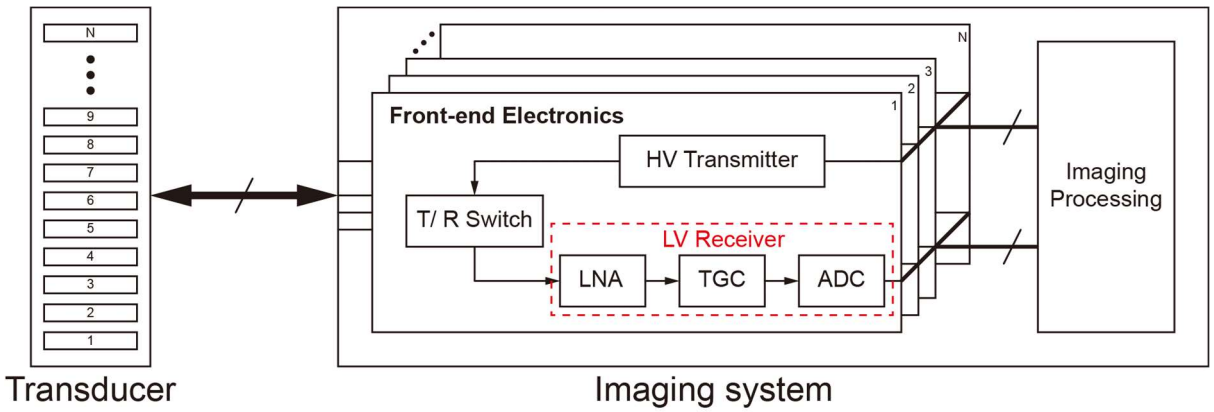


Figure 1. 2 Conventional ultrasound imaging system

The transducer at the tip of a TEE probe is connected to an imaging system via thin coaxial cables. Each transducer element is driven and read out by a front-end electronics channel in the imaging system to perform the pulse-echo operation. The front-end electronics, as shown in Fig. 1.2, typically consist of a high-voltage (HV) transmitter, a low-voltage receiver and a transmit/ receive (TX/ RX) switch [14]. The transmitter drives the transducer element by an excitation signal with an amplitude of several tens of Volt up to 100 V, to generate sufficient acoustic pressure at the penetration depth of interest. At the input of the receiver, a low-noise amplifier (LNA) conditions the weak echo signals with an amplitude of only several micro-Volts. Typically the tissue attenuation of the acoustic waves is also compensated for by time-gain compensation (TGC) in the receiver to reduce the very wide dynamic range of the ultrasound echoes (for instance > 90 dB in TEE application) into the receiver. The TX/ RX switch protects the low-voltage receiver from HV transmission events by disconnecting it from the transducer element during transmission. The conditioned echoes are digitized by analogue-to-digital converters (ADCs) and processed digitally to construct the images.

1.2 Real-time 3-D Echocardiography

While the vast majority of echocardiography devices in use today only provide cross-sectional 2-D images of the heart, it is highly desirable to be able to visualize the 3-D anatomy of the heart, especially when using the images to guide complex cardiac interventions. There are different approaches of realizing that by the current echocardiography probes. One approach is to combine multiple 2-D cross-sectional images of the heart from a 1-D ultrasound transducer array into a volumetric image. This approach requires a physical translation or rotation of a 1-D array, realised by a motor module embedded in the probe or on the imaging system [15]. The 1-D array is linearly swept or rotated spatially such that the generated 2-D imaging planes uniformly sample the whole imaging field of view. Since any inaccuracy in the movement will lead to motion artefacts in the reconstructed 3-D image, high-precision motor modules with pre-calibration are needed. This not only raises the overall cost of the imaging system, but also makes the probe heavy and bulky, which makes it more difficult to operate. More importantly, the number of generated volumes per second is heavily limited by the speed of the mechanical sweeping, thus making such probes incapable of doing real-time 3-D imaging. Missing 3-D motional information of the heart chambers and valves makes this approach less attractive in clinical practice.

An alternative approach of generating 3-D images is to use a 2-D transducer array. By spatially expanding a 1-D array into 2-D, the volumetric information of the imaging object can be acquired by steering the acoustical beam in three dimensions by transducer elements positioned in a 2-D matrix pattern, thus eliminating the need for mechanical sweeping and consequentially enabling real-time 3-D imaging.

The 2-D array approach has clear advantages compared to probes based on a 1-D array. However, fabricating a transducer array and assembling it in a probe, especially in a TEE probe, is challenging in practice. To avoid imaging artefacts caused by insufficient spatial sampling, the pitch of the transducer elements should be at most half a wavelength of the ultrasound wave (or slightly larger if the transducer elements have limited directivity) [16]. For a typical ultrasound frequency of 5 MHz for cardiovascular imaging, the required element pitch is then only 150 μm. In consequence, a 5 mm × 5 mm fully-populated 2-D transducer array has over 1000 elements. This large element count makes it challenging in two ways: first to fabricate such an array with high yield, and second to connect every individual element to the imaging system. For TEE, since

the transducer is placed inside the esophagus, the connections to the imaging system are normally realized by very thin coaxial cables with a length of several meters. The cable connection to a 2-D transducer brings two main issues. First, since the element in a 2-D array is very small, directly connecting an element to a thin coaxial cable of several meters can attenuate the received echo signal significantly, due to the large cable capacitance, thus degrading the signal-to-noise ratio (SNR) of the final image. Second, the number of coaxial cables is limited to a few hundred [17], [18] and is physically limited by the diameter of the gastroscopic tube that needs to accommodate all the cables. For a 2-D array with over 1000 elements, placing the same amount of coaxial cables in the tube is impossible.

Besides the challenges of obtaining real-time 3-D echocardiographic imaging from TEE probes, device miniaturization becomes more and more demanding since the versatility of performing TEE diagnosis in clinical practice is greatly limited by the physical dimensions of the probes. Firstly, the duration of a TEE procedure cannot be very long due to the patient's discomfort, thus making it unsuitable for long-term monitoring. More importantly, the large probe size makes it unsuitable for use in neonatal and pediatric patients.

Significant technology development has happened in recent years on both probe fabrication with 2-D arrays as well as the device miniaturization. A number of commercially available TEE probes like X7-2t (Philips Ultrasound, Bothell, WA), V5M TEE (Siemens Healthcare GmbH, Erlangen, Germany) and 6VT-D (General Electric Healthcare, Amersham, UK) are capable of producing real-time 3-D images by adopting 2-D transducers. However, these devices are still restricted to use in adults due to their physical dimensions. A micro-TEE probe (μTEE: Oldelft Ultrasound, Delft, the Netherlands) was introduced for neonatal and pediatric patients, but this probe is only capable of producing real-time 2-D images. However, a real-time 3-D imaging device with 2-D transducers inside a miniaturized TEE probe is not yet commercially available.

1.3 ASICs for Echocardiography

The challenges of realizing a new generation of miniaturized 3-D TEE probes can be addressed by implementing a miniaturized "imaging system" next to the transducer in the probe tip. This can be realized by leveraging deep-sub-micron integrated circuit (IC) technology, which has led a revolution in the market of

consumer electronics in the past 20 years. The in-probe "imaging system", which is presented as one or multiple application-specific integrated circuits (ASICs), should be capable of:

- conditioning the received weak echo signals;
- reducing the number of channels between the transducer array and an external imaging system that require cable connections;
- driving the long coaxial cables.

Integrating ASICs in the tip of a probe is promising to mitigate the interconnect bottleneck between the transducer and the imaging system; unavoidably, it introduces additional challenges to the probe design, as will be discussed in the following section.

1.3.1 Transducer-to-ASIC Integration

Although an ASIC is capable of relaxing the requirements of the interconnect between the probe head and the system, dense interconnect still remains between the transducer and the ASIC, due to the large number of elements in a 2-D array. One approach of realizing the transducer-to-ASIC interconnect is to flip-chip bond the transducer and the ASICs side-by-side on a common substrate, i.e. a printed circuit board (PCB); then the transducer elements can be connected one-to-one to the ASIC inputs via PCB routing traces (Fig. 1.3(a)) [19], [20]. This method, in principle allows multiple ASICs to be connected to the transducer, potentially relaxing the area constraint of the ASIC design by decoupling the pitch of the transducer array from the pitch of the circuitry on the ASIC. However, in order to distribute the routings of the centre elements, PCB technologies with very fine-pitch copper traces are essential. Moreover, long interconnect routings can add non-negligible parasitic capacitance to the small elements, causing SNR degradation.

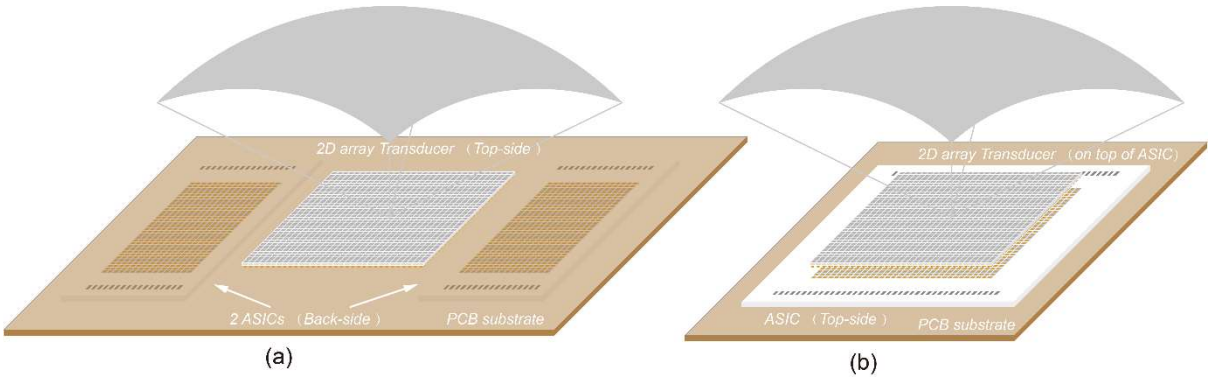


Figure 1. 3 (a) Illustration of side-by-side integration: 2 ASICs are flip-chip bonded on the back-side of a PCB substrate while a 2-D array transducer is flip-chip bonded on the top-side of the PCB; (b) Illustration of pitch-matched integration: an ASIC is wire-bonded on the top-side of a PCB substrate while a 2-D array transducer is stacked on top of the ASIC.

Another transducer-to-ASIC integration method is a pitch-matched vertical integration. This method requires the interconnect pads of the ASIC to be patterned with the same pitch as the transducer elements (Fig. 1.3(b)). Once the transducer electrodes are vertically aligned to the pads on the ASIC, element connections can be created by short vertical contacts, eliminating the parasitic capacitance due to the horizontal routing distribution [21]–[23]. Vertically stacking the transducer and ASIC is also beneficial to minimize the size of the probe head, thus making it more attractive than the first approach.

Pitch-matched integration can be realized by flip-chip bonding the well-aligned transducer and ASIC on both sides of an interposer layer, for instance a flex PCB and vertical connections can be created by vias on the flex [24]. An alternative solution proposed in [25] allows a matrix transducer to be directly mounted and constructed on top of an ASIC with an array of pitch-matched bond-pads by utilizing a custom metallic interconnect layer. Recently the rapid development of micro-machined ultrasound transducer (MUT) devices, for instance, capacitive micro-machined ultrasound transducers (cMUTs) [26] or piezoelectrical micro-machined ultrasound transducers (pMUTs) [27], which is greatly motivated by their compatibility with IC technology, enables the solution of direct integration of transducer and ASIC on one silicon die [28]. The single-die solution minimizes the parasitic capacitance due to the interconnect which is realized in the back-end metallization process of the standard IC fabrication flow.

1.3.2 Area and Power-Consumption Constraints

Though vertical integration is appealing to improve the signal integrity and minimize the size of the probe head, the layout of the ASIC must be pitch-

matched to the layout of the transducer. Given an element pitch of 150 μm for 5 MHz transducers, the electronics of an element, typically consisting of a HV transmitter, a T/R switch and a low-noise amplifier (LNA), must be squeezed in an area of 0.225 mm^2 which is very challenging for the ASIC design.

The ASICs, as additional blocks integrated in the probe head, inevitably increase the power dissipation in the probe head. Excessive power dissipation in the probe head during long-term monitoring will raise the local temperature inside the patient, and eventually may cause tissue overheating or other thermal damage. Though detailed guidelines on the power dissipation of a TEE probe cannot be found, the maximum temperature rise due to the power dissipation in both transducer and electronics should comply with FDA regulations [29]. With reference to the power dissipation of an off-the-shelf 2-D TEE probe, the maximally allowed power dissipation is estimated as 1.0 W [25], thus leading to a power budget of about 1 mW per element for a 3-D probe with a 1000-element 2-D transducer. This stringent power requirement motivates the need for power-efficient ASIC design.

1.4 Cable Count Reduction Techniques

Processing signals and communicating with an imaging system via a realistic number of cables in the probe is the key role of the ASIC. Ideally, techniques that reduce cable count should be easy to implement, not affect the volume rate and introduce minimum image quality degradation. Substantial research efforts have been made in recent years to address the cable count issue for miniaturized ultrasound probes.

1.4.1 Analogue multiplexing

Analogue multiplexing has been widely studied as an effective solution to reduce cable count and electronics complexity [30]–[32]. Both intravascular ultrasound (IVUS) probes described in [33] and [34] realize a 64-to-1 cable count reduction in receive by only connecting 1 of 64 elements to the receive path in a pulse-echo period, thus allowing an implementation of synthetic-aperture imaging by acquiring the received echoes of all the elements in 64 successive pulse-echo sequences. This approach achieves a high reduction factor and greatly simplifies the frond-end circuit design. However, the multiple successive

acquisitions cause a volume-rate reduction, which makes real-time imaging more difficult when a deeper penetration depth is required.

1.4.2 Sparse array

Selecting and connecting a limited number of elements at irregularly-spaced or random locations instead of all the elements on a fully populated 2-D array to the imaging system has also been studied as an effective approach to reduce the number of cables [35]–[37]. A drawback of such sparse arrays is that the reduced number of elements will inevitably reduce the transmitted acoustic energy, thus causing a SNR degradation in the received echoes. Moreover, the side-lobe levels of sparse arrays increase as the number of elements decreases. Both the reduction of the SNR and the increase of the side-lobe level limit the final image quality.

1.4.3 Subarray beamforming

Moving the beamforming function from the imaging system to the probe is considered as one of the most practical methods to reduce cable count. Beamforming typically refers to techniques that construct acoustic beams by combining signals of multiple elements in a transducer, and is a fundamental signal processing procedure in ultrasound imaging. The most well-known beamforming technique is called delay-and-sum (DAS) beamforming. In transmit, DAS operation applies individual time delays to the electrical transmit signals of each element, thus allowing the generated acoustic waves of the elements to focus at specific points in space or steer to certain angles (Fig. 4). Similarly, in receive, by applying a proper set of time delays, the received echo signals that are reflected from the same points can be constructively added, enhancing the SNR of the weak echo signals (Fig. 1.4).

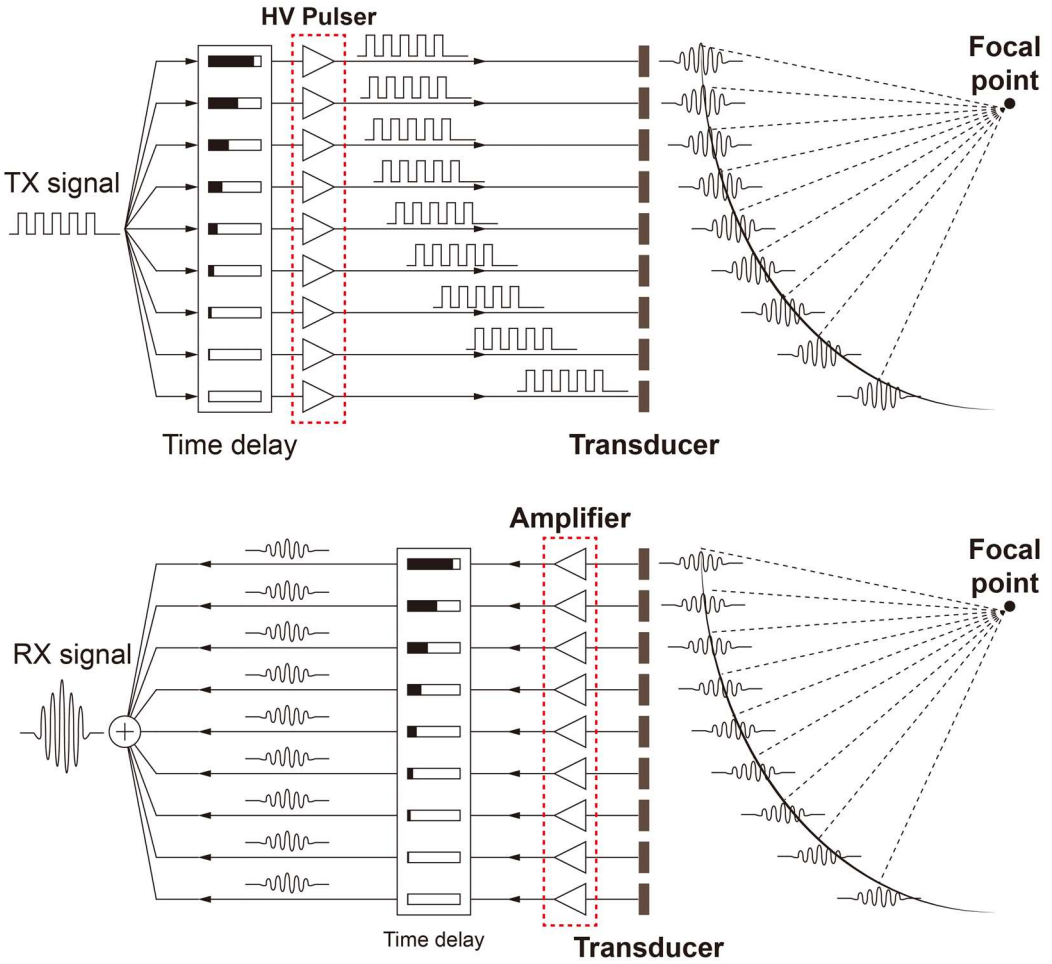


Figure 1. 4 Illustrations of DAS beamforming operations for TX (top) and RX (bottom)

An in-probe transmit circuit can be implemented by a transmit beamformer that drives high-voltage pulsers. Realizing a wide range of time delays for transmit in a probe is relatively easy since the delay can be implemented in the digital domain. Time delays equal to integer multiples of a clock period can be derived from a synchronously clocked low-voltage digital circuit. However, it is very challenging to fit a HV pulser within the small area of an element since HV metal-oxide-semiconductor (MOS) transistor devices in IC technologies typically have lateral dimensions of tens of micrometres in order to sustain a large voltage range [38], [39]. Besides the area constraint, another drawback of this approach is the high-power consumption. Since the transducer elements need to be driven by the HV pulsers in the probe, the in-probe power dissipation inevitably increases compared to the case where the elements are driven by pulsers in the imaging system.

In contrast with the transmit signals, the received echo signals are weak analogue signals. Time delay realization in the analogue domain is subject to

trade-offs among area, power consumption and the maximum achievable delay. As the required maximum delay increases proportionally with the size of the aperture, implementing analogue beamforming for a 2-D array with 1000+ elements would lead to unacceptable hardware cost and hence is not applicable for an in-probe design. Digitizing the analogue echo signals to utilize the simplicity of realizing time delays digitally is an obvious solution for receive beamforming. However, this solution has long been considered impractical due to the need for implementing an ADC for every element [40]. The stringent power and area requirements of the ASIC in a TEE probe are far beyond the performance of the prior-art ultrasound ADC designs. A more practical solution to implement the in-probe receive beamforming is to utilize the concept of subarray beamforming proposed in [41]. A fully-populated 2-D array is divided into identical subarrays with much smaller feature size, thus decreasing the required maximum time delays within each subarray and allowing the implementation of in-probe beamformers for every subarray. A second-stage beamforming will then be applied to the pre-beamformed subarray outputs on the system side which can provide the required larger time delays (Fig. 1.5). Subarray beamforming makes cable count reduction possible with a factor of about 10 with almost no image quality degradation [42]. The feasibility of applying subarray beamforming for a 2-D TEE probe then depends on a power and area efficient implementation of the analogue beamformer circuit.

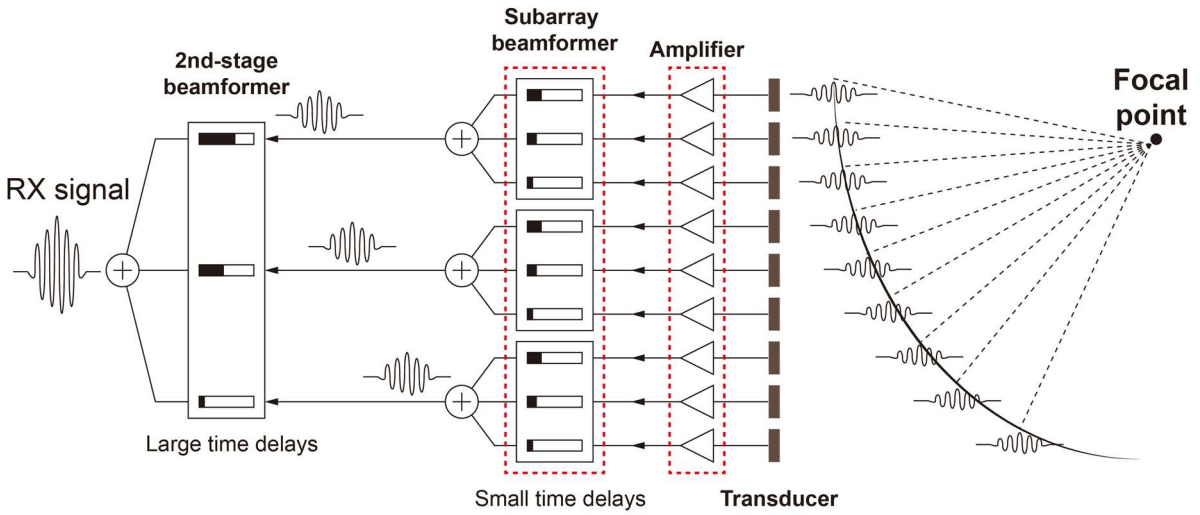


Figure 1. 5 Illustrations of DAS RX subarray beamforming operations

1.4.4 Time/ frequency division multiplexing

To reduce the cable count in reception, efforts have also been made in exploring the maximum capacity of the coaxial cables [32-35]. In [43], the

received echoes from 8 channels are oversampled at 200 MHz and time-multiplexed onto one coaxial cable. The operation principle of this time-division multiplexing (TDM) technique is shown in Fig. 1.6. A similar approach using frequency-division multiplexing (FDM) is presented in [44]. Echoes from 8 channels are combined onto a coaxial cable by modulating them to different carrier frequencies within the bandwidth of the cables (Fig. 1.7). These approaches allow all the raw echo signals of the 2-D array to be captured in the imaging system, thus not causing any compromises in volume rate. However, the limited bandwidth and transmission-line effect of the thin coaxial cable will introduce significant channel-to-channel crosstalk and distortion to the recovered signals [45]. In order to improve the signal integrity, complex equalization is typically required in the imaging system to compensate for the nonidealities of the cables [46]. Moreover, the number of element outputs merged onto one cable should also be limited, meaning a less-effective cable count reduction.

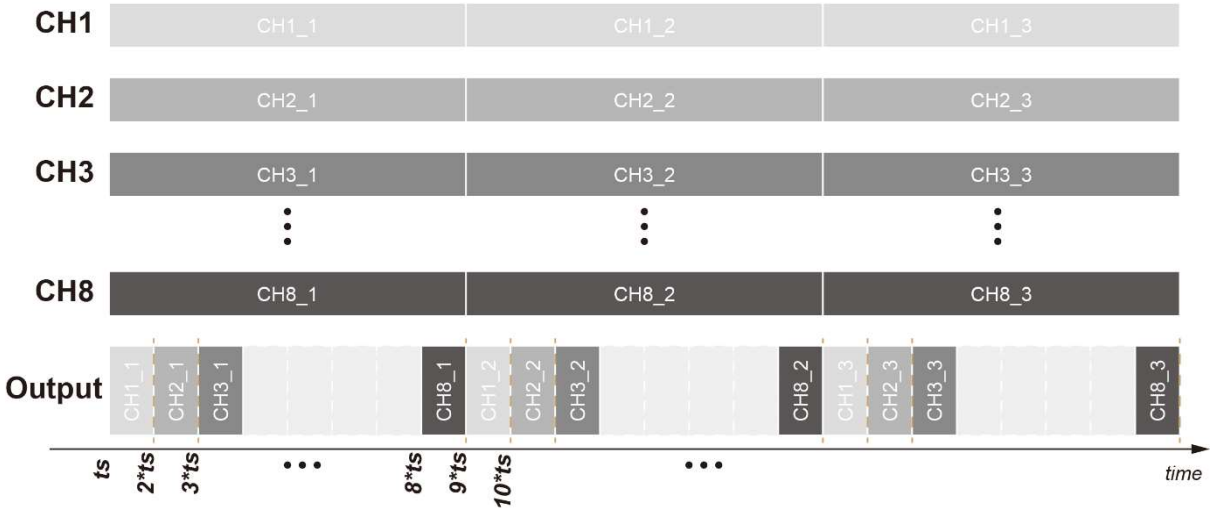


Figure 1. 6 Operating principle of time-division multiplexing over 8 channels

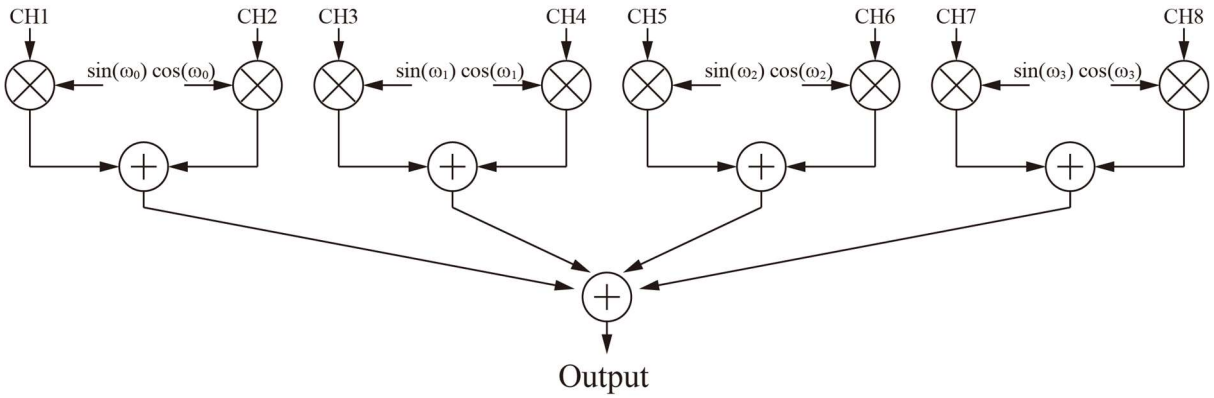


Figure 1. 7 Operating principle of frequency-division multiplexing over 8 channels

The impact of the cable's nonidealities on the signal integrity can be minimized if the echo signals on the cables are in digital format, due to the inherent high immunity to noise, crosstalk and other environment interferences of digital signals. Applying approaches such as TDM on digitized echo signals retains the benefit of fully utilizing the cable capacity without sacrificing the signal integrity, compared to its analogue counterpart. However, similar to the in-probe digital receive beamforming approach, it requires the implementation of in-probe ADCs. Moreover, for a TEE probe with a transducer frequency of several MHz and an echo-signal instantaneous dynamic range of over 50 dB, the digitized echo signal should be serially transmitted at a speed of several hundred Mbit/s. Combining echo signals of multiple elements would require a datalink circuit operating at a speed of several Gbits/s. Off-the-shelf discrete datalink ICs for standard telecommunications can easily run up to several Gbits/s or even higher. However the excessive power consumption, which is dissipated to achieve excellent communication quality (typically quantified by the bit-error-rate (BER)) makes these ICs unsuitable to be merged into the ASIC in the probe. Potentially lower power consumption can be achieved by relaxing the BER, but the impact of BER on the quality of ultrasound images has not been investigated yet. The lack of a BER requirement for digitized echo signals may prevent the optimization of the in-probe datalink design, thus making the feasibility of utilizing in-probe digitization for cable count reduction challenging.

In-probe digitization also enables data communication via optical links, which typically outperform electrical cables for high-speed data communication [47]. A preliminary study in [48] has proposed the concept of implementing a high-speed optical data link in the guidewire of an IVUS catheter. While this paper, as a first step, successfully demonstrates the optical transmission of a 10 MHz clock signal, the size of the vertical-cavity surface-emitting laser (VCSEL), which functions as an electrical-to-optical converter, is too large for the IVUS guidewire. Though optical communication seems to be very promising to address the interconnect issue in TEE probes with in-probe digitization, the challenge of assembling optical modules in the probe head remains to be tackled.

1.5 Research Contributions and Thesis Outline

Motivated by the development of miniaturized 3-D TEE probes, in this research, various IC techniques, including low-power area-efficient subarray beamforming and digital TDM are proposed to tackle the design challenges of in-

probe ASICs capable of reducing the interconnect cable count. However, the application of these techniques is not limited to only the design of TEE probes and can be easily extended to the design of other ultrasound probes, for instance intracardiac echocardiography (ICE) probes and IVUS probes, which are facing similar miniaturization challenges with an increased number of transducer elements to enhance imaging quality [24], [33], [43]. Besides effectively simplifying the interconnect between the transducer and the imaging system, the proposed circuit techniques allow the ASIC to be implemented with affordable hardware costs (mainly power consumption and area), as well as an affordable impact on the quality of the final ultrasound images. Such impact on the ultrasound image quality is also studied within the scope of this thesis.

The organization of this thesis is as follows.

In chapter 2, a front-end ASIC with low power analogue subarray beamformer circuits designed for a 32 × 32 PZT transducer is presented.

In chapter 3, a receive ASIC with in-probe digitization and digital TDM is presented to further reduce the cable count compared to analogue subarray beamforming.

In chapter 4, a quantitative study of the impact of bit errors in digitized RF data on ultrasound image quality is presented, to form a guideline for the design of a digital datalink connecting the probe to an imaging system, balancing the trade-off among power consumption, BER and cable count.

In chapter 5, a transmit ASIC is proposed to further reduce the transmit cable count while maintaining good power efficiency compared to conventional HV pulsers.

References

[1] M. AlGhatrif and J. Lindsay, “A brief review: history to understand fundamentals of electrocardiography,” *J. Community Hosp. Intern. Med. Perspect.*, vol. 2, no. 1, p. 14383, 2012.

[2] “Cardiovascular diseases (CVDs).” [Online]. Available: https://www.who.int/news-room/fact-sheets/detail/cardiovascular-diseases-(cvds). [Accessed: 26-May-2020].

[3] S. Wann and J. Tunio, "Current challenges and future directions in cardiac imaging," *J. Saudi Hear. Assoc.*, vol. 22, no. 3, pp. 121–124, 2010.

[4] I. Edler and K. Lindström, "The history of echocardiography," *Ultrasound Med. Biol.*, vol. 30, no. 12, pp. 1565–1644, 2004.

[5] T. C. Gerber, B. Kantor, and C. H. McCollough, "Radiation Dose and Safety in Cardiac Computed Tomography," *Cardiol. Clin.*, vol. 27, no. 4, pp. 665–677, 2009.

[6] P. Nordbeck *et al.*, "Measuring RF-induced currents inside implants: Impact of device configuration on MRI safety of cardiac pacemaker leads," *Magn. Reson. Med.*, vol. 61, no. 3, pp. 570–578, 2009.

[7] T. A. Gaziano, A. Bitton, S. Anand, S. Abrahams-Gessel, and A. Murphy, "Growing Epidemic of Coronary Heart Disease in Low- and Middle-Income Countries," *Curr. Probl. Cardiol.*, vol. 35, no. 2, pp. 72–115, 2010.

[8] T. Szabo, *Diagnostic Ultrasound Imaging—Inside Out*, 2nd Editio. Elsevier Inc., 2004.

[9] R. Rehman and A. N. Makaryus, *Cardiac Imaging*. StatPearls Publishing, Treasure Island (FL), 2019.

[10] J. Mathew, M. Swaminathan, and C. Ayoub, *Clinical Manual and Review of Transesophageal Echocardiography*, 3rd editio. McGraw-Hill Education - Europe, 2019.

[11] O. Khalid, R. Srivastava, A. Mulhall, A. Paladugu, M. Stoddard, and S. Lippmann, "Conscious sedation: for a TEE, is it always required?," *Echocardiography*, vol. 27, no. 1, pp. 74–76, Jan. 2010.

[12] B. E. Mirbach, "Heart Disease, A Textbook of Cardiovascular Medicine," *Chest*, vol. 81, no. 2, p. 45, Feb. 1982.

[13] M. E. Van Der Velde and S. B. Perry, "Transesophageal Echocardiography During Interventional Catheterization in Congenital Heart Disease.," *Echocardiography*, vol. 14, no. 5, pp. 513–528, Sep. 1997.

[14] K. Iniewski, *Medical Imaging: Principles, Detectors, and Electronics*, 1st Editio. Wiley-Interscience, 2009.

[15] P. A. Picot, D. W. Rickey, R. Mitchell, R. N. Rankin, and A. Fenster, "Three-dimensional colour doppler imaging," *Ultrasound Med. Biol.*, vol. 19, no. 2, pp. 95–104, 1993.

[16] R. S. C. Cobbold, *Foundations of biomedical ultrasound*. New York: Oxford University Press, 2007.

[17] S. Blaak, C. T. Lancée, J. G. Bosch, C. Prins, A. F. W. van der Steen, and

N. de Jong, “A matrix transducer for 3D Transesophageal Echocardiography with a separate transmit and receive subarray,” in *2011 IEEE International Ultrasonics Symposium*, 2011, pp. 2341–2344.

[18] Y. Katsube *et al.*, “Single-chip 3072ch 2D array IC with RX analog and all-digital TX beamformer for 3D ultrasound imaging,” *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 60, pp. 458–459, 2017.

[19] M. W. Rashid *et al.*, “Front-end electronics for cable reduction in Intracardiac Echocardiography (ICE) catheters,” in *2016 IEEE International Ultrasonics Symposium (IUS)*, 2016, pp. 1–4.

[20] M. Sautto *et al.*, “A CMUT transceiver front-end with 100-V TX driver and 1-mW low-noise capacitive feedback RX amplifier in BCD-SOI technology,” in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, 2014, pp. 407–410.

[21] M. C. Chen *et al.*, “A pixel pitch-matched ultrasound receiver for 3-d photoacoustic imaging with integrated delta-sigma beamformer in 28-nm UTBB FD-SOI,” *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2843–2856, 2017.

[22] I. O. Wygant *et al.*, “An integrated circuit with transmit beamforming flip-chip bonded to a 2-D CMUT array for 3-D ultrasound imaging,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 56, no. 10, pp. 2145–2156, 2009.

[23] E. Kang *et al.*, “23.6 A 2pA/√Hz Transimpedance Amplifier for Miniature Ultrasound Probes with 36dB Continuous-Time Gain Compensation,” in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020, pp. 354–356.

[24] D. Wildes *et al.*, “4-D ICE: A 2-D Array Transducer With Integrated ASIC in a 10-Fr Catheter for Real-Time 3-D Intracardiac Echocardiography,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 63, no. 12, pp. 2159–2173, 2016.

[25] C. Chen *et al.*, “A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 63, no. 1, pp. 47–59, 2016.

[26] M. I. Haller and B. T. Khuri-Yakub, “A surface micromachined electrostatic ultrasonic air transducer,” in *1994 Proceedings of IEEE Ultrasonics Symposium*, 1994, vol. 2, pp. 1241–1244 vol.2.

[27] M. Royer, J. O. Holmen, M. A. Wurm, O. S. Aadland, and M. Glenn, “ZnO on Si integrated acoustic sensor,” *Sensors and Actuators*, vol. 4, pp. 357–362, 1983.

[28] G. Jung *et al.*, "Single-Chip Reduced-Wire CMUT-on-CMOS System for Intracardiac Echocardiography," in *2018 IEEE International Ultrasonics Symposium (IUS)*, 2018, pp. 1–4.

[29] FDA, "Marketing Clearance of Diagnostic Ultrasound Systems and Transducers- Guidance for Industry and Food and Drug Administration Staff," *U.S. Dep. Heal. Hum. Serv. Food Drug Adm. Cent. Devices Radiol. Heal.*, pp. 18–34, 2019.

[30] J. T. Yen and S. W. Smith, "Real-time rectilinear 3-D ultrasound using receive mode multiplexing," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 51, no. 2, pp. 216–226, 2004.

[31] D. F. Lemmerhirt, X. Cheng, O. D. Kripfgans, M. Zhang, and J. B. Fowlkes, "A fully-populated 32×32 CMUT-in-CMOS array," in *2010 IEEE International Ultrasonics Symposium*, 2010, pp. 559–562.

[32] M. J. Fuller, K. Ranganathan, Shiwei Zhou, T. N. Blalock, J. A. Hossack, and W. F. Walker, "Portable, low-cost medical ultrasound device prototype," in *IEEE Ultrasonics Symposium, 2004*, 2004, vol. 1, pp. 106-109 Vol.1.

[33] M. Tan *et al.*, "A front-end ASIC with high-voltage transmit switching and receive digitization for 3-D forward-looking intravascular ultrasound imaging," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2284–2297, 2018.

[34] D. Van Willigen *et al.*, "ASIC Design for a Single-Cable 64-Element Ultrasound Probe," in *2018 IEEE International Ultrasonics Symposium (IUS)*, 2018, pp. 1–4.

[35] E. Roux *et al.*, 2-D Ultrasound Sparse Arrays Multi-Depth Radiation Optimization Using Simulated Annealing and Spiral-Array Inspired Energy Functions, *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 63, no.12, pp. 2138-2149, 2016.

[36] A. Austeng and S. Holm, "Sparse 2-D arrays for 3-D phased array imaging - design methods," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 49, no. 8, pp. 1073–1086, 2002.

[37] A.Ramalli, et al., Density-tapered spiral arrays for ultrasound 3D imaging, *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 62, no. 8, pp. 1580-1588, 2015.

[38] A. Banuaji and H. Cha, "A 15-V Bidirectional Ultrasound Interface Analog Front-End IC for Medical Imaging Using Standard CMOS Technology," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 61, no. 8, pp. 604–608, 2014.

[39] J. Lee *et al.*, "A 5.37mW/Channel Pitch-Matched Ultrasound ASIC with Dynamic-Bit-Shared SAR ADC and 13.2V Charge-Recycling TX in Standard CMOS for Intracardiac Echocardiography," *IEEE Int. Solid-State Circuits Conf.*, vol. 10, no. 4, pp. 2018–2020, 2019.

[40] C. Chen, "Front-End ASICs for 3-D Ultrasound From Beamforming to Digitization", Doctoral thesis, Delft University of Technology, 2018.

[41] B. Savord and R. Solomon, "Fully sampled matrix transducer for real time 3D ultrasonic imaging," in *IEEE Symposium on Ultrasonics*, 2003, pp. 945–953.

[42] D. Bera *et al.*, "Multiline 3D beamforming using micro-beamformed datasets for pediatric transesophageal echocardiography.," *Phys. Med. Biol.*, vol. 63, no. 7, p. 75015, Mar. 2018.

[43] G. Jung *et al.*, "Single-chip reduced-wire active catheter system with programmable transmit beamforming and receive time-division multiplexing for intracardiac echocardiography," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 188–190.

[44] M. W. Rashid, C. Tekes, M. Ghovanloo, and F. L. Degertekin, "Design of frequency-division multiplexing front-end receiver electronics for CMUT-on-CMOS based intracardiac echocardiography," *IEEE Int. Ultrason. Symp.*, vol. 1, pp. 1540–1543, 2014.

[45] Q. Liu, C. Chen, Z. Chang, C. Prins, and M. A. P. Pertijs, "A mixed-signal multiplexing system for cable-count reduction in ultrasound probes," in *2015 IEEE International Ultrasonics Symposium (IUS)*, 2015, pp. 1–4.

[46] T. M. Carpenter, M. W. Rashid, M. Ghovanloo, D. M. J. Cowell, S. Freear, and F. L. Degertekin, "Direct digital demultiplexing of analog TDM signals for cable reduction in ultrasound imaging catheters," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 63, no. 8, pp. 1078–1085, 2016.

[47] C.Sun, et al., "A Monolithically-Integrated Chip-to-Chip Optical Link in Bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 828–844, 2015.

[48] R. Stoute, M. C. Louwerse, J. van Rens, V. A. Henneken, and R. Dekker, "Optical data link assembly for 360 μm diameter IVUS on guidewire imaging devices," in *SENSORS, 2014 IEEE*, 2014, pp. 217–220.

CHAPTER 2

A FRONT-END ASIC WITH SUBARRAY BEAMFORMING INTEGRATED WITH A 32 × 32 PZT MATRIX

*Based on publication: C. Chen, **Z. Chen**, D. Bera, S.B. Raghunathan, M. Shabanimotlagh, E. Noothout, Z.-Y. Chang, J. Ponte, C. Prins, H.J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M.A.P. Pertijs, "A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography", IEEE Journal of Solid State Circuits, vol. 52, no. 4, pp. 994-1006, Apr. 2017.*

2.1 Introduction

Volumetric visualization of the human heart is essential for the accurate diagnosis of cardiovascular diseases and the guidance of interventional cardiac procedures. Echocardiography, which images the heart using ultrasound, has become an indispensable modality in cardiology because it is safe, relatively inexpensive and capable of providing real-time images. Transesophageal echocardiography (TEE), as its name indicates, generates ultrasonic images from the esophagus, by utilizing an ultrasound transducer array mounted at the tip of a gastroscopic tube (Fig. 2.1). Conventionally, the elements of the transducer array are connected using micro-coaxial cables to an external imaging system, where properly-timed high-voltage pulses are generated to transmit an acoustic pulse, and the resulting echoes are recorded and processed to form an image.

2-D TEE probes are widely used in clinical practice. They employ a 1-D phased-array transducer to obtain cross-sectional images of the heart. However, such 2-D images often fall short in providing comprehensive visual information for complex cardiac interventions, such as minimally-invasive valve replacements and septal-defect closures. Appropriate real-time 3-D imaging would be very beneficial for improving the success rate of such procedures [1].

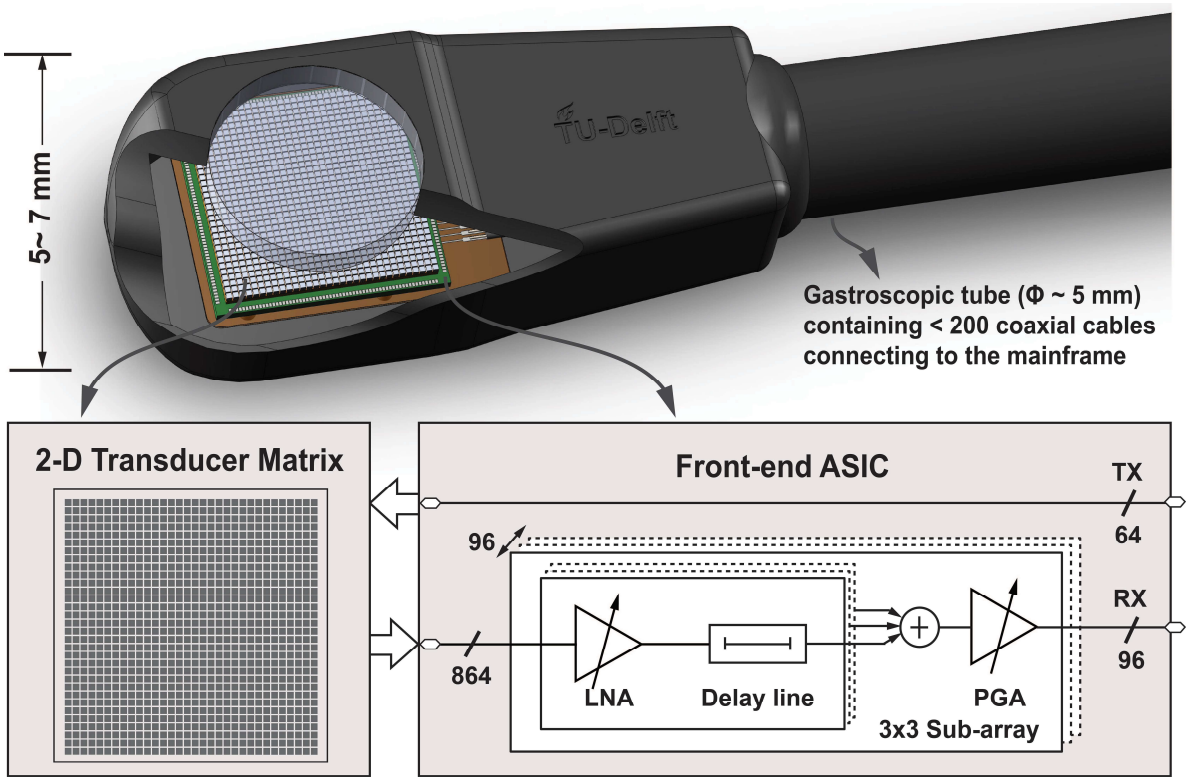


Figure 2. 1 A miniature 3-D TEE probe with a front-end ASIC.

The relatively large probe heads (typically > 10 cm^3) of current 3-D TEE probes cannot be tolerated by the patient during longer procedures (unless general anaesthesia is applied) and are too large for pediatric use. For longer-term monitoring and pediatric use, the volume of the probe tip should be constrained to an upper limit of 1 cm^3, and the tube diameter to 5 ~ 7 mm [2]. To enable real-time 3-D imaging, a 2-D phased array is required. For an array of aperture size $D \times D$, the achievable signal-to-noise ratio (SNR) and the lateral resolution both improve linearly with D. Therefore, it is desirable to make full use of the available array aperture within the probe tip (5 × 5 mm^2). In addition, the pitch of the transducer elements should not exceed half of the acoustic wavelength (λ) to minimize grating lobes and to ensure proper spatial imaging resolution [3]. For a 2-D array with a centre frequency of 5 MHz, this corresponds to a pitch of 150 μm, leading to at least 32 × 32 elements. For a gastroscopic tube with 5 mm inner diameter, the number of micro-coaxial cables (assuming 0.2mm cable outer diameter) that can be accommodated in the tube is limited to about 600, thus making it impossible to wire out all the elements of that 32 × 32 transducer array. Moreover, the number of cables should be kept well below this maximum to prevent the tube from becoming too stiff. Decreasing the aperture size to reduce the number of channels will lead to a significant deterioration in both the SNR

and the lateral resolution. As a result, channel reduction should be performed locally to reduce the number of cables with the aid of miniaturized in-probe electronics [4].

A variety of approaches have been proposed to reduce the cable count in endoscopic and catheter-based ultrasound systems. One approach is to partition part of the beamforming function, which serves to achieve spatial directivity and enhance the SNR. This is conventionally performed in the external imaging system, but can be partially moved into the probe [5, 6]. Time-division multiplexing approaches have been applied in [7, 8] to allow multiple elements to share a single cable. Solutions based on element-switching schemes [9, 10] have also been reported. All these approaches rely on the realization of a front-end ASIC that is closely integrated with the transducer array.

Design of such front-end ASICs is challenging in several aspects. First, the power consumption of the ASIC, which contributes to the overall self-heating of the probe, should be kept below an estimated 1 W [11], to avoid excessive tissue temperature rise [12]. This translates to 1 mW/element for a 1000-element array and is beyond the state-of-the-art of front-end ultrasound ASICs, which consume at least 1.4 mW/element [10, 13, 14]. Another challenge comes from the dense interconnection between the ASIC and the transducer array. Direct transducer-on-chip integration is desired, as it not only helps to get a small form factor, but also reduces the parasitic interconnect capacitance added to each transducer element. This calls for an element-matched ASIC layout, with a pitch identical to that of transducer elements. As a result, a highly compact circuit implementation for the ASIC is called for. Prior works [13, 15] compromised somewhat on the imaging quality by opting for a pitch that exceeds half of the wavelength, which may be acceptable if the resulting grating lobes are sufficiently mitigated by the limited directivity of the transducer elements. Indirect transducer-to-chip integration via interposer PCBs [6, 10] allows the use of a different pitch for the transducer array and the ASIC. However, the limited space within the TEE probe tip precludes this option.

In this chapter, we present a front-end ASIC that is optimized in both system architecture and circuit-level implementation to meet the stringent requirements of 3-D TEE probes [16]. It is directly integrated with an array of 32 × 32 piezoelectric transducer elements, which are split into a transmit and a receive array to facilitate the power and area optimization of the ASIC [17]. The receive elements are further divided into 96 subarrays, each with a switched-capacitor-

based beamformer, to realize a 9-fold cable reduction. Besides, an ultra-low-power LNA architecture [18], which incorporates an inverter-based operational transconductance amplifier (OTA) with a bias scheme tailored for ultrasound imaging, is proposed to increase the power-efficiency of the receive circuitry, while keeping the area compact. In addition to that, a mismatch-scrambling technique is applied to mitigate the effects of mismatch between the beamformer stages, and thus improve the overall dynamic range of the ASIC while receiving. These circuit techniques, while designed for matrix transducers consisting of diced lead zirconate titanate (PZT) transducer elements, are also relevant for other types of ultrasound transducers, such as capacitive micromachined ultrasonic transducers (cMUTs). The functionality of the ASIC as well as the effectiveness of the proposed techniques have been successfully demonstrated by imaging experiments.

This chapter is organized as follows. Section II describes the proposed system architecture. Section III discusses the details of the circuit implementation. Experimental results are presented in Section IV. Conclusions are given at the end of the chapter.

2.2 System Architecture

2.2.1 Transducer Matrix Configuration

In conventional ultrasound probes, each transducer element is used both as transmitter and receiver. A high-voltage CMOS process is then needed to generate the transmit pulses of typically tens of Volts [14]. The integration density of high-voltage processes is generally lower than that of their low-voltage counterparts with the same feature size, which is disadvantageous for ASICs that directly interconnect with 2-D transducer arrays with a tiny element pitch.

In this work, we use an array of 32 × 32 PZT elements with separate transmit and receive elements (Fig. 2.2). An 8 × 8 central subarray is directly wired out to transmit channels in the external imaging system using metal traces in the ASIC that run underneath 96 un-connected elements to bond-pads on the chip's periphery. These traces are not connected to any junctions in the substrate, and can hence support high transmit voltages provided that they are sufficiently spaced to prevent dielectric breakdown and routed in the top metal layers to minimize capacitive coupling to the substrate. All the other 864 elements are

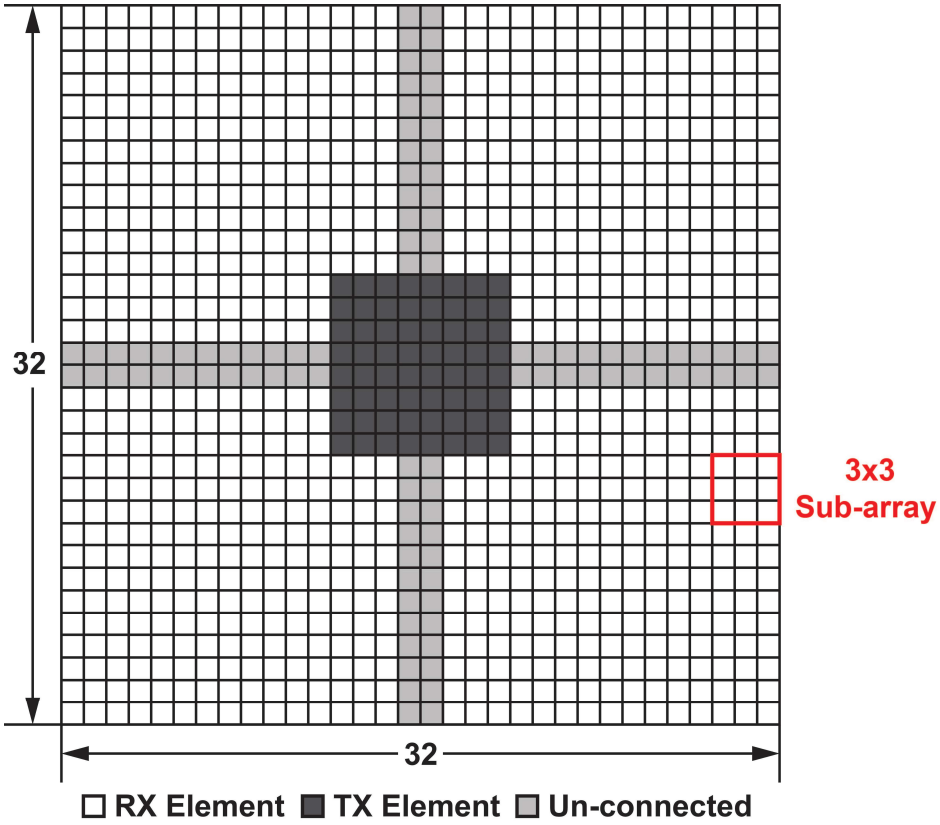


Figure 2. 2 Transducer matrix configuration.

connected directly to on-chip receiver circuits, whose outputs are fed to the imaging system's receive channels.

The use of a small central transmit array helps in reducing the overall cable count as well as obtaining a large opening angle while receiving. With respect to a conventional array configuration in which each transducer element is used for both transmit and receive, our scheme trades lateral resolution for a higher frame rate. In our scanning procedure, the transmitter is used to generate only a few wide beams, illuminating an area that can accommodate a number of parallel receive beams per transmit pulse, thus yielding a high frame rate. Similar to the sparse arrays discussed in section 1.4.2, the smaller number of transmit elements leads to a lower transmitted acoustic energy. This can be partially compensated for by using a higher transmit voltage amplitude. It should be ensured that the generated acoustic pressure is adequate for the target imaging depth. According to our numerical simulations in OnScale (OnScale Inc., 770 Marshall Street Redwood City, CA, USA), 64 elements driven with 100 V pulses should be capable to generate sufficient pressure for an imaging depth up to 10 cm [19]. Moreover, despite the missing elements in the receiver aperture, the point spread function (PSF) is comparable with a fully-populated receiver, as shown by

simulations in [20]. This configuration allows the use of a dense low-voltage CMOS technology, thus saving power and circuit area. Compared to [13], which uses the majority of elements to transmit and a sparse array to receive, it achieves better receiving sensitivity as well as lower side-lobes. Moreover, it also helps to reduce the overall in-probe heat dissipation, as transmit circuits normally consume more power [10].

The transducer array was constructed by dicing a bulk piezoelectrical material (CTS 3203 HD, CTS Corporation, Albuquerque, MN, USA) into a matrix. It is directly mounted on top of the front-end ASIC using the PZT-on-CMOS integration scheme described in [11]. The PZT matrix measures 4.8 mm × 4.8 mm with an element pitch of 150 μm and a dicing kerf width of 20 μm. It was designed for a centre frequency of 5 MHz and a 50% bandwidth (3.75 MHz ~ 6.25 MHz).

2.2.2 Subarray Beamforming in Receive

The cable-count reduction approach that we adopted in this work is to perform partial receive beamforming in the ASIC. The basic principle of ultrasound beamforming is to apply appropriate relative delays to the received signals in such a way that ultrasound waves coming from the focal point arrive simultaneously and can be constructively combined. Full-array beamforming for 32 × 32 transducer elements is impractical for circuit implementation due to the large delay depth required for each element, which is typically a few microseconds. The subarray beamforming scheme [5], also known as “micro-beamforming” [17], mitigates this issue by dividing the beamforming task into two steps. A coarse delay that is common for all elements within one subarray is applied in the external imaging system, while only fine delays for the individual elements (less than 1 μs) is applied by subarray beamformers in the ASIC, which significantly reduces the implementation complexity of the required on-chip delay lines .

The subarray size is determined based on the following concerns. First, in order to keep the symmetry of the beamforming in lateral and elevation directions, a square subarray is desired. Besides, a larger subarray brings a more aggressive cable-count reduction, but comes at the cost of an elevated grating-lobe level and a greater maximum fine delay in the subarray beamformers. We selected a 3 × 3 configuration to achieve a reasonable acoustic imaging quality, while reducing the number of cables by a factor of 9 [21]. Accordingly, the 864 receive elements of the transducer matrix are divided into 96 subarrays and

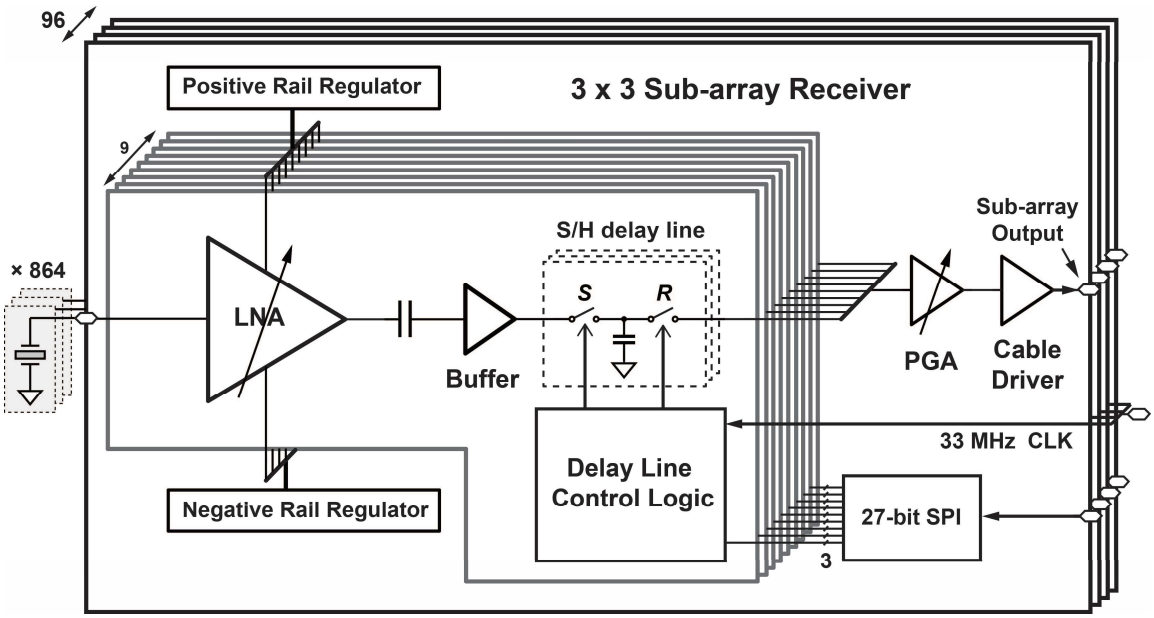


Figure 2. 3 Schematic of the 3 × 3 subarray receiver.

interfaced with 96 subarray receiver circuits in the ASIC.

The fine delays are programmable in steps of 30 ns up to 210 ns, allowing the subarray's directivity to be steered over angles of 0°, ±17°, and ± 37° in both azimuthal and elevation directions [11]. All subarrays can be programmed identically, which is appropriate for far-field beamforming and requires loading of only 9 delay settings into the ASIC, which has a negligible impact on the frame rate. The ASIC is also equipped with a mode in which all subarrays can be programmed individually (i.e. 96 × 9 settings), allowing near-field focusing at the expense of a longer programming time, and hence a slightly slower frame rate.

2.3 Circuit Implementation

Fig. 2.3 shows the schematic of a 3 × 3 subarray receiver. It consists of 9 LNAs, 9 buffers, 9 analogue delay lines, a programmable-gain amplifier (PGA) and a cable driver. The LNA output is AC-coupled to a flipped source follower buffer that drives the analogue delay line. The joint output of all 9 analogue delay lines is then amplified by the PGA. A cable driver buffers the output signal of the PGA to drive the micro-coaxial cable connecting to the imaging system. A local bias circuit (not shown) is implemented within each subarray.

The echo signals received by the transducer elements have a dynamic range of about 80 dB, 40 dB of which is associated with the fact that echoes from deeper

tissue are attenuated more along their propagation path. The gains of the LNA and the PGA are programmable to compensate for this attenuation. The LNA is optimized for a low noise figure (< 3 dB) and provides a voltage gain up to 24 dB, to reduce the impact of noise of the subsequent stages at small signal levels. The gain can be reduced to -12 dB and 6 dB to avoid output saturation at high signal levels. The PGA provides an additional switchable gain with finer steps (0, 6, 12 dB) to interpolate between the gains steps of the LNA. Thus, an overall dynamic range of more than 80 dB, which is sufficient for TEE imaging, can be achieved.

As described in Section I, all the above circuits, along with their biasing and digital control circuits, must be implemented within the area of a 3 × 3 subarray, i.e. 450 µm × 450 µm, while consuming less than 4.5 mW. Dedicated circuit techniques have been applied to meet these requirements, which will be discussed in this section.

2.3.1 LNA

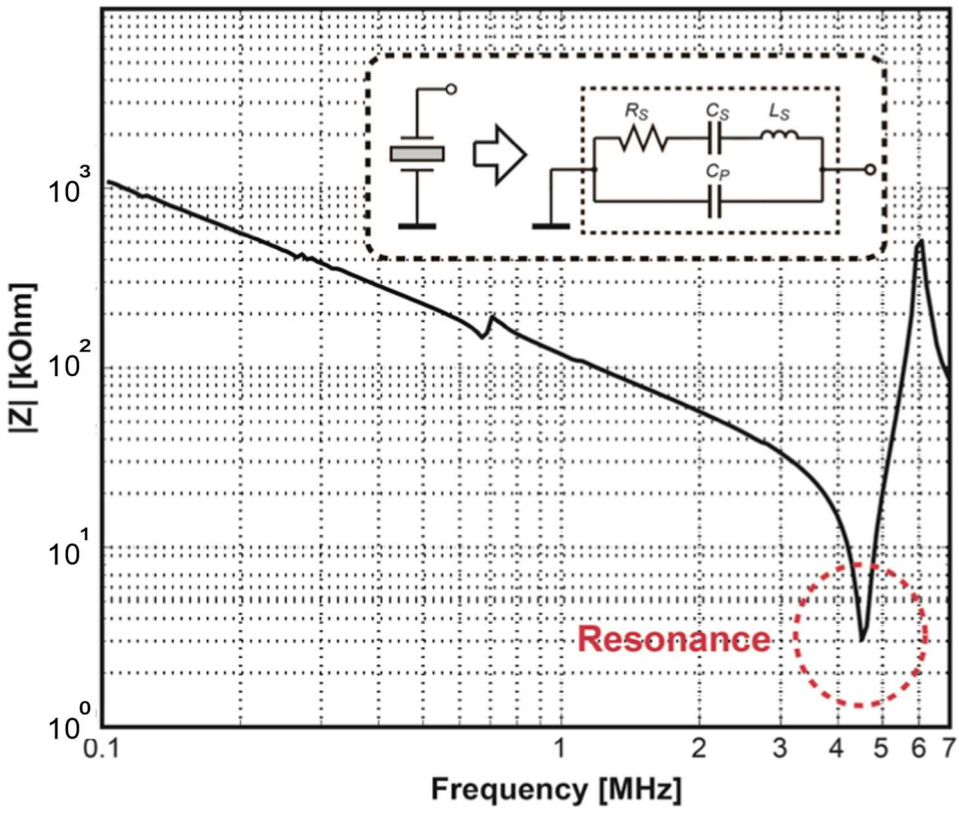


Figure 2. 4 The measured impedance of a 150 µm × 150 µm PZT transducer element and its equivalent electrical model.

The choice of the ultrasound LNA topology is dictated by the electrical impedance of the target transducer. Trans-impedance amplifiers (TIA) are widely

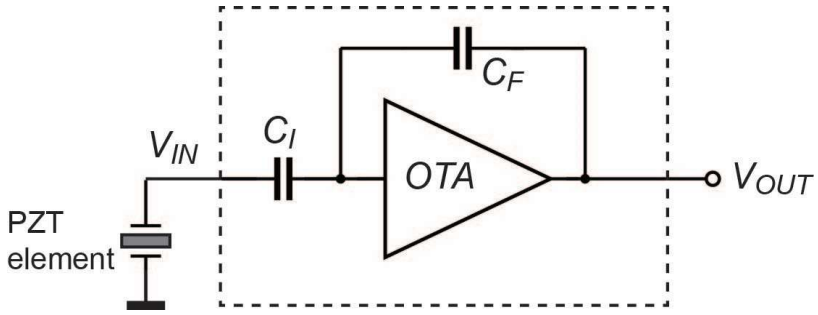


Figure 2. 5 The proposed LNA architecture.

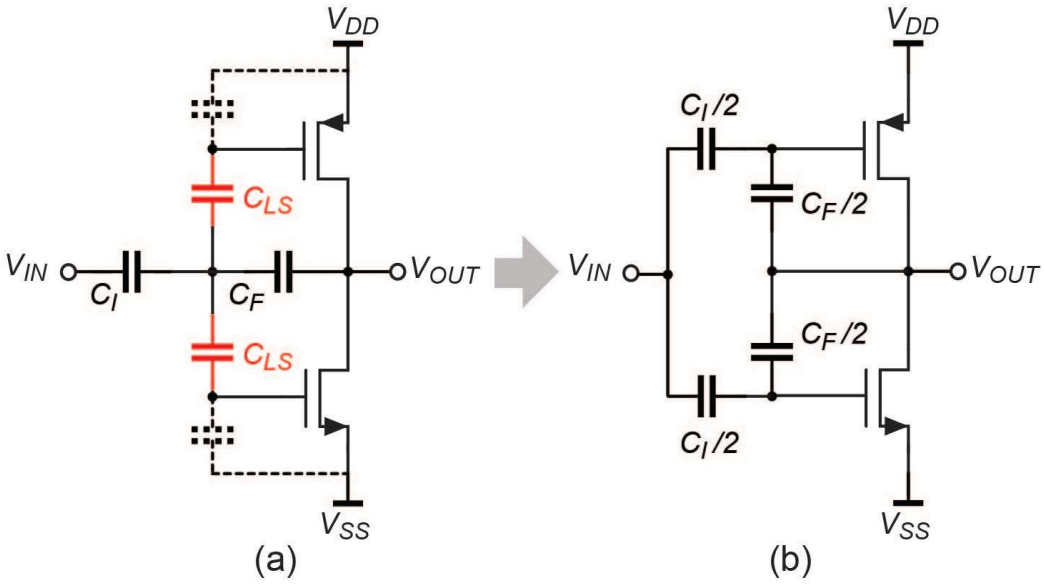


Figure 2. 6 Inverter-based OTA with split-capacitor feedback network.

used in readout ICs for CMUT transducers because of their relatively high impedance [22]. However, a similarly-sized PZT transducer has a much lower impedance around the resonance frequency, typically a couple of kΩs for our transducers (Fig. 2.4). In view of this, the TIA topology falls short in achieving an optimal noise/power trade-off, since creating a low enough input-impedance requires extra power spent on increasing the open-loop gain, rather than on suppressing the input-referred noise [18]. In this work, instead, we use a capacitive-feedback voltage amplifier, shown in Fig. 2.5, which offers a mid-band voltage gain of $A_M = C_I / C_F$. Its input impedance is dictated by the input capacitor C_I and can be easily sized to tens of kΩs within the transducer bandwidth, so as to sense the transducer's voltage rather than its current.

A current-reuse OTA based on a CMOS inverter is employed to enhance the power-efficiency of the LNA. In previous inverter-based designs [23], extra level-shifting capacitors (C_{LS}) are used to independently bias the NMOS and

PMOS transistors, as shown in Fig. 2.6(a). These level-shifting capacitors and the associated parasitic capacitors at the virtual ground node form a capacitive divider, which attenuates the input signal and thus increases the input-referred noise of the LNA. Enlarging C_{LS} helps in reducing this noise penalty, at the cost of increased die area. In this work, the level-shifting capacitors are eliminated by

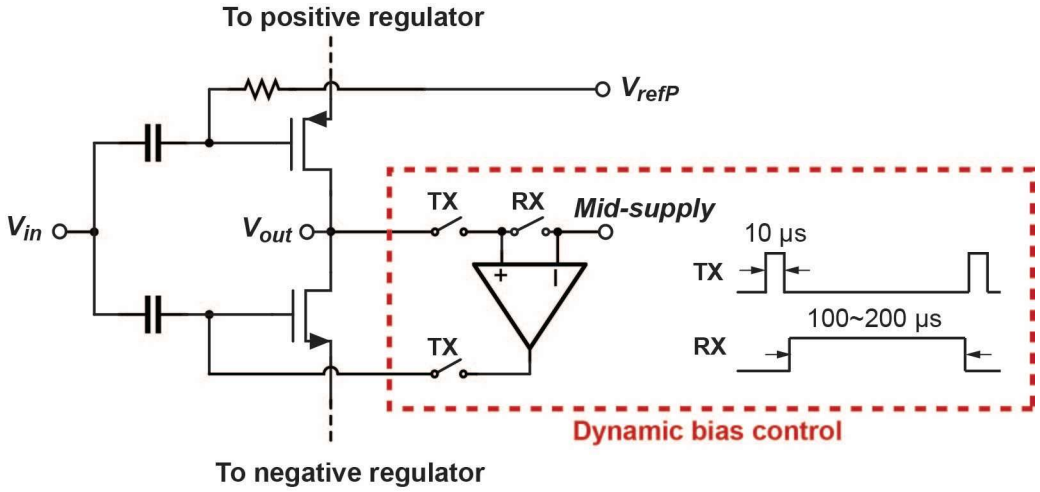


Figure 2. 7 Dynamic bias control scheme.

applying a split-capacitor feedback network [18, 24]. As shown in Fig. 2.6(b), the input bias points for the NMOS and PMOS transistors are de-coupled by splitting the input and feedback capacitors into two equal pairs, which maintains the same mid-band gain C_I / C_F and the same input impedance.

To maximize the output swing, the bias voltage of the inverter-based OTA should be properly defined. This is usually achieved with the aid of a DC control loop, in which a slow auxiliary amplifier keeps the output at the desired operating point [23]. However, such a DC control loop will recover too slowly from disturbances coupled from the metal traces that connect the transmit channels in the external imaging system to the 8 × 8 central array in the ASIC during the transmit phase. Therefore, instead, we dynamically activate the bias control loop in synchronization with the transmit/ receive (TX/ RX) cycles of the ultrasound system, as shown in Fig. 2.7. During the TX phase, the input of the LNA is grounded and the inverter is essentially auto-zeroed, while the auxiliary amplifier drives the gate of the NMOS transistor so as to bias the output at mid-supply. During the RX phase, the auxiliary amplifier is disconnected, and both its inputs are shorted to the mid-supply. Meanwhile, the LNA starts receiving the echo signal by operating at the “memorized” bias points. Given that the typical TX/ RX cycle in cardiac imaging is relatively short, ranging from 100 µs to 200 µs, the bias voltage hardly drifts during the RX phase. The relatively large sizes of

the input transistors (W/L_N = 75/0.2, W/L_P = 60/0.2), needed for flicker-noise reduction, also help to keep the bias voltages stable. The sample-and-hold operation associated with the auto-zeroing causes broadband white noise to be sampled on the gate of the NMOS transistor and held constant during the receive phase. Therefore, it appears as a small offset voltage that is superimposed on the "memorized" bias point during each transmit/receive cycle, and does not deteriorate the in-band noise performance of the LNA. Moreover, it is further filtered out by the AC-coupler following the LNA and has no impact on the bias condition of succeeding stages.

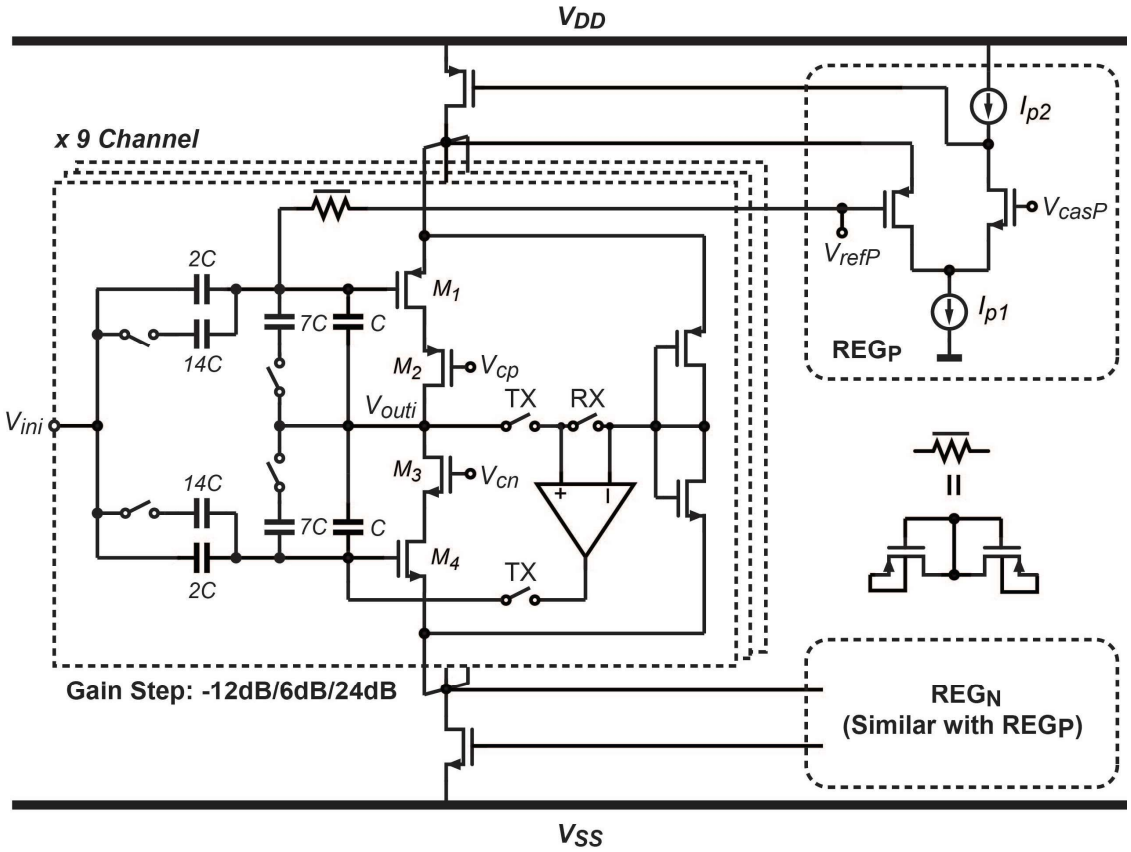


Figure 2. 8 Complete schematic of the LNA.

A well-known down-side of a single-ended inverter-based OTA is its poor power-supply-rejection ratio (PSRR) [25]. As the LNAs are closely integrated with high-frequency digital circuits for beamformer control, the supply line and the ground are inevitably noisy. To improve the PSRR, we generate two internal power rails within each subarray by means of two regulators (REG_P and REG_N in Fig. 2.8) that are shared by the 9 LNAs of a subarray. Given the fact that the loading currents of these regulators are known and approximately constant, their implementation can be kept rather simple to save area. A capacitor-less low-dropout regulator (LDO) based on a super source-follower [26], capable of

providing a PSRR better than 40 dB at 5 MHz, is adopted as the topology for both regulators.

Fig. 2.8 shows the complete schematic of the proposed LNA. The inverter-based OTA is cascoded to ensure an accurate closed-loop gain, and input transistors M_1 and M_4 are biased in weak-inversion to optimize their current-efficiency. The bias voltage of M_1, V_{refP} , which is derived from a diode-connected PMOS transistor via a high-impedance pseudo-resistor, is shared by the input gate of the positive-rail regulator REG_P. Thus, the bias current of the OTA can be defined by the difference of the reference currents ($I_{p1} - I_{p2}$) and the dimension ratio of M_1 and M_{p1}. In each channel, a unity-gain-connected inverter, implemented with long-channel transistors and consuming only 0.4 μA, is connected between the two regulated power rails to generate a mid-supply reference that is approximately 900 mV. The auxiliary amplifier for DC bias control is realized as a simple differential pair. With a current consumption of less than 1 μA, it is capable to settle within the 10 μs TX phase. A switchable capacitive feedback network, involving capacitors 14C and 7C that can be switched in or out under control of digital gain-control inputs of the ASIC, is implemented to provide the mentioned 3 gain levels for dynamic range enhancement. An explicit loading capacitor (not shown in Fig. 2.8) is added at the output of the LNA to limit its -3 dB bandwidth below 10 MHz.

2.3.2 Subarray Beamformer

Fig. 2.9 shows the circuit implementation and timing diagram of the subarray beamformer. It consists of 9 programmable analogue delay lines, each of which is built from pipeline-operated S/H memory cells that run at a sampling rate of 33 MHz, corresponding to the target delay resolution of 30 ns. Due to the fact that the sampling rate is higher than the designed bandwidth of the LNA, the increase in the noise floor caused by aliasing is negligible.

The capacitor in each memory cell is carefully sized to ensure that the associated kT/C noise is not dominant, while meeting the area requirement. With 300 fF metal-insulator-metal (MIM) capacitors, an input-referred rms noise voltage of about 118 μV is expected for each delay line, which is smaller than the output noise of the LNA at its highest gain setting.

The outputs of all 9 delay lines are passively joined together to sum up and average the charge sampled on the capacitors that are connected to the output

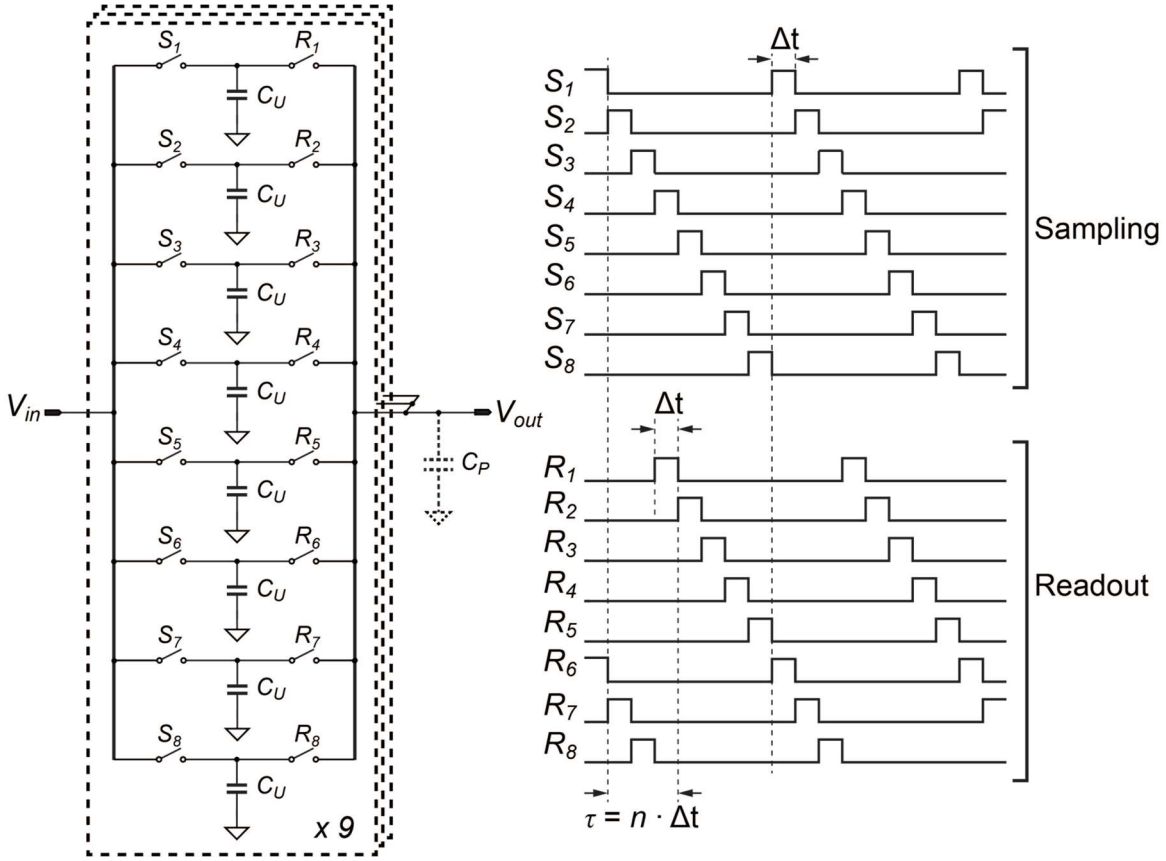


Figure 2. 9 Schematic and timing-diagram of the subarray beamformer.

node [11]. Compared to voltage-mode summation [27, 28], this scheme eliminates the need for a summing amplifier, and is thus more compact and power-efficient. However, a potential source of errors is the residual charge stored on the parasitic capacitance at the output node, which causes a fraction of the output of the previous clock cycle to be added to the output signal. This is equivalent to an undesired first-order infinite-impulse-response low-pass filter. While this filtering can be eliminated by periodically removing the charge from the output node using a reset switch [11], here we choose the simpler solution of minimizing the parasitic capacitance at the output node. It can be shown that an acceptable signal attenuation of less than 3 dB within the bandwidth from DC to 10 MHz is obtained if this parasitic is less than 20% of the total capacitance at the output node, which can be easily achieved with a careful layout. Given that the bandwidth of the transducer only extends from 3.75 MHz to 6.25 MHz, this low-pass filter does not limit the overall bandwidth of the receiver.

The control logic for programming the delay lines is also integrated within each subarray. Its core is a delay stage index rotator that determines the sequence in which the memory cells are used, as conceptually shown in Fig. 2.10. The detailed circuit implementation is shown in Fig. 2.11. It consists of an 8-stage shift register

(D_1-D_8) in which the 4-bit binary indices of memory cells (1-8) are stored and rotated. Upon startup, register D_n is preset to n. D_1 stores the index of the memory cell used for sampling the input signals, while D_2-D_8 store the indices of candidate memory cells for readout. A 3-bit selection code, provided by a built-in SPI interface, decides which of these candidates is used, allowing the delay of the individual delay line to be programmed. One-hot codes derived from the selected 4-bit binary indices are re-timed by non-overlapped clocks to control the sample/readout switches in the memory cells.

As mentioned in Section II, the SPI interfaces in all subarrays can be either loaded in parallel, or configured as a daisy-chain to load different delay-patterns to individual subarrays. With a 50 MHz SPI clock, only 0.54 μs is needed to program the ASIC's delay pattern in the parallel mode, while for the daisy-chain mode it takes about 13 μs (subarrays in each quadrant of the ASIC form one daisy-chain), leading to a 9% frame rate reduction for an imaging depth of 10 cm. As such, the daisy-chain mode enables near-field focusing at the expense of a slightly slower frame rate.

2.3.3 Mismatch-Scrambling

The S/H memory cells suffer from charge injection and clock feed-through errors, the mismatch of which introduces a ripple pattern with a period of 8 delay steps (240 ns) at the output of the delay lines. Such ripple pattern manifests itself as undesired in-band tones in the output spectrum of the beamformer, which limits the dynamic range of the signal chain.

To mitigate this interference, we propose a mismatch-scrambling technique by adding an extra memory cell and a redundant index register D_9, as shown in both Fig. 2.10 and Fig. 2.11. A pseudo-random number generator (PRNG) embedded in each subarray generates a bit sequence (PRBS) that decides whether the index of D_8 or D_9 shifts into D_1, while the other index shifts into D_9. Thus, memory cells are randomly taken out and inserted back into the sequence. This operation randomizes the ripple pattern and converts the interfering tones into broadband noise. The mismatch-scrambling function can be switched on/off with a control bit (MS_EN in Fig. 2.11).

The PRNG in each subarray is implemented as a 12-bit Galois linear-feedback shift register (LFSR) [29]. It can be re-configured as a shift register to allow the sequential loading of its initial state, i.e. the seeds. Similar to the daisy-chain

mode of the delay-pattern SPI interface, these shift registers can also be cascaded to allow different seeds to be loaded into the individual subarrays. Applying a set

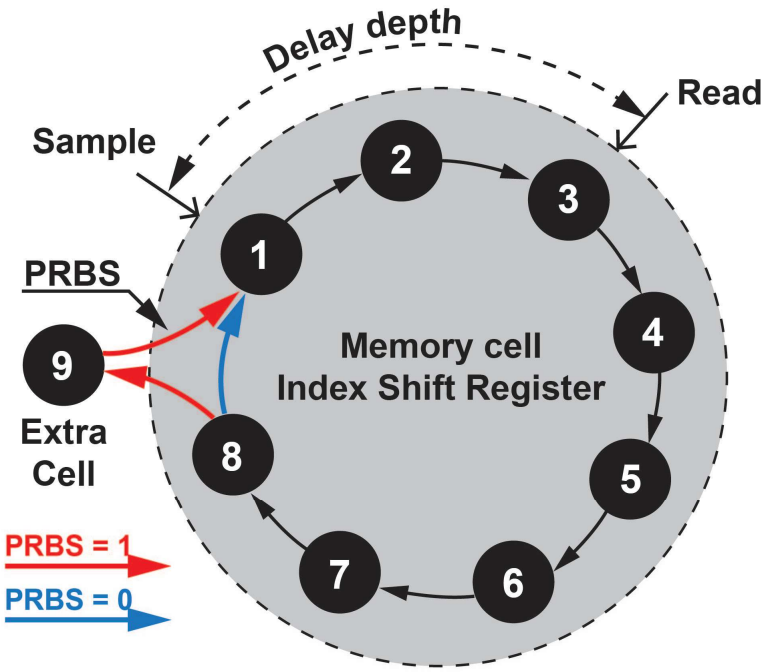


Figure 2. 10 Operation principle of mismatch-scrambling.

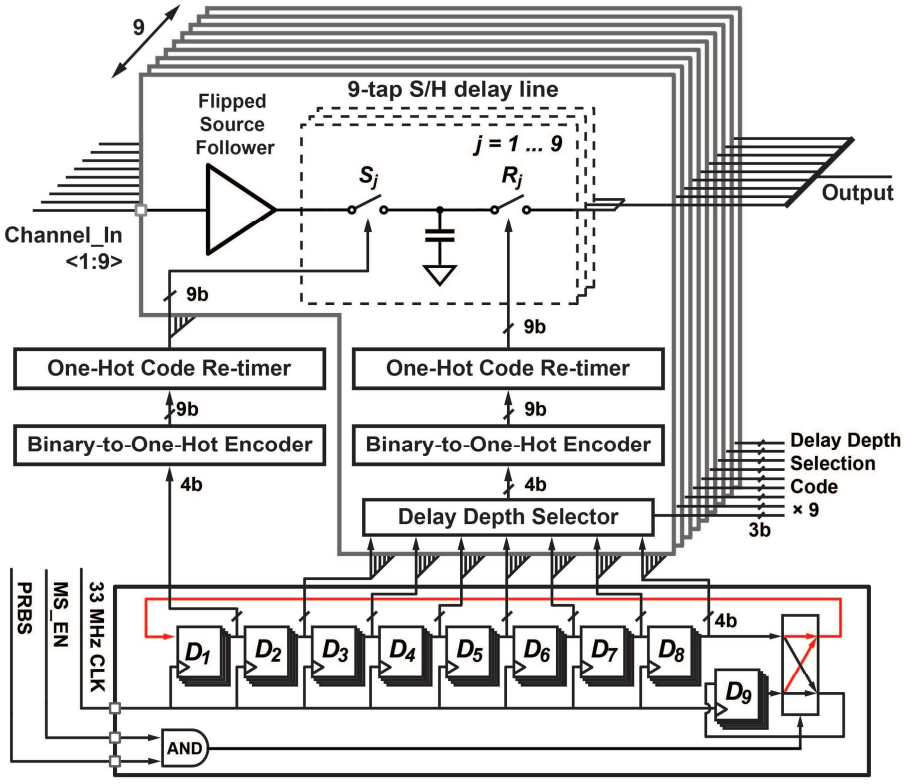


Figure 2. 11 Circuit implementation of the delay line control logic with mismatch-scrambling.

of randomized seeds for all subarrays is expected to further de-correlate the sequences of memory cell rotation on the scale of the full-array. As a result, the excess noise generated by the scrambling process can be suppressed when the output signals of the subarrays are combined by the beamforming operation in the imaging system, thus improving the SNR.

2.3.4 PGA

Fig. 2.12 shows the schematic of the PGA, which is implemented as a current-feedback instrumentation amplifier [17, 30] with a single-ended output. It consists of a differential pair of super source followers with a tuneable source-degeneration resistor R_S, which performs as a linearized trans-conductor, and a current mirror with a constant load resistor R_L, which converts the trans-conductor's output current to voltage. The voltage gain of the PGA is defined by the ratio of both resistors R_L/R_S. R_S is implemented as a switchable resistor array

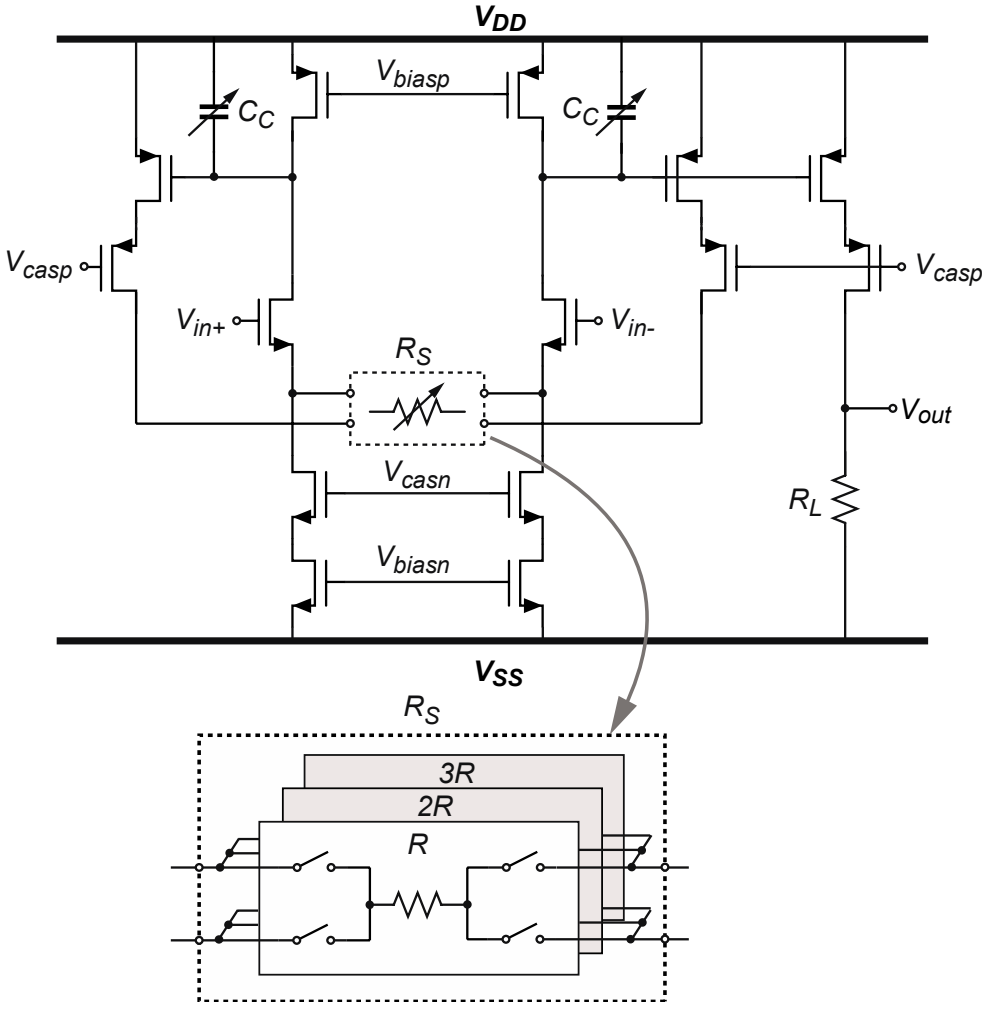


Figure 2. 12 Schematic of the PGA.

ranging from 6 kΩ to 18 kΩ, while R_L is constant (24 kΩ). To avoid using very large CMOS switches for getting small on-resistance, Kelvin connections are used to eliminate errors caused by the on-resistance of those switches (Fig. 2.12). Compensation capacitors (C_C) are added to ensure the loop stability. These capacitors are switched along with the gain settings from 800 fF at the lower gain setting to 400 fF at the highest gain setting. A differential topology is applied to improve the PGA's immunity to interference. The negative input terminal (V_{in-}) is connected to the output of a replica delay-line buffer, whose input node is AC-coupled to ground while sharing the same DC bias voltage with the other buffers.

The PGA is located after the subarray beamformer. Therefore, when comparing its noise contribution with preceding stages, the noise averaging effect [10] of the beamformer should be taken into account. It is designed to have an input referred noise density below 30 nV/√Hz to prevent adding excess noise when referred to the input of the LNA.

2.3.5 Cable Driver

The cable driver is required to fan-out the output signal of each subarray across a micro-coaxial cable with capacitance up to 300 pF. To maximize its power-efficiency, a class-AB super source follower [31], as depicted in Fig. 2.13, is adopted as the topology for the cable driver. Instead of using a high-impedance pseudo-resistor to form a quasi-floating gate, the gate of the PMOS transistor is only connected to the bias circuit during the TX phase, but kept floating during

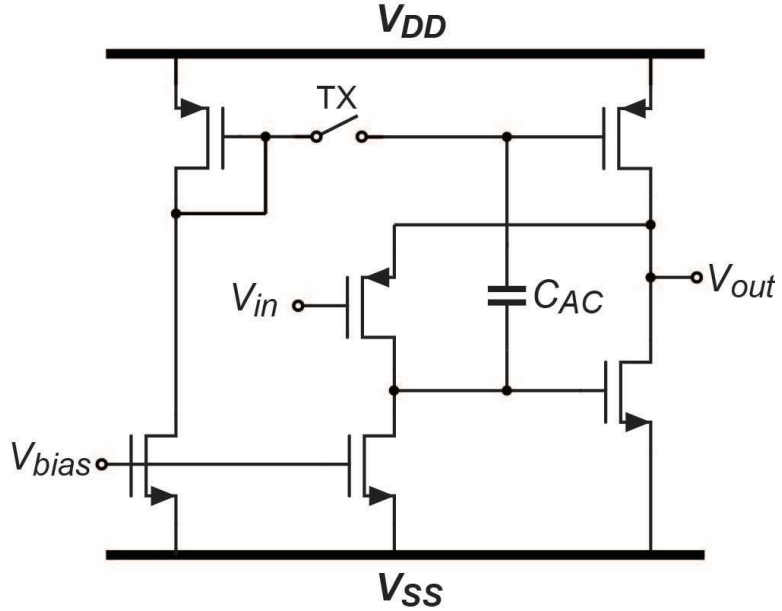


Figure 2. 13 Schematic of the cable driver.

the RX phase, similar to the dynamic DC bias scheme used in the LNA. When referred back to the input of the signal chain, the noise contribution of the cable driver is negligible as it is compressed by the gain of the PGA.

2.4 Experimental Results

The ASIC has been realized in a 0.18 µm low-voltage CMOS process with a total area of 6.1 × 6.1 mm^2, as shown in Fig. 2.14(a). Fig. 2.14(b) presents a zoom-in view of one subarray receiver that is matched to a 3 × 3 group of transducer

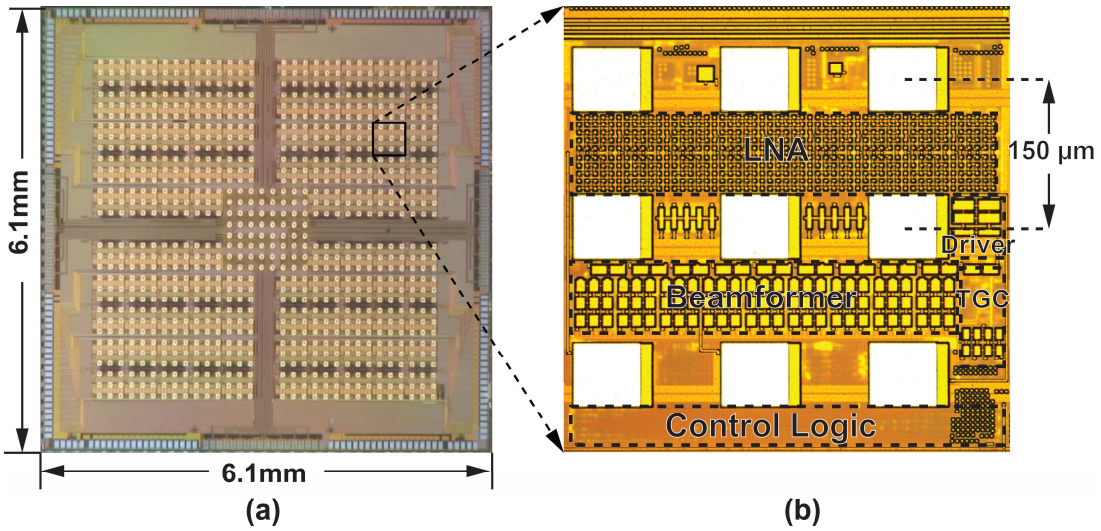


Figure 2. 14 (a) Micro-photograph of the ASIC; (b) Floor plan of one subarray receiver. Bond-pads for transducer interconnection are implemented on top of the other circuits in the top layer metal.

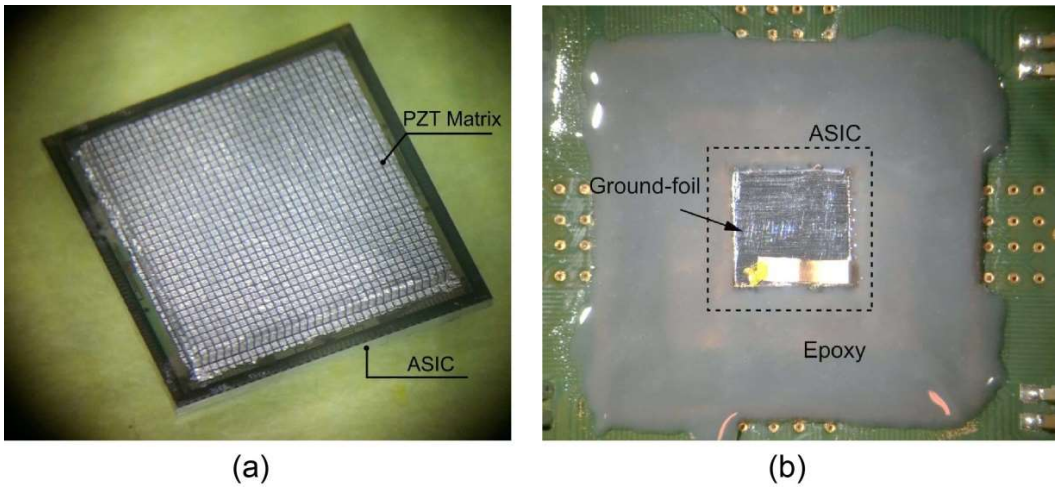


Figure 2. 15 (a) Photograph of a prototype ASIC with integrated 32 × 32 PZT matrix; (b) A prototype bonded on a daughter PCB for acoustic experiments.

elements with a pitch of 150 μm. While receiving, the ASIC consumes only 230 mW, which is less than half of the power budget for a 3-D TEE probe.

Fig. 2.15(a) shows a fabricated prototype with an integrated 32 × 32 PZT matrix transducer. The assembly has been bonded to a daughter PCB to facilitate acoustic measurements (Fig. 2.15(b)). A matching layer and ground foil are applied on top of the PZT matrix. The ground foil is directly connected to the ground potential of the ASIC via PCB traces. Bonding wires on the periphery of the ASIC are covered by a non-conductive epoxy layer for waterproofing.

The ASIC's 96-channel subarray outputs and 64-channel high-voltage transmit inputs are connected to a mother-PCB via micro-coaxial cables with a length of 1.5 m. The mother PCB is directly mounted on a programmable imaging system (Verasonics V-1 system, Verasonics Inc., Redmond, WA), which acquires the RF data from the ASIC and drives high-voltage pulses via metal traces in the ASIC to transmit elements in the transducer array. Counting in the required power-supply and digital control lines, the total number of cables required for connecting the ASIC to the imaging system is around 190.

Using this setup, the ASIC's electrical and acoustic performance has been characterized experimentally, the results of which are presented in this section.

2.4.1 Electrical Characterization

The electrical performance of the proposed LNA architecture has been fully characterized and evaluated with a separate test IC [18]. It demonstrates a 9.8 MHz bandwidth, an 81 dB dynamic range and an input-referred noise density of 5.5 nV/√Hz @ 5 MHz at its highest gain, while consuming only 0.135 mW per channel. When interfaced with an external, small PZT array that gives a receive sensitivity of about 10 μV/Pa, the LNA achieves a noise-efficiency factor (NEF) [32] that is 2.5 × better than the prior state-of-the-art [14].

Fig. 2.16 shows the measured transfer function of a 3 × 3 subarray receiver in the ASIC, with a uniform delay pattern applied to the subarray beamformer. Various combinations of LNA/PGA gain settings were applied to achieve a programmable mid-band gain ranging from –24 dB to 24 dB with a gain step of 6 dB. The measured absolute values of the mid-band gain levels are

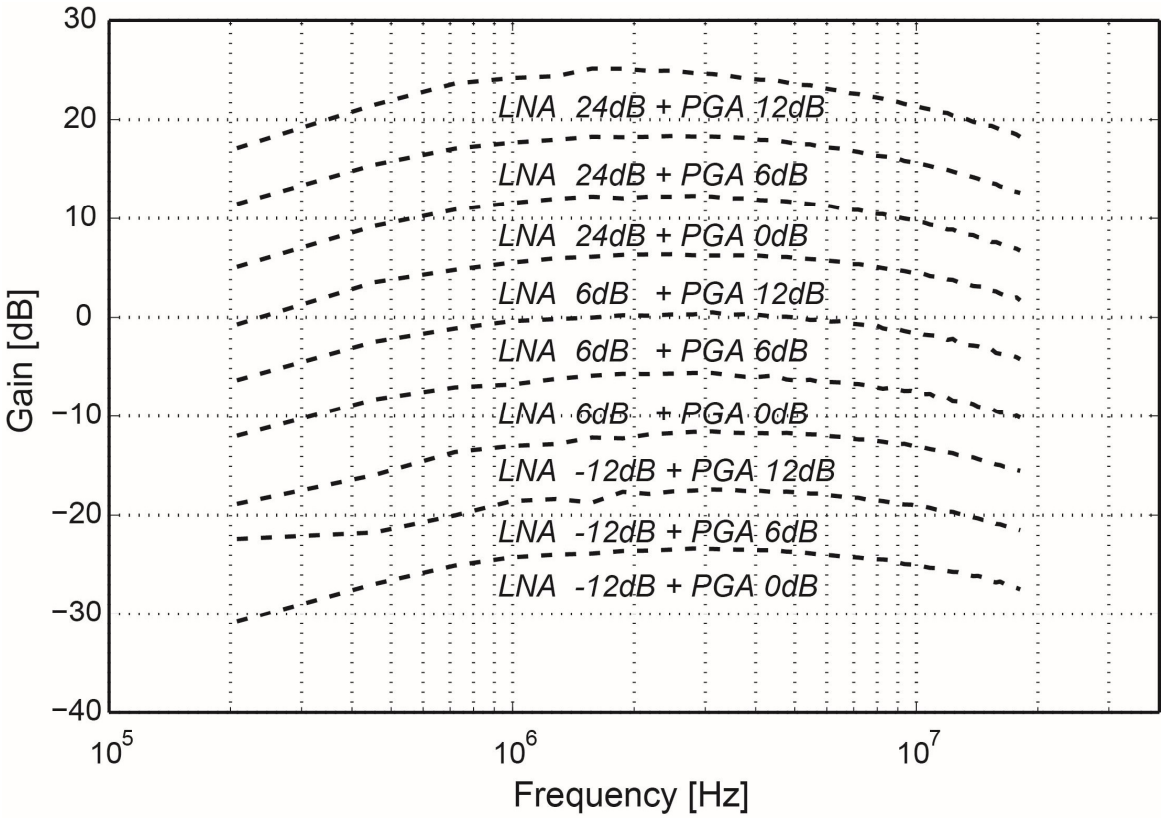


Figure 2. 16 Measured transfer functions of the ASIC with different combinations of LNA/PGA gain settings.

approximately 6 dB lower than the theoretical values of the LNA/PGA gain combinations, which can mainly be attributed to signal attenuation in the delay line buffers and cable drivers and to the attenuation associated with the parasitic capacitance at the beamformer's summing node. This deviation does not deteriorate the imaging quality, as long as an adequate SNR can be maintained at the subarray output by an appropriate selection of gain settings. The -3 dB bandwidth is about 6 MHz, ranging from 0.3 MHz to 6.3 MHz. Note that the sinc-filtering effect of the sample-and-hold operation in the beamformer also contributes to the gain roll-off at higher frequencies, which introduces 4 dB extra attenuation at 16.5 MHz (half sampling frequency).

To investigate the output noise level of the subarray receiver circuits, we use an ASIC without integrated transducer matrix, in which all bond-pads for transducer interconnection are electrically shorted to ground by means of wire bonding. With the highest LNA and PGA gain settings, the electrical output noise density of a 3 × 3 subarray is measured as 120 nV/√Hz at 5 MHz. This is in good agreement with the simulated value of 106 nV/√Hz. With a 300 mV maximum peak-to-peak output amplitude, the peak SNR at the highest gain setting thus found is about 51 dB.

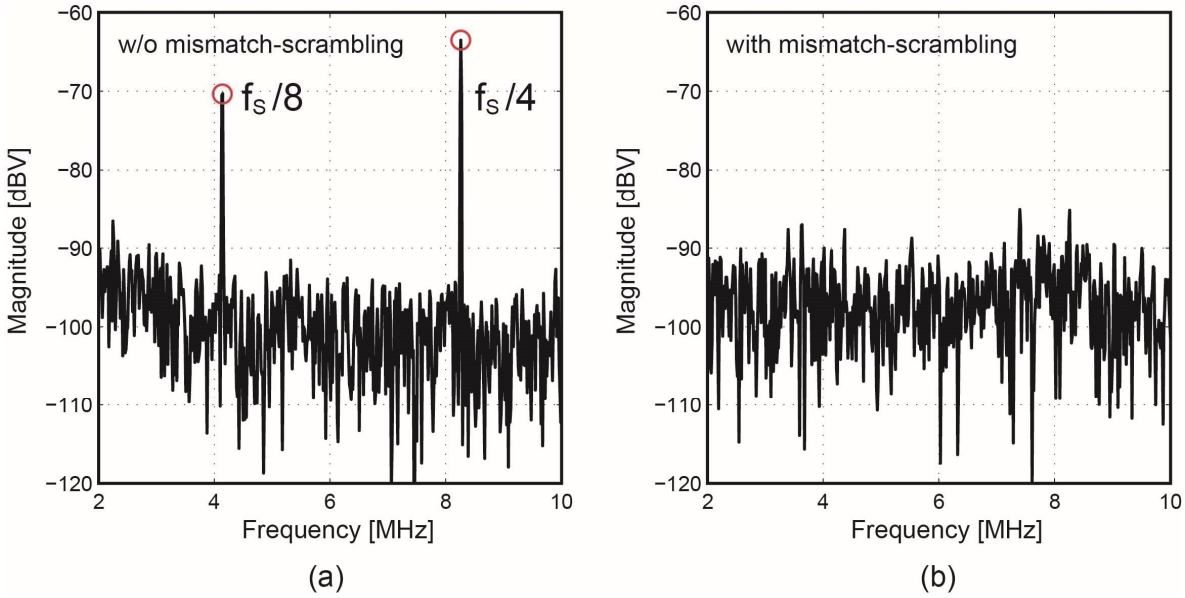


Figure 2. 17 Measured noise spectrum of the summed output of 24 subarrays without (left) and with (right) mismatch-scrambling. LNA gain = 6 dB and PGA gain = 6 dB.

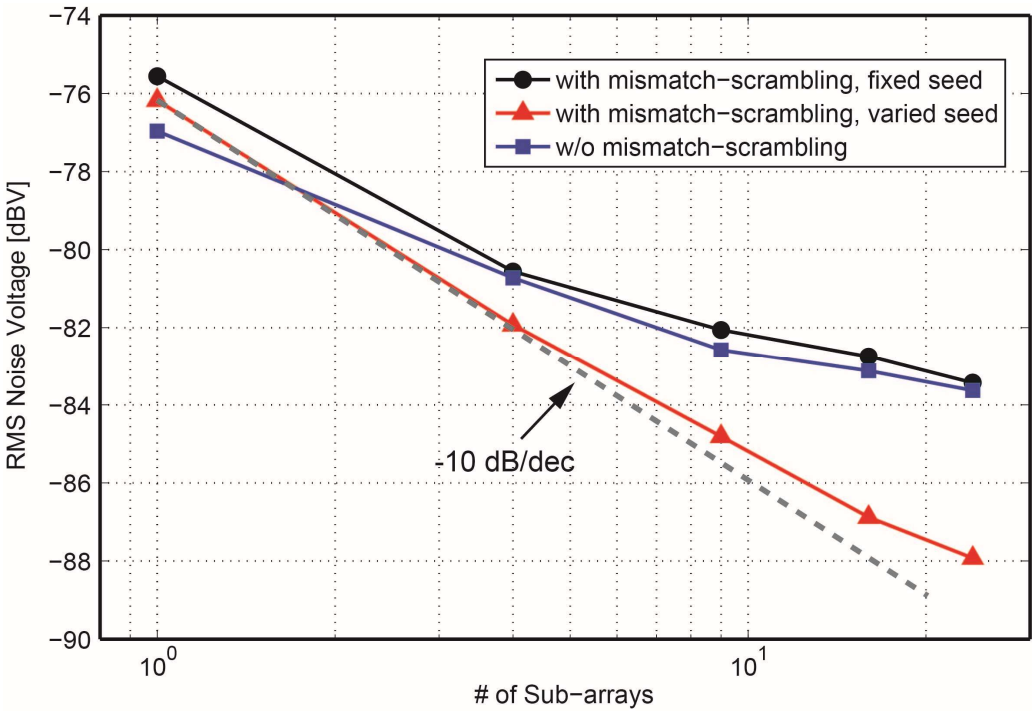


Figure 2. 18 Measured rms noise voltage after post-beamforming as a function the number of subarrays. Noise is integrated over a bandwidth of 2.5 MHz - 7.5 MHz. LNA gain = 6 dB and PGA gain = 6 dB.

Fig. 2.17(a) shows the measured output noise spectrum without enabling the mismatch-scrambling function. Two interference tones appear at fractions of the sampling frequency ($f_S/8$, $f_S/4$), which dominate the noise floor and thus reduce the dynamic range. After enabling mismatch-scrambling (Fig. 2.17(b)), these

tones get eliminated from the output spectrum, at the expense of a small increase in the noise floor (about 10 dB at frequencies close to the interference tones).

The noise power reduction associated with the system-level beamforming has been measured by combining the subarray output signals acquired using the Verasonics system. Fig. 2.18 shows the measured rms noise voltage after beamforming as a function of the number of subarrays. Ideally, if the noise at the outputs of the subarrays is uncorrelated, the noise power after beamforming should decrease inversely proportionally to the number of subarrays involved. Without mismatch-scrambling, this is not the case, because the subarray outputs signals are dominated by (correlated) mismatch-related tones. With mismatch-scrambling enabled, the noise level shows the expected improvement, i.e. decreasing at a slope close to 10 dB/dec, provided that randomized seeds are delivered to the different pseudo-range number generators. With the same seed used in all subarrays, the tones disappear from the output spectrum, but the randomized mismatch signals of different subarray are still correlated and hence are not reduced by the averaging operation of the system-level beamformer.

TABLE I. ASIC PERFORMANCE SUMMARY

RX	Supply voltage	Analogue: 1.8 V	Digital: 1.4 V
	Total power	228.9 mW	
		Analogue: 190 mW	Digital: 38.9 mW
	-3 dB Bandwidth	6 MHz	
	Input-referred noise density @ 5 MHz	w/o mismatch-scrambling: 1.0 mPa/√Hz w/ mismatch-scrambling: 2.0 mPa/√Hz (worst case*)	
	RX sensitivity	~ 5 μV/Pa @ LNA input	
	Gain steps	-12/-6/0/6/12/18/24/30/36 dB	
	HD2	43 dBc @ 300 mV_{p-p} output, 5 MHz	
TX	Max. TX pulse voltage	50 V_{p-p}	
	TX efficiency	~6 kPa/V @ 5 cm	

*The measured input-referred noise with the mismatch-scrambling function enabled varies with different delay patterns because of a systematic mismatch in the layout of S/H delay lines, which could be optimized by a better layout.

Table I summarizes the measured electrical performance of the ASIC. A system-level comparison with reported works on ASICs for 3-D ultrasound imaging is given in Table II. Our ASIC achieves both the best power-efficiency in receiving and the highest integration density.

TABLE II. SYSTEM-LEVEL COMPARISON WITH PRIOR WORKS

	[5]	[10]	[13]	[11]	**This work**
Process	1.5 µm HV	0.25 µm HV	0.18 µm HV	0.18 µm LV	**0.18 µm LV**
Transducer	CMUT	CMUT	CMUT	PZT	**PZT**
Array size	16 × 16	32 × 32	16 × 16	9 × 12	**32 × 32**
Center freq.	5 MHz	5 MHz	5 MHz	5 MHz	**5 MHz**
Element Pitch	250 µm	250 µm	250 µm	200 µm	**150 µm**
Pitch ≤ λ/2?	No	No	No	No	**Yes**
Beamform Function	TX	TX	Off-chip	RX Subarray	**RX Subarray**
# of TX el.	256	960	256	N/A	**64**
# of RX el.	32	64	256	81	**864**
Integration method	Flip-chip bonding Via Interposer	Flip-chip bonding	Flip-chip bonding Via Interposer	Direct Integration	**Direct Integration**
ASIC size	10 × 6 mm^2	9.2 × 9.2 mm^2	6 × 5.5 mm^2	3.2 × 3.8 mm^2	**6.1 × 6.1 mm^2**
RX power/el.	9 mW	4.5 mW	1.4 mW	0.44 mW	**0.27 mW**

2.4.2 *Acoustic Experiments*

The fabricated prototype shown in Fig. 2.15 was immersed in a water tank (Fig. 2.19) for the evaluation of its acoustic performance. To measure the transmit efficiency of the center subarray, all 64 TX elements were driven simultaneously by the Verasonics system and the pressure was measured at 5 cm using a

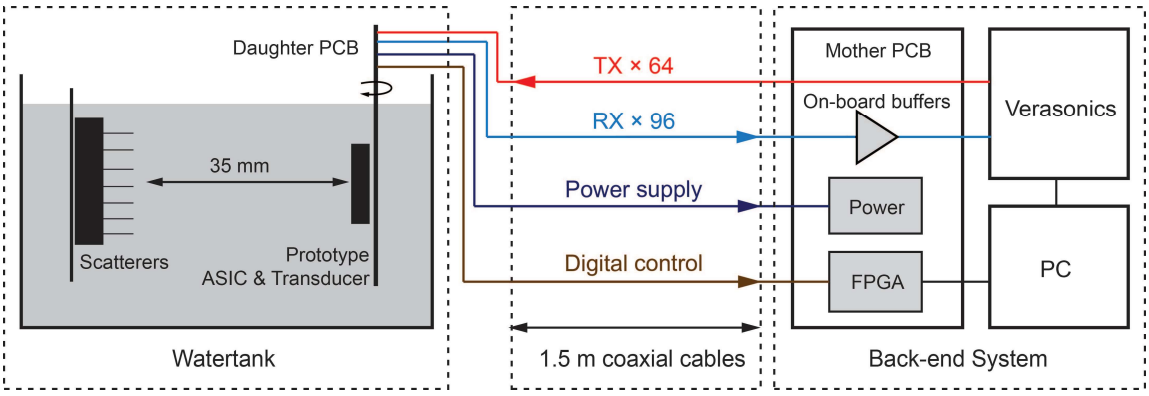


Figure 2. 19 Schematic diagram of the acoustic experiment setup. For the beam-steering measurements and the characterization of transmit pressure, scatterers were replaced by single-element transducers and a hydrophone, respectively.

hydrophone. With a 50 V excitation, a transmit pressure of 300 kPa was measured, leading to a transmit efficiency of 6 kPa/V.

To characterize the receive beam-steering function of the ASIC, a single element transducer of 0.5 inch diameter and 5 MHz central frequency (Olympus) has been used as an external source, which generates a quasi-continuous plane wave at the surface of the prototype transducer. The prototype was mounted on a rotating stage and turned from -50° to +50° with a step of 2°. The delays of subarray beamformers in the ASIC were programmed successively to steer the

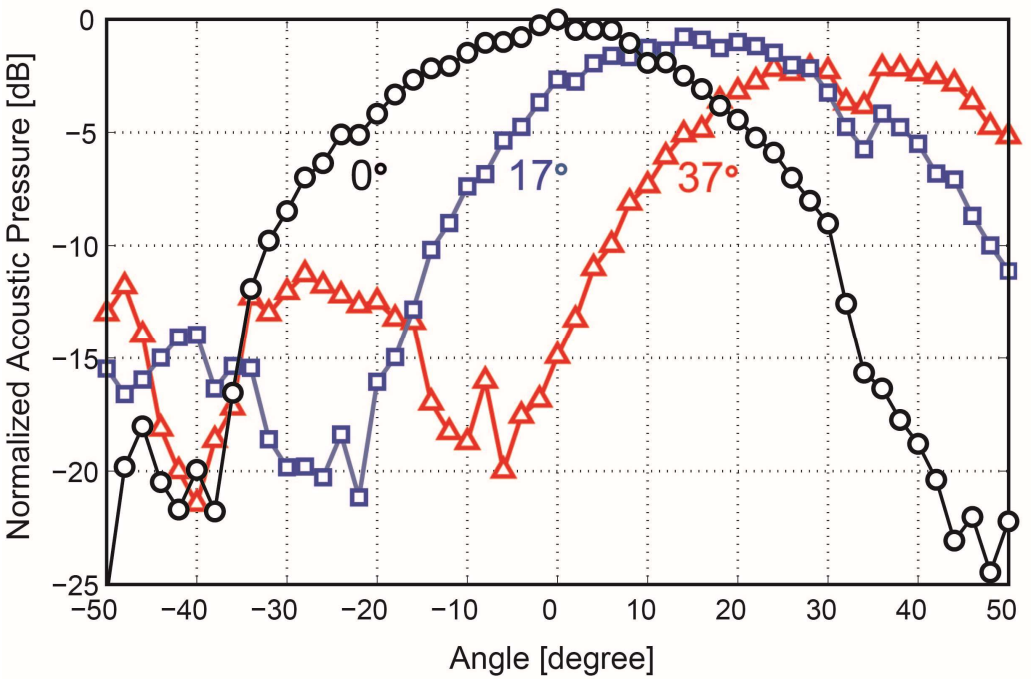


Figure 2. 20 Measured subarray beam-profile for steering angles of 0° ,17° and 37°.

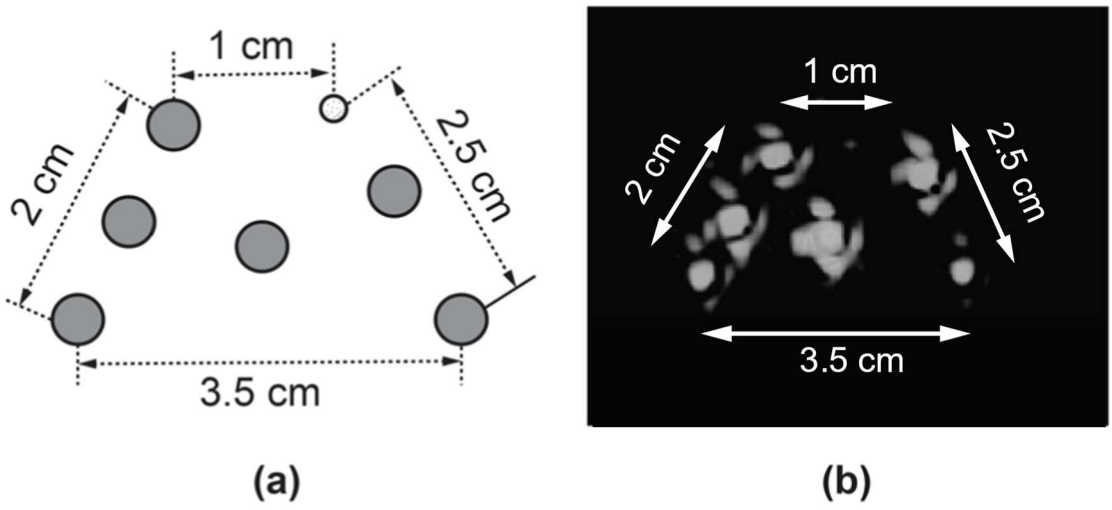


Figure 2. 21 (a) Pattern of 7 point-scatterers including 6 steel balls (gray circles) and 1 needle (the dotted circle); (b) volume-rendered 3-D image.

subarrays maximum sensitivity towards 0°, 17° and 37°. The corresponding measured subarray beam-profiles, shown in Fig. 2.20, are in good agreement with expectations, with the peak of the beams corresponding well to the programmed steering angles.

2.4.3 Imaging Results

To demonstrate the 3-D imaging capability of the prototype, a pattern of seven point scatterers (six steel balls and one needle), forming a letter "M" (Fig. 2.21(a)), was placed at a distance of approximately 35 mm in front of the transducer array. A diverging wave was transmitted from the prototype, using a pulse of 18 V (peak-to-peak), generated by the Verasonics systems and applied to the transmit subarray through the connections on the ASIC. A 3-D volume image was reconstructed by combining the subarray output signals recorded using the Verasonics system from multiple transmit-receive events, and rendered to get a frontal view of the point scatterers (Fig. 2.21(b)), which clearly shows the layout of the scatterers.

Currently, the 3-D image reconstruction has been done offline and 169 transmit-receive events were used to generate one volume as shown in Fig. 2.21(b) [33]. In a future real-time implementation, this would correspond to a frame rate of 44.4 volumes per second for an imaging depth of 10 cm. When the daisy-chain mode for delay-pattern programming is enabled, the frame rate reduces to about 40 volumes per second. We have also noted that volumes can be reconstructed from at minimum 25 transmit-receive events, at the cost of slightly degraded image quality [33]. This results in a frame rate of 300 volumes per second in the fast imaging mode.

2.5 Conclusions

A front-end ASIC with a co-integrated 32 × 32 PZT matrix transducer has been designed and implemented to enable next-generation miniature ultrasound probes for real-time 3-D transesophageal echocardiography. The transducer array is split into a transmit and a receive subarray to facilitate the power and area optimization of the ASIC. To address the critical challenge of cable-count reduction, subarray receive beamforming is realized in the ASIC with a highly-compact and power-efficient circuit-level implementation, which utilizes the mismatch-scrambling technique to optimize the dynamic range. A power- and area-efficient LNA

architecture is proposed to further optimize the performance. Based on these techniques, the ASIC demonstrates state-of-the-art power and area efficiency, and has been successfully applied in a preliminary 3-D imaging experiment.

References

[1] I. S. Salgo, "Three-Dimensional Echocardiographic Technology," Cardiol. Clin., vol. 25, pp. 231–239, May 2007.

[2] T. V. Scohy, et al., "A new transesophageal probe for newborns," Ultrasound in medicine & biology, vol. 35, pp. 1686-1689, Oct. 2009.

[3] R. S. C. Cobbold, Foundations of Biomedical Ultrasound. Oxford University Press, 2006.

[4] M. A. P. Pertijs, et al., "Low-power receive electronics for a miniature real-time 3D ultrasound probe," in IEEE International Workshop on Advances in Sensors and Interfaces (IWASI), Jun. 2015, pp. 235 - 238.

[5] B. Savord and R. Solomon, "Fully Sampled Matrix Transducer for Real Time 3D Ultrasonic Imaging," in Proc. IEEE Ultrasonics Symp. , 2003, pp. 945-953.

[6] A. Bhuyan, et al., "3D Volumetric Ultrasound Imaging with a 32 × 32 CMUT Array Integrated with Front-End ICs Using Flip-Chip Bonding Technology," in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2013, pp. 396-397.

[7] Q. Liu, C. Chen, Z. Chang, C. Prins, and M. A. P. Pertijs, "A mixed-signal multiplexing system for cable-count reduction in ultrasound probes," in IEEE International Ultrasonics Symposium (IUS), Oct. 2015, pp. 1 - 4.

[8] T. M. Carpenter, et al., "Direct Digital Demultiplexing of Analog TDM Signals for Cable Reduction in Ultrasound Imaging Catheters," IEEE Trans. Ultrason., Ferroelectr., Freq. Control, vol. 63, pp. 1078 - 1085, 2016.

[9] T. Christiansen, M. Rasmussen, J. Jensen, and E. Thomsen, "Row-column addressed 2-D CMUT arrays with integrated apodization," in International Ultrasonics Symposium, Sept. 2014, pp. 600 - 603.

[10] K. Chen, H.-S. Lee, and C. G. Sodini, "A Column-Row-Parallel ASIC Architecture for 3-D Portable Medical Ultrasonic Imaging," IEEE J. Solid-State Circuits, vol. 51, pp. 738 - 751, March 2016.

[11] C. Chen, et al., "A Prototype PZT Matrix Transducer with Low-Power Integrated Receive ASIC for 3-D Transesophageal Echocardiography," IEEE Trans. Ultrason., Ferroelectr., Freq. Control, vol. 63, pp. 47 - 59, Jan. 2016.

[12] U. S. Food and Drug Administration (FDA), "Guidance for Industry and FDA Staff–Information for Manufacturers Seeking Marketing Clearance of Diagnostic Ultrasound Systems and Transducers," Sept. 2008.

[13] A. Bhuyan, et al., "Integrated Circuits for Volumetric Ultrasound Imaging With 2-D CMUT Arrays," IEEE Trans. Biomed. Circuits Syst., vol. 7, pp. 796-804, Dec. 2013.

[14] M. Sautto, et al., "A CMUT transceiver front-end with 100-V TX driver and 1-mW low-noise capacitive feedback RX amplifier in BCD-SOI technology," in Proc. ESSCIRC, 2014, pp. 407-410.

[15] I. O. Wygant, et al., "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," IEEE Trans. Ultrason., Ferroelectr., Freq. Control, vol. 55, pp. 327-342, Feb. 2008.

[16] C. Chen, et al., "A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32 x 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography," in Symposia on VLSI circuits, 2016.

[17] Z. Yu, et al., "Front-end receiver electronics for a matrix transducer for 3D transesophageal echocardiography," IEEE Trans. Ultrason., Ferroelectr., Freq. Control, vol. 59, pp. 1500-1512, Jul. 2012.

[18] C. Chen, Z. Chen, Z. Chang, and M. A. P. Pertijs, "A compact 0.135-mW/channel LNA array for piezoelectric ultrasound transducers," in European Solid-State Circuits Conference (ESSCIRC), 2015, pp. 404 - 407.

[19] V. Daeichin, et al., “Acoustic characterization of a miniature matrix transducer for pediatric 3D transesophageal echocardiography”, in Ultrasound in Medicine & Biology, vol. 44, no. 10, pp. 2143-2154, 2018.

[20] S. B. Raghunathan, et al., "Design of a miniature ultrasound probe for 3D transesophageal echocardiography," in Proc. IEEE Ultrasonics Symp., 2014, pp. 2091-2094.

[21] S. Blaak, et al., "Design of a Micro-beamformer for a 2D Piezoelectric Ultrasound Transducer," in Proc. IEEE Ultrasonics Symp., 2009, pp. 1338-1341.

[22] I. O. Wygant, "A comparison of CMUTs and piezoelectric transducer elements for 2D medical imaging based on conventional simulation models," in International Ultrasonics Symposium, 2011, pp. 100 - 103.

[23] S. Robert, O. Abed-Meraim, and L. L. Coco, "Wide-band variable-gain LNA in 65nm CMOS with inverter based amplifier for multi-tuners cable TV reception," in European Solid-State Circuits Conference (ESSCIRC), 2009, pp. 104 - 107.

[24] M. S. Akter, R. Sehgal, F. v. d. Goes, and K. Bult, "A 66 dB SNDR pipelined split-ADC using class-AB residue amplifier with analog gain correction," in European Solid-State Circuits Conference (ESSCIRC), 2015, pp. 315 - 318.

[25] Y. Chae and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator," IEEE J. Solid-State Circuits, vol. 44, pp. 458 - 472, Feb. 2009.

[26] T. Christen, "A 15-bit 140-uW Scalable-Bandwidth Inverter-Based ΔΣ Modulator for a MEMS Microphone With Digital Output," IEEE J. Solid-State Circuits, vol. 48, pp. 1605 - 1614, July 2013.

[27] J.-Y. Urn, et al., "A single-chip time-interleaved 32-channel analog beamformer for ultrasound medical imaging," in Proc. Asian Solid State Circuits Conference (A-SSCC), Nov. 2012, pp. 193 - 196.

[28] J.-Y. Urn, et al., "An analog-digital-hybrid single-chip RX beamformer with non-uniform sampling for 2D-CMUT ultrasound imaging to achieve wide dynamic range of delay and small chip area," in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap., Feb. 2014, pp. 426 - 427.

[29] J.-P. Hong, et al., "A 0.004mm2 250μW ΔΣ TDC with time-difference accumulator and a 0.012mm2 2.5mW bang-bang digital PLL using PRNG for low-power SoC applications," in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap., Feb. 2012, pp. 240 - 242.

[30] R. F. Yazicioglu, P. Merken, R. Puers, and C. V. Hoof, "A 60 μW 60 nV/$\sqrt{\text{Hz}}$Readout Front-End for Portable Biopotential Acquisition Systems," IEEE J. Solid-State Circuits, vol. 42, pp. 1100 - 1110, May 2007.

[31] A. J. Lopez-Martin, J. Ramirez-Angulo, R. G. Carvajal, and L. Acosta, "Power-efficient class AB CMOS buffer," Electron.Lett., vol. 45, pp. 89-90, Jan. 2009.

[32] K. Chen, H.-S. Lee, A. P. Chandrakasan, and C. G. Sodini, "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver," IEEE J. Solid-State Circuits, vol. 48, pp. 2734 - 2745, Oct. 2013.

[33] D. Bera, et al., "Three-Dimensional Beamforming Combining Micro-beamformed RF Datasets," presented at the International Ultrasonics Symposium, 2016.

CHAPTER 3

A FRONT-END ASIC WITH INTEGRATED SUBARRAY BEAMFORMING ADC AND DIGITAL TIME-DIVISION MULTIPLEXER

Based on publication C. Chen, **Z. Chen***, D. Bera, E. Noothout, Z.-Y. Chang, M. Tan, H.J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M.A.P. Pertijs, "A Pitch-matched Front-End ASIC with Integrated Subarray Beamforming ADC for 3-D Ultrasound Imaging in Miniature Probes", IEEE Journal of Solid-State Circuits, vol. 53, no. 11, pp. 3050-3064, Nov. 2018*

* *equal 1st author contribution*

3.1 Introduction

Data acquisition from 2-D transducer arrays has become one of the main challenges for the development of endoscopic and catheter-based 3-D ultrasound imaging devices, such as transesophageal echocardiography (TEE) [1], intracardiac echocardiography (ICE) [2] and intravascular ultrasound (IVUS) [3, 4] probes. The main obstacle lies in the mismatch between the large number of transducer elements needed for 3-D imaging, and the limited number of cables that can be accommodated in these systems. Recent advances in transducer-on-CMOS integration methods [5, 6] have enabled the use of front-end ASICs performing signal conditioning and data-reduction close to the transducer. The concept of subarray beamforming [7], which divides the transducer array in subarrays and combines the signals received by the elements in each subarray by a local delay-and-sum operation, is capable of reducing the channel count by an order of magnitude. This has been successfully demonstrated in several ASIC prototypes [1, 8] and has made it possible to develop probes with 3000+ transducer elements [9]. However, it is still an arduous engineering problem to assemble hundreds of cables within endoscopes or catheters of ≤ 5 mm diameter [2]. Such constraints have forced system designers to trade-off imaging quality against physical dimension and fabrication cost [2].

A variety of efforts has been made in recent years to further reduce the cable-

count by making better use of the cable capacity. Time-multiplexing in the analogue domain [10] allows the signals received by multiple elements to share a single cable. However, the limited bandwidth and transmission-line effects of the micro-coaxial cables result in significant channel-to-channel crosstalk [11, 12]. Other analogue modulation methods, such as frequency-division multiplexing (FDM) [13], also suffer from the cable non-idealities.

A more radical solution is to move ADCs into the probe and perform the channel-reduction in the digital domain, where complex modulated signals can be transmitted with much better robustness against noise, interference and crosstalk. Moreover, in-probe digitization would open up the possibility to migrate more signal processing functionalities into the probe, such as post-beamforming [14] and compressive beamforming [15], which are expected to further reduce the channel count. A prerequisite to achieve this goal is an efficient way to implement a massively-parallel ADC array within the stringent power and area constraint of miniature ultrasound probes.

Based on the framework of subarray beamforming, in-probe digitization can be realized by digitizing the output of an analogue subarray beamformer with per-subarray ADCs [16]. Alternatively, digital beamforming with per-element ADCs can be considered [17-19]. The latter approach requires D^2 ADCs with an equal number of preconditioning circuits and input buffers for a $D \times D$ subarray, plus the associated digital FIFOs for the realization of delays. This is difficult to be directly integrated underneath a pitch-constrained 2-D transducer with an affordable power consumption. In [17], the area problem was addressed by using nanoscale CMOS technologies. Nevertheless, the reported element-level $\Delta\Sigma$ ADC is larger than the ideal half-wavelength pitch of 150 μm at 5 MHz, and the power dissipation is more than two orders of magnitude higher than its analogue counterpart [1]. Moving the ADC to the output of an analogue beamformer helps in reducing the area and power cost for A/D conversion. The work of [16] employs subarray beamformers based on S/H circuits followed by a stand-alone Nyquist-rate ADC. The reported silicon area and power are both dominated by the analogue beamformer, resulting in a per-channel footprint that is 12× larger than the dimension of a 5-MHz transducer element and a power consumption far exceeding the heat dissipation constraint for miniature probes [20]. More recently, [21] proposes to embed charge-redistribution SAR ADCs with a subarray beamformer, so as to save power. This approach, however, requires N SAR ADCs to implement a N-channel beamformer, resulting in a poor area efficiency.

In this work, we propose an element-pitch-matched ASIC architecture to demonstrate the feasibility of efficient in-probe digitization in miniature ultrasound probes [22]. It provides subarray beamforming for a directly integrated 5-MHz PZT matrix with a half-wavelength element-pitch of 150 μm. In each 3 × 3 subarray, a compact Nyquist-rate beamforming ADC is implemented following the analogue front-end circuits. By merging the beamforming and digitization functions coherently in the charge domain, there is no need for intermediate ADC buffers, resulting in significant power and area reduction. The outputs of four beamforming ADCs are fed into a high-speed digital serializer on the periphery of the ASIC to reduce the total output channel-count by a factor of 4. Thus, the ASIC achieves a 36-fold channel-count reduction, while consuming less than 1 mW/element in receive mode. The effectiveness of the proposed architecture has been successfully demonstrated in both electrical tests and a 3-D imaging experiment.

This chapter is organized as follows. The architecture of the proposed ASIC is discussed in Section 3.2. Section 3.3 describes the circuit implementation details of the subarray receiver and the datalink. Section 3.4 presents the experimental setup and results. A conclusion is given in Section 3.5.

3.2 System Architecture

3.2.1 Overview

Fig. 3.1 shows an overview of the proposed system. It consists of a front-end ASIC, a 5-MHz 150-μm-pitch PZT matrix and the associated external electronics. The PZT matrix is constructed from a bulk piezoelectric material (CTS 3202 HD, CTS Corporation, Albuquerque, MN, USA) that is stacked on the ASIC using the PZT-on-CMOS heterogeneous integration process described in [6]. A metallic interconnection layer and a conductive glue layer connect the bottom electrodes of the PZT elements to a bondpad array on the ASIC.

As a proof-of-concept, we use a PZT matrix with a relatively small aperture in this work, while the proposed circuit architecture and layout are both designed to facilitate the future extension to a larger array size, such as the 32 × 32 array presented in chapter 1. The matrix is divided into 3 × 24 transmit (TX) elements and 6 × 24 receive (RX) elements. Similar to [1, 6], the TX elements are directly wired-out to external high voltage pulsers using metal traces in the ASIC, thus

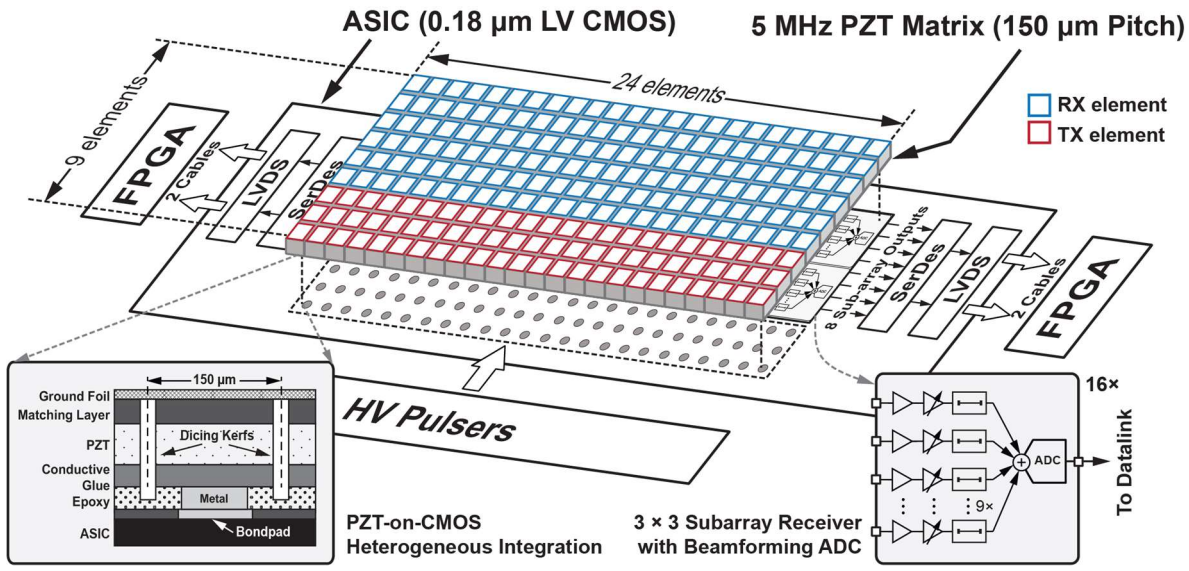


Figure 3. 1 System overview

enabling the use of a low-voltage CMOS process [3]. Nevertheless, the concepts presented in this chapter are equally applicable to an ASIC using high-voltage CMOS technology in which local pitch-matched TX pulsers are also included. In this prototype, every 3 TX elements in the same column are connected together in the ASIC to reduce the overall I/O count, turning them into a 1-D phase array with a broad beam profile in elevation direction. In a future extension to a larger array, an alternative more symmetrical transmit layout would be preferred, such as the central transmit subarray described in [1]. In RX, subarray beamforming is applied on 3 × 3 elements to realize a 9-fold channel-reduction, yielding in total 16 subarrays.

Fig. 3.2a shows the architecture of RX electronics in the ASIC. Each subarray receiver consists of a 9-channel analogue front-end (AFE) that acquires echo signals from the transducer elements and conveys them to programmable delay lines. The output of the nine delay lines are added and digitized in the charge domain by a successive approximation register (SAR) ADC. The digitized data is transferred to a datalink at the periphery of the ASIC, where the data from 4 subarrays are combined on a shared LVDS (low-voltage differential signaling) output channel, thus realizing an extra 4-fold channel-count reduction. At the system side, an FPGA [23] receives and stores the data, which is then transmitted to a PC for image reconstruction.

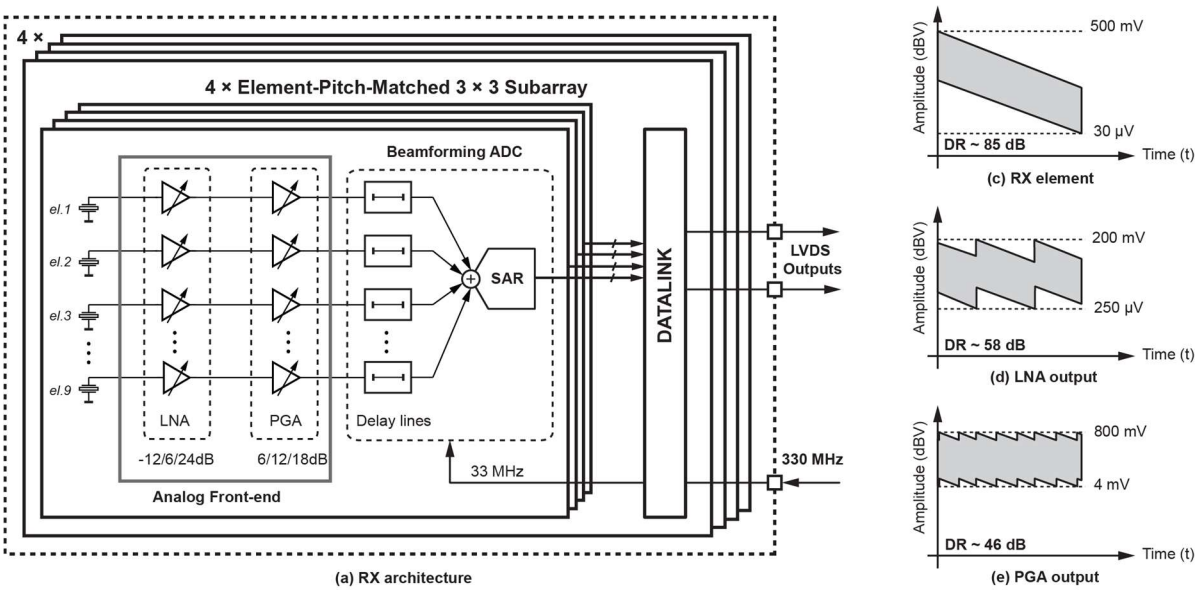


Figure 3. 2 (a) Architecture of receive electronics; (b) Signal dynamic range at the input of the LNA; (b) Signal dynamic range at the output of the LNA; (c) Signal dynamic range at the output of the PGA.

3.2.2 AFE

The AFE in each channel consists of a low-noise amplifier (LNA) and a programmable-gain amplifier (PGA). Fig. 3.2b illustrates the expected peak-to-peak voltage signal received by a transducer element as a function of time. Note that the time axis, assuming a constant speed of sound, is equivalent to the axial depth. Echoes resulting from deeper scatterers will arrive later, and will be more attenuated, leading to an overall peak-to-peak amplitude range from 30 µV to 500 mV, while the instantaneous dynamic range (DR), i.e. the ratio between the largest and smallest echoes at a given imaging depth, is about 40 dB. The depth-dependent (and hence time-dependent) attenuation can be compensated by applying time-varying gains in the AFE. Such time-gain compensation (TGC) function is implemented by distributing discrete gain-steps between the two stages in the AFE. The LNA provides a high gain for small echo signals from deep scatterers, where the acoustic and electrical noise determine the detection limit, and a lower gain for large echoes from nearby scatterers, where linearity matters. With a gain step of 18 dB, the DR is thus compressed to approximately 58 dB (Fig. 3.2c). This is further reduced by the PGA, which provides gain steps of 6 dB, resulting in an output DR of 46 dB, with peak-to-peak amplitudes ranging from 4 mV to 800 mV (Fig. 3.2d). This arrangement effectively reduces the noise and DR requirements of the succeeding circuits, while keeping the complexity of the TGC implementation modest, thus bringing significant power and area

advantages for the whole system. It can be combined with a fine-gain compensation in the digital back-end to avoid imaging artifacts associated with the gain steps.

3.2.3 Beamforming ADC

The beamformer in each subarray is constructed in a way similar to the designs described in Chapter 2. Analogue delay lines based on switched-capacitor memory cells are employed because of their simplicity and flexibility in delay control, as well as the good immunity to process/voltage/ temperature (PVT) variations [16, 24]. Each delay line consists of 8 memory cells operating in a time-interleaved fashion at a sampling rate of 30 MHz, corresponding to a delay resolution of 33 ns and a maximum range of ~233 ns. This delay range allows for pre-steering up to ±37° in both azimuthal and elevation directions [6]. The chosen delay quantization causes negligible degradation to the image quality with the aid of the imaging scheme proposed in [25], while requiring only a modest number of memory elements that fit within the available die area. The delay control logic is implemented based on a delay stage index rotator as described in [1], which can be programmed via a built-in serial-peripheral-interface (SPI) embedded in each subarray.

Dynamic focusing in the subarray beamformer is not implemented in this design as it is not required given the relatively small subarray size (3 × 3) [7, 26]. However, if desired, it can be readily added to the proposed beamforming ADC architecture by adopting the delay extension/skipping approach as described in [9].

As discussed in Section 3.2.2, the signal DR at the output of each AFE channel is 46 dB. Considering the extra √9 (9.5 dB) SNR gain provided by a 9-channel beamformer, a 10-bit ADC is required to achieve an adequate quantization resolution. For an ultrasound transducer with a ≥ 50% fractional bandwidth, the ADC sampling rate must be 4 to 10 times the transducer central frequency to maintain a satisfactory side-lobe level [27], which corresponds to 20 MS/s to 50 MS/s for our 5-MHz array. Given these specifications, a SAR ADC stands out as the architecture choice for its superior power-efficiency [28].

Most SAR ADCs perform the quantization in the voltage domain [29, 30], while switched-capacitor-based (S/H) delay lines essentially operate in the

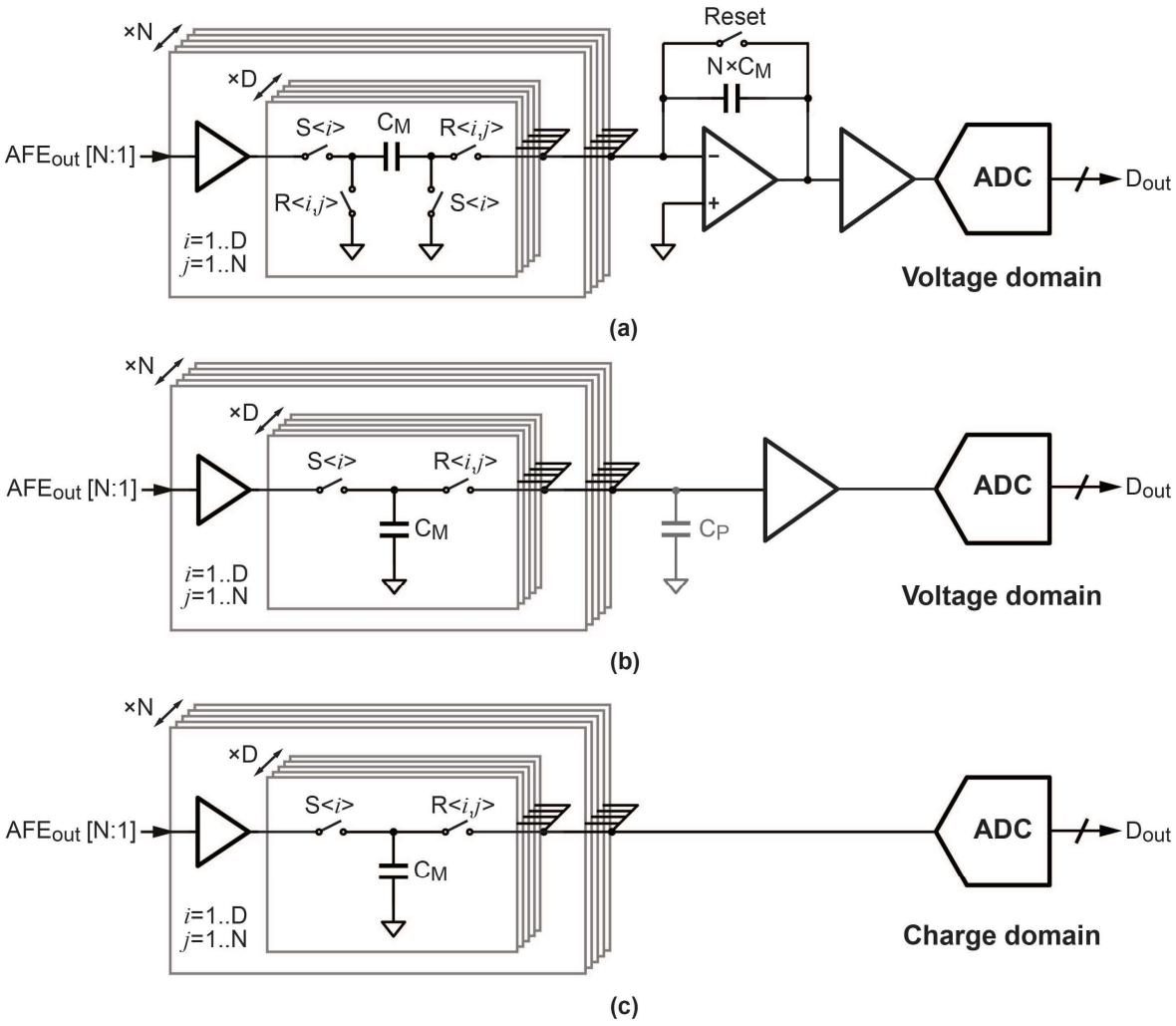


Figure 3. 3 Hybrid beamforming with post-analogue-beamforming digitizers. (a) S/H delay lines with an active summing amplifier; (b) S/H delay lines with passive charge summation and active voltage buffer as the ADC driver; (c) the proposed architecture.

charge-domain. Therefore, a charge-to-voltage conversion is required for driving the ADC.

An active summing amplifier was used in [16] to sum the charges stored on the delay-line capacitors C_M, while an extra voltage buffer drives the ADC (Fig. 3.3a). To implement a unity voltage gain, the feedback capacitance must be equal to the total memory capacitance involved in each cycle, i.e. $N \times C_M$, leading to a considerable power consumption in the amplifier; more than 10× power of the ADC in [16]. The summing amplifier can be eliminated by adopting passive charge-summation [1] (Fig. 3.3b). However, the power consumed by the ADC driver is still problematic; it is usually comparable to that of the ADC itself, as a result of the relatively large capacitance it needs to drive during a constrained input sampling time [31].

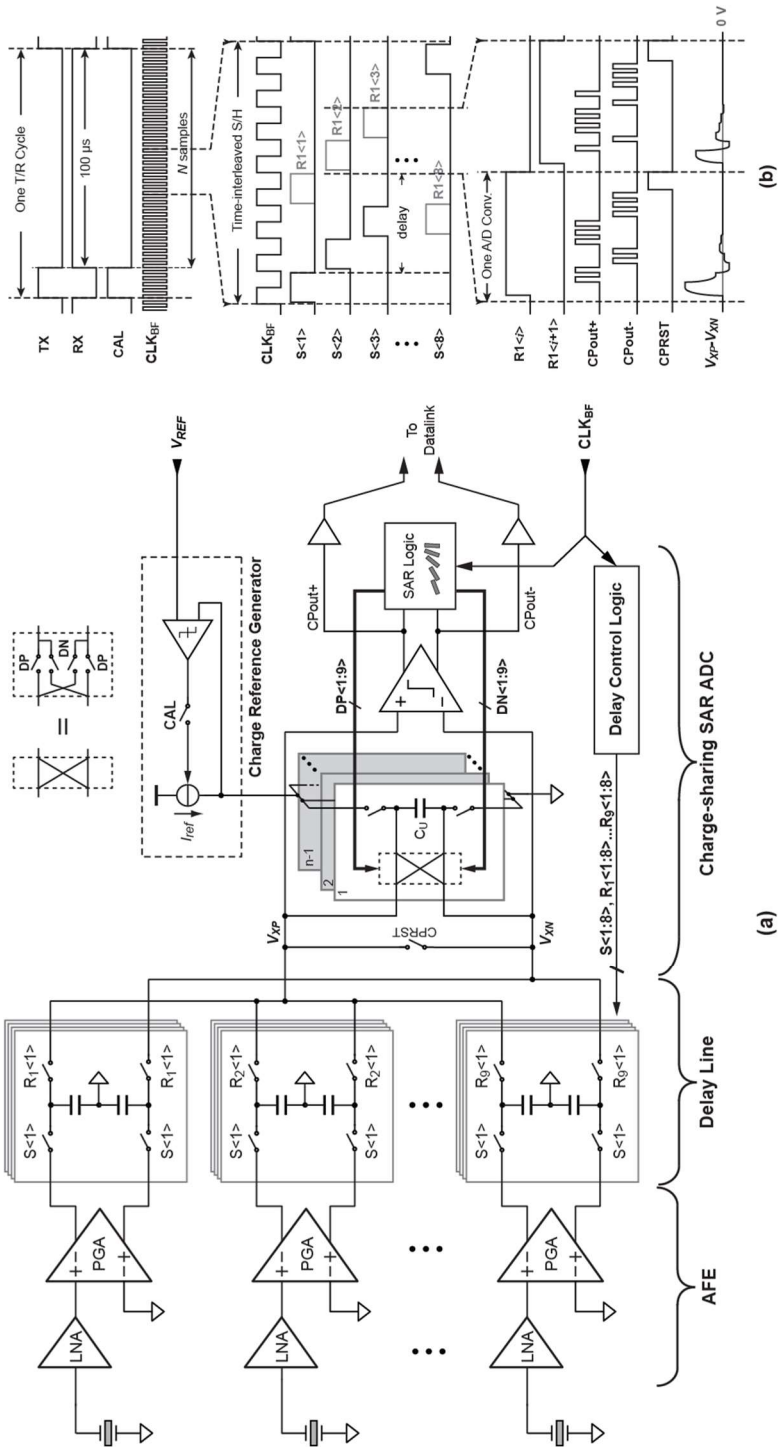


Figure 3. 4 The proposed beamforming ADC and the operation timing diagram.

To eliminate the ADC driver, we propose to perform the digitization in the charge domain, rather than in the voltage domain (Fig. 3.3c). This is achieved by sequentially neutralizing the passively-summed signal charge with binary-scaled charge references through a successive approximation process. In practice, the charge references can be realized as a precharged capacitor DAC array. By doing so, the beamformer and the digitizer are essentially merged together: the delay

lines perform as a multichannel time-interleaved input sampler in a charge-sharing SAR ADC [32]. We will refer to this circuit as a beamforming ADC.

Fig. 3.4 shows a block diagram of the ADC and its timing diagram. Both the beamforming and the digitization are performed differentially to mitigate the impact of common-mode noise and interference. In each channel, the PGA converts the single-ended LNA output to a differential voltage, which is cyclically sampled and held on memory cells under the control of non-overlapping sampling clocks, S<1:8>. The charge sampled on the memory cells is then released to the summing nodes, V_{XP} and V_{XN}, at the rising edges of channel-specific readout clocks, R_k<1:8>, where k ranges from 1 to 9. The delay of a channel is thus defined by the time interval between the falling edges of its sampling and readout clocks. Before the start of each readout phase, a capacitor DAC array is precharged to a reference voltage (V_{REF}). In each readout phase, the successive-approximation charge-balancing process starts after a short time interval reserved for the passive charge redistribution on the joint memory cells. In every bit-cycle, a dynamic comparator detects the sign of the differential voltage on the summing nodes ($V_{XP} - V_{XN}$) and dictates the polarity of the charge reference for use in the next cycle. To obviate the need for distributing an oversampled clock, self-timed SAR logic [33] is employed. By the end of the readout phase, a digital representation of the delayed-and-summed charge is available. To simplify the output routing, the differential outputs of the dynamic comparator (CPout+/-) are buffered and transmitted to the periphery of the ASIC, where the 10-bit parallel data is recovered and synchronized to a high-speed system clock for further processing.

Upon completion of a conversion, the summing nodes (V_{XP} and V_{XN}) are reset to prevent undesired signal attenuation associated with residue charge on the parasitic capacitors [1], as shown in Fig. 3.4a (CPRST). This operation also enables the calibration of the comparator offset in the background, as will be discussed in Section 3.3.

3.2.4 Datalink

Fig. 3.5 shows a block diagram of the datalink. Each subarray ADC is interfaced with a clock-data-recovery (CDR) circuit. It converts the differential return-to-zero (RZ) outputs of the SAR comparator to a single-bit non-return-to-

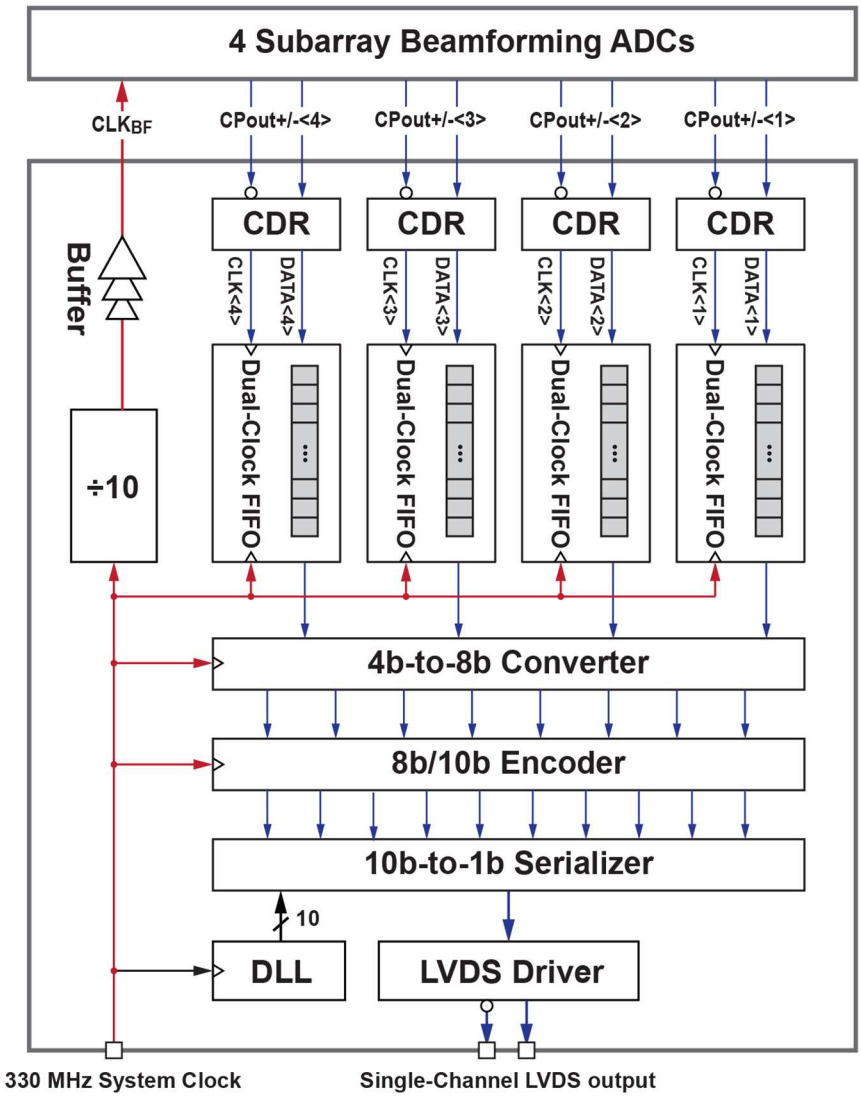


Figure 3. 5 Datalink architecture

zero (NRZ) data-stream, and extracts an asynchronous clock that is aligned with the recovered data. The data-stream is then synchronized to a 300 MHz global clock in a FIFO for further processing.

Before the serialization, every two consecutive 4-bit-wide FIFO outputs are concatenated to an 8-bit byte by a 4b-to-8b converter, which is then mapped to a 10-bit code in an 8b/10b encoder [34]. This coding scheme facilitates clock recovery at the system side without relying on a per-channel clock line. Moreover, it ensures a DC-balance in the data-stream, which helps both data recovery and error detection at the system side [34]. The 10-bit data is then serialized to a single-bit data stream at 1.5 Gb/s, which is buffered by a LVDS driver and transmitted over a twin-axial cable to the imaging system.

The ASIC receives a 300 MHz global LVDS clock from the system, which is

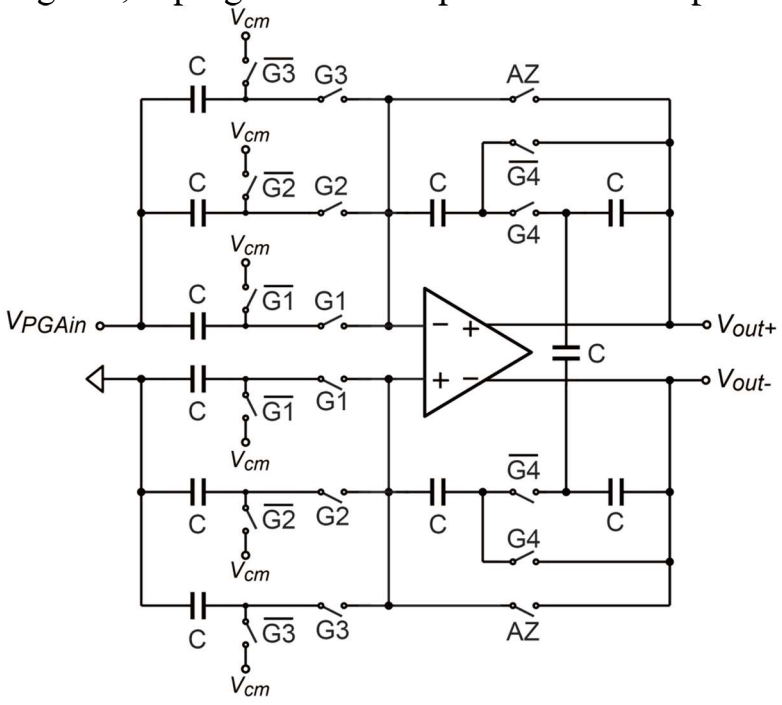
converted to CMOS logic levels at the periphery of the ASIC. Here, it serves as the main clock for the core of the datalink, and is multiplied by 5 in a delay-locked-loop (DLL) to generate the clock phases needed for serialization. It is divided down by 10 to produce the 30 MHz beamforming clock (CLK_{BF}), which is distributed across the subarray receivers via a balanced clock tree.

3.3 Circuit Implementation

3.3.1 AFE

The LNA in each AFE channel is an improved version of the design described in [1, 35]. It is implemented as a single-ended capacitive feedback current-reuse amplifier with a split capacitor network to achieve a compact layout, and consumes 75 μA.

The PGA implements three functions: 1) providing 4 fine gain steps to define the TGC gain resolution; 2) converting the LNA output to differential signals to drive the delay lines; 3) low-pass filtering prior to sampling to minimize aliasing. As shown in Fig. 3.6, a programmable capacitor network provides the desired



	G1	G2	G3	G4
6 dB	0	1	1	1
12 dB	0	1	0	0
18 dB	0	1	1	0
24 dB	1	1	1	0

Figure 3. 6 Schematic of the PGA.

gain levels ranging from 6 dB to 24 dB according to the control code map shown below. To save area, a T-type capacitor network [36], employing unit capacitors of 33 fF, is used as the feedback element across a compact differential telescopic amplifier. Each PGA consumes 100 μA.

The PGA drives a delay line that consists of 8 stages of time-interleaved differential S/H memory cells. Each cell comprises a pair of grounded metal-insulator-metal (MIM) capacitors and a set of nMOS switches for sampling and readout. The capacitors are sized as large as possible (133 fF) within the available area to minimize the kT/C noise contribution to the front-end. The worst-case settling time constant of approximately 1.5 ns is less than 1/20 of the sampling period, adequate for the required linearity in spite of the signal-dependent on-resistance of the switches.

3.3.2 Charge Reference Generation

The generation and distribution of references for a massively-parallel ADC array is challenging. In prior implementations of charge-sharing SAR ADCs [32, 37], the capacitor DAC (CDAC) is precharged by an external voltage source before the start of each conversion. Due to the significant load that this source needs to drive in a nanosecond time slot, this approach is prone to suffer from errors due to di/dt transients caused by the bondwire inductance, unless large on-chip decoupling capacitors are used. The alternative of employing on-chip reference buffers would introduce a significant power overhead [38].

In this work, we propose to precharge the CDAC with current sources to relax the power and area requirements for charge reference generation. Unlike the approach described in [38], the precharging current is locally generated in each subarray. To mitigate mismatch and PVT sensitivity, it is self-calibrated during the TX phase in reference to an external voltage (V_{REF}). This simplifies the system-level layout, as no global current reference distribution or high-current voltage reference routing is required.

Fig. 3.7 shows the schematic diagram of the charge reference generator and its timing details. It consists of a gated current source (M_P), a charge-pump and a calibration comparator. Intuitively, the charge reference generated by a gated current source can be written as:

$$Q_{REF} = I_P \cdot T_{int}$$

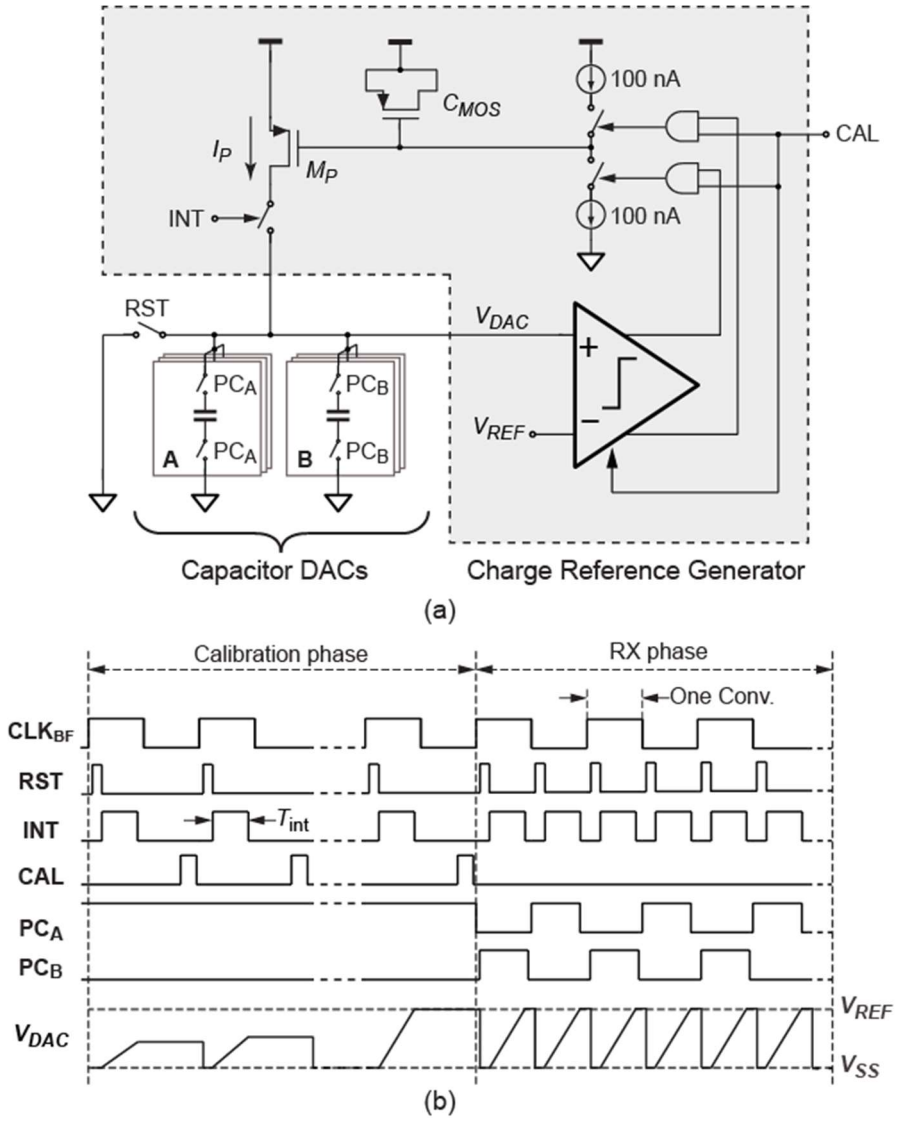


Figure 3. 7 Operation principle of charge-reference generation.

where I_P is the precharging current and Tint is the precharging duration defined on-chip. It is, however, difficult to maintain uniformity of Q_{REF} across the whole array, since both I_P and T_{int} are subject to process variations and mismatch. Therefore, we define the charge reference as:

$$Q_{REF} = C_{DAC} \cdot V_{REF}$$

where C_{DAC} is the total capacitance of the DAC array and V_{REF} is the desired voltage reference with respect to the AFE output.

As the absolute value of capacitors in modern CMOS processes is typically more strictly controlled [39], calibration is applied to I_P so that the voltage on C_{DAC} (V_{DAC}) after precharging approaches V_{REF}. This is accomplished by introducing a calibration phase in synchronization with the TX phase, when digitization is not required. During this phase, the charge-pump and the

calibration comparator are periodically activated in a short time interval (CAL) following each precharging cycle. The calibration comparator compares V_{DAC} to V_{REF}, and according to the result a unit charge packet is pumped in or pulled out from a MOS memory capacitor (C_{MOS}) at the gate of M_P to adjust the value of I_P for the next cycle. The size of the charge packet, which dictates the reference calibration resolution (LSB_{CAL}), is set by both the pulse duration time and the magnitude of the sourcing/sinking current in the charge pump. This process repeats for a defined number of cycles, at the end of which V_{DAC} has converged to V_{REF} to within ±1 LSB_{CAL}.

During the RX phase, both the charge pump and the calibration comparator are disabled, and the gated current source precharges C_{DAC} based on the bias voltage stored on C_{MOS}. The leakage on C_{MOS} (~ 4 pF) would lead to a worst-case gain drift of 0.3 dB within one RX cycle (100 μs), which is negligible given the significant time-dependent attenuation of ultrasound. The broadband white noise of the charge pump is sampled on C_{MOS} and held constant throughout the RX phase, and therefore does not contribute any in-band noise.

Both the precharging current noise and the jitter of T_{int} lead to noise charge sampled on C_{DAC}. The former is minimized by appropriate sizing of transistor M_P (WP/LP << 1), leaving jitter of the precharging clock as the dominant noise source. This clock is derived from the ASIC input clock, whose jitter performance is therefore crucial. Maximizing T_{int} helps in relaxing the jitter requirements. To do so, we use a ping-pong charge reference that consists of two identical capacitor DAC arrays, as shown in Fig. 3.7. A duration time of 25 ns (3/4 of the sampling clock period) is allocated for T_{int}, permitting the use of a system clock with moderate jitter (~ 20 ps).

In the calibration phase, only one DAC array is connected to the gated current source, while in the RX phase they are alternately used for precharging and conversions. By sharing the current source for precharging and the timing logic for generating T_{int}, the ping-pong charge reference is free from interleaving spurs caused by the DAC capacitance mismatch.

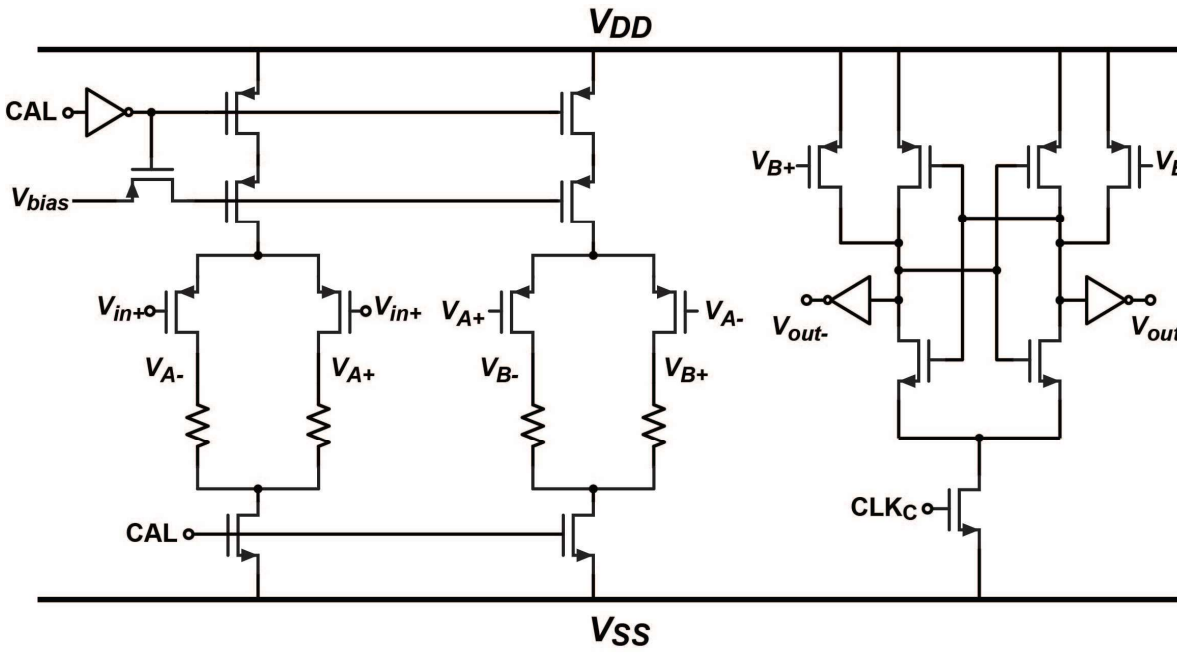


Figure 3. 8 The calibration comparator for charge-reference generation.

The topology of each DAC array is similar to [37]. The charge references corresponding to the first 7 MSBs are produced by precharging a bank of binary-scaled capacitors, while those corresponding to the last 3 LSBs are generated using charge redistribution. Metal-oxide-metal (MOM) capacitors of 23 fF with symmetric plate parasitic capacitance are utilized as unit capacitors to ensure adequate matching for a 10-bit linearity. In total, 67 unit capacitors are used in each DAC, leading to a total capacitance of about 1.5 pF.

The required reference voltage is determined by the following charge-balancing equation:

$$N \cdot V_{in,max} \cdot C_M = 4 \cdot V_{REF} \cdot C_{DAC}$$

where N is the number of subarray elements, $V_{in,max}$ is the maximum peak-to-peak differential PGA output swing and C_M is the capacitance of a unit memory cell in a delay line of the beamformer. The factor of 4 comes from the single-ended-to -differential conversion of C_{DAC}. For N = 9, $V_{in,max}$ = 800 mV, C_M = 133 fF and $C_{DAC} \approx$ 1.5 pF, V_{REF} is approximately 160 mV.

The calibration comparator is implemented as a StrongArm latch following a class-A preamplifier that is only powered during calibration (Fig. 3.8). The preamplifier consists of two cascaded stages of resistively-loaded differential pairs to warrant a sufficient gain. The first stage is dimensioned to minimize both noise and offset. Given the relatively low reference voltage, a pMOS input pair

is used. Since the comparator is powered down during the RX phase, its contribution to the overall power consumption is negligible.

3.3.3 SAR Logic

For an implementation in 0.18 µm CMOS, the high-speed SAR logic readily dominates the power consumption of the ADC, and therefore needs to be carefully minimized. Fig. 3.9 shows the schematic and the timing diagram of the proposed asynchronous SAR logic. The differential outputs of the dynamic comparator (CPout+/-) directly trigger a 10-stage differential shift-register, where each stage consists of a pair of D-flip-flops (DFFs) with an enable input. Compared to conventional implementations [29, 30], the proposed scheme minimizes the time delay between the comparator decision and the DAC switching, thus relaxing the timing for charge sharing. During the conversion, each DFF pair reads the comparator decision by sensing the rising edges of the comparator outputs. Once a rising edge on either side is detected, the DFF pair is immediately disabled and no longer responsive to succeeding comparison events until the end of the cycle. The data is then captured and frozen to control the switching of corresponding DAC elements. To identify the completion of a conversion, the enable signal of the LSB DFF is used as the DataReady signal. An additional DFF pair is used for comparator offset calibration, as will be discussed in Section 3.3.4.

To further reduce the dynamic power consumption, each DFF pair is kept deactivated until the preceding stage has come to a decision. Thus, in every bit-cycle only one DFF pair is clocked for data reading. This is achieved by embedding a local clock-gating buffer within each DFF cell, which defines a bit-wise timing window based on the outputs of the previous and the present stages (Fig. 3.9c). The clock-gating buffer is implemented as a dynamic NAND gate followed by a simple latch with a weak feedback inverter [40] (Fig. 3.9b). To prevent undesired switching events, the output of the previous stage is delayed to guarantee that its rising edge always arrives during the reset phase of the dynamic

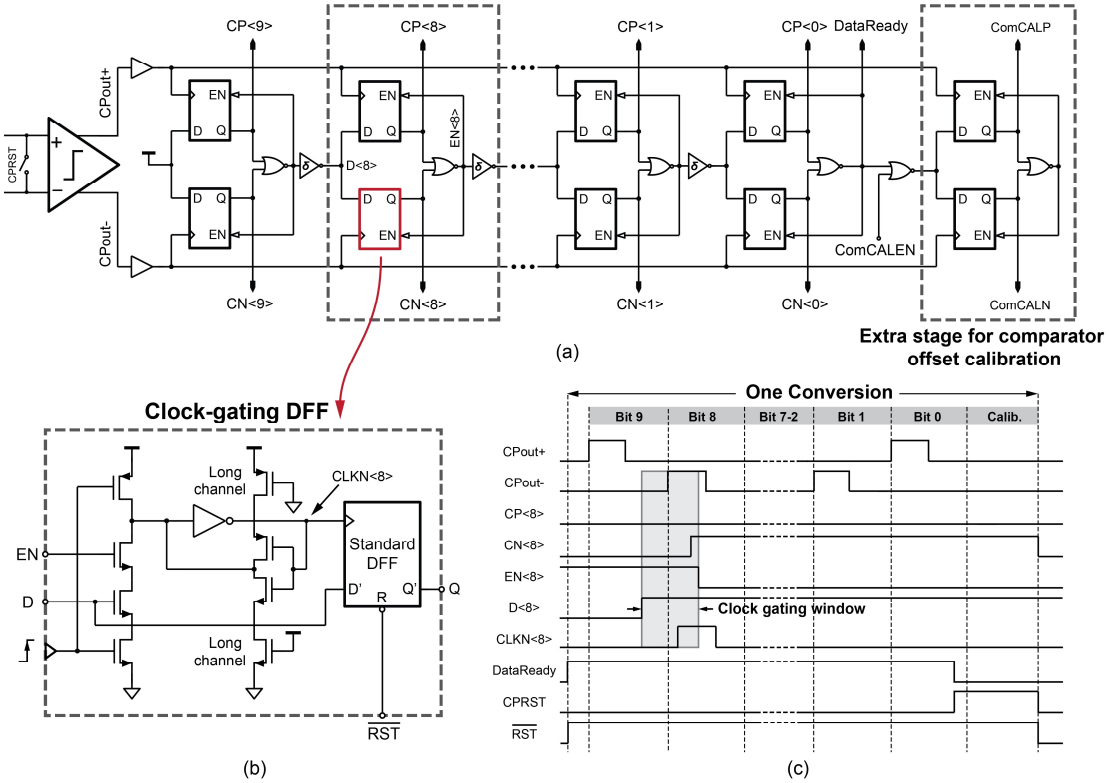


Figure 3. 9 (a) Schematic of the proposed asynchronous SAR logic; (b) the clock-gating D-flip-flop; (c) timing diagram in each conversion.

comparator. Simulation results indicate a 33% dynamic power reduction in the SAR logic thanks to the adoption of the clock-gating scheme.

3.3.4 Dynamic Comparator

An inherent limitation of the charge-sharing SAR conversion is the discrepancy between the charge-domain signal approximation and the voltage-domain quantization, which leads to more stringent requirements on the input-referred noise and offset of the dynamic comparator [37]. Fig. 3.10 shows the schematic of the dynamic comparator, the core of which is a double-rail latch-type voltage sense amplifier [41]. Its first stage is sized to ensure a sufficiently low input-referred noise. A self-timer circuit takes the comparator outputs and the DataReady signal to generate an oversampling clock that schedules the evaluation and reset of the dynamic comparator.

In contrast to a voltage-domain SAR ADC, the input offset of the comparator in a charge-sharing ADC would result in a dynamic charge offset that degrades the conversion linearity [37], and therefore should be minimized. Such offset is dependent on the input common-mode voltage [30] during charge sharing, which, in turn, depends on the parasitic capacitance at the summing nodes and therefore

varies between subarrays. To avoid the need for individual offset trimming for each subarray, the offset is self-calibrated in a way similar to [42], which involves a charge pump and an auxiliary input pair with one gate connecting to an external calibration voltage. In contrast with [42], the offset calibration is performed in the background while the SAR conversion is on-going. As described in Section 3.2.3, the comparator input nodes are shorted to clear the residual charge at the end of each conversion, resulting in an input voltage that is close to the common-mode voltage during the LSB cycles. Therefore, by triggering one more comparison, the polarity of the offset can be detected, allowing the charge pump to adjust the bias voltage of the auxiliary input pair. This additional comparison is realized by adding an extra stage in the asynchronous SAR logic, as shown in Fig. 3.9. By repeating this process for successive SAR conversions, the offset voltage is progressively minimized within a finite number of ADC cycles. The background calibration can be disabled by nulling the input of the extra logic stage.

Because of the common-mode charge stored on the parasitic capacitances of the C_{DAC} and switches during precharging, as well as the relatively low reference voltage, the input common-mode of the comparator slightly decreases as the SAR

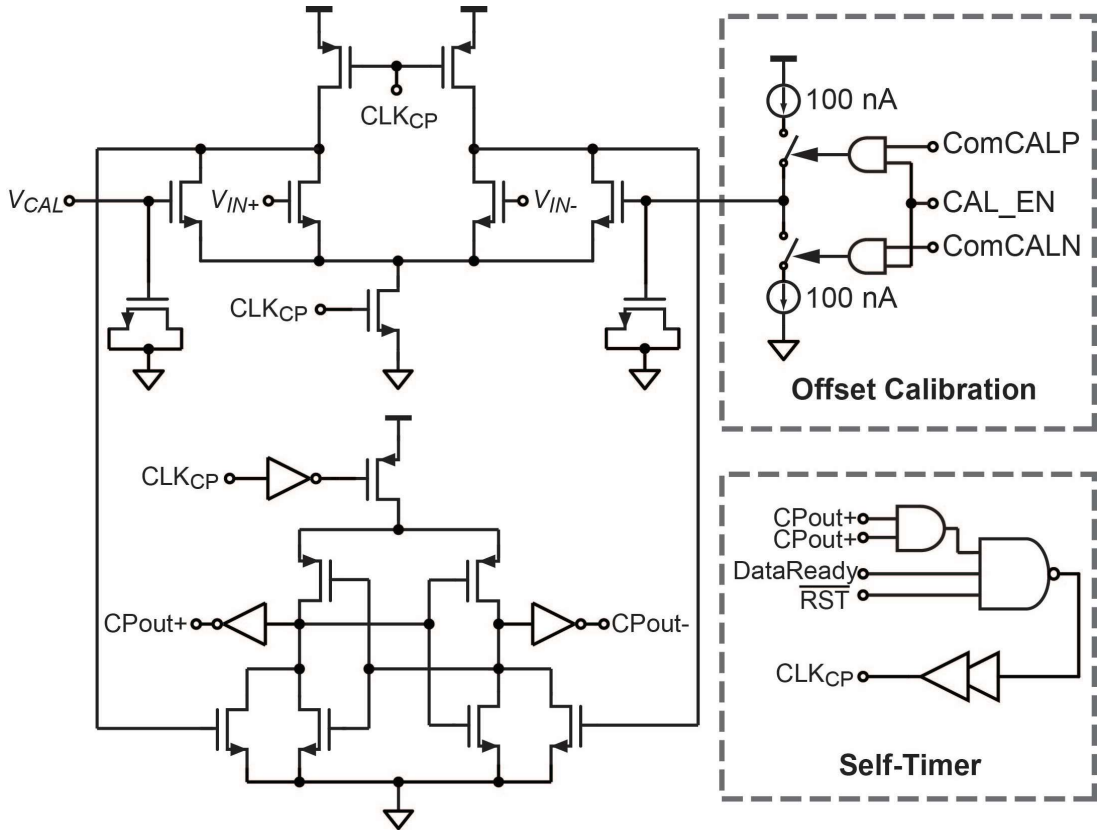


Figure 3. 10 Dynamic comparator with offset calibration.

conversion proceeds, which leads to a bit-dependent dynamic offset. However, since the variation of the input common-mode is only a small portion of its absolute value, the resulting offset variation and dynamic error charge have a negligible impact on the linearity.

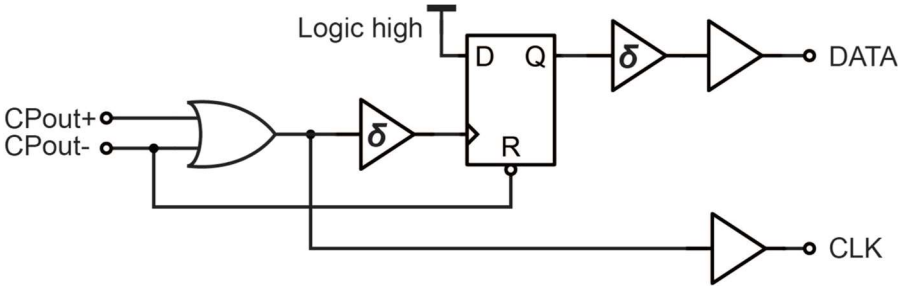


Figure 3. 11 Clock-data-recovery circuit

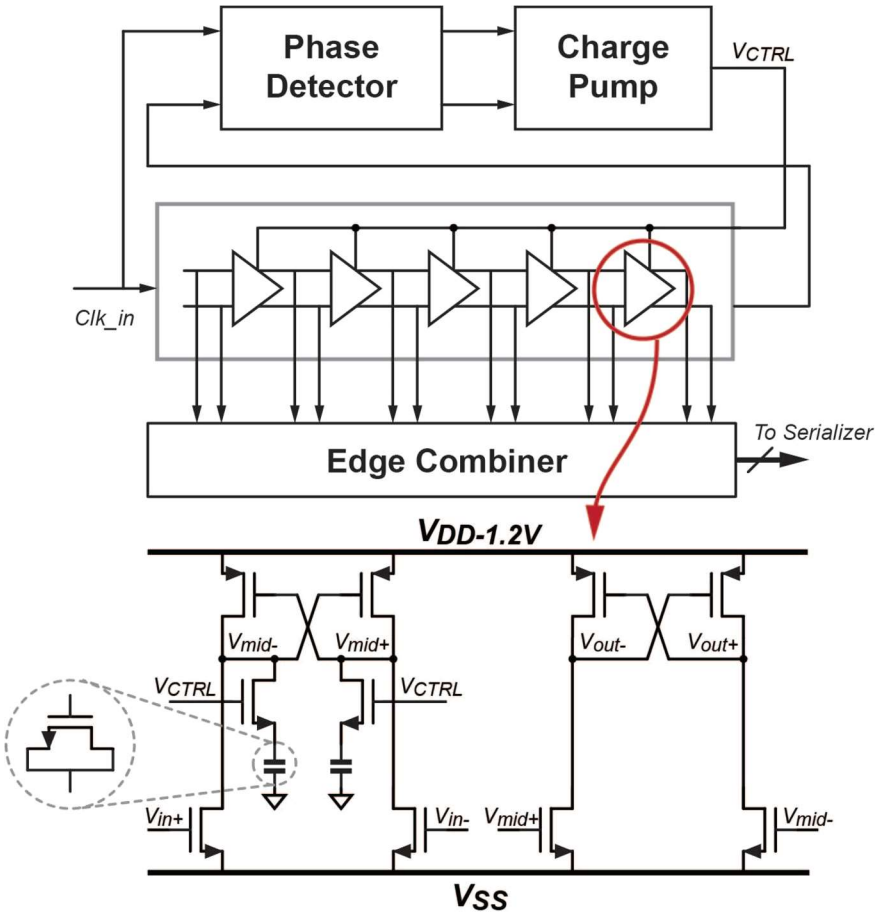


Figure 3. 12 Delay-lock-loop

3.3.5 CDR and FIFO

The differential comparator outputs from each subarray are received by CDR circuits at the ASIC periphery, which reconstruct the serial ADC output and a

corresponding asynchronous clock (Fig. 3.11). Since the comparator outputs are in RZ format, the clock can be reconstructed from an "OR" operation of the two outputs. A DFF driven by this clock reconstructs the serial ADC data. The DFF has a constant logic high input and is reset by the negative comparator output (CPout-). Proper delays are added to enhance the circuit's immunity to timing uncertainties.

The recovered clock and data are fed to a dual-clock FIFO for further synchronization. The "read" operation of the FIFO is driven by the 300 MHz global clock. In order to simplify the data reconstruction at the system side, once a valid data stream is received, the FIFO is expected to operate in neither "empty" state nor "full" state. The "full" state is avoided by selecting a FIFO queue-depth of 16, more than the 10 bits of a single conversion result. To avoid the "empty" state, a 5-cycle delay is applied between the start of the "write" operation and the start of the "read" operation to make sure that enough data is written to the FIFO before reading. The FIFO and the following encoders were implemented and optimized using logic synthesis tools. To enable a bit-error-rate (BER) test for the high-speed data exportation, the FIFO inputs can be switched to the output of an on-chip pseudo-random bit sequence (PRBS) generator with a sequence length of 2^{16}-1.

3.3.6 DLL

Fig. 3.12 shows a block diagram of the DLL, which is based on [43]. It consists of a 5-stage differential voltage-controlled delay line (VCDL), a phase detector, a charge-pump and an edge combiner. The delay cell in the VCDL is implemented by cascading two differential cross-coupled inverters, the first of which is loaded by RC branches consisting an NMOS switch and a MOS capacitor. By increasing the switch control voltage V_{CTRL}, more capacitance is added to the inverter's load, thus increasing the delay. Once the loop is stable, the edge combiner receives the outputs of the delay cells and generates five consecutive equal-width pulses, which are fed into a 10:1 multiplexer for data serialization.

3.4 Experimental Results

The ASIC has been fabricated in a 0.18 μm 1P6M low-voltage CMOS process and has an area of 4.8 × 2.5 mm^2, as shown in Fig. 3.13a. The floor plan of a 3 × 3 subarray receiver is shown in Fig. 3.13b, while its power and area breakdown

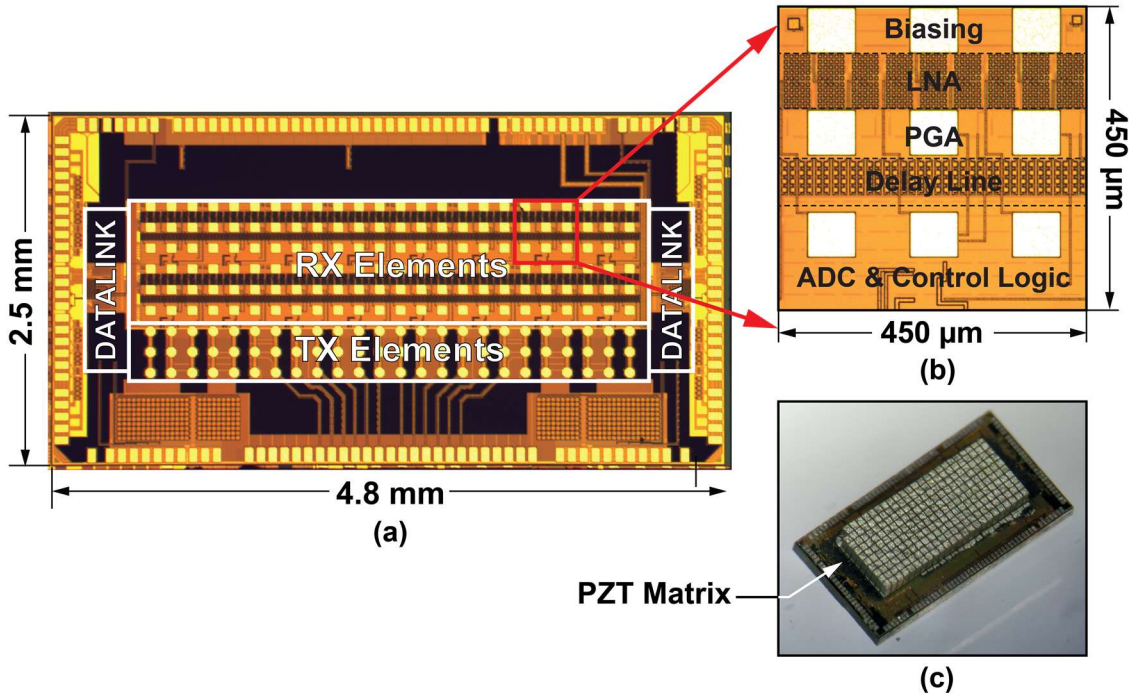


Figure 3. 13 Chip microphotograph (a), (b) and prototype with fabricated PZT matrix (c)

are shown in Fig. 3.14. The bondpads for transducer interconnection are implemented in the top (6th) metal layer, while the 5th metal layer is reserved as a grounded shield to protect the LNA inputs from digital interference. All building blocks are powered by a 1.8 V supply except for the VCDL in the DLL, which is powered by a separate 1.2 V supply. While receiving, each subarray receiver consumes 4.3 mW, corresponding to 0.46 mW/element. The beamforming ADC along with the delay programming logic occupies about half of the subarray area, while consuming only 36% of the subarray power (1.58 mW). The total power including the datalink and LVDS drivers is 130.5 mW, corresponding to 0.91 mW/element.

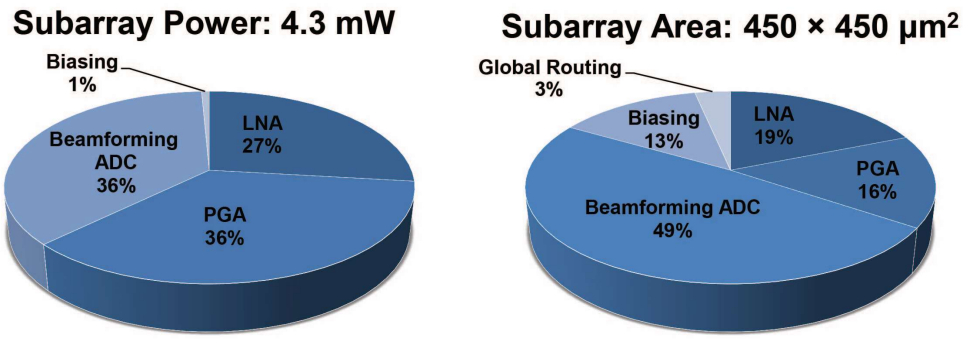


Figure 3. 14 RX subarray power and area breakdown.

Fig. 3.13c shows a fabricated prototype with an integrated 24 × 9 PZT matrix transducer. It is wire-bonded to a daughter PCB for both electrical and acoustic tests. The daughter PCB is mounted on a custom-designed mother PCB, where an FPGA receives and buffers the high-speed RF data before transmitting it to a PC for image reconstruction.

3.4.1 Electrical Measurements

The electrical performance of the prototype ASIC has been characterized by wire-bonding test input signals to the selected RX transducer pads. The reconstructed digital outputs of each subarray receiver are converted back to a voltage signal according to Eq. (3) to facilitate the performance evaluation.

Fig. 3.15 shows the measured subarray receiver transfer function at 12 AFE gain settings. It achieves an overall mid-band gain range of 49 dB, stepping from -7 dB to 42 dB with an average step size of 4.5 dB. The deviation from the ideal gain step (6 dB) is mainly caused by the insufficient open-loop gain of the PGA core amplifier at high gain modes. The average -3 dB bandwidth of the subarray receiver is measured as 11.9 MHz.

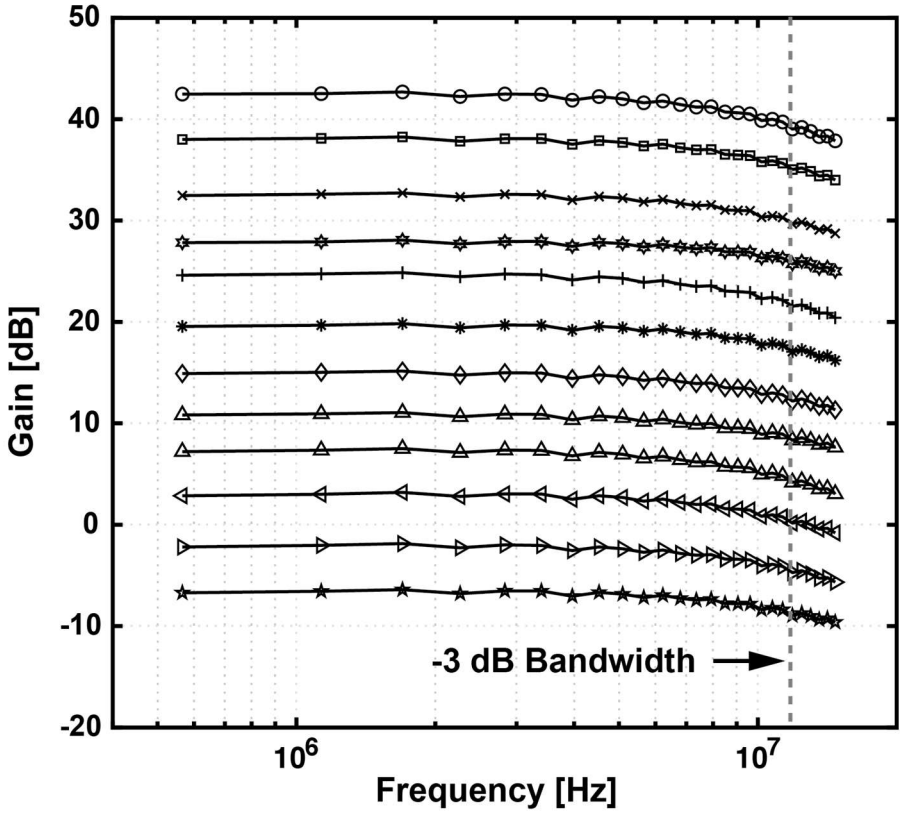


Figure 3. 15 Measured RX transfer function at 12 AFE gain settings.

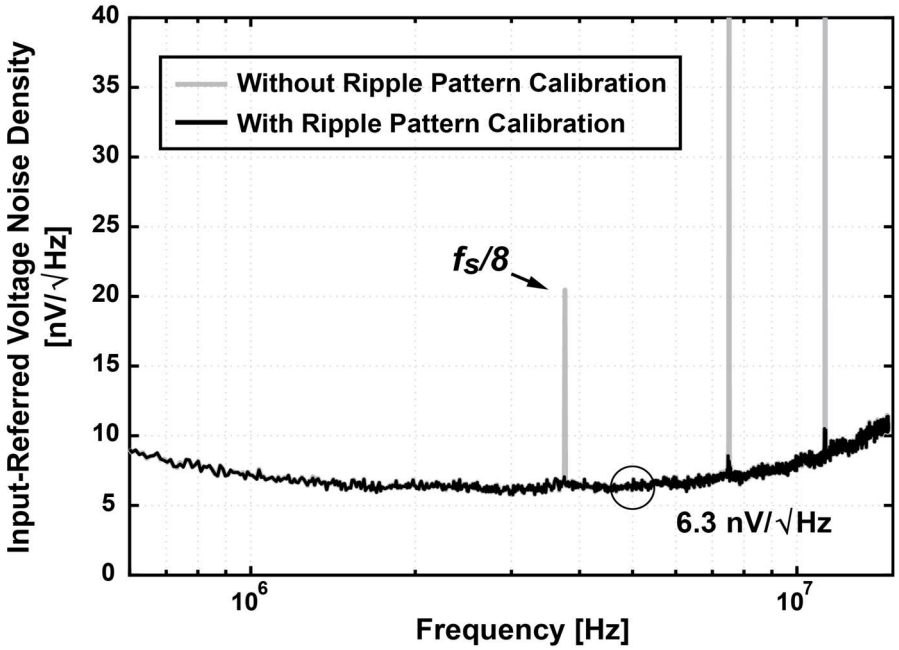


Figure 3. 16 Measured input-referred noise density spectrum of one subarray receiver.

Fig. 3.16 shows the measured subarray input-referred voltage noise spectrum at the highest AFE gain setting, which indicates an input-referred voltage noise density of 6.3 nV/√Hz at 5 MHz. Before applying the digital back-end calibration (Section 3.3.1), the ripple pattern introduced by delay line mismatches appears as in-band interference tones at fs/8 (3.75 MHz) and its harmonics. By subtracting the pre-recorded ripple pattern (obtained from 100 iterations with grounded inputs) from the output signal, these interference tones get significantly reduced from the spectrum without deteriorating the noise floor.

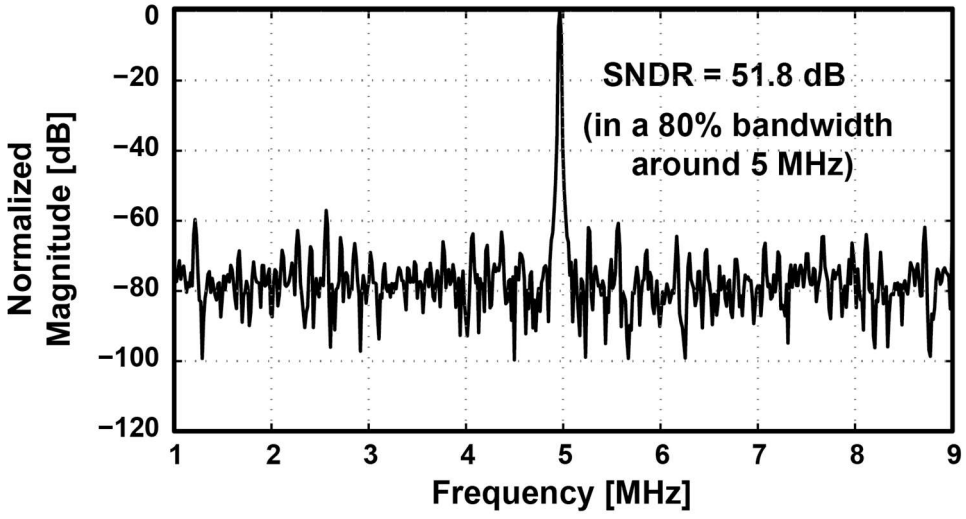


Figure 3. 17 Measured RX subarray output spectrum with a sinusoidal test input.

Fig. 3.17 shows the measured output spectrum of one subarray receiver at the highest AFE gain setting with a 4.95 MHz sinusoidal test input with a peak value

of 3.1 mV. It achieves a peak SNDR of 51.8 dB within an 80% bandwidth (3 MHz to 7 MHz) around the centre frequency (5 MHz), where the AFE dominates the noise floor.

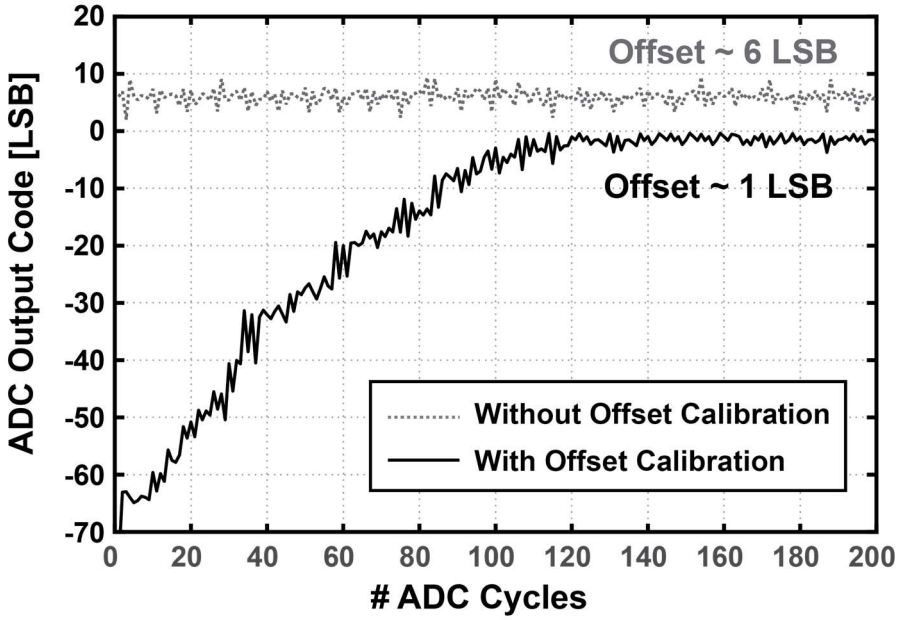


Figure 3. 18 Convergence of the background comparator offset calibration process.

Fig. 3.18 shows the transient response of one subarray output with the proposed background comparator offset calibration enabled. Upon initialization, the offset settling process takes about 120 ADC cycles (~ 4 μs) to converge. Without calibration, the original output offset of the tested subarray (also shown in Fig. 3.18) is about 6 LSB, which is reduced to -1 LSB after calibration.

The high-speed datalink has been evaluated separately using the on-chip PRBS generator, which shows a BER better than 10^{-9} across 1 m coaxial cables (HQDP-020, Samtec, New Albany, IN, USA). To better demonstrate the channel-

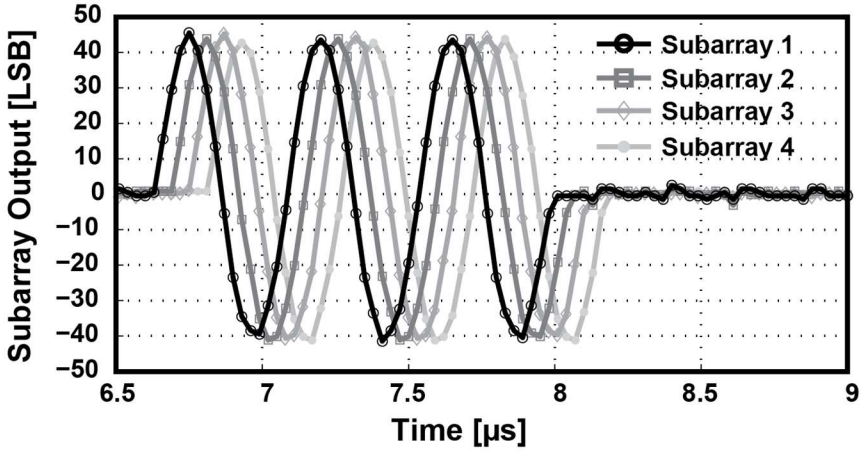


Figure 3. 19 Reconstructed 4-Subarray outputs from a single LVDS channel.

TABLE I. COMPARISON TO PRIOR WORK

	This Work	ISSCC'14 [Um]	ISSCC'17 [MCh]	TBCAS'17 [Ki]	EMB'15 [Chira]	VLSI'16 [CC]
Process	**180 nm**	130 nm	28 nm	130 nm	130 nm	180 nm
Transducer	**PZT**	CMUT	CMUT	N/A	N/A	PZT
RX Array Size	**24 × 6**	64 × 1	4 × 4	N/A	N/A	32 × 32
No. of Channels	**144**	64	16	64	128	864
Center freq.	**5 MHz**	3 MHz	5 MHz	5 MHz	2.5 – 4.5 MHz	5 MHz
RX Architecture	**AFE+Analogue S/H + ADC + Datalink**	Analogue S/H + ADC + FIFO	AFE+ADC + FIFO	ADC + FIFO	ADC + Datalink	AFE+ Analogue S/H
ADC Architecture	**SAR**	SAR	ΔΣ	SAR	ΔΣ	N/A
Nyquist rate	**30 MHz**	20-40 MHz	20 MHz (OSR = 48)	20-40 MHz	20 MHz (OSR = 24)	33 MHz
Pitch-Matched	**Yes (150 µm)**	No	Yes (250 µm)	No	No	Yes (150 µm)
Channel Reduction	**36-fold**	64-fold	16-fold	64-fold	2-fold	9-fold
Integration Method	**Direct Integration**	Wire-bonding	Flip-chip	Wire-bonding	Wireless	Direct Integration
Delay Resolution	**33 ns**	6.25 ns	8.33 ns	6.25 ns	N/A	30 ns
Active Area/el.	**0.026 mm^2***	0.303 mm^2	0.088 mm^2	0.473 mm^2	N/A	0.023 mm^2
RX Power/el.	**0.91 mW***	17.81 mW	33.19 mW	9.45 mW	36.1 mW	0.27 mW
Peak SNDR	**51.8 dB**	N/A	58.9 dB**	48.5 dB***	65 dB	52 dB

* Including the datalink and LVDS drivers.

**ADC only, excluding the analogue front-end.

*** Calculated as signal power/noise power, measured without mismatching scrambling.

reduction capability of the datalink, we programmed 4 subarrays that share the same high-speed data output channel with differential uniform delays (33 ns, 100 ns, 166 ns and 233 ns). A 3-cycle sinusoidal signal is chosen as the common input to these subarrays, with a frequency of 2 MHz so as to better illustrate the relative time delay. Fig. 3.19 depicts the reconstructed time-domain output waveform of these 4 subarrays, recovered from the shared LVDS output port, which clearly shows the expected relative time delays. The worst-case inter-subarray crosstalk is measured as -57 dBc. The measured gain mismatch across 16 subarrays is less than 0.1 dB.

Table I compares this work with state-of-the-art digitization solutions for 3-D ultrasound imaging systems [16-18, 44]. Based on the table, this work achieves a 10 × improvement in power efficiency, as well as a 3.3 × improvement in integration density. When compared with our previous analogue output receiver ASIC [1], the subarray digitization only costs about 70 % extra power and is realized within the same die size. On the other hand, the high-speed datalink introduces a non-negligible power overhead due to the relatively large feature size of the chosen technology. This, however, can be reduced in the future by adopting a more advanced CMOS technology, or applying on-chip digital beamforming [14] or compression techniques [15].

3.4.2 Acoustic Measurements

The acoustic performance of the fabricated prototype has been characterized by mounting a waterbag on top of the PZT-on-ASIC assembly, as shown in Fig. 3.20a. A 3-needle phantom was immersed in water and placed at about 20 mm in front of the PZT matrix. A diverging wave was transmitted from the prototype by driving 6 elements at the center of the TX subarray (Fig. 3.2) using 20 V (peak-

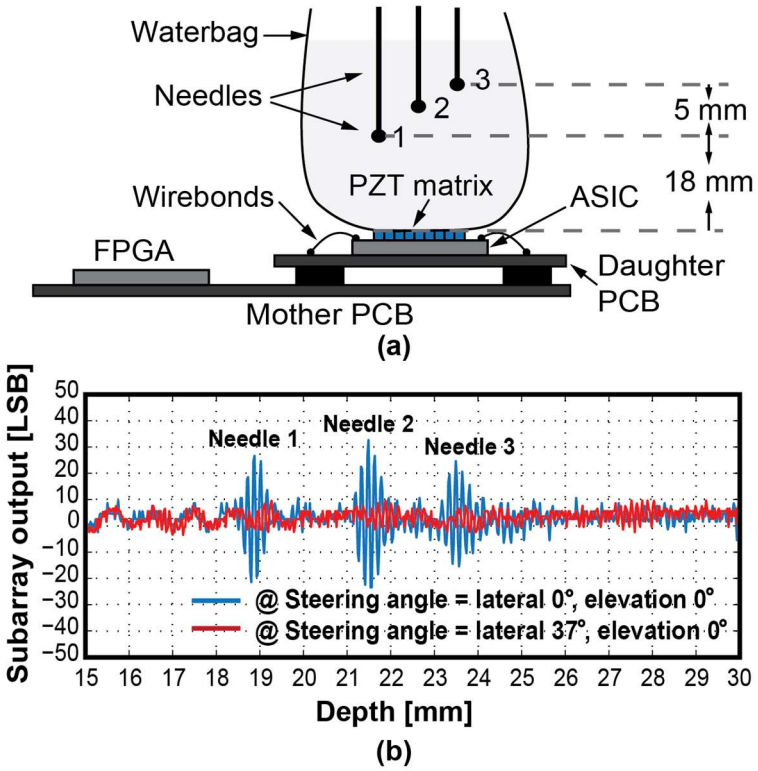


Figure 3. 20 (a) Setup for imaging experiments. (b) Recorded subarray output waveforms with different lateral steering angles.

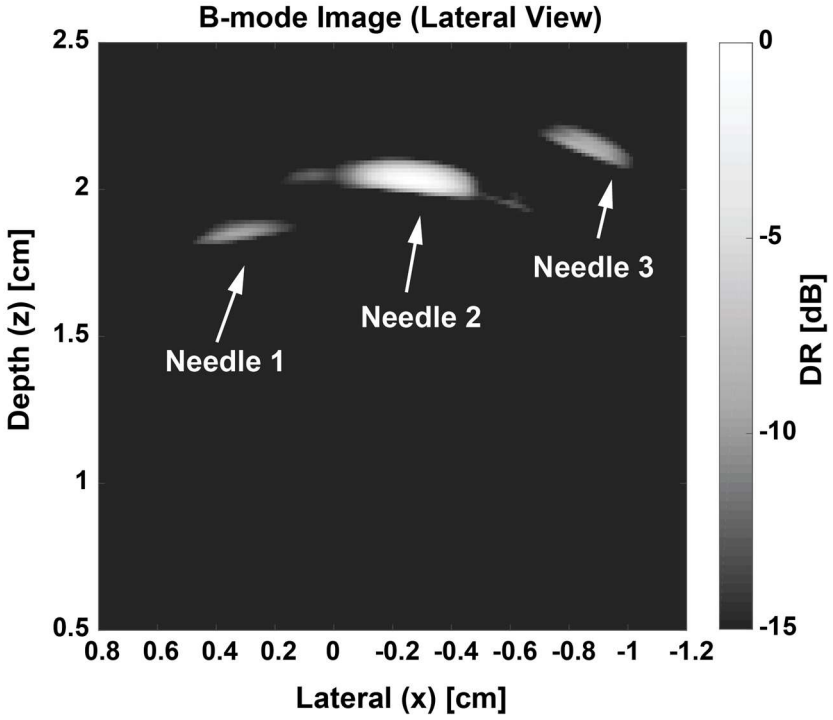


Figure 3. 21 Reconstructed B-mode image. The visible side-lobes of Needle 2 are as expected for the relatively small RX aperture.

to-peak) 3-cycle pulses. In several successive TX-RX cycles, the 16 subarrays in the prototype were steered to different angles to scan the volume.

Fig. 3.20b shows the recorded digital outputs of one subarray receiver with different programmed steering angles at the lateral direction. It clearly shows an increase of the echo amplitude when the subarray beamformer is steered towards the specific needle.

Fig. 3.21 illustrates a reconstructed B-mode image in the lateral direction. It is obtained by recording and combining the digital outputs of all subarrays, and performing the post-beamforming computation in software. The positions of all 3 needles are clearly shown in the image with a spatial resolution in line with the relatively small RX aperture.

The image was reconstructed from 25 beams (TX/ RX cycles) with a PRF of 5 kHz, leading to a theoretical volume rate of 200 volumes/second. In practice, however, the imaging rate is limited by the data transfer speed between the FPGA and the PC, as well as the software post-beamforming computing time. This constraint could be resolved by migrating the image reconstruction function to the FPGA [45], or implementing it in a digital ASIC [14]; adopting a graphics processing unit (GPU) can be another promising solution to speed up the long post-beamforming computing time [46].

3.5 Conclusions

We have presented a front-end ASIC that enables power- and area-efficient in-probe digitization for next-generation endoscopic and catheter-based 3-D ultrasound imaging systems. It employs a low-power beamforming ADC to realize an additional 4-fold channel count-reduction compared to prior analogue subarray beamformer designs. The ADC directly digitizes the subarray beamformer output in the charge domain to eliminate the need for intermediate buffers, resulting in significant reduction in power consumption and silicon area. Self-calibrated charge-references are proposed to further optimize the power-efficiency as well as facilitate the system-level design. The ASIC achieves an overall 36-fold channel-count reduction and a state-of-the-art power-efficiency with less than 1 mW/element power dissipation in receive, which is acceptable even when scaled up to a 1000-element probe. A fabricated prototype with integrated transducer has been successfully applied in preliminary 3-D imaging experiments.

References

[1] C. Chen et al., "A Front-End ASIC With Receive Sub-array Beamforming Integrated With a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography," *IEEE J. Solid-State Circuits,* vol. 52, no. 4, pp. 994 - 1006, 2017.

[2] D. Wildes et al., "4-D ICE: A 2-D Array Transducer With Integrated ASIC in a 10-Fr Catheter for Real-Time 3-D Intracardiac Echocardiography," *IEEE Trans. Ultrason., Ferroelect., Freq. Control,* vol. 63, no. 12, pp. 2159-2173, 2016.

[3] M. Tan et al., "A front-end ASIC with high-voltage transmit switching and receive digitization for forward-looking intravascular ultrasound," in *IEEE Custom Integrated Circuits Conference (CICC),* Austin, TX, 2017.

[4] G. Gurun et al., "Single-Chip CMUT-on-CMOS Front-End System for Real-Time Volumetric IVUS and ICE Imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Control,* vol. 61, no. 2, pp. 239-250, 2014.

[5] I. O. Wygant et al., "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control,* vol. 55, no. 2, pp. 327-342, Feb. 2008.

[6] C. Chen et al., "A Prototype PZT Matrix Transducer with Low-Power Integrated Receive ASIC for 3-D Transesophageal Echocardiography," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control,* vol. 63, no. 1, pp. 47 - 59, Jan. 2016.

[7] B. Savord and R. Solomon, "Fully Sampled Matrix Transducer for Real Time 3D Ultrasonic Imaging," in *Proc. IEEE Ultrasonics Symp.*, 2003, pp. 945-953.

[8] Z. Yu et al., "Front-end receiver electronics for a matrix transducer for 3D transesophageal echocardiography," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control,* vol. 59, no. 7, pp. 1500-1512, Jul. 2012.

[9] Y. Katsube et al., "Single-Chip 3072ch 2D Array IC with RX Analog and All-Digital TX Beamformer for 3D Ultrasound Imaging," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap.,* 2017, pp. 458-459.

[10] C. Daft, S. Panda, P. Wagner, and I. Ladabaum, "Two Approaches to Electronically Scanned 3D Imaging Using cMUTs " in *IEEE Int. Ultrason. Symp. (IUS),* 2006, pp. 685-688.

[11] T. M. Carpenter, M. W. Rashid, M. Ghovanloo, D. M. J. Cowell, S. Freear, and L. D. F, "Direct Digital Demultiplexing of Analog TDM Signals for Cable Reduction in Ultrasound Imaging Catheters," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control,* vol. 63, no. 8, pp. 1078 - 1085, 2016.

[12] Q. Liu, C. Chen, Z. Chang, C. Prins, and M. A. P. Pertijs, "A mixed-signal multiplexing system for cable-count reduction in ultrasound probes," in *IEEE International Ultrasonics Symposium (IUS),* Oct. 2015, pp. 1 - 4.

[13] M. W. Rashid, C. Tekes, M. Ghovanloo, and F. L. Degertekin, "Design of Frequency-Division Multiplexing Front-End Receiver Electronics for CMUT-on-CMOS Based Intracardiac Echocardiography," in *IEEE Int. Ultrason. Symp. (IUS),* 2014, pp. 1540-1543.

[14] B. Lam, M. Price, and A. P. Chandrakasan, "An ASIC for Energy-Scalable, Low-Power Digital Ultrasound Beamforming," in *Proc. IEEE International Workshop on Signal Processing Systems,* 2016, pp. 57-62.

[15] T. Chernyakova and Y. C. Eldar, "Fourier-Domain Beamforming: The Path to Compressed Ultrasound Imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Control,* vol. 61, no. 8, pp. 1252-1267, 2014.

[16] J.-Y. Um et al., "An analog-digital-hybrid single-chip RX beamformer with non-uniform sampling for 2D-CMUT ultrasound imaging to achieve wide dynamic range of delay and small chip area," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap.,* Feb. 2014, pp. 426 - 427.

[17] M.-C. Chen et al., "A Pixel-Pitch-Matched Ultrasound Receiver for 3D Photoacoustic Imaging with Integrated Delta-Sigma Beamformer in 28nm UTBB FDSOI," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap.,* 2017, pp. 456-457.

[18] Y.-J. Kim et al., "A Single-Chip 64-Channel Ultrasound RX-Beamformer Including Analog Front-End and an LUT for Non-Uniform ADC-Sample-Clock Generation," *IEEE Trans. Biomed. Circuits Syst. ,* vol. 11, no. 1, pp. 87-97, 2017.

[19] M. D'Urbino et al., "An Element-Matched Band-Pass Delta-Sigma ADC for Ultrasound Imaging," in *IEEE Asian Solid-State Circuits Conference (A-SSCC),* 2017.

[20] U. S. Food and Drug Administration (FDA), "Guidance for Industry and FDA Staff–Information for Manufacturers Seeking Marketing Clearance of Diagnostic Ultrasound Systems and Transducers," Sept. 2008.

[21] T. Kim and S. Kim, "A 12.1mW, 60dB SNR, 8-Channel Beamforming Embedded SAR ADC for Ultrasound Imaging Systems," in *IEEE Asian Solid-State Circuits Conference (A-SSCC),* 2017, pp. 141-144.

[22] C. Chen et al., "A 0.91mW/Element Pitch-Matched Front-End ASIC with Integrated Subarray Beamforming ADC for Miniature 3D Ultrasound Probes," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap.,* 2018, pp. 1-2.

[23] Altera, "Cyclone V Device Datasheet," 2016.

[24] Z. Yu, M. A. P. Pertijs, and G. C. M. Meijer, "An ultrasound beamformer using pipeline-operated S/H delay stages and charge-mode summation," *Electron. Lett.,* vol. 47, no. 18, pp. 1011-1012, Sept. 2011.

[25] D. Bera et al., "Multiline 3D beamforming using micro-beamformed datasets for pediatric transesophageal echocardiography," *Phys. Med. Biol.*, vol. 63, no. 7, Apr. 2018.

[26] P. Santos, G. U. Haugen, L. Løvstakken, E. Samset, and J. D'hooge, "Diverging Wave Volumetric Imaging Using Subaperture Beamforming,"

IEEE Trans. Ultrason., Ferroelectr., Freq. Control, vol. 63, no. 12, pp. 2114-2124, Dec. 2016.

[27] B. D. Steinberg, "Digital Beamforming in Ultrasound," *IEEE Trans. Ultrason., Ferroelect., Freq. Control,* vol. 39, no. 6, pp. 716-721, 1992.

[28] B. Murmann. ADC Performance Survey 1997-2017. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[29] Y. Zhu et al., "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits,* vol. 45, no. 6, June 2010.

[30] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *IEEE J. Solid-State Circuits,* vol. 45, no. 4, pp. 731-740, April 2010.

[31] M. J. Kramer, E. Janssen, K. Doris, and B. Murmann, "A 14 b 35 MS/s SAR ADC Achieving 75 dB SNDR and 99 dB SFDR With Loop-Embedded Input Buffer in 40 nm CMOS," *IEEE J. Solid-State Circuits,* vol. 50, no. 12, pp. 2891-2900, 2015.

[32] J. Craninckx and G. V. d. Plas, "A 65fJ/Conversion-Step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," presented at the *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Pap.,* 2007.

[33] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-µm CMOS," IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2669-2680, Dec. 2006.

[34] A. X. Widmer and P. A. Franaszek, "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," *IBM Journal of Research and Development,* vol. 27, no. 5, pp. 440-451, Sept. 1983.

[35] C. Chen, Z. Chen, Z. Chang, and M. A. P. Pertijs, "A compact 0.135-mW/channel LNA array for piezoelectric ultrasound transducers," in *European Solid-State Circuits Conference (ESSCIRC)*, 2015, pp. 404 - 407.

[36] K. A. Ng and Y. P. Xu, "A Compact, Low Input Capacitance Neural Recording Amplifier," *IEEE Trans. Biomed. Circuits Syst.,* vol. 7, no. 5, pp. 610-620, 2013.

[37] B. Malki, T. Yamamoto, B. Verbruggen, P. Wambacq, and J. Craninckx, "A 70 dB DR 10 b 0-to-80 MS/s Current-Integrating SAR ADC With Adaptive Dynamic Range," *IEEE J. Solid-State Circuits,* vol. 49, no. 5, pp. 1173-1183, 2014.

[38] J. Kuppambatti and P. R. Kinget, "Current Reference Pre-Charging Techniques for Low-Power Zero-Crossing Pipeline-SAR ADCs," *IEEE J. Solid-State Circuits,* vol. 49, no. 3, pp. 683-694, 2014.

[39] B. Razavi, Design of Analog CMOS Integrated Circuits. Boston: McGraw-Hill, 2001.

[40] A. G. M. Strollo, E. Napoli, and D. D. Car0, "New Clock-Gating Techniques for Low-Power Flip-flops," in *International Symposium on Low Power Electronics and Design,* Rapallo, Italy, 2000, pp. 114-119.

[41] D. Schinkel, E. Mensink, E. Klumperink, E. v. Tuijl, and B. Nauta, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," presented at the *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Pap.,* 2007.

[42] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," in *Proc. Asian Solid State Circuits Conference (A-SSCC),* 2008, pp. 269-272.

[43] H. H. Chang, J. W. Lin, C. Y. Yang, and S. I. Liu, "A Wide Range Delay-Locked Loop with a Fixed Latency of One Clock Cycle," *IEEE J. Solid-State Circuits,* vol. 37, no. 11, pp. 1021–1027, Aug. 2002.

[44] M. K. Chirala, P. Huynh, J. Ryu, and Y.-H. Kim, "A 128-ch Δ-Σ ADC based Mixed Signal IC for full Digital Beamforming Wireless Handheld Ultrasound Imaging System," in *IEEE Engineering in Medicine and Biology Society (EMBC),* 2015, pp. 1339-1342.

[45] G.-D. Kim et al., "A Single FPGA-Based Portable Ultrasound Imaging System for Point-of-Care Applications," *IEEE Transactions on Utrasonics, Ferroelectrics, and Frequency Control,* vol. 59, no. 7, pp. 1386-1394, Jul. 2012.

[46] A. F. Elnokrashy et al., "GPU-based reconstruction and display for 4D ultrasound data," in *Proc. IEEE Ultrasonics Symp.*, 2009.

CHAPTER 4

IMPACT OF BIT ERRORS IN DIGITIZED RF DATA ON ULTRASOUND IMAGE QUALITY

*Based on publication **Z. Chen**, M. Soozande, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong and M. A. P. Pertijs, "Impact of Bit Errors in Digitized RF Data on Ultrasound Image Quality", IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 67, no. 1, pp. 13-24, Jan. 2020.*

4.1 Introduction

In conventional ultrasound probes, all transducer elements are individually connected to an imaging system using cables. This approach becomes impractical with the increase of the number of elements, e.g. in 2-D transducer arrays for 3-D imaging [1], [2]. Moreover, in the case of small elements with a relatively high electrical impedance, e.g. in catheter-based transducers, the cable load leads to significant attenuation, thus reducing the image quality [3], [4]. Integration of an application-specific integrated circuit (ASIC) in the probe head, capable of locally conditioning and processing the echo signals, is a solution that can address these issues (Fig. 4.1(a)). By pre-processing the element-level echo signals, an ASIC allows the probe to use far fewer cable connections to the imaging system, thus enabling emerging miniature 3-D ultrasound probes which utilize high-density 2-D transducers (> 1000 elements) and small-size catheters [1], [5], [6].

A variety of efforts have been made recently in ASIC designs for the reduction of cable count. In [9] and [10], the cable-count limitation is addressed by using analogue time-division multiplexing (TDM) and frequency-division multiplexing (FDM), realizing eight-fold and four-fold cable-count reductions, respectively. In chapter 2, an ASIC design adopting the concept of two-step beamforming [7] has been shown. Local subarray pre-beamforming is realized by analogue micro-beamformer circuits in the ASIC, leading to an order-of-magnitude cable-count reduction by only transferring the pre-beamformed signals.

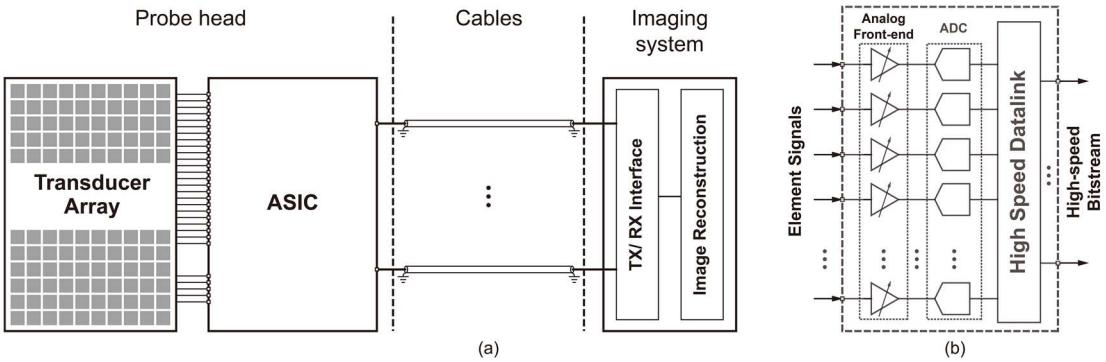


Figure 4. 1 (a) Block diagram of an ultrasound probe with in-probe ASIC; (b) Architecture of a receive ASIC with in-probe digitization

The above-mentioned approaches all suffer from the inherent vulnerability of analogue signals to crosstalk and interference, and the design complexity of analogue processing circuits. In Chapter 3, an ASIC design that utilizes massively-parallel analogue-to-digital converters (ADCs) to enable local digital signal processing (DSP) has been presented (Fig. 4.1(b)). That design successfully realizes a 4-fold channel count reduction. ASIC designs that adopted a similar concept of locally digitizing and digitally processing echoes in the ASICs can be found in [11], [12]. Compared to analogue approaches, in-probe digitization enables more robust digital data communication, allows high-speed wireline datalink technology to be leveraged to further reduce cable count, and opens the path towards the use of optical and wireless links in future ultrasound devices.

However, to be able to adopt digital datalinks in future ultrasound probes, a deep understanding on the requirements of such datalinks becomes crucial. On one hand, the datalink design is subject to stringent power constraints, especially for invasive ultrasound probes, in which in-probe power dissipation has to be limited to prevent tissue overheating [1]; on the other hand, the performance of the datalink, which is typically evaluated by the bit-error rate (BER), i.e. the ratio of the number of bit errors in a received bitstream and the total number of transmitted bits during a certain time interval, needs to be sufficient to minimize the impact of the nonideal data transmission on the reconstructed ultrasound image quality.

The BER requirement for data communication is highly application-specific and may vary by several orders of magnitude. Very low BER is often required in inter-system data connections. For instance, 1000BASE-X requires a BER better than 1E-12, as defined by the IEEE 802.3 standard [13]. On the other hand,

substantially higher BER levels are acceptable in some other applications, like telemetry in implantable devices for bio-potential recording. It has been reported in [14] that a BER below 2E-6 is sufficient to extract the spike information from recorded neural signals.

The BER requirements can have a significant impact on the power consumption of the datalink design, and on the maximum data rate that can be supported by a cable, as will be discussed in Section II. However, the impact of bit errors on ultrasound imaging has not been studied in much detail. In [15], [16], the impact of the BER on the quality of real-time echocardiogram transmission has been studied, but the transmitted data in this research is a series of reconstructed ultrasound images, not the RF data. A BER specification of 1E-5 has been reported for a wireless datalink in a capsule ultrasound imaging device [17], but without details regarding the motivation for this choice. In [18], a forward-looking IVUS probe with receive digitization has been reported with a BER of approximately 2E-3; however, the impact of the high BER on the reconstructed image quality has not yet been discussed.

This chapter investigates the impact of bit errors in digitized element-level RF signals on the reconstructed image quality. Although the motivation of this study is to understand the requirement of the datalink design in the ASIC presented in Chapter 3, we extend the scope of the study to similar ultrasound probes that utilize in-probe digitization and face similar power and cable count constraints. Rather than the specific matrix transducer used in Chapter 3, we consider in this chapter, as a first step, the simpler case of a 128-element linear-array and phased-array transducer. We propose a simulation setup to quantitatively assess image quality in the presence of bit errors based on objective image quality metrics (IQM). Moreover, the efficiency of different coding schemes for data transmission is also studied. A minimum BER requirement is derived from the simulation results, which can guide the datalink design in future ultrasound probes.

This chapter is organized as follows. Section 4.2 discusses the factors affecting BER in digital ultrasound probes. Section 4.3 introduces the proposed simulation setup for image quality analysis (IQA), followed by the simulation results in Section 4.4. Finally, Section 4.5 presents discussions and conclusions.

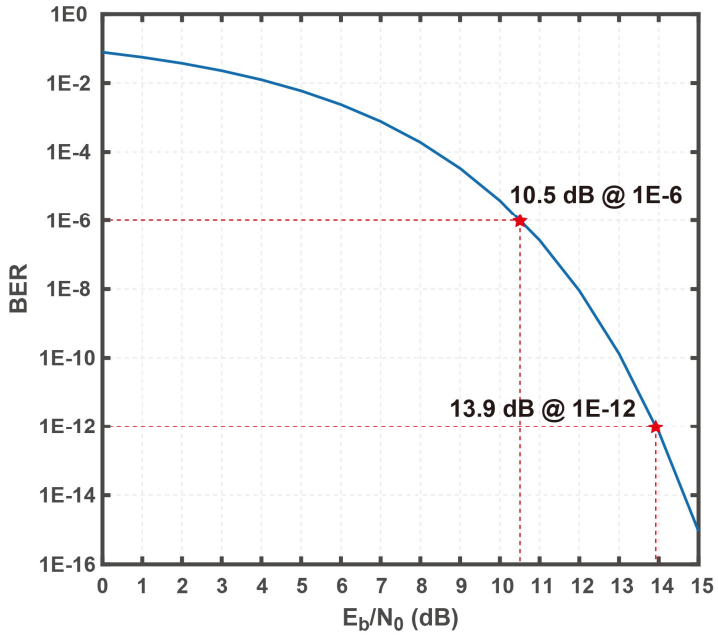


Figure 4. 2 BER vs. E_b/N_0 plot for an AWGN channel with 2-PAM coded data

4.2 BER in Data Transmission

The BER of a noise-limited communication system can be estimated from the ratio of the energy per bit and the noise power spectral density (E_b/N_0) in the receiver, where E_b is the signal energy associated with each data bit and N_0 is the noise power spectral density [19]. Fig. 4.2 shows the BER vs. E_b/N_0 curve for data with two-level pulse amplitude modulation (2-PAM) transmitted across a channel with additive white Gaussian noise (AWGN), obtained in a MATLAB simulation (The MathWorks, Inc., Natick, MA, United States). Though not all sources of bit errors can be considered as white noise, the curve is helpful to understand the relation between BER and E_b/N_0. Fig. 4.2 shows that E_b/N_0 reduces with the relaxation of the BER requirement. To achieve a BER of 1E-12, a minimum E_b/N_0 of 13.9 dB is required, while if the BER is relaxed to 1E-6, the required E_b/N_0 is also reduced to 10.5 dB.

Both E_b and N_0 are affected by the cascade of transmitter, communication channel and receiver. The nonideal channel is the most significant limiting factor of E_b/N_0 since the channel is typically subject to stringent physical constraints. Efforts need to be taken in the transmitter and receiver design to compensate the channel nonideality, to achieve the required BER. A channel inevitably introduces channel loss and noise, causing an E_b/N_0 reduction. For wireline communication using cables as channels, channel loss becomes more significant

at high frequency due to the cables' skin effect and dielectric losses [20]. Moreover, the channel dispersion introduces inter-symbol interference (ISI), i.e. the phenomenon that a symbol transmitted across the cable is affected by the preceding symbol [21]. ISI is data-dependent and cannot be considered as white noise.

To minimize the impact of ISI, a typical method is to implement equalizer circuits in the transmitter and/or the receiver to compensate for the frequency response of the channel [22]. A communication system with sufficient equalization should guarantee that ISI does not dominate the BER performance, thus making the system noise-limited.

Although the BER performance is limited by E_b/N_0, forward error detection/ correction (FEDC) coding can effectively reduce the impact of the bit errors in the received data [21], [23]. FEDC adds redundant bits to the transmitted data and allows the receiver to detect and even correct a finite number of bit errors. FEDC is required in the existing 4-PAM standard improving the raw BER from 1E-6 to 1E-12 [24]. The BER mentioned in this chapter is the raw BER measured before the error correction in the receiver.

For catheter-based/ endoscopic ultrasound imaging applications, the receivers will be implemented in the imaging system, where substantial computation power can be made available. In such a case, we can assume ISI can be fully compensated by complex equalizations in the receiver, making the system noise-limited. Then it becomes crucial to know the BER requirement of the system to maximize the data rate per cable, or to minimize E_b/N_0, and eventually the in-probe power dissipation. For example, if a datalink is transmitting data at 0.9 Gbit/s across a 2-meter Sumitomo cable (0.4DS-PBA, Sumitomo Electric) which has a nominal attenuation of 5 dB at 0.9 GHz and 8.4 dB at 2 GHz, according to Fig. 4.2, when relaxing the BER requirement from 1E-12 to 1E-6, a designer can either increase the data rate to 2 Gbit/s on the cable, or, with the same data rate, reduce the transmit power by 3.4 dB, saving half of the power consumed in the probe for data transmission.

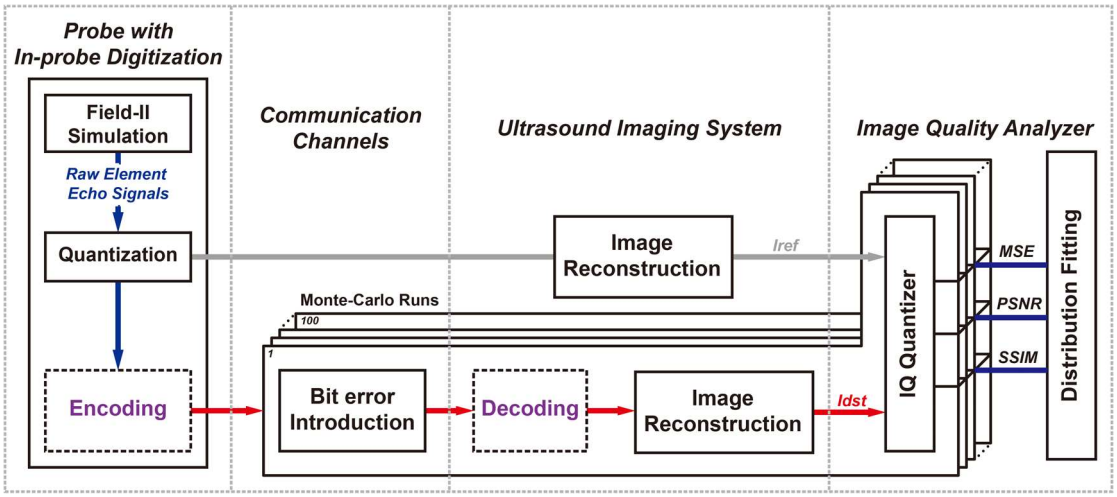


Figure 4. 3 Block diagram illustrating the simulation flow.

4.3 Evaluation Methods

4.3.1 Overview

We have performed a MATLAB simulation to emulate the proposed ultrasound system consisting of an ultrasound probe with receive digitization, a datalink and back-end image reconstruction. Fig. 4.3 illustrates the simulation flow: raw element echo signals are acquired from a simulation using the ultrasound simulation tool Field-II [25], [26] on a transducer with a predefined phantom, and then quantized and encoded in a binary format; bit errors are randomly introduced to the binary data with prescribed BER levels; a reference image I_{ref} and distorted images I_{dst} are reconstructed from the binary data before and after the bit-error introduction, respectively; lastly, objective IQMs are calculated from a 100-run Monte-Carlo simulation to evaluate the image quality of the distorted images. If FEDC is enabled, extra encoding and decoding steps are applied to the binary data before and after the introduction of the bit errors. The effectiveness of FEDC on image quality improvement can be analysed by turning on and off this option.

4.3.2 Raw Echo Data Acquisition

As representative case studies, a linear array and a phased array transducer, both with 128 elements, have been simulated using Field-II. The methodology

Table I. Simulation parameters for both the linear array and phased array transducers in Field II

	Linear Array	**Phased Array**
No. of elements	128	128
Center frequency	5 MHz	5 MHz
Wavelength (λ)	308 μm	308 μm
Element pitch	λ	λ / 2
Element width	0.9 × λ	0.9 × λ / 2
Kerf	0.1 × λ	0.1 × λ / 2
Element height	5 mm	5 mm

can also be applied to other transducers with different array sizes and array configurations, such as 2-D transducers.

Both transducers have a centre frequency of 5 MHz and a fractional bandwidth of 100%. The element pitches of the linear and phased array transducers are one wavelength and half wavelength of the centre frequency, respectively. The parameters of the two transducers are listed in Table I.

We have created a 2-D simulation phantom with a size of 40 mm × 55 mm, positioned at 10 mm from the surface of the transducers, composed of 150,000 (6.5 per wavelength) randomly distributed scatterers (Fig. 4.4). The region between the transducer and the phantom (marked by slash lines) is acoustically transparent while the speed of sound is assumed to be 1540 m/s. Four hyperechoic

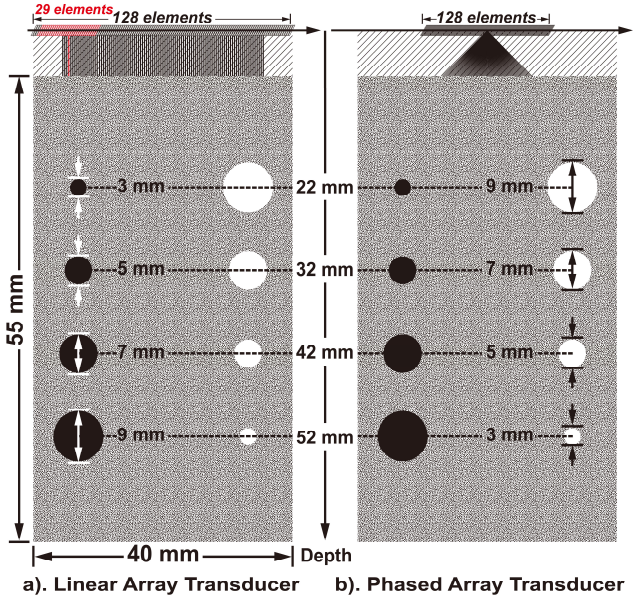


Figure 4. 4 Imaging phantom and its positioning in the Field-II simulation

and four anechoic circular regions with different diameters are placed 10 mm away from the centre of the phantom at different depths (from 22 mm to 52 mm, with a step of 10 mm), marked by the white and black circles in Fig. 4.4. All depths are measured from the transducer surface. The amplitudes of the scatterers, representing the return echo intensities, are set to 10 and 0 in the hyperechoic and anechoic regions, respectively; the amplitudes of the background scatterers are randomly set, following a Gaussian distribution with mean of 0 and standard deviation of 1.

For the linear array transducer, 29 elements are active in each pulse-echo simulation, and for the phased array transducer, all elements are active to steer beams from -45° to 45° with an angular step of 0.91°, thus forming 100 scanlines across the aperture in both cases. A fixed transmit focus point is placed at a depth of 50 mm, while multiple focal points at a depth from 10 mm to 65 mm, with a step of 5 mm are used in receive. The active elements are excited by a 2-cycle sinusoidal burst in transmit. Hamming apodization is applied in both transmit and receive. The sampling frequency in reception is set to 20 MS/s, 4 × the transducers' centre frequency. The calculated raw element echo signals are acquired and stored in two data sets. Each point in these data sets indicates a sample of the element-level echo signals. Propagation attenuation is not taken into account in the simulation for simplicity, since it is assumed that attenuation will be fully compensated for by time-gain compensation in the analogue front-end before analogue-to-digital conversion, thus leading to similar echo signals. The signals are digitized to binary data with 10-bit resolution across their full signal swing.

4.3.3 Bit-Error Introduction

The random bit-error introduction is realized by feeding the binary data into a noisy binary symmetric channel. The channel randomly introduces bit errors according to the predefined channel error probability, which is an accurate approximation of the channel BER when the data set is large enough. We use six discrete BER levels from 1E-6 to 1E-1 for this simulation, one level per decade.

4.3.4 Error Detection and Correction

Different FEDC schemes can be applied to the binary data to improve its immunity to bit errors. Since the encoding should be done in the probe, a simple and low-power hardware implementation of the encoding scheme is crucial.

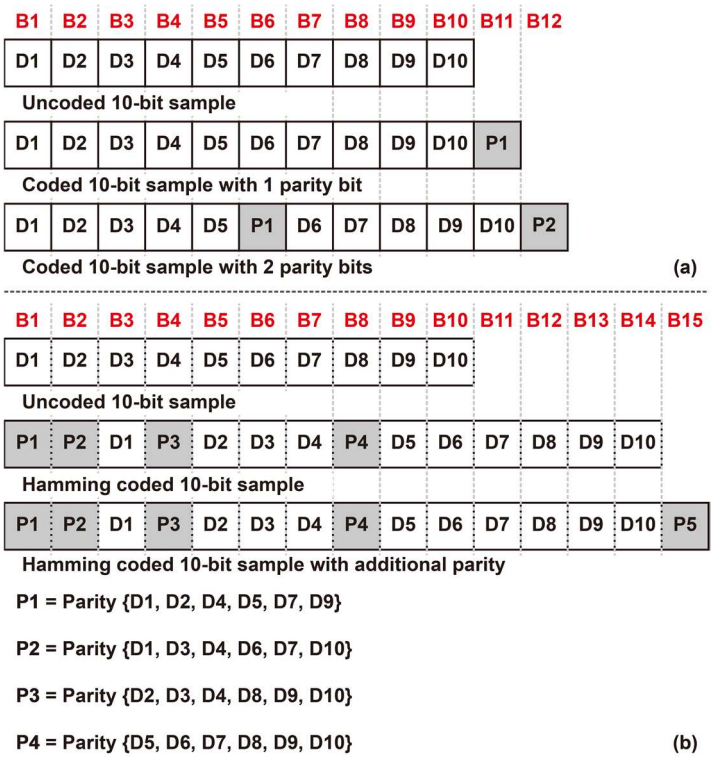


Figure 4. 5 Illustrations of the FEDC schemes: (a) parity checking; (b) Hamming coding

Moreover, stronger error detection/correction capability often requires more redundancy. Powerful encoding schemes improve the received BER at the cost of a reduction of the effective data rate per channel, unless a higher bit rate is adopted. A lower effective data rate implies that more cables will be needed, while a higher bit rate translates into higher power consumption to keep the same BER. The trade-off between error detection/ correction capability and redundancy needs to be carefully considered when choosing a suitable encoding scheme in the ultrasound probe design. The simulation should take this trade-off into account.

Two types of FEDC schemes, parity checking [27] and Hamming coding [28], have been used in the simulation. Parity checking can detect any odd number of bit errors in a string of binary data. It is the simplest error-detection code in terms of hardware implementation which adds only one redundant bit, but parity cannot detect an even number of bit errors and is not capable of correcting the detected errors. Hamming coding uses more than one parity bit in a string of binary data and arranges them in a way that error bits at different locations produce unique parity-check results. By adding more redundant bits to a string of binary data, Hamming coding enables not only the detection of bit errors but also the correction of single-bit errors [28].

Since the echo signals are digitized with 10-bit resolution, the FEDC encoding is also applied to every 10-bit binary sample. Fig. 4.5 shows the different encoding schemes that have been applied.

Parity coding extends a 10-bit sample (D10~D1) to 11 bits or 12 bits by adding an even parity bit in every 10 bits or 5 bits, as shown in Fig. 4.5(a). The effective transmission rate in the two cases is 90.9% and 83.3%, respectively.

Hamming coding extends a 10-bit binary sample to 14 bits by adding 4 redundant bits (P1 - P4) and P1 - P4 are the parity bits of the specific bits in the 10-bit binary sample (Fig. 4.5(b)).

Any single-bit error in the coded 14-bit data produces a unique combination of P1 - P4, thus allowing the decoder to identify the locations of the single-bit errors and to correct them [28]. However, the error detection and correction will fail if the coded data contains multi-bit errors. Since the evaluated BER range is from 1E-6 to 1E-1, there is still a large probability that multi-bit errors, especially dual-bit errors, appear in the coded 14-bit data. An additional parity bit (P5) is added to enable dual-bit error detection. P5 is the even parity bit of all the data bits (D10~D1) and parity bits (P4~P1). The combination of P5 and P1- P4 detects dual-bit errors and corrects single-bit errors. Then the effective transmission rate of the Hamming coding is 71.4% and 66.7%, in cases w/ and w/o the global parity bit.

The data with bit errors is firstly decoded before image reconstruction on a sample-by-sample basis if FEDC is enabled. Parity bits are separated from the data bits and sent to a parity checker. For coding with only a parity-check bit, samples which fail the parity check are discarded and replaced by 0. For Hamming coding, if a sample fails both the parity check of P1 – P4 and P5, the error in the sample is considered as a single-bit error and the error bit is flipped; if a sample only fails the parity check of P5, the error is considered as a single-bit error at P5 and the sample is considered as error-free; while if a sample only fails the parity check of P1 – P4, the error in the sample is considered as a dual-bit error and the sample is discarded. The error-corrected 10-bit data is converted to decimal format for image reconstruction.

4.3.5 Image Reconstruction

The image reconstruction uses simple delay-and-sum beamforming. The beamformed data B at the k^{th} time sample is calculated by:

$$\mathrm{B}(k) = \frac{N}{N - N_{err}} \times \sum_{i=1}^{N} S_i(k) \tag{1}$$

where N, N_{err} are the total number of samples and the number of error samples in one beamforming operation, respectively; and S_i is the delayed echo signal of the i^{th} element. Since, as mentioned, samples with detected errors have been replaced by zeros, this expression effectively represents a beamforming operation on the $(N - N_{err})$ correct samples. Envelopes extracted from the beamformed data are logarithmically compressed and then displayed on a 50 dB gray-scale image. The dynamic range of the envelopes is limited to 100 dB, with respect to the maximum value in the reference image, for the following IQM calculations.

4.3.6 Image Quality Analysis

Since a reference image can be constructed from the raw error-free element echo data, a full-reference IQA can be performed. Three full-reference IQM are adopted in the evaluation: peak-signal-to-noise ratio (PSNR), structural similarity (SSIM) and contrast-to-noise ratio (CNR).

PSNR is calculated as the ratio between the maximum pixel power in a reference image and the mean-squared error (MSE) of a distorted image, where MSE is defined as the averaged squared difference between the values of the pixels in the reference image and in a distorted image [29]. For reference image R and distorted image D consisting of m × n pixels, the equations of PSNR and MSE are given as:

$$PSNR = 10 \cdot \log_{10} \frac{[\max(R)]^2}{MSE} \tag{2}$$

and

$$\mathrm{MSE} = \frac{1}{m \cdot n} \sum_{i=1}^{m} \sum_{j=1}^{n} [R(i,j) - D(i,j)]^2 \tag{3}$$

PSNR is one of the most widely used IQM for full-reference IQA because it is simple to calculate, has clear physical meaning, and is mathematically convenient for image quality optimization [30]. However, in some cases, it shows low

correlation with the perceptual quality of the distorted images, especially for ultrasound images in which significant speckle noise exists [31].

In contrast to statistical metrics like MSE and PSNR, SSIM is based on the human visual perception. It has been used in several studies on the quality assessment on medical ultrasound videos and shows good correlation with the subjective score provided by medical experts [31]. The computation of the SSIM index is based on a multiplication of three terms: a luminance term, a contrast term and a structural term [30]. For a reference image R and a distorted image D, SSIM is calculated as:

$$SSIM = \frac{(2\mu_R \cdot \mu_D + C_1)(2\sigma_{RD} + C_2)}{(\mu_R^2 + \mu_D^2 + C_1)(\sigma_R^2 + \sigma_D^2 + C_2)} \tag{4}$$

where μ_R, μ_D, σ_R, σ_D, and σ_{RD} are the means, standard deviations, and cross-covariance of the two images, C_1 and C_2 are two constants $\ll 1$, to avoid instability for $\mu_R = \mu_D = 0$ and $\sigma_R = \sigma_D = 0$.

Another widely used IQM in medical ultrasound imaging is CNR [32]. It is used to quantify the detectability of a region of interest (ROI), normally a cyst, from its background, and is typically calculated by [33]:

$$CNR = \frac{|\mu_{ROI} - \mu_{bg}|}{\sqrt{\sigma_{ROI}^2 + \sigma_{bg}^2}} \tag{5}$$

where μ_{ROI}, μ_{bg}, σ_{ROI}, σ_{bg} are the means of the image pixel intensity inside the ROI and in the background, and the standard deviations of the image pixel intensity inside the ROI and in the background, respectively. The pixel intensity used in the CNR calculation is after logarithmic compression [34]. Since CNR quantifies the contrast between two regions in one image, the impact of BER is evaluated by the CNR degradation between the distorted image and the reference image.

Since the bit errors are randomly introduced to the binary data, bit errors occurring at the most-significant bit (MSB) and at the least-significant bit (LSB) of a sample will have a significantly different impact on the calculated PSNR, and SSIM values. Furthermore, the distortions due to bit errors will only influence the calculated CNR when they are appearing in a ROI in distorted images. To obtain representative values for the IQMs despite this varying impact of bit errors, we perform a 100-run Monte-Carlo simulation and obtain IQM estimates from

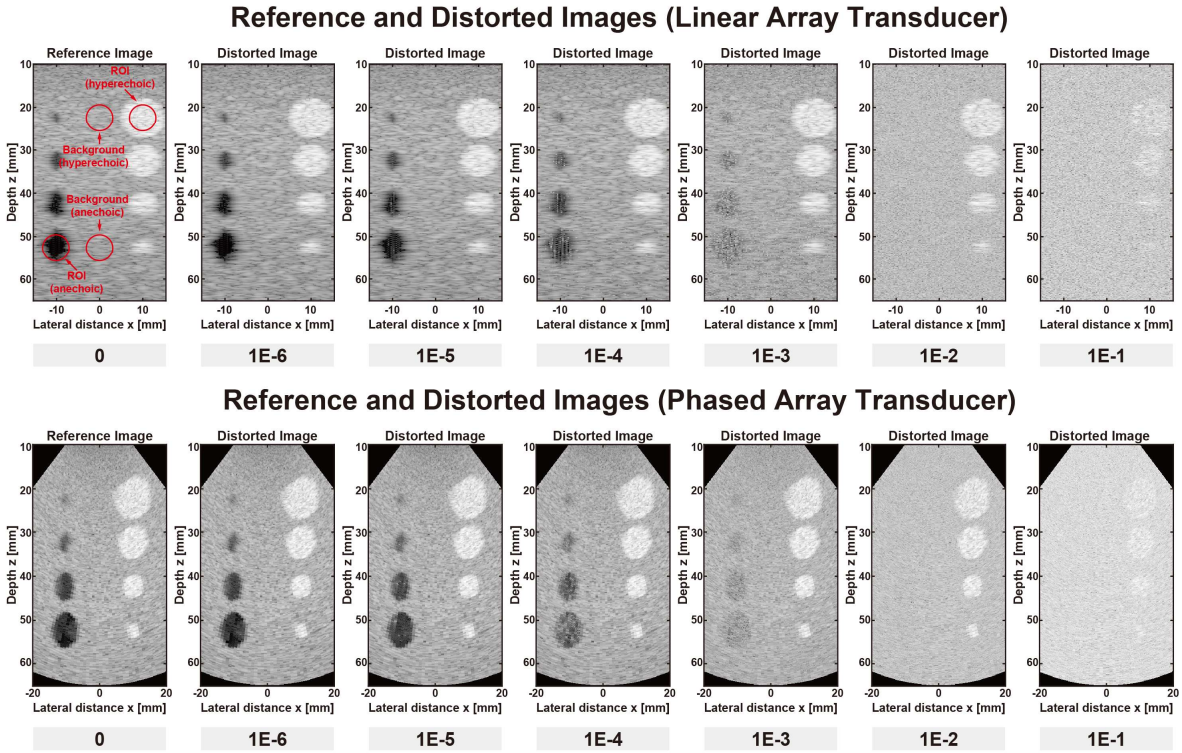


Figure 4. 6 Reference and distorted images for both linear array and phased array transducers at different BER levels (without error detection or correction)

the statistics of sets of distorted images produced. The reliability of the results is reflected by the confidence intervals of the IQM estimates.

4.4 Simulation Results

The reference image I_{ref} is directly reconstructed from the digitized raw element echo signals, without bit errors. A set of distorted images $I_{dst}\langle 1{:}\,6\rangle$ is reconstructed from the error data with BER levels from 1E-1 to 1E-6, when FEDC is off. Fig. 4.6 shows I_{ref} (left-most images) and $I_{dst}\langle 1{:}\,6\rangle$ for both linear array and phased array transducers.

For $I_{dst}\langle 1{:}\,6\rangle$ in both linear array and phased array imaging, when the BER is 1E-2 or higher, only the hyperechoic regions can still be distinguished, while the anechoic regions and the background are below the noise floor; when the BER level goes down to 1E-3 ~ 1E-5, both the hyperechoic and anechoic regions can be distinguished, but erroneous pixels are still easily visible in the anechoic regions; when the BER level is further reduced to 1E-6, the distorted image is almost the same as the reference image.

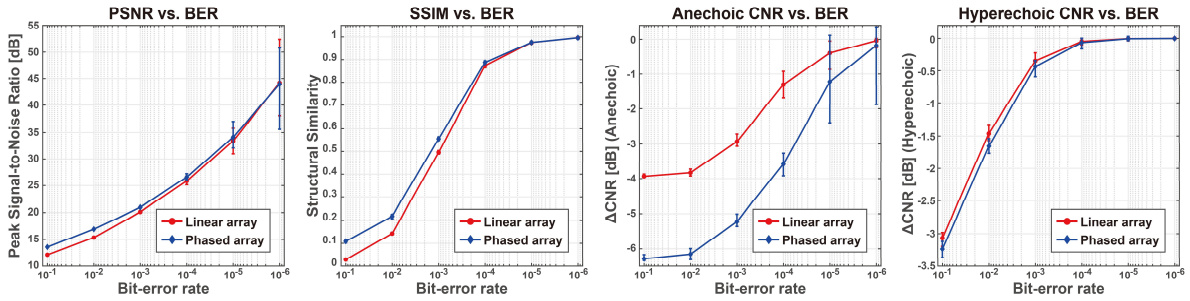


Figure 4. 7 IQM vs. BER plots for images from both linear array and phased array transducers (without error detection or correction)

The statistics of PSNR, SSIM and CNR degradation ($CNR_{dst} - CNR_{ref}$) between $I_{dst}\langle 1{:}\,6\rangle$ and I_{ref} are derived from a 100-run Monte-Carlo simulation. CNR degradations for both hyperechoic and anechoic regions are calculated. The ROI and background regions for CNR calculation are marked in Fig. 4.6. The calculated IQMs can be plotted using the mean values of the Monte-Carlo results. The PSNR can be very well represented by their mean values (μ) at high BER levels, since the high BER leads to a small relative standard deviation (σ / μ). However, when BER is lower (≤ 10E-5), the large relative standard deviation makes the mean values less representative for the expected image quality. Therefore, we display the IQMs in error-bar plots, where the upper and lower bounds are the maximum and minimum values in the 100 runs, allowing the IQMs at low BER levels to be estimated using the worst-case values in the plots.

Fig. 4.7 shows the error-bar plots of the 5 IQMs versus BER for both the linear array and phased array imaging. The trends of the IQM curves are in good agreement with the image quality observed in Fig. 4.6. For the unacceptable images (BER > 1E-2), we get PSNR < 20 dB and SSIM < 0.25 respectively. The CNR degradations in hyperechoic region and anechoic region are over -3.5 dB and -1.5 dB respectively. For images with no visible distortions (BER < 1E-6), we get PSNR > 40 dB and SSIM > 0.99, and the CNR degradations are very close to 0. In contrast with most telecommunication applications, which normally require BER levels better than 1E-12 ~1E-15 [35]–[37], the quality of the reconstructed ultrasound images remains high at BER < 1E-6.

When FEDC is on, 4 distorted images I_{dst_a}, I_{dst_b}, I_{dst_c} and I_{dst_d} are reconstructed from the data coded by: a) one parity bit; b) two parity bits; c) Hamming code and d) Hamming code with one additional parity bit. The distorted images together with the reference image from the phased array transducer at different BER levels are shown in Fig. 4.8.

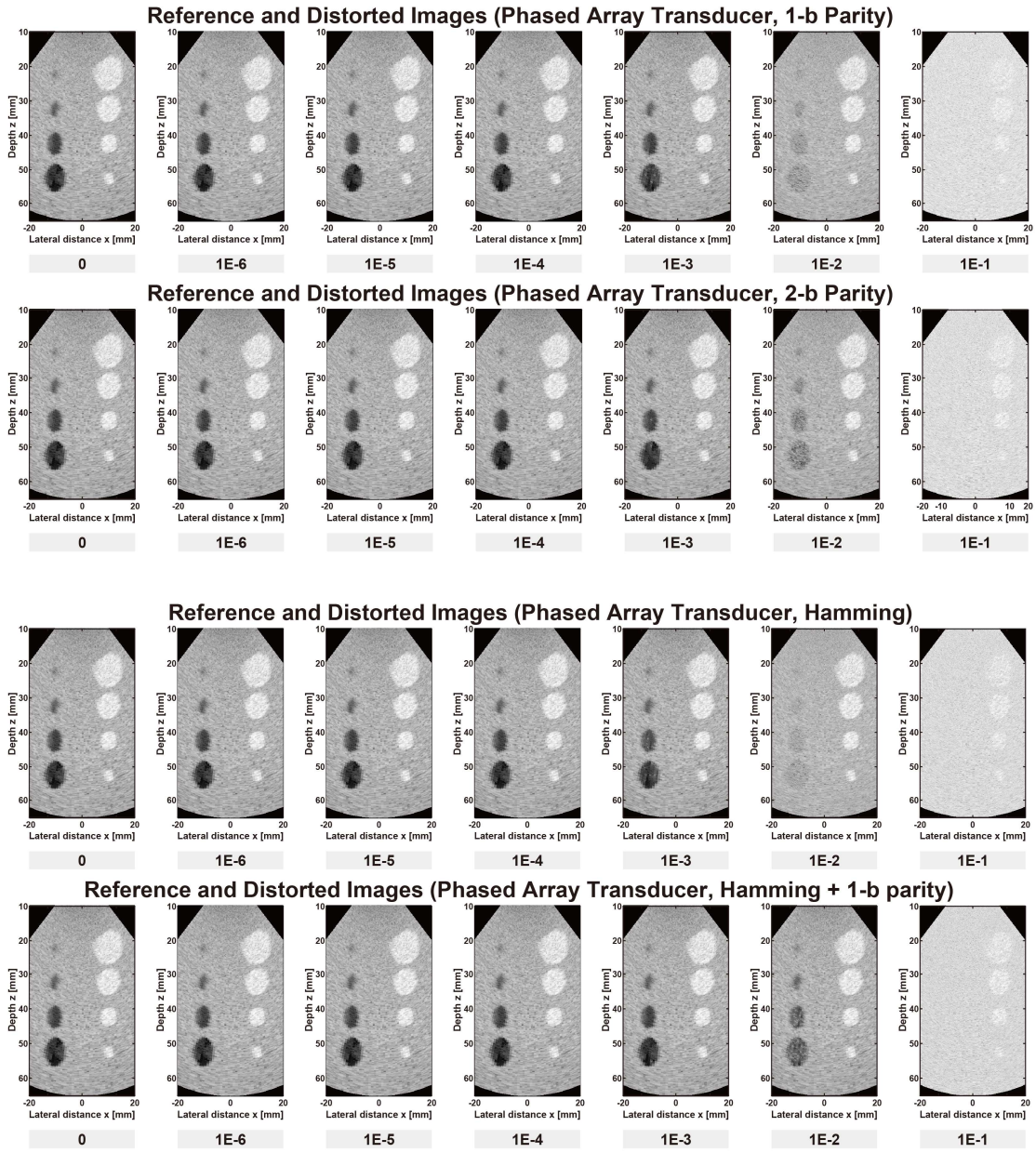


Figure 4. 8 Reference and distorted images for phased array transducers at different BER levels, with error detection using parity bits and error detection and correction using Hamming coding.

Visually the image quality of the 4 distorted images at BER = 1E-1 does not differ from the image quality of I_{dst} in Fig. 4.6. However, when BER reduces to 1E-2, all 4 images with FEDC show much more distinguishable anechoic regions from the background, compared with I_{dst}. I_{dst_d} shows the best image quality, though several defective pixels can still be observed in the anechoic regions. When the BER level is further reduced to 1E-3, hardly any difference can be seen between I_{dst_d} and the reference image, while I_{dst_a}, I_{dst_b} and I_{dst_c} show

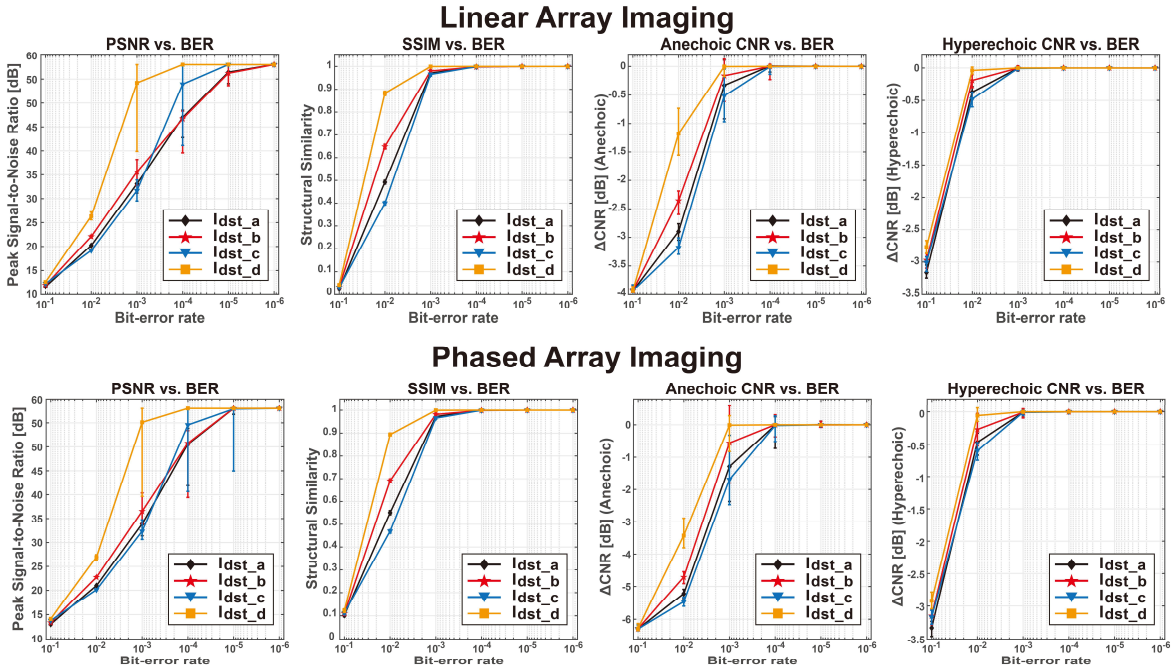


Figure 4. 9 IQM vs. BER plots for images from both linear array and phased array transducers (with error detection or correction)

similar image quality. All the images at BER level of 1E-4 or better are almost the same as the reference image.

Fig. 4.9 shows the error-bar plots of the IQMs of the 4 images with FEDC versus BER for both the linear array and phased array imaging. PSNR values higher than 58 dB are rounded to 58 dB, to be better displayed in the plots. I_{dst_d} outperforms all others in all the IQMs in both linear array and phased array images when BER is better than 1E-2. When BER is better than 1E-4, the PSNR values of all the 4 distorted images are > 45 and the SSIM and CNR degradations are also very close to their theoretical limits. This is also well aligned with the visual perception of the images in Fig. 4.8.

The effectiveness of the encoding is quantitatively evaluated by comparing the IQMs of the un-encoded data image I_{dst} and the 4 encoded data images in Fig. 4.7. and Fig. 4.9. At BER = 1E-1, there is no significant difference among the 5 distorted images. Encoding is not effective at very high BER levels. This can be expected because the data encoding is applied in every 10-bit sample. For example, BER = 1E-1 implies that majority of the samples contain bit errors and are discarded in the image reconstruction. The images are reconstructed from the remaining insufficient data samples. At BER = 1E-2, encoding significantly improves the three image quality metrics for all the 4 encoded data images, especially for I_{dst_d}. The PSNR and SSIM of I_{dst_d} using Hamming coding and

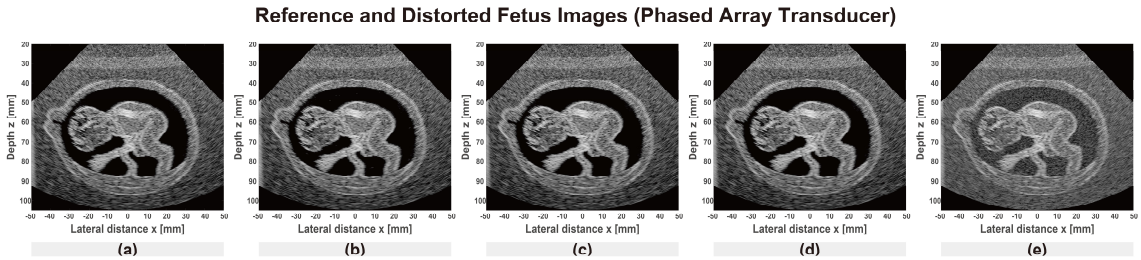


Figure 4. 10 (a) Reference fetus image; and four distorted images from data, (b) without error detection or correction, BER = 1E-6, (c) with 1-bit parity coding, BER = 1E-4, (d) with Hamming coding with additional parity bit, BER = 1E-3 and (e) without error detection

1-b parity are > 25 dB and > 0.88 respectively, which are already better than the metrics of I_{dst} obtained at BER = 1E-4. The degradation of CNR for hyperechoic regions is almost negligible. However, the degradation of CNR for anechoic regions in phased array imaging is over 3 dB. When BER ≤1E-4, we have PSNR > 45 dB, SSIM > 0.97, there is virtually no CNR degradation for all the 4 distorted images, while the BER level needs to be reduced to 1E-6 for I_{dst} to have similar results.

Though the encoding is not beneficial to the image quality when the BER is very high or very low, it effectively relaxes the BER requirement by roughly two orders of magnitude when the BER is between 1E-2 and 1E-5. For images reconstructed from data with Hamming coding, the image quality at BER = 1E-3 is still very high; even for images reconstructed from data with simple 1-bit parity coding, a comparable image quality can be obtained at BER = 1E-4.

To verify whether the conclusions can be applied to more complex images, we adopt an artificial phantom for a 3-month fetus [38] in the simulation. A reference image (a) and four distorted images from un-encoded data at BER = 1E-6 (b), 1-bit parity coded data at BER = 1E-4 (c), Hamming coded data with additional

Table II. IQM values of the four distorted fetus images in Figure 10

Distorted Images			IQM	
	Coding	BER	PSNR	SSIM
(b)	*No coding*	*1E-6*	*46.63*	*0.9978*
(c)	*1-b Parity coding*	*1E-4*	*54.08*	*0.9996*
(d)	*Hamming coding + 1-b parity*	*1E-3*	*47.74*	*0.9987*
(e)	*No coding*	*1E-3*	*17.61*	*0.5987*

parity bit at BER = 1E-3 (d) and un-encoded data at BER = 1E-3 (e) are shown in Fig. 4.10. The imaging artefacts due to the high BER can be clearly observed in (e), while when reducing the BER to 1E-6, the distorted image (b) is almost identical to the reference image (a). Similar image quality can also be obtained by proper data coding, even when the BER remains high. The image quality metrics of the distorted images are shown in Table II. The PSNR and SSIM of images (b), (c) and (d) are over 45 dB and 0.995, respectively, a lot better than the 17.61 dB and 0.6 of image (e), which indicates that the distorted images from coded data are indeed very close to the reference image despite the high BER levels.

4.5 Discussion and Conclusion

We have built a simulation model to quantitatively evaluate the quality of B-mode ultrasound images reconstructed from digitized element-level RF echo signals with different BER levels. According to the simulation results shown in section IV, ultrasound images show inherent resilience to BER levels which are typically unacceptable in many standard data communication protocols, such as 1000BASE-X. The image quality, which is quantified by PSNR, SSIM and CNR, shows unnoticeable degradation for BER levels lower than 1E-6. Unlike other applications which can also be immune to high BER but require complex encoding algorithms [16], simple coding schemes with low hardware cost prove to be very efficient for ultrasound imaging in further improving the immunity to bit errors. Simple 1-bit parity coding with 9% added redundancy helps to retain similar image quality for BER up to 1E-4, and Hamming coding with 33.3% added redundancy allows the BER to increase to 1E-3.

The inherent resilience to bit errors is due to the averaging effect in beamforming. At high BER levels, where the bit errors can be modelled as a Gaussian-distributed noise superimposed to the raw element data, the beamforming operation effectively reduces the noise power by a factor of N, where N is the number of elements involved in the beamforming, thus reducing the impact of a bit error on the final image. At high BER levels, phased array imaging is more resilient to bit errors compared to a linear array transducer with the same number of elements, since the receive beamforming in a phased array system involves the echo signals of all the elements in the array, not a subset of the elements, thus resulting in a larger N. However, if the aperture in a linear

array imaging is expanded to the point where all elements are involved, a similar image quality is expected from both linear array and phased array imaging.

The resilience to bit errors can be further enhanced by compounding multiple consecutive B-mode images in the time domain, which is commonly used to improve the ultrasound image quality. Similar to the spatial beamforming in a single frame, the inherent averaging effect in a compounding operation can also be effective on suppressing the image artefacts due to bit errors. By enabling averaging in both the spatial and time domains, real-time ultrasound images are likely to tolerate higher BER than static B-mode images, which are already proven to be quite immune to bit errors.

The conclusion of this work can serve as a guideline in the datalink design of ultrasound probes with in-probe receive digitization. The simulation results reveal that a non-standard datalink design with relatively poor BER performance (>1E-6) can be quite acceptable for ultrasound imaging applications. This allows the datalink to operate at a higher data rate per cable, thus reducing the number of cables required, or to operate at the same data rate per cable, while reducing the overall power consumption.

References

[1] C. Chen et al., “A Prototype PZT Matrix Transducer With Low-Power Integrated Receive ASIC for 3-D Transesophageal Echocardiography,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control,* vol. 52, no. 4, pp. 994–1006, 2016.

[2] J. Janjic et al., “A 2-D Ultrasound Transducer With Front-End ASIC and Low Cable Count for 3-D Forward-Looking Intravascular Imaging: Performance and Characterization,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control,* vol. 65, no. 10, pp. 1832–1844, 2018.

[3] I. O. Wygant et al., “An integrated circuit with transmit beamforming flip-chip bonded to a 2-D CMUT array for 3-D ultrasound imaging,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control,* vol. 56, no. 10, pp. 2145–2156, 2009.

[4] I. Cicek, A. Bozkurt, and M. Karaman, “Design of a front-end integrated

circuit for 3D acoustic imaging using 2D CMUT arrays," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control,* vol. 52, no. 12, pp. 2235–2241, 2005.

[5] E. Kang et al., "A Reconfigurable Ultrasound Transceiver ASIC With 24×40 Elements for 3-D Carotid Artery Imaging," *IEEE J. Solid-State Circuits,* vol. 53, no. 7, pp. 2065–2075, 2018.

[6] Y. Katsube et al., "Single-chip 3072ch 2D array IC with RX analogue and all-digital TX beamformer for 3D ultrasound imaging," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.,* vol. 60, pp. 458–459, 2017.

[7] B. Savord and R. Solomon, "Fully sampled matrix transducer for real time 3D ultrasonic imaging," in *IEEE Symposium on Ultrasonics,* 2003, pp. 945–953.

[8] C. Chen et al., "A pitch-matched front-end ASIC with integrated subarray beamforming ADC for miniature 3-d ultrasound probes," *IEEE J. Solid-State Circuits,* vol. 53, no. 11, pp. 3050–3064, 2018.

[9] T. M. Carpenter, M. W. Rashid, M. Ghovanloo, D. M. J. Cowell, S. Freear, and F. L. Degertekin, "Direct digital demultiplexing of analog TDM signals for cable reduction in ultrasound imaging catheters," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control,* vol. 63, no. 8, pp. 1078–1085, 2016.

[10] M. W. Rashid, C. Tekes, M. Ghovanloo, and F. L. Degertekin, "Design of frequency-division multiplexing front-end receiver electronics for CMUT-on-CMOS based intracardiac echocardiography," *IEEE Int. Ultrason. Symp.,* vol. 1, pp. 1540–1543, 2014.

[11] M. C. Chen et al., "A pixel pitch-matched ultrasound receiver for 3-d photoacoustic imaging with integrated delta-sigma beamformer in 28-nm UTBB FD-SOI," *IEEE J. Solid-State Circuits,* vol. 52, no. 11, pp. 2843–2856, 2017.

[12] J. Lee et al., "A 5.37mW/Channel Pitch-Matched Ultrasound ASIC with Dynamic-Bit-Shared SAR ADC and 13.2V Charge-Recycling TX in Standard CMOS for Intracardiac Echocardiography," *IEEE Int. Solid-State Circuits Conf.,* vol. 10, no. 4, pp. 2018–2020, 2019.

[13] IEEE, "IEEE Standard for Information technology— Telecommunications and information exchange between systems— Local and metropolitan area networks— Specific requirements Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and p," The Institute of Electrical and Electronics Engineers, Inc., New York, NY, 2002.

[14] C. Bulach, U. Bihr, and M. Ortmanns, "Evaluating the influence of the bit error rate on the information of neural spike signals," 2012 *19th IEEE Int. Conf. Electron. Circuits, Syst.,* pp. 21–24, 2012.

[15] E. Cavero, A. Alesanco, and J. García, "Enhanced protocol for real-time transmission of echocardiograms over wireless channels," *IEEE Trans. Biomed. Eng.,* vol. 59, no. 11, pp. 3212–3220, 2012.

[16] S. Pudlewski and T. Melodia, "On the performance of compressive video streaming for wireless multimedia sensor networks," *IEEE Int. Conf. Commun.,* 2010.

[17] J. Wang et al., "Capsule Ultrasound Device: Characterization and Testing Results," in *IEEE International Ultrasonics Symposium (IUS),* 2017, pp. 1–4.

[18] M. Tan et al., "A front-end ASIC with high-voltage transmit switching and receive digitization for 3-D forward-looking intravascular ultrasound imaging," *IEEE J. Solid-State Circuits,* vol. 53, no. 8, pp. 2284–2297, 2018.

[19] U. Madhow, Fundamentals of digital communication. Cambridge University Press, 2008.

[20] B. Analui, "Signal integrity issues in high-speed wireline links: analysis and integrated system solutions," California Institute of Technology, Pasadena, California, 2005.

[21] B. Sklar, DIGITAL COMMUNICATIONS Fundamentals and Applications, 2nd ed. Pearson Education, 2016.

[22] B. Razavi, "Double Decision Feedback Equalizer," *IEEE Soild-State Circuits Mag.,* vol. 9, no. 4, pp. 13–132, 2017.

[23] S. M. J. Alam, M. R. Alam, G. Hu, and M. Z. Mehrab, "Bit Error Rate Optimization in Fiber Optic Communications," *Int. J. Mach. Learn. Comput.,* vol. 1, no. 5, pp. 435–440, 2011.

[24] Aurangozeb, M. Mohammad, and M. Hossain, "Analog to Sequence Converter-Based PAM-4 Receiver with Built-In Error Correction," *IEEE J. Solid-State Circuits,* vol. 53, no. 10, pp. 2864–2877, 2018.

[25] J. A. Jensen and N. B. Svendsen, "Calculation of Pressure Fields from Arbitrarily Shaped, Apodized, and Excited Ultrasound Transducers," *IEEE Trans. Ultrason. ferroelectronics Freq. Control,* vol. 39, no. 2, pp. 262–267, 1992.

[26] J. A. Jensen, "Field: A Program for Simulating Ultrasound Systems," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control,* vol. 34, pp. 351–353, 1996.

[27] R. E. Ziemer and W. H. Tranter, Principles of Communication Systems, Modulation, and Noise. 2014.

[28] R.W.Hamming, "Error Detecting and Error Correcting Codes," *Bell Syst.*

Tech. J., vol. 196, no. 4, pp. 147–160, 1950.

[29] R. Dosselmann and D. Y. Xue, "Existing and emerging image quality metrics," in *Canadian Conference on Electrical and Computer Engineering,* 2005, pp. 1906–1913.

[30] Z. Wang, A. C. Bovik, H. R. Sheikh, and E. P. Simoncelli, "Image quality assessment: From error visibility to structural similarity," *IEEE Trans. Image Process.,* vol. 13, no. 4, pp. 600–612, 2004.

[31] M. Razaak, M. G. Martini, and K. Savino, "A Study on Quality Assessment for Medical Ultrasound Video Compressed via HEVC," *IEEE J. Biomed. Heal. Informatics,* vol. 18, no. 5, pp. 1552–1559, 2014.

[32] A. Rodriguez-Molares, O. M. Hoel Rindal, J. D'hooge, S.-E. Masoy, A. Austeng, and H. Torp, "The Generalized Contrast-to-Noise Ratio," in 2018 *IEEE International Ultrasonics Symposium,* 2018.

[33] M. S. Patterson and F. S. Foster, "The Improvement and Quantitative Assessment of B-Mode Image Produced by An Annular Array/Cone Hybrid," *Ultrasound Imaging,* vol. 5, no. 3, pp. 195–213, 1983.

[34] M. O. Sumati Krishnan, Kenneth Wayne Rigby, "Improved estimation of phase aberration profile," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control,* vol. 44, no. 3, pp. 701–713, 1997.

[35] J. Poulton et al., "A 14-mW 6 . 25-Gb / s Transceiver in 90-nm CMOS," *IEEE J. Solid-State Circuits,* vol. 42, no. 12, pp. 2745–2757, 2007.

[36] H. Won et al., "A 0.87 W transceiver IC for 100 gigabit ethernet in 40 nm CMOS," *IEEE J. Solid-State Circuits,* vol. 50, no. 2, pp. 399–413, 2015.

[37] B. Garlepp et al., "A 1-10Gbps PAM2, PAM4, PAM2 partial response receiver analog front end with dynamic sampler swapping capability for backplane serial communications," in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers,* 2005, pp. 376–379

[38] Calculation of B-mode image of synthetic fetus: [online] Available: https://field-ii.dk/?examples/fetus_ example/fetus_ example.html [30-Apr-2012]

CHAPTER 5

A POWER-EFFICIENT TRANSMIT BEAMFORMER ASIC FOR MINIATURE ULTRASOUND PROBES

*Based on **Z. Chen**, E. Noothout, Z.-Y. Chang, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong and M. Pertijs, "A Power-Efficient Transmit Beamformer ASIC for Minimally Invasive Ultrasound Probes", in preparation for submission.*

5.1 Introduction

Medical ultrasound imaging is a widely used diagnostic tool, thanks to its excellent safety record, capability of producing real-time images, and low cost [1]. Besides the well-known diagnostic use of ultrasound, high-intensity focused ultrasound (HIFU) is an emerging therapeutic modality in the treatment of diseases like prostate cancer [2] and neurological disorders [3]. HIFU employs high acoustic intensity to generate heat in tissue, which rapidly raises the local temperature and destroys the tissue through thermal ablation [4]. Although one advantage of ultrasound in clinical practice is its non-invasive character, there are more and more clinical needs to utilize ultrasound in minimally-invasive manner. Minimally-invasive ultrasound imaging methodologies, such as intravascular ultrasound (IVUS) imaging, reduce the acoustic attenuation by putting ultrasound probes close to the target, thus enabling the usage of higher ultrasound frequencies to improve the spatiotemporal resolution of the images [5]. Similarly, minimally-invasive HIFU probes allow the generation of more acoustic pressure at the focal point and minimize the surrounding tissue damage [6].

For non-invasive ultrasound probes, all transducer elements are individually connected to an imaging system using cables, while for catheter-based or endoscopic ultrasound probes which are used in a minimally-invasive manner,

minimizing cable count is critical due to their size limitation. This can be realized by integrating an application-specific integrated circuit (ASIC) with the transducer in the probe head [7]–[11]. In transmit (TX), the ASIC locally generates the high-voltage (HV) signals to drive each individual transducer element, and for imaging applications where the echoes also need to be received, the ASIC is also capable of conditioning and processing the echoes, thus decoupling the element count and cable count.

Although an ASIC allows a probe to use fewer cables, it also brings unwanted power dissipation into the human body, which contributes to the overall self-heating of the probe. Recent ultrasound imaging probe designs have focused on minimizing the ASIC power dissipation in receive (RX) [7]–[10], while the power dissipation of the TX circuitry has received relatively little attention. A power-efficient TX ASIC allows an imaging probe to transmit more acoustic power under the same self-heating regulation, which leads to deeper imaging depth and higher signal-to-noise ratio (SNR), thus improving the image quality. The impact of the TX power efficiency becomes more dramatic in HIFU since the transmitters are often required to operate quasi-continuously to generate the high acoustic intensity [6], [12].

In typical medical ultrasound imaging or HIFU applications, ultrasound transducers are excited by electrical signals with amplitudes up to several tens or even hundreds of Volts. An ultrasound transmitter can be implemented by a HV linear amplifier [13]–[15], but most commonly a HV pulser is used [16]–[19], for its better power efficiency. The electrical energy delivered by a pulser to the transducer is partially converted to acoustic energy but is also partially wasted in self-heating and charging/ discharging of the transducer's parasitic capacitance. As a result, the power efficiency of a pulser degrades dramatically when driving a transducer with large parasitic capacitance, which may either be associated with the transducer-ASIC interconnect or with the physical structure of the transducer itself, for example in piezoelectric micromachined ultrasonic transducers (pMUTs) [20]. A shunt inductor in parallel with the transducer helps to cancel out the large parasitic capacitance, but at the cost of narrower transducer bandwidth and more system integration complexity [21]. The three-level pulser proposed in [22] recycles half of the charge on the capacitor by utilizing a mid-level supply. A drawback of this approach is that the mid-level supply is generated by an on-chip DC-DC converter and an off-chip capacitor, which comes with an increase in size that is undesired for minimally-invasive devices.

The transmitter in [23] is implemented by an array of HV switches which connect an array of transducer elements to a HV pulse train that is generated by a pulser in the system, pulsing at the resonant frequency of the transducer elements. An element is pulled up and down by connecting it to the HV pulse train via its associated HV switch. Although the same amount of power is wasted in charging/ discharging the parasitic capacitance of the transducer element, by proper dimensioning of the HV switches, only a small fraction of this power is dissipated in the HV switches, thus minimizing the in-probe power dissipation. However, since the timing of the pulse is defined by the system-side pulser, this architecture is not capable of providing in-probe beamforming.

In this chapter we propose a power-efficient HV transmitter suitable for interfacing transducers with large capacitive loading. The transmitter is capable of providing sufficient TX beamforming functionality with only three HV connections to the system. The design does not require any off-chip components, thus relaxing the system integration complexity. Given the large size of the HV MOS devices in a HV process, the proposed HV transmitter is not targeted to be fit within an area of an element of a matrix transducer, such as that shown in Chapter 2. Instead, it is more suitable for direct integration with the elements of a 1-D transducer array. However, the split-array transducer configuration presented in Chapter 2 could allow one or two HV transmitter ASICs to be connected to the small central 8 × 8 TX array in the probe head, next to a low-voltage (LV) RX beamformer ASIC on top of which the matrix transducer is fabricated. Such a chip-set can realize full TX and RX capability locally in the probe with effective cable count reduction, thus making this transmitter design also valuable for 3-D imaging. Similarly, the transmitter ASIC can be combined with the RX ASIC presented in Chapter 3 to provide TX capability with only three HV connections.

This chapter is organized as follows. Section 5.2 describes the proposed transmitter architecture. Section 5.3 discusses the details of the circuit implementation. The experimental results are presented in Section 5.4. Conclusions are given in Section 5.5.

5.2 Proposed Transmitter Architecture

5.2.1 Transmitter Power Consumption

Most HV pulsers level-shift a LV pulse signal to HV using a HV push-pull stage (Fig. 5.1(a)). The power consumption of such a pulser when driving the capacitive part of a transducer at frequency f is:

$$P_{pulser} = f \cdot CV^2 \tag{1}$$

where C is the loading capacitance and V is the pulse amplitude. So ideally if the center frequency, the loading capacitance and the pulse amplitude are determined, when the loading capacitance dominates the impedance of a transducer element, the power consumption of the pulser to drive such transducer element is almost constant. It is dissipated on the resistive part of the pull-up and pull-down devices. However, the pull-up and pull-down devices in a pulser are typically quite large to guarantee a short transition time of the output signal. HV MOS transistors such as double-diffused MOS (DMOS) devices normally have substantial parasitic capacitance to the substrate due to the large isolation structure. The actual power dissipation of the pulser is increased to:

$$P'_{pulser} = \left(1 + \frac{C_{par}}{C}\right) \cdot P_{pulser} \tag{2}$$

where C_{par} is the total parasitic capacitance introduced by pulser itself.

A transmitter using a HV switch, as in [8], [9], [23], is shown in Fig. 5.1(b). Here, a selected transducer element is connected to a system-side pulser using an on-chip HV switch. As in the conventional pulser, the combined dissipation of the system-side pulser and the on-chip switch equals $f \cdot CV^2$ when driving the

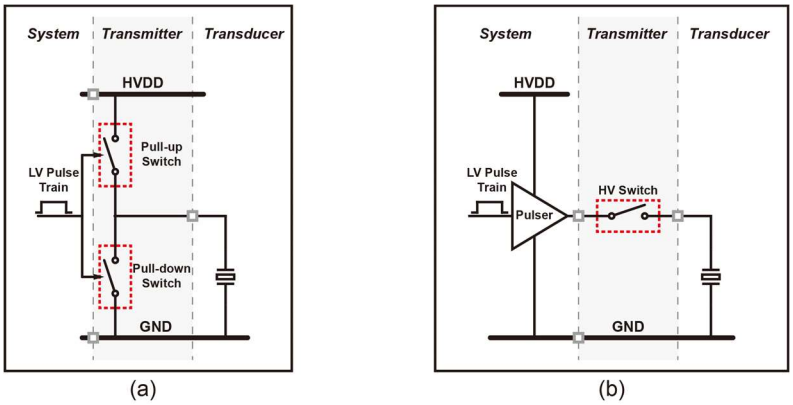


Figure 5. 1 HV transmitters implemented with: (a) HV pulser and (b) HV switch

same capacitive load. Since the HV switch is connected in series with the pull-up and pull-down devices in the pulser, this power is dissipated partially in the pulser and partially in the switch. If the switch is dimensioned such that its on-resistance (R_S) is much smaller than the on-resistance of the pull-up and pull-down devices (R_U and R_D), the in-probe power dissipation is only a small fraction of $f \cdot CV^2$:

$$P_{SW} = \frac{1}{2} \cdot f \cdot CV^2 \cdot \left(\frac{R_S}{R_S + R_U} + \frac{R_S}{R_S + R_D} \right) \quad (3)$$

A large switch dimension introduces more parasitic capacitance to the load, but it also effectively reduces R_S. Since the extra power dissipation due to the parasitic capacitance of the HV devices is less sensitive to dimensions of the devices, the on-chip power dissipation can be minimized by implementing a large on-chip HV switch.

5.2.2 TX Beamforming

Besides generating HV TX signals, beamforming functionality should also be realized in the transmitter design, to allow the transmitted acoustic beam to be steered/ focused spatially. As shown in Fig. 5.2(a), the TX beamformer delays the HV TX signals to precisely compensate for the travel-time differences among the elements in the transducer array and drives the HV pulsers. Note that in a typical imaging sequence, the transmit beam scans the volume of interest in successive pulse-echo cycles, implying that the time delays are not fixed, but change from cycle to cycle [24].

In practice, time delays are typically derived from a high-frequency clock, resulting in time quantization of the delays. This finite time-delay resolution introduces errors in the beamforming operation, which may result in reduced image quality [25]. One way of mitigating this problem is to increase the operating frequency of the TX beamformer. However, this solution comes at the cost of higher dynamic power consumption and a larger chip area. Therefore, it is important to know the minimum time-delay resolution required.

A recent study on focused-beam transmission using a 96-element 2.5 MHz linear array transducer [26] shows that a TX beamformer with a time-delay resolution equal to ¼ of the transducer's resonant period can provide almost indistinguishable images compared to an ideal TX beamformer with continuous time delays. For a 5 MHz transducer, which is targeted in this work, this translates

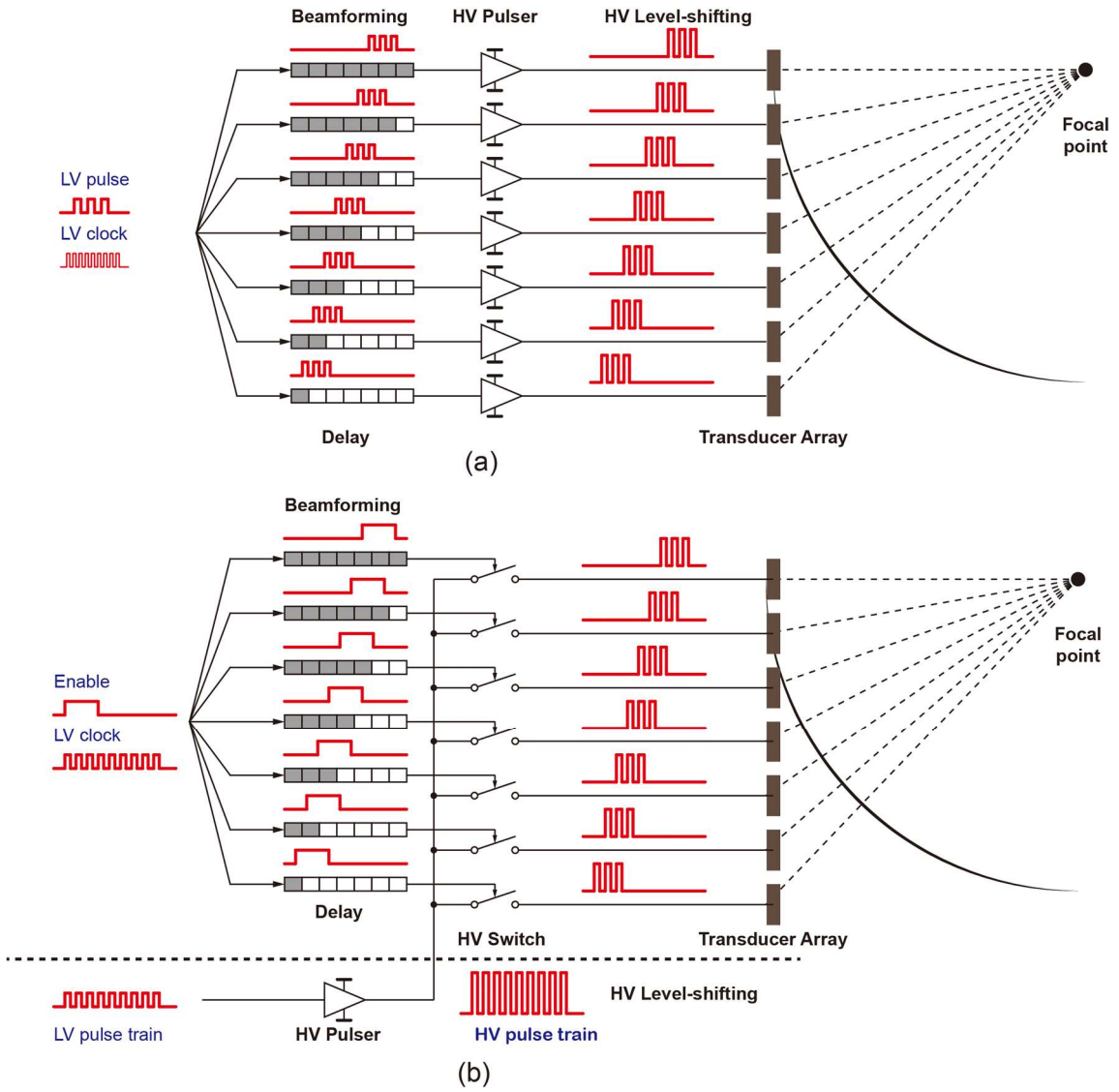


Figure 5. 2 Illustrations of HV TX beamforming for transmitters with (a) HV pulser and (b) HV switch

into a delay resolution of 50 ns. This relatively relaxed requirement enables some potentially power-efficient transmitter architectures.

For a TX beamformer using on-chip HV pulsers, the time-delay resolution is determined by the period of the beamformer clock, which can easily operate at several hundreds of MHz, even in the 180 nm HV CMOS process used in this work, generating a time-delay resolution of several nanoseconds, more than adequate for the 50 ns requirement of a 5 MHz transducer. However, this solution comes with the power dissipation associated with on-chip pulsers.

A more power-efficient TX beamformer can be constructed using on-chip HV switches, by generating a continuous HV pulse train at the transducer's resonant frequency using a system-side pulser, and connecting this to the elements of the

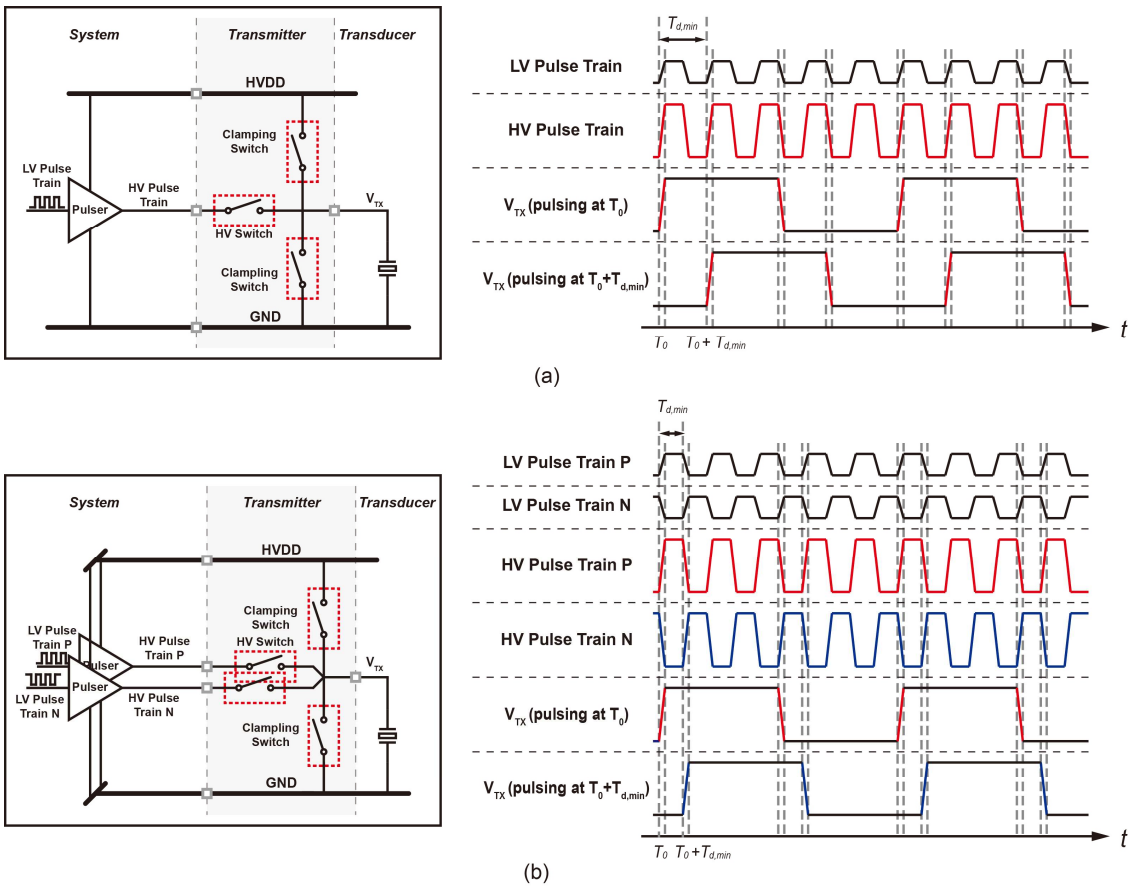


Figure 5. 3 Proposed transmitter architecture and its operation timing diagram with (a) one HV switch and one HV pulse train input and (b) two HV switches and two complementary HV pulse train inputs

transducer array via on-chip HV switches at the moment that an element should be pulsed, as shown in Fig. 5.2(b). However, the delay resolution that can thus be obtained equals the transducer's resonance period, which is far too coarse [26].

One way of realizing a higher time-delay resolution in a TX beamformer using on-chip HV switches is to employ multiple phase-shifted HV pulse trains and to connect each transducer element to the pulse train that provides a pulse closest to the moment that element should ideally be pulsed. While the use of *N* phases improves the delay resolution by a factor *N*, it also implies that each element should be equipped with *N* HV switches, significantly increasing the die size. Moreover, extra HV cable connections to the ultrasound system are required.

5.2.3 Proposed transmitter

The proposed transmitter architecture is shown in Fig. 5.3(a). Similar to the transmitter in Fig. 5.1(b), the proposed transmitter requires a HV pulse train

generated by a system-side pulser. In order to provide adequate time-delay resolution without additional HV pulse train inputs, the frequency of the HV pulse train is chosen to be 5 × the transducer's resonant frequency. To preserve the advantage of the lower power dissipation in the HV switch implementation, the transducer element should be pulled up and down by connecting it to the system-side pulser via the HV switch. To generate TX signals (V_{TX}) at the transducer's resonant frequency, the element should be clamped to the HV supply of the system-side pulser and clamped to ground after it has been pulled up and down, respectively. Since the pull-up and pull-down switches responsible for this clamping together are similar to a conventional pulser, the proposed transmitter can be seen as a combination of a HV switch and a pulser. It combines the power-efficiency advantage of a HV switch with the higher time-delay resolution of a pulser.

The time-delay resolution ($T_{d,min}$) of the proposed transmitter architecture is determined by the maximum frequency of the input HV pulse train, which is limited by the cable capacitance. In order to further improve the resolution by 2 ×, the final proposed transmitter (Fig. 5.3(b)) uses two complementary HV pulse trains with an additional switch path. The complete transmitter design requires 3 HV external cable connections while achieving a time-delay resolution equals to 1/10 of the transducer's resonant period.

To prove the concept of the proposed transmitter architecture, we present a 32-channel TX ASIC that pulses with up to 30 V peak-to-peak amplitude at 5 MHz. The proposed TX ASIC is capable of providing beamforming functionality with a time-delay resolution of 20 ns, while only using 3 HV cable connections to an ultrasound system: a 30 V HV supply and two complementary 30 V pulse trains pulsing at 25 MHz.

5.3 Circuit Implementation

5.3.1 Clock Extraction Circuit

Since the power-efficiency of the proposed transmitter is improved by pulling-up and pulling-down the transducer elements by external pulsers, not by the on-chip HV supply and ground, the LV clock and its associated switch-control signals should be accurately aligned with the HV pulse trains, especially when the HV pulse trains have slow rising/ falling edges, due to the large cable

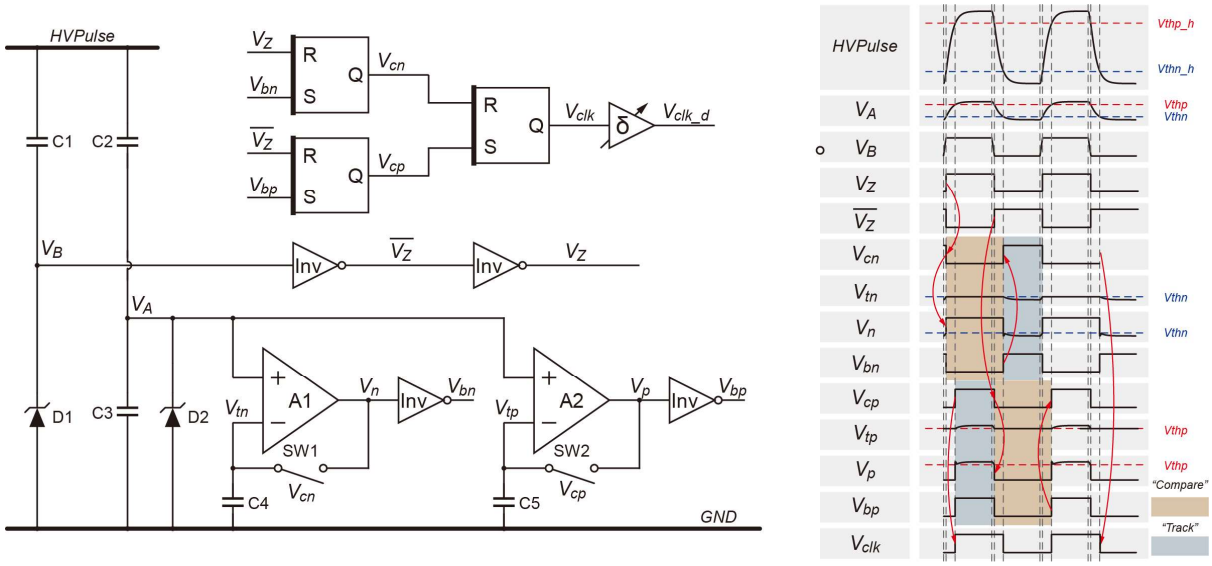


Figure 5. 4 Clock extraction circuit and its timing diagram

capacitance. One way of creating a synchronous LV clock is to extract it from the HV pulse train by an on-chip voltage divider. The rising edges of this clock coincide with the moment that the HV pulse train has almost reached its high level, and the falling edges with the moment that it has almost returned to ground. The threshold voltages V_{thp} and V_{thn} for the rising edge and falling edge are also desired to be extracted from the HV pulse train, so that they can be automatically adapted to any change on the amplitude of the HV pulse train.

The proposed circuit to extract the LV clock and its associated timing diagram are shown in Fig. 5.4. Two HV metal-oxide-metal (MOM) capacitors C2 and C3 form a capacitive voltage divider, the capacitive ratio of which is set such that the swing of the output signal V_A is 5 V. In order to generate the edges of the synchronous LV clock V_{clk}, two amplifiers A1 and A2 serve as voltage buffers in the "Track" phase to generate proper threshold voltages V_{thp} and V_{thn}, and as comparators in the "Compare" phase to toggle the LV clock according to the acquired threshold voltages held on capacitors C4 and C5.

As HVPulse starts to rise, V_{cn} is high, turning on the switch transistor SW1; A1 is in the "Track" phase. V_A is tracked by both V_n and V_{tn}. When the voltage of HVPulse exceeds 5 V, V_B becomes high and resets V_{cn} by an RS latch, thus turning off SW1. The threshold voltage V_{thn} is then sampled and held on C4. A1 is now in the open-loop "Compare" phase, making V_n high until V_A drops below V_{thn}, which corresponds to the moment at which HVPulse drops below an equivalent high-voltage threshold V_{thn_h} at its falling edge. This sets the SR latch that generates V_{cn}, turning the working mode of A1 to "Track" again, and resets

another SR latch that generates V_{clk}, thus defining the falling edge of the LV clock.

Similarly, the threshold voltage V_{thp} is tracked and held by A2 and C5 respectively, and the falling edge of V_{bp} is obtained at which HVPulse exceeds an equivalent high-voltage threshold V_{thp_h} during its rising edge. This sets the SR latch that generates V_{clk}, thus defining the rising edge of the LV clock.

V_{clk} is fine-tuned by an adjustable delay element before applying it to the beamformer logic control circuits. Two identical extraction circuits are implemented on-chip to extract two complementary LV clocks from the two complementary HV pulse trains.

5.3.2 HV Pulse Train Switch

Fig. 5.5(a) shows the schematic of the HV pulse train switch, which connects HVPulse to the transducer output V_{TX}. In order to ensure the HV pulse train is fully disconnected from the transducer when it is clamped to either HV supply or ground, a switch consisting of two serially connected n-type HV laterally-diffused MOS (LDMOS) transistors (Mb1 and Mb2) with joint-source connection is used. The back-to-back connection contributes to an overall ON-resistance of 94 Ω and guarantees that the parasitic body diodes of the transistors will not be turned on simultaneously.

Since the gate-source voltage of the LDMOS transistors cannot exceed 5 V, the gate voltages of Mb1 and Mb2 (V_{GH1} and V_{GH2}) are generated by level-shifting the low-side 5 V control signals to a floating supply domain between the source voltage FVSS and a floating supply FVDD equals to FVSS + 5 V. FVDD is generated by a bootstrap circuit similar to that presented in [23]. It consists of two LDMOS transistors Mb3 and Mb4, a diode D2, two bootstrap capacitor C1 and C2, and a protection Zener diode D1. When the HV pulse train is disconnected from the transducer, the bottom plate of C1 is shorted to ground via M4, and M3 is turned on through D2 and C2, thus pre-charging C1 to 5 V. When M3 and M4 are off, C1 is acting as a floating battery to provide charge to properly turn on Mb1 and Mb2. To minimize the voltage drop across C1 when it delivers charge to the level-shifters and the gates of Mb1 and Mb2, C1 should be sufficiently large. In this work, it is implemented by a 34 pF metal-insulator-metal (MIM) capacitor.

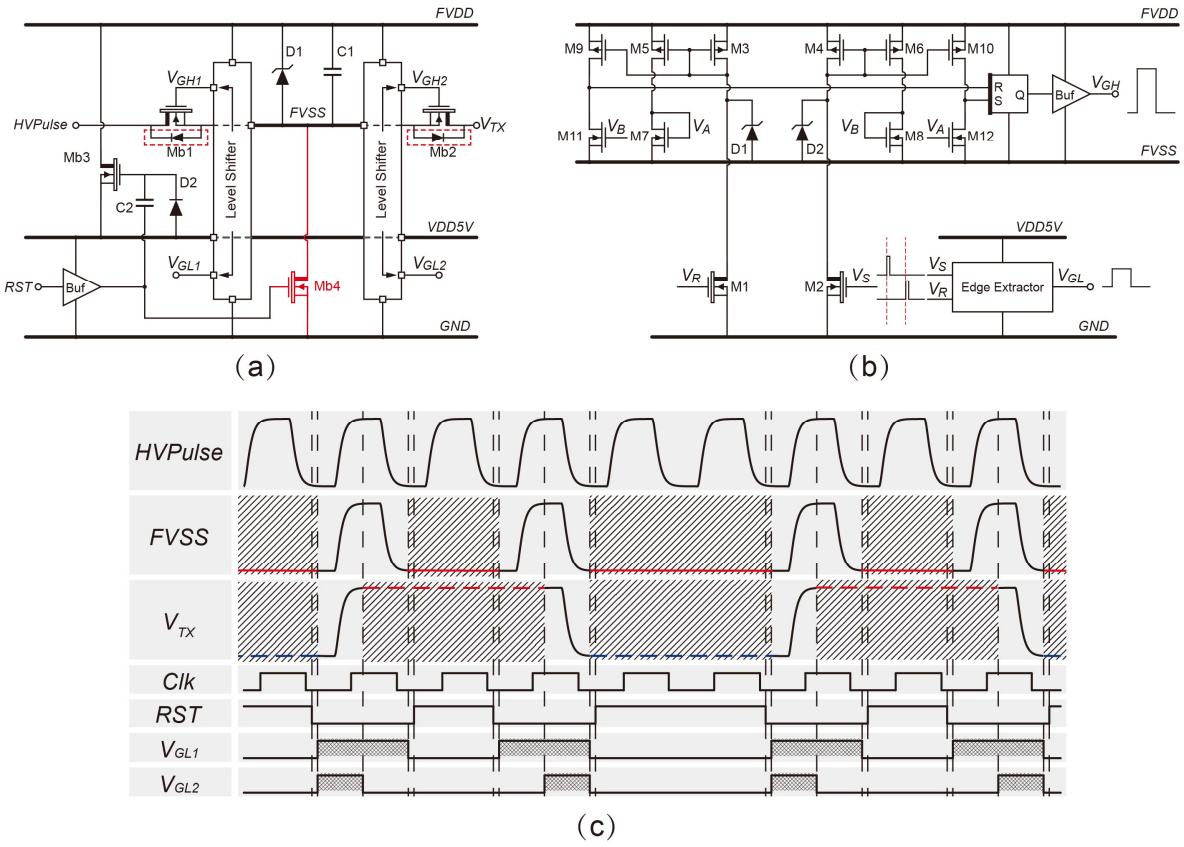


Figure 5. 5 (a) Schematic of the back-to-back connected switch and the associated control circuit; (b) Schematic of the level-shifter in (a); (c) Timing diagram of the back-to-back switch operation

The level-shifter shown in Fig. 5.5(b) level-shifts a low-side gate-control voltage V_{GL} into the high-side floating supply domain. Rather than doing this directly, an edge extractor circuit first converts V_{GL} into two pulses V_S and V_R that correspond to the rising and falling edges of V_{GL}, respectively. These pulses, with a pulse width of about 1 ns, then drive HV pull-down transistors M1 and M2 to transfer the edge information to the floating supply domain, where a digital SR latch restores the pulse and generates the high-side signal V_{GH}. This edge-based approach saves power by minimizing the shoot-through currents in M1 and M2.

Unlike conventional level-shifters that operate on a static high-side supply voltage, FVDD and FVSS are floating on the input HV pulse train. The rapid voltage change on FVDD leads to large dv/dt current noise I_N and eventually generates substantial voltage spikes which may mis-trigger the SR latch, causing the back-to-back switch to turn on and off unintentionally. Instead of directly connecting the M1 and M2 to the latch, the proposed level-shifter uses two diode-connected PMOS transistors M3 and M4 to sense I_N and subtract it from the signal current I_S and I_R, by replicating it using current mirrors formed by M5 ~

M12. The sizes of M3 and M4 are selected so that their gate-source voltages are less than 5V when M1 or M2 is on.

Fig. 5.5(c) shows the timing diagram of the HV pulse train switch circuit. V_{clk_d} is the output of the clock extraction circuit. RST is initially high to turn on M3 and M4, pre-charging C1 to 5 V. To pull up V_{TX}, RST becomes low, thus switching off both Mb3 and Mb4 and making FVSS and FVDD floating. Then V_{GL1} and V_{GL2} become high, switching on Mb1 and Mb2 at the same moment. Once V_{TX} has been pulled up, V_{GL2} becomes low to switch off Mb2 and V_{TX} is clamped to the HV supply. Mb1 remains on until HVPulse is pulled down, thus allowing FVSS to be discharged through the channel of M1, not through its forward-biased body diode. When both Mb1 and Mb2 are off, FVSS is reset to ground via Mb4, making sure the body diodes of Mb1 and Mb2 are always reverse-biased. Similarly, Mb4 is off and Mb1 and Mb2 are on to pull down V_{TX}; Mb1 is switched on a half-cycle earlier than Mb2 to pull up FVSS to the same voltage of V_{TX}. In order to make sure the gate voltages of Mb1 and Mb2 do not exceed 5 V, a non-overlapping period of 0.8 ns is created between RST and V_{GH1} and V_{GH2}.

5.3.3 Pull-up Switch

The pull-up switch M1 is implemented by a 36 V PMOS transistor (Fig. 5.6(a)). A small ON-resistance of 18.1 Ω was realized by sizing of M1 with a large W / L ratio (1300 µm /0.45 µm). Since the absolute gate-source voltage of M1 cannot exceed 5 V, the gate voltage of M1 is controlled by a capacitively-coupled level shifter consisting of a bootstrap capacitor C1 and two Zener diodes D1 and D2. During start-up, V_{PUL} is reset to high; the bottom plate of C1 is thus connected to 5 V via the low-side buffer, while its top plate slowly settles to HVDD by the leakage current of D1, pre-charging C1 to (HVDD – 5 V). During this reset phase, M1 is off.

During normal operation, M1 is turned on and off by directly coupling V_{GL} to the high-side gate control signal V_A via the pre-charged C1. V_A is buffered between HVDD and HVSS before driving the large gate of M1. HVSS is generated off-chip and is 5 V below *HVDD*. C1 is implemented by a HV metal-oxide-metal (MOM) capacitor with capacitance of 585.9 fF, sufficiently large compared to the overall parasitic capacitance at node A, thus maximizing the voltage swing of V_A and minimizing the associated time-delay due to the level-

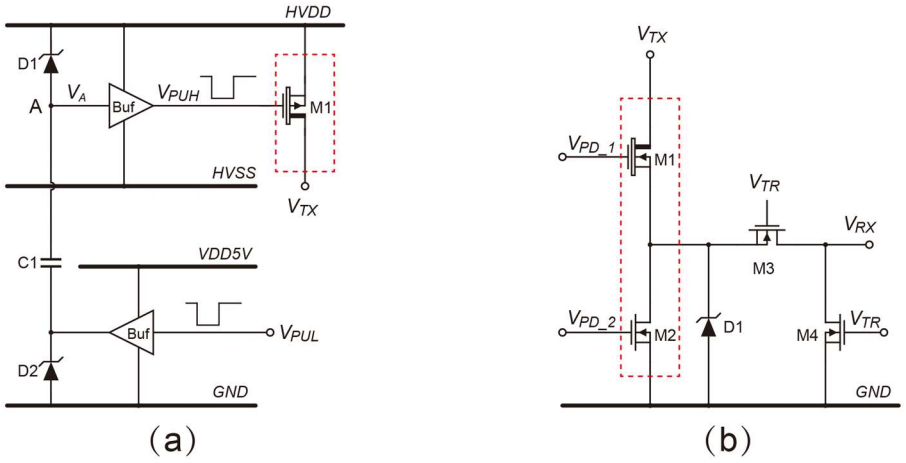


Figure 5. 6 (a) Schematic of the pull-up switch and its associated control circuit and (b) Schematic of the pull-down switch and TX/RX switch

shifting. This level shifter structure does not require any HV MOS devices by only using a HV capacitor, bringing in significant area benefit.

A drawback of this single-ended level shifter structure is that V_A is very sensitive to the supply bounce of HVDD, caused by the transient current through the inductive part of the supply line, thus turning on and off M1 unintentionally. However, this is less of an issue for this design, since HVDD is only used to clamp the transducer voltage to high; no large transient currents should be expected to be drawn from HVDD. The supply bounce can be further minimized by moderate on-chip decoupling capacitors.

5.3.4 Pull-down and TX/ RX Switches

As shown in Fig. 5.6(b), the pull-down switch is implemented by a n-type HV LDMOS transistor M1 in series with a 5 V NMOS transistor M2, the gates of which are controlled by V_{PD_1} and V_{PD_2}, respectively. During TX, M1 and M2 are turned on or off simultaneously, clamping the TX voltage to ground to generate the desired TX waveform; M3 forms a TX/ RX and is turned off to isolate the LV RX circuit from the pulser; M4 is turned on, shorting the input of the LV RX circuit to ground. After TX, in order to detect returning echo signals, M2 and M4 are off and M1 and M3 are on; thus, the received echo signal is read-out through M1 and M3. Compared to directly connecting an additional HV TX/ RX switch to the transducer element, this scheme significantly reduces the parasitic capacitance added to the transducer element, thus effectively improving SNR in RX. M1, M2 and M3 are sized such that the resistances of the pull-down

path and the RX path are 6.8 Ω and 60 Ω respectively. A Zener diode D1 prevents the drain-source voltage of M2 from exceeding 5 V.

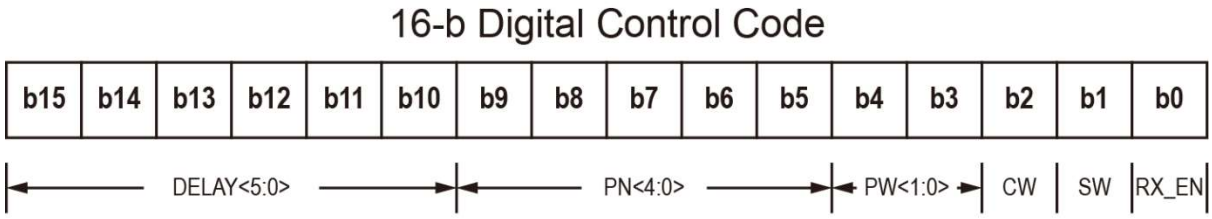


Figure 5. 7 Register table for 16-b TX digital control

5.3.5 Logic Control Circuits

The operation of each of the 32 channels of the proposed TX beamformer is configurated by a 16-b digital code (Fig. 5.7) via a built-in shift register. The 6-b code DELAY<5:0> specifies the number of 20 ns clock cycles before the transmission starts; PN<4:0> specifies the number of pulses transmitted in one transmit event. The duty cycle of the pulse can be adjusted in 4 discrete steps: 30%, 40%, 50% and 60%, by the 2-b PW code. By changing the duty cycle, the fundamental energy of the output pulse signals can be tuned, thus realizing an apodization function. The transmitter can be reconfigured to act as a conventional pulser (using only the pull-up and pull-down switches and not the pulse train) and to pulse continuously via the SW and CW bits, respectively. RX_EN is the read-out enable bit that opens the TX/ RX switch after the transmit event.

5.4 Measurement Results

A 32-channel HV transmitter chip has been fabricated in a 180 nm HV BCD technology. Its die micrograph is shown in Fig. 5.8(a). The whole chip measures 6160 μm × 1970 μm while the core area is about 5200 μm × 670 μm. The floorplan of a single-channel transmitter is shown in Fig. 5.8(b). The width of the transmitter is 150 μm, which make it compatible to a 32-channel, 5 MHz phased-array transducer, the pitch of which is typically 150 μm, half of the wavelength of the centre frequency. The HV pull-up and pull-down switches together with

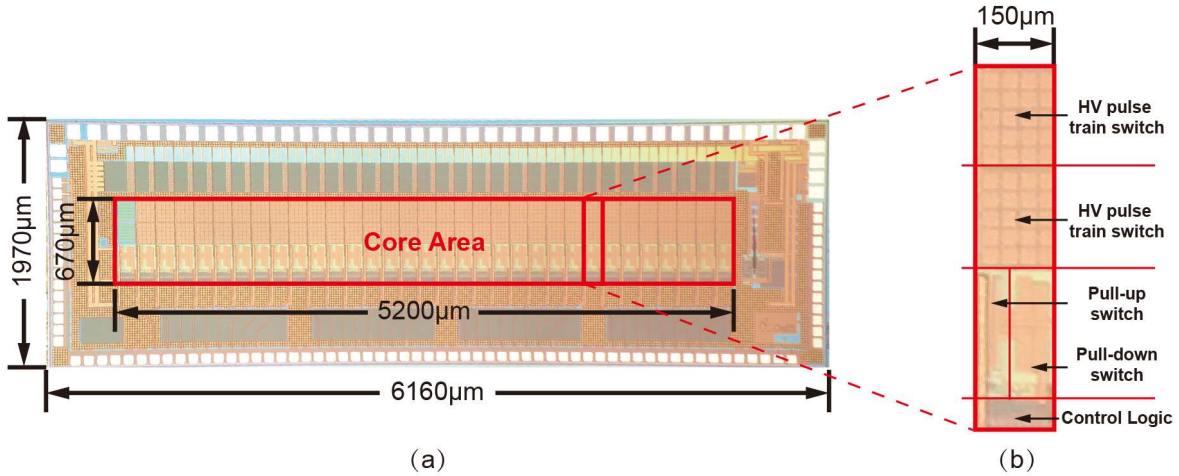


Figure 5. 8 (a) Micrograph of the transmitter ASIC; (b) Floorplan of a single-channel

the two HV pulse train switches occupy over 85% of the transmitter area, while the rest is for the 1.8 V and 5 V control logic and level-shifters.

The functionality of the proposed transmitter is electrically characterized by loading it with a 10 pF surface-mounted-device (SMD) capacitor, to mimic the transducer capacitance. Two complementary 30 V, 25 MHz pulse trains are generated by discrete HV transistors on a test PCB, capable of driving up to 2 nF of capacitive load. Fig. 5.9(a) shows the waveforms of the two complementary HV pulse trains and the waveform of a 1-cycle pulse from one channel transmitter output. The edges of the output waveform are well-overlapped with the edges of the HV pulses trains, demonstrating that the load capacitor is pulled up and down by the HV pulse trains.

The configurability of the chip is demonstrated by the waveforms shown in Fig. 5.9(b), (c) and (d). Transmitters in three adjacent channels are firstly programmed to pulse 1, 3 and 5 cycles, and to provide duty cycles of 30%, 50% and 70%, respectively. A minimum delay of 20 ns also applied to every two adjacent channels and can be observed in the 3 waveforms.

The power dissipation of the proposed transmitter is measured and compared with a conventional pulser. Since the power is mainly supplied by the HV pulse trains, to calculate the power consumption, both the transient voltages and the transient currents of the HV pulse trains would need to be acquired simultaneously. To overcome the challenge of measuring real-time currents, an

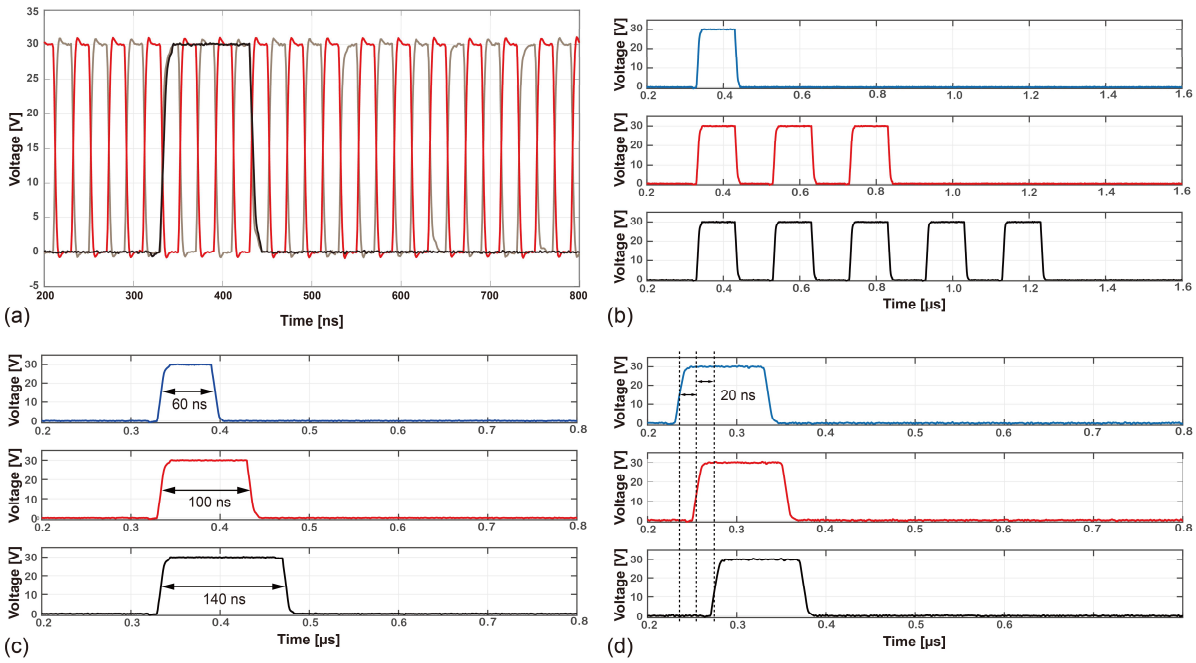


Figure 5. 9 (a). waveforms of the two complementary 30 MHz HV pulse trains and 1-cycle 5 MHz pulse transmitter output; outputs of 3 adjacent transmitters with: (b), 1, 3 and 5-cycles 5 MHz pulses; (c) 1-cycle pulse with 30%, 50% and 70% duty cycles and (d) 20ns delays between every two adjacent transmitters

indirect power measurement method is adopted by using a pair of on-chip thermal resistors. A sensor resistor R_S and a heater resistor R_H with resistances of 2030 Ω and 274 Ω are implemented by N+ and P+ type silicided poly resistors, respectively. The heater resistor R_H is connected to an external DC voltage supply and acts as a power source. The power dissipated in R_H causes a change

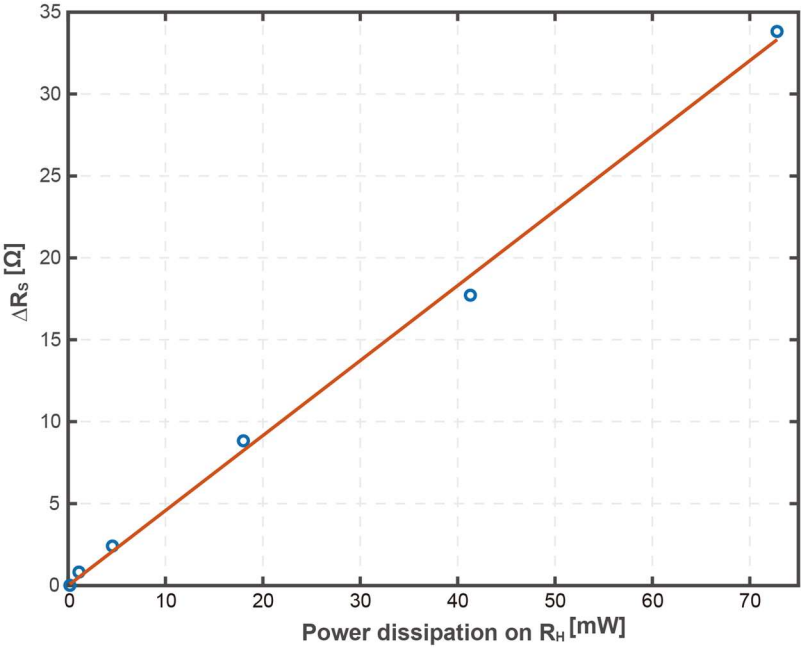


Figure 5. 10 Plot of sensor resistance change ΔR_S vs. power dissipation in ΔR_H

of the die temperature, which is sensed through a change in the resistance of R_S. By sweeping the DC voltage across R_H, the relationship between the change of resistance of R_S (ΔR_S) and the power dissipated in R_H is extracted, as shown in Fig. 5.10. To measure the power dissipation of the transmitter, R_H is disconnected from the voltage supply and one transmitter channel is turned on. The power dissipation of the transmitter can then be indirectly obtained by measuring ΔR_S and determining the equivalent power dissipation.

The transmitter is configured to generate 5-cycle 5 MHz pulses with a pulse repetition frequency of 50 kHz. The power dissipation causes a resistance variation of 0.67 Ω, corresponding to a power consumption of 1.45 mW. With the same pulsing configuration the transmitter can also operate as a conventional pulser by disabling the HV pulse train switches. The power consumption is then 3.79 mW, approximately 2.6 times higher, close to the simulated factor of 3.2 times. The discrepancy may be caused by a deviation of the capacitance of the SMD capacitor from the 10 pF value used in the simulation.

5.5 Conclusion

This chapter has presented a power-efficient HV transmitter design that is capable of providing TX beamforming functionality with only three HV connections to the system. The power-efficiency and beamforming functionality have been verified by a prototype ASIC consisting of 32 transmitter channels. When loaded by a 10 pF capacitor, the proposed HV transmitter generates 30 V, 5 MHz pulses with 2.6 times lower power consumption than a conventional pulser generating the same pulses. Supplied by two complementary 25 MHz pulse trains, the ASIC is capable of providing a minimum delay resolution of 20 ns, which is small enough for TX beamforming in miniature probes operating at frequencies below 10 MHz, such as transesophageal echocardiogragy (TEE) and intra-cardiac echocardiography (ICE) probes. The proposed HV transmitter can be a good alternative to a conventional pulser in future miniature probe designs where the in-probe power dissipation is crucial.

References

[1] Q. Huang and Z. Zeng, "A Review on Real-Time 3D Ultrasound Imaging Technology.," *Biomed Res. Int.*, vol. 2017, p. 6027029, 2017, doi: 10.1155/2017/6027029.

[2] L. Mearini and M. Porena, "Transrectal high-intensity focused ultrasound for the treatment of prostate cancer: past, present, and future.," *Indian J. Urol.*, vol. 26, no. 1, pp. 4–11, 2010, doi: 10.4103/0970-1591.60436.

[3] J. L. Foley, S. Vaezy, and L. A. Crum, "Applications of high-intensity focused ultrasound in medicine: Spotlight on neurological applications," *Appl. Acoust.*, vol. 68, no. 3, pp. 245–259, 2007, doi: 10.1016/j.apacoust.2005.09.009.

[4] Y. Kim, H. Rhim, M. J. Choi, H. K. Lim, and D. Choi, "High-intensity focused ultrasound therapy: an overview for radiologists.," *Korean J. Radiol.*, vol. 9, no. 4, pp. 291–302, 2008, doi: 10.3348/kjr.2008.9.4.291.

[5] T. Ma, B. Zhou, T. K. Hsiai, and K. K. Shung, "A Review of Intravascular Ultrasound-based Multimodal Intravascular Imaging: The Synergistic Approach to Characterizing Vulnerable Plaques.," *Ultrason. Imaging*, vol. 38, no. 5, pp. 314–331, Sep. 2016, doi: 10.1177/0161734615604829.

[6] O. Farhanieh, A. Sahafi, R. Bardhan Roy, A. S. Ergun, and A. Bozkurt, "Integrated HIFU Drive System on a Chip for CMUT-Based Catheter Ablation System," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 3, pp. 534–546, 2017.

[7] C. Chen *et al.*, "A Front-End ASIC With Receive Sub-array Beamforming Integrated With a 32×32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 994–1006, Apr. 2017, doi: 10.1109/JSSC.2016.2638433.

[8] M. Tan *et al.*, "A front-end ASIC with high-voltage transmit switching and receive digitization for 3-D forward-looking intravascular ultrasound imaging," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2284–2297, 2018, doi: 10.1109/JSSC.2018.2828826.

[9] D. Van Willigen *et al.*, "ASIC Design for a Single-Cable 64-Element Ultrasound Probe," in *2018 IEEE International Ultrasonics Symposium (IUS)*, 2018, pp. 1–4, doi: 10.1109/ULTSYM.2018.8580162.

[10] E. Kang *et al.*, "23.6 A 2pA/√Hz Transimpedance Amplifier for Miniature

Ultrasound Probes with 36dB Continuous-Time Gain Compensation," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020, pp. 354–356.

[11] M. C. Chen *et al.*, "A pixel pitch-matched ultrasound receiver for 3-d photoacoustic imaging with integrated delta-sigma beamformer in 28-nm UTBB FD-SOI," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2843–2856, 2017, doi: 10.1109/JSSC.2017.2749425.

[12] C. Christoffersen, T. Ngo, R. Song, Y. Zhou, S. Pichardo, and L. Curiel, "Quasi Class-DE Driving of HIFU Transducer Arrays," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 1, pp. 214–224, Feb. 2019, doi: 10.1109/TBCAS.2018.2888990.

[13] Z. Gao, P. Gui, and R. Jordanger, "An Integrated High-Voltage Low-Distortion Current-Feedback Linear Power Amplifier for Ultrasound Transmitters Using Digital Predistortion and Dynamic Current Biasing Techniques," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 61, no. 6, pp. 373–377, 2014.

[14] J. Park, C. Hu, X. Li, Q. Zhou, and K. K. Shung, "Wideband linear power amplifier for high-frequency ultrasonic coded excitation imaging," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 59, no. 4, pp. 825–832, 2012.

[15] R. Chebli and M. Sawan, "Fully Integrated High-Voltage Front-End Interface for Ultrasonic Sensing Applications," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 54, no. 1, pp. 179–190, 2007.

[16] G. Jung *et al.*, "A Reduced-Wire ICE Catheter ASIC with Tx Beamforming and Rx Time-Division Multiplexing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 6, pp. 1246–1255, 2018, doi: 10.1109/TBCAS.2018.2881909.

[17] P. Behnamfar, R. Molavi, and S. Mirabbasi, "Transceiver Design for CMUT-Based Super-Resolution Ultrasound Imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 383–393, 2016.

[18] M. Tan *et al.*, "A 64-Channel Transmit Beamformer With ±30-V Bipolar High-Voltage Pulsers for Catheter-Based Ultrasound Probes," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1796–1806, 2020.

[19] M. Sautto *et al.*, "A CMUT transceiver front-end with 100-V TX driver and 1-mW low-noise capacitive feedback RX amplifier in BCD-SOI technology," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, 2014, pp. 407–410, doi: 10.1109/ESSCIRC.2014.6942108.

[20] Y. Qiu *et al.*, "Piezoelectric micromachined ultrasound transducer (PMUT)

arrays for integrated sensing, actuation and imaging," *Sensors (Switzerland)*, vol. 15, no. 4, pp. 8020–8041, 2015, doi: 10.3390/s150408020.

[21] E. Brunner, "How Ultrasound System Considerations Influence Front-End Component Choice." Analog Devices Inc., 2002.

[22] K. Chen, H. Lee, A. P. Chandrakasan, and C. G. Sodini, "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2734–2745, 2013.

[23] E. Kang *et al.*, "A Reconfigurable Ultrasound Transceiver ASIC With 24×40 Elements for 3-D Carotid Artery Imaging," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 2065–2075, 2018, doi: 10.1109/jssc.2018.2820156.

[24] K. Iniewski, *Medical Imaging: Principles, Detectors, and Electronics*, 1st Edition. Wiley-Interscience, 2009.

[25] M. B. Stuart, J. Jensen, T. Di Ianni, and J. A. Jensen, "Image quality degradation from transmit delay profile quantization," in *2015 IEEE International Ultrasonics Symposium (IUS)*, 2015, pp. 1–4.

[26] Master Thesis: F. Fool, "Beamforming for novel matrix arrays - Fresnel Zone Beamforming and Stolt Migration." 2017

CHAPTER 6

CONCLUSION

In this thesis, various integrated circuit designs, implemented in both analogue and digital manners and for both low-voltage receive and high-voltage transmit functionality, have been proposed as promising solutions to tackle the interconnection bottleneck for next-generation miniature 3-D ultrasound probes. Firstly, the proposed low-power analogue receive subarray beamformer ASIC allows to use 9 × fewer receive cables by only sending out the pre-beamformed receive echoes of 3 × 3 subarrays. As an additional step forward, an ASIC with digital TDM has been proposed that combines 4 pre-beamformed subarray signals onto one cable by firstly digitizing them using a group of subarray beamforming ADCs, which has been demonstrated to be an efficient way of moving digitization inside miniature ultrasound probes. The study on the impact of bit errors in digitized RF data transmission on ultrasound image quality has revealed the potential to further reduce cable count by exploiting the robustness for bit errors to increase the data rate per cable. Moving from receive to transmit, a power-efficient transmit beamformer ASIC capable of providing sufficient TX beamforming functionality has been proposed which requires only 3 HV cable connections to the system, significantly relaxing the interconnection challenge for transmit. This chapter summarizes the original contributions and the main findings of the thesis. In addition, suggestions for future work on potential solutions to further minimize cable count in 3-D miniature ultrasound probes are presented.

6.1 Main Contributions

- Realization of a 9-fold cable-count reduction by means of an on-chip analogue subarray beamforming circuit with record power-efficiency (Chapter 2)

We have demonstrated a 9-fold receive-cable-count reduction by implementing analogue subarray beamformers in a front-end ASIC integrated with a 32 × 32 PZT transducer array. With the proposed transducer partitioning, which allows the majority of the elements to be used only for reception, the

transducer array can be interfaced to an imaging system with less than 200 cables. The ASIC achieves a record power efficiency (0.27 mW/element) that is 5× better than the state-of-the-art. Compared to the targeted 1 mW/element, this leaves room to adopt more aggressive on-chip cable count reduction techniques.

- Demonstration of the feasibility of cable-count reduction by means of hybrid subarray beamforming and digital TDM (Chapter 3)

We have demonstrated a 36-fold receive-cable-count reduction by implementing digital TDM circuits together with subarray beamformers and ADCs in a front-end ASIC integrated with a 9 × 24 prototype transducer array. The channel count reduction realized by subarray beamformers enables digitization within the subarrays while meeting the stringent power and area requirements. Digital TDM further reduces channel/ cable count with better signal integrity compared to its analogue counterpart.

- Investigation of the impact of bit errors in digitized RF data on B-mode ultrasound image quality (Chapter 4)

Our study reveals that there is unnoticeable image quality degradation when BER level is lower than 10^{-6}, about 5~6 orders of magnitude higher than the BER requirements typically used in digital communication. This relatively relaxed BER requirement can be valuable to guide future digital ultrasound probe designs to optimize the trade-off among power consumption, data rate and cable count in the datalink.

- Demonstration of a new power-efficient ultrasound transmitter architecture with 3 HV cable connections (Chapter 5)

We have demonstrated a new ultrasound transmitter that is more than two times more power-efficient than a conventional pulser while only requiring 3 HV cable connections. Supplied by two complementary 25 MHz pulse trains, the transmitter is capable of providing a minimum delay resolution of 20 ns, which is small enough for miniature probes with frequencies below 10 MHz.

6.2 Main Findings

- Receive subarray beamforming is an efficient and reliable cable count reduction technique for real-time 3-D ultrasound imaging. With a power- and area- efficient circuit implementation, a subarray beamformer ASIC can be

integrated with a 2-D ultrasound transducer with 1000+ elements in a pitch-matched manner and realizes an order of magnitude cable count reduction factor.

- A split-array transducer configuration with small TX aperture allows to use an affordable number of cables for TX without integrating area-costly TX ASICs in the probe; while relaxing the area constraint for implementing more efficient RX cable count reduction techniques across a fully populated 2-D transducer array.

- Cable count reduction is always at the cost of the final image quality or frame rate. A good balance should be made according to the targeted applications.

- The high tolerance to bit errors in the raw element RF data for B-mode ultrasound imaging relaxes the design challenge of the datalink of ultrasound probes with in-probe receive digitization; this allows the datalink to be optimized for either a more aggressive cable count reduction factor or lower in-probe power consumption.

6.3 Future Work

- Digitally-assisted cable count reduction techniques in deep sub-micron CMOS technologies:

Chapter 3 has demonstrated the feasibility of in-probe digitization within the subarray and subsequent cable count reduction by digital TDM in 180nm CMOS technology. The higher integration density that can be achieved in deep sub-micron technologies would allow the implementation of element-level digitization as well as more complex digital processing algorithms to further reduce the cable count. This would bring us the flexibility of accessing either the raw data of every (receive-only) element across the full array, or fully compressed/ beamformed data with minimum cable count, depending on the application requirements. A recent study in Stanford [1] proposed a digital subarray beamformer by implementing on-chip element-level digitizers in a 4 × 4 cMUT subarray in 28nm FDSOI technology. However the pitch of the active circuit per element is still beyond the desired half wavelength transducer pitch, and the power consumption per element exceeds the power-consumption target of a miniature probe. Moreover, the work is still based on the concept of subarray beamforming. If raw digitized element data is accessible, together with on-chip

digital memories more advanced beamforming techniques can be applied for efficient data reduction, thus cable reduction.

- Optical links to expand the communication channel capacity:

With the benefit of deep-submicron technologies, the communication channels, typically micro-coaxial cables in current ultrasound probes, start to become the bottleneck for data communication. Optical fibres, which have a much wider bandwidth than copper cables, can be an alternative to coaxial cables. The relatively low BER requirement for ultrasound probes studied in Chapter 4 would allow a fully populated 2-D array to communicate with the imaging system with only several optical fibres. A recent preliminary study [2] on an assembly of a vertical-cavity surface-emitting laser (VCSEL) and a CMOS chip in an IVUS probe shows a promising prototype for adopting optical link in a digital ultrasound probe.

- Extending the BER study to flow imaging:

Since ultrasound probes are typically not only used for B-mode imaging but also for measuring blood flow using the Doppler effect, it would be very valuable to extend the BER study in Chapter 4 by evaluating the effect of bit errors on Doppler flow imaging.

- Advanced transducer-ASIC integration and packaging solutions:

Although different transducer-ASIC integration techniques and packaging solutions do not directly affect the cable count of an ultrasound probe, they may bring significant limitations on the choice of cable count reduction techniques. For instance, if the parasitic capacitance from transducer-ASIC integration dominates the load of an on-chip transmitter, it may not be possible to reduce the TX cable count by integrating a transmitter in the probe due to excessive undesired in-probe power dissipation on the parasitic capacitances. The PZT-on-CMOS integration solution shown in Chapter 2 and 3 is a good solution to minimize the parasitic effects, but it is based on a relatively labour-intensive dicing process [3] and may be less attractive for mass production. cMUT [4] and pMUT [5] transducers can be good alternatives to bulk-piezo transducers in terms of fabrication cost and integration density, provided their performance is comparable to PZT transducers. For applications where full TX/ RX aperture is required, the technology choice for the ASIC is limited to a feature size that is typically higher than 130 nm, due to the need for a HV process for transmitter design, thus complicating cable-count reduction techniques that require powerful digital processing. Having separate TX and RX chips would allow both chips to

be optimized in their favourable processes. Advanced 3-D packaging solutions, for instance through-silicon-vias (TSVs) would allow the two chips to be stacked vertically, similar to the approach taken in advanced CMOS imager sensors [6], [7], thus not affecting the form factor of the probe head.

References

[1] M. C. Chen *et al.*, “A pixel pitch-matched ultrasound receiver for 3-d photoacoustic imaging with integrated delta-sigma beamformer in 28-nm UTBB FD-SOI,” *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2843–2856, 2017.

[2] R. Stoute, M. C. Louwerse, J. van Rens, V. A. Henneken, and R. Dekker, “Optical data link assembly for 360 μm diameter IVUS on guidewire imaging devices,” in *SENSORS, 2014 IEEE*, 2014, pp. 217–220.

[3] C. Chen, et al., "A Prototype PZT Matrix Transducer with Low-Power Integrated Receive ASIC for 3-D Transesophageal Echocardiography," IEEE Trans. Ultrason., Ferroelectr., Freq. Control, vol. 63, pp. 47 - 59, Jan. 2016.

[4] A. Bhuyan *et al.*, “Integrated Circuits for Volumetric Ultrasound Imaging With 2-D CMUT Arrays,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 796–804, 2013.

[5] D. E. Dausch, J. B. Castellucci, D. R. Chou, and O. T. von Ramm, “Theory and operation of 2-D array piezoelectric micromachined ultrasound transducers,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 55, no. 11, pp. 2484–2492, 2008.

[6] C. C. Liu *et al.*, “6.8 A 1.5V 33Mpixel 3D-stacked CMOS image sensor with negative substrate bias,” in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 124–125.

[7] Q. Liu, A. Edward, M. Kinyua, E. G. Soenen, and J. Silva-Martinez, “A Low-Power Digitizer for Back-Illuminated 3-D-Stacked CMOS Image Sensor Readout With Passing Window and Double Auto-Zeroing Techniques,” *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1591–1604, 2017.

SUMMARY

This thesis describes low-power application-specific integrated circuit (ASIC) designs to mitigate the constraint of cable count in miniature 3-D TEE probes. Receive cable count reduction techniques including subarray beamforming and digital time-division multiplexing (TDM) have been explored and the effectiveness of these techniques has been demonstrated by experimental prototypes. Digital TDM is a reliable technique to reduce cable count but it requires an in-probe datalink for high-speed data communication. A quantitative study on the impact of the datalink performance on B-mode ultrasound image quality has been introduced in this thesis for data communications in future digitized ultrasound probes. Finally, a high-voltage transmitter prototype has been presented for effective cable count reduction in transmission while achieving good power efficiency.

Chapter 1

Chapter 1 introduces the application background as well as the motivation of this thesis work. 3-D TEE probes rely on 2-D ultrasound transducers with more and more elements for better image quality, while probe miniaturization calls for a reduction of the number of cables accommodated in the gastroscopic tube, thus causing a communication challenge between the imaging system and the transducer elements. In-probe ASICs capable of processing ultrasound signals and reducing cable count are promising to mitigate this problem, but the ASIC design is subject to stringent power and area constraints. A review of various cable count reduction techniques is presented. In-probe transmission, subarray beamforming and multiplexing are identified as promising approaches, in particular if they are used in combination and if they are combined with in-probe digitization, so that multiplexing can be implemented in the form of digital TDM. These approaches are explored in the next chapters.

Chapter 2

In chapter 2, a front-end ASIC with low power analogue delay-and-sum (DAS) circuits for a 32 × 32 PZT transducer is presented. To reduce the cable count in transmit, a split transmit-receive topology is adopted instead of employing area-hungry high-voltage transmit circuits. Only an 8 × 8 central subarray is directly wired out to the transmit channels in the external imaging system while keeping the majority of the elements for receive. The analogue DAS circuits are designed for a subarray beamforming scheme with a subarray size of 3 × 3, thus realizing a 9-fold cable count reduction. A technique to mitigate the ripple signal associated with mismatch of the analogue DAS circuits is also proposed to enhance the dynamic range of the received echo signals. The ASIC was integrated with a 32 × 32 PZT transducer. Electrical and acoustic characterization results are presented.

Chapter 3

Chapter 3 presents a receive ASIC with digital TDM function to further reduce cable count. The digital TDM is applied over the pre-beamformed 3 × 3 subarray signals as described in chapter 2 instead of raw element signals, thus significantly relaxing the power and area constraints of the ADC design. An ADC architecture with incorporated beamforming function is proposed to optimize the power consumption. High-speed datalinks perform 4 × TDM to the digitized subarray data and transmit the serialized data to the system with a speed of 1.65 Gb/s and a BER < 10e-9. Thus, an overall 36-fold output channel reduction is demonstrated with a 9 × 24 prototype transducer while achieving a power consumption of < 1mW per element, which is almost equally contributed by the front-end plus ADC and the high-speed datalink.

Chapter 4

In chapter 4, a quantitative study of the impact of BER in digitized RF data on ultrasound image quality is presented. A simulation setup is proposed to quantitatively assess the quality of B-mode images in the presence of bit errors based on multiple objective image quality metrics. The efficiency of different coding schemes for data transmission is also studied. A case study reveals that there is unnoticeable image quality degradation when BER level is lower than 1E-6, about 5~6 orders of magnitude lower than the BER requirement typically used in digital communication. This low BER requirement allows the datalink to operate at a higher data rate per cable, thus reducing the number of cables required,

or to operate at the same data rate per cable, while reducing the overall power consumption.

Chapter 5

In Chapter 5, an ultrasound transmitter ASIC is proposed to further minimize the transmit cable count while achieving better power efficiency compared to conventional HV pulsers. The design employs two high-frequency high-voltage pulse trains provided by the imaging system, which are intermittently connected to the transducer elements to realize the rising and falling edges of the desired high-voltage pulses. In between, the elements are clamped to ground or a high-voltage DC, also provided by the system. Thus, with only 3 HV connections to the imaging system, the proposed transmitter is capable of providing full TX beamforming function while only dissipating half of the power consumption of a conventional pulser.

Chapter 6

Chapter 6 summarizes the original contributions and the main findings of this thesis. The prototyping ASICs presented in this thesis provide over an order of magnitude of cable count reduction in both reception and transmission, while achieving state-of-the-art power- and area-efficiency. The revealed high BER tolerance in ultrasound data transmission shows potential to further reduce cable count for ultrasound probes with in-probe digitization. Possible future work for further cable count reduction, like in-probe digital data compression, optical communication and advanced transducer-ASIC integration and packaging solutions are also discussed in this chapter.

SAMENVATTING

Dit proefschrift beschrijft laagvermogen applicatiespecifieke geïntegreerde schakelingen (ASICs) om het benodigde aantal kabels in miniatuur 3D TEE-sondes te verminderen. Verschillende technieken zijn onderzocht voor het verminderen van het aantal benodigde kabels in ontvangst, waaronder subarray bundelvorming en digitale tijdverdelingsmultiplexing (TDM). Daarbij is de effectiviteit van deze technieken aangetoond met experimentele prototypes. Digitale TDM is een betrouwbare techniek om het aantal kabels te verminderen, maar het vereist een datalink in de sonde met een snelle datacommunicatie. In dit proefschrift wordt een kwantitatieve studie naar de invloed van de datalinkprestaties op de beeldkwaliteit van de B-mode echografie geïntroduceerd voor datacommunicatie in toekomstige gedigitaliseerde ultrasone sondes. Ten slotte is er een prototype van een hoogspanningsschakeling gepresenteerd voor een effectieve vermindering van het aantal kabels bij de transmissie, waarmee een goede vermogens-efficiëntie wordt bereikt.

Hoofdstuk 1

Hoofdstuk 1 introduceert de toepassingsachtergrond en de motivatie van dit proefschrift. 3D TEE-sondes vereisen 2D-ultrasone transducenten met steeds meer elementen voor een betere beeldkwaliteit, terwijl de miniaturisatie van de sonde een vermindering van het aantal kabels in de gastroscopische buis vereist, waardoor een communicatieprobleem ontstaat tussen het beeldvormingssysteem en de transducenten. Het gebruik van ASIC's in sondes is veelbelovend om ultrasone signalen te verwerken en het aantal kabels te verminderen, maar het ASIC-ontwerp is onderhevig aan strikte vermogens- en oppervlaktebeperkingen. Er wordt een overzicht gegeven van verschillende technieken om het aantal kabels te verminderen. Transmissie in de sonde, subarray bundelvorming en multiplexing worden geïdentificeerd als veelbelovende aanpak, met name als ze in combinatie worden gebruikt en als ze worden gecombineerd met digitalisering in de sonde, zodat multiplexing kan worden geïmplementeerd in de vorm van digitale TDM. Deze methodes worden in de volgende hoofdstukken onderzocht.

Hoofdstuk 2

In hoofdstuk 2 wordt een front-end ASIC met een laagvermogen analoge vertraag-en-sommerings (DAS) schakeling voor een 32 × 32 PZT transducent gepresenteerd. Om het aantal kabels bij het verzenden te verminderen, wordt een gesplitste zend-ontvangst-topologie toegepast in plaats van gebruik te maken van hoogspanningscircuits die veel ruimte innemen. Enkel een 8 × 8 centrale subarray is rechtstreeks verbonden met de zendkanalen in het externe beeldvormingssysteem waardoor de meerderheid van de elementen beschikbaar blijft voor ontvangst. De analoge DAS-schakelingen zijn ontworpen voor een subarray bundelvormingsschema met een subarray-afmeting van 3 × 3, waardoor een 9-voudige vermindering van het aantal kabels wordt gerealiseerd. Er wordt ook een techniek voorgesteld om het rimpelsignaal dat is geassocieerd met mismatch van de analoge DAS-circuits te verminderen, om het dynamisch bereik van de ontvangen echosignalen te vergroten. De ASIC werd geïntegreerd met een 32 × 32 PZT-transducer. Tot slot worden resultaten van de elektrische en akoestische karakterisering gepresenteerd.

Hoofdstuk 3

Hoofdstuk 3 presenteert een ontvangst-ASIC met digitale TDM-functie om het aantal kabels verder te verminderen. De digitale TDM wordt toegepast over de gebundelvormde signalen van de 3 × 3 subarray's, zoals beschreven in hoofdstuk 2, in plaats van over de onbewerkte elementsignalen. Het vermogen en de benodigde oppervlakte voor het ADC-ontwerp worden daardoor aanzienlijk verminderd. Een ADC-architectuur met ingebouwde bundelvormingsfunctie wordt voorgesteld om het vermogensverbruik te optimaliseren. Hoge-snelheid dataverbindingen voeren 4 × TDM uit op de gedigitaliseerde subarray-data en verzenden de geserialiseerde data naar het systeem met een snelheid van 1.65 Gb/s en een BER < 10e-9. Daarmee wordt een 36-voudige vermindering van het aantal outputs aangetoond met een 9 × 24 prototype transducer, terwijl een vermogensverbruik van <1 mW per element wordt bereikt, waarbij de front-end en ADC vrijwel hetzelfde vermogen gebruiken als de snelle datalink.

Hoofdstuk 4

In hoofdstuk 4 wordt een kwantitatieve studie gepresenteerd over de impact van de bitfoutkans (BER) in gedigitaliseerde RF-data op de beeldkwaliteit van

echografie. Er wordt een simulatieopstelling voorgesteld om de kwaliteit van B-mode beelden kwantitatief te beoordelen in de aanwezigheid van bitfouten op basis van meerdere objectieve beeldkwaliteitsmetrieken. Ook wordt de efficiëntie van verschillende coderingsschema's voor datatransmissie bestudeerd. Een casestudy laat zien dat er een onmerkbare verslechtering van de beeldkwaliteit is wanneer de BER lager is dan 1e-6, ongeveer 5-6 ordes van grootte lager dan de vereiste BER die doorgaans wordt gebruikt in digitale communicatie. Deze lagere eis aan de BER stelt de datalink in staat om met een hogere datasnelheid per kabel te werken, waardoor het aantal benodigde kabels wordt verminderd, of om met dezelfde datasnelheid per kabel te werken, terwijl het totale vermogensverbruik wordt verminderd.

Hoofdstuk 5

In Hoofdstuk 5 wordt een ASIC voorgesteld voor het uitzenden van ultrasone signalen, die het aantal transmissiekabels verder kan minimaliseren en tegelijkertijd een betere vermogens-efficiëntie bereikt in vergelijking met conventionele hoogspanningspulsers. Het ontwerp maakt gebruik van twee hoogfrequente hoogspanningspulstreinen die worden geleverd door het beeldvormingssysteem, die met tussenpozen zijn verbonden aan de transducenten om de stijgende en dalende flanken van de gewenste hoogspanningspulsen te realiseren. Tussendoor worden de elementen verbonden met aarde of een hoogspannings-DC, ook geleverd door het systeem. Met slechts 3 hoogspannings-verbindingen met het beeldvormingssysteem is de voorgestelde zender dus in staat om een volledige TX bundelvormingsfunctie te leveren terwijl slechts de helft van het vermogen van een conventionele pulser wordt gedissipeerd.

Hoofdstuk 6

Hoofdstuk 6 geeft een samenvatting van de unieke bijdragen en de belangrijkste bevindingen van dit proefschrift. De ASIC prototypes die in dit proefschrift worden gepresenteerd zorgen voor een reductie van het aantal kabels in zowel ontvangst als transmissie met meer dan een orde van grootte, terwijl ze tegelijkertijd een state-of-the-art vermogens- en oppervlakte-efficiëntie bereiken. De onthulde hoge bitfoutkans-tolerantie bij gegevensoverdracht van ultrasone data toont het potentieel aan van het verder verminderen van het aantal kabels in ultrasone sondes, door gebruikt te maken van digitalisering in de sonde. Mogelijke toekomstige werkzaamheden voor een verdere vermindering van het

aantal kabels worden ook in dit hoofdstuk besproken, zoals digitale datacompressie in de sonde, optische communicatie en geavanceerde transducer-ASIC-integratie en ASIC-behuizingen.

TABLE OF FIGURES

LIST OF ABBREVIATIONS

1-D	One-dimensional
2-D	Two-dimensional
3-D	Three-dimensional
AWGN	Additive white Gaussian noise
AFE	Analogue front-end
A/D	Analogue-to-digital
ADC	Analogue-to-digital converter
ASIC	Application-specific integrated circuit
BER	Bit-error-rate
cMUT	Capacitive micro-machined ultrasound transducer
CVD	Cardiovascular disease
CDR	Clock-data-recovery
CMOS	Complementary Metal Oxide Semiconductor
CT	Computed tomography
CNR	Contrast-to-noise ratio
DAS	Delay-and-sum
DLL	Delay-locked-loop
DFF	D-flip-flops
DSP	Digital signal processing
DAC	Digital-to-analogue converter
DMOS	Double-diffused MOS
DR	Dynamic range
FPGA	Field programmable gate array
FIFO	First-in, first out
FEDC	Forward error detection/ correction
FDM	Frequency-division multiplexing
FDSOI	Fully-depleted silicon-on-insulator
HIFU	High-intensity focused ultrasound

HV	High-voltage
IQA	Image quality analysis
IQM	Image quality metrics
IC	Integrated circuit
ISI	Inter-symbol interference
ICE	Intracardiac echocardiography
IVUS	Intravascular ultrasound
LDMOS	Laterally-diffused MOS
PZT	Lead zirconate titanate
LSB	Least-significant bit
LFSR	Linear-feedback shift register
LDO	Low-dropout regulator
LNA	Low-noise amplifier
LV	Low-voltage
LVDS	Low-voltage differential signaling
MRI	Magnetic resonance imaging
MSE	Mean-squared error
MIM	Metal-insulator-metal
MOM	Metal-oxide-metal
MOS	Metal-oxide-semiconductor
MUT	Micro-machined ultrasound transducer
MSB	Most-significant bit
NEF	Noise-efficiency factor
NRZ	Non-return-to-zero
OPA	Operational transconductance amplifier
PSNR	Peak-signal-to-noise ratio
pMUT	Piezoelectrical micro-machined ultrasound
PCB	Printed circuit board
PVT	Process/voltage/ temperature
PGA	Programmable-gain amplifier
PRBS	Pseudo-random bit sequence
PRNG	Pseudo-random number generator

PAM	Pulse amplitude modulation
PRF	Pulse repetition frequency
RX	Receive
ROI	Region-of-interest
RZ	Return-to-zero
SPI	Serial peripheral interface
SNR	Signal-to-noise ratio
SNDR	Signal-to-noise-and-distortion ratio
SSIM	Structural similarity
SAR	Successive-approximation-register
SMD	Surface-mounted-device
SC	Switched-capacitor
TSV	Through-silicon-vias
TDM	Time-division multiplexing
TGC	Time-gain compensation
TEE	Transoesophageal echocardiography
TIA	Trans-impedance amplifiers
TX	Transmit
TX/ RX	Transmit/ receive
TTE	Transthoracic echocardiography
VCSEL	Vertical-cavity surface-emitting laser
VCDL	Voltage-controlled delay line

LIST OF PUBLICATIONS

Journal Articles

Z. Chen, M. Soozande, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong and M. A. P. Pertijs, "Impact of Bit Errors in Digitized RF Data on Ultrasound Image Quality", *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 67, no. 1, pp 13-24, Jan. 2020;

C. Chen, **Z. Chen**, D. Bera, E. Noothout, Z.-Y. Chang, M. Tan, H.J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M.A.P. Pertijs, "A Pitch-Matched Front-End ASIC With Integrated Subarray Beamforming ADC for Miniature 3-D Ultrasound Probes", *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3050-3064, Nov. 2018 ***(equal 1st author contribution)***;

C. Chen, **Z. Chen**, D. Bera, S.B. Raghunathan, M. Shabanimotlagh, E. Noothout, Z.-Y. Chang, J. Ponte, C. Prins, H.J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M.A.P. Pertijs, "A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography", *IEEE Journal of Solid State Circuits*, vol. 52, no. 4, pp. 994-1006, Apr. 2017;

D. Bera, S.B. Raghunathan, C. Chen, **Z. Chen**, M.A.P. Pertijs, M.D. Verweij, V. Daeichin, H. J. Vos, A. F. W. van der Steen, N. de Jong and J.G. Bosch, "Multiline 3D beamforming using micro-beamformed datasets for pediatric transesophageal echocardiography", *Physics in Medicine and Biology*, vol. 63, no. 7, Mar. 2018;

C. Chen, S.B. Raghunathan, Z. Yu, M. Shabanimotlagh, **Z. Chen**, Z.-Y. Chang, S. Blaak, C. Prins, J. Ponte, E. Noothout, H. J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M.A.P. Pertijs, "A Prototype PZT Matrix Transducer with Low-Power Integrated Receive ASIC for 3D Transesophageal Echocardiography", *IEEE Trans. on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 63, no. 1, pp. 47-59, Jan. 2016;

M. D'Urbino, C. Chen, **Z. Chen**, Z.-Y. Chang, J. Ponte, B. Lippe and M.A.P. Pertijs, "An Element-Matched Electromechanical ΔΣ ADC for Ultrasound Imaging", *IEEE Journal of Solid-State Circuits*, vol. 53, no. 10, pp. 2795-2805, Apr. 2018;

M. Tan, C. Chen, **Z. Chen**, J. Janjic, V. Daeichin, Z.-Y. Chang, E. Noothout, G. van Soest, M. D. Verweij, N. de Jong and M.A.P. Pertijs, "A Front-End ASIC with High-Voltage Transmit Switching and Receive Digitization for 3D Forward-Looking Intravascular Ultrasound Imaging", IEEE Journal of Solid-State Circuits, vol. 53, no. 8, pp. 2284-2297, Aug. 2018;

J. Janjic, M. Tan, V. Daeichin, E. Noothout, C. Chen, **Z. Chen**, Z.-Y. Chang, R. H. S. H. Beurskens, G. van Soest, A. F. W. van der Steen, M. D. Verweij, M.A.P. Pertijs and N. de Jong, "A 2-D Ultrasound Transducer With Front-End ASIC and Low Cable Count for 3-D Forward-Looking Intravascular Imaging: Performance and Characterization", *IEEE Trans. on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 65, no. 10, pp. 1832-1844, Jul. 2018;

V. Daeichin, D. Bera, S.B. Raghunathan, M. Shabanimotlagh, **Z. Chen**, C. Chen, E. Noothout, H. J. Vos, M.A.P. Pertijs, J.G. Bosch, N. de Jong and M.D. Verweij, "Acoustic characterization of a miniature matrix transducer for pediatric 3D transesophageal echocardiography", *Ultrasound in Medicine & Biology*, vol. 44, no. 10, pp. 2143-2154, Oct. 2018;

Z. Chen, E. Noothout, Z.-Y. Chang, H. J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M. A. P. Pertijs, "A Power-Efficient Transmit Beamformer ASIC for Minimally Invasive Ultrasound Probes", in preparation for submission.

Conference Proceedings

Z. Chen, M. Soozande, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong and M. A. P. Pertijs, "A quantitative study on the impact of bit errors on image quality in ultrasound probes with in-probe", *IEEE Ultrasonics Symp. (IUS)*, Sept. 2018, *(Abstract)*.

Z. Chen, E. Kang, Z.-Y. Chang, H. J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M. A. P. Pertijs, "A Power-Efficient Transmit Beamformer ASIC for 3-D Catheter-Based/ Endoscopic Probes" , *IEEE Ultrasonics Symp. (IUS)*, Sept. 2018, *(Abstract)*.

J. Li, **Z. Chen**, M. Tan, D. van Willigen, C. Chen, Z.-Y. Chang, E. Noothout, N. de Jong, M.D. Verweij, and M.A.P. Pertijs, "A 1.54mW/Element 150μm-Pitch-Matched Receiver ASIC with Element-Level SAR/Shared-Single-Slope Hybrid ADCs for Miniature 3D Ultrasound Probes," in Dig. Symp. on VLSI Circuits, pp. 220-221, July 2019.

C. Chen, **Z. Chen**, D. Bera, E. Noothout, Z.-Y. Chang, M. Tan, H.J. Vos, J. G. Bosch, M. Verweij, N. de Jong and M.A.P. Pertijs, "A 0.91 mW/Element Pitch-Matched Front-End ASIC with Integrated Subarray Beamforming ADC for Miniature 3D Ultrasound Probes", in *Dig. Techn. Papers ISSCC*, Feb. 2018, pp. 186-187.

C. Chen, **Z. Chen**, D. Bera, E. Noothout, Z.-Y. Chang, H.J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M.A.P. Pertijs, "A Front-End ASIC for Miniature 3-D Ultrasound Probes with In-Probe Receive Digitization," in *Proc. IEEE Ultrasonics Symp. (IUS)* (*Best student paper award*), Sept. 2017.

C. Chen, **Z. Chen**, D. Bera, S.B. Raghunathan, M. Shabanimotlagh, E. Noothout, Z.-Y. Chang, J. Ponte, C. Prins, H.J. Vos, J.G. Bosch, M.D. Verweij, N. de Jong and M.A.P. Pertijs, "A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography," in *Dig. Symp. on VLSI Circuits*, June 2016, pp. 38-39.

C. Chen, **Z. Chen**, Z.-Y. Chang and M.A.P. Pertijs, "A Compact 0.135-mW/Channel LNA Array for Piezoelectric Ultrasound Transducers," in *Proc. ESSCIRC 2015,* Sept. 2015, pp. 404-407.

M. D'Urbino, C. Chen, **Z. Chen**, Z.-Y. Chang, J. Ponte, B. Lippe and M.A.P. Pertijs, "An Element-Matched Band-Pass Delta-Sigma ADC for Ultrasound Imaging", in *IEEE Asian Solid-State Circuits Conference (A-SSCC)* (*Best student paper award*), Nov. 2017, pp. 137-140.

M. Tan, C. Chen, **Z. Chen**, J. Janjic, V. Daeichin, Z.-Y. Chang, E. Noothout, G. van Soest, M. Verweij, N. de Jong and M. A. P. Pertijs. "A Front-End ASIC with High-Voltage Transmit Switching and Receive Digitization for Forward-Looking Intravascular Ultrasound", in *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2017, pp. 1-4.

M. Shabanimotlagh, S. Raghunathan, D. Bera, **Z. Chen**, C. Chen, V. Daeichin, M.A.P. Pertijs, J.G. Bosch, N. de Jong and M.D. Verweij, "Acoustic Characterization of a 32×32 Element PZT-on-ASIC Matrix Transducer for 3D

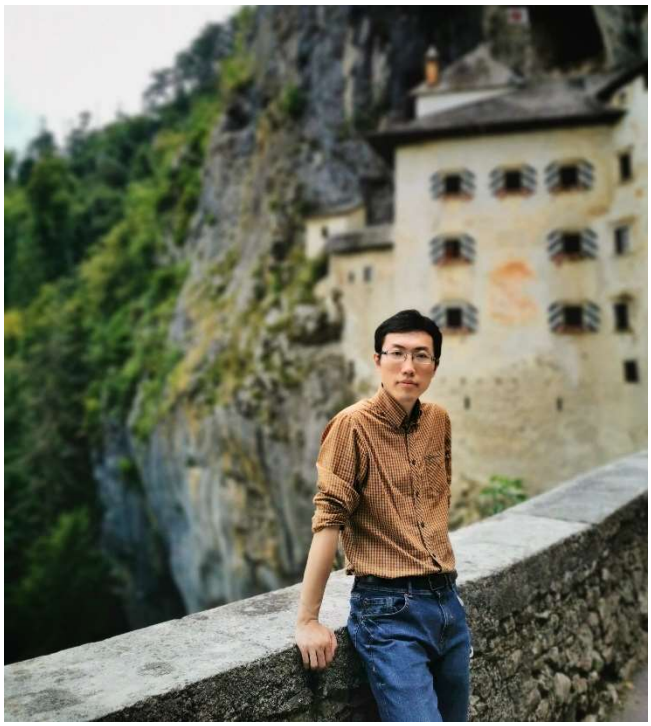
Transesophageal Echocardiography", in *Dutch Bio-Medical Engineering Conference, The Netherlands*, Jan. 2017.

D. Bera, H.J. Vos, S. Raghunathan, C. Chen, **Z. Chen**, M.D. Verweij, M.A.P. Pertijs, N. de Jong and J. Bosch, "Three-dimensional beamforming combining micro-beamformed RF datasets", in *Proc. IEEE Ultrasonics Symp. (IUS)*, Sept. 2016.

M. A. P. Pertijs, C. Chen, S. Raghunathan, Z. Yu, M. ShabaniMotlagh, **Z. Chen**, Z.-Y. Chang, E. Noothout, S. Blaak, J. Ponte, C. Prins, J.G. Bosch, M.D. Verweij and N. de Jong, "Low-power Receive Electronics for a Miniature Real-Time 3D Ultrasound Probe", in *Proc. IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, Jun. 2015.

C. Chen, **Z. Chen**, S. B. Raghunathan, D. Bera, Z. Chang, S. Blaak, C. Prins, J. Ponte, J.G. Bosch, M.D. Verweij, M.A.P. Pertijs and N. de Jong, "Low Power Receive Electronics for a Miniature Real-Time 3D Ultrasound Probe", presented in *Conference for ICT-Research in the Netherlands (ICT.OPEN)*, The Netherlands, Mar. 2015.

ABOUT THE AUTHOR



Zhao Chen was born in Shandong, China, in 1989. He received his B.Sc. degree in Microelectronics, Fudan University, Shanghai, China, in 2011 and his M.Sc. degree (with distinction) in Electrical and Electronic Engineering, Imperial College London, London, UK, in 2012. From 2012 to 2014, he worked as a research associate in Electrical and Computer Engineering department, National University of Singapore, Singapore. From 2014 to 2019, he pursued his Ph. D degree in Electronic Instrumentation Laboratory, Delft University of Technology, Delft, the Netherlands, working on analogue and mixed-signal IC design for medical ultrasound imaging. From April 2019, he became a post-doc researcher in the same laboratory in TU Delft. His research interests include analogue and mixed-signal IC design for sensor interfaces and medical imaging.

From February 2020, he started to part-timely (70%) work for Philips Research, Eindhoven, the Netherlands, where he focuses on IC and system designs for various ultrasound applications.

ACKNOWLEDGEMENT

This is the place where I would like to give my deepest gratitude to those who accompanied me in my six and a half years Ph. D adventure. The experience of working and interacting with them is the most valuable fortune for me in this adventure:

First and foremost, I would like to thank my promotor Dr. Michiel Pertijs. It is he who offered me this great opportunity to join the exciting MICA project and to be a part of the EI lab. Without him, my adventure would not have started. More importantly, Michiel shows me an excellent example of a good IC designer during my daily life working with him. It is not just his deep and unique insight in circuit designs, but also his attention to details, his analytical ability, logical and critical thinking that always amaze me. I've learned a lot from his way of thinking and solving problems, which I believe is much more valuable than the knowledge I learned from him and will benefit me in my rest life. As a promotor, Michiel is always there to give support and never be impatient to answer sometimes my "stupid" questions. I sincerely believe it is a great honour and fortune for me to work under his supervision during my Ph. D life.

Next, I would like to thank my promotor Prof. Nico de Jong. I can hardly imagine people from three different fields without sufficient knowledge of others can work together on this challenging multi-disciplinary project for so long time and achieve so much success without Nico's coordination. As the project manager, Nico was the "bad" guy who stopped the interesting but long technical discussions and made decisions to ensure the project was moving forward as scheduled; while as a promotor, he was always there to give me the required resources to work with. I'm so grateful to work in such a team led by him.

In addition, I would like to thank Dr. Hans Bosch, Dr. Martin Verweij and Dr. Rik Vos. Given the multi-disciplinary nature of MICA, their expertise in physical acoustics and ultrasound imaging allowed me to really view this project from different angles. The technical meetings with them to define the system architecture and to analyse issues we met in the experiments were the best lecture

classes for me to understand ultrasound systems and now become some of my best memories of my Ph. D life. They are excellent coaches!

I would like to express my special thanks to Chao Chen and Deep Bera, my teammates in MICA. I met Chao from day one I arrived at the Netherlands. He helped me a lot not only on catching up on the project but also on settling my life in Delft. We have closely worked together for about four years on almost everything in MICA, tape-outs, building measurement setups, experiments… And he was such a diligent, creative and passionate guy that always inspired me to work with him, discuss with him and to learn from him. It was such an exciting and memorable experience. It was a great honour to work as duo with him and to achieve so much success in MICA! My first impression to Deep was that he has the magic to talk to every strangers on the street easily. He likes talking and of course also beers. We had enjoyed so many great talks after a couple of beers during our conferences all around the world. In a chat Deep always has a sharp view on what happened in our daily life and he manages to bring this character also to his work. When I worked with Deep to address problems, he can often sharply pinpoint the key of the problem and his solid knowledge in his field always encourages me to rely on his judgement to solve the image problems we had during the experiments. A big thanks to him for all the B-mode images in our publications! Luckily for me we again become colleagues at Philips. I'm really looking forward to again teaming with him!

I would like to thank my other teammates Shreyas Raghunathan and Maysam Shabanimotlagh. In the measurement of MICA-I, we worked together day and night in the lab to try to understand our first acoustic sample and it was a mystery land to all of us at that time. I'm very happy eventually we made it, with all your helps.

I would also like to give my big thank to Zu-yao and Lukasz, the heroes behind our every prototypes. We tried to challenge them on all kinds of non-standard things, bonding, soldering, cabling, etc., but they can always give us what we want! Of course I want to thank Emile Noothout, the magician who builds transducers on the ASICs. Without him, the project concept can never land to reality.

I would like to thank my colleagues from Applied Physics and Erasmus MC: Mehdi, Verya, Fabian, Djalma, Henry and Robert. They are always willing to help me to understand an ultrasound imaging system from their expertise.

I would like to thank Fei, Ting and Chao Zhang, my old 14th floor colleagues! We have spent so many evenings together on 14th floor in EWI, with countless

talks on our projects, on families, on our future careers… All those evenings and nights are the most valuable memories of my Ph. D life!

I would like to thank all my colleagues and former colleagues in Pertijs' group: Zeyu, Peng, Qing, Mingliang, Douwe, Eunchul, Jing, Taehoon, Yannick, and Jae-sung, for all your help in the past! I'm always impressed by your talents and it's a great pleasure to work with you. I also want to say thank to all the master students who I have worked with from our group: Qilong, Yuming, Michele, Yixin and Farzad.

I would like to thank other colleagues: Long, Hui, Xiaoliang, Weihan, Yu, Guijie, Sining, Liqiang, Yiyu, Jiang, Burak, Accel and Bahman. Thanks for all the help I received from them and for all the great time we spent together.

I would like to thank our technician Ron van Puffelen, who made this excellent 3-D conceptual drawing of a miniature TEE probe and allowed me to use it in the cover of this thesis!

Of course I would like to give my big thanks to our secretary Joyce! She is always smiling and supportive to me. I'll miss the day-outs she organized.

Finally I would like to express my deep gratitude to my wife Anqi and to my parents. It is their love, trust and sacrifice supporting me to reach here. I am and will always be grateful to them.

Zhao Chen

Delft, 2020