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A 0.7-V 0.43-pJ/cycle Wakeup Timer based on a Bang-bang Digital-Intensive Frequency-Locked-Loop for IoT Applications

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***Abstract*—A 40-nm CMOS wakeup timer employing a bang-bang digital-intensive frequency-locked loop (DFLL) for Internet-of-Things (IoT) applications is presented. A self-biased $\Sigma\Delta$ Digitally Controlled Oscillator (DCO) is locked to an RC time constant via a single-bit chopped comparator and a digital loop filter. Such highly digitized architecture fully exploits the advantages of advanced CMOS processes, thus enabling operation down to 0.7 V and a small area (0.07 mm^2). Most circuitry operates at 32$\times$ lower frequency than the DCO in order to reduce the total power consumption down to 181 nW. High frequency accuracy and a 10$\times$ enhancement of long-term stability is achieved by the adoption of chopping to reduce the effect of comparator offset and 1/f noise and by the use of $\Sigma\Delta$ modulation to improve the DCO resolution. The proposed timer achieves the best energy efficiency (0.43 pJ/cycle at 417 kHz) over prior art while keeping excellent on-par long-term stability (Allan deviation floor $<$20 ppm) and temperature stability (106 ppm/^{o}C).**

***Index Terms*—Wakeup timer, Digital-intensive, Frequency locked-loop, internet of things, Low-power, Oscillator.**

I. Introduction

Remote wireless sensor nodes for the Internet of Things (IoT) rely on duty-cycling to achieve extremely low average power consumption but this requires an accurate wakeup timer. Such timer must avoid off-chip components, such as quartz crystals, and occupy minimum area to save costs and module size. It must consume ultra-low power ($<$1 μW), since it is continuously active, while operating at a low supply voltage for compatibility with a wide range of energy sources (e.g., button batteries, energy scavengers) and to simplify power management [1], [2]. Because of size and power limitations, RC oscillators are a preferred choice. However, the frequency stability of conventional RC relaxation oscillators is limited by the delay of power-hungry continuous-time comparators, which are vulnerable to PVT variations [3]–[5]. Oscillators based on frequency-locked loops (FLL) circumvent such limitations, but they heavily rely on analog-intensive circuits, which require significant power, area and a high supply voltage [6], [7]. Hence, they are not friendly to technology scaling in terms of area and required supply voltage.

Alternatively, this paper presents a wakeup timer employing a digital-intensive FLL (DFLL) architecture to fully exploit the advantages of advanced CMOS processes, thus allowing low area, low power and low supply voltage. The proposed timer achieves the best energy efficiency (0.43 pJ/cycle) at the lowest supply voltage (0.7 V) over the state of the art [2], [3], [5], [8]–[11], while maintaining excellent on-par long-term stability (Allan deviation floor below 20 ppm) in a small area (0.07 mm^2 in 40-nm CMOS). These advances are enabled by the use of a bang-bang DFLL architecture employing a chopped dynamic comparator and a low-power high-resolution self-biased $\Sigma\Delta$ digitally-controlled oscillator (DCO). The rest of the paper is organized as follows: the architecture of the proposed oscillator and the circuit implementation are introduced in section II and III, respectively; section IV describes the measurement results; conclusions are drawn in section V.

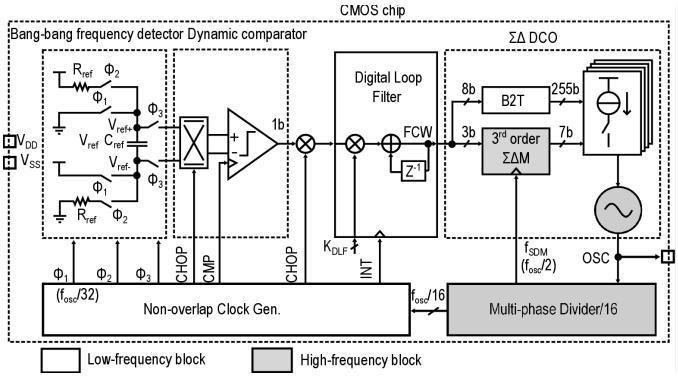

Fig. 1. Architecture of the proposed DFLL wakeup timer.

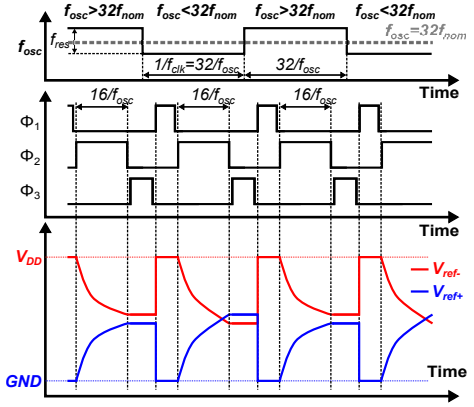

Fig. 2. Timing diagram of the DFLL and its frequency locking behavior.

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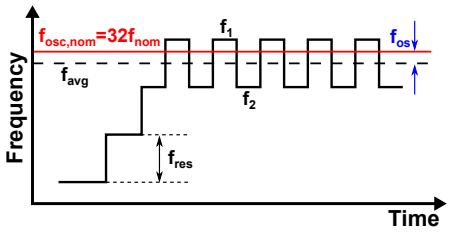


Fig. 3. Illustration of the frequency error due to the DCO finite resolution.

II. Timer Architecture

The architecture of the proposed DFLL and its timing diagram are shown in Fig. 1 and Fig. 2, respectively. A differential frequency detector (FD) is driven at a clock frequency f_{clk}=f_{osc}/32 derived from the output frequency of the DCO f_{osc}. The capacitor C_{ref} is charged to $V_{ref} = V_{ref+} - V_{ref-} = V_{DD}$ during phase Φ_1 and discharged via resistors R_{ref} during phase Φ_2 [7]. At the end of Φ_2, the output of the FD $V_{ref} = V_{DD}[1 - 2e^{-1/(4R_{ref}C_{ref}f_{clk})}]$ indicates the relation between the clock frequency f_{clk} and the FD nominal frequency $f_{nom} = 1/(4R_{ref}C_{ref}\ln 2)$. For example, V_{ref} will be positive if $f_{clk} < f_{nom}$ and negative otherwise (Fig. 2). The differential circuit topology of the FD ensures a high immunity against supply and ground noise. The sign of V_{ref} is detected by a dynamic comparator and is further processed by a digital loop filter driving the DCO in a negative feedback to ensure that, on average, $V_{ref} = 0$ and, hence, $f_{osc}/32 = f_{nom}$.

The only analog components in the DFLL are a switching passive RC network for the FD, a comparator and a DCO. As shown in Section III, such analog circuits can be implemented using switches and inverter-based structures, so that they can be easily integrated in a nanometer CMOS process with a low power consumption, a low supply voltage and a small area.

III. Circuit Implementation

The DFLL output frequency is set to $f_{osc,nom} = 32f_{nom} = 8/(R_{ref}C_{ref}\ln 2) \approx 417$ kHz with $R_{ref} = 5.5$ MΩ and $C_{ref} = 5$ pF chosen for minimum die area occupation. The resistor R_{ref} is implemented by a series combination of non-silicided p-poly and n-poly resistors with opposite temperature coefficients (TC) to provide a first-order compensation of the TC of f_{osc}. Both R_{ref} and C_{ref} are implemented as switchable arrays that can be digitally tuned to compensate for process spread.

The DCO output frequency is fed into a multi-phase clock divider to provide all the clocks required in this self-clocked FLL (Fig. 2). The large adopted frequency division factor (32×) is advantageous: Φ_2 and, consequently, the output frequency (f_{osc}) can be accurately set thanks to the availability of multiple phases; moreover, most of the circuit in Fig. 1 runs at a much lower frequency, thus saving power. For example, a fixed and relatively long comparator delay (≈ 4.8 μs) can be allowed compared to the ∼ns delay of continuous-time comparators [3], thus enabling the comparator to be optimized for power instead of speed. A longer comparator delay is allowed in this architecture, since f_{osc} only depends on the duration of Φ_2. The main drawback of running the loop filter at a lower frequency is an increase in the loop settling time.

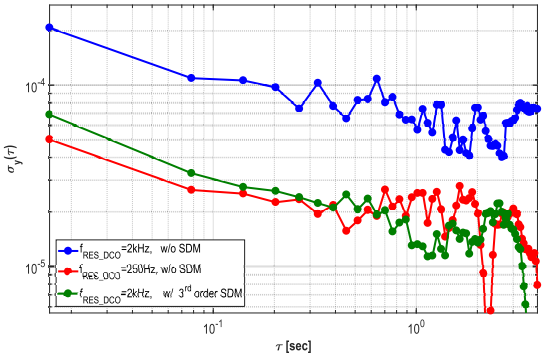


Fig. 4. Impact of DCO resolution on the Allan deviation.

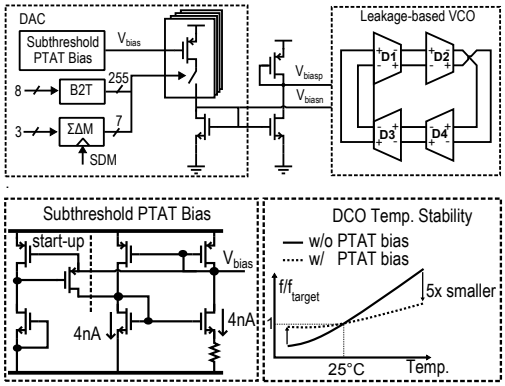


Fig. 5. Implementation of the self-biased ΣΔ DCO.

Unlike traditional RC relaxation oscillators requiring continuous-time comparators, the comparator is implemented as a dynamic StrongARM latch. However, the offset of the comparator may degrade the accuracy of the wakeup timer and introduce a temperature-dependent frequency error, while its flicker noise directly affects the long-term stability of the timer. To suppress the effect of both offset and flicker noise, the dynamic comparator is chopped at a frequency of $f_{osc}/256$ by means of an analog and a digital modulator at the comparator input and output, respectively.

The digital loop filter (Fig. 1) comprises a configurable gain (K_{DLF} in Fig. 1) and a digital accumulator which, thanks to the comparator output being single-bit, are implemented in a compact and low-power form by a bit-shifter and a up/down counter, respectively. By changing the digital filter gain, the overall bandwidth of the DFLL can be easily configured and more reliably predicted than in conventional analog FLL's, which are more vulnerable to PVT variations. This feature allows the DFLL to flexibly trade-off bandwidth and noise for different IoT scenarios. For example, applications dealing with fast temperature or supply changes prefer a higher loop gain, which results in wider loop bandwidth; instead, applications requiring a lower period jitter need a lower loop gain to minimize the DCO step that would otherwise show as additional jitter.

Due to the bang-bang operation of the DFLL, the DCO output frequency will continuously toggle in the steady state.

If the random noise in the loop is neglected, the DCO control word will toggle between two consecutive values corresponding to the frequencies f_1 and f_2 that straddle f_{nom}, as shown in Fig. 3. Since such locking condition is satisfied for any f_{nom} between f_1 and f_2, this would result in a worst-case frequency offset $|f_{os}| < \frac{f_1-f_2}{2} = \frac{f_{res}}{2}$, where f_{res} is the DCO resolution. Although this source of inaccuracy is partially mitigated by the dithering effect of random noise, care has been taken to maximize the DCO resolution not to degrade the timer accuracy. Moreover, although the DCO noise is high-pass filtered by the loop and hence does not affect the timer long-term stability, the long-term stability is also affected by the DCO resolution. Fig. 4 shows the simulated Allan deviation for different DCO resolutions, thus demonstrating that a lower f_{res} leads to a lower Allan deviation floor, i.e. a better long-term stability. This effect can be intuitively explained as follows. A higher DCO resolution causes less quantization noise to be injected in the loop. In the equivalent linear model of the loop, this directly affects the equivalent gain of the single-bit comparator. A decrease in noise implies a smaller signal at the comparator input and, hence, a higher equivalent comparator gain. The higher comparator gain reduces the output jitter due to noise in both the comparator and the DCO. Consequently, $f_{res} = 250$ Hz was chosen for the DCO. Meanwhile, sufficient tuning range for the DCO is required to tackle its frequency drift over PVT. Therefore, a high-resolution DCO is required, which is challenging with the very limited power budget in the wakeup timer ($\ll 1\mu$W). To address this challenge, two techniques are employed (Fig. 5): temperature compensation facilitated by a local proportional-to-absolute-temperature (PTAT) current bias, and a $\Sigma\Delta$ DAC to improve the DCO resolution. A 4-stage differential ring oscillator employing an ultra-low-power leakage-based delay cell is adopted to keep the oscillator power below 60 nW (Fig. 5) [8]. A subthreshold PTAT current bias is used to lower the DCO temperature drift while exploiting a nW oscillator topology. This effectively reduces the oscillator temperature drift by 5×, thus relaxing the DAC design. The self-clocked $\Sigma\Delta$ DAC consists of 255+7=262 unary-coded elements driven by an 8-b integer thermometric DAC clocked at $f_{osc}/32$ and a 3-b fractional DAC processed by a 3rd-order digital $\Sigma\Delta$ modulator. Thanks to the feedback loop, no strict linearity requirements are required for the DAC other than the monotonicity necessary for loop stability. Monotonicity is ensured by the unary nature of the DAC. The $\Sigma\Delta$ modulator is clocked at $f_{osc}/2$ (16× oversampling ratio) to further improve the DCO resolution from 2 kHz to below 250 Hz. The enhancement in resolution given by the $\Sigma\Delta$ operation improves the Allan deviation floor in the same way as a standard DCO with the same equivalent resolution, as illustrated in Fig. 4.

IV. Measurements

The 0.07-mm^2 wakeup timer was fabricated in a standard TSMC 1P5M 40-nm CMOS process (Fig. 6) and draws 259 nA from a single 0.7-V supply (power breakdown: 32% FD/comparator, 38% digital, 30% DCO). This corresponds to a state-of-the-art energy efficiency 0.43 pJ/cycle.

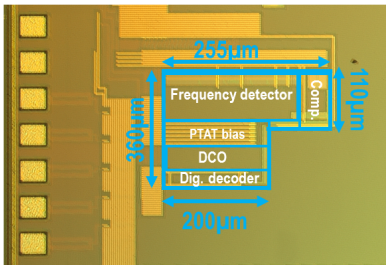
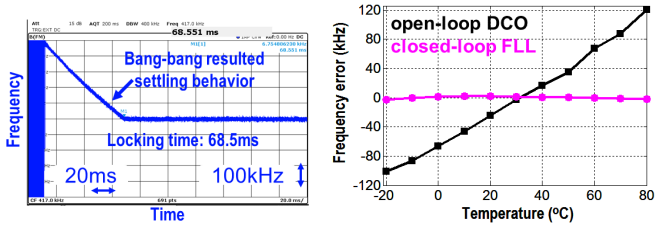


Fig. 6. Chip micrograph.



(a) (b)

Fig. 7. Measured DFLL settling (KDLF=1/8) (a) and open/closed loop performance (b).

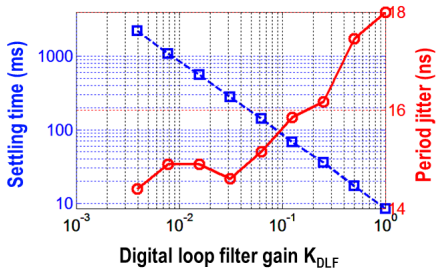
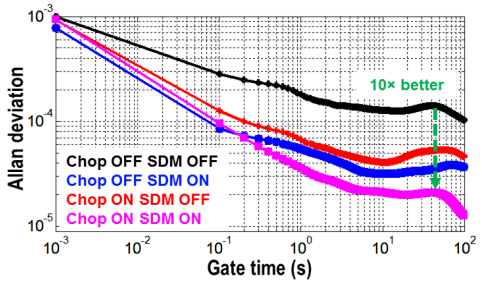


Fig. 8. Measured settling time and period jitter versus loop gain K_{DLF}.

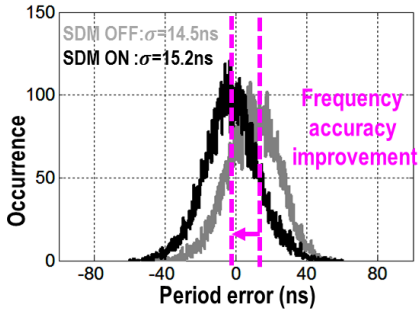
Once enabled, due to the bang-bang operation, the frequency of the DFLL increments or decrements towards the steady-state frequency (Fig. 7(a)). The locking of the FLL can be observed in Fig. 7(a), in which the DCO output frequency in open-loop and closed loop configuration are compared. Although long-term stability is one of the critical performance for wakeup timers, it is interesting to observe that, thanks to the digital-intensive nature of the architecture, the settling time can be easily configured and traded off for jitter if required by the target application. This can be accomplished by tuning the digital loop-filter gain K_{DLF} (Fig. 8). The period jitter is 15.2 ns$_{rms}$ and slightly improves (14.5 ns$_{rms}$) disabling the $\Sigma\Delta$ modulation and hence its quantization noise. Thanks to the self-clocked $\Sigma\Delta$ and the chopped comparator, the long-term stability (Allan deviation floor) improves by 10× down to 12 ppm beyond 100s integration time (Fig. 9(a)). The long-term stability is relatively stable against temperature and supply voltage variations (Fig. 10). The temperature sensitivity of the output frequency improves from 134 ppm/°C to 106 ppm/°C when activating the chopping and the $\Sigma\Delta$ modulation, thanks to smaller errors due to a smaller DCO step and the mitigation of comparators offset (Fig. 11). The timer operates over the 0.65-0.8-V supply range with a deviation of $\pm 0.6\%$ (Fig. 11).

Although such temperature and supply sensitivity are sufficient for typical IoT applications and are on par with state-of-the-art designs (see Table I), simulations shows that they are limited by the on-resistance of the FD switches at such low supply and can be improved by proper re-design.

The performance is summarized and compared with other sub-μW state-of-the-art designs in Table I. Being integrated in the most advanced CMOS process (40 nm) among nW timers to show its scaling advantages, the presented timer achieves the best power efficiency at the lowest operating supply voltage among state-of-the-art sub-μW timing references.



(a)



(b)

Fig. 9. Measured long-term stability (a) and period jitter (b).

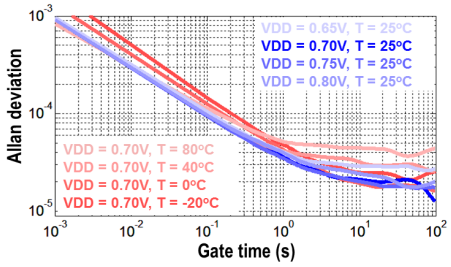


Fig. 10. Measured long-term stability.

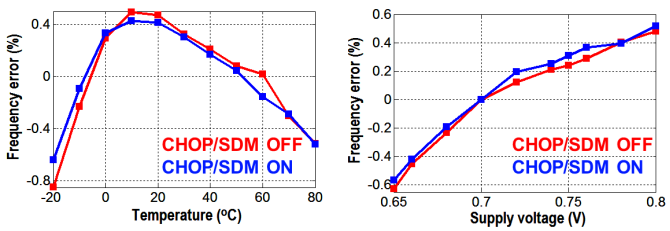


Fig. 11. Measured frequency stability.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	[5] ISSCC'17	[3] JSSC'16	[8] ISSCC'16	[2] JSSC'16	[10] JSSC'16	[10] ISSCC'14	[11] VLSI'12
Architecture	**DFLL**	Relaxation oscillator	Relaxation oscillator	Analog FLL	Analog FLL	Capacitive discharging	RC oscillator	Relaxation oscillator
Process (nm)	**40**	65	65	180	180	250	65	90
Frequency (Hz)	**417k**	1350k	18.5k	3K	70.4k	6.4k	33k	100k
VDD (V)	**0.7**	1.4	1	0.85 - 1.4	1.3	0.8	1.15 - 1.45	0.8
Power (nW)	**181**	920	130	4.7	110	75.6	190	280
Freq. Var. to VDD (%)	**±0.6 @ 0.65–0.8V**	±0.54@ 0.9–2.0V	<±0.25@ 0.95-1.05V	±0.14@ 0.85-1.4V	±0.23@ 1.2-1.8V	±0.27@ 0.6-0.9V	<±0.14@ 1.15-1.45V	±0.3@ 0.5–1.0V
TC (ppm/°C)	**106 @ -20-80°C**	96@ 0-145 °C	85@ -40-90 °C	13.8@ -25-85 °C	34.3@ -40-80 °C	144@ -20-80°C	38@ -20-90 °C	105@ -40-90°C
Allan Deviation Floor (ppm)	12 (>100s)	-	20(>100s)	63(>100s)	7(>12s)	60 (>100s)	4 (>2s)	-
Energy/Cycle (pJ/Cycle)	**0.43**	0.68	6.5	1.6	1.56	11.8	5.8	2.8
Area (mm^2)	**0.07**	0.005	0.032	0.5	0.26	1.08	0.015	0.12

V. Conclusion

A ultra-low-power wakeup timer employing a bang-bang digital-intensive frequency-locked loop has been integrated in a 40-nm CMOS process. Thanks to the highly digital architecture, this timer achieves the best power efficiency (0.43 pJ/cycle) at an extremely low-supply voltage and in a low area, while keeping on-par long-term stability and on-par stability over supply and temperature variations. This demonstrates that the proposed architecture is suitable for IoT applications requiring accurate ultra-low-power timers integrated in advanced CMOS processes.

References

[1] F. Sebastiano, et al., "A 65-nm CMOS Temperature-Compensated Mobility-Based Frequency Reference for Wireless Sensor Networks," *IEEE J. Solid-State Circuits,* vol. 46, no. 7, pp. 1544-1552. Jul. 2011.

[2] M. Choi, et al., "A 110nW Resistive Frequency Locked On-Chip Oscillator with 34.3ppm/°C Temperature Stability for System-on-Chip Designs," *IEEE J. Solid-State Circuits,* vol. 51, no. 9, pp. 2106-2118. Jun. 2016.

[3] A. Paidimarri, et al., "An RC Oscillator with Comparator Offset Cancellation," *IEEE J. Solid-State Circuits,* vol. 51, no. 8, pp. 1866-1877. Aug. 2016.

[4] J. Koo, et al., "A Quadrature Relaxation Oscillator with a Process-Induced Frequency-Error Compensation Loop," *IEEE ISSCC Dig. Tech. Papers,* pp. 94-95. Feb. 2017.

[5] A. Savanth, et al., "A 0.68nW/kHz Supply-Independent Relaxation Oscillator with 0.49%/V and 96ppm/°C Stability," *IEEE ISSCC,* pp. 96-97. Feb. 2017.

[6] S. M. Kashmiri, K. Souri, and K. A. A. Makinwa, "A scaled thermal-diffusivity-based 16 MHz frequency reference in 0.16 m CMOS," *IEEE J. Solid-State Circuits,* vol. 47, no. 7, pp. 1535-1545. Jul. 2012.

[7] J. Lee, P. Park, S. Cho, and M. Je, "A 4.7MHz 53μW Fully Differential CMOS Reference Clock Oscillator with 22dB Worst-Case PSNR for Miniaturized SoCs," *IEEE ISSCC,* pp. 106-107. Feb. 2015.

[8] T. Jang, et al., "A 4.7nW 13.8ppm/°C Self-Biased Wakeup Timer Using a Switched-Resistor Scheme," *IEEE ISSCC,* pp. 102-103. Feb. 2016.

[9] H. Wang and P. Mercier, "A Reference-Free Capacitive-Discharging Oscillator Architecture Consuming 44.4pW/75.6nW at 2.8Hz/6.4kHz," *IEEE J. Solid-State Circuits,* vol. 51, no. 6, pp. 1423-1435. Jun. 2016.

[10] D. Griffith, P. T. Roine, J. Murdock, and R. Smith, "A 190nW 33kHz RC oscillator with±0.21% temperature stability and 4ppm long-term stability," *IEEE ISSCC Dig. Tech. Papers,* pp. 300-301. Feb. 2014.

[11] T. Tokairin, et al., "A 280nW, 100kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme," *VLSI Symposium,* pp. 16-17. Jun. 2012.