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A New Single-Phase High Step-Up Active-Switched Quasi Z-Source NNPC Inverter With Common Ground Feature

MILAD SHAMOUEI-MILAN [1], REZA ASGARNIA [1], MILAD GHAVIPANJEH MARANGALU [2,3], KOUROSH KHALAJ MONFARED [4], YOUSEF NEYSHABOURI [5], AND HANI VAHEDI [6]

[1]Faculty of Electrical and Computer Engineering, SBU, Tehran 19839-69411, Iran
[2]Department of Information Engineering, Computer Science and Mathematics, University of L'Aquila, 67100 L'Aquila, Italy
[3]Faculty of Electrical and Computer Engineering, Tabriz University, Tabriz 51666, Iran
[4]School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Tehran 14155-6619, Iran
[5]Faculty of Electrical and Computer Engineering, Urmia University, Urmia 57153, Iran
[6]Delft University of Technology, 2628CD Delft, Netherlands

CORRESPONDING AUTHOR: MILAD GHAVIPANJEH MARANGALU (e-mail: m.ghavipanjeh@tabrizu.ac.ir)

ABSTRACT Quasi-Z source (qZS) multilevel inverters have become popular in sustainable energy systems, particularly in photovoltaic (PV) systems. This study proposes a qZS five-level nested neutral point clamped (5L-NNPC) inverter, benefiting from continuous input current, high voltage gain, and insignificant voltage stress across semiconductors. The proposed topology provides a common ground between the input sources and the inverter's DC link, thus entirely eliminating leakage current, making it a suitable candidate for PV applications. Moreover, model predictive control (MPC) is employed to regulate the voltages of flying capacitors and the output current of the 5L-NNPC inverter. The study also includes analyses of steady-state performance, circuit design, efficiency, and control considerations. Finally, experimental results are presented to validate the converter's performance.

INDEX TERMS Five-level nested neutral point clamped, model predictive control, quasi Z-source (qZS).

I. INTRODUCTION

The effects of global warming have been exacerbated in recent years by the growing use of fossil fuels. To mitigate the consequences of this crisis, renewable energy sources such as PV systems have been offered. Meanwhile, in PV systems, the generated DC voltage is low. Therefore, to provide the desired voltage magnitude, high step-up multilevel inverters are required [1], [2], [3], [4]. In medium-voltage and high-power applications, multilevel inverters are often utilized because of the numerous advantages they have over two-level inverters such as lower total harmonic distortion (THD), higher power quality, and lower voltage stress on semiconductors [5], [6]. Therefore, multilevel inverters have gained attention among both researchers and industries. Multilevel inverters can be categorized into three main groups: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC) topologies [7], [8], [9].

These kinds of multilevel topologies have been utilized in numerous applications, including PV systems and uninterruptible power supplies [10], [11]. However, the maximum AC side voltage in the conventional multilevel inverters is limited. For instance, the peak AC output voltage of an NPC inverter cannot exceed half of the DC input voltage. In the CHB inverter, the peak AC output voltage is approximately equal to the sum of the DC source voltages. To generate the AC output voltage and provide the required voltage boosting factor, an extra DC-DC boost stage should be used [12], [13]. Using an extra boost stage leads to not only an increase in cost and size but also a decrease in the total efficiency of the system. The Z-source inverter (ZSI) and qZSI have been presented to address the mentioned drawbacks of conventional multilevel inverters [14], [15]. These topologies accomplish buck-boost voltage operation with a single-stage power conversion. Using the shoot-through state, the ZSI/qZSI can

increase the DC-link voltage. As a result, these topologies do not need an additional energy conversion stage, improving the system reliability. To apply the benefits of the qZSI to multilevel inverters, some topologies have been proposed in [16], [17].

The Authors in [18] and [19] utilize the coupled inductor approach, providing a high voltage gain. Meanwhile, applying this method may lead to a voltage spike across the semiconductors, reducing their lifetime. In [18], the discontinuous input current leads to an increase in the input source stress. The topology presented in [19] employs three active power switches, requiring a complex control system. The converter in [20] utilizes a switched inductor. Nevertheless, the common ground between the input source and output DC links has been eliminated. Additionally, the presence of numerous passive components in this converter increases weight, size, and conduction losses. A novel quasi-switched-capacitor-inductor Z-source structure is suggested in [21]. However, the current stress of the switches in this converter is significantly high. The Z-source-based topologies have a discontinuous input current and no common ground. This converter also has a high startup current, which affects the lifetime of the circuit elements [22]. Quasi-z-source topologies have been suggested as a solution to address the challenges of z-source structures. These kinds of topologies have some features such as high voltage gain and continuous input current [23], [24], [25]. The high voltage stress on power semiconductors in [23] necessitates using switches and diodes with a high voltage rate. The authors in [24] propose a new topology with numerous diodes, which increases power losses and the size of the converter while decreasing its efficiency and power density. In [25], the proposed structure benefits from using active switches. However, employing four inductors reduces the converter's efficiency and power density and imposes high voltage stress on the diodes. Although [26] has a continuous input current, its input current has a significant ripple and cannot be a proper choice for PV applications. [27] has a low voltage gain and must be added to the transformer's number of turns to provide a suitable voltage gain during low-duty cycles. A new three-phase NPC-based converter has been suggested in [28]. This topology has significant features, including reduced power devices compared to the alternative structures with comparable operations.

On the other hand, from the control and modulation viewpoint, conventional PWM-based modulation techniques are widely used in multilevel topologies to control and balance the flying capacitors and neutral point voltages. Meanwhile, the 5L-NNPC inverter lacks sufficient redundant modes, reducing the use of those techniques. MPC methods have been studied for high-power medium-voltage applications. The MPC-based solutions offer some advantages, such as achieving a wide variety of control objectives and mitigating the requirement of modulators and PI controllers while improving the capability of dynamic responsiveness [29], [30], [31]. In [32], a new boosting structure with continuous input current and insignificant voltage stress on power switches and diodes, tied to a single-phase 5L-NNPC inverter, is proposed. Fig. 1 depicts the general circuit of the suggested structure. The input DC source is amplified and fed into the NNPC structure using a qZS network. This converter offers low voltage stress and allows the utilization of semiconductors with small parasitic components, thus reducing the converter's cost and enhancing efficiency. Also, the MPC method is expanded in this paper to control the single-phase 5L-NNPC inverter.

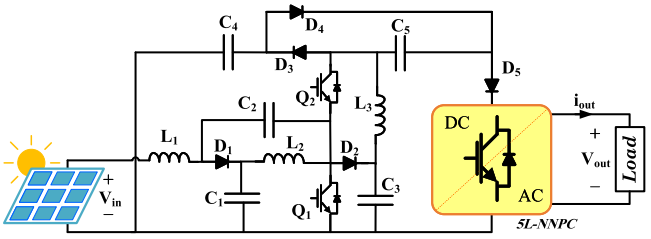

FIGURE 1. Equivalent circuit of a single phase high gain active-switched qzs NNPC inverter.

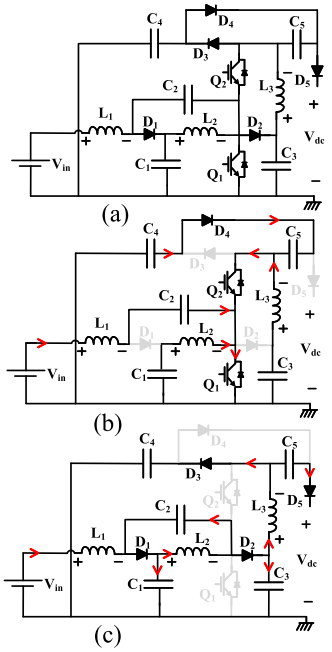

FIGURE 2. (a) Boosting topology, (b) mode I, and (c) mode II.

II. PROPOSED DC-DC HIGH STEP-UP CONVERTER

Fig. 2(a) shows the proposed boosting structure. Increasing the input voltage to the desired level is the main goal of this converter. In this structure, two switches (Q_1, Q_2), five diodes (D_1, D_2, D_3, D_4, D_5), three inductors (L_1, L_2, L_3), and five capacitors (C_1, C_2, C_3, C_4, C_5) are employed. The input current is continuous because of a series inductor with the input source. To simplify the analysis, it is assumed that all capacitors are sufficiently large to maintain a constant steady-state voltage. Additionally, the converter is considered to operate in continuous current mode (CCM).

A. OPERATION MODES

The switches are turned OFF/ON at the same time to simplify the drive circuit. Hence, two operating modes are predicted.

MODE I: Fig. 2(b) illustrates mode I. Both switches are turned ON during this mode. Inductors become magnetized due to the presence of a positive voltage across them. As a result, the current flowing through the inductors rises linearly. C_2 and the input source charge L_1 through the first switch, and the voltages of C_1 and C_3 magnetize L_2 and L_3, respectively. All diodes, except D_4, are in a reverse bias state. As a result of deactivating D_5, the inverter is supplied by the DC bus capacitors. The voltage of inductors is represented in (1).

$$\begin{cases} V_{L_1} = V_{in} + V_{C_2} \\ V_{L_2} = V_{C_1} \\ V_{L_3} = V_{C_3} \end{cases} \tag{1}$$

MODE II: Fig. 2(c) illustrates the second mode. This mode is denoted when the switches are OFF. The sum of the input source and C_1 voltages discharge L_1. Furthermore, while the negative voltage of C_3 demagnetizes L_2, the voltage summation of C_3 and C_4 demagnetizes L_3. As a result, the inductors' current decreases proportionally regarding the negative voltage across them. Except for D_2, all diodes are active in this mode. Therefore, the voltage of the DC bus is equal to the combined voltage of capacitors C_4 and C_5. The voltages across inductors are indicated by (2).

$$\begin{cases} V_{L_1} = V_{in} - V_{C_1} \\ V_{L_2} = V_{C_1} - V_{C_3} \\ V_{L_3} = V_{C_3} - V_{C_4} \end{cases} \tag{2}$$

B. BOOSTING FACTOR

The capacitors' voltages are calculated by using the volt-second balance and KVL. To prevent saturation, the average voltage across the inductors should be zero over the entire switching period, according to the volt-second strategy. The V_{dc} equals the sum of C_4 and C_5 voltages. The capacitors and V_{dc} voltages are obtained by (3).

$$\begin{cases} V_{C_1} = \dfrac{1-D}{1-2D} V_{in}, \; V_{C_2} = \dfrac{DV_{in}}{1-2D} \\ V_{C_3} = \dfrac{V_{in}}{1-2D}, \; V_{C_4} = \dfrac{V_{in}}{(1-2D)(1-D)} \\ V_{C_5} = \dfrac{V_{in}}{(1-2D)(1-D)}, V_{dc} = V_{C_4} + V_{C_5} \end{cases} \tag{3}$$

By applying the voltages of the capacitors and V_{dc} equation, the boosting factor (B) can be expressed by (4).

$$B = \frac{V_{dc}}{V_{in}} = \frac{2}{(1-2D)(1-D)} \tag{4}$$

C. VOLTAGE AND CURRENT STRESSES

The voltage stress across the power switches and diodes plays a crucial role in choosing the appropriate components. When the semiconductors are OFF, the voltage stress across them can be expressed by (5).

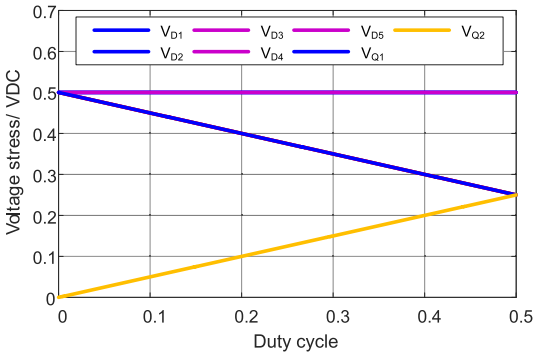

FIGURE 3. Normalized voltage stress across semiconductors.

$$\begin{cases} V_{D_1} = V_{D_2} = V_{Q_1} = \dfrac{1-D}{2} V_{dc} \\ V_{D_3} = V_{D_4} = V_{D_5} = \dfrac{V_{dc}}{2}, \; V_{Q_2} = \dfrac{D}{2} V_{dc} \end{cases} \tag{5}$$

Fig. 3 illustrates the normalized voltage stress across power switches and diodes. Regardless of duty cycle value, the voltage stress of V_{D3}, V_{D4}, and V_{D5} are equal to half of the V_{dc}. In addition, although the voltage stress across the second switch will be increased as the duty cycle percentage exceeds, this value is less than one-fourth of the V_{dc} for all duty cycle ranges. Also, when the duty cycle increases from 0 to 0.5, the normalized voltage stress across the first switch reduces from 0.5 to 0.25.

The voltage stress across switches and diodes is always limited to a maximum of half the output voltage. Hence, it is feasible to employ semiconductors with low voltage ratings in high voltage applications, permitting the use of switches and diodes with low ON-resistance and forward voltage, respectively. Notably, the suggested converter reduces total power losses and overall cost by using the power switches and diodes mentioned above.

Regarding the ampere-second balance, the average current flowing through capacitors throughout a switching period is zero. The average current of the inductor can be determined by applying the ampere-second balance and KCL as:

$$\begin{cases} I_{L_1} = \dfrac{2I_{dc}}{(1-D)(1-2D)} \\ I_{L_2} = \dfrac{2I_{dc}}{(1-D)(1-2D)} \\ I_{L_3} = \dfrac{2I_{dc}}{1-D} \end{cases} \tag{6}$$

The average current that flows through power switches and diodes can be calculated during the activation state. The current stresses of switches and diodes are indicated as:

$$\begin{cases} I_{D_1} = \dfrac{2I_{dc}}{(1-D)(1-2D)}, I_{D_2} = \dfrac{2I_{dc}}{1-D} \\ I_{D_3} = I_{D_4} = I_{D_5} = I_{dc} \\ I_{Q_1} = \dfrac{(1+3D)I_{dc}}{(1-D)(1-2D)}, I_{Q_2} = \dfrac{(1-D-2D^2)I_{dc}}{(1-D)(1-2D)} \end{cases} \tag{7}$$

It should be noted that the average passing current through D_3, D_4, and D_5 is I_{dc}, regardless of the duty cycle percentage. Because of the low current passing through the mentioned diodes, the proposed converter can utilize diodes with a low current rate, which increases efficiency and decreases costs.

The root mean square (RMS) current of capacitors is indicated below.

$$\begin{cases} I_{C_1,RMS} = I_{C_2,RMS} = \dfrac{2I_{dc}}{(1-D)(1-2D)}\sqrt{\dfrac{D}{1-D}} \\ I_{C_3,RMS} = \dfrac{2I_{dc}}{(1-D)}\sqrt{\dfrac{D}{1-D}} \\ I_{C_4,RMS} = I_{C_5,RMS} = I_{dc}\sqrt{\dfrac{1-D}{D}} \end{cases} \tag{8}$$

D. POWER LOSS ANALYSIS

Parasitic components in the converter result in losses and efficiency reduction. Converter losses can be classified into two main types: conduction loss and switching loss. Conduction loss in the converter is computed as follows.

$$P_L = \frac{4{I_{dc}}^2}{(1-D)^2}\left(\frac{r_{L_1}}{(1-2D)^2} + \frac{r_{L_2}}{(1-2D)^2} + r_{L_3}\right) \tag{9}$$

$$P_D = V_f I_{dc}\frac{6D^2 - 13D + 7}{(1-D)(1-2D)} \tag{10}$$

$$P_{Q,conduction} = \frac{{I_{dc}}^2}{(1-D)^2(1-2D)^2}(r_{ds_1}(1+3D)^2 + r_{ds_2}(1-D-2D^2)) \tag{11}$$

$$P_C = ESR_1{I_{C_1,RMS}}^2 + ESR_2{I_{C_2,RMS}}^2 + ESR_3{I_{C_3,RMS}}^2 + ESR_4{I_{C_4,RMS}}^2 + ESR_5{I_{C_5,RMS}}^2 \tag{12}$$

where r_L, V_f, r_{ds}, and ESR are the inductors resistance, the forward voltage of diodes, the ON-resistance of switches, and the equivalent series resistance of capacitors, respectively. Notably, the voltage drop of diodes is considered equal to simplify calculations. The switching loss of switches is calculated in (13).

$$P_{Q,\text{Switching}} = \frac{V_{dc}I_{dc}f(t_{on}+t_{off})(1+3D-4D^2-2D^3)}{4(1-D)(1-2D)} \tag{13}$$

where t_{on} represents turn-ON time and t_{off} indicates turn-OFF time. Fig. 4(a) shows the loss breakdown of the proposed converter. It is observable that the most significant part of the loss is related to the diodes, whereas the capacitors contribute the most negligible part.

By employing power loss equations caused by different components, the converter efficiency can be calculated by (14).

$$\text{Efficiency} = \frac{P_{in} - (P_L + P_D + P_C + P_{Q,Conduction} + P_{Q,Switching})}{P_{in}} \tag{14}$$

Fig. 4(b) shows the experimental efficiency curves of the proposed converter versus output power. Regarding this figure, the maximum value of the experimental efficiency of the proposed converter at 100 W output power is 94.01 %.

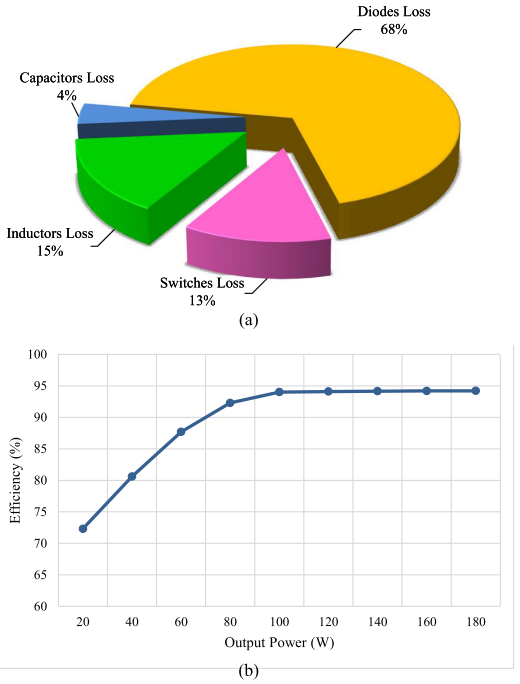

FIGURE 4. (a) The loss breakdown of the proposed converter and (b) the experimental efficiency curve of the proposed converter versus output power.

E. COMPONENTS CONSIDERATION

The voltage of inductors and current of capacitors are obtained by (15).

$$\begin{cases} V_L = L\dfrac{dI_L}{dt} = L\dfrac{\Delta I_L}{DT} \\ I_c = C\dfrac{dV_c}{dt} = C\dfrac{\Delta V_c}{DT} \end{cases} \tag{15}$$

where V_L and I_c denote voltage across inductors and flowing current through capacitors, respectively. Also, ΔI_L and ΔV_c represent inductor current ripple, and voltage ripple across capacitors, respectively. The value of inductors and capacitors can be calculated as (16).

$$\begin{cases} L_1 = \dfrac{(1-2D)V_{dc}D}{2f\Delta I_{L_1}},\ L_2 = \dfrac{D(1-D)^2V_{dc}}{2f\Delta I_{L_2}} \\ L_3 = \dfrac{D(1-D)V_{dc}}{2f\Delta I_{L_3}},\ C_3 = \dfrac{4DV_{in}}{(1-D)^2(1-2D)fR_o\Delta V_C} \\ C_1 = C_2 = \dfrac{4DV_{in}}{(1-D)^2(1-2D)^2R_of\Delta V_C} \\ C_4 = C_5 = \dfrac{2DV_{in}}{(1-D)(1-2D)fR_o\Delta V_C} \end{cases} \tag{16}$$

The discontinuous current mode (DCM) provides a higher voltage gain and removes the diode's reverse recovery challenge. However, the components' peak current rises because of the mitigation in conducting time. The critical values of inductors in the boundary mode between DCM and CCM can

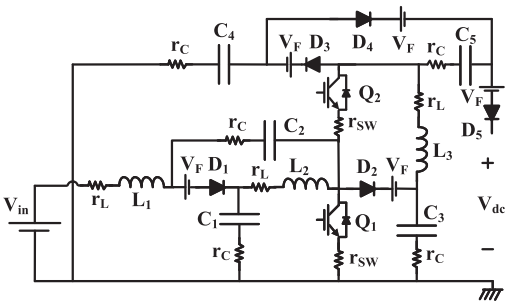

FIGURE 5. The non-ideal components of the converter.

be expressed by (17).

$$\begin{cases} L_{1,critical} = \dfrac{(1-2D)^2(1-D)DR_o}{8f} \\ L_{2,critical} = \dfrac{(1-2D)^3(1-D)DR_o}{8f} \\ L_{3,critical} = \dfrac{(1-D)^2DR_o}{8f} \end{cases} \tag{17}$$

F. NON-IDEAL BOOST FACTOR

Since the duty cycle is nearly equal to 0.5, the ideal boost factor is approaching infinity. However, in non-ideal circumstances, these parasitic components avert the attainment of an infinite voltage gain. Fig. 5 shows the non-ideal components in the circuit. Using volt-second balance and KVL results in the non-ideal voltage gain as (18).

$$B = \frac{\dfrac{2}{(1-D)(1-2D)} - V_{FD}}{1 + V_{LD} + V_{QD} + V_{CD}} \tag{18}$$

where V_{LD}, V_{QD}, V_{CD}, and V_{FD} denote the voltage drop resulting from the parasitic elements of inductors, switches, capacitors, and diodes, respectively. The influence of parasitic elements is calculated as follows:

$$V_{FD} = \frac{V_f}{V_{in}} \frac{4D^2 - 8D + 4}{(1-2D)(1-D)} \tag{19}$$

$$V_{LD} = \frac{r_L}{R_o} \frac{16D^2 - 16D + 12}{(1-D)^2(1-2D)^2} \tag{20}$$

$$V_{QD} = \frac{r_{ds}}{R_o} \frac{8D^4 - 4D^3 - 2D^3 - 2D^2 + 4}{(1-D)^2(1-2D)^2} \tag{21}$$

$$V_{CD} = \frac{ESR}{R_o} \frac{8D^4 - 2D^3 - 10D^2 + 4}{(1-D)(1-2D)} \tag{22}$$

Fig. 6 shows the non-ideal and ideal boosting factors. The curves behave identically for duty cycles less than 0.3, and the difference is negligible. Meanwhile, the difference between curves becomes more obvious when the duty cycle exceeds 0.3. When the duty cycle passes 0.45, the impact of the non-ideal behavior of components intensifies. As a result, the non-ideal boosting factor is reduced dramatically and achieves zero at a duty cycle of 0.5. Also, as the duty cycle is near 0.5,

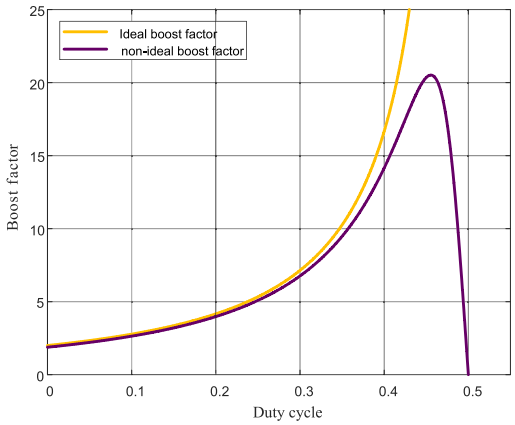

FIGURE 6. Waveforms of ideal and non-ideal boost factor.

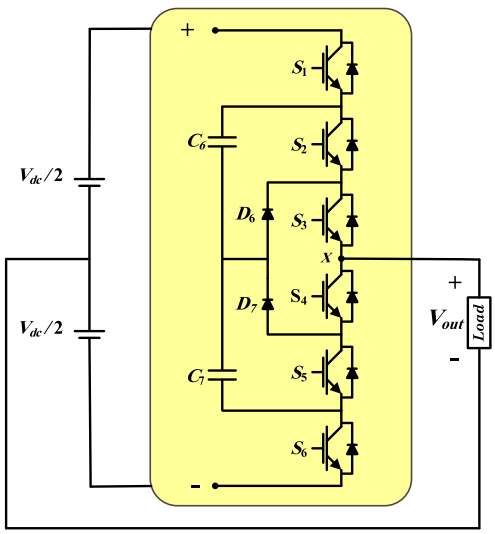

FIGURE 7. Five-level NNPC topology.

the ideal boosting factor approaches infinity. Regarding the non-ideal curve, the proposed topology provides a maximum boost factor value of 20.51 as the duty cycle reaches 0.45.

III. OPERATION PRINCIPLES OF THE SUGGESTED INVERTER

The configuration of the proposed multilevel inverter is shown in Fig. 7. The input DC link of the 5L-NNPC is supplied by the proposed quasi-z-source converter. As shown in Fig. 7, 5L-NNPC employs six unidirectional switches, two clamp diodes, and two flying capacitors. Each flying capacitor's voltage should be set at one-fourth of the DC-bus voltage. The switching states of the 5L-NNPC inverter are summarized in Table 1.

A. MATHEMATICAL MODEL OF 5L-NNPC

The section presents the mathematical model of the 5L-NNPC inverter, utilizing its discrete-time model to achieve control objectives. The reference output current with an amplitude of

TABLE 1. The Switching States of 5L-NNPC

State		Switching Device Status						Flying Capacitors Voltages		Output voltage
		S_1	S_2	S_3	S_4	S_5	S_6	v_{C6}	v_{C7}	
5		1	1	1	0	0	0	No impact	No impact	$+ V_{dc}/2$
4		1	0	1	1	0	0	Charging ($i_{out} > 0$) Discharging ($i_{out} < 0$)	No impact	$V_{dc}/2 - v_{c6} = V_{dc}/4$
3	3A	0	1	1	0	0	1	Discharging ($i_{out} > 0$) Charging ($i_{out} < 0$)	Discharging ($i_{out} > 0$) Charging ($i_{out} < 0$)	$v_{c6} + v_{c7} - V_{dc}/2 = 0$
	3B	1	0	0	1	1	0	Charging ($i_{out} > 0$) Discharging ($i_{out} < 0$)	Charging ($i_{out} > 0$) Discharging ($i_{out} < 0$)	$V_{dc}/2 - v_{c6} - v_{c7} = 0$
2		0	0	1	1	0	1	No impact	Discharging ($i_{out} > 0$) Charging ($i_{out} < 0$)	$v_{c7} - V_{dc}/2 = -V_{dc}/4$
1		0	0	0	1	1	1	No impact	No impact	$-V_{dc}/2$

I and frequency of f_o is calculated by (23).

$$i_o^*(k) = I \times sin(2\pi f_o t) \tag{23}$$

B. MODEL OF LOAD CURRENT

Using Table 1, the output voltage of the inverter is calculated by (24). In terms of switching states and flying capacitor voltages, the output voltage is written.

$$\begin{cases} v_o = S_1 V_{dc} + (S_2 - 1)v_{C6} + (S_3 - 1)v_{C7} \\ +(1 - S_1)(v_{C6} + v_{C7}) - \dfrac{v_{dc}}{2} \end{cases} \tag{24}$$

where v_{C_6} and v_{C_7} are the flying capacitors voltages.

The inverter's output voltage can be expressed as follows, in terms of load currents, based on Fig. 7 and using KVL.

$$v_o = Ri_o + L\frac{di_o}{dt} \tag{25}$$

In (25), R and L denote the resistance and inductance of the load, and v_o represents the output voltage of the inverter. Also i_o indicates the load current. The load current model in the continuous-time domain can be written as:

$$\frac{di_o}{dt} = \frac{1}{L}v_o - \frac{R}{L}i_o \tag{26}$$

A forward Euler approximation is employed to substitute the derivative of the load current di_o/dt. The derivative is estimated using the approximation in (27).

$$\frac{di_o}{dt} = \frac{i_o(k+1) - i_o(k)}{T_s} \tag{27}$$

where T_s is the sampling time. The discrete-time model of the output current is produced by replacing equation (27) with equation (26).

$$i_o^p(k+1) = \frac{T_s}{L}v_o^p(k) + \left[1 - \frac{T_s R}{L}\right]i_o^m(k) \tag{28}$$

where $i_o^p(k+1)$ represents future inverter's load current, $v_o^p(k)$ denotes indicates inverter's output voltage, and $i_o^m(k)$ represents measured inverter load current.

C. MODEL OF FLYING CAPACITOR VOLTAGES

The mathematical model of flying capacitor voltages in the continuous-time domain is calculated in terms of capacitor current.

$$\begin{cases} v_{C_6}(t) = v_{C_6}(0) + \dfrac{1}{C_6}\int_0^t i_{C_6}(\tau)d\tau \\ v_{C_7}(t) = v_{C_7}(0) + \dfrac{1}{C_7}\int_0^t i_{C_7}(\tau)d\tau \end{cases} \tag{29}$$

The currents of the flying capacitors can be explained as a function of the switching states and output current based on Table 1. These currents are indicated in (30).

$$\begin{cases} i_{C_6}(k+1) = (S_1 - S_2)i_o(k) \\ i_{C_7}(k+1) = (S_5 - S_6)i_o(k) \end{cases} \tag{30}$$

The equation (29) can be defined as (31).

$$\begin{cases} v_{C_6}(k+1) = v_{C_6}(k) + \dfrac{T_s}{C_6}i_{C_6}(k+1) \\ v_{C_7}(k+1) = v_{C_7}(k) + \dfrac{T_s}{C_7}i_{C_7}(k+1) \end{cases} \tag{31}$$

The discrete-time model of flying capacitor voltages is derived by replacing (30) with (31). This product results in (32), as

TABLE 2. Comparison of the Proposed Topology With Some Other Topologies

	Boost factor	Diode voltage stress	Auxiliary switch voltage stress	Input current	Common ground	Efficiency (%)
Proposed	$\frac{2}{(1-2D)(1-D)}$	$\frac{V_{in}}{2}$	$\frac{1-D}{2}V_{in}$	Continuous	✓	94.01 at 100W
[13]	$\frac{2}{1-2D}$	$\frac{2}{1-2D}V_{in}$	$\frac{2}{1-2D}V_{in}$	Continuous	✓	Not Reported
[14]	$\frac{2}{1-2D}$	$\frac{V_{in}}{1-2D}$	-	Discontinuous	×	91 at 1.2 kW
[15]	$\frac{1+D}{1-3D}$	$\frac{1+D}{2(1-3D)}V_{in}$	$\frac{1+D}{2(1-3D)}V_{in}$	Continuous with significant ripple	×	94
[16]	$\frac{2}{1-2D}$	$\frac{V_{in}}{1-2D}$	-	Discontinuous	×	85.3 at 880W
[17]	$\frac{1}{1-2D}$	$\frac{V_{in}}{2(1-2D)}$	-	Continuous	✓	90.53
[21]	$\frac{2}{2D^2-4D+1}$	$\frac{V_{in}}{2D^2-4D+1}$	$\frac{1-D}{2D^2-4D+1}V_{in}$	Continuous	×	Not Reported
[22]	$\frac{2}{1-3D}$	$\frac{V_{in}}{1-3D}$	-	Discontinuous	×	Not Reported
[25]	$\frac{1}{1-4D+2D^2}$	$\frac{V_{in}}{1-4D+2D^2}$	-	Continuous with significant ripple	✓	91 at 500W
[26]	$\frac{1-2D}{D(1-D)}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{D(1-D)}$	Continuous with significant ripple	✓	93 at 280W
[27]*	$\frac{1}{D^2-3D+1}$	$\frac{2-D}{D^2-3D+1}V_{in}$	$\frac{1-D}{D^2-3D+1}V_{in}$	Continuous	✓	91.3 at 360W

* n=1

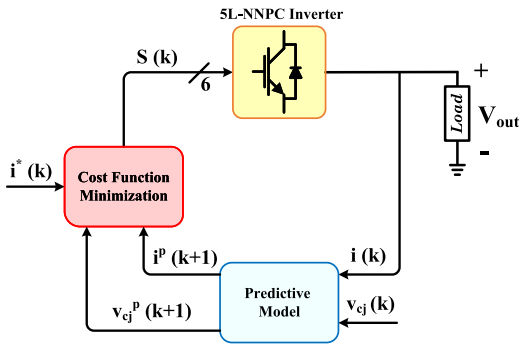

FIGURE 8. Block diagram of MPC method.

follows.

$$\begin{cases} v_{C_6}(k+1) = v_{C_6}(k) + \dfrac{T_s}{C_6}(S_1 - S_2)i_o(k) \\ v_{C_7}(k+1) = v_{C_7}(k) + \dfrac{T_s}{C_7}(S_5 - S_6)i_o(k) \end{cases} \tag{32}$$

D. COST FUNCTION

The purpose of the MPC-based control strategy is to regulate the output current and voltage of the flying capacitors by minimizing the deviation between the actual and desired values. The criterion is developed as a cost function as given in (33).

$$\begin{cases} g = \lambda_i \, |i_o^*(k+1) - i_o^p(k+1)| \\ + \lambda_{cap} \, |V_j^*(k+1) - v_j^p(k+1)| \end{cases} \tag{33}$$

where λ_i and λ_{cap} denote the weighting factors for the output current control and the flying capacitor voltages control, respectively and j represents the sequence of flying capacitors (C_6, C_7). Fig. 8 demonstrates the block diagram of the MPC method for a 5L-NNPC.

IV. PERFORMANCE COMPARISON

As a summary of Table 2, the proposed converter provides a low-ripple continuous input current and common ground between the input source and the output capacitor. Moreover, the maximum voltage stress of the diodes is half of the input source, regardless of the duty cycle.

The maximum voltage stress of diodes in the proposed converter and the other surveyed structures is depicted in Fig. 9(a). According to this figure, the diodes in the suggested converter withstand smaller voltage stress than the others in the entire duty cycle range. This value equals half of the input voltage, creating a circumstance in which the converter can be used in high-voltage applications.

Fig. 9(b) shows the boosting factor of the suggested converter compared to the studied topologies. What stands out from the illustration is that the provided converter is higher

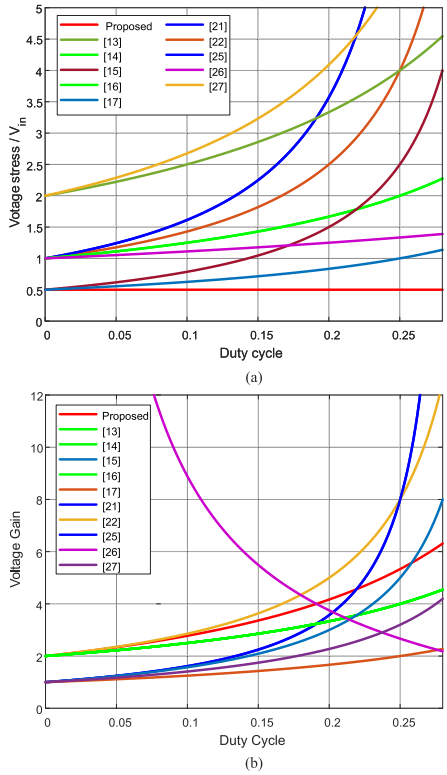

FIGURE 9. Topologies comparison of (a) diode stress voltage and (b) gain voltage.

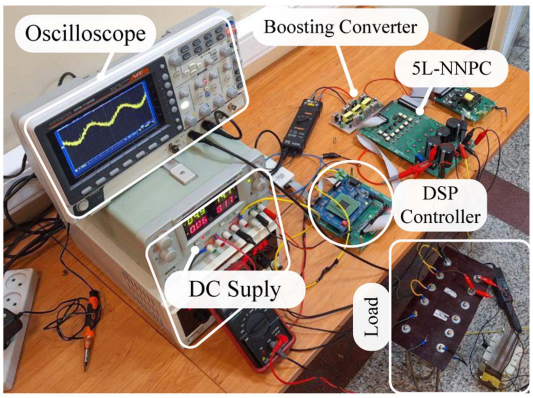

FIGURE 10. Photograph of the whole experimental prototype.

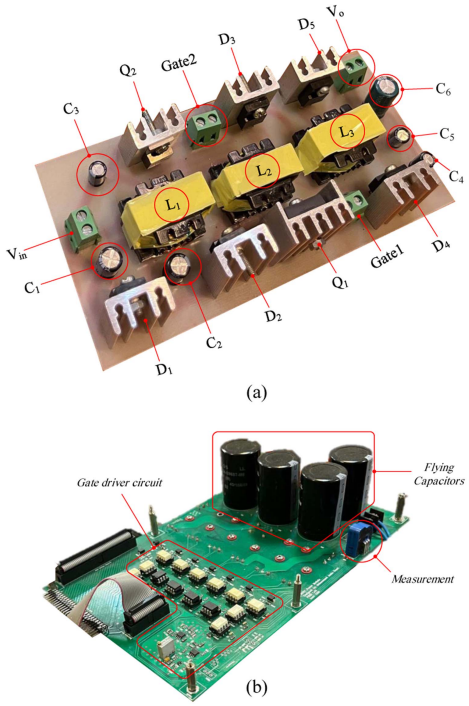

FIGURE 11. The prototype of (a) boosting converter and (b) 5L-NNPC inverter.

TABLE 3. Experimental Parameters

Variable	Experimental
L_1 (μH)	120
L_2 (μH)	200
L_3 (μH)	500
D_1-D_5	MBR20200
Q_1	IRFP260
Q_2	IRF540
C_1 and C_2 (μF)	22
C_3 (μF)	4.7
C_4 and C_5 (μF)	4.7
Frequency (kHz)	60
Duty cycle	27%
Flying Capacitors Voltage (V)	50
DC-link Capacitors (V)	1000
Flying Capacitors (μF)	1000
Load Apparaent Power (kVA)	1.6
Load Resistance (Ω)	12
Load Inductance (mH)	10

than others, except for [13, 26], in a wide duty cycle range of less than 22%. However, it should be noted that the suggested structure in [13] suffers from discontinuous input current and a lack of common ground, while the converter in [26] has the disadvantage of significant input current ripple.

V. EXPERIMENTAL RESULTS

To verify the theoretical performance, experimental prototypes of the whole setup, boosting structure, and 5L-NNPC inverter are implemented, as depicted in Figs. 10 and 11. Table 3 contains the prototype's detailed parameters. The duty cycle is %27, and the input voltage is 35 V, a value that is close to the voltage of a stand-alone solar panel. The control scheme is implemented on a TMS-320F28335 digital signal processor (DSP).

The currents of L_1, L_2, and L_3 are shown in Fig. 12(a)–(c), respectively. The inductors' currents increase linearly when

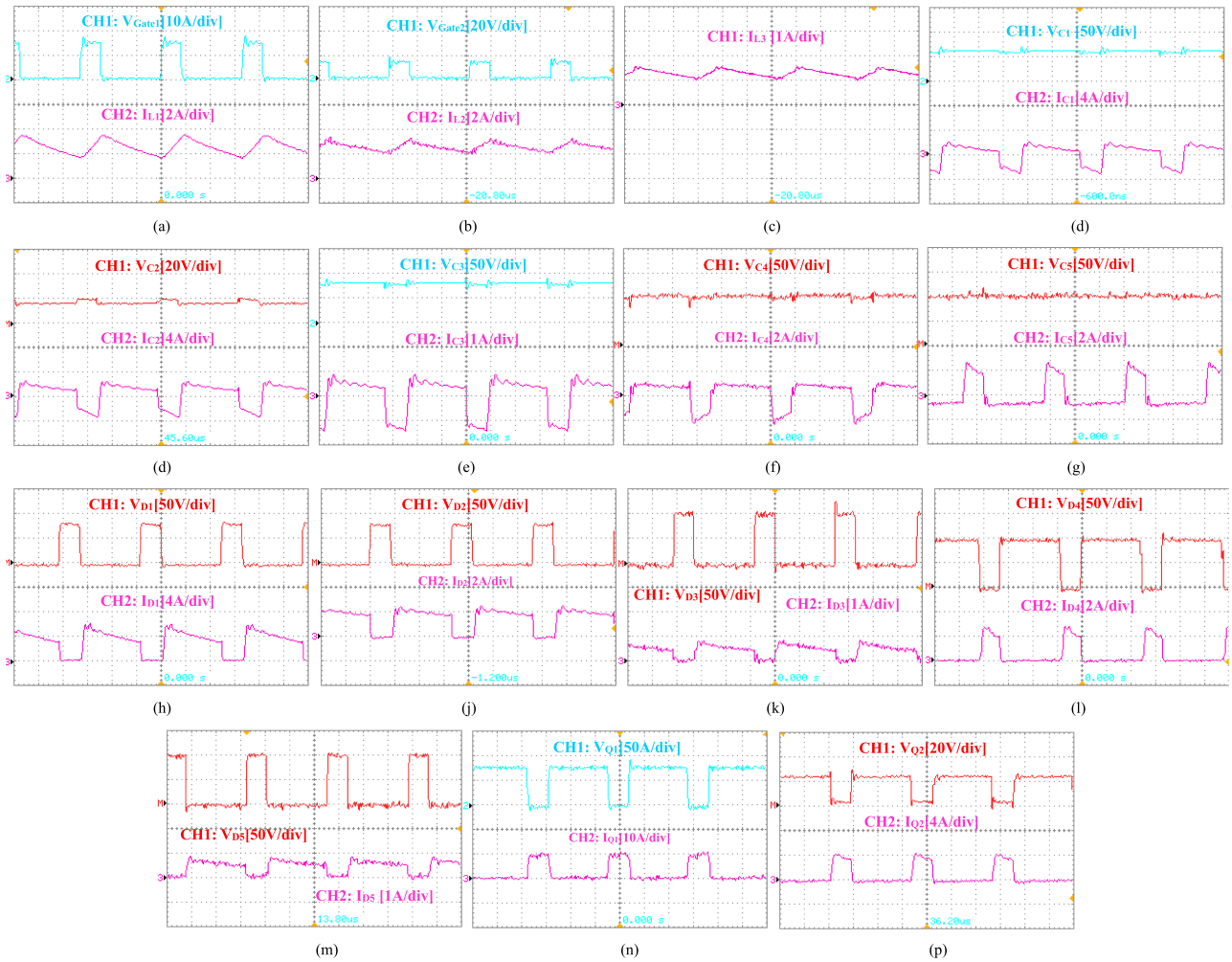

FIGURE 12. Experimental result of proposed boosting converter (a)–(p).

switches are ON, decreasing linearly during the OFF state. The continuous input current is denoted by L_1, which makes the proposed converter suitable for photovoltaic applications. The average current passing through L_3 is about 1.36 A.

Fig. 12(d)–(h) indicate the voltage waveforms of C_1, C_2, C_3, C_4, and C_5 besides their currents, respectively. The current passing through C_2 equals the input current when switches are ON. Additionally, the currents of C_1 and L_2 are identical during this state. It is observable that the capacitors' current decreases/increases linearly due to linear changes in the inductors' current. The positive and negative currents indicate the charging and discharging of the capacitors, respectively.

The voltage across the D_1, D_2, D_3, D_4, and D_5, alongside their currents, is shown in Fig. 12(j)–(n), respectively. D_1 and D_2 have equal voltage stress with an amplitude of approximately 73 V. Correspondingly, D_3, D_4, and D_5 have the same voltage stress, clamped to about 100 V. Notably, the voltage stress of all diodes is less than half of the output voltage. Consequently, high-quality diodes with insignificant parasitic components can be employed, reducing cost and loss.

Fig. 12(p)–(q) displays the voltage stress of Q_1 and Q_2. Due to the low voltage stress across switches, utilizing MOSFETs with low voltage withstanding is accessible. These switches have smaller ON resistance, which causes a reduction in the conduction loss and cost. Additionally, switches turn OFF/ON simultaneously, resulting in simplification in the drive and control circuits.

As depicted in Fig. 13(a), the 5L-NNPC is regulated to produce a current with a magnitude of 5 A (peak) and a frequency of 60 Hz. The voltages of the flying capacitor are kept controlled at 50 V, as indicated in Fig. 13(b).

In order to achieve dynamic loading conditions for the control method, two experiments were performed.

First, A sudden change in the estimated value of the load resistance while the actual value of the load is constant. The estimated value of the load suddenly changed by 25%. This value is usually the maximum reasonable amount for resistive loads. As can be seen in Fig. 14, against this amount of change, the quality of the load current has dropped a small amount.

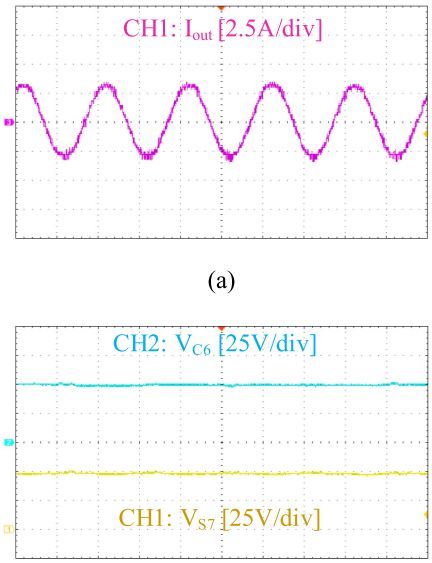

FIGURE 13. Experimental result of the inverter's performance (a) output current waveform and (b) voltage of capacitors.

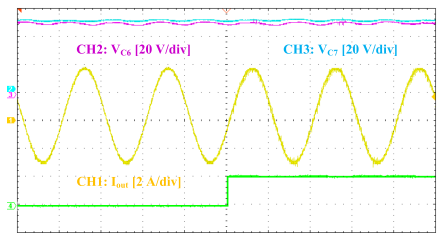

FIGURE 14. A step change in the estimated value of the load resistance.

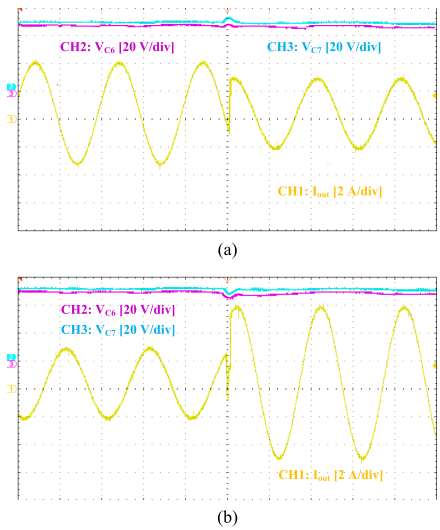

FIGURE 15. A step change in the load current reference.

Second, a sudden change in the load current reference. As shown in Fig. 15(a) and (b), a step change is applied in the reference current, and the experimental results are depicted. Fig. 15(a) and (b) show the accurate current tracking and well-regulated capacitor voltages during the transient state. These experimental results figures were added in the revised manuscript.

VI. CONCLUSION

A quasi-z-source inverter is introduced in this paper which is based on a combination of a novel qZS structure and a 5L-NNPC inverter. In the steady-state operating mode of qZS topology, the capacitor voltages, boosting factor, current and voltage stress of the component, and non-ideal boost factor have been analyzed. To provide a sinusoidal output current, a single-phase 5L-NNPC inverter is connected to the proposed qZS converter. The 5L-NNPC generates a 5-level voltage waveform at its AC side utilizing two flying capacitors per phase. The 5L-NNPC in combination with the introduced qZS topology is a good candidate for PV applications. However, 5L-NNPC lacks sufficient redundant switching states to regulate the voltages of flying capacitors. To tackle this problem, a multi-objective MPC-based control scheme is developed to control the AC side current of the inverter and adjust the voltages of flying capacitors simultaneously. The experimental results support the effectiveness and performance of the introduced structure.

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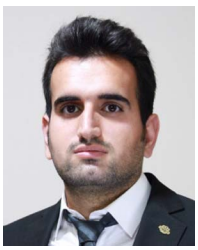
REFERENCES

[1] R. Asgarnia and E. Afjei, "A novel high-efficient step-up converter with continuous input current, common ground, and minimum stress on semiconductors," *IET Power Electron.*, vol. 16, no. 7, pp. 1128–1145, 2023.
[2] N. V. Kurdkandi et al., "A new seven-level transformer-less grid-tied inverter with leakage current limitation and voltage boosting feature," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 1, pp. 228–241, Jan. 2023.
[3] S. H. Fard and H. T. Malazi, "A Two-dimensional self-coordination mechanism of agents in a minority game," in *Proc. 8th Int. Conf. Fundamentals Softw. Eng.*, 2019, pp. 20–36.
[4] R. Asgarniya, A. M. Kamalkhani, and E. Afjei, "A non-isolated ultra step-up converter based on switched inductors and conventional boost converter," in *Proc. 12th Smart Grid Conf.*, 2022, pp. 1–6.
[5] M. Shamouei-Milan, M. Hassanifar, Y. Neyshabouri, S. Golshannavaz, and D. Nazarpour, "A new hybrid T-type nested neutral point clamped (NNPC) multilevel inverter with improved voltage balancing strategy," in *Proc. 28th Iranian Conf. Electr. Eng.*, 2020, pp. 1–6.
[6] M. Hassanifar, M. Shamouei-Milan, and Y. Neyshabouri, "T-type nested neutral point clamped (T-NNPC) multilevel inverter: Identification and diagnosis of IGBT switch failures," in *Proc. 13th Power Electron., Drive Syst. Technol. Conf.*, 2022, pp. 409–413.
[7] M. Hassanifar, M. Shamouei-Milan, Y. Neyshabouri, D. Nazarpour, and S. Golshannavaz, "Fast detection and localization of open-circuit switch faults in nested neutral point clamped (NNPC) inverter," in *Proc. 11th Power Electron., Drive Syst. Technol. Conf.*, 2020, pp. 1–6.

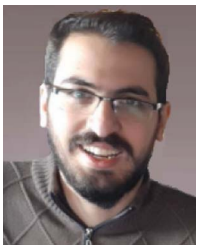
[8] M. S. Kim, J. Pribadi, and D. C. Lee, "Six-level hybrid diode-clamped inverter topology and DC-link capacitor voltage balancing control," *IEEE Trans. Power Electron.*, vol. 39, no. 6, pp. 7192–7205, Jun. 2024.
[9] M. G. Marangalu, N. V. Kurdkandi, K. K. Monfared, I. Talebian, Y. Neyshabouri, and H. Vahedi, "A new high step-up SC-based grid-tied inverter with limited charging spike for RES applications," *IEEE Open J. Power Electron.*, vol. 5, pp. 295–310, 2024.
[10] N. V. Kurdkandi et al., "A new transformer-less common grounded three-level grid-tied inverter with voltage boosting capability," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 1896–1909, Sep. 2021.
[11] R. Asgarniya, M. Shamouei-Milan, M. G. Marangalu, M. R. Islam, and E. Afjei, "Design, analysis, and implementation of a transformer-less step-up converter with continuous input current and high voltage gain ratio," in *Proc. IEEE IAS Glob. Conf. Renewable Energy Hydrogen Technol.*, Male, Maldives, 2023, pp. 1–6.
[12] A. Samadian, M. G. Marangalu, S. H. Hosseini, M. Sabahi, M. R. Islam, and R. Shah, "High step-up common grounded switched quasi Z-source DC-DC converter using coupled inductor," in *Proc. IEEE 1st Ind. Electron. Soc. Annu. On-Line Conf.*, kharagpur, India, 2022, pp. 1–7.
[13] S. Naderi and H. Rastegar, "A new non-isolated active quasi Z-source multilevel inverter with high gain boost," *IEEE Access*, vol. 11, pp. 2941–2951, 2023.
[14] A. -V. Ho and T. -W. Chun, "Single-phase modified Quasi-Z-source cascaded hybrid five-level inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5125–5134, Jun. 2018.
[15] A. Anwar et al., "An impedance network-based three level quasi neutral point clamped inverter with high voltage gain," *Energies* 13, no. 5, 2020, Art. no. 1261.
[16] A. -V. Ho and T. -W. Chun, "Topology and modulation scheme for three-phase three-level modified Z-source neutral-point-clamped inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11014–11025, Nov. 2019.
[17] C. Qin, C. Zhang, A. Chen, X. Xing, and G. Zhang, "A space vector modulation scheme of the quasi-Z-source three-level T-type inverter for common-mode voltage reduction," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8340–8350, Oct. 2018.
[18] M. Amirbande, M. S. Zarbil, A. Vahedi, and M. Rivera, "Simple boost control of a new high voltage gain z-source inverter," in *Proc. 9th Annu. Power Electron., Drive Syst. Technol. Conf.*, 2018, pp. 169–173.
[19] X. Pan, Z. Pang, Y. Liu, S. Yin, and C. Ju, "Enhanced-boost bidirectional quasi-Z-source inverter with novel active switched inductor cells," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 3041–3055, Sep. 2020.
[20] I. Fadlika, Q. A. Sias, H. M. H. Zain, I. D. Wahyono, and A. N. Afandi, "Improved two switched-inductor quasi-Z-source inverter with high voltage gain and reduced inductor current ripple," in *Proc. Conf. Power Eng. Renew. Energy*, 2018, pp. 1–6.
[21] F. Xupeng, L. Qiang, W. Pu, and W. Song, "Improved quasi-switched-z-source inverter with high voltage gain," in *Proc. Chin. Automat. Congr.*, 2020, pp. 673–677.
[22] V. Jagan and S. Das, "High boosting type Z-source inverter/ improved Z-source inverter for solar photovoltaic system," in *Proc. Annu. IEEE India Conf.*, 2015, pp. 1–6.
[23] A. Kumar, Y. Wang, M. Raghuram, P. Naresh, X. Pan, and X. Xiong, "An ultra high gain quasi Z-source inverter consisting active switched network," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 67, no. 12, pp. 3207–3211, Dec. 2020.
[24] P. K. Gayen and S. Das, "An enhanced ultra-high gain active-switched quasi Z-source inverter," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 69, no. 3, pp. 1517–1521, Mar. 2022.
[25] X. Zhu, B. Zhang, and D. Qiu, "A new nonisolated quasi-Z-source inverter with high voltage gain," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 2012–2028, Sep. 2019.
[26] A. Sarikhani, M. M. Takantape, and M. Hamzeh, "A transformer-less common-ground three-switch single-phase inverter for photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8902–8909, Sep. 2020.
[27] G. Zarei, E. Babaei, M. B. B. Sharifian, H. Aghaei, and S. Asl, "High voltage gain switched Z–source inverter with low current stress," *IET Power Electron.*, 17, no. 1, pp. 38–53, Jan. 2024.
[28] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A new nested neutral point-clamped (NNPC) converter for medium-voltage (MV) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6375–6382, Dec. 2014.
[29] A. Dekka and M. Narimani, "Model predictive control of a five-level nested neutral point clamped converter," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2018, pp. 759–763.
[30] A. Dekka and M. Narimani, "Capacitor voltage balancing and current control of a five-level nested neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10169–10177, Dec. 2018.
[31] M. R. Chowdhury, S. Chowdhury, M. A. Rahman, and M. R. Islam, "Advanced switching sequences based model-predictive control for single-phase NPC converters," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3515–3526, Apr. 2022.
[32] M. Shamouei-Milan, R. Asgarniya, M. G. Marangalu, M. R. Islam, and A. Mehrizi-Sani, "A single-phase high gain active-switched quasi z-source NNPC inverter," in *Proc. IEEE IAS Glob. Conf. Renew. Energy Hydrogen Tech.*, Male, Maldives, 2023, pp. 1–6.

MILAD SHAMOUEI MILAN was born in Poldasht, West Azerbaijan Province, Iran, in 1997. He received the B.Sc. and M.Sc. degrees in electrical engineering in 2020 and 2023, respectively. His research interests include design, analysis, control methods, fault detection, and fault-tolerant of multilevel converters/inverters and their specific applications.



REZA ASGARNIA was born in Ilam, Iran, in 1998. He received the B.Sc. and M.Sc. degrees in electrical engineering in 2020 and 2023, respectively. His current research interests include the design and analysis of power converters, control in power electronics, soft-switching techniques, and renewable energy systems.

MILAD GHAVIPANJEH MARANGALU was born in Urmia, Iran, in 1992. He received the B.Sc. degree in electrical engineering and the M.Sc. degree in power electrical engineering from Urmia University, Urmia, Iran, in 2014, and 2018, respectively, and the Ph.D. degree in power electronics & power systems from the University of Tabriz, Tabriz, Iran, in 2022. Over the past six years, he has focused on the design and control of grid-tied power electronic converters. His Ph.D. thesis, titled Design of an Improved Grid-Tied Multilevel Inverter for Photovoltaic Applications, resulted in the creation of three prototype grid-tied inverters. His master's thesis, Designing a Single DC-Source Five-Level Inverter for Photovoltaic Applications Considering MPPT Algorithm, further showcases his expertise in this area. During his doctoral studies, he was also a guest Researcher with the Tallinn University of Technology, Tallinn, Estonia, where he collaborated with the Power Electronics Research Group from 2021 to 2022. He is currently a Postdoctoral Researcher with the University of L'Aquila, L'Aquila, Italy. Dr. Ghavipanjeh has authored and coauthored 40 journal and conference papers. His current research interests include multilevel inverters, grid-tied photovoltaic inverters, high step-up power electronic converters, control systems for multilevel inverters, and renewable energy systems.



KOUROSH KHALAJ MONFARED received the M.Sc. and Ph.D. degrees in electrical engineering in 2017 and 2022, respectively. He is currently an Assistant Professor of electrical engineering with the School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran. His current research interests include advanced control in power electronics, multilevel converter applications, renewable energy systems, and pulsed power technology.

YOUSEF NEYSHABOURI received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering in 2011, 2013, and 2018, respectively. He is currently an Assistant Professor with the Faculty of Electrical and Computer Engineering, Urmia University, Urmia, Iran. His current research interests include multilevel power converters and their application in the power system.

HANI VAHEDI received the Ph.D. degree (with honors) from École de Technologie Superieure (ÉTS), University of Quebec, Quebec, QC, Canada, in 2016. He has authored or coauthored more than 60 technical papers in IEEE conferences and Transactions. He also published a book on Springer Nature and a book chapter in Elsevier. He is the Inventor of the PUC5 converter, holds multiple U.S./World patents, and transferred that technology to the industry, where he was developing and commercializing the first bidirectional Electric Vehicle DC Charger based on his invention. After seven years of experience in industry, he joined Delft University of Technology, Delft, The Netherlands, where he is currently an Assistant Professor with the DCE&S Group, working towards the electrification of industrial processes for clean energy transition. His research interests include multilevel converter topologies, control and modulation techniques, and their applications in the electrification of industrial processes and clean energy transition, such as smart grids, renewable energy conversion, electric vehicle chargers, green hydrogen production (electrolyzers), and fuel-cell systems. He was the recipient of the Best Ph.D. Thesis Award for the academic year during 2016–2017 from ETS. He is an Active Member of the IEEE INDUSTRIAL ELECTRONICS SOCIETY (IES) and its Student & Young Professionals (S&YP) committee. He is the Co-Chair of special sessions, Co-Organizer of the S&YP Forum, and Co-Chair of three M video sessions in IES conferences. He is also an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE OPEN JOURNAL OF INDUSTRIAL ELECTRONICS SOCIETY.