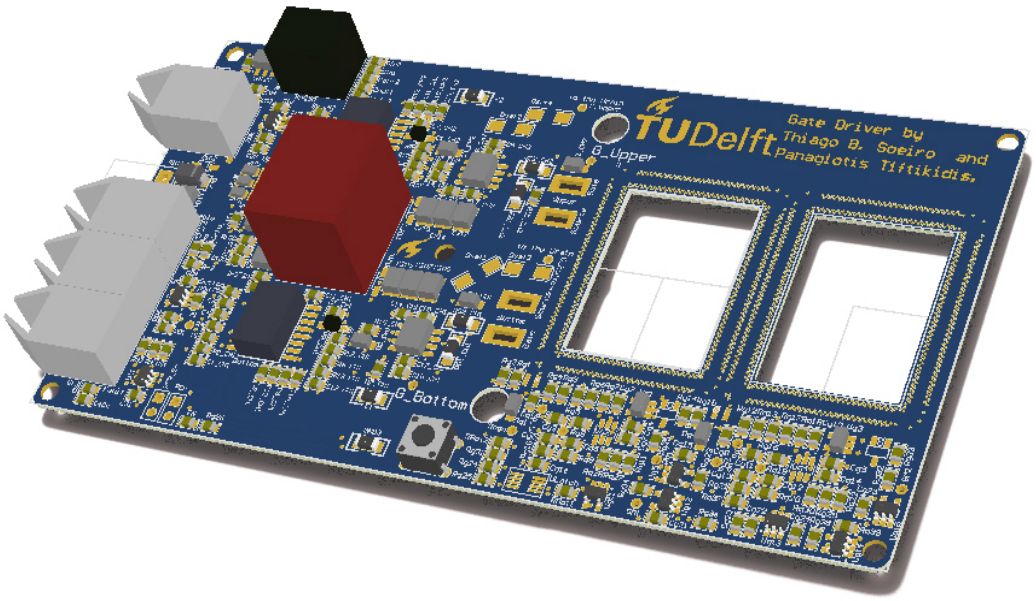
Developing Gate Drivers with Ultra-Fast Short-Circuit Detection for High Performance Semiconductor Technology



Master of Science Thesis by Panagiotis Tiftikidis

Faculty of Electrical Engineering, Mathematcis and Computer Science

Departmet of Electrical Sustainable Energy

DC Systems, Energy Conversion and Storage

Developing Gate Drivers with Ultra-Fast Short-Circuit Detection for High Performance Semiconductor Technology

Master of Science Thesis

Delft University of Technology

by

Panagiotis Tiftikidis

Supervisor:	Dr. Thiago Batista Soeiro
Thesis Committee:	Pr. dr. Pavol Bauer Dr. Thiago Batista Soeiro Dr. Aleksandra Lekic

An electronic version of this thesis is available at `https://repository.tudelft.nl`

Wednesday 14th October, 2020

TU Delft Delft University of Technology

DC Systems, Energy Conversion and Storage

Abstract

The last ten years with the entrance of the SiC devices at the power electronics industry, new fundamental requirements have emerged. New types of gate drivers need to be developed due to the need for creating two voltage levels for driving the SiC based power switches efficiently; one positive and one negative bias voltage. Besides this requirement, extra measures need to be taken for the proper operation of the driver and its sufficient protection. The electromagnetic interference is increased compared with the conventional silicon based applications, which potentially can cause malfunction or disruption at the operation of the gate driver. Furthermore, ultra-fast response in case of faults must be designed, because of the lower fault capability of the new devices. Sophisticated methods are employed with the measurement of di/dt being one of them. This work focuses on proposing, designing, and testing of a robust gate driver capable of detecting and isolating in less than 1 μs a short-circuit of a power module. It uses the PCB principle embedded Rogowski coil so that the gate driver control can re-build a voltage signal, which is an image of the current flowing through the upper and bottom active switches. Finally, a comparison band logic interrupts the gate ON signal when the current reaches a prohibitive level. Simulation and experimental tests are used to verify the advantages of the proposed gate driver.

Acknowledgments

At this point I would like to thank the following people who played their role helping me to accomplish this project.
Firstly, I would like to express my deepest appreciation to my supervisor Dr. T. Batista Soeiro, for guiding and supporting me at every stage of the project.
Secondly, I would like to thank Francesca Grazian and Marco Stecca for their help in different parts of the project. Especially without Thiago and Marco, during this coronavirus period we live, I could not reach up to end of this project.
Last but not least, I would like to express my gratitude to my family and my friends for their support and encouragement during these two years.

’Ενα ευχαριστώ,
σε όλους όσους στερήθηκαν και βοήθησαν αυτά τα δύο χρόνια.

Contents

List of Figures **vi**

List of Tables **vii**

1 Introduction **1**
1.1 Background . . . 1
1.2 Project Outline . . . 2

2 Problem Definition **3**
2.1 Semiconductor Materials . . . 3
2.2 Problems . . . 3
2.3 Methodology . . . 3

3 Short-Circuit Detection Methods **5**
3.1 De-saturation . . . 5
3.2 Shunt Resistor . . . 6
3.3 Current Transformer . . . 6
3.4 Rogowski Coil . . . 7
3.5 Leg Voltage Measurement . . . 9
3.6 Method Selection . . . 9
3.7 Coil Design . . . 10
3.7.1 Step 1. Shape and size of the coil . . . 10
3.7.2 Step 2. Winding configuration . . . 11
3.7.3 Step 3. Number of turns . . . 11

4 High-Voltage Gate Drivers **13**
4.1 Gate Driver Role . . . 13
4.2 Gate Driver Design . . . 13
4.2.1 Communication with the microcontroller . . . 14
4.2.2 Gate driver selection . . . 14
4.2.3 Signal process circuit . . . 15
4.2.4 Power supply . . . 17
4.2.5 Design summary . . . 18

5 Simulation Results and PCB Design **20**
5.1 Rogowski Coil Equivalent Circuit . . . 20
5.2 Determine the Optimized Value of R_d . . . 20
5.3 Rogowski Coil Model . . . 22
5.4 Active Integrator Model . . . 25
5.5 Printed Circuit Board Design . . . 27
5.5.1 Creation of the electrical circuit . . . 28
5.5.2 Assignment of footprints at the components of the circuit . . . 29
5.5.3 Implementation of the connections on the board . . . 30

6 Experimental Results **31**
6.1 Coil Parameters . . . 31
6.2 Normal Turn-On . . . 32
6.3 Digital Signal Process Circuit Test . . . 34
6.4 Short-Circuit Test . . . 35

7 Conclusion **37**
7.1 Gate Driver Design with Integrated Protection System 37
7.2 Recommendations for Future Research 37

Bibliography **38**

A Appendix A **40**

List of Figures

1.1 Half bridge module 1

3.1 I-V curve of IGBT [1] 5
3.2 De-saturation method detection circuitry [2] 5
3.3 Current measurement over-current detection circuitry [3] 6
3.4 Circular Rogowski coil [4] 7
3.5 Passive integrator circuit 8
3.6 Active integrator circuit 9
3.7 SiC module overview (a) and pins configuration (b) [5] 10
3.8 Top view dimensions (a) and side view dimensions (b) [5] 10
3.9 One side winding configuration 11
3.10 Clearance distance of pads on PCB 12
3.11 Dimensions of the designed coil 12

4.1 Power semiconductor driving steps 13
4.2 Totem-pole configuration for current boosting 15
4.3 Non-ideal active integrator model 16
4.4 Reaction circuit 17
4.5 Generation of voltage supply 18
4.6 Input of the MOD pin 18
4.7 Gate driver circuit 19

5.1 Rogowski coil distributed model 20
5.2 Rogowski coil lumped model 20
5.3 ((a) Step response; and (b) Bode diagram without using damping resistor 21
5.4 (a) Step response; and (b) Bode diagram for five different values of damping resistance 22
5.5 Rogowski coil Simulink model 23
5.6 Current transition during a turn-on procedure 23
5.7 The distances for the measurement of the self-inductance 24
5.8 Voltage signals of the coil during both normal turn-on and short-circuit cases . . . 25
5.9 Simulink model of active integrator 25
5.10 Input and output integrator voltages for R_{in}=200 Ω, C=200 pF and R_{ext}=200 MΩ 26
5.11 Integrator output for different values of R_{in}, C and R_{ext} 26
5.12 (a) Integrator output with a short-circuit at 0.5 seconds; and (b) its response for different values of capacitances 27
5.13 Digital signal processing circuit 28
5.14 Gate driver IC configuration on PCB 29
5.15 Power supply subsystem ln the PCB design 29
5.16 Rogowski coil shape 30
5.17 PCB and 3D model of the gate driver 30

6.1 (a)PCB with the module and (b) experimental setup 31
6.2 Coil impedance measurement using Agilent 4294A impedance analyzer 31
6.3 Wire impedance measurement using Agilent 4294A impedance analyzer 32
6.4 Double-pulse test schematic 32
6.5 V_{GS} (yellow curve) and V_{DS} of the bottom switch (green curve) and current across the inductor (light blue curve) during a double pulse test 33
6.6 Current flowing through the switch (purple curve) and Rogowski coil output (yellow curve) 33
6.7 Threshold value definition 34
6.8 Low voltage test flowchart 34

6.9 Rogowski integrated voltage (yellow curve), current flowing through the switch (purple curve) and comparator output (green curve) 34
6.10 V_{GS} (yellow curve) and V_{DS} of the bottom switch (green curve) and mains current (light blue curve) during the comparator trip test 35
6.11 V_{GS} of bottom switch (yellow curve), V_{GS} of upper switch(green curve), current across the switch (orange curve), output of the integrator (light blue curve) and fault detection signal (purple curve) during a low inductive short-circuit with high di/dt 35
6.12 V_{GS} of bottom switch (yellow curve), current across the inductor L of Figure 6.4 (dark blue curve), V_{DS} across the bottom switch(green curve), current across the bottom switch (orange curve), output of the integrator (light blue curve) and fault detection signal (purple curve) during a low di/dt fault 36

A.1 Rows 1-20 of the code for calculating the mutual and self-inductance 40
A.2 Rows 21-44 of the code for calculating the mutual and self-inductance 41
A.3 Rows 45-56 of the code for calculating the mutual and self-inductance 41

List of Tables

3.1 Rogowski coil window opening dimensions 11
3.2 Clearance requirements for uncoated external conductors 12

4.1 Gate driver requirements 13
4.2 ACPL-344JT operating features 14
4.3 D latch truth table 16
4.4 Gate driver components 19

1 | Introduction

1.1 Background

The progress on the field of Power Electronics, has facilitated the transition to more and more DC power applications instead of AC. The charging of electric vehicles, solar park installations or even more domestic applications like phone or laptop chargers will have lower power losses because of the number of required converters will be reduced.
The traditional Silicon (Si) made power switches are gradually replaced by Silicon Carbide (SiC), which exhibit better performance characteristics, like lower switching times or higher breakdown voltages. Higher efficiencies are achieved, but on the other side new needs are created like:

- consideration for limiting of the electromagnetic interference (EMI) design
- new short-circuit (SC) detection methods

The EMI reduction is a need created by the very fast switching transitions, which result in large dV/dts that combined with the parasitic capacitances currents will flow through the components of the circuit that may affect its operation.
Three different types of short-circuits can be defined; short-circuit I, short-circuit II and short-circuit III. The short-circuit I type, which is also known as hard short-circuit, is a direct turn-on of the switch to a short circuit [6],[7]. Initially, the power switch is off and no current is flowing through it. When it gets into the fault, the current rises up to its saturation value, which can be a few kiloamperes [7]. The second short-circuit type happens when the device is under load. The slope of the current is determined by the DC voltage of the leg and the short-circuit loop inductance. Usually, type II faults have worse consequences than the corresponding type I. As type III are characterized all the cases of short-circuits that happen during the time that the current flows through the freewheling diode connected in parallel with the power switch. Both type II and type III are called faults under load (FUL), since they are failures during the ON-state of the device, while the short-circuit type I starts when the device is OFF.
Besides the typical faults, there are additional risks in case of using a half-bridge module, which are used for achieving higher voltage levels.

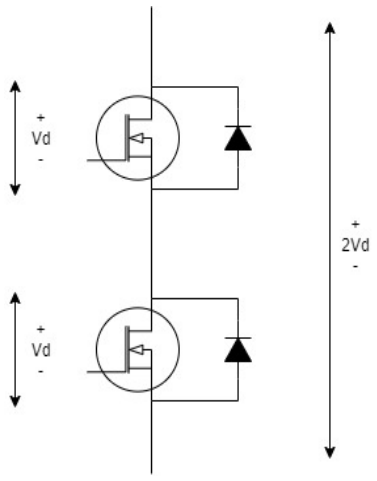


Figure 1.1: Half bridge module

If the two gates of the module is shown on Figure 1.1 are not exited simultaneously twice the nominal voltage will be applied across the switch that is on.
While the EMI issues can be handled, with selecting components with low values of coupling capacitances, the second problem needs a more sophisticated way to be confronted. The smaller

size of the dice of the SiC MOSFETs compared with the Si based devices, results in a lower SC capability, since the thermal breakdown of the switch will happen faster [8]. The most common method for SC detection is the desaturation method, which for SiC devices is not as efficient as it is for the corresponding Si ones, because it cannot offer adequately fast protection.
A series of methods has been employed for satisfying this protection need. Besides the direct measurement of the current flowing through the switch, a number of methods evaluating the di/dt has been developed. Sensing the current ratio across the parasitic inductances or Rogowski coils (flexible or not) are the two most acquainted ones. The first one is based on the level of influence of the parasitics on the voltage across them during a normal turn-on and the differences that are observed when a fault event takes place. On the other side the basic principle of Rogowski coil is the voltage that is inducted across a coil wounded around a current conductor, because of the coupling between the conductor and the coil.

1.2 Project Outline

The project focuses on creating a gate driver capable of detecting and isolating in less than 1 μs a short-circuit, holding at the same time the EMI at very low levels. The thesis is organized as follows. At **Chapter 2**, the state of art in the semiconductor technology is presented. The problems that are introduced are analytically described, along with the methodology that was followed for finding a solution.
At **Chapter 3**, the short-circuit detection methods are presented, with their advantages and disadvantages being analysed. This is followed by the selection of the most suitable method and its design.
Chapter 4 is devoted to the analysis of the basic principles of gate drivers and especially for high voltage applications. The necessary ICs are selected, accompanied by proper passive components for creating the driver stage and the signal processing circuits. Closing this chapter the power supply unit is shown.
Chapter 5 includes the simulation models that were developed for better understanding of the theoretically analysed concepts and validating all the assumptions that were made. The results of these models composed the basis of the whole design.
At **Chapter 6** the experimental results are presented, while **Chapter 7**, summarizes the most important parts of the project.

2 | Problem Definition

At the section 2.1 of the chapter a brief analysis of contemporary semiconductor devices will be performed. Following this, occurring problems because of their use will be presented in the section 2.2, while in the section 2.3 the approached methodology for solving them will be analyzed.

2.1 Semiconductor Materials

From 2009, when they became commercially available, Wide band-gap semiconductor materials, like Silicon Carbide and Gallium Nitride (GaN), have become the standard for high performance solutions in the power electronics field [9]. Compared with the traditional silicon based power devices, they result in higher efficiencies and power density of the application at hand as well as the ability of operating under higher temperatures [10],[8],[11]. The increased efficiencies is a result of the decreased switching times and of the on-resistance, reducing the power dissipation on the switches. This allows the increment of the switching frequency, leading to reduction of volume of the components. The last of their benefits is their electric field break down capability, which can be up to ten times higher than the Si based power switches [9],[12].
Between the wide band-gap devices, the SiC-based precede because of their unique advantage of being able to be doped within a wide rage both with n and p-type carriers[9]. As will be presented also later in the report, this is the material that the research is mainly based on.

2.2 Problems

Although the aforementioned benefits of using wide band-gap devices, there are also a few problems that need to be encountered. Two of the most important of them are:

- the need a fast short-circuit protection system
- the need for mitigating the noise induced by the fast switching transitions

The short-circuit withstand capability both of SiC and GaN devices is much smaller than the one of the classic power switches, therefore these faults need to be isolated within a few microseconds [8],[2],[13]. A thermal breakdown is more potential in these devices, due to the smaller sizes of their chips. Moreover, the short-circuit current values can become large because the drive needs of a SiC MOSFET require a high positive bias voltage, which is in the range of 20 V [8].
Besides the thermal breakdown, which causes the destruction of the device, there are also reliability issues caused by the operation under overload conditions on the switch. These issues are worsened combined with the high positive bias voltage. Thus, the first requirement for the gate driver is the existence of a very fast protection system. The time that was set as the target for detecting and reacting in case of a SC was 1 μs.
The second requirement is the highest possible noise immunity of the system. The existing parasitics in every application, induce false currents and voltage signals, known as Electromagnetic Interference (EMI), with their values being significantly high due to the high dV/dt and dI/dt during the switching transients [8],[13],[14]. For increasing the noise immunity of the gate driver, the value of the parasitic capacitances must be as low as possible, because the voltage commutations are larger than the corresponding ones of the current.

2.3 Methodology

The research approach to the project is presented below:

- The first step comprises the literature review for comprehending the concepts of the high voltage gate drivers and the short-circuit protection methods. Given that the power device

is SiC module, most of the literature research was related with this material. Another topic to be researched is the ways to achieve an adequate level of noise immunity.

- The second step is to propose a generic design of the gate driver along with the protection scheme that was selected.
- The third step is the creation of simulation models for validating the theoretical assumptions and the correctness of the design from the previous step.
- The final step of the project is the PCB design and a series of experimental sessions to extract some of the parameters of the setup and confirm the efficiency of the protection scheme.

3 | Short-Circuit Detection Methods

At this chapter the examined short-circuit detection methods will be analyzed. Furthermore, the selection and the design of the most suitable protection scheme will be presented.

3.1 De-saturation

The most traditional method for detecting a short-circuit is the de-saturation method. It is commonly used for protecting bipolar devices under over-current conditions [8], [15]. Many modern gate driver ICs have integrated a de-saturation protection circuit.
The technique is based on the measurement of the voltage across the switch, when the state of the device is ON (V_{CE} for the bipolar and V_{DS} for the unipolar devices) [2].

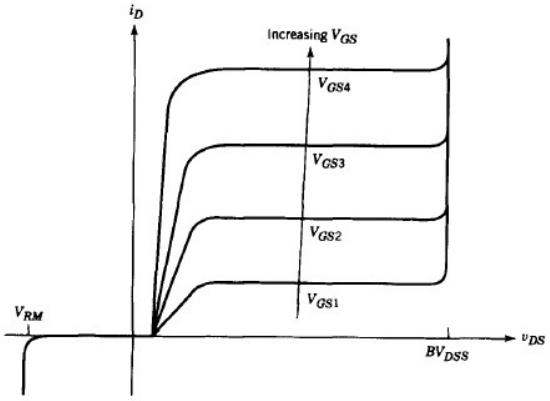


Figure 3.1: I-V curve of IGBT [1]

The logic of the method is based on the increment of the current during a short-circuit. When the current starts to rise above the knee of the curve of Figure 3.1, the device is dragged out of saturation and the voltage across it is increased [8],[2]. This voltage is compared with a threshold voltage and when this last one is exceeded the protection system is triggered.

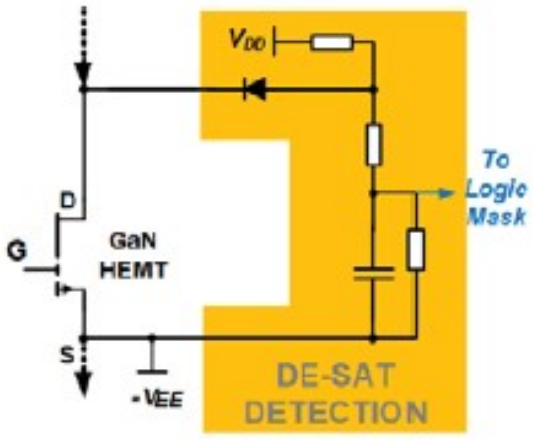


Figure 3.2: De-saturation method detection circuitry [2]

As it can be observed at Figure 3.2, an RC low-pass filter is used, to absorb parasitic currents,

which are caused due to the high dV/dt [2]. The filter introduces a certain blanking time, which is necessary because during the turn-on process of the switches, when the voltage across the device becomes larger than the threshold. This time gives enough time to the voltage across the switch to be stabilized at its steady-state value, without being sent a false tripping signal [8]. The introduced delay is dependent on the parameters R and C and is given by:

$$\tau = R \cdot C \tag{3.1}$$

3.2 Shunt Resistor

The second method is a current measurement method using a shunt resistor. The under-protection device is connected in series with the resistance with the voltage signal across it being sent into a RC filter. Like the de-saturation method, the RC filter is used to prevent a false turn-off because of noise introducing a delay [16] and is given by 3.1. Although this is a very simple method to be implemented, there are few drawbacks like [15]:

- Increased stray inductance
- Increased conduction losses
- Not offering galvanic isolation

Especially the first two items make this method inappropriate to be implemented, thus there will be no more elaboration on this method.

3.3 Current Transformer

The current measurement is a very simple detection method. The current that flows through the device which is under protection, is downgraded using a current transformer. Having a lower current, enables the implementation of a low voltage over-current detection system, as is shown in Figure 3.3.

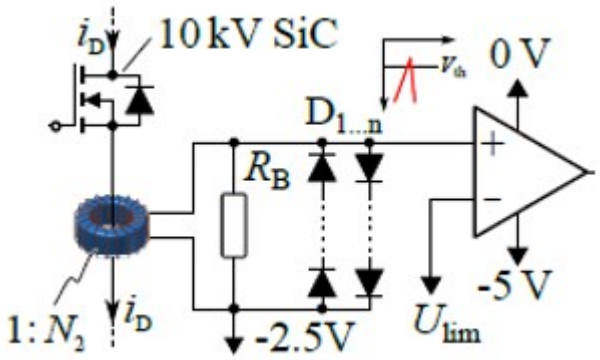


Figure 3.3: Current measurement over-current detection circuitry [3]

At this figure, the nominal current of the SiC MOSFET is 75 A. With the current transformer having a turn ratio 1:30 and the value of R_B being 1 Ω, when the value of the switch becomes larger than 75 A, a voltage signal higher than 2.5 V, is led into the positive input of the comparator. There, if the threshold value is exceeded, the reaction circuit is turned on.
The main disadvantage of this method is the saturation problem as every magnetic component may face. This will influence the implemented detection system, affecting the protection of the application as a result. Another drawback is the inserted stray inductance in the circuit [17], with the ringing phenomena during the switching transitions being amplified.

3.4 Rogowski Coil

For measuring the rate of change of the current over the time, a Rogowski coil is used. A Rogowski coil is an air-core transformer [18], which is placed around the conductor, and is used for measuring the di/dt of the current that flows through this conductor, which is expected to be high enough in a short circuit phenomenon. This method outmatches the shunt and the current measurement in terms of linearity, bandwidth and weight. Furthermore, it is a method that can offer galvanic isolation of the protection circuitry from the high voltage side, because of the airgap [19]. Besides the above, it does not increase the stray inductance, like the shunt resistor and current measurement methods [17].

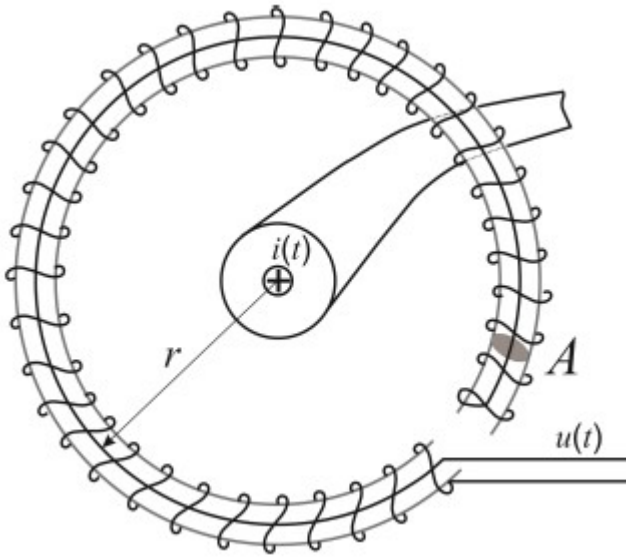


Figure 3.4: Circular Rogowski coil [4]

The operation of a Rogowski coil is based on the Faraday's Induction law [17]. According to [20], the value of this voltage is given by:

$$V_{ind} = -\sum_{i=1}^{N} \frac{d\Phi}{dt} = -M \cdot \frac{di}{dt}, \tag{3.2}$$

where N is the number of the turns of the coil and M is the mutual inductance between the conductor of the current and the coil that is placed around it. Assuming that the magnetic flux will be equal at every turn of the coil, its value is given by:

$$M = \frac{N}{l} \cdot A \cdot \mu_0, \tag{3.3}$$

with l being the total length of the coil, A the area that is enclosed within a single turn and $\mu_0 = 4 \cdot \pi \cdot 10^{-7}$ the magnetic constant.
One of the disadvantages of this method is that the protection circuitry do not react in low di/dt. This results in overcurrents which will be detected by the integrated desaturation protection of the gate driver IC. Another drawback of the Rogowski coil protection is the need for an integrating circuitry, to retrieve the value of the current.
After integrating the signal, it is compared with a threshold value, which refers to a di/dt for a normal turn-on of the power switch, so when the integrated signal exceeds this value, a turn-off

signal is sent at the gate of the power semiconductor. As for the integration of the signal at the output of the coil there are two ways to integrate it:

1. Passive integration, using passive RC components
2. Active integration, using an operational amplifier (Op-Amp) along with passive components

Passive integration
A passive integrator circuit is shown at the figure below.

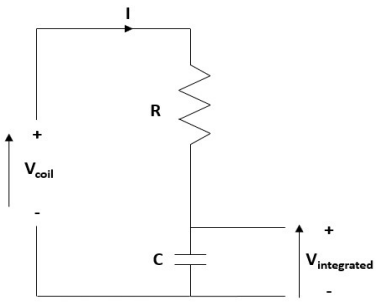


Figure 3.5: Passive integrator circuit

As can be seen on Figure 3.5 the input voltage of the circuit is the output voltage of the coil. Following Kirchhoff's law for this circuit the following relationship is obtained:

$$I = \frac{V_{coil} - Vintegrated}{R} \tag{3.4}$$

As it is known the current that flows through the capacitor is given by:

$$I_C = C \cdot \frac{dV_{integrated}}{dt} \tag{3.5}$$

The combination of Equations 3.4 and 3.5 results in:

$$C \cdot \frac{dV_{integrated}}{dt} = \frac{V_{coil} - Vintegrated}{R} \tag{3.6}$$

Selecting proper values for R and C, keeping the ratio R/C high enough, it can be assumed that $V_{coil} - V_{integrated} \approx V_{coil}$. Eventually, the Equation 3.6 becomes:

$$\frac{dV_{integrated}}{dt} = \frac{V_{coil}}{R \cdot C} \Rightarrow V_{integrated} = \frac{1}{R \cdot C} \cdot \int V_{coil} dt \tag{3.7}$$

Active integration

In Figure 3.6 an active integration circuitry is presented:
The configuration of Figure 3.6 is called *Inverting Integrator*, with the positive terminal of the output of the coil being connected to the negative input of the Op-Amp and the negative terminal (ground) being connected to the positive input. This configuration is selected to neutralize the minus sign at the Equation 3.2.
The mathematical analysis of the circuit is based on the concept of the *Virtual Ground*, which is explained in [21]. According to this, the two inputs of the amplifier is assumed to have the same voltage value, without being short-circuited. This means that:

$$V_+ \approx V_- = 0 \tag{3.8}$$

Taking into consideration the equation above, the currents of the circuit are described by the following relationships:

$$I_{in} = \frac{V_{coil}}{R_{in}} \tag{3.9}$$

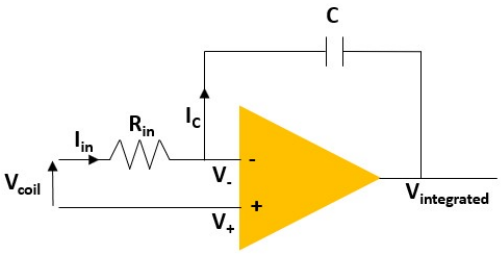


Figure 3.6: Active integrator circuit

$$I_C = C \cdot \frac{dV}{dt} = -C \cdot \frac{dV_{integrated}}{dt} \tag{3.10}$$

Considering that the Op-Amp is ideal, meaning there is no current that flows through it, the two currents I_{in} and I_C are equal. This means that:

$$I_{in} = I_C \Rightarrow -C \cdot \frac{dV_{integrated}}{dt} = \frac{V_{coil}}{R} \Rightarrow V_{integrated} = -\frac{1}{R_{inw} \cdot C} \cdot \int V_{coil} dt \tag{3.11}$$

As can be seen at Equation 3.11, the output signal has the opposite polarity to the input one, proving mathematically the *Inverting Integrator* that was analysed before.

3.5 Leg Voltage Measurement

The last detection method that was examined, is proposed in [8] for protecting GaN HEMTs. The basis of this method is the measurement of the leg voltage of the switch, which can be named V_m. Under normal operating conditions and with V_{dc} being the input voltage V_m=V_{dc}. In case of a short-circuit there is a voltage dip across the leg, reducing the value of V_m. The voltage drop is caused by the sudden increase of the leg current, with all the parasitics like the stray inductances of the power device or the PCB.
It is clear that the higher the value of the parasitics the larger the dip at V_m, with the stray inductance of the PCB influencing it the most. At the simulation results of [8] was shown that for a value of L_{PCB} at 1.7 nH there is a voltage dip of 30 V, when the V_{dc} was 400 V.

3.6 Method Selection

For selecting the most appropriate method the disadvantages of each one of them were summarized. Starting with the de-saturation, this is a method that:

- needs the blanking time for non false triggering, i.e. 0.5 - 1 μs,
- has a very complex design for SiC MOSFETs, because stronger dependence on the on-state voltage compared with the IGBTs.

The second way to protect the power module was by using a shunt resistor. As it was analyzed at the corresponding paragraph, due to the major drawbacks, especially for high power applications, this method is deemed inappropriate and will therefore not be selected. Thirdly, a current transformer method was investigated. The drawbacks for this method are:

- the possible saturation issues in case of large current
- the inserted stray inductance, increasing the ringing phenomena during the switching transitions and deteriorating the circuit performance [17].

The alternative for this is proposed to be a di/dt measurement method, using a **Rogowski coil**.This method neutralizes the two issues using a current transformer, but there are also some drawbacks when using it, for instance:

- the need of an integration circuit, making the design slightly more complex
- the possibility of non-triggering in case of low di/dt

Finally a voltage measurement of the leg of the switch method was examined. Although it was proved to be a very fast and efficient protection method, it was tested only on GaN HEMTs.
Eventually, the di/dt measurement method using Rogowski coil is selected, because its drawbacks either do not influence the circuit performance or even if they do this influence can be mitigated. More specifically, the integrating of the signal can be very fast by selecting the appropriated components. At the same time, the non-triggering possibility is minimized, by selecting a gate driver IC with integrated de-saturation protection, that will detect and react in this case. Furthermore, the use of an air-gaped Rogowski coil ensures the galvanic isolation of the components that constitute the signal processing circuitry.

3.7 Coil Design

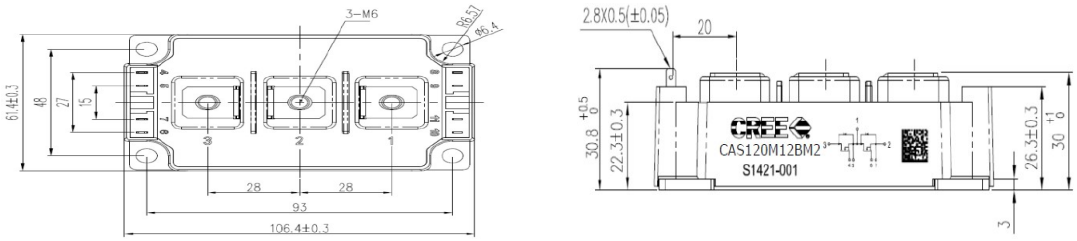
3.7.1 Step 1. Shape and size of the coil

After selecting the protection scheme, the next step is the design of the Rogowski coil. The coil will be implemented on a PCB board, with the KiCad program being used for its design [22]. The most dominant factor for this design are the limitations because of the shape and the dimensions of the power switch that is to be protected.

(a) (b)

Figure 3.7: SiC module overview (a) and pins configuration (b) [5]

The power module of Figure 3.7 will be used for this project. According to Figure 3.7b, the current will flow from pin 3 to pin 2, with its direction being shown at 3.7a. Based on this figure, two custom made window-shaped Rogowski coils that will be built around the pins 2 and 3, will efficiently protect the power module.
The next step of the design is based on the dimensions of the module, which are taken from the datasheet of the manufacturer[5]. From this, the size of the window opening will be determined, where the two pins (2 and 3) will be placed in.



(a) (b)

Figure 3.8: Top view dimensions (a) and side view dimensions (b) [5]

As it can be seen on Figure 3.8, all the dimensions are not given. More specifically, the sides of the pins 2 and 3, which are necessary for defining the size of the opening of the window. These dimensions were taken by a direct measurement on the module. The minimum required opening dimensions are presented on Table 3.1.

Table 3.1: Rogowski coil window opening dimensions

Parameter	Size
Coil horizontal opening	20 mm
Coil vertical opening	23 mm

3.7.2 Step 2. Winding configuration

Rogowski coils are devices with high noise sensitivity. Besides all the small turns of the coil, a large one turn loop is created with its start being the start point of the coil and its end the end point [20], [23], [24]. This results into inducted voltages to the coil in case of conductors carrying currents on the horizontal plane of the coil. For neutralizing this undesirable effect, a return loop must be added to counterbalance the positive magnetic field with an equal negative one.
The second requirement originates from the assumption is made for extracting the Equation 3.3. According to this,the magnetic flux at every turn of the coil is the same. To satisfy this assumption, the winding must be as similar as possible.
The next target is the mitigation of the measurement error in case the current conductor is not placed exactly in the middle of the coil. Since the positions of the coil and the module will be fixed it is not that possible, but even a small disposition may lead to a significant error. Eventually, four extra turns are added, one at each corner, in order to reduce measurement errors [20].

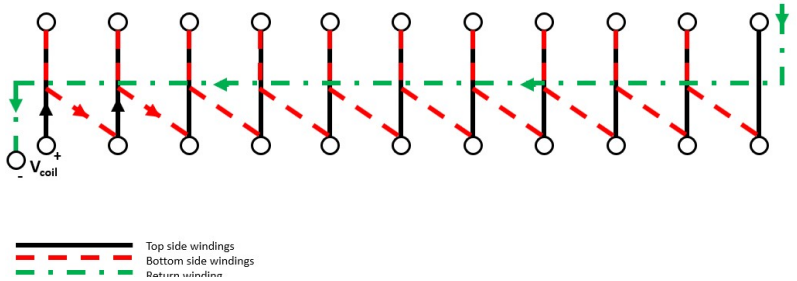


Figure 3.9: One side winding configuration

3.7.3 Step 3. Number of turns

The next step of the design is the calculation of the number of turns. The higher this number is, the better measurement accuracy the coil will have. On the other hand, the self-inductance (L_c) and capacitance (C_c) are increased, decreasing the bandwidth of the coil.

$$\omega_0 = \frac{1}{\sqrt{L_c \cdot C_c}} \tag{3.12}$$

The advantages of the increased number of turns overpass this disadvantage, thus their maximization will be attempted. This is limited by three factors:

- the clearance requirements on the PCB
- the width of the conductor

- the size of the coil sides

Starting with the first bullet, the clearance is defined as the minimum distance between two conductors. This distance is dependent on the difference of the voltage of these two conductors. According to Table 6.1 of IPC-2221A [25], and taking into consideration that the voltage will be only a few volts, result in the clearance requirements of the application being at 0.1 mm.

The second parameter is the width of the conductor, which is related with the current that

Table 3.2: Clearance requirements for uncoated external conductors

Voltage Between Conductors (DC or AC peaks) (V)	**Clearance (mm)**
0-15	0.1
16-30	0.1
31-50	0.6
51-100	0.6

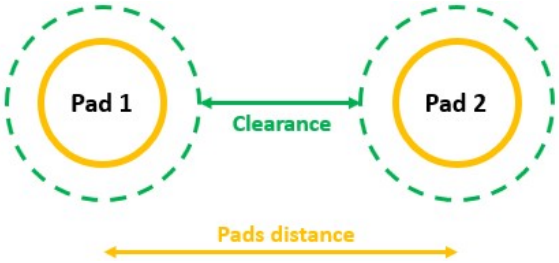


Figure 3.10: Clearance distance of pads on PCB

flows through it.According to Figure 6.4-A of [25], the width of the traces, which eventually will compose the windings of the coil, will be 0.1 mm.
Moving to the last bullet, besides the window opening, there are also some geometrical limitations. Ideally, the two coils must be identical, resulting in the same base analysis as well. At the same time there should be no overlap between their windings.
Eventually, the number of turns will be in total 269, with increased winding density at the corners. Figure 3.11 shows all the dimensions of the designed coils.

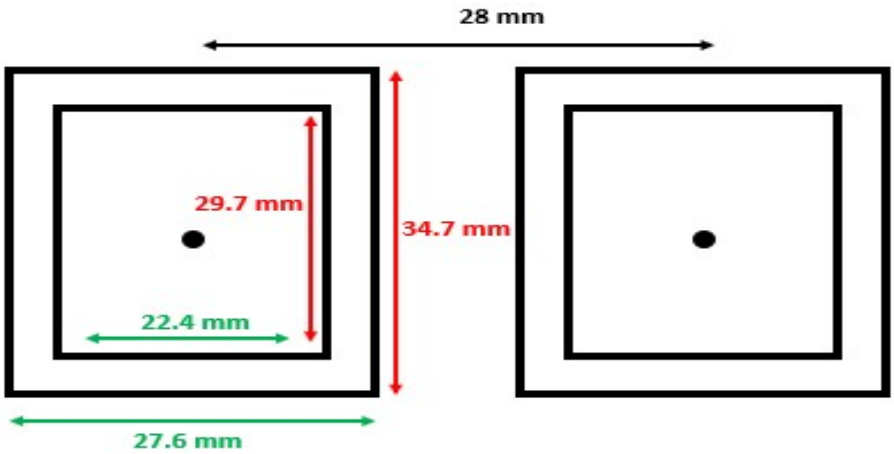


Figure 3.11: Dimensions of the designed coil

4 | High-Voltage Gate Drivers

In this chapter, the role of the gate driver at a power application will be explained. Furthermore, parameters that need to be taken into consideration for the design of the gate driver, will be analyzed as well. The gate driver design includes different subsystems which are:

- the communication with the microcontroller
- the selection of the gate driver IC
- the design of the signal processing circuit
- the design of the power supply system

4.1 Gate Driver Role

All the power applications operate according to the microcontroller ~~is~~ used. It could be said that the microcontroller is the brain of the application. On the other side, the signals a microcontroller produces are control signals without having the ability of driving a power switch. For achieving the amplification of the control signal a gate driver is used, being practically a power amplifier which converts the control signals into power signals.

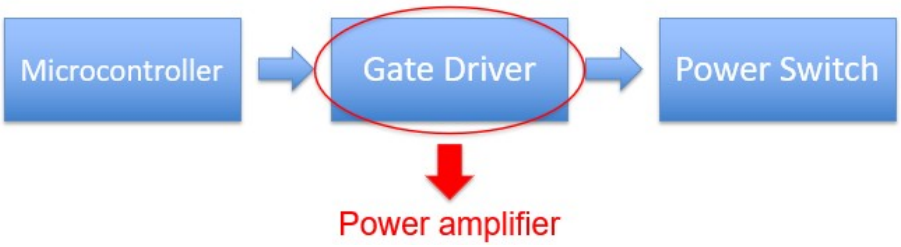


Figure 4.1: Power semiconductor driving steps

As it can be seen in 4.1, the output of the gate driver is the input of the semiconductor. Depending on the material of the switch, the appropriate voltage levels will be created for the on ($V_{positive}$) and the off ($V_{negative}$) states. For the case of wide bandgap materials, the $V_{negative}$ will have a value lower than zero (usually -5V) to prevent a false trigger of the switch, while the $V_{positive}$ depends on the material(at least 4V for GaN devices and 15V for SiC devices).

4.2 Gate Driver Design

The next step of the project is the design of the gate driver. The power needs were analyzed above. The noise immunity was selected based on the switching times of the power device that will be tested [5]. The requirements for this design are presented:

Table 4.1: Gate driver requirements

Driving voltage levels	$V_{negative} \leq$ -5V and $V_{positive} \geq$ 15V
Driving current peak value	$\geq$ 20A
Isolation level	$\geq$ 1.2 kV
Noise immunity	$\geq$40 kV/μs

The range of the voltages is selected to ensure sufficient drive capability for the module. The same principle applies for the current, with its minimum value being selected at 20 A. This is not the maximum average current the gate of the power module will be driven with, but the amplitude of a current pulse with its duration being equal with the switching transition time. As for the isolation level, it should be much higher, e.g. 5 times higher than the highest voltage the module can operate at. The noise immunity level selection was based on the voltage produced dV/dt during the switching transitions. According to [5], with an applied testing voltage of V_{dc}=600 V, the switching times of the module are t_{on}=34 ns and t_{off}=22 ns. The shortest turn-off time will cause worse EMI issues, with the voltage over time ratios being 17.65 kV/μs and 27.27 kV/μs for turn-on and turn-off respectively. Thus, to be at the safe side a value like of 40 kV/μs, was selected as the noise immunity barrier.

4.2.1 Communication with the microcontroller

The first stage of the operation of a gate driver is to receive the signal from the microcontroller. This connection will be established using the optic fibers of [26]. Optic fibers satisfy both isolation and noise immunity requirements.
In total 3 different transmitter-receiver pairs are used. Two of them are used for sending the PWM signals from the microcontroller one for each power switch of the module. These signals will be processed before being driven into the input of the gate driver IC. The last pair is used for sending the detected fault signal back to the microcontroller.

4.2.2 Gate driver selection

Besides the requirements of Table 4.1, it is desirable for the gate driver to have an extra over-current protection in case the designed protection, which is described in the previous chapter, does not detect the fault. Additionally, features like under-voltage lockout (UVLO) or Miller clamping are desired for a more qualitative operation of the driver. The UVLO will prevent the insufficient voltage supply at the output of the IC, while the Miller clamp prevents a false turn-on of the power device, which can be destructive for it.
The aforementioned desired features can be satisfied by selecting an integrated circuit (IC) for the gate driver, instead of building it with low power components. The extra over-current protection scheme in all of the modern ICs use the desaturation technique for fault detection, while most of them offer UVLO and Miller clamp of the output. The main characteristics that the selection of the IC was based on are:

- low propagation delays
- low rise and fall times
- fast short-circuit protection

Eventually, the IC that was selected is the ACPL-344JT produced by the Avago Technologies [27]. It provides a voltage isolation level of 5 kV (rms value), with the low and the high side being connected through optocouplers. Its key characteristics are presented at the following table, with Common Mode Rejection (CMR), being the equivalent of the noise immunity that was set as a requirement above.

Table 4.2: ACPL-344JT operating features

Part No	**Output Voltages**	$\mathbf{I_{output}}$	$\mathbf{t_{propagation}}$	$\mathbf{t_{rise}}$ $\mathbf{t_{fall}}$	$\mathbf{t_{desat}}$	**CMR**	$\mathbf{C_{parasitic}}$
ACPL-344JT	-10V $\leq V_{negative} \leq$ 0V 15V $\leq V_{positive} \leq$ 25V	2.5A	150 ns	70 ns 50 ns	600 ns	50 kV/μs	1.3 pF

As can be seen on Table 4.2, the current output is inadequate, being much smaller than the target value of 20 A. For providing sufficiently high gate current a low power MOSFET in a totem-pole configuration is used. According to [28], the maximum value of a current pulse is 22.2 A, which satisfies the initial requirement.

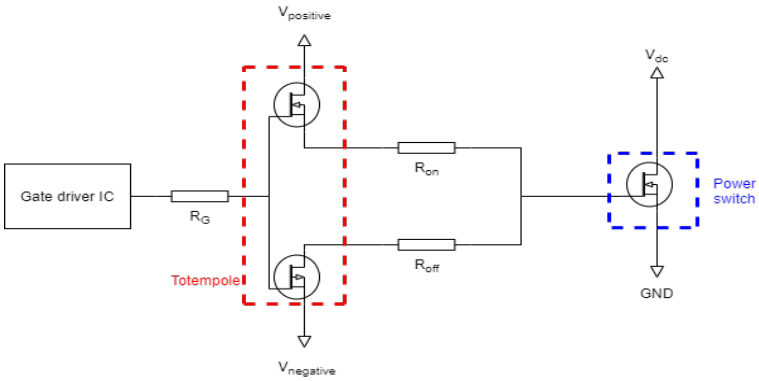


Figure 4.2: Totem-pole configuration for current boosting

4.2.3 Signal process circuit

The process of the signal received by the Rogowski coils is also a part of the gate driver's operation. It is composed by two subsystems which are:

- the integrator circuit
- the reaction circuit

Integrator selection

The first subsystem is the integrator circuit. For the integration of the output voltage of the coil the active integration method will be used. There are two benefits of using an operational amplifier for integrating the signal compared with the passive integrating method, which are:

- the wider bandwidth
- the amplification of the voltage signal

The bandwidth of the constructed coil is determined by two factors:

- the resonance frequency from Equation 3.12, which defines the upper bandwidth limit
- the type of the integrator, which influences the lower bandwidth limit

In the case of using a passive integrator, the lower bandwidth is the RC cut-off frequency. On the other hand, when an operational amplifier is used, the lower bandwidth is caused by the non-ideality of the active integrator configuration [29].
Besides the bandwidth, there is an additional benefit of using an Op-Amp, which is the better control of the integrated signal, by controlling the closed gain loop of the circuit. As for the selection of the values of the components R_{in} and C 3.6, it was made after the proper tuning of the integrator and was based on the non-ideal model of the Op-Amp, with a resistor being connected in parallel with the capacitor. As is referred in [29], this resistor is an intrinsic resistor of the amplifier's IC, with its value being a few megaohms. To control the value of this resistor an external resistor was connected in parallel. This control is very important, because the value of this resistance highly influences the DC gain of the integrator.

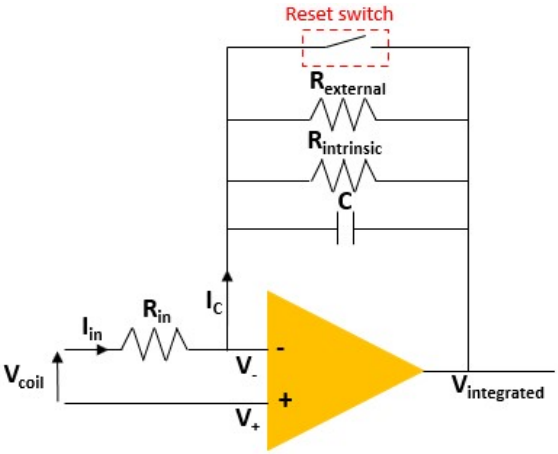


Figure 4.3: Non-ideal active integrator model

A low power switch is connected in parallel with the capacitor, otherwise when the PWM signal would be LOW, the output of the integrator would get negative, affecting the measurement and inserting an error [29]. The reset switch will be on when the power module is off and off on the other way around.

Reaction system

The reaction subsystem has one basic requirement: The quick response in case of fault. There are two inputs at this subsystem, which are the output of the integrator and the threshold voltage. When the first exceeds the value of the second then the system will be triggered. In any other case, which indicates that the system operates under normal conditions, no action is needed. As for the output of the system it is driven into the gate of the switch and is sent back to the microcontroller using an optic fiber.

On Figure 4.4, the reaction circuit is presented along with the 7 different components that compose it. These are:

- two operational amplifiers
- two D type latches
- two AND gates with 3 inputs each and
- one OR gate

The operational amplifiers compare the integrated signals from the Rogowski coils with the threshold value. Their output is driven into the D input of the latch flip-flops.

Table 4.3: D latch truth table

D	**CLK**	**R**	**Q**	$\overline{Q}$
X	X	1	0	1
X	0	0	Latch	Latch
X	1	0	Latch	Latch
0	⌐↓	0	0	1
1	⌐↓	0	1	0

As can be seen on Table 4.3, if the level enable (LE) input of a D latch is not HIGH, then its

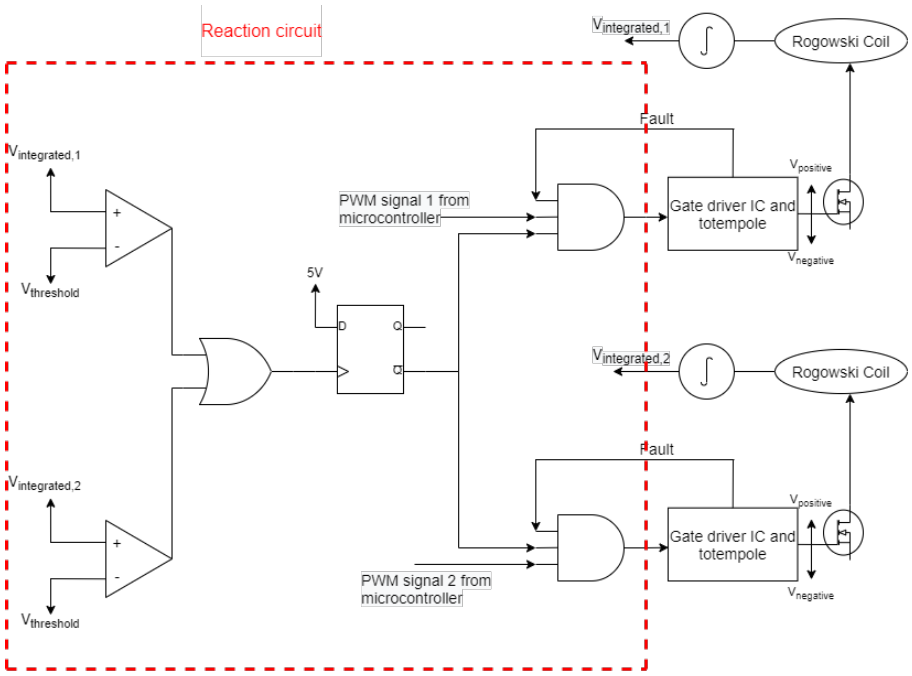


Figure 4.4: Reaction circuit

outputs will be latched. For the output Q following the input D, the LE must be HIGH. At the reaction circuit of Figure 4.4, the LE is connected with $\overline{Q}$ output, meaning that in normal operating conditions the input D is low, while the outputs Q and $\overline{Q}$ are LOW and HIGH respectively. In case of a fault, the signal of D will be HIGH, turning $\overline{Q}$ into LOW. As a result, the output of the 3-input AND gate will become LOW, a signal that is sent to the gate driver which turns off the device. At the same time, the fault signal is sent to the microcontroller through the OR gate.
There are two more inputs at the AND gates of Figure 4.4. The one is the PWM signals, that are received from the microcontroller. The second one is the $\overline{F}$ signals from the integrated desaturation protection of the gate driver. This will be activated in case of a fault with low di/dt and as was described above will turn off the device.

4.2.4 Power supply

The power supply subsystem is responsible for the creation of the voltages that will be applied at the gates of the switches of the power module. At the same time its characteristics must respect the requirements of Table 4.1.
The generation of the predefined voltages is designed with multiple components working together, as is presented on Figure 4.5. Two ICs, the oscillator and the gate driver, and a center tapped power transformer are used.
The oscillator is an analog device which produces a digital PWM output signal, which has a fixed frequency. The frequency value is controlled by the input pin SET of the IC and the value of the resistance that is connected to it (R_{SET}). According to [30] the frequency will be given by:

$$f_{out} = \frac{1MHz}{N_{DIV}} \cdot \frac{50k\Omega}{R_{SET}} \tag{4.1}$$

The N_{DIV} is an internal frequency divider which is defined to be one. The duty cycle (D) of the PWM signal is controlled by the MOD input pin of the IC. The value of this pin ranges from 0.05 to 0.95, producing an output signal with its duty cycle being between 5% and 95%.
This output signal is driven into the input of a gate driver, since it needs to be converted into

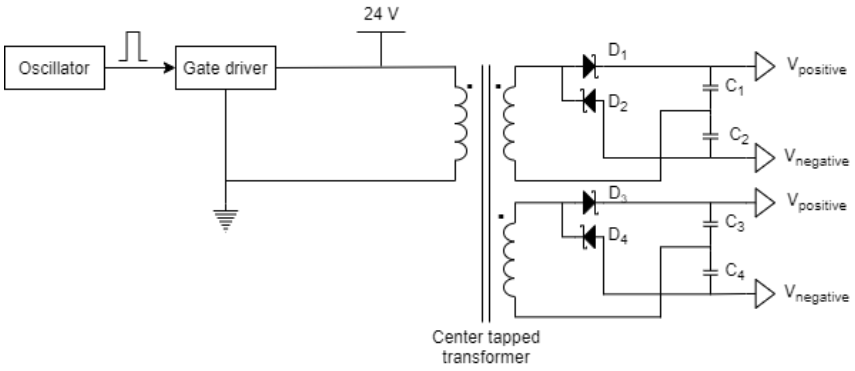


Figure 4.5: Generation of voltage supply

a voltage signal. This gate driver is the UCC27533 which is a 5-pin gate driver IC, having the simplest form. After the gate driver the PWM signal is a voltage signal with its value being either 0 or 24 V.
The aforementioned voltages are driven into a center tapped transformer, the T60403-F4099-X011 from VACUUMSCHMELZE [31]. The transformer has a parasitic coupling capacitance which is given by the manufacturer at 2.5 pF. At the same time the isolation requirement of 1.2 kV is satisfied, protecting also the other two components. When the output of the gate driver is 24 V, the upper diodes D_1 and D_3 are conducting charging the upper capacitors C_1 and C_3 with 24 V for a time interval $t_{up} = \frac{D}{f_{out}}$. The remaining time of the oscillator's switching period, the output of the gate driver is 0 V and the lower pair of capacitors are charged, creating the negative bias voltage.
Since the input of the transformer is 24 V, the algebraic summary of the $V_{positive}$ and $V_{negative}$ will be 24. To satisfy the requirements of Table 4.1, the two voltages were selected to be 19 V and -5 V.
Taking into consideration all the previous analysis and the instructions from the [30] as well, a voltage divider was connected with the ratio of the resistances being given by R_1/R_2=V_1/V_2.

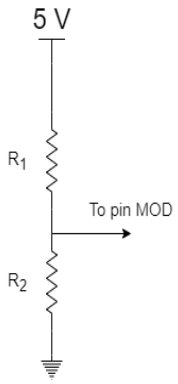


Figure 4.6: Input of the MOD pin

4.2.5 Design summary

All the previous analysis is summarized in Figure 4.7 and 4.4, where the schematic of the gate driver is presented and the role of each component is briefly described.

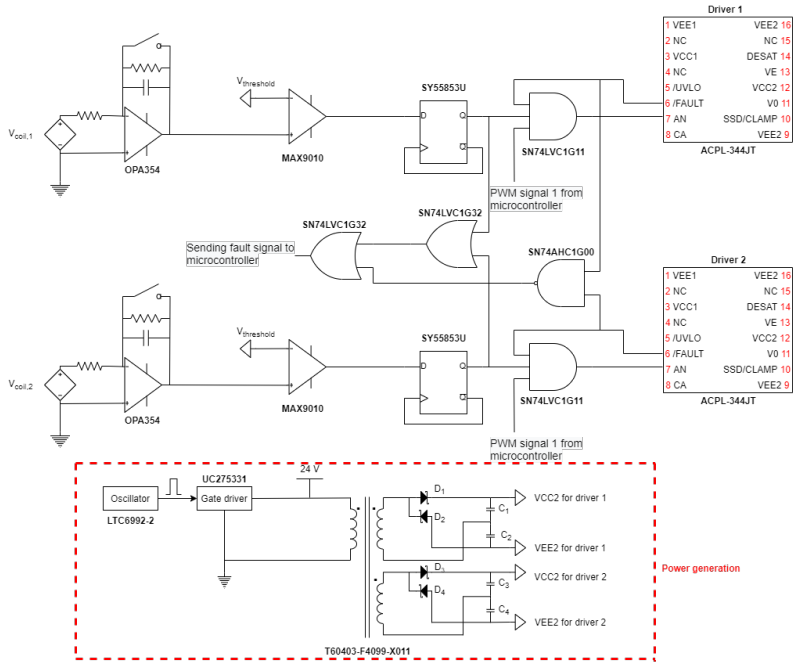


Figure 4.7: Gate driver circuit

Table 4.4: Gate driver components

Component	Part No	Role
Gate driver IC	ACPL-344JT	Amplifying the control signals for driving the power module
Totempole	ZXMC4559DN8	Boosting the current flowing to the gates of the power switches
Operational amplifier	OPA354	Wide bandwidth Op-Amp used for integrating the coil signals
Low power p-MOSFET	BSS84P	Reset the output of the integrator resulting in the correction of measurement errors
Operational amplifier	MAX9010	Fast comparing the integrated signal with the threshold value
D-latch	SY55853U	Control of the transition from the normal operation to fault situation
AND gate	SN74LVC1G11	Control of the PWM signal is sent to the gate driver IC
NAND gate	SN74AHC1G00	Checking if there is a fault detected by the integrated protection of the gate driver IC
OR gate	SN74LVC1G32	Checking if a short-circuit has been detected from the Rogowski coils
OR gate	SN74LVC1G32	Checking if there is a fault in the system and sending the signal at the microcontroller
Oscillator	LTC6992-2	Creating the control signals for generating the bias voltages
Gate driver IC	UCC27533	Converting the control signals of the oscillator into voltages
Center tapped transformer	T60403-F4099-X011	Creating the targeted voltage levels

5 | Simulation Results and PCB Design

For validating the theoretical assumptions and the correctness of the operation of the gate driver simulation models were developed. Subsequently, the design of the Printed Circuit Board (PCB) was implemented. At this chapter it will be presented:

- simulation codes and models with the results
- circuits and footprints from the PCB design

At the first paragraph of this chapter the equivalent electrical circuit of a Rogowski coil will be presented and analyzed. At the second step the way to determine the optimized value of the damping resistor which is connected in parallel at the output of the coil will be shown.

5.1 Rogowski Coil Equivalent Circuit

The Rogowski coil can be depicted as an electrical circuit driven by a dependent voltage source, with the value being $M \cdot di/dt$. Every turn of the coil has its self-inductance, resistance and self-capacitance, creating a circuit like the one of Figure 5.1, with N being the number of turns of the coil.

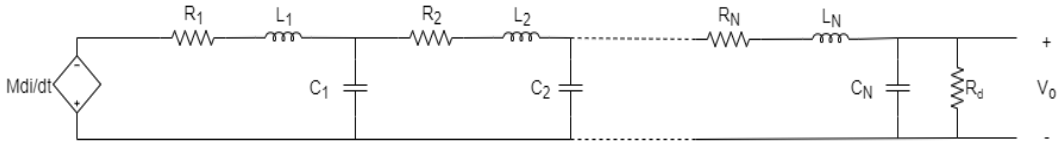


Figure 5.1: Rogowski coil distributed model

These parasitic inductances and capacitances create N number of resonances, with the value of each one of them given by 3.12. During normal operation the Rogowski coil is used below the first resonant frequency, thus the distributed model can be simplified to a lumped model [17],[20].

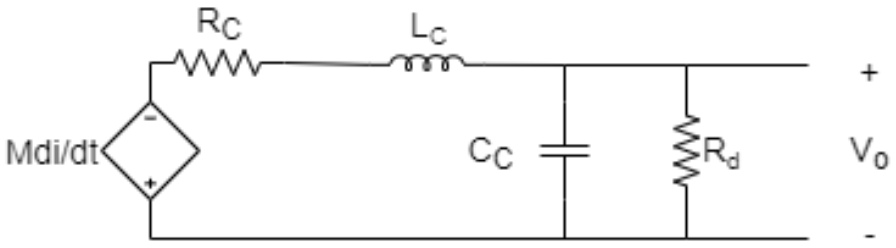


Figure 5.2: Rogowski coil lumped model

At the Figure 5.2 the R_C, L_C and C_C represent the ohmic resistance, self-inductance and capacitance of the coil respectively, while R_d is the external damping resistance.

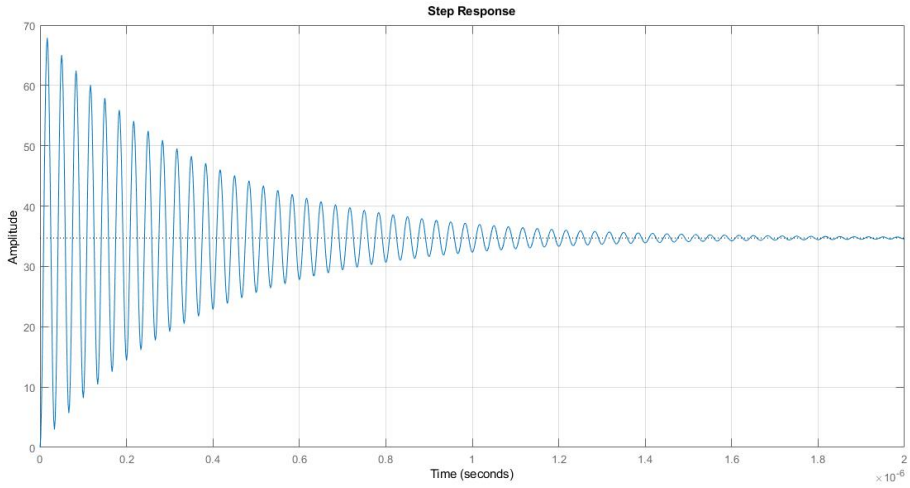
5.2 Determine the Optimized Value of R_d

At this stage of the project two questions were set to be answered. These were:

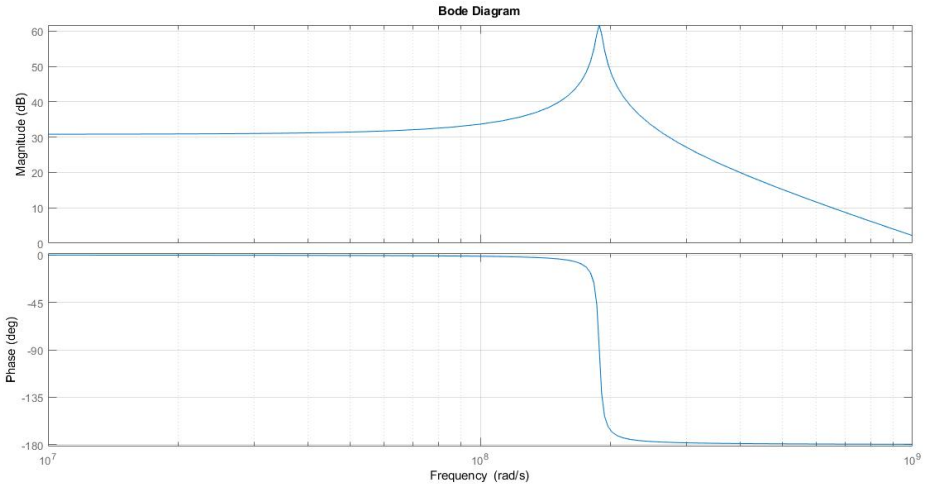
- Is the damping resistance that important for the operation of the coil?
- and if yes, What is its optimal value for achieving maximum detection efficiency?

For answering the first question, the extraction of the transfer function in case there is no damping resistance is necessary. Based on Figure 5.2, ignoring the R_d the transfer function of the undamped system is:

$$H_{undamped}(s) = \frac{V_o(s)}{di/dt} = \frac{M}{s^2 \cdot L_c \cdot C_c + s \cdot R_c \cdot C_c + 1} \tag{5.1}$$



(a)



(b)

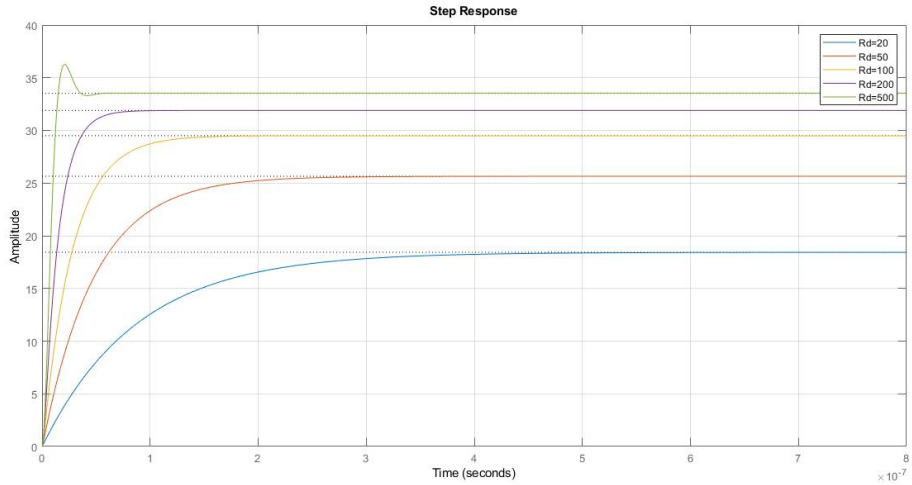
Figure 5.3: ((a) Step response; and (b) Bode diagram without using damping resistor

As can be seen on Figure 5.3a the output of the coil gets stabilized after a few microseconds. The slow output response renders the use of a damping resistor necessary. When the damping resistor is included in the analysis the transfer function is a little more complicated as it is shown below:

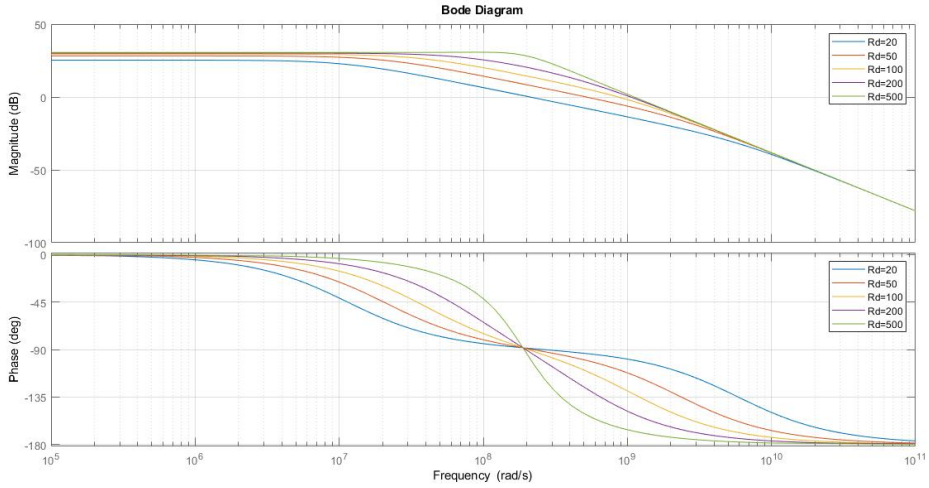
$$H_{damped}(s) = \frac{V_o(s)}{di/dt} = \frac{M}{^2 \cdot L_c \cdot C_c + s \cdot (R_c \cdot C_c + \frac{L_c}{R_d}) + (1 + \frac{R_c}{R_d})} \tag{5.2}$$

Correspondingly the step response and the Bode diagram, for five different values of R_d are

presented.



(a)



(b)

Figure 5.4: (a) Step response; and (b) Bode diagram for five different values of damping resistance

As it can be seen in both figures of 5.4 the value of the resistance with no damping oscillations is around 200 Ω, showing fast output response, following the input within some tens of nanoseconds. For faster response, a higher R_d value could be selected, trading off part of the measurement accuracy of the coil.

5.3 Rogowski Coil Model

Following the model from Figure 5.2, a Simulink model was built for simulating the operation of the Rogowski coil.

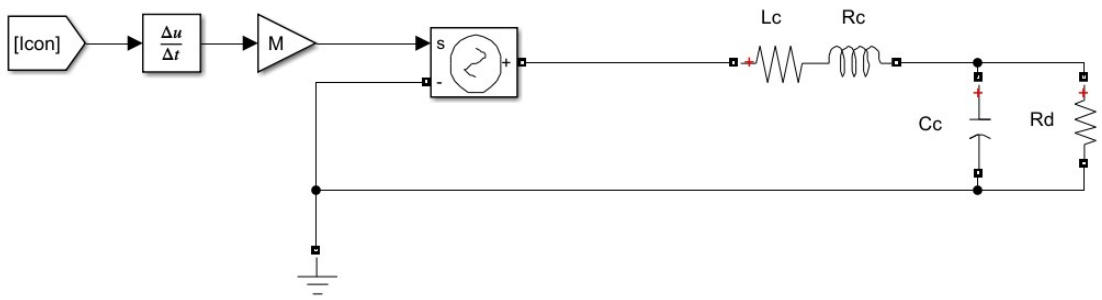


Figure 5.5: Rogowski coil Simulink model

On Figure 5.5 the input of the coil has been attributed as a controlled voltage source. The control signal of this source is the ratio of the current over time, multiplied with a gain M, which is the mutual inductance of the coil.
Two different current inputs were created, one for the normal turn-on of the module and one for a short-circuit case. For the normal turn-on the data from [5] was used for a transition up to the nominal value of the current.

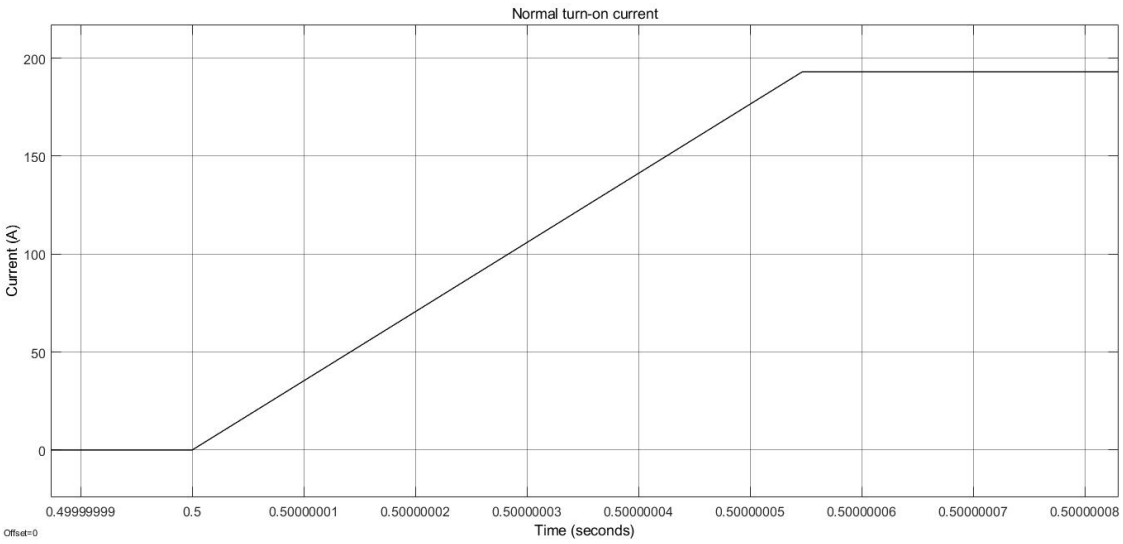


Figure 5.6: Current transition during a turn-on procedure

For the short-circuit case it is considered that initially the value of the current was 193 A. When a short-circuit happens, it is the stray inductance between the two terminals of the module that causes the high current slope. Supposing an ordinary operating voltage value being 800 V, with the value of the stray inductance being 15 nH, the current will rise dramatically with its slope being 53.3 kA/μs.
The difficult part of the simulations was the approximation of the values of the lumped parameters of the Rogowski coil. From the Equation 3.3, the two parameters that are missing for calculating the mutual inductance are the length of the coil and the cross-section of a winding.
Following the mutual inductance the next parameter that needed to be calculated was the self-inductance. There are no available formulas for calculating directly the inductance value of a window type coil with rectangular cross section. Thus, a holistic approach was decided for solving this problem.
The voltage of a coil is given by:

$$V_L = L \cdot \frac{di}{dt} \tag{5.3}$$

According to Faraday's law of induction the voltage is given by:

$$V = -N \cdot \frac{d\Phi}{dt} \tag{5.4}$$

The minus signal of Equation (5.4) denotes only the Lenz's law and will be neglected. As for the magnetic flux flowing through an area A of this equation it is equal to:

$$\Phi = B \cdot A = \frac{\mu_0 \cdot I}{2 \cdot \pi \cdot x} \cdot A, \tag{5.5}$$

where x is the distance from the measurement point of the magnetic flux with the current conductor. Considering the cross-sectional area of the turns being equal, the only parameter that does not have a fixed value is the distance x, since the ratios of the currents will be removed. Thus, the total magnetic flux of the coil will be $\Phi_{total} = \Phi_1 + \Phi_2 + ... + \Phi_N$, where Φ_1 is the flux of turn 1, Φ_2 is the flux of turn 2 etc. Their values are given by:

$$\Phi_i = \frac{\mu_0 \cdot h}{2 \cdot \pi} \cdot ln(\frac{outer_i}{inner_i}), \tag{5.6}$$

Eventually, the self-inductance of the coil will be given after combining the Equations (5.3) and

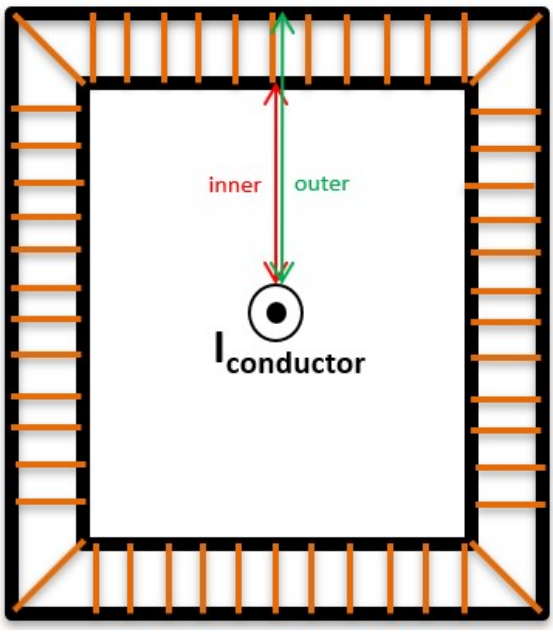


Figure 5.7: The distances for the measurement of the self-inductance

(5.4) as:

$$L = N \cdot \Phi_{total} \tag{5.7}$$

Eventually, the mutual and the self-inductance are calculated M=9.834 nH L_c=3.43 μH. and all the calculations are presented in Appendix A. As for the value of the AC resistance of the coil at a frequency of 10 MHz, both [32] and [33] returned values around 17 Ω
The last parameter that needed to be defined was the parasitic capacitance of the windings of the coil. This is taken from the Equation 3.12, with the resonance frequency of the coil being approximated at 30 MHz. Although this approximation is theoretically arbitrary, it reflects a typical bandwidth limit of similar constructed PCB Rogowski coils printed on PCB. Furthermore, the target of this simulation was to observe the voltage signal at the output of the coil, with its value being influenced only by the values of the resistance and the inductance.

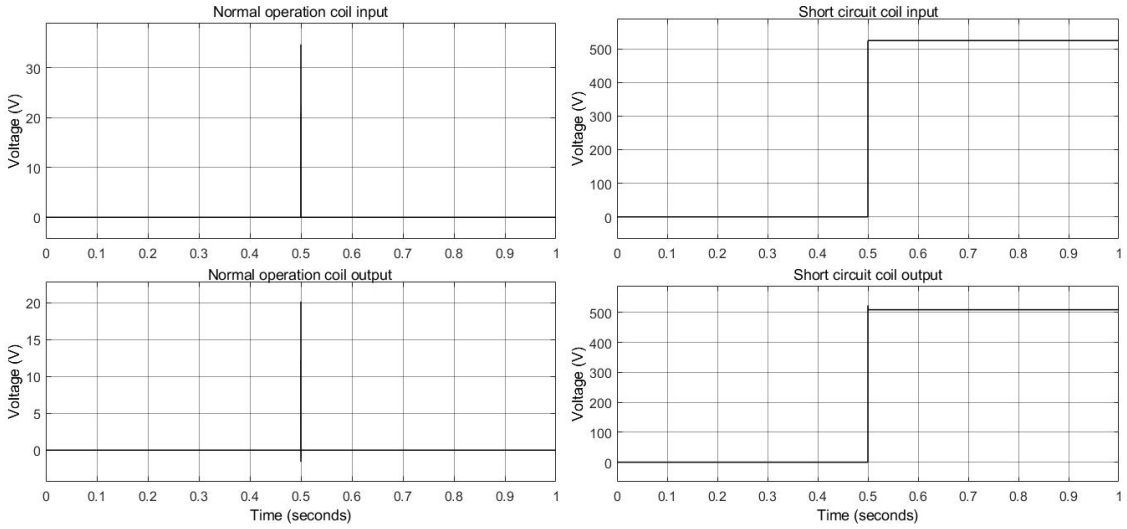


Figure 5.8: Voltage signals of the coil during both normal turn-on and short-circuit cases

As it can be seen on Figure 5.8 during a normal turn-on the voltage of the coil looks like a Dirac delta function, while in the case of a short-circuit it looks like a step function. These two output signals will be driven into the integrator, which is the next simulation model that was developed.

5.4 Active Integrator Model

As can be seen on Figure 5.8, the output signal of the coil during a normal turn-on transition, can be characterized as a delta function. Integrating this type of signals may result in an inadequate value to be recognized by the comparator. For that reason, a simulation model was developed for making clear if there is the need for an extra signal amplifier after the integrator. The model that was built on Simulink is presented below:

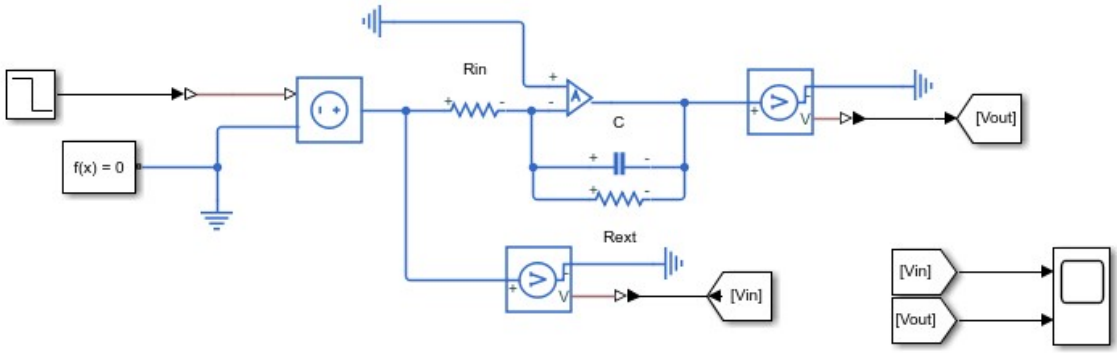


Figure 5.9: Simulink model of active integrator

According to [34], a typical value of the gain of the amplifier that was selected for the application is 110 dB, and it was also the value that was inserted at the simulation model. The external resistance represents the intrinsic resistance of the amplifier that is not taken into consideration at the component's block. Different values of the components were tested to make clear the level each of them influences the operation of the integrator.

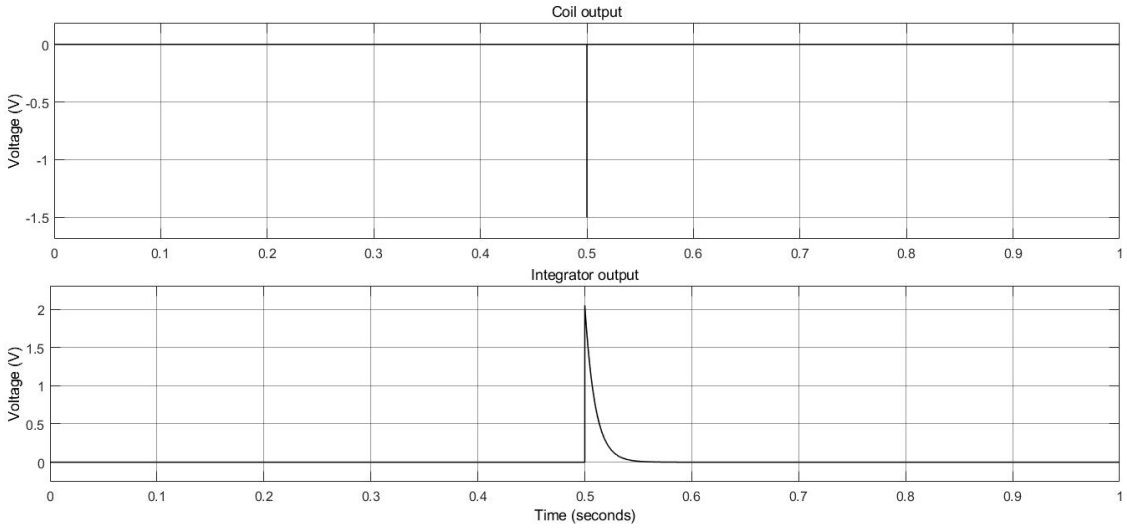


Figure 5.10: Input and output integrator voltages for R_{in}=200 Ω, C=200 pF and R_{ext}=200 MΩ

The inverting configuration is proved on the Figure 5.10, with the coil voltage being negative and the output of the integrator positive. The value of this voltage during the turn-on will give the guidance for selecting the reference value of the comparator. This signal must be adequate for being recognized from the comparator, otherwise it will not function properly. As it can be seen on Figure 5.10, the output voltage reaches a value slightly larger than 1 V, which is sufficient.
The integrator must be properly tuned, so its function will be according to the requirements which are set depending on the application. To realize the direction that should be followed for this tuning the values of the components of the integrator were altered.

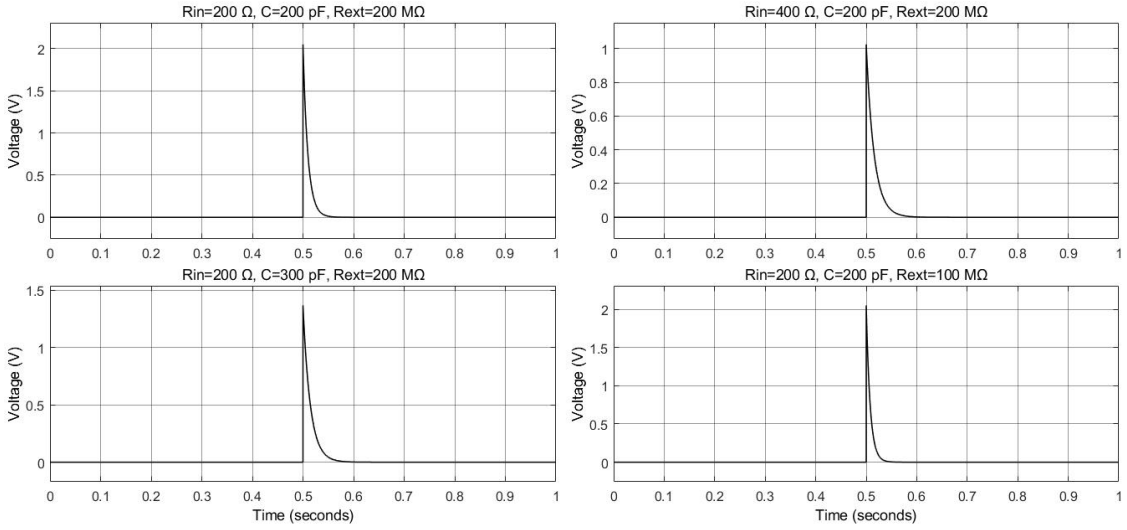
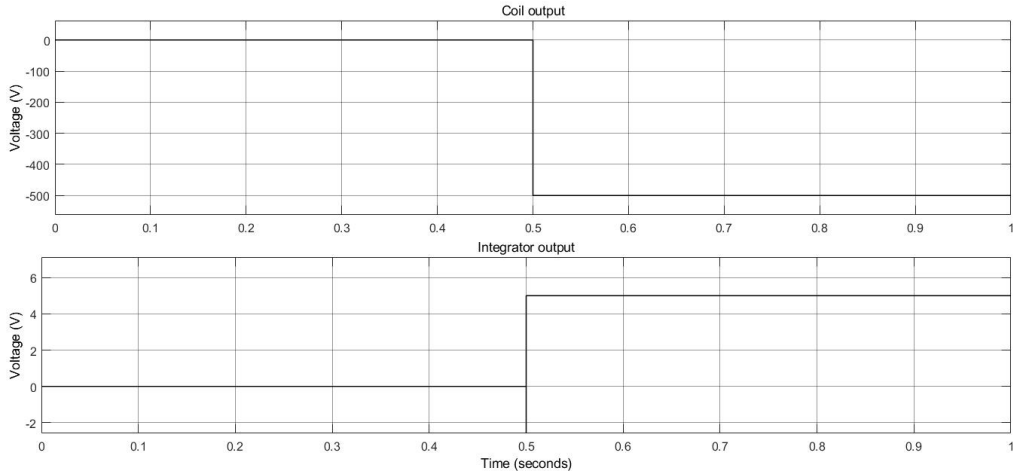
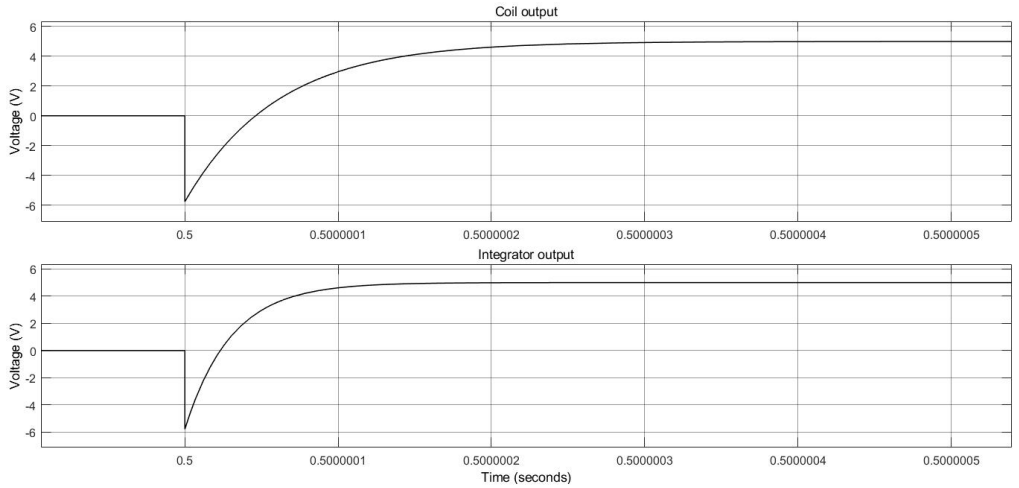


Figure 5.11: Integrator output for different values of R_{in}, C and R_{ext}

The upper left waveform is the same one with the bottom one of Figure 5.10, while at the other three one of the parameters is changed. In the case of altering the R_{in} or C the output voltage is decreased, because of the increment of the voltage drop across them. On the other side, the RC time constant is increased, increasing the falling time as well. As for the case of reducing the value of R_{ext}, since it stays at MΩ range, it does not influence the output voltage that much.
The last simulation was for the case of a short-circuit and how fast the integrator output reacts.



(a)



(b)

Figure 5.12: (a) Integrator output with a short-circuit at 0.5 seconds; and (b) its response for different values of capacitances

The voltage has a supply limit of 5 V, this is why it does not exceed this value. As for the response, it is shown on Figure 5.12b, that the smaller value of capacitance results in faster response of the integrator.

5.5 Printed Circuit Board Design

The final step of the theoretical part of the project was the design of the Printed Circuit Board (PCB). The software offers the most common libraries for the components and only the Rogowski coil had to be designed manually. The procedure of the PCB design took place in three stages:

1. Creation of the electrical circuit
2. Assignment of footprints at the components of the circuit
3. Implementation of the connections on the board

5.5.1 Creation of the electrical circuit

Besides the Footprint Editor that was mentioned above, the other tools that are provided by KiCad and were used are:

- Schematic Layout Editor, for creating the electrical circuit
- Symbol Editor, for creating non-existing components
- Footprint Editor, for creating non-existing footprints
- PCB Layout Editor, for creating the connections on the PCB

The creation of the electrical circuit includes the placement of the components and all the connections between them. Two different subsystems were created for being better visualized.

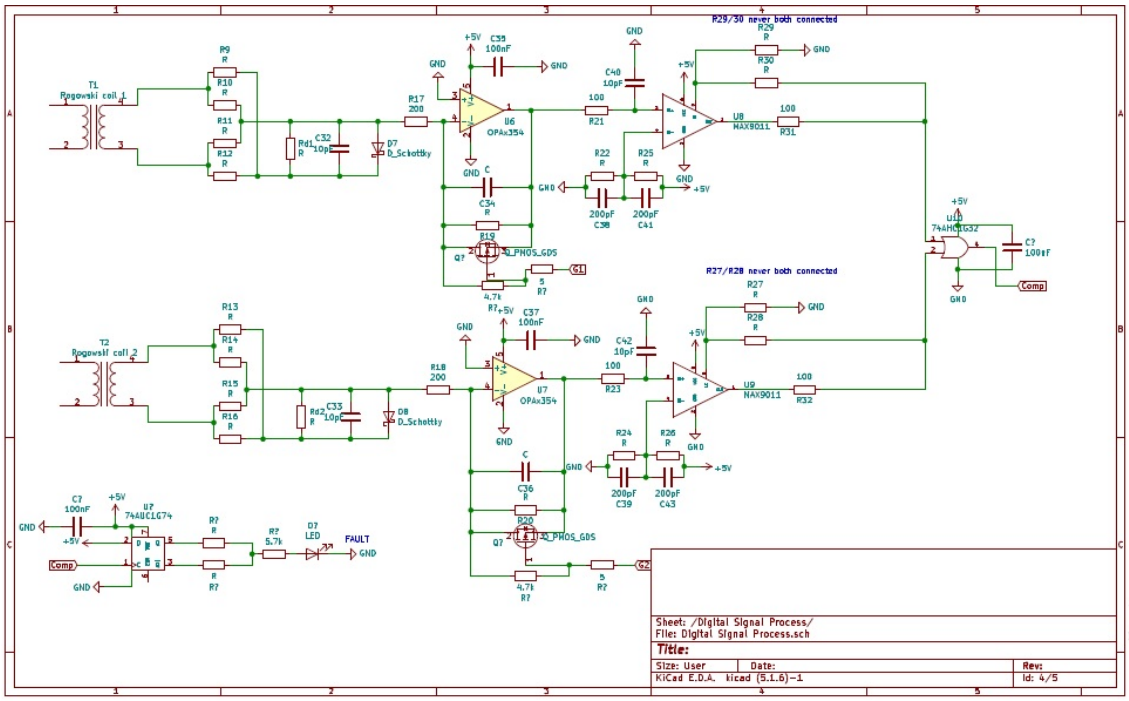


Figure 5.13: Digital signal processing circuit

The first one is the digital signal process with all the existing components being on Figure **??**. Following this the gate driver with the power supply system are presented. Only one of the two gate drivers is shown, but everything is the same at the second one as well.

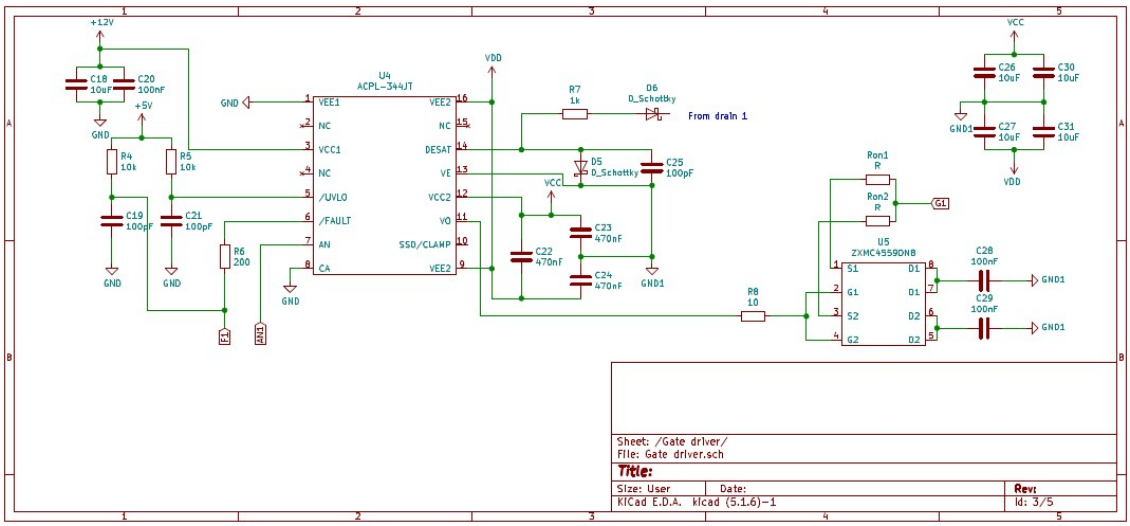


Figure 5.14: Gate driver IC configuration on PCB

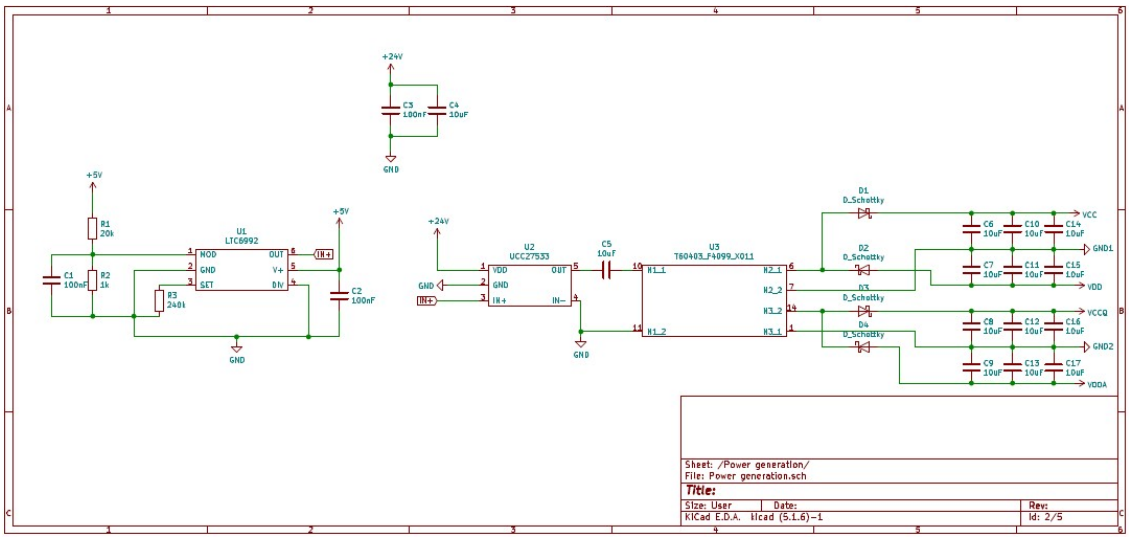


Figure 5.15: Power supply subsystem ln the PCB design

5.5.2 Assignment of footprints at the components of the circuit

After having designed the electrical circuit, the next task was to assign footprints at every component.
The most challenging part of this stage was the creation of the Rogowski coils. Each turn of the coils requires two pins for creating all the connections of the windings. This means that in total 1076 circle circle through-hole pads were used for creating the footprint of the coil.
The rest of the footprints were either already included in the libraries of KiCad, or the manufacturers were giving detailed description of how they should have been designed. Except the transformer for the power supply, the connectors and the transmitter/receiver of the optic fibers, the rest of the components were selected to be surface mounted devices, for making easier the connections on the board.

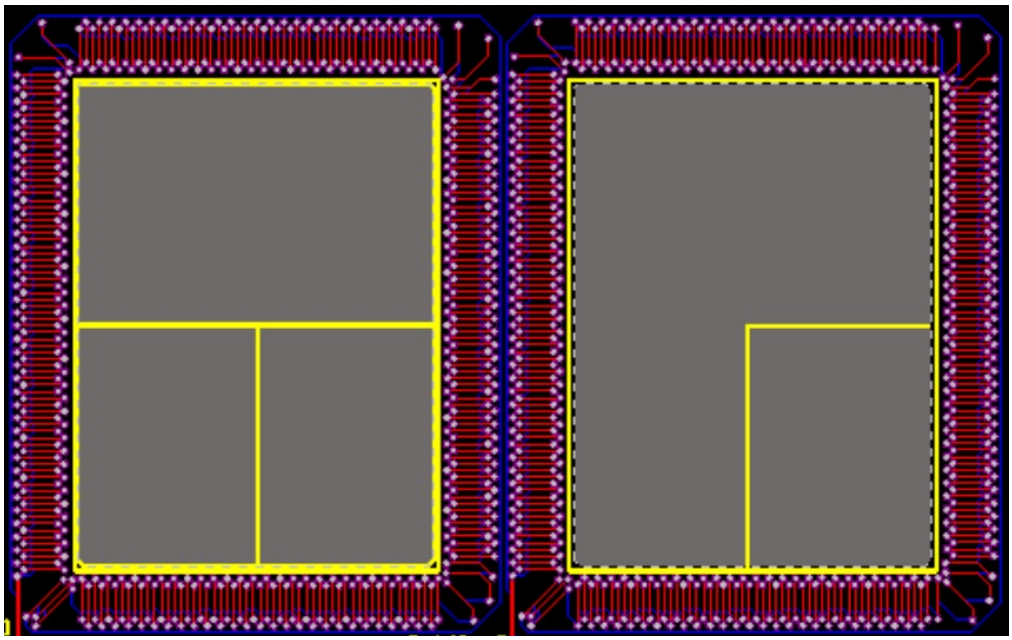


Figure 5.16: Rogowski coil shape

5.5.3 Implementation of the connections on the board

The third stage of the PCB design was the placement of the components on the board and the implementation of the copper traces for connecting them. The target was the highest volume efficiency of the board, with respect to the clearance and creepage requirements. The clearance and creepage requirements for external conductors and a polution severity of 2, for a voltage level of 1.2 kV according to [25] and [35] are 6 and 12 mm. These distances can be halved if needed with coating to the exposed conductors or parts of the components.
The way the Rogowski coil is designed, with a need return winding, creates the need of more than 2 copper layers. Thus, four copper layers will be used, enabling also the use of multiple power planes. The top layer is used for making the connections between the components. The bottom layer was mainly used as the ground power plane for the low side and as the common points for the high sides. The two inner layers are used for creating the power planes of the supply voltages of 5V and 12V and the bias voltages of the module.

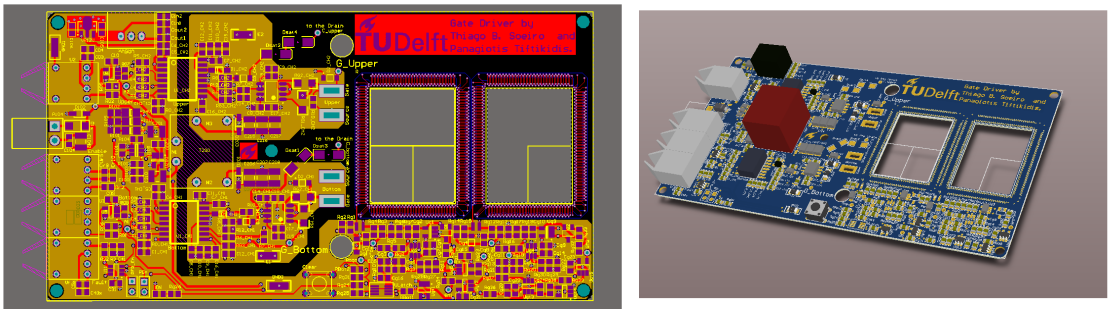
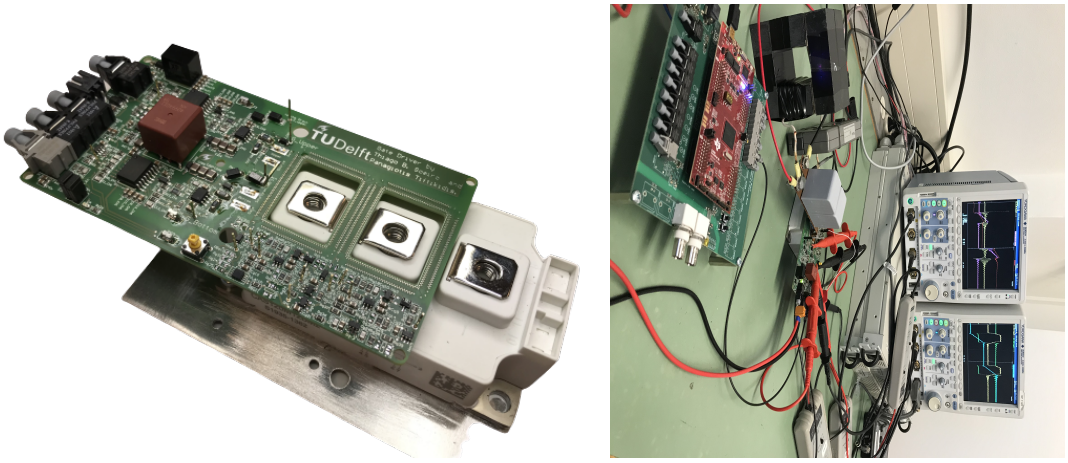


Figure 5.17: PCB and 3D model of the gate driver

6 | Experimental Results

For validating all the theoretical assumptions and the proper operation of the printed board there were two different setups. The first was for testing the operation of the low voltage components of the short-circuit detection system, while the second included the application of high-voltage across the module.



(a) (b)

Figure 6.1: (a)PCB with the module and (b) experimental setup

6.1 Coil Parameters

Before starting the experiments the parameters of the coil were measured. Using an the impedance analyzer 4294A made by Agilent the resonance frequency of the coil was measured 36 MHz.

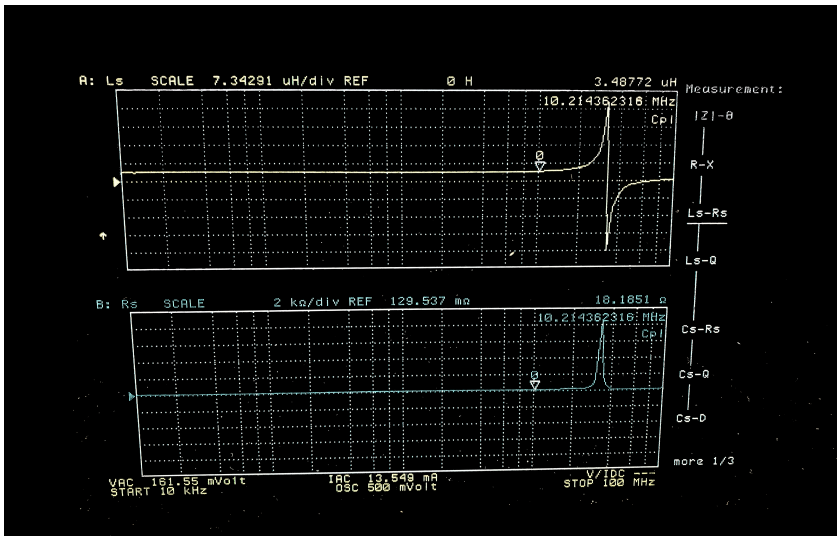


Figure 6.2: Coil impedance measurement using Agilent 4294A impedance analyzer

On Figure 6.2 these two values include also the impedance of the wire. This was measured separately as is shown below.

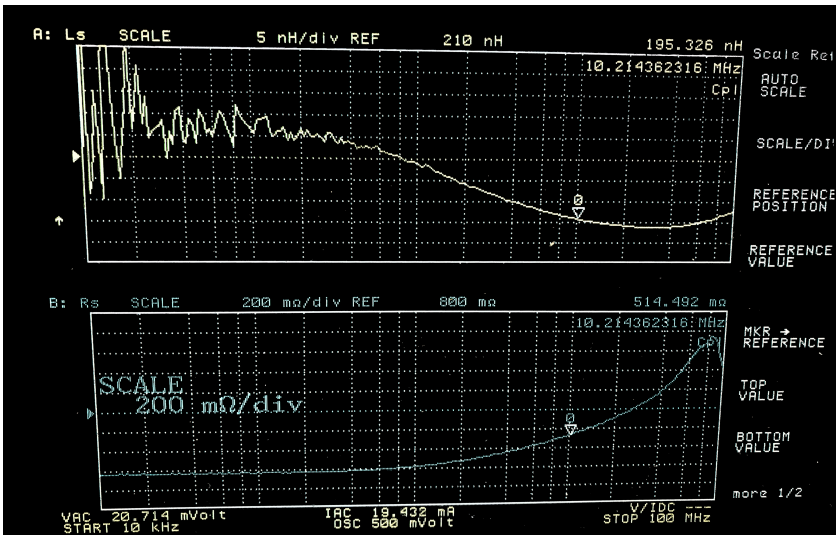


Figure 6.3: Wire impedance measurement using Agilent 4294A impedance analyzer

After substracting the values of the Figures above, the self-inductance value was 3.292 μH and the AC resistance at 10 MHz was measured 17 Ω.Compared with the theoretical value of the self-inductance, which was estimated around 2.8 μH, there is a small difference which can be explained because the coil has slightly different geometry from a typical rectangular. As for the bandwidth, it could be even higher but the target for high measurement capability and accuracy led to the increased winding density limiting the bandwidth.

6.2 Normal Turn-On

After having measured the parameters of the coil, the next step was the validation of the accurate operation of the gate driver. A double pulse test setup is used for this, with its schematic being presented at the next figure.

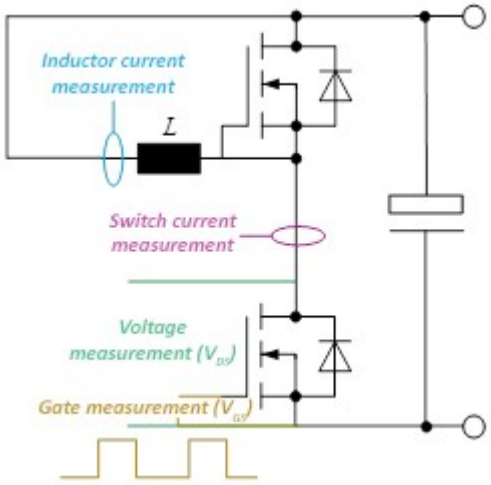


Figure 6.4: Double-pulse test schematic

According to [36], the first pulse is for charging the current of the inductor to the desired value, while the second pulse correlates with the turn-on and turn-off switching transients being of

interest.

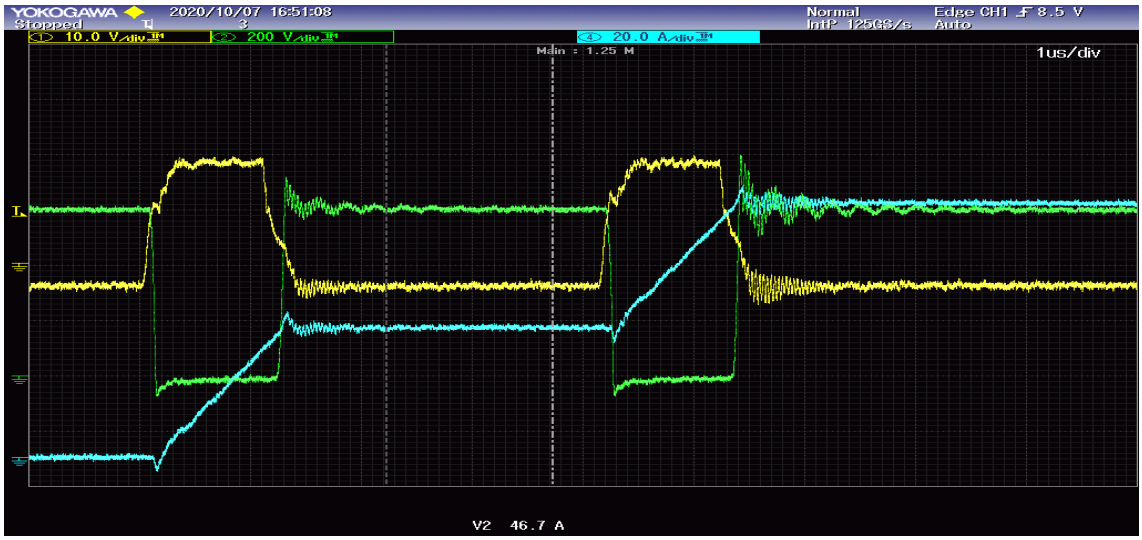


Figure 6.5: V_{GS} (yellow curve) and V_{DS} of the bottom switch (green curve) and current across the inductor (light blue curve) during a double pulse test

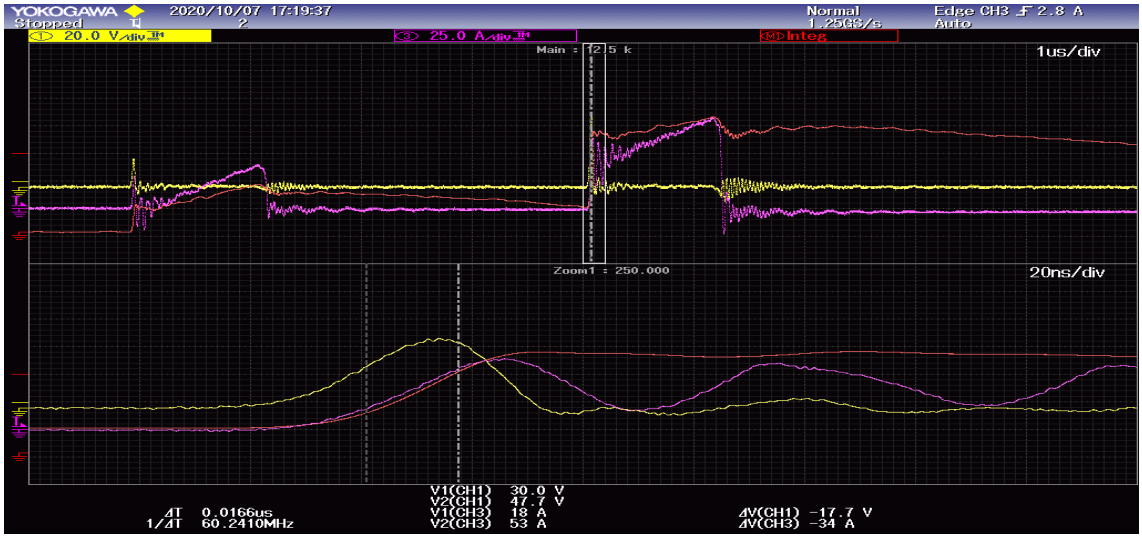


Figure 6.6: Current flowing through the switch (purple curve) and Rogowski coil output (yellow curve)

As can be seen on Figure 6.5, the SiC MOSFET is driven efficiently. Furthermore, following the design at the output of the coil a voltage signal is induced when a current switching transition happens. The value of this signal reaches up to 50 V, as is depicted at the zoomed time slot of Figure 6.6. This value reflects the threshold value that must be applied on the input of the comparator. Since the value is larger than the 5 V the logic ICs can tolerate, a proper tuning of the integrator was requisite for downgrading it.

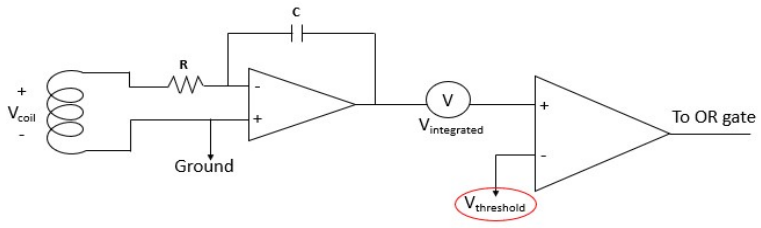


Figure 6.7: Threshold value definition

6.3 Digital Signal Process Circuit Test

Before applying short-circuit conditions the confirmation of the operation of the digital signal process system according to the design was essential.

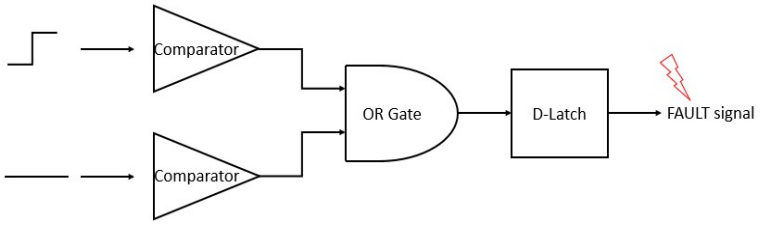


Figure 6.8: Low voltage test flowchart

In practice $V_{threshold}$ was set to be lower than $V_{integrated}$ during a normal turn-on. This a value was selected to be 2.5 V. When $V_{integrated}$ becomes larger than this, the comparator must trip.

Figure 6.9: Rogowski integrated voltage (yellow curve), current flowing through the switch (purple curve) and comparator output (green curve)

Having the same principles with Section 6.2, the second pulse is the one with the interest being on. As can be seen on 6.9, it is confirmed that when $V_{integrated}$ exceeds the predefined value of $V_{threshold}$ a tripping signal is sent by the comparator. The delay for this signal is approximately

50 ns, with the turn off of the module starting after 250 ns. The corresponding V_{GS}, V_{DS} and mains current signals are presented below.

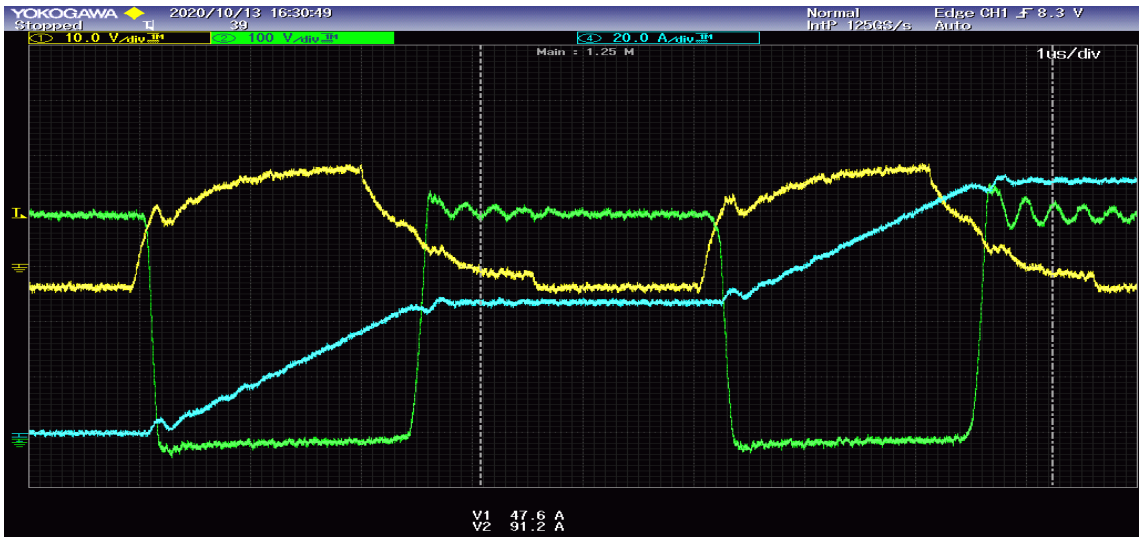


Figure 6.10: V_{GS} (yellow curve) and V_{DS} of the bottom switch (green curve) and mains current (light blue curve) during the comparator trip test

6.4 Short-Circuit Test

The last experimental setup was for checking the response of the coil under a short-circuit event. Two different fault types were applied; one with low inductive character and high current over time ratio and one with low current over time ratio.

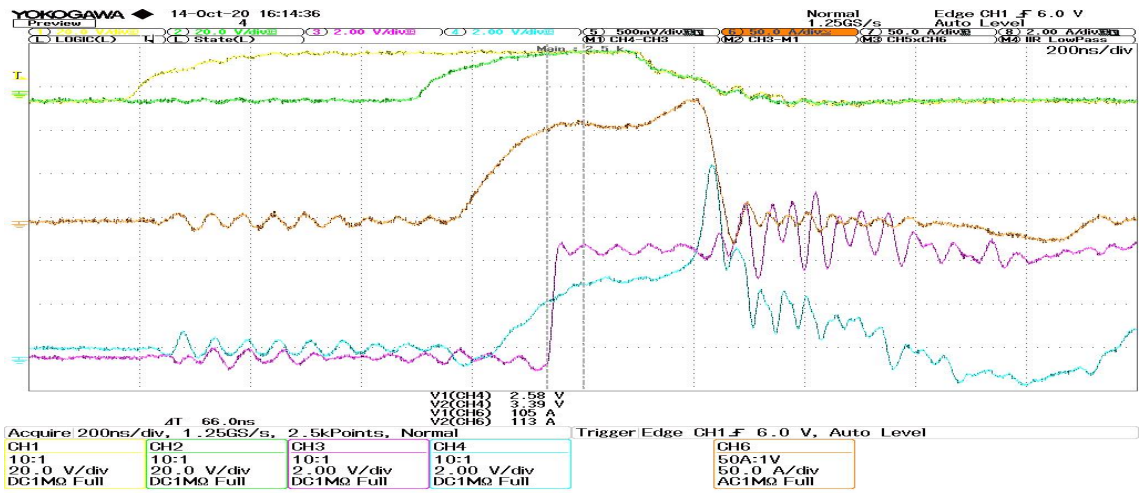


Figure 6.11: V_{GS} of bottom switch (yellow curve), V_{GS} of upper switch(green curve), current across the switch (orange curve), output of the integrator (light blue curve) and fault detection signal (purple curve) during a low inductive short-circuit with high di/dt

As can be seen on Figure 6.11 the slope of the fault current is 0.5 kA/µs. The fault is detected

after approximately 180 ns, with the detection circuitry having a delay of 220 ns, concluding to 400 ns of efficient protection of the module in this case, with the current reaching around 140 A, a value much lower than the nominal. As can be seen on Figure 6.12 the detection trips protecting

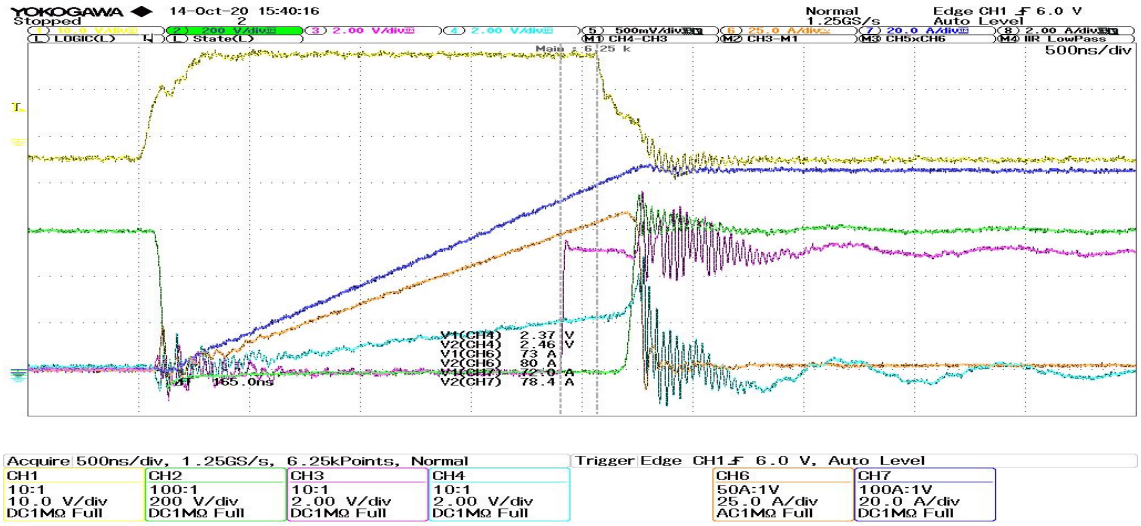


Figure 6.12: V_{GS} of bottom switch (yellow curve), current across the inductor L of Figure 6.4 (dark blue curve), V_{DS} across the bottom switch(green curve), current across the bottom switch (orange curve), output of the integrator (light blue curve) and fault detection signal (purple curve) during a low di/dt fault

the module even in lower current slopes. In this case the di/dt is 10 times lower than the previous case and again the device is protected efficiently with the current that flows through the switch not exceeding the 85 A.

7 | Conclusion

7.1 Gate Driver Design with Integrated Protection System

The development of the technology of the semiconductor field has introduced new wide band-gap materials. This has also emerged the need for new design considerations for their drivers, like the necessity for two voltage levels, fast short-circuit protection and reduced electromagnetic interference.
At this thesis project the main focus was on the protection of the device with a di/dt method being selected for this purpose. In Chapter 1 background information was offered. In Chapter 2 the targets of the project and the scientific approach were defined. In Chapters 3 and 4 the literature analysis of the short-circuit detection methods and the high-voltage gate drivers respectively is contained. In Chapter 5 the design of the gate driver and the development of simulation models are presented. Finally, in Chapter 6 the experimental tests on the board are shown, while Chapter 7 is a summary of all the above and contains some proposals for future research as well.
The first target was the design of a sufficient protection system for the SiC module. For achieving this two rectangular shaped Rogowski coils were integrated on the design of the board of the gate driver. One of the basic considerations of this design was the minimization of the coupling capacitances to avoid parasitically created currents interrupt the operation of the gate driver. Secondly, the speed of the protection (detection and reaction) system was indispensable to have sufficient protection in less that 1 μs. In Section 5.3 this requirement is satisfied based on the developed simulation model of Rogowski coil. Furthermore, in Section 5.5, the minimum distances and the special care for selecting ICs were presented. The printed board was tested in the laboratory as is shown in Chapter 6 proving that the power device can be sufficiently protected.

7.2 Recommendations for Future Research

This thesis project has three different points that could be the trigger for further research and comprehension of developing gate drivers for high voltage devices. These are:

1. Optimize the simulation models of the coil.
2. Design and implement a custom-made isolated converter for the power supply of the gate driver.
3. Program a Field-programmable gate-array (FPGA) for controlling more accurately the application .

Bibliography

[1] Mohan, Undeland, and Robbins, *POWER ELECTRONICS Converters, Applications and Design, 3^{th} Edition, Greek Version.* Tziolas Publications, 2010.

[2] H. Li, X. Lyu, K. Wang, Y. Abdullah, B. Hu, Z. Yang, J. Wang, L. Liu, and S. Bala, "An ultra-fast short circuit protection solution for e-mode gan hemts," in *2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2018, pp. 187–192.

[3] D. Rothmund, "10 kv sic-based medium-voltage solid-state transformer concepts for 400v dc distribution systems," 2018.

[4] K. Brydak and A. Szlachta, "Measuring methods of welding process parameters," *Measurement Automation Monitoring*, vol. 62, p. 26, 01 2016.

[5] *1.2 kV, 13 mΩ All-Silicon Carbide Half-Bridge Module*, Cree, Inc.

[6] J. Lutz, R. Dobler, J. Mari, and M. Menzel, "Short circuit iii in high power igbts," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–8.

[7] J. Lutz and T. Basler, "Short-circuit ruggedness of high-voltage igbts," in *2012 28th International Conference on Microelectronics Proceedings*, 2012, pp. 243–250.

[8] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, B. J. Blalock, and F. Wang, "Design and performance evaluation of overcurrent protection schemes for silicon carbide (sic) power mosfets," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 5418–5425.

[9] K. Ino, M. Miura, Y. Nakano, M. Aketa, and N. Kawamoto, "Sic power device evolution opening a new era in power electronics," in *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2019, pp. 1–3.

[10] R. Pittini, Z. Zhang, and M. A. E. Andersen, "Switching performance evaluation of commercial sic power devices (sic jfet and sic mosfet) in relation to the gate driver complexity," in *2013 IEEE ECCE Asia Downunder*, 2013, pp. 233–239.

[11] J. Wang, Z. Shen, C. DiMarino, R. Burgos, and D. Boroyevich, "Gate driver design for 1.7kv sic mosfet module with rogowski current sensor for shortcircuit protection," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 516–523.

[12] H. Wang, J. Zhao, Z. Zheng, and H. Sun, "Driving a silicon carbide power mosfet with a fast short circuit protection," in *2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2018, pp. 260–265.

[13] S. Mocevic, J. Wang, R. Burgos, D. Boroyevich, M. Jaksic, M. Teimor, and B. Peaslee, "Phase current sensor and short-circuit detection based on rogowski coils integrated on gate driver for 1.2 kv sic mosfet half-bridge module," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 393–400.

[14] C. M. Dimarino, "Design and validation of a high-density 10 kv silicon carbide mosfet power module with reduced electric field strength and integrated common-mode screen," 2019.

[15] A. Maerz, T. Bertelshofer, R. Horff, and M. Bakran, "Requirements of short-circuit detection methods and turn-off for wide band gap semiconductors," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1–6.

[16] T. Ishigaki, H. Kageyama, A. Shima, D. Hisamoto, K. Tomiyama, Y. Sasaki, and S. Ibori, "Freewheeling diode-less sic-inverter with fast short-circuit protection for industrial applications," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1–5.

[17] A. Ahmed, L. Coulbeck, A. Castellazzi, and C. M. Johnson, "Design and test of a pcb rogowski coil for very high di/dt detection," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, pp. DS1a.2–1–DS1a.2–4.

[18] G. Robles, J. M. Martinez, J. Sanz, B. Tellini, C. Zappacosta, and M. Rojas, "Designing and tuning an air-cored current transformer for partial discharges pulses measurements," in *2008 IEEE Instrumentation and Measurement Technology Conference*, 2008, pp. 2021–2025.

[19] M. Chiampi, G. Crotti, and A. Morando, "Evaluation of flexible rogowski coil performances in power frequency applications," *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 3, pp. 854–862, 2011.

[20] D. Gerber, T. Guillod, and J. Biela, "Igbt gate-drive with pcb rogowski coil for improved short circuit detection and current turn-off capability," in *2011 IEEE Pulsed Power Conference*, 2011, pp. 1359–1364.

[21] A. A. ELECTRONICS. Operational amplifier: Inverting op amp and the concept of virtual ground in op amp. [Online]. Available: https://www.youtube.com/watch?v=AuZ00cQ0UrE

[22] J.-P. Charras, D. Hollenbeck, and W. Stambaugh. Kicad eda-schematic capture and pcb design software. [Online]. Available: https://kicad-pcb.org

[23] C. Jiao, J. Zhang, Z. Zhao, Z. Zhang, and Y. Fan, "Research on small square pcb rogowski coil measuring transient current in the power electronics devices," *Sensors*, vol. 19, p. 4176, 09 2019.

[24] J. D. Ramboz, "Machinable rogowski coil, design, and calibration," *IEEE Transactions on Instrumentation and Measurement*, vol. 45, no. 2, pp. 511–515, 1996.

[25] *Generic Standard on Printed Board Design, IPC-2221A, p.43*, Institute of Printed Circuits (IPC), 2 1998.

[26] *DC-50MBd Versatile Link Fiber Optic Transmitter and Receiver for 1 mm POF and 200 μm PCS*, Avago Technologies.

[27] *Automotive 2.5A Gate-Drive Optocoupler with Integrated IGBT Desat Overcurrent Sensing, Miller-Current Clamping, and Under-Voltage Lockout Feedback*, Avago Technologies.

[28] *COMPLEMENTARY 60V ENHANCEMENT MODE MOSFET*, Zetex Semiconductors.

[29] J. Wang, "Switching-cycle control and sensing techniques for high-density sic-based modular converters," 2017.

[30] *Voltage-Controlled Pulse Width Modulator*, Analog Devices Inc.

[31] *Drive transfmormer*, Vacuumschmelze.

[32] E. A. Software. Rectangular wire resistance. [Online]. Available: https://www.emisoftware.com/calculator/resistance-rectangular-wire/

[33] C. ELECTRONICS. Rectangular conductor resistance calculator. [Online]. Available: https://chemandy.com/calculators/rectangular-conductor-resistance-calculator.htm

[34] *OPAx354 250 MHz, Rail-to-Rail I/O, CMOS Operational Amplifiers*, Texas Instruments.

[35] *Standard for Insulation Coordination Including Clearances and Creepage Distances for Electrical Equipment,*, UL-840, 2007.

[36] S. Tiwari, T. Undeland, S. Basu, and W. Robbins, "Silicon carbide power transistors, characterization for smart grid applications," 09 2012, pp. LS6d.2–1.

A | Appendix A

```
1 -   clc
2 -   clear all
3
4 -   distance=0.36e-3;          %distance between windings
5 -   m0=4e-7*pi;
6 -   l=2e-3;
7 -   h=1.6e-3;
8     %% Turns distances for total inductance of horizontal side
9 -   up=34.7e-3/2;
10 -  down=29.7e-3/2;
11 -  Fh=m0*h*log(up/down)/(2*pi);
12 -  Fh=0;
13 -  N_a=27;
14 -  for i=1:1:N_a
15 -      d(i)=sqrt(down^2+(i*distance)^2);
16 -      u(i)=sqrt(up^2+(i*distance)^2);
17 -      F_h(i)=m0*h*log(u(i)/d(i))/(2*pi);
18 -      Fh=Fh+F_h(i);
19 -  end
20
```

Rows 1-20 of the code for calculating the mutual and self-inductance

```
21      %% Turns distances for total inductance of vertical sides
22 -    ups=(sqrt((27.6e-3/2)^2+(distance/2)^2));
23 -    downs=(sqrt((22.4e-3/2)^2+(distance/2)^2));
24 -    Fvl=0;
25 -    Fv=0;
26 -    N_b=35;
27 -    for i=1:1:N_b
28 -        ds(i)=sqrt(downs^2+((i-1)*distance)^2);
29 -        us(i)=sqrt(ups^2+((i-1)*distance)^2);
30 -        F_v(i)=m0*h*log(us(i)/ds(i))/(2*pi);
31 -        Fv=Fv+F_v(i);
32 -    end
33
34 -    upsl=(sqrt((27.6e-3/2)^2+(distance/2)^2));
35 -    downsl=(sqrt((22.4e-3/2)^2+(distance/2)^2));
36 -    Fdl=m0*h*log(upsl/downsl)/(2*pi);
37 -    Fd=0;
38 -    N_c=37;
39 -    for i=1:1:N_b
40 -        dsl(i)=sqrt(downsl^2+((i-1)*distance)^2);
41 -        usl(i)=sqrt(upsl^2+((i-1)*distance)^2);
42 -        F_d(i)=m0*h*log(usl(i)/dsl(i))/(2*pi);
43 -        Fd=Fd+F_d(i);
44 -    end
```

Rows 21-44 of the code for calculating the mutual and self-inductance

```
45      %% Turns at the corners
46 -    u=sqrt((27.6e-3/2)^2+(34.7e-3/2)^2);
47 -    d=sqrt((22.4e-3/2)^2+(29.7e-3/2)^2);
48 -    Fc=m0*h*log(u/d)/(2*pi);
49
50 -    Ntotal=4*(N_a+0.5)+2*(N_b+1)+2*(N_c+1)+11;
51 -    A=h*l;
52 -    Ftotal=4*Fh+2*(Fv+Fd)+9*Fc+Fvl+Fdl;
53 -    l_m=110e-3;
54      %% Coil parameters
55 -    Lc=Ftotal*Ntotal;
56 -    M=Ntotal*A*m0/l_m;
```

Rows 45-56 of the code for calculating the mutual and self-inductance