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A 66-dB SNDR Pipelined Split-ADC in 40-nm CMOS Using a Class-AB Residue Amplifier

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***Abstract*— This paper presents a closed-loop class-AB residue amplifier for pipelined analog-to-digital converters (ADCs). It consists of a push–pull structure with a "split-capacitor" biasing circuit that enhances its power efficiency. The amplifier is inherently quite linear, and so incomplete settling can be used to save power while still maintaining sufficient linearity. This also allows the amplifier's gain to be corrected by adjusting its bias current. When combined with digital gain-error detection, in this case the split-ADC technique, the result is a power-efficient gain calibration scheme. In a prototype pipelined ADC, this scheme converges in only 12 000 clock cycles. With a near-Nyquist input, the ADC achieves 66-dB SNDR and 77.3-dB SFDR at 53 MS/s. Implemented in 40-nm CMOS, it dissipates 9 mW, of which 0.83 mW is consumed in the residue amplifiers. This represents a 1.8× improvement in power efficiency compared to state-of-the-art class-AB residue amplifiers.**

***Index Terms*— Analog gain correction, analog-to-digital conversion, class-AB residue amplifier, differential sampling, incomplete settling, split-ADC calibration, split-capacitor bias control technique.**

I. Introduction

RESIDUE amplification is often used to ease the noise requirements of the back-end stages of high-resolution analog-to-digital converters (ADCs). However, the corresponding amplifiers usually consume significant amounts of power. In recent years, many alternative techniques have been developed to improve power efficiency. Some examples include capacitive charge pumps [1], zero-crossing detectors [2], [3], class-AB amplifiers [4]–[6], virtual ground reference buffers [7], time-based amplification [8], dynamic amplifiers [9], [10], and pulsed bucket brigades [11]. Most of these approaches, however, improve power efficiency at the expense of analog performance, such as gain accuracy and/or linearity. Various calibration schemes [12]–[25] can be used to detect and correct these errors. Although amplifier gain errors can be corrected in a low-power way [12], nonlinearity correction usually requires considerable power [13], [14].

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This paper proposes a power-efficient class-AB residue amplifier that leverages digital calibration while keeping its power overhead to a negligible level. The amplifier is sufficiently linear by design, and so only its gain error needs to be corrected. A "split-capacitor" biasing technique is proposed, which eliminates the need for additional level-shifting capacitors [4], [5], [26], thus reducing its power dissipation (by ∼1.6×) and area. Moreover, incomplete settling is used [15], [16] to improve its power efficiency by almost 4×. As a proof of concept, the proposed class-AB residue amplifier was used to replace the class-A residue amplifiers of a previous pipelined ADC [16]. This resulted in a 4× improvement in the ADC's analog power efficiency.

The amplifier's gain error is calibrated by a combination of analog and digital techniques. Its gain error is detected in the digital domain by using the split-ADC technique [16]–[20]. This was chosen due to its deterministic nature, which requires less clock cycles to converge than statistics-based approaches [14], [21]. In addition, it can operate continuously in the background, unlike other deterministic methods such as queue based [4], [13], foreground [1], [22] and skip and fill [23], [24], which either interrupt the regular conversion cycle or sacrifice conversion speed. Since the detection can be performed at a slow rate (≪ sampling rate F_S), it consumes negligible digital power. After detection, the amplifier's gain error is corrected by adjusting its bias current. This preserves the ADC's resolution, since the error is corrected at its source, i.e., in the analog domain. Moreover, this approach requires no additional power overhead.

The remainder of this paper is organized as follows. Section II presents the design of the proposed class-AB residue amplifier. Section III discusses the use of incomplete settling in the residue amplifier. Section IV describes the ADC implementation details. Section V discusses the gain calibration scheme used in this paper. Finally, Sections VI and VII present the measurement results and the conclusion.

II. Class-AB Residue Amplifier Design

A single-stage push–pull class-AB residue amplifier is conceptually illustrated in Fig. 1(a). Two ideal voltage sources act as level shifters to independently bias the NMOS and PMOS transistors. Due to its class-AB nature, the amplifier can output currents much larger than its quiescent current, thus eliminating slewing. Furthermore, it supports a large output swing, and its bias current is reused to double its effective transconductance. Since both transistors

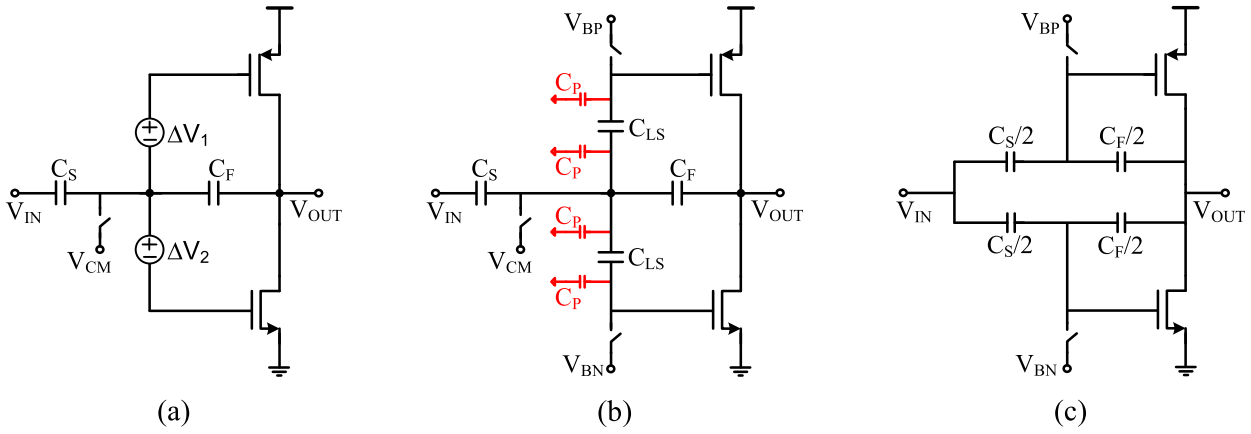

Fig. 1. Class-AB amplifier half circuit with (a) ideal voltage source level shifters, (b) capacitor level shifters, and (c) proposed split-capacitor bias scheme.

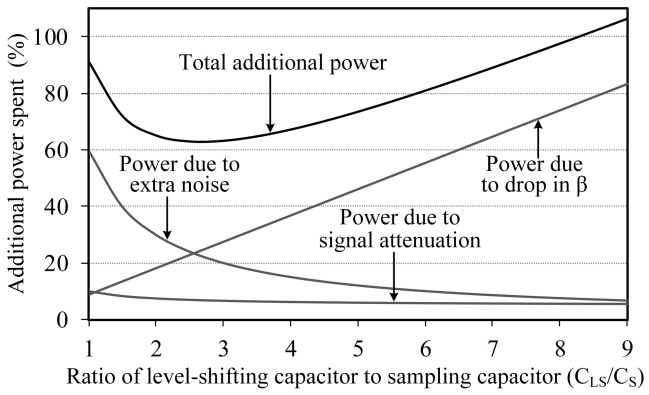

Fig. 2. Simulated power penalty due to extra capacitor level shifters (C_{LS}) in a class-AB amplifier compared to ideal voltage source level shifters.

provide gain, the amplifier also does not suffer from excess noise.

A. Split-Capacitor Biasing Technique

The level-shifting function of the voltage source can be implemented by a switched-capacitor circuit [4], [5], [26], as shown in Fig. 1(b). However, these level-shifting capacitors C_{LS} increase chip area and significantly degrade the amplifier's power efficiency (Appendix A). First, the switched-capacitor approach adds kT/C noise. Second, the input signal is attenuated by the voltage divider formed by C_{LS} capacitors and the gate–source capacitances of the transistors. Therefore, C_{LS} capacitors need to be quite large to mitigate both these effects. However, doing this increases the parasitic capacitance (C_P) at the virtual ground, reducing the amplifier's feedback factor β. Consequently, its bandwidth and loop gain $A\beta$ drop (A = amplifier's open-loop gain). Fig. 2 shows this tradeoff under the assumption that parasitic capacitance C_P is 5% of the intended capacitance C_{LS}. Even at the optimum point, the presence of C_{LS} capacitors requires an additional 63% of power to achieve the same bandwidth and noise as the amplifier in Fig. 1(a).

This paper presents a "split-capacitor" biasing technique that eliminates the drawbacks of C_{LS} capacitors. As shown in Fig. 1(c), it uses the already available sampling C_S and feedback C_F capacitors to perform the level-shifting operation. Both capacitors are split in half and used to store the level-shifting voltages, allowing the amplifier's NMOS and PMOS transistors to be biased independently. Hence, C_{LS} capacitors, and their associated drawbacks, are eliminated.

Splitting the capacitors into two halves [Fig. 1(c)] has no effect on the circuit's noise performance. Although the sampled noise across each $C_S/2$ capacitor is doubled ($2kT/C_S$) compared to a single C_S capacitor, it transfers to the amplifier's output with a $2\times$ lower gain ($\sim C_S/2C_F$). Hence, each $C_S/2$ capacitor contributes an output noise power of $(2kT/C_S)\times(C_S/2C_F)^2 = (1/2)\times(kT/C_S)\times(C_S/C_F)^2$. The overall noise power, therefore, remains the same as in the case of a single C_S capacitor. Intuitively, this can be understood by realizing that the total sampling capacitance stays the same after the splitting, and so the associated noise power must also be the same. In fact, the proposed class-AB amplifier achieves the same performance as the amplifier with ideal level shifters [Fig. 1(a)].

In a multi-bit/stage implementation, C_S usually consists of an array of capacitors to interpolate the reference voltages. Any mismatch in these capacitors can cause ADC nonlinearity, which then requires calibration or trimming. In this design, the two $C_S/2$ capacitors are not used to interpolate the mid-reference of the 1.5 bit/stage MDAC. Instead, it is generated by a third reference voltage. Since there is no interpolation, the impact of mismatch in the two $C_S/2$ capacitors on the ADC's integral nonlinearity (INL) and differential nonlinearity (DNL) performance is negligible (Appendix B). However, the split-capacitor approach does require two bottom-plate switches and clock drivers, which leads to a minor increase in area and power. The two bottom-plate sampling clocks should also be well synchronized to ensure that the signals sampled on the split capacitors are as equal as possible.

B. Linearity Considerations

The proposed amplifier achieves the required linearity by design. It consists of a differential pair with grounded source nodes (i.e., a class-AB amplifier), whose transistors are biased

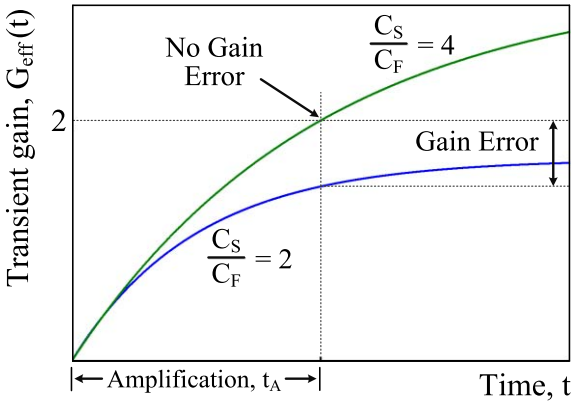

Fig. 3. Gain settling of an amplifier for different capacitor ratios (C_S/C_F).

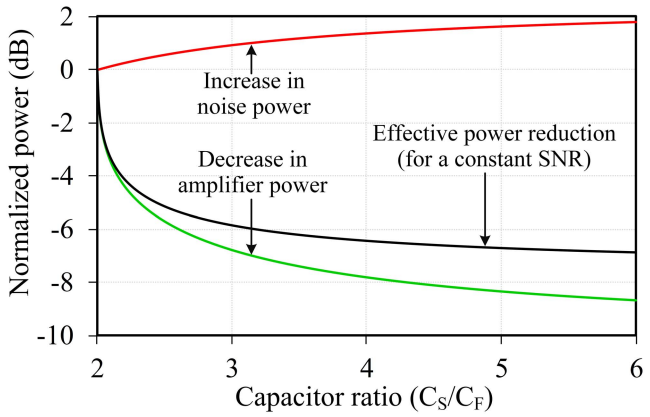

Fig. 4. Amplifier power and noise as a function of the capacitor ratio (C_S/C_F) normalized to that of $C_S/C_F = 2$.

in the strong-inversion saturation region. For the same power dissipation, the resulting class-AB amplifier is more linear than a differential pair with a tail current source (Appendix C). Although this choice slightly degrades the amplifier's power efficiency (g_m/I_d), it is offset by the fact that digital nonlinearity calibration is not required. A more serious drawback is that the amplifier has no common-mode (CM) rejection capability. However, this can be addressed by circuit techniques, which will be discussed in Section IV-B.

Assuming an ideal quadratic behavior in the strong-inversion saturation mode, the amplifier's differential output current will be a perfectly linear function of its input voltage [27]. In practice, however, this assumption is not completely valid, and so there will be some residual distortion. Furthermore, transistor mismatch will give rise to even-order distortion. To address these issues, the amplifier is used in a feedback configuration. However, due to its inherent linearity, only a low loop gain is required to achieve sufficient linearity.

III. Incomplete Settling

Incomplete settling is used in the proposed residue amplifier to lower its bandwidth, and thus significantly reduce its power dissipation. As shown in [15] and [16], this also optimizes the tradeoff between noise and power, with the optimum configuration being an integrator [9].

A. Amplifier Gain

Fig. 3 illustrates the amplifier's gain settling $G_{\text{eff}}(t)$ for two different capacitor ratios (C_S/C_F). Here, $G_{\text{eff}}(t)$ represents the amplifier's transient closed-loop gain, defined as the ratio of the instantaneous amplitude of the output signal to the amplitude of the input step. At the end of an amplification period t_A, this is given by

$$G_{\text{eff}}(t = t_A) = \frac{A\beta}{1 + A\beta}\frac{C_S}{C_F}(1 - \exp^{-t_A/\tau}) \tag{1}$$

where τ is the closed-loop time constant of the amplifier.

In this paper, the ADC uses a 1.5 bit/stage MDAC, requiring a gain $G_{\text{eff}} = 2$. Due to the amplifier's finite gain, a capacitor ratio $C_S/C_F = 2$ would result in the significant gain error, even when the amplifier settles completely (i.e., $\exp^{-t_A/\tau} \approx 0$). This design combines a higher capacitor ratio, $C_S/C_F = 4$, with incomplete settling. As a result, the desired gain can be obtained by simply adjusting the amplifier's time constant τ, as shown in Fig. 3. This facilitates the implementation of an analog gain correction as will be discussed in Section V-B.

B. Power Dissipation and Noise

For a given noise performance, incomplete settling decreases the amplifier's power dissipation. This can be seen by calculating the power dissipation and noise of the closed-loop amplifier as a function of its degree of settling (t_A/τ). To simplify the analysis, a high loop gain is assumed [$A/(1 + A\beta) \approx 1/\beta$], and the amplifier's gate–source capacitance is ignored [$\beta = C_F/(C_S+C_F)$]. By following a similar approach to in [15], the power dissipation can be expressed as follows:

$$P_{\text{amp}} \propto \frac{C_L}{t_A}\left(\frac{t_A}{\tau}\right)\left(1 + \frac{2}{1 - \exp^{-t_A/\tau}}\right). \tag{2}$$

Assuming the amplifier's noise bandwidth is limited by its load capacitor C_L, the variance of the output noise voltage (i.e., the noise power) at time t_A can be expressed as [16]

$$P_n = \left(1 + \frac{C_S}{C_F}\right)\frac{\gamma kT}{C_L}(1 - \exp^{-2t_A/\tau}) + \frac{kT}{C_L}\exp^{-2t_A/\tau} \tag{3}$$

where γ is the noise factor of the MOS transistor ($\approx$2/3). The second term in (3) is the noise power that arises because load capacitor C_L is reset at the start of each amplification cycle.

Fig. 4 illustrates the effect of reduced settling on the amplifier's power dissipation and noise performance using (2) and (3). Over the entire sweep, $(C_S + C_F)$ is kept constant. Also, gain G_{eff} of 2 is maintained with $\sim$0.1% accuracy, which in the case of $C_S/C_F = 2$ would require near-complete settling ($t_A/\tau \approx 7$). As the capacitor ratio is increased, the amplifier's settling (t_A/τ) is reduced to keep $G_{\text{eff}} = 2$. This decreases the power dissipation according to (2) but with an increase in noise power given by (3). As the decrease in power dissipation is much faster than the increase in noise, the amplifier's overall power efficiency improves. A ratio of $C_S/C_F = 4$ is chosen in this design.

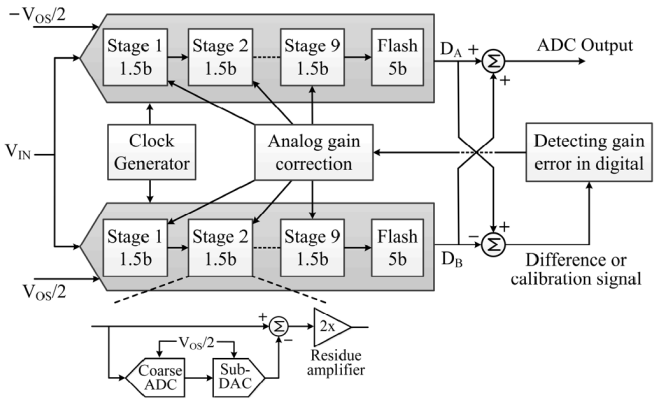

Fig. 5. Implemented pipelined split-ADC structure.

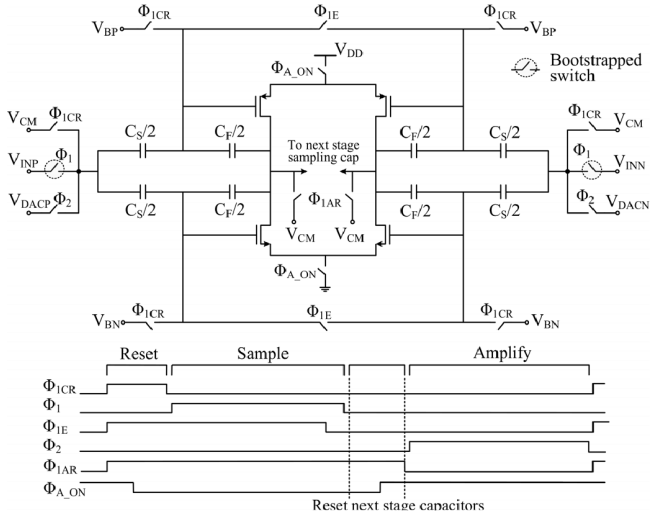

Fig. 6. MDAC-stage topology with timing diagram.

In the case of complete settling, sampling clock jitter results in negligible noise because the residue amplifier's output does not change much at the sampling moments. However, this is not the case with incomplete settling, resulting in a jitter-induced noise voltage σ_v. As shown in [15], the worst-case (i.e., output voltage = ADC full scale) jitter noise voltage $\sigma_{v,\text{worst}}$ normalized to the LSB of the ADC back end is given by

$$\frac{\sigma_{v,\text{worst}}}{\text{LSB}_{\text{back}}} = 2^{B_{\text{back}}} \times \frac{\sigma_t}{\tau} \times \frac{\exp^{-t_A/\tau}}{1-\exp^{-t_A/\tau}} \tag{4}$$

where σ_t is the standard deviation of the clock jitter and B_{back} is the ADC back-end resolution in bits. As expected, the impact of jitter on the output noise voltage is larger for incomplete settling (i.e., with less t_A/τ) or for large timing jitter (σ_t/τ). Note that a timing jitter σ_t in the range of 1 ps or less is required to sample high-frequency input signal with ∼12-bit accuracy. With $t_A = 0.5/(50\text{ MHz})$, $\sigma_t = 1$ ps, and $B_{\text{back}} = 11$ bits, the jitter noise contribution is below 0.12 LSB rms for $t_A/\tau > 1$ and so is not a limiting factor in this design.

IV. ADC Implementation Details

A. ADC Architecture

As a test vehicle for the proposed amplifier, the SHA-less 12-bit pipelined split-ADC shown in Fig. 5 was implemented. Each split-ADC comprises nine 1.5-bit MDAC stages using the proposed class-AB residue amplifier, followed by a 5-bit flash-ADC back end. The extra 2 bits in the back end are only used to improve the calibration accuracy. The digital outputs of the two split-ADCs are averaged to provide the overall ADC output and subtracted to generate a calibration signal.

To enable gain-error detection, a differential offset voltage (V_{OS}) is added to the reference path of the split-ADC. The capacitors are scaled down by a factor of 2 per stage for stages 1–3 (C_S, $C_S/2$, $C_S/4$, $C_S/4$, ...), while the residue amplifiers are only scaled down twice (g_m, $g_m/2$, $g_m/2$, ...). Note that the ADC's power efficiency can be further improved by implementing a more aggressive stage scaling, i.e., resolving a higher number of bits per stage.

B. MDAC Design

A 1.5 bit/stage MDAC is used in the first nine stages of the ADC, each effectively resolving 1 bit. The MDAC topology and its timing scheme are shown in Fig. 6. Bootstrapped switches and bottom-plate sampling are used to ensure good linearity. Although a "flip-around" MDAC usually achieves better speed and noise performances, a "non-flip-around" MDAC topology was chosen for two reasons. First, it simplifies the gain calibration [18], [23], as both the input signal (V_{IN}) and the sub-DAC reference (V_{DAC}) experience the same gain error. Second, the difference in the speed and noise performances of the two topologies is not significant since a capacitor ratio (C_S/C_F) of 4 is used.

The use of incomplete settling means that the output of the residue amplifier will depend on its previous output, resulting in intersymbol interference (ISI). To avoid this, an additional clock phase ($\Phi_{1\,\text{CR}}$) is used to reset all MDAC capacitors. This phase is also used to establish the amplifier's bias voltages. To minimize its overhead, $\Phi_{1\,\text{CR}}$ is made 24× shorter than the sampling (Φ_1) and amplification (Φ_2) phases.

The proposed amplifier is pseudodifferential and hence exhibits equal CM and differential-mode gain. As a result, CM signals will be amplified as they propagate through the stages and may overload the ADC. To avoid this, the CM impedance of the sampling network is increased during Φ_1 [4] by disconnecting the CM switches. Thus, only the differential signal is captured on the sampling capacitors, eliminating any CM signal propagation. When not in use, the residue amplifiers are switched OFF by the Φ_{A_on} clock, which reduces their power dissipation by about half.

C. Bias Design

As discussed in Section III-A, effective gain G_{eff} of the residue amplifier varies with its time constant τ and hence can be adjusted by tuning its bias current I_B, via a bias current DAC. The dependence of G_{eff} on I_B is shown in Fig. 7, along with the amplifier's bias circuit. The DAC's LSB step is chosen to ensure that G_{eff} can be set to ∼10-bit accuracy,

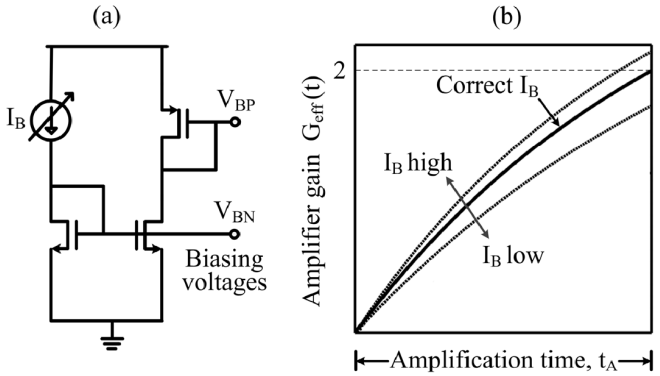

Fig. 7. (a) Amplifier's bias circuit. (b) Dependence of its gain on the bias current (I_B).

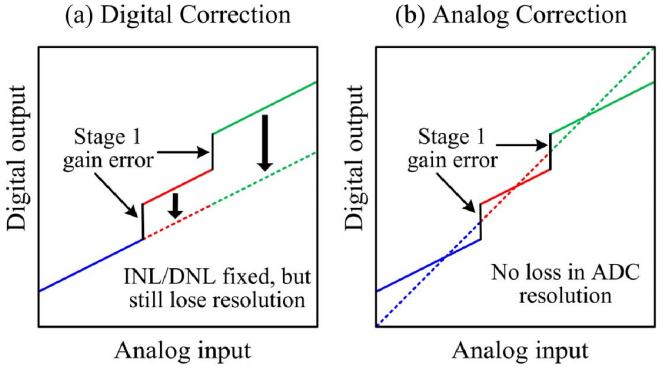

Fig. 8. Comparison of (a) digital and (b) analog gain correction. Solid lines: before the correction. Dashed lines: after the correction.

while its range is set to about ±25% to compensate for the variation of G_{eff} over process, voltage, and temperature (PVT). Both requirements can be met by a 9-bit bias current DAC. Simulations show that even with the minimum bias current, the amplifier's transistors still operate in the strong-inversion saturation region, and therefore the amplifier maintains its linearity over the full DAC range.

In this design, a 3-bit current DAC sets the nominal current of the amplifier. In addition, 5-bit coarse and 5-bit fine binary current DACs are implemented to correct the gain errors. There is approximately 1-bit overlap between the coarse and fine DACs to avoid large DNL or missing current steps. The LSB current is 80 nA, which can be increased or decreased by a factor of 2. It should be noted that the extra programmability is not essential, and is added for test purposes. Apart from some extra leakage current, there is no significant power penalty associated with this gain correction approach. However, there is an area penalty, since the individual current DACs are sized for monotonicity. The entire bias block occupies 0.05 mm^2, which is around 7% of the ADC core area. The accuracy of the bias current and hence the area of the bias block can be relaxed by using a multi-bit/stage ADC architecture [9], which imposes less stringent requirements on residue amplifier accuracy.

V. Gain Calibration

In this paper, an efficient residue amplifier gain calibration scheme is proposed that significantly reduces calibration power. This section discusses its implementation, and how amplifier gain errors can be detected in the digital domain and then corrected in the analog domain.

A. Error Detection in the Digital Domain

A split-ADC calibration technique [16]–[20] is used to detect amplifier gain error. It is fully deterministic, which speeds up the convergence of the calibration. Moreover, it operates in the background and so does not impact the ADC's conversion speed [4], [13]. However, the split-ADC approach adds area and power overhead since some of the blocks are not noise limited and also cannot be split in half (e.g., comparators and flash ADCs). The overall ADC power dissipation is, therefore, increased by about 10%.

To detect gain errors, a differential offset voltage V_{OS} is applied to the split-ADC's coarse ADC and sub-DAC references (Fig. 5). This shifts their input–output transfer curves relative to each other, so that they do not exhibit identical errors for the same input. As a result, when the transfer curve of one ADC exhibits a jump due to a gain error, the transfer curve of the other ADC will not and so can be used as a reference to detect this error. In a split-ADC topology, the difference of the two ADC outputs contains the error information. If the two ADCs make no errors, then their difference will be a straight line, representing the digitized offset voltage V_{OS}. Any deviation from this line indicates errors in the ADC conversion. For example, gain errors in residue amplifiers generate abrupt jumps at the transition between two sub-ranges, whereas a gain mismatch between two split-ADCs gives a tilt in the difference signal. Once the errors have been detected in the digital domain, the next step is to perform the error correction. Note that the digital power required for error detection is negligible since it operates at a much lower rate than the ADC's sampling rate F_S.

B. Analog Gain Correction

While digital error detection can be performed at a subsampling rate ($\ll F_S$), digital error correction must be done at F_S and thus will consume considerable power [13], [14]. Moreover, unlike analog error correction, which corrects errors at their source, digital error correction cannot recover the resolution loss caused by gain errors. Fig. 8 shows the difference between digital and analog error correction. For simplicity, only the first stage is assumed to have a gain error, causing jumps in the ADC's input–output transfer curve at the MSB transitions. Digital error correction [Fig. 8(a)] eliminates this discontinuity by adjusting the bit weight or digital gain of the encoder, which realigns the ADC's sub-ranges but does not remove the slope error of the input–output transfer. In contrast, analog error correction [Fig. 8(b)] resolves gain error in the analog domain where it arises. As a result, it eliminates the slope error and thereby also removes the jumps.

In this design, an analog gain correction approach is adopted by tuning the amplifier's bias current as discussed in Section IV-C. Since the detected error of a pipelined stage is affected by the errors of succeeding stages, the calibration

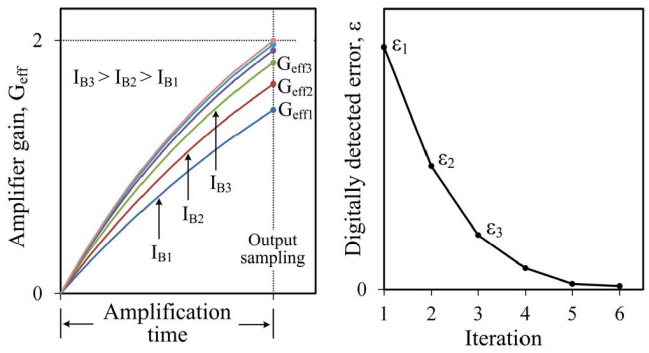

Fig. 9. Convergence of a single-stage gain calibration.

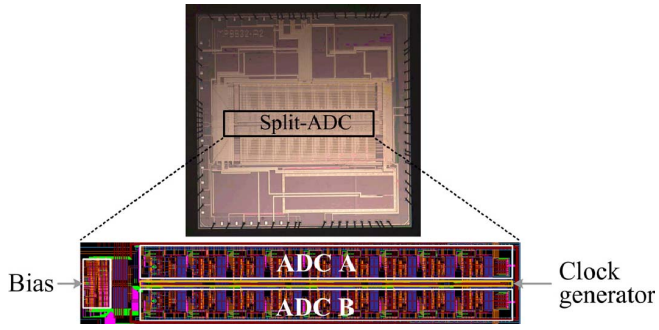

Fig. 10. Die photograph.

starts from the back end of the ADC and progresses toward the first stage. To calibrate a particular stage, the residue amplifier's gain error is detected using the split-ADC technique, which is continuously running in the background. If its gain deviates from the desired value, its bias current is adjusted until the correct gain is reached.

Fig. 9 illustrates the convergence of a single-stage gain calibration. Consider an initial bias current I_{B1} that results in a gain of G_{eff1}. Since the digital gain of the encoder is set to 2, this results in a gain error ε_1, which is digitally detected by the split-ADC technique. The polarity of ε_1 indicates whether the bias current needs to be increased or decreased. Since the gain is lower than 2 in this case, the bias current is increased to I_{B2}. Consequently, the amplifier's gain also increases from G_{eff1} to G_{eff2}, resulting in a smaller gain error ε_2. By following similar steps for a couple of iterations and tuning the bias current appropriately, $G_{eff} = 2$ can be obtained. Since the bias current is only used to achieve the desired gain, there is no additional power penalty associated with this gain correction approach.

VI. Measurement Results

The prototype ADC was fabricated in a 40-nm digital CMOS process and occupies about 0.76 mm^2 (Fig. 10). The ADC's full signal range is 1.5 $V_{pp\text{-}diff}$ with a 1-V supply. Fig. 11 shows the measured spectra of 32× decimated ADC output data at $F_S = 53$ MS/s with a 25.7-MHz input signal, before and after gain calibration. The split-ADC difference signal is shown in Fig. 12 with 12-bit resolution. Since the calibration of different stages

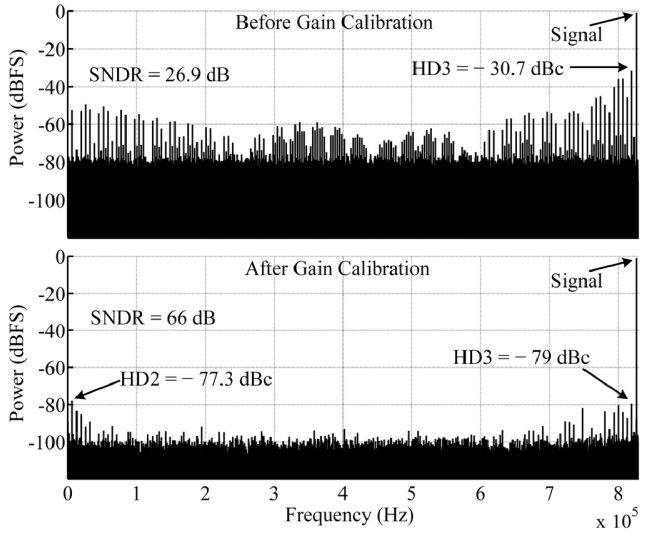

Fig. 11. Measured 32× decimated ADC output spectra for $F_{IN} = 25.7$ MHz and $F_S = 53$ MS/s.

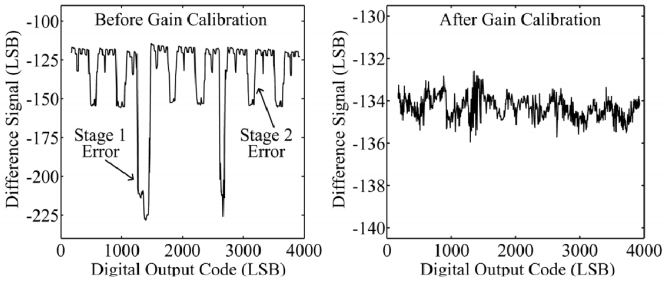

Fig. 12. Split-ADC difference signal before and after the gain calibration.

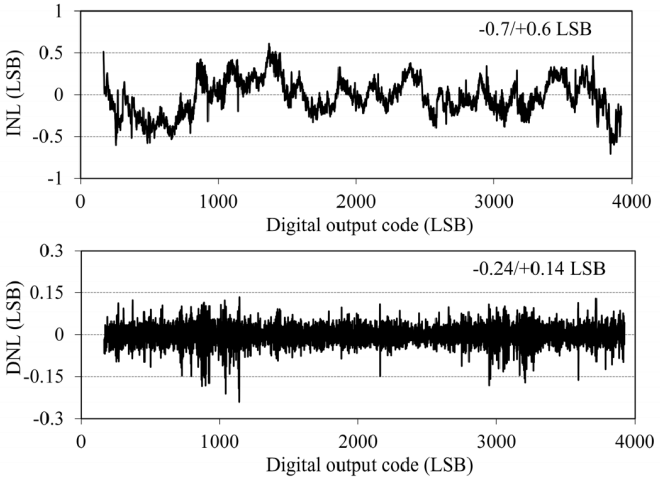

Fig. 13. INL and DNL after the gain calibration.

is deterministic and orthogonal, convergence is reached in 12 000 clock cycles. As expected, the ADC's performance improves significantly after gain calibration, achieving 66-dB signal-to-noise-plus-distortion-ratio (SNDR) and 77.3-dB spurious-free dynamic range (SFDR). The higher order harmonics in the spectra are most likely due to ISI on the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

	Shin JSSC 2014 [3]	Kim JSSC 2012 [4]	Boo JSSC 2015 [7]	Oh JSSC 2014 [8]	Panigada JSSC 2009 [14]	Sehgal JSSC 2015 [16]	Miyahara JSSC 2014 [25]	This work
Technology	55nm	90nm	65nm	0.13µm	90nm	40nm	0.18µm	40nm
Number of calibration cycles	-	2.2×10^4	-	-	2×10^9	7×10^4	3.2×10^4	1.2×10^4
Clock frequency F_S (MS/s)	200	30	250	70	100	195	60	53
Supply voltage (V)	1.1	1.2	1.2	1.3	1.2 / 1	1	1.6	1
SNDR at Nyquist (dB)	63.2	64.5	65.7	65.2	68.8	64.8	73.3	66
Total power (mW)	30.7	2.95	49.7	6.38	130	53	67.8	9
➢ FoM at Nyquist (dB)	158.3	161.6	159.7	162.6	154.7	157.5	159.7	160.7
Clock power (mW)	-	0.54	7.2	1.02	20	18	18	6.2
➢ Clock power/Total power		18%	14%	16%	15%	34%	26%	69%
Analog power (mW)	-	2.09	42.5	5.36	93	35	39	2.8
➢ FoM at Nyquist (dB)		163.1	160.4	163.3	156.1	159.3	162.2	165.8

FoM = SNDR + 10 $\log_{10}$ (Bandwidth / Power)

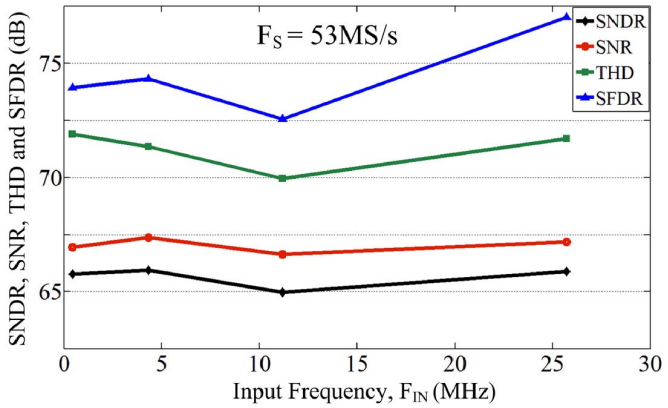

Fig. 14. Measured ADC performance versus input frequency at a clock speed of 53 MS/s.

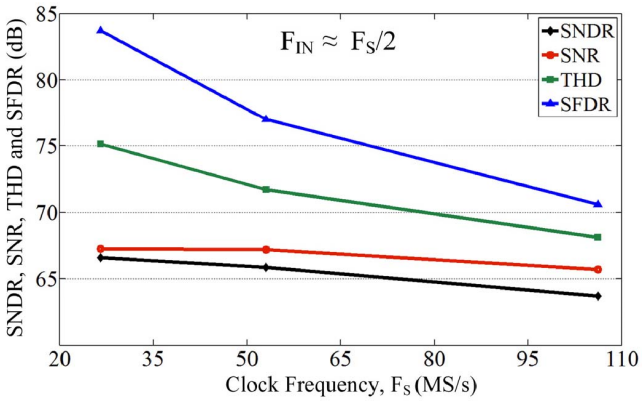

Fig. 15. Measured ADC performance versus clock frequency with input signal close to Nyquist.

reference voltages, as will be discussed later on in this section. Fig. 13 shows the ADC's INL (−0.7/+0.6 LSB) and DNL (−0.24/+0.14 LSB) after gain calibration. The INL profile indicates the existence of both sub-ranging and full-scale distortion, which is mainly caused by ISI or signal-dependent references. The finite linearity and residual gain error of the amplifiers will also contribute to these sub-ranging INL errors, but to a lesser extent.

Fig. 14 shows the ADC's measured performance at $F_S = 53$ MS/s as the frequency of the input signal is swept. Over the entire range, the ADC's SNDR is better than 65 dB. In addition, the ADC's performance at various clock frequencies is shown in Fig. 15 for near-Nyquist input signals. The performance degradation with increased F_S is due to the signal dependence of the ADC's reference voltage V_{REF}. At higher clock speeds, more signal-dependent charge is drawn from the on-chip reference capacitor C_{REF}. Because of this, reference voltage V_{REF} varies with the input signal, causing ISI and degrading linearity. A larger reference capacitor C_{REF} could mitigate this or, instead, the large chip area consumed by C_{REF} could be traded for an on-chip reference buffer that settles within 1 clock cycle, at the cost of extra power dissipation. Despite this ISI effect, the ADC achieves better than 64-dB SNDR with near-Nyquist inputs up to $F_S = 106$ MS/s.

The results of an amplitude sweep for near-Nyquist input signals at $F_S = 53$ MS/s are shown in Fig. 16. As expected, the ADC's SNR improves as the signal amplitude (V_{IN}) increases. Its SNDR also improves until the signal becomes large enough to degrade the linearity. Note that the curves of SFDR and total harmonic distortion (THD) versus V_{IN} experience a dip around −9 dBFS. This is due to the fact that for small input signals

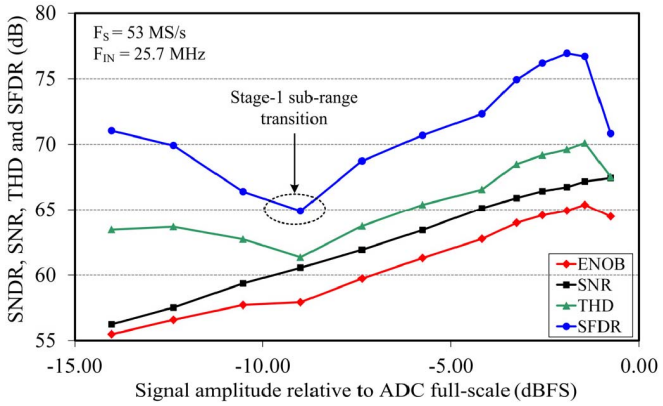

Fig. 16. Measured ADC performance as a function of input amplitude.

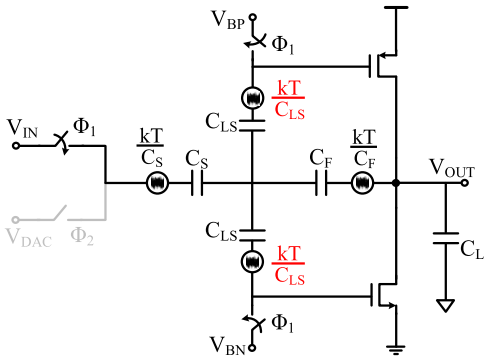

Fig. 17. Additional noise sources due to level-shifting capacitors C_{LS}.

(V_{IN} < stage-1 comparator threshold $V_{C,th}$), stage-1 residue signal is always in the mid-subrange. Therefore, no sub-range transitions take place, and so the corresponding transition jumps do not occur. As V_{IN} becomes larger, the residue signal of stage-1 spans all three sub-ranges, causing jumps at the sub-range transitions (due to gain error) and degraded linearity. However, when V_{IN} becomes even larger, these errors become relatively small, thus leading to improved linearity (i.e., SFDR and THD).

Excluding off-chip references, the ADC dissipates 9:2.8 mW analog power and 6.2-mW clock power. The rather large clock power is due to the reuse of a clock generator originally intended for operation at 1 GS/s [16]. The proposed residue amplifiers dissipate only 0.83 mW, which is 30% of the analog power and 9% of the overall ADC power.

Table I gives the performance summary and a comparison with state-of-the-art pipelined ADCs. Compared to [4], [14], [16], and [25], the proposed design requires the least number of calibration clock cycles, due to the use of the split-ADC technique and the fact that no nonlinearity correction is required. Mainly due to the high clock power, the ADC's overall power efficiency is only in line with the state-of-the-art. However, the proposed residue amplifier results in a significant reduction in its analog power. Compared to [16] which describes a similar ADC with a different residue amplifier, this paper achieves 4× better analog power efficiency. Compared to the other designs in Table I, it achieves a 1.8× improvement in analog power efficiency.

VII. Conclusion

A proof-of-concept pipelined split-ADC is fabricated in 40-nm CMOS that utilizes four main techniques to achieve both an excellent analog power efficiency and negligible calibration power dissipation.

1) A class-AB residue amplifier with a split-capacitor biasing technique is proposed. It sets the biasing of the NMOS and PMOS transistors independently of each other, eliminating additional level-shifting capacitors as well as their power penalty.
2) Linearity is ensured by biasing the amplifier's transistors in the strong-inversion saturation region and applying some feedback.
3) Incomplete settling is used to improve the amplifier's power efficiency.
4) Amplifier gain error is corrected by tuning its bias current, thus significantly reducing the calibration power.

The ADC achieves an SNDR/SFDR of 66/77.3 dB with near-Nyquist input at 53 MS/s clock speed and dissipates 9-mW power, of which the residue amplifiers consume only 0.83 mW.

Appendix A
Limitations of Using Extra Level-Shifting Capacitors

As discussed in Section II-A, the use of explicit level-shifting capacitors C_{LS}: 1) introduces kT/C noise; 2) attenuates the input signal; and 3) reduces the amplifier's feedback factor β. In this appendix, an analytical approach is used to explain each of these effects and a comparison is made with the proposed design.

A. Noise

The level-shifting capacitors C_{LS} sample kT/C noise at the end of the sampling phase Φ_1, similar to the sampling C_S and feedback C_F capacitors (Fig. 17). During the amplification phase Φ_2, these noise sources transfer to the amplifier output. Neglecting the amplifier's finite bandwidth and loop gain, the overall integrated output noise power at the end of the amplification phase Φ_2 can be expressed as

$$P_{\text{noise}} = \frac{kT}{C_S}\left(\frac{C_S}{C_F}\right)^2 + \frac{kT}{C_F} + \gamma\frac{kT}{C_L}\left(\frac{1}{\beta}\right) + 2\frac{kT}{C_{LS}}\left(\frac{1}{2\beta}\right)^2. \tag{5}$$

The last term in (5) is the noise contribution due to the two level-shifting capacitors C_{LS}, where $(1/2\beta)$ represents the gain of each kT/C_{LS} noise source from the NMOS or PMOS gate to the amplifier output. To reduce this noise contribution, the C_{LS} capacitor size must be increased. The proposed design, however, completely removes this additional noise contribution by eliminating C_{LS} capacitors and instead uses a split-capacitor technique (Section II-A) to perform the level-shifting operation.

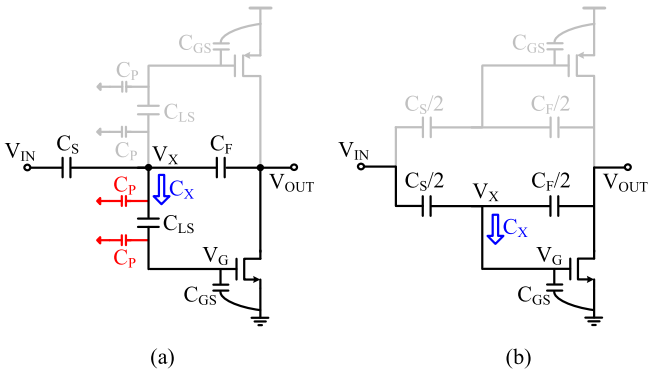

Fig. 18. Input signal and feedback factor attenuation for (a) additional capacitor level shifters C_{LS} and (b) proposed level-shifting solution.

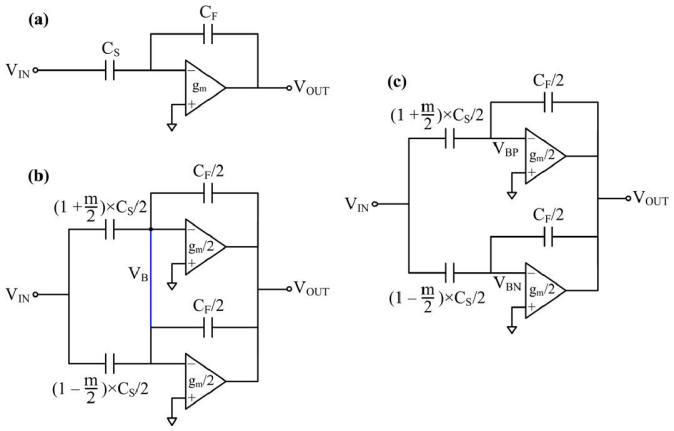

Fig. 19. (a) Negative feedback amplifier. (b) Splitting the amplifier in half. (c) Disconnecting the virtual ground nodes.

B. Signal Attenuation

The input signal has to pass through C_{LS} capacitors to drive the NMOS and PMOS transistor gates. Hence, C_{LS} capacitors need to be significantly larger than the amplifier's gate–source capacitance (C_{GS}) to avoid signal attenuation. Note that even if an ideal level shifter is used, there is always signal attenuation from the input of the amplifier (V_{IN}) to the transistor gate (V_G) because of finite C_{GS} capacitance. Hence, to analyze the effect of additional C_{LS} capacitors, the signal attenuation (α) is calculated from the virtual ground node (V_X) of the amplifier [Fig. 18(a)] to the transistor gate (V_G) as follows:

$$\alpha = 1 - \frac{V_G}{V_X} = \frac{C_P + C_{GS}}{C_{LS} + C_P + C_{GS}} \tag{6}$$

where C_P is the parasitic capacitance due to C_{LS} capacitor. In contrast, the proposed design [Fig. 18(b)] does not lose signal from the virtual ground node to the transistor gate ($V_G = V_X$) as there is no extra level-shifting capacitors C_{LS}.

C. Reduction in Feedback Factor

Although increasing C_{LS} capacitor size reduces noise and signal attenuation, it adds more parasitic capacitance C_P at the virtual ground node [Fig. 18(a)]. Thus, the amplifier's feedback factor reduces, degrading its bandwidth and loop gain. The feedback factor β of the amplifier is given by

$$\beta = C_F/(C_S + C_F + 2C_X) \tag{7}$$

where C_X is the equivalent capacitance looking into the level shifters, as shown in Fig. 18. Note that parasitic capacitances from the sampling and feedback capacitors are not considered as they are similar in both cases. For the class-AB amplifier with capacitor level shifters [Fig. 18(a)], C_X is considerably larger due to the added parasitic capacitance C_P as follows:

$$C_X = \frac{C_{LS}(C_P + C_{GS})}{C_{LS} + C_P + C_{GS}} + C_P. \tag{8}$$

The proposed class-AB amplifier exhibits a higher feedback factor β since capacitance C_X is the same as the amplifier's gate–source capacitance C_{GS}, i.e., $C_X = C_{GS}$.

APPENDIX B
GAIN ERROR AND DNL DUE TO SPLIT-CAPACITOR MISMATCH

Consider the simple inverting amplifier shown in Fig. 19(a). To simplify the discussion, the effect of its finite loop gain and bandwidth is ignored. Fig. 19(b) shows the circuit of Fig. 19(a) split into two half circuits, where m is introduced to analyze the effect of mismatch between the two half circuits. ($m = 0$ indicates no mismatch.) Disconnecting the virtual ground nodes of the two split amplifiers allows them to have independent input bias (V_{BN} and V_{BP}), as shown in Fig. 19(c). The circuit in Fig. 19(c) is a model of the proposed split-capacitor technique that biases the amplifier's NMOS and PMOS sides without using additional level shifters. If the split capacitors are perfectly matched ($m = 0$), then the amplifiers in Fig. 19(b) and (c) will behave in the same way.

Introducing a mismatch (m) in split capacitors does not cause gain error in the amplifier of Fig. 19(b), assuming that the overall capacitance is still the same. However, it will result in a gain error for the amplifier of Fig. 19(c) as the virtual ground nodes are not connected. Using the principle of superposition, gain G of the amplifier of Fig. 19(c) can be derived as follows:

$$G = -\frac{C_S}{C_F}\left(1 - \left(\frac{m}{2}\right)^2 \times \frac{C_S}{C_S + C_F}\right). \tag{9}$$

The relative error in gain (ε_{ge}) is given by

$$\varepsilon_{ge} = \left(\frac{m}{2}\right)^2 \times \frac{C_S}{C_S + C_F}. \tag{10}$$

Since the effect of mismatch between the two half circuits is quadratic [as can be seen in (10)] and m is much smaller than 1, the resulting gain error ε_{ge} is negligible. However, because of this gain error, there could be jump (DNL) or missing code in the ADC transfer. The magnitude of DNL depends on gain error ε_{ge} as well as the number of bits yet to be resolved from the back end ($B_{\text{back end}}$), and can be approximated as follows:

$$\text{DNL (due to gain error)} = \varepsilon_{ge} \times 2^{B_{\text{backend}}}. \tag{11}$$

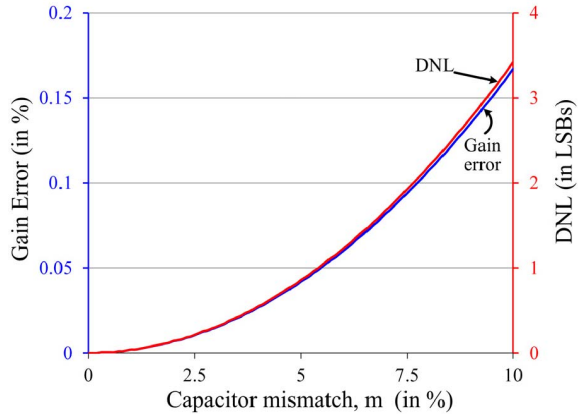

Fig. 20. Simulated gain error and DNL because of split-capacitor mismatch.

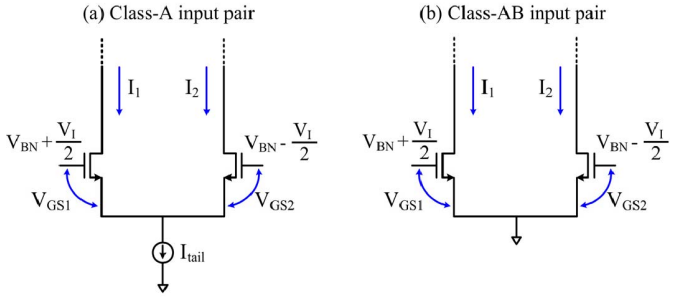

Fig. 21. Differential pairs with (a) tail current source and (b) grounded source nodes.

Fig. 20 shows the simulated gain error and DNL due to the mismatch (m) in split capacitors, assuming that $B_{\text{backend}} = 11$ bits. In 40-nm CMOS technology, it is quite straightforward to achieve better than 1% matching for sub-picofarad capacitors. However, even if the mismatch is 5%, the resulting gain error will still be around 0.05% and the DNL will be less than 1 LSB. Therefore, the mismatch in the split capacitors does not limit the performance of the ADC. Moreover, this design uses gain calibration to correct the residue amplifier gain error and hence removes the DNL caused by it.

Appendix C
V–I Characteristics of Class-A and Class-AB Differential Pairs

Fig. 21 shows class-A and class-AB differential pairs, which are biased in the strong-inversion saturation region. In this Appendix, the V–I transfer of both the input pairs is analyzed to compare their linearity or large signal behavior. To simplify the analysis, a quadratic V–I characteristic is assumed for the MOSFETs. For both pairs, the differential output current changes with the input voltage as follows:

$$I_{\text{DIFF}} = I_1 - I_2 = \frac{\beta_n}{2}[(V_{\text{GS1}} - V_{\text{th}})^2 - (V_{\text{GS2}} - V_{\text{th}})^2] \quad (12)$$

where $\beta_n = \mu_n C_{\text{ox}}(W/L)$, and V_{th} is the threshold voltage of the transistor. Assuming $P = V_{\text{GS1}} - V_{\text{th}}$ and $Q = V_{\text{GS2}} - V_{\text{th}}$,

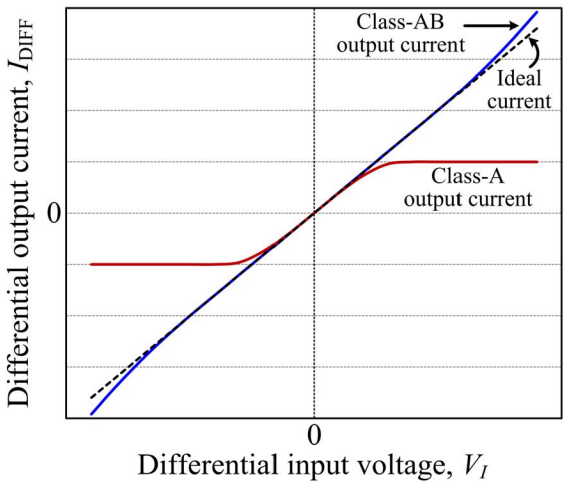

Fig. 22. V–I characteristics of the two differential pairs.

(12) can be rewritten as

$$I_{\text{DIFF}} = \frac{\beta_n}{2}[P^2 - Q^2] = \frac{\beta_n}{2}(P+Q)(P-Q)$$
$$\Rightarrow I_{\text{DIFF}} = \frac{\beta_n}{2}(P+Q)V_I \quad (13)$$

where $(P - Q) = V_I$ is the differential input voltage. Now, the expression of $(P + Q)$ for both the input pairs needs to be derived.

For the class-A differential pair with a tail current source [Fig. 21(a)], the sum of the currents $(I_1 + I_2)$ is equal to tail current I_{tail} as follows:

$$I_{\text{tail}} = I_1 + I_2 = \frac{\beta_n}{2}[P^2 + Q^2]$$
$$\Rightarrow I_{\text{tail}} = \frac{\beta_n}{2}\left[\frac{(P+Q)^2}{2} + \frac{(P-Q)^2}{2}\right]$$
$$\Rightarrow (P+Q) = \sqrt{\frac{4I_{\text{tail}}}{\beta_n} - V_I^2}. \quad (14)$$

Substituting the expression of $(P + Q)$ from (14) into (13) results in

$$I_{\text{DIFF}} = \frac{1}{2}\beta_n V_I \sqrt{\frac{4I_{\text{tail}}}{\beta_n} - V_I^2}. \quad (15)$$

Taylor series expansion of (15) indicates third and higher order harmonics in the differential output current I_{DIFF}, whereas individual MOSFET currents contain only second-order harmonic component. This is because the source nodes of the input transistors (i.e., the drain of the tail current source) vary nonlinearly with the input signal.

For the class-AB differential pair, the source nodes are connected to the ground instead of a current source [Fig. 21(b)]. So, the sum $(P + Q)$ can be expressed as

$$(P+Q) = \left(V_{\text{BN}} + \frac{V_I}{2} - V_{\text{th}}\right) + \left(V_{\text{BN}} - \frac{V_I}{2} - V_{\text{th}}\right)$$
$$= 2(V_{\text{BN}} - V_{\text{th}}) \quad (16)$$

where both the biasing voltage V_{BN} and threshold voltage V_{th} are constants. Consequently, the sum $(P + Q)$ is also a constant and the output current I_{DIFF} changes linearly with input voltage V_I as follows:

$$I_{\mathrm{DIFF}} = \beta_n V_I (V_{\mathrm{BN}} - V_{\mathrm{th}}). \tag{17}$$

The above discussion shows analytically that the differential pair with grounded source nodes (i.e., class-AB amplifier) is more linear than that with a tail current source (i.e., class-A amplifier). Fig. 22 graphically illustrates this by plotting the differential output current as a function of the differential input voltage. The same bias current is considered for both the amplifiers. Since the current in a class-A amplifier is limited by the tail current source, the output current experiences a large error as the input voltage is increased. The linear range of the amplifier can be widened by increasing tail current I_{tail}, i.e., at the expense of power dissipation. In contrast, the output current in a class-AB amplifier is not limited by any fixed current source. Therefore, it can provide larger output current and so is more linear than a differential pair with a tail current source for the same power dissipation.

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Dr. Bult is an author of more than 60 international publications and holds more than 60 issued U.S. patents. He is a Broadcom Fellow, an IEEE Fellow, was awarded the Lewis Winner Award for outstanding conference paper on ISSCC 1990, 1992 and 1997, was co-recipient of the Jan Van Vessem Best European Paper Award at ISSCC 2004 and the Distinguished Paper Award of ISSCC 2014. He was also awarded the ISSCC Best Evening Panel Award in 1997 and 2006 and the Best Forum Speaker Award at ISSCC 2011. He has served more than 12 years on the ISSCC Technical Program Committee, 18 years on the ESSCIRC Technical Program Committee and 7 years as a member of the ESSCIRC/ESSDERC Steering Committee.