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A 0.9-V 28-MHz Highly Digital CMOS Dual-*RC* Frequency Reference With ±200 ppm Inaccuracy From −40 °C to 85 °C

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***Abstract*— This article presents an energy-efficient dual-*RC* frequency reference intended for wireless sensor nodes. It consists of a digital frequency-locked loop (FLL) in which the frequency of a digitally controlled oscillator (DCO) is locked to a temperature-independent phase shift derived from two different *RC* poly-phase filters (PPFs). Phase shifts with complementary temperature coefficients (TCs) are generated by using PPFs made from different resistor types (p-poly and silicided p-poly). The phase shift of each filter is determined by a zero-crossing (ZC) detector and then digitized by a digital phase-domain ΔΣ modulator (Φ-ΔΣM). The results are then combined in the digital domain via fixed polynomials to produce a temperature-independent phase shift. This highly digital architecture enables the use of a sub-1-V supply voltage and enhances energy and area efficiency. The 28-MHz frequency reference occupies 0.06 mm^2 in a 65-nm CMOS process. It achieves a period jitter of 7 ps (1σ) and draws 142 μW from a 0.9-V supply, which corresponds to an energy consumption of 5 pJ/cycle. Furthermore, it achieves ±200 ppm inaccuracy from −40 °C to 85 °C after a two-point trim.**

***Index Terms*— CMOS frequency reference, digital frequency-locked loop (FLL), digital phase-domain ΔΣ modulator (Φ-ΔΣM), digitally assisted, *RC* poly-phase filter (PPF), temperature compensation, trimming, wireless sensor node, zero-crossing (ZC) detector.**

I. Introduction

WIRELESS sensor nodes in battery-powered Internet-of-Things (IoT) applications, such as Bluetooth Low Energy (BLE), require stable on-chip frequency references with low energy consumption (<10 pJ/cycle) and high frequency stability (<±300 ppm) [1]. For radio applications, 24-MHz quartz crystal oscillators are widely used as PLL reference clocks. Although they can provide excellent frequency stability over process, voltage, and temperature (PVT) variations, quartz crystals cannot be integrated in standard CMOS. As a result, their use increases system cost and size, which can be a bottleneck for miniaturized IoT sensor nodes. Microelectromechanical systems (MEMS) and bulk acoustic wave (BAW) resonators are gaining popularity because they can be co-packaged with a CMOS die while also achieving high stability. However, their use still incurs extra packaging complexity and thus cost [2], [3].

To overcome this, the use of CMOS frequency references has been widely investigated. These produce an output frequency that is locked to the time delay or phase shift of on-chip electric components. For instance, *LC* frequency references can be implemented with inaccuracies of less than ±120 ppm from −50 °C to 170 °C [4]. Nevertheless, these typically operate at several gigahertz and thus consume milliwatts of power. References based on thermal diffusivity (TD) are locked to the rate at which heat diffuses through bulk silicon [5], [6]. Although this is quite well defined in advanced lithography technology, they require heaters that typically dissipate a few milliwatts and only achieve moderate inaccuracy: ±1000 ppm over the military temperature range (−55 °C–125 °C).

Due to their low-cost integration and high energy efficiency, several *RC* frequency references have been proposed [7]–[16]. However, the temperature coefficient (TC) of on-chip resistors is typically quite large (>100 ppm/°C), and thus, the inaccuracy of on-chip *RC* time constant is typically limited to a few percent over temperature. This can be significantly reduced by combining resistors with opposite TCs. Due to process spread, however, the resulting composite resistors require trimming at multiple temperatures, typically via an analog switch matrix [11], [16]. Furthermore, the finite resolution of the matrix and the ON-resistance of the switches limits the inaccuracy of the resulting references to about ±1% over the industrial temperature range [17]. Recently, significantly lower inaccuracy (∼±200 ppm) has been achieved with digital temperature compensation schemes [7]–[10], [12]–[15].

This article presents a highly digital dual-*RC* frequency reference, which is fabricated in a 65-nm CMOS process and achieves an inaccuracy of ±200 ppm from −40 °C to 85 °C and a period jitter of 7 ps (1σ) and consumes an energy of 5 pJ/cycle at 28 MHz while only occupying 0.06 mm^2. This is achieved by applying a digital temperature compensation

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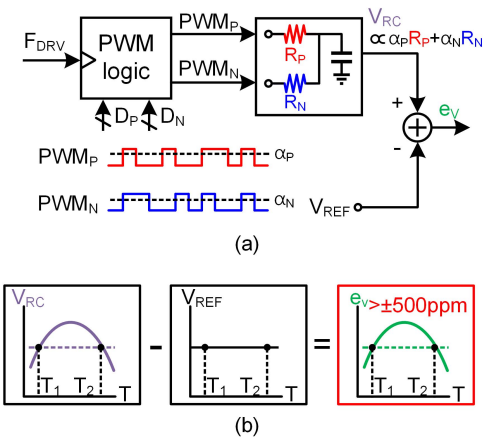

Fig. 1. Switched-resistor trimming based on the pulsewidth modulation. (a) Block diagram. (b) Resulting temperature inaccuracy.

scheme to a digital frequency-locked loop (FLL), whose main building blocks are a highly digital phase-domain $\Delta\Sigma$ modulator (Φ-$\Delta\Sigma$M) and an area-efficient $\Delta\Sigma$-based digitally controlled oscillator (DCO). This article is an extended version of [15] and includes a detailed analysis and description of the proposed frequency reference.

This article is organized as follows. Section II describes previous frequency references with digital temperature compensation schemes, while Section III explains the overall architecture of the proposed dual-*RC* frequency reference. Section IV describes the features of the proposed digital Φ-$\Delta\Sigma$M. In Section V, the implementation details about the DCO are presented. Section VI presents the measurement results. Finally, the article ends with conclusions.

II. Digital Temperature Compensation Schemes

A. Switched-Resistor Trimming

Instead of using an analog switch matrix to trim a composite resistor, a switched-resistor trimming scheme can be used [7]–[9]. As shown in Fig. 1, the effective resistance of two parallel-connected resistors with complementary TCs (R_P and R_N) can be trimmed by switches driven by pulsewidth modulation (PWM) signals (PWM_P and PWM_N). Their pulse densities (α_P and α_N) can then be chosen to zero the TC of the resulting composite resistor and, hence, an *RC* filter. The required pulse densities can be determined by a two-point calibration. This approach results in a frequency reference with low energy consumption of ~1 pJ/cycle. However, its inaccuracy is limited to ~±530 ppm by the resistors' higher order TCs. In [9], lower inaccuracy (±140 ppm) is achieved by using a composite resistor made from three different switched resistors. However, this requires a more expensive three-point calibration.

B. Digital Linear Compensation

Alternatively, a digital temperature sensor (TS) and a high-order compensation polynomial [$p_P(\cdot)$] can be used to generate a phase reference (μ_T) whose temperature dependence accurately matches that of the phase shift of an *RC* filter [5], [6]. As shown in Fig. 2, to facilitate comparison in the digital domain, the filter's phase shift (μ_P) is first digitized by a high-resolution analog Φ-$\Delta\Sigma$M. In [12] and [13], the order of the compensation polynomial is significantly reduced by employing a resistor-based TS whose digital output has a non-linear temperature dependence that is very similar to that of an *RC* filter's phase shift. In [12], a linear polynomial is then sufficient to achieve an inaccuracy of ±400 ppm from −40 °C to 85 °C after a two-point calibration. In [13], somewhat better inaccuracy (±200 ppm) is achieved with a higher order compensation polynomial.

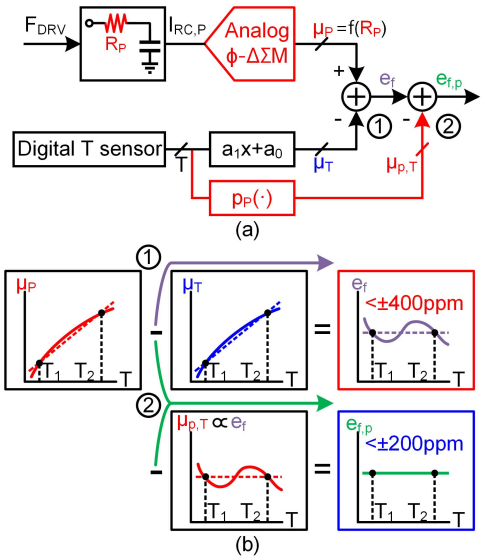

Fig. 2. Digital linear compensation with the digital TS. (a) Block diagram. (b) Resulting temperature inaccuracy.

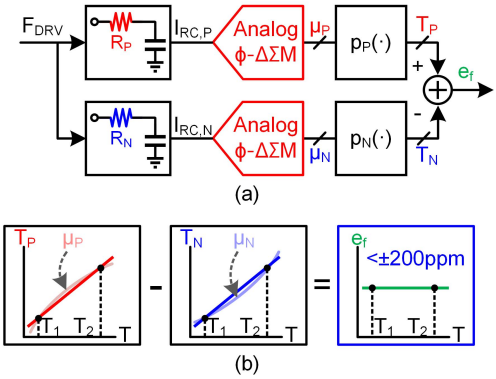

Fig. 3. Dual *RC*-based digital compensation. (a) Block diagram. (b) Resulting temperature inaccuracy.

C. Dual RC-Based Digital Compensation

A somewhat simpler approach, which eliminates the need for the explicit TS, is the dual-*RC* architecture [14]. Here, the phase shifts of two *RC* filters with complementary TCs are digitized and then appropriately combined to accurately cancel their temperature dependencies. As shown in Fig. 3, each non-linear phase shift is digitized by an analog Φ-$\Delta\Sigma$M, and its output $\mu_{P,N}$ is fed to a digital linearizing polynomial $p_{P,N}(\cdot)$. This polynomial compensates for the individual

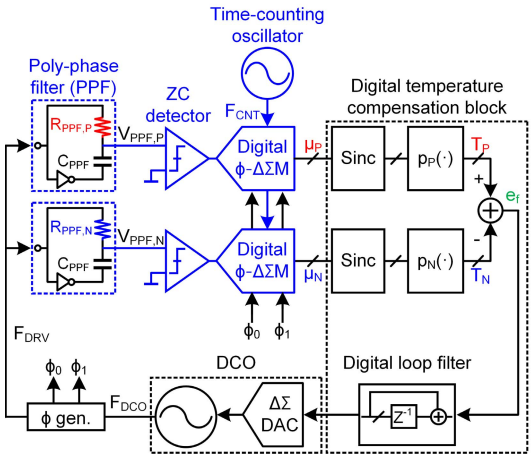

Fig. 4. Proposed dual RC-based frequency reference.

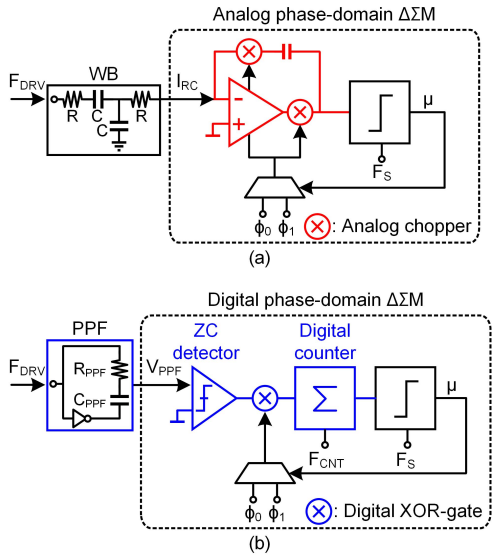

Fig. 5. Comparison of (a) conventional analog Φ-ΔΣM and (b) proposed digital Φ-ΔΣM.

high-order TCs of μ_P (or μ_N), producing linear functions of temperatures (T_P and T_N), which can then be combined to produce a temperature-independent phase reference (e_f). With this approach, an inaccuracy of ±200 ppm from −40 °C to 85 °C was achieved.

However, this architecture requires two analog high-resolution Φ-ΔΣMs, one for each of the two RC filters, and thus consumes considerable energy and area (107 pJ/cycle and 1.65 mm^2 in [14]). The goal of the proposed frequency reference is to maintain the excellent accuracy of the dual-RC architecture while also significantly improving its energy and area efficiency.

III. Proposed Dual-RC Frequency Reference

A. Operating Principle

The proposed dual-RC frequency reference (see Fig. 4) consists of a digital FLL, in which the output frequency of a DCO is locked to a temperature-independent phase shift derived from two RC PPFs. Note that compared to the Wien bridge (WB) filters used in [12]–[14], the use of a PPF

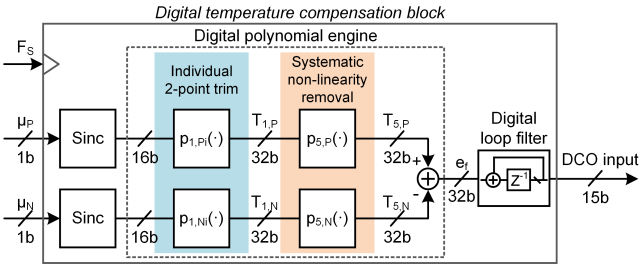

Fig. 6. Digital temperature compensation block: decimation filter, digital polynomial engine, and digital loop filter.

requires fewer components (4 instead of 7) and results in a larger output voltage swing and TC [18]. Phase shifts with complementary TCs are generated by using PPFs made from different resistor types (p-poly and silicided p-poly). These are digitized by digital Φ-ΔΣMs, which consists of a zero-crossing (ZC) detector [18], a digital counter clocked by a time-counting oscillator's output F_{CNT}, and some digital logic. The bitstream (BS) outputs (μ_P and μ_N) of the Φ-ΔΣMs are decimated by sinc filters and then linearized by digital polynomials. The resulting complementary phase shifts (T_P and T_N) are combined to generate a temperature-independent frequency error e_f. At steady state, e_f is driven to zero by a digital loop filter so that the DCO's output frequency F_{DCO} (=28 MHz) is not affected by the temperature drift.

Fig. 5 compares a conventional analog Φ-ΔΣM with the proposed digital Φ-ΔΣM. The chopper phase detector of the analog Φ-ΔΣM used in [12]–[14] [see Fig. 5(a)] is replaced by a ZC detector and a digital XOR gate. The XOR gate [see Fig. 5(b)] detects the phase difference between the ZCs of the PPF and the reference phases (Φ_0 and Φ_1) selected by the BS μ. Its output is then integrated by a digital counter clocked by a high-frequency clock F_{CNT} (∼280 MHz), which replaces an area-inefficient analog integrator. This highly digital architecture allows Φ-ΔΣM to operate at a supply voltage below 1 V, further improving its energy efficiency.

B. Digital Temperature Compensation

As shown in Fig. 6, the output BSs (μ_P and μ_N) of each Φ-ΔΣM are decimated by sinc filters, each implemented as a 16-bit up counter that realizes the target conversion rate of 3 Hz. To compensate for the effect of process spread on the PPFs, the decimated outputs are first applied to the first-order polynomials ($p_{1,\mathrm{Pi}}$ and $p_{1,\mathrm{Ni}}$), whose coefficients are obtained from a two-point calibration. The systematic non-linearity in the resulting temperature-dependent outputs ($T_{1,P}$ and $T_{1,N}$) is then removed by fixed fifth-order polynomials ($p_{5,P}$ and $p_{5,N}$), resulting in linear functions of temperature ($T_{5,P}$ and $T_{5,N}$). These are then subtracted to derive the frequency error signal e_f that drives the digital loop filter (a 32-bit accumulator). To minimize numerical errors, all the polynomials are implemented with 32-bit floating-point arithmetic. Eventually, the 32-bit floating-point word of the accumulator output is converted into the 15-bit fixed-point word to drive the DCO. A truncation error from 1 LSB of the word may result in a 360-Hz frequency drift, which will be introduced in Section V.

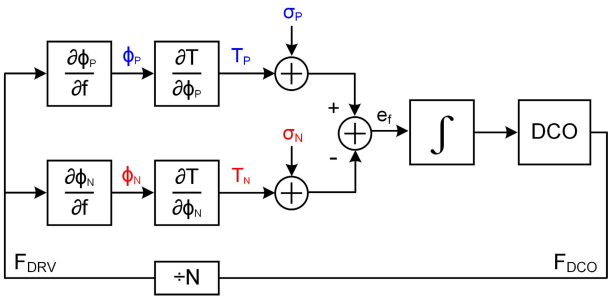

Fig. 7. Linearized model of the dual *RC*-based FLL.

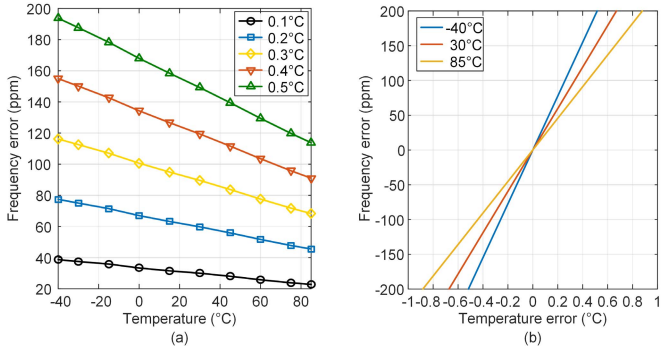

Fig. 8. Simulated frequency error over (a) temperature by a fixed absolute temperature measurement error and (b) temperature error at three temperature points.

This corresponds to 13 ppm of the output frequency and is a negligible error.

C. Requirements for Temperature Errors

A linearized model of the proposed dual *RC*-based FLL at a steady-state frequency f_0 is shown in Fig. 7, where the derivatives $\delta\phi_{P,N}/\delta f$ and $\delta T/\delta\phi_{P,N}$ represent the frequency-to-phase gain and the phase-to-temperature gain of each PPF, respectively. Resistor spread and ZC detector offset will cause errors in the ZC outputs and, hence, in the temperature outputs (T_P and T_N) of the digital Φ-ΔΣMs. This, in turn, will degrade the accuracy of the output frequency.

Denoting the temperature errors due to resistor spread in the two PPFs as σ_N and σ_P, the relative frequency error is given by [14]

$$\frac{\sigma_f}{f_0} = \frac{\sqrt{\sigma_P^2+\sigma_N^2}}{f_0}\cdot\left|\frac{1}{\frac{\delta\phi_P}{\delta f}\frac{\delta T}{\delta\psi_P}-\frac{\delta\phi_N}{\delta f}\frac{\delta T}{\delta\psi_N}}\right| = \frac{\sqrt{\sigma_P^2+\sigma_N^2}}{\left|\frac{1}{\mathrm{TC}_P}-\frac{1}{\mathrm{TC}_N}\right|} \quad (1)$$

where σ_f denotes the output frequency error, the derivative $\delta T/\delta\psi_{P,N}$ is the phase-to-temperature gain of each PPF at f_0, and $\mathrm{TC}_{P,N}$ are the TCs of the two resistors. From (1), it can be seen that the relative frequency error can be minimized if the two TCs have opposite polarities. In the chosen 65-nm CMOS process, this consideration led to the choice of p-poly resistor ($\mathrm{TC}_N = -0.032\%/°\mathrm{C}$ at 30°C) and silicided p-poly resistor ($\mathrm{TC}_P = 0.24\%/°\mathrm{C}$ at 30 °C).

The effect of the errors σ_N and σ_P on the output frequency was verified by simulations of the system shown in Fig. 7. The PPF's frequency-to-phase and phase-to-temperature gains were determined by the circuit-level simulation. As shown in Fig. 8(a), a temperature error of 0.1 °C results in frequency errors of 39, 30, and 23 ppm at −40 °C, 30 °C, and 85 °C, respectively. This agrees well with (1), which predicts that 0.1 °C errors in either σ_P or σ_N will result in frequency errors of 38, 28, and 23 ppm at −40 °C ($\mathrm{TC}_P = 0.32\%/°\mathrm{C}$ and $\mathrm{TC}_N = -0.043\%/°\mathrm{C}$), 30 °C ($\mathrm{TC}_P = 0.24\%/°\mathrm{C}$ and $\mathrm{TC}_N = -0.032\%/°\mathrm{C}$), and 85 °C ($\mathrm{TC}_P = 0.2\%/°\mathrm{C}$ and $\mathrm{TC}_N = -0.026\%/°\mathrm{C}$), respectively. Since the TCs are temperature-dependent, the resulting frequency error is also temperature-dependent, as shown in Fig. 8(b). The worst case situation occurs at −40 °C. Therefore, to achieve the target frequency inaccuracy (<±200 ppm) from −40 °C to 85 °C, the temperature errors should be less than ±0.5 °C at −40 °C but can be ∼1.7× greater at 85 °C.

IV. Proposed Digital Φ-ΔΣM

A. Operating Principle

Fig. 9(a) shows the schematic of the proposed digital Φ-ΔΣM. The PPF ($R_{\mathrm{PPF}} = 120$ kΩ and $C_{\mathrm{PPF}} = 8.4$ pF) is driven by F_{DRV} ($=F_{\mathrm{DCO}}/128 = 218.75$ kHz), which is the same as the sampling frequency F_S and the frequency at the output of the phase DAC F_{DAC}. The ZC detector senses the ZC points of the PPF's differential outputs (V_{PPF}). As shown in Fig. 9(b), the phase difference F_{XOR} between the ZC detector output F_{ZCD} and F_{DAC} is detected by the XOR gate and integrated by a 13-bit up/down counter. The counter's MSB, i.e., its output polarity, is then sampled by F_S with +45° phase shift to create the desired demodulation signal at the F_{DAC}. Finally, the resulting BS controls the phase references in a ΔΣ manner. To cover the full range of the phase shift of both PPFs over temperature, the phase references Φ_0 and Φ_1 are set by digital logic to ±22.5° (with respect to F_{DRV}).

B. Time-Quantization Noise of the Counter

The digital Φ-ΔΣM uses an up/down counter as an integrator, which only counts integer values and thus introduces quantization errors at the end of each up/down cycle [19]. To minimize this time-quantization noise, the counter clock F_{CNT} needs to be carefully chosen. In the proposed frequency reference, the simplest way of generating F_{CNT} would be to use the DCO output. As shown in Fig. 10(a) [20], [21], if the DCO consists of an N-stage ring oscillator, and then, the edges of each of its stages can be combined to generate $F_{\mathrm{CNT}} = N \cdot F_{\mathrm{DCO}}$. In this case, however, the up/down signal F_{XOR} is exactly synchronized with F_{CNT}, i.e., the period (t_{IN}) of F_{XOR} is $2N$ times that of F_{CNT} (t_{CNT}), and thus, the counter can only change by N different values during a single ΔΣ cycle [see Fig. 10(b)]. This limits the resolution of the modulator, as shown in Fig. 10(c). To achieve the target temperature resolution of <10 mK for both PPFs, a phase resolution of 0.14 m° is required for the digital Φ-ΔΣM. To meet this requirement, F_{CNT} would then have to be greater than 560 GHz, which is not realistic.

In this work, however, a free-running oscillator implemented by a current-controlled oscillator (CCO) generates a counter clock F_{CNT}, which is asynchronous to F_{XOR}, as shown in

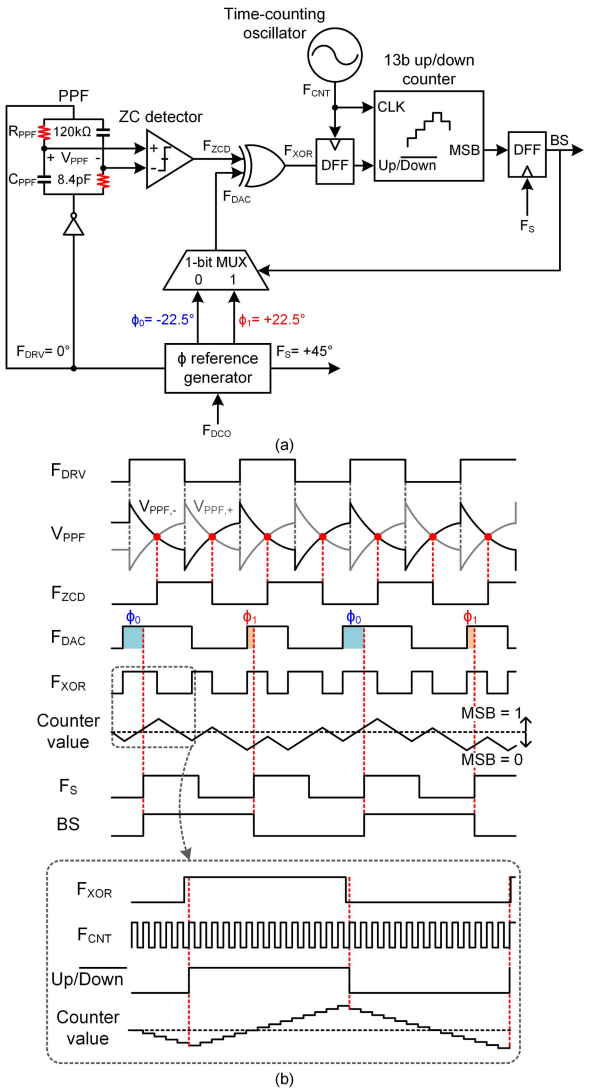

Fig. 9. Proposed digital Φ-ΔΣM. (a) Schematic. (b) Operating timing diagram.

Fig. 11(a). Fig. 11(b) shows the resulting timing relationship between the up/down signal and F_{CNT}. In the example shown, although the phase of F_{CNT} changes by 4.2 cycles in the first up-counting period, this is truncated by the counter to four cycles. The resulting time-quantization error will propagate to the start of the next down-counting period. Since F_{CNT} is asynchronous to F_{XOR}, these counting errors will be relatively random and can be modeled as an additive white-noise source. With $t_{\mathrm{IN}} \approx N \cdot t_{\mathrm{CNT}}$, the counter randomly outputs the surrounding values around N, whose standard deviation σ_{CNT} is much smaller than t_{CNT} [see Fig. 11(c)]. Consequently, unlike the case when $t_{\mathrm{IN}} = N \cdot t_{\mathrm{CNT}}$, this case will, on average, have higher resolution, limited only by the time-quantization noise associated with F_{CNT}. Since this noise occurs at the input of the integrator, it will not be shaped. To check its impact on the phase resolution of the Φ-ΔΣM, the in-band phase noise referred to the input of the XOR gate for a bandwidth F_{BW} is derived in the Appendix and is given by

$$\sigma_{\mathrm{PHASE}} = \sqrt{\frac{2}{3 \cdot \mathrm{OSR}}} \cdot \frac{F_{\mathrm{DRV}}}{F_{\mathrm{CNT}}} \tag{2}$$

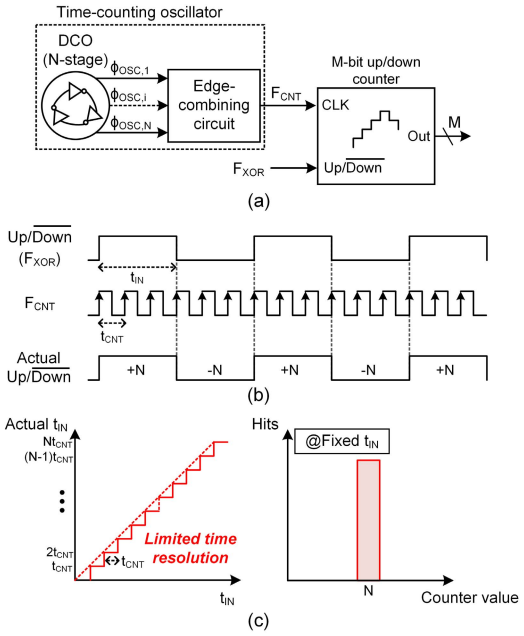

Fig. 10. (a) Schematic of the up/down counter clocked by the F_{CNT} generated from the internal DCO. (b) Timing diagram of the up/down signal and the F_{CNT}. (c) Time detection range and hit map of the counter.

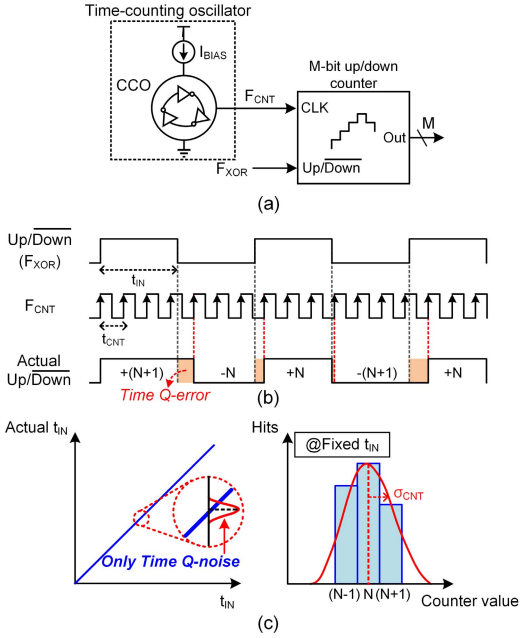

Fig. 11. (a) Schematic of the up/down counter clocked by the F_{CNT} generated from the free-running oscillator. (b) Timing diagram of the up/down signal and F_{CNT}. (c) Time detection range and hit map of the counter.

where the over-sampling ratio (OSR) of the Φ-ΔΣM is calculated as the ratio $F_{\mathrm{DRV}}/2F_{\mathrm{BW}}$. It can be seen that this noise is reduced by increasing the OSR. In this work, F_{DRV} of the PPF, which limits the modulator's sampling frequency, is chosen to be 218.75 kHz and F_{CNT} of the time-counting oscillator is set to ~280 MHz. Considering the desired conversion rate of 3 Hz, the temperature resolution of Φ-ΔΣM is estimated to be less than 10 mK, thereby satisfying the target temperature resolution.

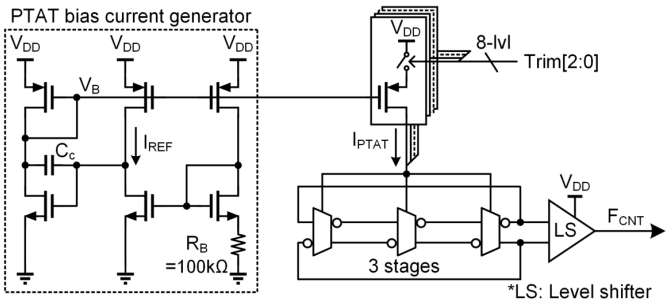

Fig. 12. Schematic of the time-counting oscillator.

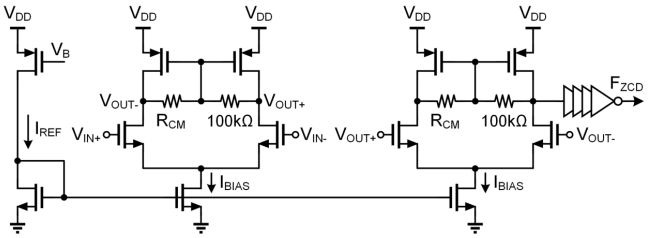

Fig. 13. Schematic of the ZC detector.

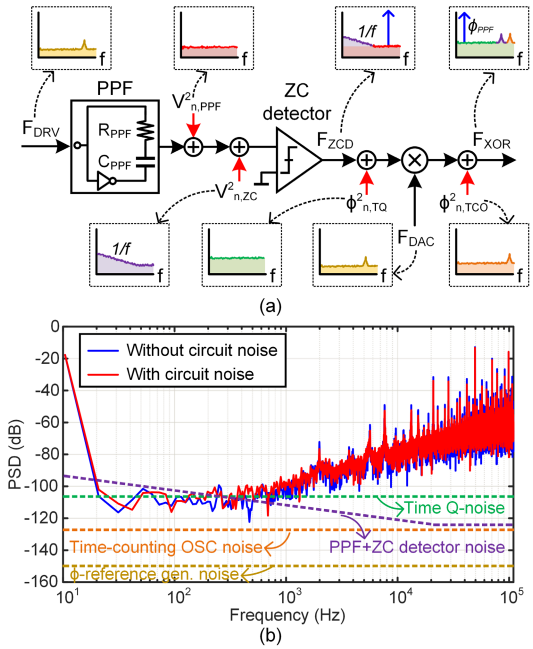

Fig. 14. (a) Noise sources of the proposed digital Φ-ΔΣM. (b) Simulated PSDs of the digital Φ-ΔΣM with and without the circuit noise.

C. Time-Counting Oscillator

Fig. 12 shows the schematic of the time-counting oscillator. It is designed as a three-stage CCO, which is biased with a supply-insensitive proportional-to-absolute-temperature (PTAT) current source and generates the output frequency F_{CNT}. Since the temperature drift of the PTAT current directly changes F_{CNT}, it may degrade the phase resolution of Φ-ΔΣM. From simulations, however, since F_{CNT} deviates by ±14% across temperature variation, the resolution can only vary from 8.6 to 11.4 mK, based on the value of 10 mK. A resolution variation of ±1.4 mK can be negligible. To compensate for the process variations in F_{CNT}, a 3-bit current DAC is used to adjust it to the nominal frequency of 280 MHz with 14-MHz least-significant bit (LSB) control. The time-counting oscillator dissipates 39.9 μW from a 0.9-V supply.

D. Up/Down Counter

Since the up/down counter operates as an integrator and is not reset periodically, it can wrap around (or overflow) [19]. Therefore, the counter size should be chosen carefully. After one period of the PPF's driving signal F_{DRV}, the maximum counter value C_{MAX} is expressed as

$$C_{\mathrm{MAX}} = \pm\frac{F_{\mathrm{CNT}}}{\pi F_{\mathrm{DRV}}} \cdot (\phi_{\mathrm{PPF}} - \phi_{\mathrm{DAC}}). \tag{3}$$

As shown in Fig. 9(b), at steady state, the counter state increments or decrements around approximately half of the maximum code. As long as C_{MAX} is less than half the maximum code, counter wrap-around does not happen. From (3), the larger the difference between the PPF's phase shift ϕ_{PPF} and that of the phase DAC output ϕ_{DAC}, the larger C_{MAX} will be. From simulations, ϕ_{PPF} will vary by ∼21° over the operating temperature range, and the maximum phase is ∼97° from Monte Carlo simulations. Given that $\phi_{\mathrm{DAC}} = -22.5°$, $F_{\mathrm{CNT}} = 280$ MHz, and $F_{\mathrm{DRV}} = 218.75$ kHz, C_{MAX} is estimated as ±853. It is, therefore, necessary to use at least an 11-bit counter. Accounting for the variations of F_{CNT}, due to the finite resolution of the trimming DAC, a 13-bit counter was chosen. In addition, to avoid the meta-stability of the counter, the counter's up/down signal F_{XOR} is reclocked by F_{CNT}, as shown in Fig. 9(b). All digital blocks related to the counter were synthesized using the standard cells provided in a 65-nm CMOS process and drawn only 15.6 μW from a 0.9-V supply.

E. ZC Detector

Fig. 13 shows the schematic of the ZC detector, which is basically a two-stage comparator and has an output buffer. The comparator stage consists of an nMOS input pair with pMOS loads and a resistive common-mode feedback (CMFB), which makes it insensitive to the common-mode variations of the PPF's output. The size of the input transistor is carefully designed to reduce the kickback on the PPFs. This results in an output frequency error of <480 ppm as the supply voltage varies from 0.85 to 1.05 V. The comparator consumes 5.3 μA biased from the PTAT current source and has a gain of 20.8 dB and a bandwidth of 127 MHz. From Monte Carlo simulations, the offset voltage of the ZC detector deviates by ±25 mV, and it can be translated into the phase error of ±1.2° at the ZC detector output F_{ZCD}, which will shift the Φ-ΔΣM output over temperature. Finally, after a two-point trim, it will lead to a temperature error of ∼0.6 °C at 85 °C for the p-poly PPF, and thus, the target frequency inaccuracy (<200 ppm) can be achieved.

F. Noise Analysis

Fig. 14(a) shows the noise sources of the proposed digital Φ-ΔΣM. It denotes the PPF's output-referred noise ($V_{n,\mathrm{PPF}}$),

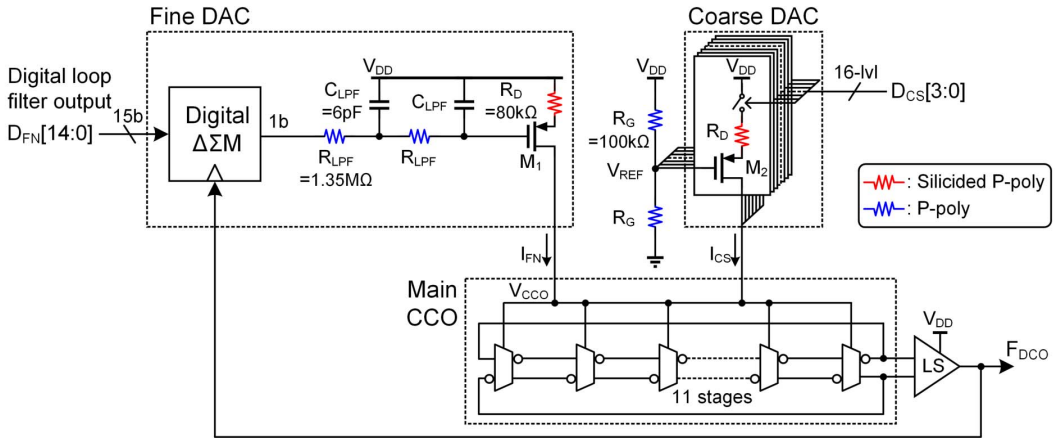

Fig. 15. Circuit implementation of the proposed DCO.

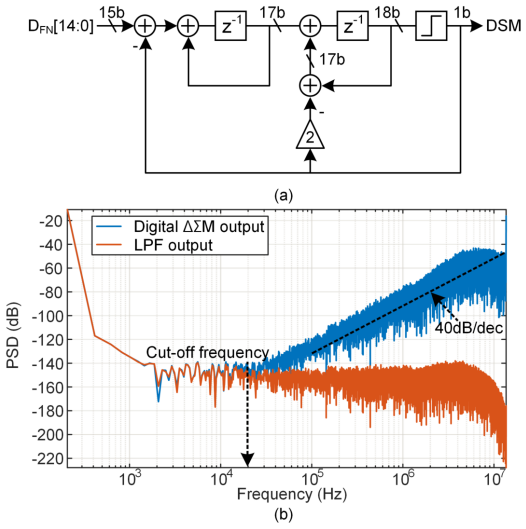

Fig. 16. (a) Block diagram of the second-order digital ΔΣM. (b) Simulated PSDs of the digital ΔΣM output and the LPF output.

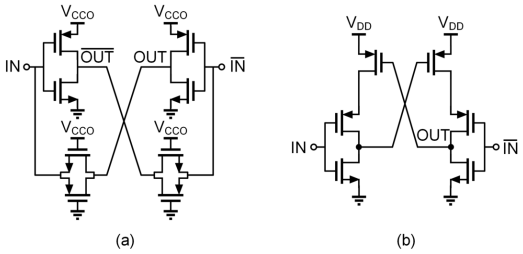

Fig. 17. Schematic of (a) CCO delay cell and (b) level shifter.

the ZC detector's input-referred noise ($V_{n,\mathrm{ZC}}$), the time-counting oscillator's noise referred to the XOR input ($\Phi_{n,\mathrm{TCO}}$), and the time-quantization noise referred to the XOR input ($\Phi_{n,TQ}$). Since the output voltage of the ZC detector (F_{ZCD}) is demodulated by the XOR gate via the phase DAC output (F_{DAC}), its $1/f$ noise is up-modulated to F_{DRV} and then low-pass filtered through Φ-ΔΣM and the decimation filter, while the PPF's phase shift (Φ_{PPF}) is down-converted to DC. Therefore, the low-frequency noise and the offset of the ZC detector can be suppressed. The output phase noise from F_{CNT} results in fractional counts of the up/down counter, which can be referred to the XOR input [19]. The noise is up-modulated to $2F_{\mathrm{DRV}}$ by the up/down counter's modulation and filtered out by the decimation filter like $V_{n,\mathrm{ZC}}$, thus suppressing the low-frequency noise. Then, considering (7) in the Appendix, the power of the input-referred noise from F_{CNT} is expressed as

$$\Phi^2_{n,\mathrm{TCO}} = \frac{8}{F^2_{\mathrm{CNT}}} L_\Phi(f + 2F_{\mathrm{DRV}})(f + 2F_{\mathrm{DRV}})^2 \qquad (4)$$

where $L_\Phi(f)$ is the phase noise of F_{CNT} [19]. It should be noted that $\Phi_{n,\mathrm{TCO}}$ is the equivalent noise on the input phase signal and different from $L_\Phi(f)$. Only the phase noise at an offset $2F_{\mathrm{DRV}}$ from the carrier affects the output. If $L_\Phi(f)$ is below -67 dBc/Hz for offset frequencies above $2F_{\mathrm{DRV}} = 437.5$ kHz, $\Phi_{n,\mathrm{TCO}}$ will be below $\Phi_{n,\mathrm{TQ}}$. From simulations, since $L_\Phi(f)$ at 437.5-kHz frequency offset is -86 dBc/Hz, the phase-noise induced noise is negligible. On the other hand, since the DCO output F_{DCO} is commonly used to generate both F_{DRV} and F_{DAC}, their phase noises are fully correlated. As a result, to first order, this noise will not appear at the output of the XOR gate. The noise from the phase reference generator is unavoidable, but it turns out that this is negligible. Fig. 14(b) shows the simulated output PSDs of the digital Φ-ΔΣM with and without the circuit noise. It confirms that the total output noise is mainly limited by the time-quantization noise.

V. Digitally Controlled Oscillator

In a digital FLL, the DCO should have sufficient tuning range to accommodate PVT variations and high resolution to facilitate the target inaccuracy. Fig. 15 shows the circuit diagram of the DCO, which consists of an 11-stage CCO, which is controlled by a 4-bit coarse current-steering DAC and a 15-bit fine ΔΣ DAC. The coarse DAC covers a frequency shift of ±50% in the 28-MHz nominal frequency over process corners, while the fine ΔΣ DAC covers ±12% over voltage and temperature variation with a resolution of 360 Hz.

Compared to area- and power-hungry Nyquist DACs in [5], [6], [14], a ΔΣ DAC can be implemented in a compact area and provide high-resolution outputs. As shown in Fig. 16(a), it is driven by a digital ΔΣM, which is implemented using a second-order error-feedback structure [22]. To effectively

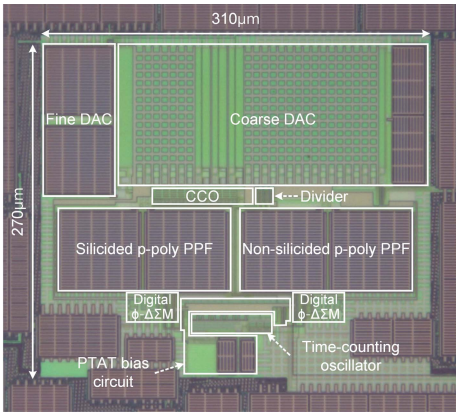

Fig. 18. Chip microphotograph.

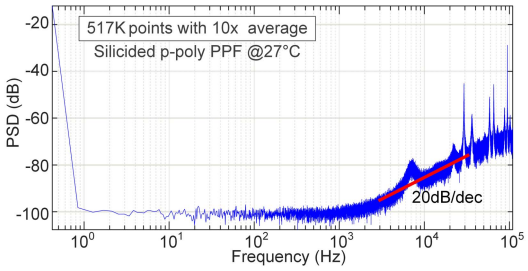

Fig. 19. Measured PSD of the digital Φ-ΔΣM's BS with 517k samples and averaged over ten FFTs in a silicided p-poly PPF at room temperature.

remove the shaped quantization noise from the modulator, a passive second-order low-pass filter (LPF) ($R_{\rm LPF} = 1.35$ MΩ and $C_{\rm LPF} = 6$ pF) is used, which achieves the cutoff frequency of 20 kHz. Fig. 16(b) shows the simulated PSD of the modulator output to a −6-dB full-scale (FS) DC input at a sampling rate of 28 MHz. The LPF properly reduces total out-of-band noise by ∼91 dB.

After the LPF, a source-degenerated g_m generates the driving current of the CCO. To suppress the current-to-frequency noise at the CCO output, it is combined with a degeneration resistor ($R_D = 80$ kΩ), thus achieving a target g_m of ∼9 μS. A silicided p-poly resistor is used since its TC well compensates for the TC of the PMOS transistor. As a result, compared to using a p-poly resistor, the temperature drift of the output current can be reduced from 44.5% to 16.4%.

Similar to the fine DAC, the g_m circuit biased with the same voltage $V_{\rm REF}$ is applied to the coarse DAC, and its output current is controlled by a 15-bit unary DAC from 4-bit binary code ($D_{\rm CS}$) via a binary-to-thermometer decoder. Each branch provides 3 μA, and the CCO's input current at room temperature is set to 24 μA. The CCO is designed as an 11-stage current-starved ring oscillator, whose tuning gain $K_{\rm CCO}$ is 1.17 MHz/μA. As shown in Fig. 17, its delay cell consists of two inverters cross-coupled to each other in a feed-forward manner using transmission gates, which reduces the common-mode errors by ensuring pseudo-differential operation [23]. The level shifter is implemented as a push–pull structure and realizes a 50% duty cycle of the output frequency. The period jitter of the free-running CCO can be estimated from the phase noise of the oscillator [24]. The simulated phase noise at 1-MHz offset is ∼−119 dBc/Hz,

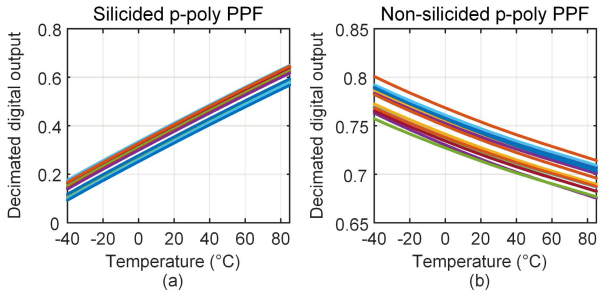

Fig. 20. Measured decimated digital output versus temperature: (a) Silicided p-poly PPFs. (b) p-poly PPFs.

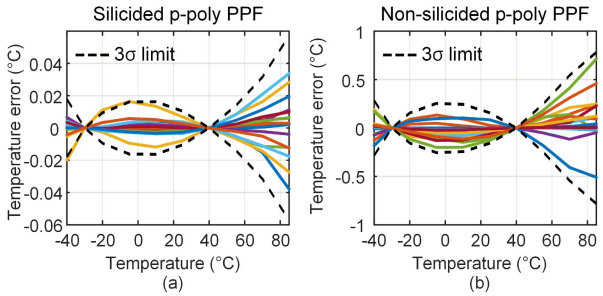

Fig. 21. Measured temperature error: (a) Silicided p-poly PPFs. (b) p-poly PPFs.

which can be translated into the period jitter as

$$\sigma^2_{\rm period,rms} = \frac{2T^2_{\rm DCO}}{\pi^2}\int_0^{F_{\rm DCO}/2} L(f)\sin^2(\pi f T_{\rm DCO})df \qquad (5)$$

where $L(f)$ is the phase noise at frequency offset f. The resulting period jitter was designed to be ∼6.3 ps below the target period jitter of 7 ps corresponding to ∼200 ppm frequency error of the output period.

VI. Measurement Results

The prototype frequency reference is fabricated in a 65-nm CMOS technology, and the chip microphotograph is shown in Fig. 18. It occupies an area of 0.06 mm^2 and consumes 142 μW from a 0.9-V supply (∼26% is consumed by each digital Φ-ΔΣM and ∼16% by the DCO). 16 samples in ceramic dual-in-line (DIL) packages were characterized from −40 °C to 85 °C in a temperature-controlled oven. To minimize the effects of oven temperature drift, they were placed in good thermal contact with an aluminum metal block. The actual temperature of the DIL packages was established by a platinum Pt-100 resistor sensor. For flexibility, the decimation filter, the digital polynomial engines, and the digital loop filter were implemented in an external field programmable gate array (FPGA).

A. Frequency Stability

To characterize the phase shift of the PPFs over temperature, an external reference frequency of 28 MHz is used instead of the DCO output. Fig. 19 shows the measured output spectrum of Φ-ΔΣM with a PPF (silicided p-poly) driven at the 218.75-kHz frequency. It is quite flat, confirming that the noise floor is dominated by the time-quantization noise

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER STATE-OF-THE-ART WORKS

	This work	JSSC18 [14]	ISSCC20 [12]	ISSCC21 [13]	VLSI20 [10]	CICC21 [9]	ISSCC20 [7]	VLSI20 [8]
Technology	**65nm**	180nm	180nm	180nm	180nm	65nm	65nm	40nm
Frequency	**28MHz**	7MHz	16MHz	16MHz	116kHz	100MHz	32MHz	428kHz
Supply voltage [V]	**0.85-1.05**	1.7-2.0	1.6-2.0	1.6-2.0	1.8-2.0	1.1-2.5	1.1-2.3	1-1.4
Area [mm^2]	**0.06**	1.65	0.3	0.14	1.2	0.19	0.18	0.07
Power [μW]	**142**	750	400	158.4	0.694	101	34	0.38
Energy [pJ/cycle]	**5**	107	25	9.9	5.98	1.01	1.06	0.9
TC compensation	High-order compensation						1st-order compensation	
Polynomial order	**5**	4	1 / 6[a]	4[b] / 5	-[c]	2[d]	1	
Temperature range [°C]	**-40 to 85**	-45 to 85	-45 to 85	-45 to 85	-15 to 85	-40 to 95	-40 to 85	-40 to 80
TC [ppm/°C]	**2.56**	2.5	6.15 / 1.54[a]	5.2[b] / 3.07	8.7	2.1[d]	8.4	8
Line sensitivity [%/V]	**0.29**	0.18	0.12	0.2	0.38	0.008[e]	0.008[e]	0.27
# of samples	**16**	8	20	18	10	20	6	1
Period jitter (1σ)	**7ps (196ppm)**	23.8ps (166ppm)	39ps (624ppm)	10.2ps (163ppm)	-	13.3ps (1330ppm)	24ps (768ppm)	-
Allan deviation [ppm]	**2**	0.33	0.32	0.35	4	1.6	2.5	10

[a]Applying 6th-order polynomial function, [b]With 1-point calibration, [c]Piece-wise linear approximation, [d]With 3-point calibration, [e]Using LDO

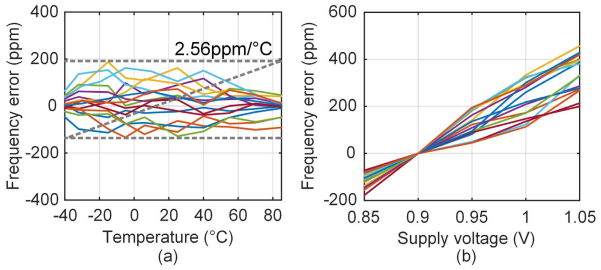

Fig. 22. Measured frequency error versus (a) temperature and (b) supply voltage.

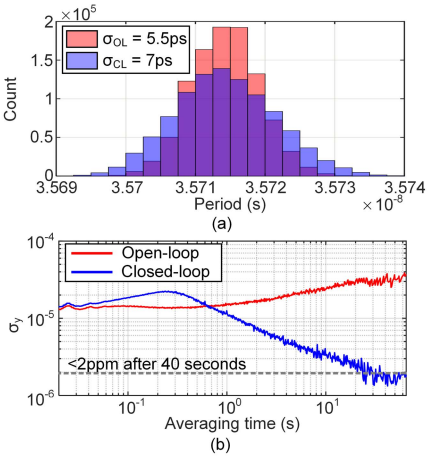

Fig. 23. Measured (a) period jitter and (b) Allan deviation for open- and closed-loop configurations.

of the counter. By decimating 2^{16} output bits, a temperature resolution of <10 mK was achieved for both PPFs. Fig. 20 shows the decimated digital outputs of the silicided p-poly and p-poly PPFs from −40 °C to 85 °C for 16 samples. The decimated digital output of silicided p-poly and p-poly PPFs varies from 0.15 to 0.6 and from 0.75 to 0.7 over temperature, which translates into phase shifts of ∼21.4° and ∼2.4°. After a two-point trim (−30 °C and 40 °C), the decimated digital output of each sample is mapped into the temperature via its individual linear function ($p_{1,i}$ in Fig. 6). Next, the remaining systematic non-linearity is corrected with fixed fifth-order polynomials (p_5 in Fig. 6), whose coefficients were determined from 16 chips in the same batch. Although the systematic nonlinearity may vary from different batches, a nonlinearity variation is negligible due to its systematic nature [25]. Therefore, a wafer-level calibration can be applied. As shown in Fig. 21, the resulting 3σ temperature errors for silicided p-poly and p-poly PPFs are measured to be 0.06 °C and 0.76 °C, respectively.

After the coefficients of the first- and fifth-order polynomials [$p_1(\cdot)$ and $p_5(\cdot)$] are loaded into the FPGA, the closed-loop output frequency of the FLL is measured. Fig. 22 shows the resulting output frequency errors of 16 samples over temperature and supply voltage. This is less than ±200 ppm (+190/−130 ppm) from −40 °C to 85 °C, which corresponds to a TC of 2.56 ppm/°C (box method). The resulting inaccuracy is unexpectedly non-zero at two trim points (−30 °C and 40 °C). It could be limited by open-loop calibration, which means that the digital offset and gain error of the first-order coefficients are not allowed to make zero frequency error at two points. As in [14], however, this calibration error could be eliminated if we obtain the digital polynomial coefficients from the closed-loop configuration. The measured worst case line sensitivity is 580 ppm from 0.85- to 1.05-V supply voltage, corresponding to a supply sensitivity of 0.29%/V. It is mainly determined by the supply-dependent phase delay of the ZC detector.

As shown in Fig. 23, the closed-loop period jitter is also measured, and it achieves 7 ps or 196 ppm of the period, which is almost the same as the open-loop jitter of 5.5 ps. It can be seen that the short-term period jitter is dominated by the DCO. There is a discrepancy of about 15% between the measured and the estimated open-loop jitter, and it is expected that it resulted from process variations. Even so, the target period jitter of 7 ps is achieved from the measured closed-loop jitter. Due to the 3-Hz loop sample rate of the frequency reference, this frequency reference may not track a fast thermal transient (>3 Hz), and the measured Allan deviation is increased to ∼20 ppm with an averaging time of 0.2 s. However, the measured Allan deviation floor is effectively improved by the closed-loop operation and reaches a floor of <2 ppm over 40 s averaging time, which is limited by low-frequency $1/f$ noise of the FLL and dominated by the digital Φ-$\Delta\Sigma$M.

B. Comparison to Previous Works

Table I shows the performance summary of the proposed dual-*RC* frequency reference and comparison with previous state-of-the-art *RC* frequency references. Thanks to its highly digital architecture and low-voltage operation, this work is 27× smaller (0.06 mm^2) and consumes 20× less energy (5 pJ/cycle) than a previous dual-*RC* reference [14]. Compared to a recent work [13], this work consumes 2× less energy and 2× smaller area. Compared to [7] and [8], this work shows more than 3× improvements in TC (2.56 ppm/°C). Finally, this work consumes 5× less energy than the most accurate reference [12] while achieving a comparable inaccuracy.

C. Digital Design Complexity

Like other recent digitally assisted frequency references [8], [10], [12]–[15], the digital blocks for the temperature compensation scheme of this work were implemented off-chip. When synthesized with standard cells and laid out by a standard place and route tool, their power and area are estimated to be 34 μW and 0.07 mm^2, respectively. Even when this is considered, this work still achieves the competitive energy efficiency and the smallest area.

VII. Conclusion

An energy-efficient dual-*RC* frequency reference is implemented in a standard 65-nm CMOS technology for wireless sensor nodes. The frequency reference uses digital Φ-$\Delta\Sigma$Ms that digitize the phase shifts of two *RC* PPFs, which are combined in the digital domain to achieve a temperature-independent output frequency. Thanks to this highly digital architecture, the frequency reference operates in a 0.9-V supply and achieves a low energy consumption of 5 pJ/cycle while occupying only 0.06 mm^2. Furthermore, it achieves ±200 ppm inaccuracy from −40 °C to 85 °C after a two-point trim. These features make the proposed frequency reference suitable for practical use in the IoT applications.

Appendix

In this appendix, the time-quantization noise for the proposed digital Φ-$\Delta\Sigma$M is derived. Although it is very similar to the quantization noise introduced by the quantizer of a $\Delta\Sigma$M, a factor of 2 should be considered in the time-quantization noise due to the addition at both the start and ends of the up/down counting state. Denoting that the time-quantization noise is sampled at every half cycle of the input signal of the integrator, whose period is $1/2F_{\mathrm{XOR}}$ $(=1/4F_{\mathrm{DRV}})$ and its bandwidth is $2F_{\mathrm{DRV}}$, the noise power $(\sigma^2{}_Q)$ for a bandwidth F_{BW} at the integrator input can be calculated as

$$\sigma_Q^2 = \frac{2}{12}\cdot\frac{F_{\mathrm{BW}}}{2F_{\mathrm{DRV}}} = \frac{1}{12}\cdot\frac{F_{\mathrm{BW}}}{F_{\mathrm{DRV}}} = \frac{1}{24\cdot\mathrm{OSR}}. \tag{6}$$

As in [19], to check the impact on the input phase noise, the phase-to-count gain (K) of the counter is defined as the ratio of half the period of the F_{XOR} and the period of the F_{CNT}

$$K = \frac{1/4F_{\mathrm{DRV}}}{1/F_{\mathrm{CNT}}} = \frac{F_{\mathrm{CNT}}}{4F_{\mathrm{DRV}}}. \tag{7}$$

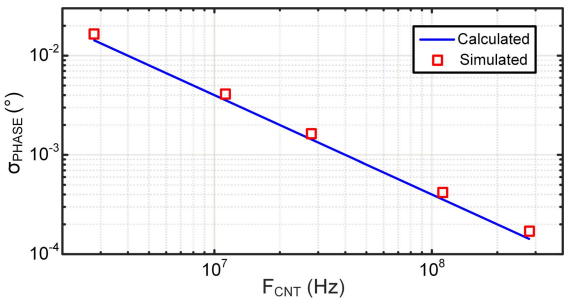

Fig. 24. Calculated input-referred phase noise and simulated phase noise of the digital Φ-$\Delta\Sigma$M according to the F_{CNT}.

By converting the time-quantization noise into the phase noise, it can be seen at the input of the XOR gate, resulting in the input-referred phase noise with an in-band power of $\sigma^2{}_{n,\mathrm{TQ}}$, where

$$\sigma_{n,\mathrm{TQ}}^2 = \frac{\sigma_Q^2}{K^2}. \tag{8}$$

Combining (7) and (8), the rms in-band phase noise $(\sigma_{\mathrm{PHASE}})$ can be finally derived as

$$\sigma_{\mathrm{PHASE}} = \sqrt{\frac{1}{24\cdot\mathrm{OSR}}}\cdot\frac{4F_{\mathrm{DRV}}}{F_{\mathrm{CNT}}} = \sqrt{\frac{2}{3\cdot\mathrm{OSR}}}\cdot\frac{F_{\mathrm{DRV}}}{F_{\mathrm{CNT}}}. \tag{9}$$

This is confirmed by system-level simulations, as shown in Fig. 24. The simulated and calculated results are well matched.

Acknowledgment

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