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A capacitance spectroscopy-based platform for realizing gate-defined electronic lattices

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Electrostatic confinement in semiconductors provides a flexible platform for the emulation of interacting electrons in a two-dimensional lattice, including in the presence of gauge fields. This combination offers the potential to realize a wide host of quantum phases. Capacitance spectroscopy provides a technique that allows one to directly probe the density of states of such two-dimensional electron systems. Here, we present a measurement and fabrication scheme that builds on capacitance spectroscopy and allows for the independent control of density and periodic potential strength imposed on a two-dimensional electron gas. We characterize disorder levels and (in)homogeneity and develop and optimize different gating strategies at length scales where interactions are expected to be strong. A continuation of these ideas might see to fruition the emulation of interaction-driven Mott transitions or Hofstadter butterfly physics. https://doi.org/10.1063/1.5046796

I. INTRODUCTION

Artificial lattice structures have the potential for realizing a host of distinct quantum phases.[1] Of these, the inherent length scale of optical platforms allows for a clean emulation of quantum mechanical band physics, but also means interactions are weak and going beyond a single-particle picture is difficult.[2,3] For electronic implementations in solid-state, interactions can be made non-perturbatively strong, potentially leading to a host of emergent phenomena. An example is shown in graphene superlattices, where not only Hofstadter's butterfly physics[4–7] but also interaction-driven and emergent fractional quantum Hall states in the butterfly appear.[8] The ideal platform would host a designer lattice with tunable electron density and lattice strength, allowing to emulate band physics for a wide variety of lattice types and giving access to the strong-interaction limit of correlated Mott phases.[9–13] Semiconductor heterostructures with nanofabricated gate structures provide this flexibility in lattice design and operation, yet inherent disorder in the host materials as well as the short length scales required make the realization of clean lattices difficult.[14–16]

In this letter, we introduce a novel experimental platform for realizing artificial gate-induced lattices in semiconductors based on a capacitance spectroscopy technique,[17–19] with the potential to observe both single-particle band structure physics such as Hofstadter's butterfly and many-body physics such as the interaction driven Mott insulator transition. We discuss different gating strategies for imprinting a two-dimensional periodic potential at length scales, where interactions are expected to be strong, characterize intrinsic disorder levels, and show first measurements of double gate devices.

II. HETEROSTRUCTURE AND CAPACITANCE SPECTROSCOPY

To host the 2D electron gas (2DEG), we use a GaAs quantum well with AlGaAs barriers, grown by molecular beam epitaxy. The substrate contains a highly Si-doped GaAs layer that acts as a back gate. It is tunnel coupled to the 2DEG through a $Al_xGa_{1-x}As$ tunnel barrier [see Fig. 1(a) and Table I]. There is no doping layer above the quantum well in order to avoid an important source of disorder. A metallic top gate is fabricated on the surface. A variable capacitor forms between the back and top gates: when an alternating potential difference is applied between them, electrons tunnel back and forth between the back gate and the 2DEG, modifying the capacitance by an amount proportional to the density of states (DOS) of the 2DEG. The tunnel frequency depends mainly on the thickness and the Al content (x) of the tunnel barrier. At the limits of zero or infinite DOS, the system behaves like a simple parallel plate capacitor, described by the distance between top gate and back gate or top gate and 2DEG, respectively. The capacitance is read out using a bridge design with a reference capacitor,[20] where the voltage at the bridge point is kept constant [Fig. 1(b)] by changing the amplitude ratio and phase difference of AC signals applied to each capacitor (see Sec. A in the supplementary material for experimental details).

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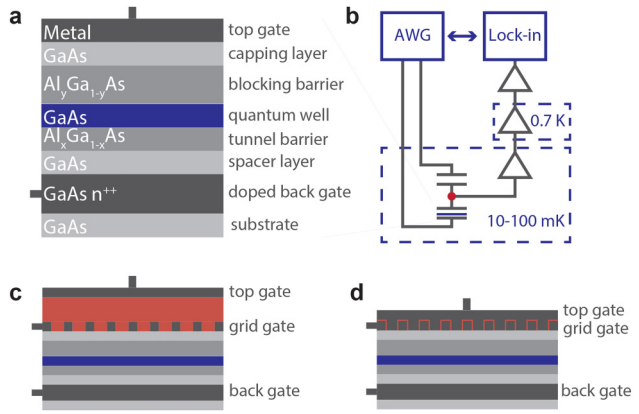

FIG. 1. (a) Schematic diagram showing the various layers of the samples with a single global gate. (b) Bridge set-up for equilibrium capacitance measurements, where sinusoidal signals are applied by a waveform generator (WG) on both the sample back gate and on a reference capacitor of 45 pF. The relative amplitude and phase difference between these two signals are adjusted to maintain a constant zero voltage at the bridge point (red dot), which is amplified in different stages and read out using a lock-in amplifier. The bridge point is connected to the grid gate when there is a grid gate present, and to the top gate otherwise. [(c) and (d)] Schematic diagrams of two different two-layer gate geometries, designed to impose a periodic potential on the 2DEG, comprising either of a deposited dielectric (c) or a dielectric obtained by oxidation of the first metallic layer (d). Dielectric spacer is depicted in red. The other colors are as in panel (a).

To impose a periodic potential in the 2DEG, we pattern a metallic gate into a grid shape before making the top gate. From a capacitance spectroscopy perspective, this double-gate structure can be made with two different designs. In the first design, the top gate is separated from the grid gate by a thick dielectric layer, rendering its capacitance to the grid gate negligible (a few pF compared to tens of pF). In that case, we can ignore the grid gate from an AC perspective altogether [Fig. 1(c)]. Alternatively, we can minimize the separation between the two gate layers, such that the capacitance between the two top gates (100s of pF) exceeds the sample capacitance. Here, the two gates effectively form a single gate [Fig. 1(d)], as seen in AC. We investigate both designs below, starting with describing the fabrication (limits) and following with measurements of disorder levels and imposed potentials.

TABLE I. Heterostructure details.

	W1	W2	M1	W3	M2
Capping layer	GaAs	GaAs	GaAs	GaAs	GaAs
	10 nm	10 nm	5 nm	10 nm	5 nm
Blocking barrier (Al content)	0.316	0.316	0.316	0.315	0.360
	60 nm	60 nm	40 nm	60 nm	60 nm
Quantum well	GaAs	GaAs	GaAs	GaAs	GaAs
	23 nm	23 nm	23 nm	23 nm	23 nm
Tunnel barrier (Al content)	0.316	0.316	0.316	0.315	0.199
	13 nm	13 nm	14 nm	14 nm	16 nm
Spacer layer	GaAs	GaAs	GaAs	GaAs	GaAs
	25 nm	15 nm	15 nm	15 nm	15 nm
Back gate	GaAs n^{++}	GaAs n^{++}	GaAs n^{++}	GaAs n^{++}	GaAs n^{++}
	800 nm	800 nm	400 nm	400 nm	400 nm
Tunneling frequency at 0T, $n \approx 10^{11}$ cm^{-2}	1 MHz	200 kHz	2 kHz	30 kHz	100 kHz
Lowest field at which Landau levels can be distinguished	3 T (at 4 K)	0.65 T	0.50 T	0.40 T	0.25 T
Comments	n^{++} doped substrate	n^{++} doped substrate			

III. GATE DESIGN AND FABRICATION

We distinguish devices with a single global gate [Fig. 1(a)] and devices with two layers of gates: a grid gate and a uniform global gate on top [Figs. 1(c) and 1(d)]. The former will be used to characterize disorder levels in Sec. IV, whereas the latter allows for the imposition of a periodic potential. The strength of the imparted periodic potential depends on the dielectric choice [thick or thin, compare Figs. 1(c) and 1(d)], gate design, grid gate pitch, and the maximum voltages that can be applied. Grid gates are made with a pitch of 100–200 nm [Figs. 2(a) and 2(b)], which is mainly limited by the fabrication constraints. The maximum voltage is determined by the onset of leakage through the heterostructure or the accumulation of charges in the capping

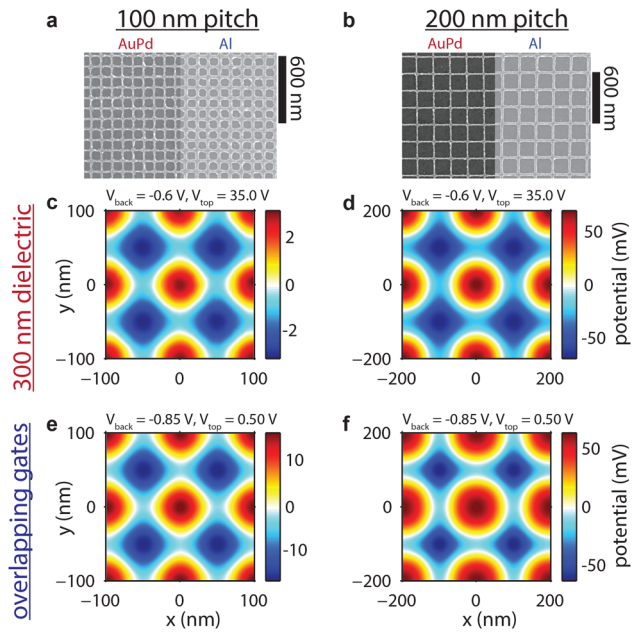

FIG. 2. (a) Electron micrograph of 100 nm periodic AuPd and Al grid gate structures for two different gate designs. (b) Similarly, for 200 nm periodic gate structures. [(c)–(f)] Electrostatic simulations of imparted potential in the 2DEG in both designs and both gate pitches (100 and 200 nm) using denoted gate voltages. For (c) and (d), we use a 350 nm SiO_2 dielectric and flat top gate. For (e) and (f), we use a 5 nm spacer dielectric (oxidized Aluminum oxide) separating the two top gates. Voltages used are roughly the empirical maximum voltage difference we can set for both designs (see Fig. 5), $V_{grid} = -0.45$ V for both. Width of the metal grids are taken as 22 nm and 25 nm for AuPd and Al grids, respectively, for reasons explained below.

layer, and thus depends on heterostructure details such as the Al concentration and layer thicknesses.

The expected imparted potentials at the 2DEG with typical maximum voltages for both designs are shown in Figs. 2(c)–2(f) (calculated using COMSOL electrostatic simulation software). In order to observe a Mott transition and the corresponding localization of electrons on individual sites, the periodic potential amplitude must exceed the local Coulomb repulsion (typically several meVs).[21] For 200 nm grids, both designs show similar maximum effective periodic potentials, and they should suffice for the formation of quantum dots. For the 100 nm grids, however, the achievable potentials exceed the charging energy only when using the overlapping gate design. For the smaller pitch grid, effective shielding of the top gate voltage by the grid gate is larger when the top gate is farther away from the heterostructure. Therefore, an overlapping gate design is required to go to sufficiently strong periodic potentials for localization at 100 nm site-to-site pitch.

Furthermore, we note that screening induced by mobile charges in the back gate region has both desired and undesirable consequences. An intended benefit is that disorder from charged impurities or defects in the heterostructure is partly screened, and the more so the closer to the back gate the impurities or defects are located.[13] However, electron-electron interactions and the gate-voltage imposed potential modulation itself are partly screened as well, and more so as the lattice dimension is reduced.

Double gate devices with either a thick [Fig. 1(c)] or a thin dielectric [Fig. 1(d)] between the two gates require different fabrication processes. Here, we discuss the fabrication of the active regions in both designs, which have a size of 200 μm by 200 μm. The detailed information for all steps in the fabrication is provided in Sec. B of the supplementary material. In both designs, the square grid metallic gates are fabricated at pitches of 100–200 nm using electron beam lithography and evaporation of metals in a standard lift-off process [Figs. 2(a) and 2(b)]. In the first design, both gates are made of Ti/Au(Pd) and separated by $>$ 200 nm layer of oxide, such as plasma-enhanced chemical vapor deposition grown SiO_x or plasma-enhanced atomic layer deposition grown AlO_x. In the second design, both gates are made of Al, and an oxygen (remote) plasma oxidation step is used after depositing the first Al layer to ensure sufficient electrical isolation between the two layers by transforming part of the Al gate to Aluminum oxide.[22] In this design, we measure resistances exceeding 1 GΩ over several volts.

Because of the fabrication process, there are limits in the periodicity and homogeneity of the grid gate layer. We typically find (1) that plaquettes of smaller size than $40\,nm \times 40\,nm$ will not lift off and that (2) the grain size of a particular metal determines the narrowest lines that can be made reliably with liftoff. For the materials used here, AuPd and Al, these effects limit the minimum lattice pitch [Fig. 3(a)]. Furthermore, we have analyzed the homogeneity of the lattices by using image processing techniques to give the statistics of the non-metal plaquette areas [Fig. 3(b)]. A more relaxed lattice constant means higher relative homogeneity but this is not necessarily helpful: it also increases the flux through a single plaquette when a perpendicular magnetic field is applied (relevant for Hofstadter butterfly physics, as will be described below) and it decreases the charging energy, relevant for Mott interaction physics.

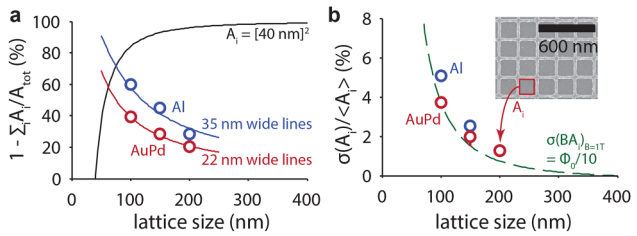

FIG. 3. (a) Fraction of surface area covered by the grid gate as function of lattice size. Black line indicates a grid with the smallest possible plaquettes allowed by the lift-off process, whereas the blue (red) line indicates the percentage of surface area covered by a grid with metallic lines of 35 nm (22 nm). (b) Variation in relative area of non-metal plaquettes in the grid gate layer (A_i, see inset) as function of lattice size, as a measure of fabrication (in)homogeneity. The green dashed line indicates variations in plaquette area that coincide with variations of a tenth of a flux quantum at 1 T (see Discussion below). Blue (red) points indicate grid gates made of Al (AuPd) for both figures.

IV. MEASUREMENTS

A. Global gates: Disorder levels

In order to assess disorder levels, we first measure the devices with a single uniform top gate. We measure the capacitance at frequencies below and above the rate at which electrons tunnel between the 2DEG and the doped back gate region as a function of bias voltage [Figs. 4(a) and 4(b)] and magnetic field. Having measured the capacitance at low and high frequencies, we calculate the equilibrium DOS. There are essentially two unknown parameters in this conversion, namely the distance from top to bottom gate and the relative location of the 2DEG itself. The former can be directly inferred from the capacitance at high frequency, the latter by using either the known effective mass or the Landau level splitting with magnetic field as benchmarks (see Sec. C in the supplementary material for details on this conversion).

As a magnetic field is turned on, we see the onset of Landau level formation. For magnetic fields above 2 T, we observe a splitting between the spin subbands of the Landau levels which increases with the applied magnetic field [Fig. 4(c)]. For a given magnetic field, the separation between the two subbands of any Landau level is significantly larger than the Zeeman energy with $g = -0.44$ for bulk electrons in GaAs.[17] This enhanced Zeeman splitting is an effect of the Coulomb repulsion between electrons in the same subband.[23]

We focus on the low-field data [Fig. 4(d)] and infer disorder levels from the density of states data [Fig. 4(e)]. Gaussian fits to the Landau levels yield typical widths ranging between 0.4 and 1 meV at densities above 10^{11} cm^{-2}, which, although hard to compare directly to the mobilities reported for transport-based wafers,[14–16] is comparable to previously reported values for similar heterostructures.[24] The Landau levels themselves [aliased at low fields in Fig. 4(d)] become visible above fields of roughly 0.25 T, corresponding to

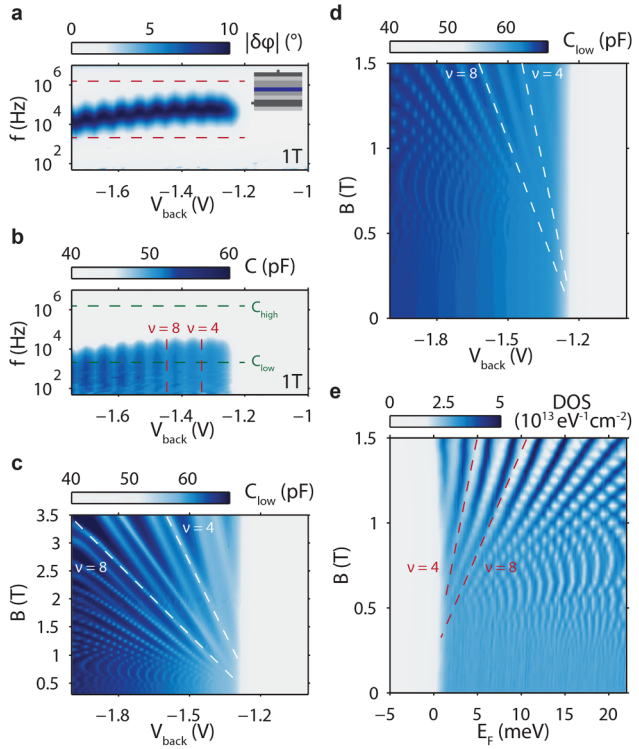

FIG. 4. (a) Bridge equilibrium phase as function of back gate bias and measurement frequency. (b) Global gate capacitance as function of back gate bias and measurement frequency. (c) Landau fan diagram: device capacitance as function of back gate bias and magnetic field, showing onset of accumulation, integer quantum Hall levels and exchange splitting. (d) Zoom in of Landau fan diagram for low field regime of (c). (e) Calculated density of states (DOS) from (d), allowing us to assess disorder from Landau level visibility. The gaps at filling factors $\nu = 4$ and $\nu = 8$ are indicated. At lower fields, the small Landau level spacing leads to aliasing in the image.

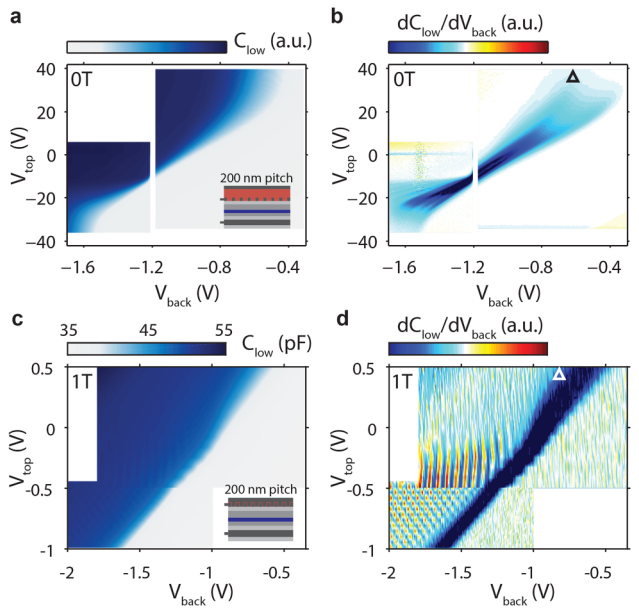

FIG. 5. (a) Capacitance as function of back gate and top gate voltages for a device with a 200 nm periodic square grid gate and a 360 nm SiO2 dielectric separating the two gate layers [see inset and Fig. 3(a)]. (b) Derivative of capacitance data. [(c) and (d)] Similar data taken for a device with aluminum overlapping gates (see inset) at 1 T. Black and white triangles in (b) and (d) indicate the gate voltages used in Figs. 2(d) and 2(f), respectively. The onset of accumulation shows broadening in (b) whereas Landau levels get blurred out with increasing top gate voltage in (d).

densities per Landau level of 1.2×10^{10} cm^{-2} and cyclotron gaps of 0.43 meV. The Landau level width did not change when we increased the mixing chamber temperature from 10 mK to 100 mK or when we varied the excitation voltage. Furthermore, the Landau level width was consistent across fabrication schemes, but did vary with the wafer used. Therefore, we consider it a heuristic metric for the achievable disorder levels on a particular wafer.

We have tried to optimize wafer design to minimize this disorder, while allowing for the imposition of a periodic potential. All in all, over 20 different GaAs/Al$_x$Ga$_{1-x}$As wafers grown by molecular beam epitaxy have been used. Growth details of the wafers can be found in Table I.

The initial wafer (W1) design was based on Dial *et al.*,[25] and was grown on a conducting substrate. This simplifies the fabrication of single-gate devices, as an unpatterned ohmic back gate contact can be directly evaporated on the back side of the wafer, while simple metallic pads fabricated on the front side can be directly bonded to and used as a top gate. A double-gate design requires dedicated bond pads, which would give a sizable contribution to the total capacitance when fabricated directly on the wafer. The device used for Figs. 5(a) and 5(b) in the main text, fabricated on one of the first rounds of wafers (W2), therefore, had bond pads on top of the thick dielectric separating the two gates. This strategy is not compatible with the second design, where there is no thick dielectric layer, and also gives a very low wire bonding yield due to poor adhesion of the dielectric layers on the GaAs surface. Furthermore, handling both sides of a substrate during fabrication risks contaminating the front surface, and is particularly suboptimal when detailed features (grid gates) are present as well. Subsequent wafers were, therefore, grown with a 400–800 nm thin degenerately Si doped back gate region that is contacted from the front side of the wafer, and is etched to form electrically isolated device and bond pad mesas.

We have further tried to optimize the wafer stacks aiming to increase the amplitude of the periodic potential at the 2DEG and to decrease disorder levels. A stronger periodic potential can be obtained by either increasing the maximum possible gate voltage, reducing the separation between the grid gate and the 2DEG or increasing the distance between the 2DEG and the back gate. The latter may also reduce disorder caused by dopant diffusion from the back gate. Increasing the quantum well thickness is also expected to reduce the effect of disorder by accommodating more of the electron wave-function away from the interfaces. Concretely, we have first varied spacer layer thickness (25 and 35 nm) and quantum well widths (15 and 30 nm). In further attempts to optimize the trade-off between the periodic potential that can be set at a fixed voltage and the maximum voltage we can apply to the gates before leakage sets in, we varied the blocking barrier thickness (40, 50, 60, and 70 nm) and fabricated devices with a thin dielectric layer (see wafers M1 and W3) added underneath the grid gate. None of these, however, managed to noticeably increase the maximum potential we could impose on the 2DEG, or to decrease disorder levels. The strongest effect on disorder was

obtained by changing the aluminum concentration in the $Al_xGa_{1-x}As$ blocking and tunnel barrier (from $x = 0.31$ everywhere to $x = 0.36$ in the blocking barrier and $x = 0.20$ in the tunnel barrier), while slightly increasing the tunnel barrier thickness in order to keep the tunnel rates roughly the same (see Table I). The measurements shown in Figs. 4, 5(c), and 5(d) are taken on this optimized wafer, called M2.

B. Grid gates: Periodic potential strength

For measurements of two-layer gate devices of both designs (Fig. 5), we keep the grid gate potential fixed, given that it serves as the gate voltage of the first transistor in the amplification chain, and map out the remaining two gate voltages over as large a range as possible. Initial devices of both designs indeed show accumulation as a function of the two gate voltages [transition from light gray to blue in Figs. 5(a) and 5(c)]. At voltages where we expect a flat periodic potential (close to the center of each panel in Fig. 5), and for our final set of devices, we can still distinguish well-defined Landau levels, indicating that the added fabrication steps themselves do not severely increase the disorder levels (data not shown). This disorder in the potential landscape also leads to a broadening of the onset of accumulation, seen in the center of Figs. 5(a) and 5(c).

For devices of the first design, this broadening increases as we move away from the center, along the gray-blue boundary [Fig. 5(a)]. This suggests that we see a gate-voltage induced spatial variation in the 2DEG potential that exceeds disorder levels (0.4–1 meV) at low densities. Based on electrostatic simulations of the strength of the imposed potential, the gate-voltage induced variation is indeed expected to exceed the disorder levels (Fig. 2). The asymmetry between positive and negative top gate values seen in the data could possibly be explained by effective disorder levels being smaller when charges accumulate mainly underneath the grid gate, as compared to when charges accumulate mainly underneath the dielectric. Finally, in Fig. 5(b) we resolve separate lines at the onset of accumulation for negative top gate voltages. Even though we expect to see evidence of miniband formation, we do not attribute these splittings to miniband formation, as they show a much larger periodicity in back gate voltage than the 6 mV expected from the density of states calculation (see below).

For devices of the second design, the widening of the onset of accumulation is less pronounced , but the effect of gating is seen at finite magnetic fields, where a voltage difference between the grid and top gate effectively blurs out the gaps between Landau levels [Figs. 5(c) and 5(d)]. This indicates that the imposed local potential variation must be comparable to or stronger than the Landau level spacing at 1 T (1.7 meV). We conclude that also for the second design, the 200 nm periodic potential exceeds disorder levels.

Increasing further the amplitude of the potential variation induced by the gates was limited by saturation of the gating effect. For the first gate design, we find a saturation to the effect of the top gate in gating the 2DEG at gate voltages exceeding 35 V in absolute value. This could be a sign of charges building up at interface of the capping layer and the dielectric, or in the dielectric itself, which screen the effect of the top gate. This saturation limits the potential we can impose on the 2DEG. For the second gate design, a maximum voltage difference of roughly 2 V can be set between the back gate and the surface gates before leakage starts to occur. As an attempt to allow for larger gate voltages before leakage through the heterostructure occurs, we have tried the same fabrication but with an additional 5 nm ALD-grown AlO_x dielectric placed underneath the grid gate. This indeed prevents leakage but the gating effect saturated at the same voltages where leakage occurred for devices without this additional dielectric. Therefore, 2 V was still the maximum voltage we could apply between the back and surface gates in the second design.

V. DISCUSSION: WHAT TO SEARCH FOR IN FUTURE DATA

As we have just seen, (i) the periodic potential exceeds disorder levels. In order to see Hofstadter's butterfly and Mott physics, however, we also need to (ii) be able to resolve the induced density of states modulations and (iii) the lattice potential from the grid itself should be sufficiently homogeneous. The latter two considerations will be discussed below, based on the data presented.

Using either gate design, we find both gates to influence the accumulation of charges in the quantum well as expected, but neither shows clear evidence of a lattice potential imposed on the 2DEG (Fig. 5). At zero magnetic field, a lattice potential would lead to minibands that manifest as periodic modulations in the density of states (and capacitance) with a period corresponding to two electrons per lattice site, or $5\times10^9\,\mathrm{cm}^{-2}$ for a 200 nm square grid. Expressed in mV on the back gate, this corresponds to a period of 6 mV. Furthermore, at finite magnetic field, Landau levels are expected to show structure due to Hofstadter butterfly physics,[15,26] with the largest gaps expected around $k \pm 1/4$ of a flux quantum Φ_0 threading each lattice plaquette (with k an integer; Φ_0 corresponds to 104 mT for a 200 nm grid). Finally, a strong enough periodic potential would allow interaction effects to dominate. Miniband gaps are expected to split as filling starts to occur with a period of one electron per lattice site, akin to the interaction-driven Mott transition.[11] None of these effects are visible in Fig. 5 nor in many detailed targeted scans of magnetic field and gate voltages on devices with 200 and 100 nm grid gate periodicity.

If we compare the $5\times10^9\,\mathrm{cm}^{-2}$ density modulations expected from miniband formation with the $1.2\times10^{10}\,\mathrm{cm}^{-2}$ broadening of low-field Landau levels (global gate devices at high densities, i.e., we do not have evidence that we can resolve density variations below $1.2\times10^{10}\,\mathrm{cm}^{-2}$), it is reasonable that gaps are not yet seen opening up at densities corresponding to the filling of (pairs of) electrons on each lattice site. This suggests that either lattice size or wafer disorder has to be further reduced. As it proves hard to lift off plaquettes of metal that are smaller than roughly 40 nm by 40 nm, there is not much room to reduce lattice dimension further in this particular fabrication scheme [Fig. 3(a)]. For 100 nm pitch grids, the period of the density modulations is expected to be

four times larger, but is still comparable to current best-case scenario Landau level broadening. As such, reducing intrinsic disorder seems necessary. An appropriate goal would be to make double layer gate devices with Landau levels that are distinguishable at fields below 100 mT.

The visibility of Hofstadter butterfly gaps depends not only on the intrinsic disorder in the device but also on the inhomogeneity in the plaquette sizes, as this would entail a different number of flux quanta threading through different plaquettes. If the size variations from electron micrographs of our devices translated to identical size variations in the periodic potential [Fig. 3(b)], we should just be able to distinguish the largest gaps.[15] It is hard to assess, however, whether this indicator from the electron micrographs directly correlates to the relevant physics in the 2DEG.

VI. OUTLOOK

There is room for further optimization of these devices. On the heterostructure side, the distance between the back gate and the 2DEG can be further increased, compensating with a decreased Al content in the tunnel barrier to keep the tunnel rate fixed. Furthermore, part of the spacer layer can be grown at reduced temperatures, which has been shown to strongly reduce disorder by limiting the diffusing of Si dopants from the back gate region.[24] On the fabrication side, there is still room left for a modest reduction of the lattice periodicity with the current lift-off process. Even smaller length scales can be obtained by switching to dry etching of the grid pattern, albeit at an unknown impact to wafer disorder levels.

In summary, we have demonstrated a novel platform intended for the realization of artificial lattices of interacting particles. Although fine tuning the design to the point where a sufficiently homogeneous and strong periodic potential can be applied remains to be done, the quantum Hall data already show how the strong-interaction, low-temperature limit can be reached. Such a platform has potential for studying the interaction-driven Mott insulator transition[11,27] and Hofstadter butterfly physics[4] with finite interactions, and can be extended from the steady-state measurements presented here to include time-domain measurements of excited states.[25]

SUPPLEMENTARY MATERIAL

See supplementary material for details on the capacitance bridge technique, device design, fabrication, and the conversion from capacitance data to density of states.

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[1]J. I. Cirac and P. Zoller, Nat. Phys. **8**, 264 (2012).
[2]M. C. Rechtsman, J. M. Zeuner, Y. Plotnik, Y. Lumer, D. Podolsky, F. Dreisow, S. Nolte, M. Segev, and A. Szameit, Nature **496**, 196 (2013).
[3]D. Tanese, E. Gurevich, F. Baboux, T. Jacqmin, A. Lemaître, E. Galopin, I. Sagnes, A. Amo, J. Bloch, and E. Akkermans, Phys. Rev. Lett. **112**, 146404 (2014).
[4]D. Hofstadter, Phys. Rev. B **14**, 2239 (1976).
[5]C. R. Dean, L. Wang, P. Maher, C. Forsythe, F. Ghahari, Y. Gao, J. Katoch, M. Ishigami, P. Moon, M. Koshino, T. Taniguchi, K. Watanabe, K. L. Shepard, J. Hone, and P. Kim, Nature **497**, 598 (2013).
[6]L. A. Ponomarenko, R. V. Gorbachev, G. L. Yu, D. C. Elias, R. Jalil, A. A. Patel, A. Mishchenko, A. S. Mayorov, C. R. Woods, J. R. Wallbank, M. Mucha-Kruczynski, B. A. Piot, M. Potemski, I. V. Grigorieva, K. S. Novoselov, F. Guinea, V. I. Fal'ko, and A. K. Geim, Nature **497**, 594 (2013).
[7]B. Hunt, J. D. Sanchez-Yamagishi, A. F. Young, M. Yankowitz, B. J. LeRoy, K. Watanabe, T. Taniguchi, P. Moon, M. Koshino, P. Jarillo-Herrero, and R. C. Ashoori, Science **340**, 1427 (2013).
[8]G. L. Yu, R. V. Gorbachev, J. S. Tu, A. V. Kretinin, Y. Cao, R. Jalil, F. Withers, L. A. Ponomarenko, B. A. Piot, M. Potemski, D. C. Elias, X. Chen, K. Watanabe, T. Taniguchi, I. V. Grigorieva, K. S. Novoselov, V. I. Fal'ko, A. K. Geim, and A. Mishchenko, Nat. Phys. **10**, 525 (2014).
[9]C. A. Stafford and S. Das Sarma, Phys. Rev. Lett. **72**, 3590 (1994).
[10]E. Manousakis, J. Low Temp. Phys. **126**, 1501 (2002).
[11]T. Byrnes, N. Kim, K. Kusudo, and Y. Yamamoto, Phys. Rev. B **78**, 075320 (2008).
[12]A. Singha, M. Gibertini, B. Karmakar, S. Yuan, M. Polini, G. Vignale, M. I. Katsnelson, A. Pinczuk, L. N. Pfeiffer, K. W. West, and V. Pellegrini, Science **332**, 1176 (2011).
[13]P. Barthelemy and L. M. K. Vandersypen, Ann. Phys. **525**, 808 (2013).
[14]K. Ensslin and P. Petroff, Phys. Rev. B **41**, 12307 (1990).
[15]M. Geisler, J. Smet, V. Umansky, K. von Klitzing, B. Naundorf, R. Ketzmerick, and H. Schweizer, Phys. Rev. Lett. **92**, 256801 (2004).
[16]C. Albrecht, J. Smet, K. von Klitzing, D. Weiss, V. Umansky, and H. Schweizer, Phys. Rev. Lett. **86**, 147 (2001).
[17]R. C. Ashoori, Ph.D. thesis, Cornell University, 1991; available at https://arxiv.org/abs/cond-mat/0607739
[18]R. Ashoori, H. Stormer, J. Weiner, L. Pfeiffer, S. Pearton, K. Baldwin, and K. West, Phys. Rev. Lett. **68**, 3088 (1992).
[19]R. Ashoori, J. Lebens, N. Bigelow, and R. Silsbee, Phys. Rev. B **48**, 4616 (1993).
[20]R. E. Cavicchi and R. H. Silsbee, Rev. Sci. Instrum. **59**, 176 (1988).
[21]L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, "Electron transport in quantum dots," in *Mesoscopic Electron Transport*, edited by L. L. Sohn, L. P. Kouwenhoven, and G. Schön (Springer Netherlands, Dordrecht, 1997), pp. 105–214; available at https://link.springer.com/chapter/10.1007%2F978-94-015-8839-3_4
[22]S. J. Angus, A. J. Ferguson, A. S. Dzurak, and R. G. Clark, Nano Lett. **7**, 2051 (2007). pMID: 17567176.
[23]T. Ando and Y. Uemura, J. Phys. Soc. Jap. **37**, 1044 (1974).
[24]J. Jang, B. M. Hunt, L. N. Pfeiffer, K. W. West, and R. C. Ashoori, Nat. Phys. **1**, 1 (2016).
[25]O. E. Dial, R. C. Ashoori, L. N. Pfeiffer, and K. W. West, Nature **448**, 176 (2007).
[26]D. Pfannkuche and R. Gerhardts, Phys. Rev. B **46**, 12606 (1992).
[27]M. Imada, A. Fujimori, and Y. Tokura, Rev. Mod. Phys. **70**, 1039 (1998).