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Multi-functional LED Module Integration and Miniaturization for Solid State Lighting Applications

Proefschrift

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To youth and happiness in Holland,

To love of my dear family,

To life

Contents

Summary

Summary

Solid State Lighting (SSL) develops towards small size, high lumen output, high working temperature, and multi-functional applications. These trends are more desirable in miniaturized LED applications such as retrofit G4 LED devices. Retrofit G4 LEDs were chosen in this work as a technical carrier due to the miniaturized size challenge and high lumen requirements. The solutions for miniaturized retrofit G4 can also be extended to other applications of consumer lighting applications with similar requirements.

In Chapter 1, seven retrofit G4 LEDs are analyzed and compared for size, lumen output, number of LED dies, and system efficacy. Currently, there is no real retrofit G4 LED which gives high lumen output similar to traditional halogen G4 lamps. This is mainly due to the big size capacitor requirement and poor thermal management. Therefore, working temperatures of LED dies, capacitors and rectifier (Schottky diodes) were further analyzed via thermal infrared imager. Thermal management in such miniaturized SSL applications is crucial for not only lumen output but also reliability. A rectifier composed of Schottky diodes suffers high reverse leakage current under high working temperatures. Electrolytic capacitors lifetime drops by 50% for each 10 °C rise in the operating temperature. Furthermore, such capacitors are usually too bulky for miniaturized systems such as G4 LED applications.

Therefore, in Chapter 2, chip level packages with different packaging methods are investigated for lower junction temperature. A LED product with traditional surface mounted devices (SMD) technology was chosen. The simulation calculation was compared for Chip on board (COB), and Chip on Heatsink (COH) technology. Compared with traditional SMD, COH package lowers the junction temperature by 30% and brings a 27% drop of the total thermal resistance. The total power from the LED with COB or COH technology can, therefore, be pushed from 1 W to 1.5 W within the limited volume.

However, with all chip level packages, it is still not possible to generate enough lumen output within the limited size compared to traditional halogen G4 lamps. Therefore, Chapter 3 focused on the driver topology to power up more LED dies within the small form factor. Both the linear mode and switch mode driver were investigated. Linear driver brings inductor-free topology which saves volume. However, the linear driver suffers from low energy efficiency and not possible for smart sensor control. Therefore, switch mode driver was introduced. With the help of the control IC, the driver can power up multiple LEDs and give control to sensor systems. With both modes of LED drivers, components involved were then divided as off-chip and on-chip categories.

Therefore, Chapter 4 focused on monolithic wafer level integration (WLP) on a silicon substrate. Silicon substrate is chosen in this work due to the low voltage application, excellence thermal conductivity, and the possibility for on-chip device integration. In Chapter 4, a rectifier composed of four Schottky diodes was monolithically integrated on silicon. Such Schottky diodes with guard ring structures processed under a standard BiCMOS process can reach a breakdown voltage of 27 V. The breakdown voltage mainly relies on n-well doping concentration. Based on the integrated Schottky diodes, a WLP rectifier was tested as part of the G4 LED driver in Chapter 4. In order to guarantee the high-quality light output, the spice model of Schottky diode was derived from characterization, thus have the whole driver circuit simulated to avoid light flicker. Not only Schottky diodes, smart sensors targeting for SSL applications were also investigated for monolithic wafer level integration. Temperature sensor and light sensor based on silicon were studied. The methodology of how to choose such sensors in miniaturized SSL systems is also presented in Chapter 4.

After this initial test, it is clear that in order to get more lumen output, more LED dies need to be integrated. However, wafer level process is usually 2D, thus not possible to shrink the size as small as traditional G4. Therefore, Chapter 5 reports a silicon-based rigid/flex substrate used in this work for miniaturization. A 2D wafer level process enabled silicon substrate to be planarly fabricated, then easily released and assembled

into 3D for uniform light distribution. Five silicon islands equipped with LED dies placed with a light reflection layer on silicon were connected by Aluminium/Polyimide interconnects. Such flexible Aluminium/Polyimide interconnects, with designed Mean Time To Failure (MTTF) up to 25,000 hours, allowed bending angles up to 90°. Such flexible hinges also brought a “breeze” effect for this novel WLP flexible package when heated up which allows further absorbing of the tension caused by thermal expansion. The final Rth of the package is only 2.3 k/W thanks to the superior thermal conductivity of the silicon substrate. The package can work up to 2 W input to reach 85 lumen output, with the working temperature at 85 °C. Such 3D substrate folding provided volume saving together with possibilities for device integration, heat management, smart control, etc. The main application of such designed WLP package is in general aimed at retrofit G4 LEDs.

Based on the integrated rectifier, smart sensors, and flexible substrate developed, two prototypes were built and are described in Chapter 5. One is based on inductor free linear driver, with the total size only 1/4 of the original G4 LED and increased lumen output up to 90 lm (increased 60 % compared with original G4 LED). The other is a switch mode buck driver with a similar total size as the original G4 LED, but with lumen output increase up to 64 %. Furthermore, smart control for light output was also demonstrated by dimmed light when reaching high working temperatures (>85 ˚C). Such a platform enables wafer level integration for both monolithic and heterogeneous devices. However, these two prototypes are still missing heatsink/heat pipes for better thermal management.

It is worth to mention, that since flexible substrate was introduced in the system for size reduction, flexible substrate based sensors were also investigated in Chapter 6. Polyimide mentioned in Chapter 5 was chosen as presence sensor antenna material. A millimeter wave (mmW) sensor operated at 60 GHz with flexible antenna composed of Polyimide and aluminum were simulated, designed, and further tested. A vertical transition between microstrip and CPW lines was also investigated. Such Polyimide (PI) based antenna provides comparable performance compared with traditional antenna fabricated on Quartz substrate, but at a much lower price.

In summary, silicon-based rigid/flex substrate demonstrated great potential for SSL applications aimed at miniaturization and multi-functions, with combining the silicon-based wafer level integration technologies and the flex interconnects for volume saving and improved reliability.

Samenvatting

Samenvatting

Solid State Lighting (SSL) ontwikkelt zich in de richting van klein formaat, hoge lichtopbrengst, hoge bedrijfstemperatuur en multifunctionele toepassingen. Deze trends zijn meer wenselijk in geminiaturiseerde LED-toepassingen zoals retrofit G4 LED-apparaten. Retrofit G4-LED's werden in dit werk gekozen als een technische drager vanwege de uitdaging met verkleinde afmetingen en hoge lumenvereisten. De oplossingen voor geminiaturiseerde retrofit G4 kunnen ook worden uitgebreid naar andere toepassingen van consumentenverlichtingsapplicaties met vergelijkbare vereisten.

In hoofdstuk 1 worden zeven retrofit G4-LED's geanalyseerd en vergeleken op grootte, lichtopbrengst, aantal LED-stempels en systeemeffectiviteit. Op dit moment is er geen echte retrofit G4 LED die een vergelijkbaar hoge lichtopbrengst geeft als traditionele halogeen G4-lampen. Dit komt voornamelijk door de grote condensatorbehoefte en slecht thermisch beheer. Daarom werden werktemperaturen van LED-chips (dies), condensatoren en gelijkrichter (Schottky-diodes) verder geanalyseerd met behulp van een thermische infraroodbeeldvormer (imager). Thermisch beheer in dergelijke geminiaturiseerde SSL-toepassingen is cruciaal voor niet alleen de lumen-output, maar ook de betrouwbaarheid. Een gelijkrichter die is samengesteld uit Schottky-dioden lijdt onder hoge werktemperaturen aan een hoge omkeerlekstroom. De levensduur van de elektrolytische condensatoren daalt met 50% voor elke stijging van 10 °C in de bedrijfstemperatuur. Verder zijn dergelijke condensatoren gewoonlijk te volumineus voor geminiaturiseerde systemen zoals G4 LED-toepassingen.

Daarom worden in hoofdstuk 2 chipniveau-pakketten met verschillende verpakkingsmethoden onderzocht voor lagere junctietemperatuur. Er is gekozen voor een LED-product met traditionele SMD-technologie (surface mounted devices). De simulatieberekening werd vergeleken voor Chip on board (COB) en Chip on Heatsink (COH) -technologie. In vergelijking met traditionele SMD verlaagt het COH-pakket de junctietemperatuur met 30% en brengt het een daling van 27% van de totale thermische weerstand met zich mee. Het totale vermogen van de LED met COB- of COH-technologie kan daarom binnen het beperkte volume van 1 W naar 1,5 W worden geschakeld.

Bij alle chipniveau-pakketten is het echter nog steeds niet mogelijk om voldoende lichtop-output te genereren binnen de beperkte afmeting in vergelijking met traditionele halogeen G4-lampen. Daarom richtte Hoofdstuk 3 zich op de driver-topologie om meer LED-chips (dies) in te schakelen binnen de kleine vormfactor. Zowel lineaire modus als schakelmodus drivers werden onderzocht. De lineaire driver brengt met zich mee inductor-vrije topologie die volume bespaart. De lineaire driver heeft echter een lage energie-efficiëntie en is daarom niet mogelijk voor slimme sensorbesturing. Daarom werd de driver voor de schakelmodus geïntroduceerd. Met behulp van de besturings-IC kan de bestuurder meerdere LED's inschakelen en de besturing van sensorsystemen regelen. Met beide modi van LED-drivers werden de betrokken componenten vervolgens verdeeld als niet-on-chip- en on-chip-categorieën.

Daarom concentreerde Hoofdstuk 4 zich op monolithische wafer-niveau-integratie (WLP) op siliciumsubstraat. Siliciumsubstraten zijn in dit werk gekozen dankzij de lage spanningstoepassing, uitstekende thermische geleidbaarheid en de mogelijkheid voor on-chip apparaatintegratie. In hoofdstuk 4 was een gelijkrichter die uit vier Schottky-diodes bestond monolithisch geïntegreerd op silicium. Dergelijke Schottky-diodes met beschermingsringstructuren verwerkt onder een standaard BiCMOS-proces, kunnen een doorslagspanning van 27 V bereiken. De doorslagspanning hangt hoofdzakelijk af van de n-well dotering concentratie. Op basis van de geïntegreerde Schottky-diodes werd in hoofdstuk 4 een WLP-gelijkrichter getest als onderdeel van de G4 LED-driver. Om de hoge kwaliteit van de licht-output te garanderen, werd het spice-model van de Schottky-diode afgeleid van de karakterisering, waardoor het hele stuurcircuit werd gesimuleerd om lichtflikkering te voorkomen. Niet alleen Schottky-diodes, maar ook slimme sensoren gericht op SSL-toepassingen werden onderzocht voor monolithische integratie op

substraatniveau. Temperatuur en licht sensoren op basis van silicium werden bestudeerd. De methode voor het kiezen van dergelijke sensoren in geminiaturiseerde SSL-systemen wordt ook gepresenteerd in hoofdstuk 4.

Na deze eerste test is het duidelijk dat er meer LED-chips (dies) moeten worden geïntegreerd om meer lichtopbrengst te krijgen. Het proces van substraatniveau is echter meestal 2D, dus het is niet mogelijk om de grootte zo klein te maken als de traditionele G4. Daarom rapporteert hoofdstuk 5 een op silicium gebaseerd rigide/flex-substraat dat in dit werk wordt gebruikt voor miniaturisatie. Een 2D substraatniveau proces heeft het mogelijk gemaakt om het siliciumsubstraat vlak te fabriceren, vervolgens de structuur eenvoudig los te maken van het substraat en assembleren in 3D voor uniforme lichtverdeling. Vijf siliciumeilanden uitgerust met LED-chips (dies) geplaatst met een lichtreflectie-laag op silicium werden verbonden door middel van aluminium/polyimide verbindingen. Dergelijk flexibel aluminium/polyimide verbindingen, met ontworpen Mean Time To Failure (MTTF) tot 25.000 uren, staan buighoeken toe tot 90°. Dergelijke flexibele scharnieren brachten ook een "bries" -effect met zich mee voor dit nieuwe WLP-flexibele pakket wanneer het wordt opgewarmd, waardoor de spanning die wordt veroorzaakt door thermische uitzetting verder wordt geabsorbeerd. De uiteindelijke R_{th} van de verpakking is slechts 2,3 k/W dankzij de superieure thermische geleidbaarheid van het siliciumsubstraat. Het pakket kan tot 2 W input verwerken om 85 lumen output te bereiken, met een werktemperatuur van 85 °C. Dergelijke 3D-substraatvouwing bood volumebesparingen samen met mogelijkheden voor apparaatintegratie, warmtebeheer, slimme besturing, enz. De hoofdtoepassing van een dergelijk ontworpen WLP-pakket is in het algemeen gericht op retrofit G4-LED's.

Op basis van de geïntegreerde gelijkrichter, slimme sensoren en het ontwikkelde flexibele substraat zijn twee prototypen gebouwd en beschreven in hoofdstuk 5. Eén is gebaseerd op een inductorvrije lineaire driver, met een totale afmeting van slechts 1/4 van de originele G4 LED en verhoogd lumen output tot 90 lm (toegenomen 60% vergeleken met de originele G4 LED). De andere is een schakelmodus buck-driver met een vergelijkbare totale grootte als de originele G4-led, maar met lumen-output verhoogt deze tot 64 %. Bovendien werd slimme controle voor de lichtop-output ook gedemonstreerd bij gedimd licht bij het bereiken van hoge werktemperaturen (> 85 ˚C). Een dergelijk platform maakt integratie op substraatniveau mogelijk voor zowel monolithische als heterogene apparaten. Echter, deze twee prototypen missen nog steeds heatsink/heat pipes voor beter thermisch beheer.

Het is de moeite waard om te vermelden dat, omdat flexibel substraat in het systeem werd geïntroduceerd voor het verkleinen van de afmetingen, sensoren op basis van flexibel substraat ook werden onderzocht. Polyimide genoemd in Hoofdstuk 5 werd gekozen als antennemateriaal van de aanwezigheidssensor. Een millimetergolf (mmW) -sensor op 60 GHz met flexibele antenne samengesteld uit Polyimide en aluminium werden gesimuleerd, ontworpen en verder getest. Een verticale overgang tussen microstrip- en CPW-lijnen werd ook onderzocht. Een dergelijke op polyimide (PI) gebaseerde antenne biedt vergelijkbare prestaties in vergelijking met traditionele antennes die zijn gefabriceerd op kwartsubstraat, maar voor een veel lagere prijs.

Samengevat toonde silicium-gebaseerd rigide / flex-substraat een groot potentieel voor SSL-toepassingen gericht op miniaturisatie en multi-functies, met een combinatie van op silicium gebaseerde wafer-niveau-integratietechnologieën en de flex-interconnects voor volumebesparing en verbeterde betrouwbaarheid.

Chapter 1 Introduction

1.1 Solid State Lighting

Electronics systems influence every aspect of our lives and play a vital role in day to day activities. The semiconductor industry is a key driver for the development of many industries such as education, transportation, biomedical, communication and entertainment, etc. One of the most influential developments in the semiconductor industry over the last decade has been with the advent of Solid State Lighting (SSL) for the general lighting application. Similar to the history of electronics which turns from vacuum tube era to the semiconductor revolution, lighting industry today is also following the similar path which turns traditional incandescent bulb to SSL systems.

Technology for the lighting industry began with the invention of the incandescent bulb by Thomas Alva Edison in 1879. Later in the year 1906, General Electric patented the first tungsten light bulb. Though incandescent lamps are very cheap to manufacture, they were inefficient as they convert only about 1% to 5% of the consumed electricity into usable light. The next generation of lighting technology followed by the introduction of the fluorescent lamp in the 1930s. These lamps have improved efficiency than incandescent bulbs but contain small amount toxic gases like mercury which is harmful to the environment. Due to the above drawbacks of incandescent and fluorescent lamps, there is a need for the lighting industry to create lighting systems that are efficient, have lower manufacturing cost and reduced pollution[1]. For this development, there has been a lot of interest in the field of Solid State Lighting as it provides good potential for energy efficient, safe and affordable lighting solutions. Solid State Lighting, commonly called SSL, is a novel lighting technology basically composed of light emitting diode (LEDs), microelectronics drivers, and a housing. Such a technology brings lighting industry from incandescent glass bulbs into the domain of electronics, enables a lighting system with microelectronics and MEMS functionalities, such temperature sensing, presence sensing and other functions [2]. In the recent survey, the lighting market, including light sources(LEDs), electronics and luminaries are estimated to increase from €50 billion in 2010 to €70 billion by the year 2020 [3].

Solid State Lighting refers to light obtained from semiconductor devices. The first report on electroluminescence was published by Henry J Round in 1907 when he found that current passed through carborundum diode emitted light. But the invention of Light Emitting Diode is credited to Russian scientist Losev who correctly explained the phenomena of light emission in silicon carbide diodes used in his work on radio receivers [4]. Light Emitting Diodes are p-n junction diodes which forward biased emit light by spontaneous recombination of electron-hole pairs and simultaneous emission of photons. LEDs are made from silicon carbide material or III–IV semiconductor like gallium arsenide, gallium nitride. The light emitted from LED occupies a narrow spectrum, and the specific wavelength or color depends on the band gap of the material. Early developed LEDs emit mainly red, blue, and green light which used as indicators, displays in electronic systems due to their low lumen/watt till the early '90s.

The development of white LEDs in mid-'90s provided interest to use LEDs as an alternative to general lighting. Most white light LEDs use an LED emitting at a shorter wavelength (e.g. blue) and a wavelength converter (e.g. phosphor). The light emitted by the blue LED is absorbed by the phosphor material and converted as white light with a longer wavelength. [1] Such invention has accelerated the growth of SSL-systems since white light is widely applied in the consumer market. SSL systems offer new possibilities to the lighting industry since it is energy saving, high reliability, good color rendering, and low power dissipation. LED is a highly energy efficient lighting technology which has the potential to fundamentally

change the future of lighting. However, the design of the LED lighting system, as a multi-domain system, is complex and different from conventional lighting. It provides many design and reliability challenges in the area of electrical, packaging, optical and luminaries. The design of Solid State Lighting (SSL) system is different from the conventional lighting system design, but closer to a microelectronics system design.

Despite many advantages, the high price of the SSL system is still the main drawback for consumers. Novel SSL applications, though with advanced features, still need to compete with low-cost existing solutions in the consumer market. Though energy saving leads to fewer energy bills on lighting, the initial high cost of LEDs compared with traditional lighting is still the greatest barrier in switching to LED technology from conventional lighting. Therefore, EU and China have already established regulations to foster such transition, to ensure less energy consumption and less CO_2 emission. Depending on the application, the packaging of the current luminaries accounts for up to 60% of the overall manufacturing costs [1]. Therefore, creative packaging solutions are necessary to bring the costs down, e.g. wafer level packaging, which will be illustrated later in this work.

1.2 Challenge for Miniaturized Solid State Lighting Applications

One key market for SSL lighting is consumer lighting, in which retrofit lamps play a very important role. Retrofit LED lighting allows to combine the advantages of solid state lighting with the existing infrastructure. Among these retrofit LED products, G4 LEDs are considered as a real challenge due to the intrinsic miniaturized size. Therefore, challenges for such miniaturized SSL application is representative. The solutions can be extended to solve other retrofit problems. Therefore, G4 retrofit LEDs were chosen as a technical carrier in this work.

Halogen incandescent bulbs usually operate at high temperature (surface temperature around 250°C - 350°C), so protective glass and plastic shell is usually needed as thermal shields for security reasons [5]. G4 Halogen lamps, as shown in Fig. 1.1, offer a white light source with excellent color rendering and a large amount of visible and infrared energy due to the high operating temperature. Some hot spots on the bulb wall itself can approach as high as 700°C. This heat generation is, on one hand, critical to the self-cleaning effect of halogen lamps to prolong the lifetime of the filament. On the other hand, the high temperature has consequences for the lamp architecture by safety requirements and applications. The efficiency of a typical 12V G4 halogen lamp ranges from 14-18 lumen/Watt (lm/W), not taken into account the fixture losses and transformer losses. Therefore, a G4 halogen lamp, as a traditional consumer light source, needs to be improved due to its low energy efficiency and short lifetime.

Fig. 1.1 Traditional G4 halogen lamp (Halogen Capsule lamp, 20W, G4, Warm white, 310 lumen) [6]

The comparison between LED retrofit lamps and halogen lamps were listed in Table 1.1. Today still more than 90% of consumer luminaries sold today are designed for conventional G4, due to its very tiny size. There is a strong desire for a G4 LED capsule replacing the very inefficient conventional halogen lamp,

within the limited volume. Furthermore, it is also very challenging to generate the desired lumen within the limited volume which have been historically constrained by the limitation of halogen bulbs. Lumen, symbolled as lm, is a universal measure unit of total quantity of visible light emitted by a source. Lamps used for lighting are commonly labeled with their light output in lumens. Therefore, effective solutions are focusing on how to get more lumen output from retrofit miniaturized SSL applications in this work. In order to reach this goal, two main challenges are identified for small form factor applications: thermal management and functional driver electronics integration.

At this moment, there are a variety of products from different companies providing G4 LED retrofit lamps. However, none of them can compete with traditional halogen lamps. Besides its high cost, the lumen output is the biggest issue, which is closely related to thermal management. In incandescent light sources, 90% heat is dissipated through the glass encapsulation and for a large part by radiation (Fig. 1.2). Halogen bulbs are similar to incandescent light, but more efficient. This is because a small amount of halogen gas mixes with tungsten vapor within the bulbs allows it to work at a much higher temperature. However, it is worth to mention that halogen lamps produce a considerable amount of infrared (IR) and ultraviolet (UV) radiation that not only leads to energy waste but also damages to fabrics and artwork. But for LED lighting, since they do not produce heat in the form of infrared (IR) radiation (unless if they are IR LEDs), waste heat is much less compared by traditional light sources. Most of the heat is dissipated through the package and mainly by convection. Due to current packaging technologies, it is difficult to provide more than 100 lm within a limited space. Furthermore, none of the products on the market has the same size as traditional G4, which makes it even more difficult to compete with traditional lighting products. As a start, 7 commercially available G4 LED products were firstly chosen to be analyzed, as shown in Table 1.2. With respect to their technology concepts, design approaches, packaging materials, and performance, these products fall into two categories: high performance and small volume.

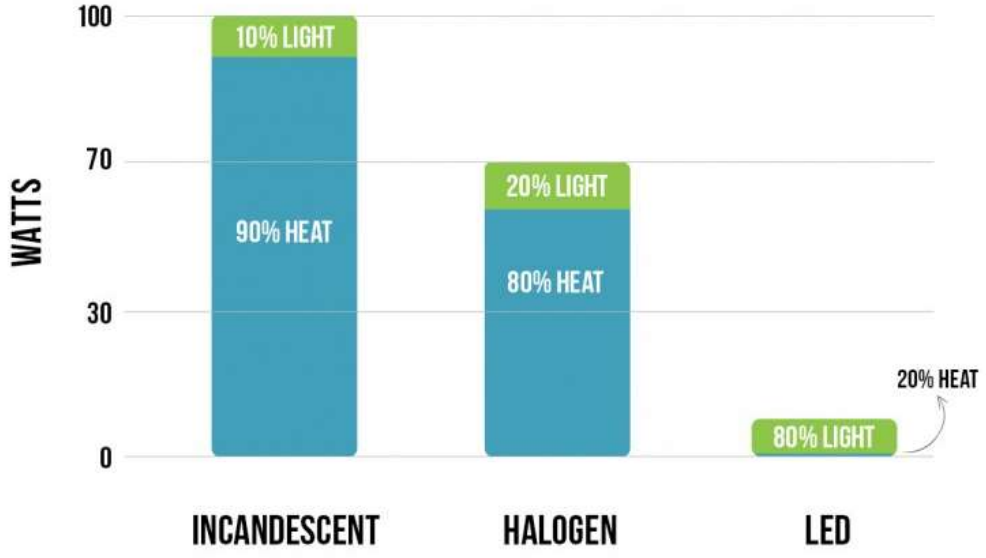

Fig. 1.2 Energy consumption comparison with the equivalent light output of incandescent lamps, halogen lamps, and LED lamps [7]

Table 1.1 Comparison of Traditional halogen lamps with LED retrofit lamps and main challenges

Type of lamps	Characteristics	Main challenges
Halogen lamps	white light Excellent beam control Compact size High lumen maintenance Short lifetime (1-3 years) Large amounts of visible and infrared light	Be more energy efficient. Through 3 times longer life than incandescent bulbs, a lifetime of halogen lamps is only around 3600 hours. Color control/rendering. IR and UV radiation can be damaging to fabrics and artwork. Working temperature can lead to skin burns if touched.
LED retrofit lamps	Significant energy savings Long lifetime up to 50,000 hours Minimized maintenance and related costs Cool burning Instant ON/OFF, no warm-up time Compatible controls No mercury or lead, RoHS compliant Extremely low ultraviolet (UV) and infrared (IR) light	Size limitation for electronics e.g. Capacitor (without proper electronic design, a capacitor for energy storage can be as large as a G4 halogen lamp) Lumen output to be comparable with halogen lamps (e.g. high energy efficiency, high energy density) Thermal management within the size limitation (e.g. miniaturized heatsink, active cooling devices, etc.)

Table 1.2. State of the art of Retrofit G4 LEDs characteristics

`	Lumen (lm)	Size		No. LEDs	Power (W)	System efficacy (lm/W)	category
		Diameter (mm)	Length (mm)				
halogen	350	9	32	-	20	18	
1	56	13	37	1	1	56	Small volume
2	110	9	34	24	1.5	73	
3	180	30	4	12	2.4	75	
4	60	14	41	4	0.8	75	High performance
5	140	14	36	6	2	67	
6	120	19	45	5	2	60	
7	250	17	41	18	2.2	114	

Firstly, LEDs with different power input were chosen in these products. 6 out of 7 products were using mid-power LEDs instead of high power LEDs. Mid-power LEDs have been applied more and more in recent years, due to uniformity, tuneable string voltage, and low price. However, mid-power LED packages are usually bigger than high-power ones. On the other hand, high-power LEDs are more compact, usually with high flux, and more reliable. For high-performance category, usually more LEDs are applied.

Secondly, let us take a look at the topology of the driver design. Despite a various number of LEDs and different design concepts, the driver systems for G4 LEDs are similar. The input voltage requirement of G4 LED capsule is 12V AC. A driver for a G4 LED usually contains four Schottky diodes as a rectifier, a large capacitor for energy storage, and an IC driver. A common topology design of the driver is shown in Fig. 1.3. The input 12V AC is first converted into DC by a bridge rectifier. The bridge rectifier commonly uses Schottky diodes due to their low forward voltage drop and high current conduction. After the rectifier, there are mainly two methods to maintain a constant current in LED driver systems: a linear driver or a switch mode driver. However, no matter which driver system is applied, a sizable capacitor is necessary. The capacitor is too bulky for the total system in terms of the size, and brings reliability problems when it becomes too close to LED chips.

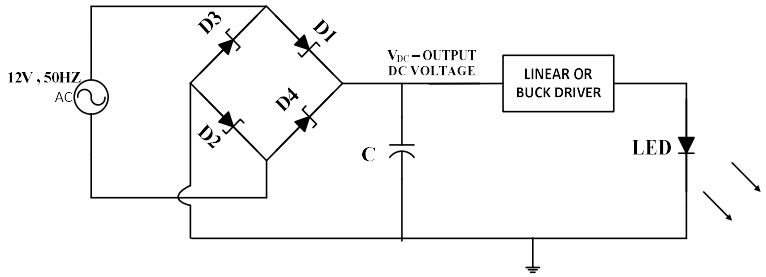

Fig. 1.3 Schematic of a low power 12V LED system

Thirdly, thermal management is paid special attention since it is crucial for a lifetime. For improved thermal management, heat sinks are also designed according to different technology concepts. Therefore, such designs usually go along with large form factors, typically 3 times the size of conventional G4 halogen lamps. Because high junction temperature will induce thermal activation of non-radiative electron-hole recombination, it is important to keep junction temperature low to have a reliable system.

Therefore, for better understand the thermal behavior of these 7 LED retrofit G4 products, all drivers are separated and a thermal infrared imager is applied to each driver to find the location(s) with the highest working temperature (see Fig. 1.4). The measurements were carried out when the lamp is the just light up and when they are stable (after 1 hour). This is due to the fact that in most failures of LED lamps, driver systems are identified as a weak point, and among driver failure mechanisms, the high temperature is the most influential factor.

The measurements were focused on the LED, PCB, Schottky diodes, and capacitors (see Fig.1.5 and Fig. 1.6). Junction temperatures are the highest in the system. When just light up, we noticed in sample 3, 4, 5 and 7, the temperature of Schottky diodes are almost as high as LEDs, while the temperature of LEDs is the highest in the system. After 1 hour, the temperature of the Schottky diodes of sample 3, 5, 6 and 7 are still almost as high as LEDs. The temperature increase of Schottky diodes ranges from 2 to 33 °C among different samples. In silicon-based commercialized Schottky diodes, the increase of temperature

leads to a reduction of the forward voltage of drops 1.2mV/°C [2]. But more severe, the reverse leakage current is increased with temperature, which leads to thermal instability. Therefore, it is important to have Schottky diodes with better reliability or apply them in a better thermal managed system.

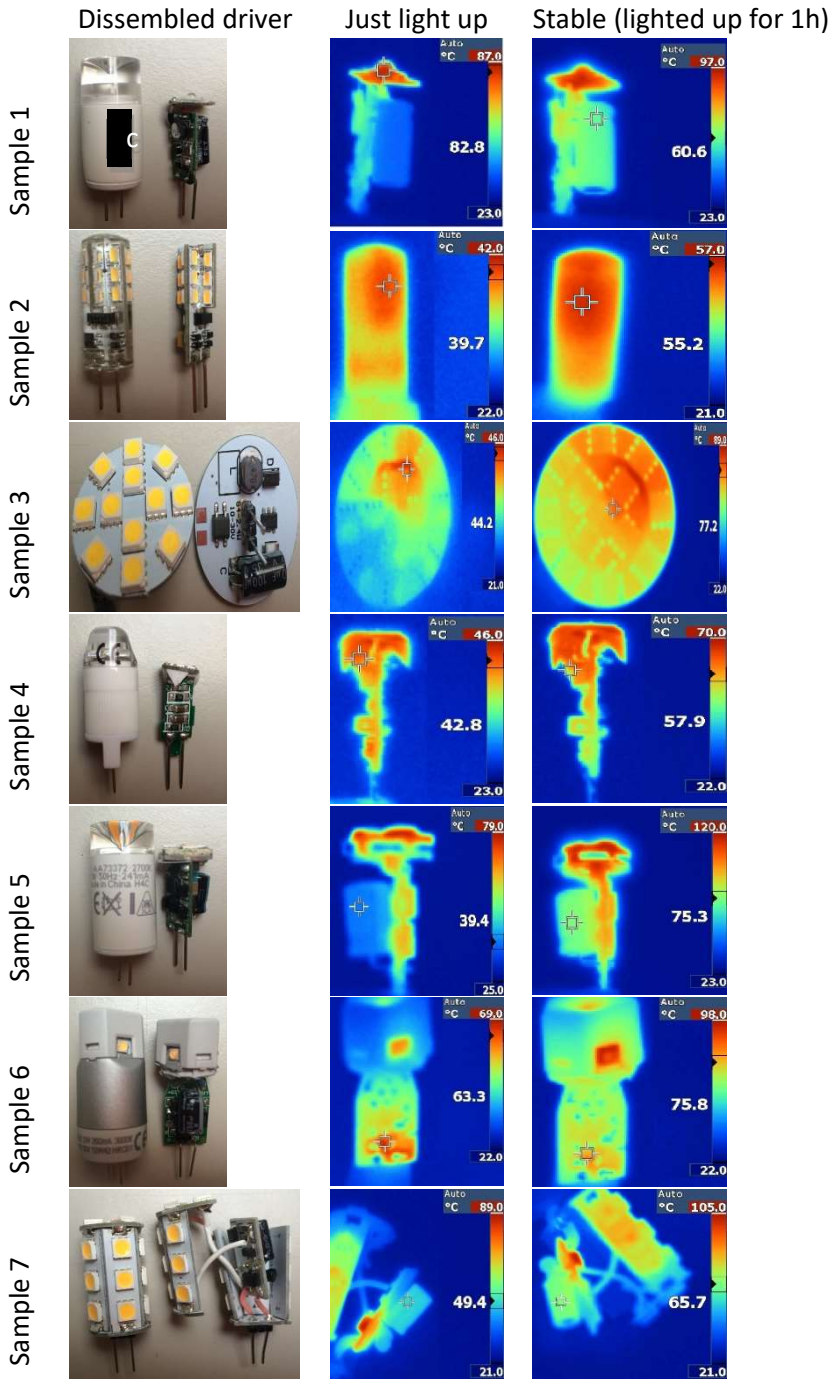

Fig. 1.4 Dissembled driver and infrared camera photos of seven samples.

More specifically, the capacitor was recognized as the most vulnerable component in most LED drivers. Therefore, we take close look at capacitors applied in G4 LEDs. 6 out of 7 products are using electrolytic

capacitors as energy storage, whose lifetime is relatively short compared to LED dies. Due to the small form factor, the capacitors are heated up by 10 to 35 °C from just light up to 1-hour stable operation. The lifetime of an electrolytic capacitor drops by 50% for each 10 °C rise in the operating temperature. A typical electrolytic capacitor can survive 10000 h at 105°C, while most LED products claim themselves with a lifetime of 25000 h. [3] Furthermore, electrolytic capacitors are usually bulky which brings crucial problems to miniaturized applications such as G4 LEDs. To sum up, the electrolytic capacitor is too big and not reliable enough for miniaturized systems such as G4 LED applications.

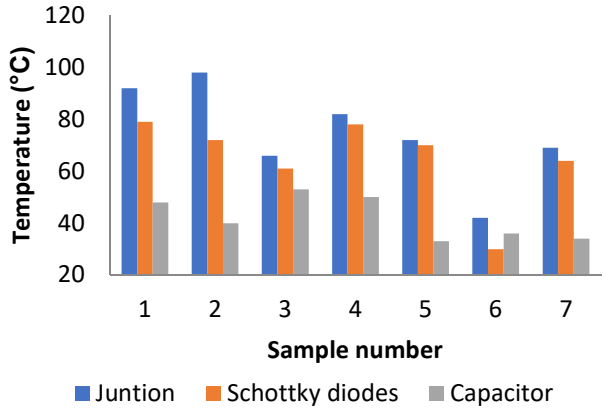

Fig. 1.5 Temperature comparison of 7 samples when just light up.

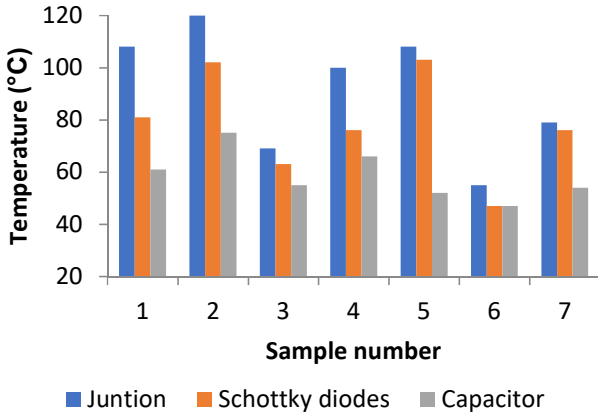

Fig. 1.6 Temperature comparison of 7 samples when they are stable after lighting up for 1 hour.

Consequently, G4 LED applications require novel capacitor technologies with higher temperature tolerance and smaller form factors. Thin film capacitors are one of the promising replacement, since they are with longer lifetime compared with electrolytic capacitors. Dielectric, ferroelectric, and piezoelectric thin films are excellent candidates for multifunctional miniaturized applications, with respect to performance, size, and cost. High dielectric constant materials such as BaTiO3, PbZrxTi1-xO3 (PZT) are reported in [4]. Besides ultrahigh-k dielectric materials, large capacitance areas are also interested by researchers, such as high-density trench capacitors [5]. With DRIE etching, the lateral size of these capacitors can be minimized by three orders of magnitude in comparison with thin film, without the need for ultra-high k materials.

Furthermore, it worth to mention that none of these 7 G4 LED products on the market were equipped with smart control. With smart lighting, you can easily change your home atmosphere with a single touch, or dim them, or change the color temperature. Besides improved customer experiences, implementing an advanced LED lighting system offers energy and maintenance savings. Presence sensing and light sensing can save energy when there is no need. Temperature sensors can protect the LED luminaires from overheat. However, with these 7 G4 LED products, it is difficult to combine smart sensing due to the size limitation and high working temperature. Therefore, it is essential to develop a new packaging concept for miniaturize G4 LED size, and provides multi-functional controls.

To sum up, with a detailed analysis of G4 LED drivers, challenges for miniaturized SSL applications are:

1) small form factor;

2) high temperature under stable operation;

3) reliability risks for capacitors and Schottky diodes during high working temperature;

4) smart control for further energy saving.

Therefore, a new package developed targeting at these challenges will be introduced in the following of this work. To develop such miniaturized and multi-functional package, we need to first take a close look into packaging methods of the LED dies, to estimate how much lumen we could maximum get out this G4 size. Based on this limitation, we can decide how many LED dies are needed in this system. Hence, the driver circuit can be simulated to improve the efficiency and guarantee high-quality light output. Based on the simulation results, the components needed for the driver can be then divided into on-chip components and off-chip components. On-chip components are possible to fabricate in-house with BiCMOS process to be monolithically integrated on a silicon wafer. Off-chip components then need to be packaged to fit in the miniaturized system. Based on such requirements, a silicon-based rigid/flex substrate is then investigated and tested for this G4 retrofit LED application.

1.3 Thesis Outline

As mentioned before in introduction, retrofit G4 LED was chosen as a technical carrier for this miniaturized SSL system integration, due to its size limitation and high lumen output expectation. Therefore, state of the art products was analyzed by an infrared camera to identify the critical components (e.g. capacitor, rectifier, etc.). To improve lumen output in such a small form factor, better thermal management and smart control are needed for improved performance and reliability.

Based on such request, different packaging methods were compared for G4 LED packages in Chapter 2. Such comparison offers insight for thermal management of critical components. For better understand the driver circuit and the components involved, G4 LED driver was analyzed in Chapter 3. Two modes of the driver were introduced, linear mode driver and switch mode driver, respectively. Components related to the two set up were divided into on-chip components and off-chip components based on in-house available technology.

Silicon wafer level integration was then introduced for on-chip components in Chapter 4. Monolithic integrated Schottky diodes behave as rectifiers for G4 LED. Spice models of in-house fabricated Schottky diodes, NPN transistors, resistors, etc. were generated. Simulation-based on these spice models guaranteed a high quality of light output. Temperature sensor and light sensor were also investigated for on-chip integration. Design methodology for such sensors in miniaturized applications was also introduced. Based on these in-house fabricated devices, integrated driver system was initially tested in Chapter 4.

However, lumen output tested in Chapter 4 were not enough for G4 retrofit, therefore more LEDs need to integrate into the system. As a result of that, a silicon-based 3D rigid/flex substrate was introduced in this thesis for multifunctional LED module integration and miniaturization. Such substrate is not only suitable for wafer level integration for SSL applications, but also possible to combine the advantage of silicon integration for LED, driver electronics, and sensors, and the folding properties for miniaturization. This is due to the benefits of the silicon substrate who offers numbers of possibility for device integration, either monolithically or heterogeneously. Meanwhile, the high thermal conductivity of silicon provides fast heat dissipation for LED dies.

Therefore, in Chapter 5, such a micro-machining technology platform is proposed, fabricated, and tested. A new method of photolithography for 3D packages is developed. Wafer level device integration developed in Chapter 3 and 4 can be further combined with such a platform. Chapter 5 also demonstrated this 3D WLP performance with different driver scenarios.

Since flexible substrate was introduced in the system for size reduction in Chapter 5, flexible substrate based sensors were also investigated in Chapter 6. A polyimide-based flexible antenna for millimeter wave presence sensing was simulated, designed, and tested. A vertical transition between microstrip and CPW lines also enables the signal transfer through polyimide substrate to IC chips with a bond wire-free connection. This opens the door for sensors integration on a flexible substrate, which leads to cost reduction. In the end, a summary of the major findings of each chapter is listed.

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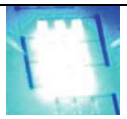
Chapter 2 LED Packaging Technologies

2.1 Solid State Lighting System

Electronics components comprise more than 50% of a complete SSL system cost. [1] Therefore, as already mentioned in the introduction, an SSL system design is much closer to a microelectronics system design. Electronic packaging usually refers to chip-level packaging, board-level packaging, and system-level packaging. Chip-level packages include electronic functional devices (e,g, active, passive, or electromechanical devices, etc.). The board-level packages assemble chips or multi-chips together with additional components, e.g. capacitors, resistors, inductors, switches, etc. System-level packages normally refer to the outer enclosure or shell of the electronics, such as PCB to PCB interconnections. [2,3]

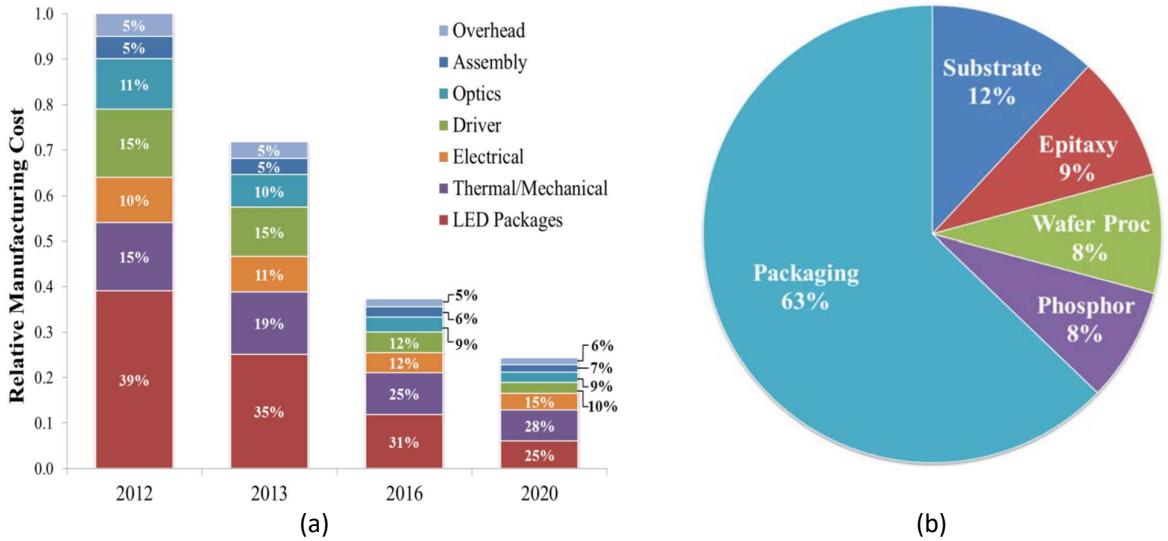
For an SSL system, the main semiconductor IC components of this system are LED dies, power converters and driver circuitry. The assembly process is usually separated into levels from 0 to 5. A summary of SSL system components and its functions is presented in Table 2.1. [2] Level 0 is epitaxial and chip production. Level 1 is chip packaging. level 2 is soldering the LED onto a substrate, e.g. PCB. Level 3 is the LED driver control and integration. Level 4 is lighting source design, and level 5 is the system of lighting. For package free chip production, level 1 can be eliminated. Elimination of level 1 avoids the use of lead frames and bonding wires, therefore reduces the total thermal resistance of the system.

Table 2.1 Levels of SSL System

Level	System Component	Example	Function
0	LED Die		To achieve high luminous efficiency
1	LED Package		For electrical connection, heat dissipation and mechanical stability.
2	Multi LED Board		Increasing the number of LEDs for higher lumen output.
3	LED Power Control and Drivers		To convert AC to DC and provide constant current and control of the LED.
4	Luminaire Designs		To enable usage of LED bulb as conventional bulb by using retrofit design.
5	Lighting System Designs		Multiply interconnected luminaries for lighting system on a large scale.

A composition of the cost analysis of a retrofit lamp is shown in Fig. 2.1 (a) [3]. It worth to mention here that cost breakdown might change as a function of time, as shown in Fig. 2.1 (b). As a common A19 60W retrofit lamp, the manufacturing cost is expected to change, especially for LED packages and driver, which are 35% and 15% in the year of 2013 compared with 25% and 10% anticipated by 2020, respectively. Since LED packaging and thermal/mechanical/electronics are crucial for the total system cost, the integration of both packaging and electronics for the SSL system results in the reduction of total system cost.

From Fig. 2.1(a), it is also clear that in the early phase of product development, the major cost component of the LED system is the LED package which contributes to about 30% of the total LED bulb. When taking a close look into level 1 LED packages, the result is clear that packaging methods greatly influence the total cost, as shown in Fig. 2.1 (b). Manufactures are performing more and more packaging activities at a wafer level in order to reduce the total package cost.



(a) (b)

Fig. 2.1 (a)Cost breakdown Projection for a typical A19 retrofit lamp (b) Typical cost breakdown for an LED package [3]

Therefore, an essential challenge in LED technology is to choose proper packaging methods that provide circuit support and protection, heat dissipation, signal distribution, manufacturability and serviceability, power distribution. [4] Today, more and more LED lighting manufacturers focus on technology gaps to develop packages with different methods that enable heat to be conducted efficiently away to the environment, especially for high brightness LED applications.[5]

2.2 Packaging Methods

The advantages of LEDs are well recognized as energy saving, high efficiency, small size, and lightweight. However, current LED integration technologies are facing challenges to give the desired lumen within the limited volume. LEDs typically have a chip size of 0.2-1.0 mm.[7] Such tiny devices can be applied for a wide range of applications after proper packaging. LED dies, as heat sensitive semiconductor components, are often mounted onto substrates which provide electrical insulation and adequate thermal conductivity. Multiple layers are usually applied to such substrates. However, each layer is a potential risk which brings additional thermal resistivity. With multiple layers and different thermal coefficients of expansion, potential risks are delamination, corrosion, and degradation.

Standard LED package is named Surface Mounted Devices (SMD) package, which contains thermal resistance of LED package, PCB board, heatsink, and applied glue between components. Chip on board (COB) avoided the application of SMD substrate, therefore minimum the thermal resistance. Chip on heatsink (COH) consists of a typical aluminum cooler with a glue bonded chip, which greatly reduced thermal resistance. [8] In this work, we mainly focus on novel chip level packages for solid state lighting applications (chip on board and chip on heatsink), compared with traditional surface mounted devices, as illustrated in Fig. 2.2.

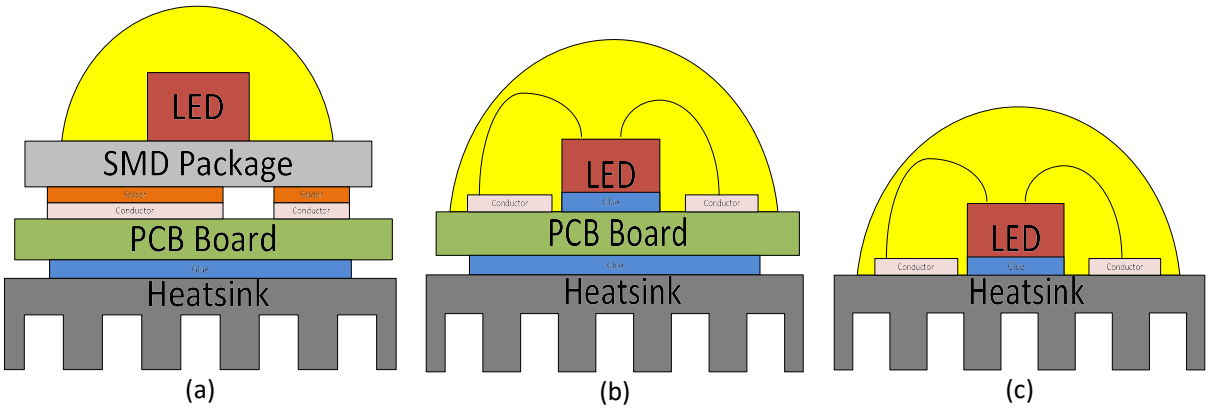


Fig. 2.2 Typical LED system with SMD packages, chip on board, and chip on heatsink [8]

With continuous demands of high performance, low cost, and miniaturized solid state lighting applications, advanced electronic packaging technology will keep facing challenges including innovative thermal management solutions. Thermal management of consumer LED lamps is very important because the excess heat can reduce the light output, produce color shift, and shorten lifetime. Therefore, effective thermal management becomes critical for LED integration methods.

The challenges in thermal management can be viewed in practical as three problems:
1) Heatsink temperature must be maintained at a relatively low level despite high local heat density;
2) High heat loads must meet requirements for critical interfaces (e.g. solder joint) for system connection;
3) The working temperature of critical components (e.g. capacitor) meet the requirement of the desired reliability.

2.3 Thermal Analysis for LED Lamps

In LED lamps, the total heat is generated by 3 sources: heat from the LED junction (blue LED), heat from the phosphor, and heat from the LED driver. From these sources, the total generated heat is mainly dissipated in three ways: conduction, convection, and radiation.[9]

Conduction of heat transfer through solid mediums can be described by Fourier's law, and calculated as:

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)+\dot{q}=\rho c_p\frac{\partial T}{\partial t}$$

where $\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)$ is the net transfer of thermal energy into the control volume, $\dot{q}$ is the thermal energy generation, and $\rho c_p\frac{\partial T}{\partial t}$ is the change in thermal energy storage. k is thermal conductivity(which might be a function of temperature), ρ is density, c_p is heat capacity. [10]
For one-dimensional heat conduction, the thermal resistance of solids is introduced. Therefore, heat transfer through conduction can be written as:

$$q_{cond} = \frac{\Delta T}{R}; R = \frac{d}{kA}$$

where A is the cross-section for transferred amount of heat q_{cond}, d is the thickness, ΔT is the temperature difference. In this work, interface heat resistance is neglected since it is quite small compared with the whole thermal resistance of the whole lamp package.
Convection of heat transfer can be regarded as:

$$q_{conv} = hA(T_s - T_\infty)$$

where h is the convective heat transfer coefficient, A is surface area implied in the heat transfer process, T_s is the system temperature and T_∞ is the reference temperature. Parameter h is not a constant but depends on the type of convection, surface structure, and other geometrical parameters. [11]
Natural convection is a rather complex mechanism. Thermal expansion causes density differences, and thus hot air rises driven by force of density differences. The velocity of air is usually dependent on the geometric environment.

Radiation of heat transfer between surfaces is usually explained as:

$$q_{rad} = \varepsilon \sigma A T^4$$

where σ is Boltzmann constant (5.6704×10-8 W/m2K4), A is the radiating surface area, T is the temperature, ε is the emissivity. [12]

The Optical energy loss is partially converted into heat by the efficiency of the phosphor. The energy of lumen output was calculated based on the following equation:

$$\varepsilon_{e,white}\left[\frac{lm}{W}\right] = WPE\,(T, I) \cdot \varepsilon_{o,ph}\left[\frac{lm}{W}\right] \cdot \eta_{QD} \cdot \eta_{ph}(T) \cdot \eta_{pkg}$$

where $WPE\,(T, I)$ is the output optical power at junction temperature T and forward current I. It is also called wall-plug-efficiency which equals to internal quantum efficiency multiply extraction efficiency and then multiply electrical efficiency. $\varepsilon_{o,ph}$is the luminous efficacy of phosphor; η_{QD} is the quantum deficit in pumping phosphor; η_{ph} is phosphor quantum efficiency; and η_{pkg} is package efficiency. [13]

Based on these fundamental equations, a FEM model was build up to analyze the thermal behavior of a selected retrofit G4 LED product, to check the threshold for junction temperature with increased power input.

2.4 Model Set Up and Simulation Analysis

After fully understand the generated heat source and heat dissipation methods, software COMSOLTM Multi-physics 4.2 was used as a finite element method (FEM) tool for simulation. Models based on Finite element method (FEM) simulations were investigated to find a thermal-efficient integration method that enables heat dissipation and more uniformed heat distribution. The heat transfer module was used to calculate the temperature distribution. Through thermal simulation results and experiments, one can specifically determine which design is the best for applications demanding high lumen output within limited space such as G4 LED retrofit lamps.

An LED product on market (1W, 50 lumen, CRI 80) was chosen as a representative for our packaging study with respect to thermal management. The package was chosen as the driver design is representative of the market considering the state of the art. It equals to 5W of traditional halogen lamps which gives it 80% energy saving. It provides a homogenous light distribution with a 360° radiation angle. A simplified model was built for thermal investigations, as Fig. 2.3 explains. A round PCB (FR4) with a white LED is placed with

LED driver under it. The LED lamp is put into a G4 socket but has no heat dissipated through the socket. The measurement of thermal behavior was used to calibrate the simulation models since the model was build up based on several simplifications.

There are several ways to measure the thermal behaviors of an LED product, which are the thermocouple, thermography and transient thermal analysis. In this work, a thermocouple was chosen for characterization since it is quick responded, standardized, and with a wide operation range.

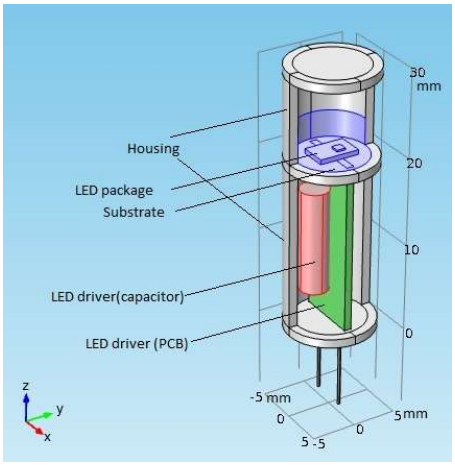


Fig. 2.3 FEM model for a G4 LED product for thermal calculations. (with half housing)

The efficiency of blue LED is around 40% to 50%. Phosphor changing blue light into white light causes stokes losses, which is usually around 60% to 80%. The efficiency of LED driver is usually around 70% to 90% [8]. For a 1W LED product, the typical heat from LED junction is 0.3-0.4W, heat from the phosphor is 0.1-0.2W, and heat from the driver is 0.1-0.2W. The total electrical input power of the chosen LED is 1W, which is calculated to have 0.13W heat from electronics, 0.54W heat from LED lamp as boundary conditions.

The model developed for FEM analysis have the same dimensions as the real retrofit lamp. The module is composed of the housing, LED package, substrate, LED driver, and metal feet. A detailed structure of driver electronic part was simplified in modeling. The temperature of the air of this simulation was set to 25°C, which is the same for thermocouple measurements. The model was cooled by nature convection, conduction, and surface-to-ambient radiation.

In the following paragraphs, examples were analyzed in detail for different cases as Fig 2.4 demonstrated (surface mounted devices on PCB substrate, surface mounted devices on PCB and aluminum substrate, chip on FR4 board, chip on ceramic board, and chip on aluminum heatsink). Case 1 and Case 2 are representative for SMD packages mentioned in Fig. 2.2a. Case 3 and Case 4 correspond to COB packages shown in Fig. 2.2b. Case 5 belongs to COH package illustrated in Fig. 2.2c. Heat distribution of cases with different packaging methods, as well as substrate materials were compared. One great advantage of thermal simulations is to compare different modules without actually building each.

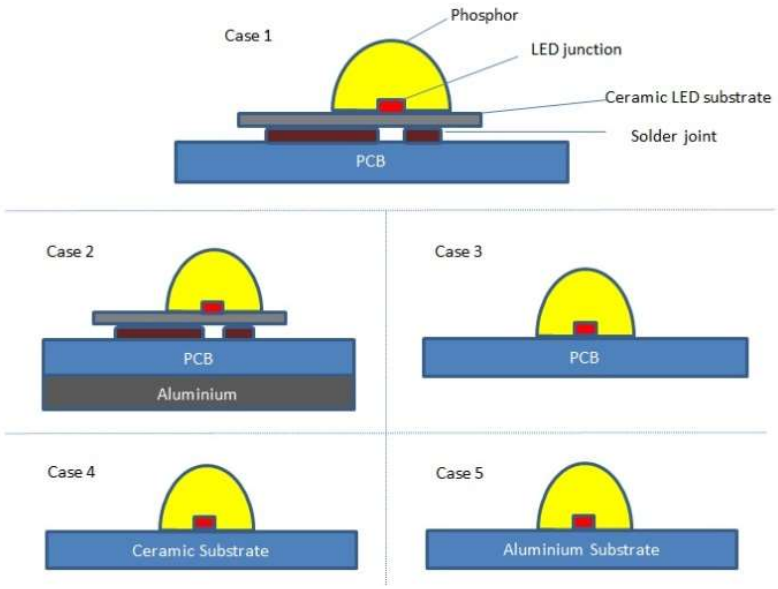


Fig. 2.4 Cross-section of study cases. In Case 1, LED package is surface mounted on PCB substrate. In Case 2, LED package is surface mounted on PCB and aluminum substrate. In Case 3, LED chip is directly mounted on PCB board. In Case 4, LED chip is directly mounted on ceramic board. In Case 5, LED chip is directly mounted on aluminum spreader.

2.4.1 Case 1. SMD High Power LED on an FR4 PCB

An existing LED G4 product was chosen as an example for SMD high power LED on an FR4 printed circuit board (PCB). This case is mainly investigated to calibrate the FEM model for case 2-5 analysis.

The following figure with a simplified geometry of the discussed model is given in Fig. 2.5. The PCB board is a round shape FR4 disc with copper covered on both sides. The surface mounted devices (SMD) LED is soldered to PCB by lead-free solder. Junction temperature has been reported to be directly related to optical performance, which usually refers to lumen output [14]. To evaluate the accuracy of the simulation, temperature measurements were done to calibrate the model. Since the chosen product is already a mature product in the market, housing temperature and solder temperature measured by thermocouple were used to calibrate the model. The experiments data and the simulated data were matched to adjust the existed G4 retrofit model, to improve simulation results on other derived models.

The results of both simulation and measurement showed that the junction temperature was around 85°C with no extra cooling parts. The solder joints reached about 73°C and PCB was about 60°C. The thermal resistance of the module is defined as the temperature difference of backside of the substrate (work as a heat spreader) and ambient temperature, divided by thermal input power. In this case, it was 46.3 K/W. It worth to mention here that usually thermal resistance of the package should be the temperature difference of junction temperature and ambient temperature. However, in actual cases, junction temperature is very difficult to measure, therefore, the temperature of the backside of substrate/heat spreader was chosen in this work.

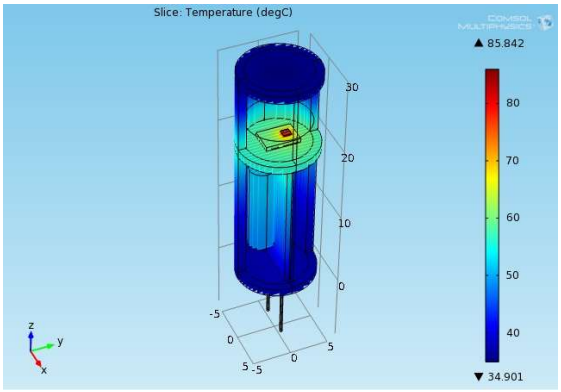


Fig. 2.5 Calculated surface temperature of a G4 LED product (with half housing).

2.4.2 Case 2. SMD High Power LED on an FR4 PCB and Aluminum Substrate

In this case, a 1mm thick aluminum substrate was pasted under FR4 by thermal glue. This substrate is designed to behave as the heat spreader to have heat spread better than Case 1.

Thermal resistance was 44.3K/W from LED to ambient based on the simulated model showed in Fig. 2.6. This design provided a possible design methodology for heat management for high power LEDs. By changing substrate composition, LED lamps enabled to have better thermal management properties.

However, it did not exhibit an obvious decrease in thermal resistance or junction temperature compared with Case 1. This is partly due to the thermal resistance introduced by surface mounted devices technology. As a result of that, other packaging methods will be studied and discussed.

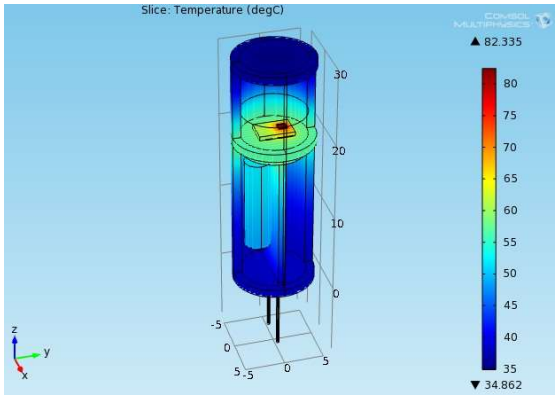


Fig. 2.6 Calculated surface temperature of Case 2 (with half housing).

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2.4.3 Case 3. COB High Power LED on an FR4 PCB

Since SMD LEDs usually have a certain internal resistance, it appears reasonable to glue the die directly onto a PCB, which is called chip-on-board (COB) technology. COB technology gives better thermal performance since the interconnection resistances decreased. To evaluate COB effect for the chosen LED, a model was simulated for thermal distribution.

In this case, LED dies with similar performance as case 1 investigated were glued by an adhesive resin. After that, wire bonding and encapsulation were done to protect the chip from mechanical or chemical damage. The thermal simulation (Fig. 2.7) showed that by choosing chip-on-board technology, the junction

temperature dropped more than 6 °C compared with case 1 and heat spread better by the FR4 substrate. The thermal resistance of the packaging from the junction to ambient was reduced to only 38.0 K/W.

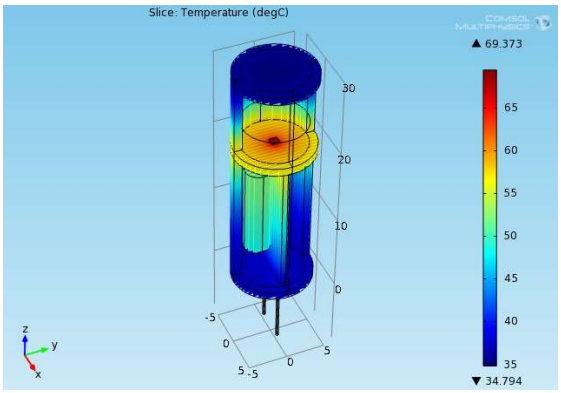

Fig. 2.7 Calculated surface temperature of Case 3 (with half housing)

2.4.4 Case 4. COB High Power LED on a ceramic PCB

In Case 4, FR4 PCB was replaced by ceramic (Al_2O_3) PCB. Using a ceramic substrate, the heat is spread by the substrate while on FR4 PCB the heat is spread by the copper layers. Choosing ceramic instead of FR4 could reduce the junction temperature even further (around 3 °C lower compared with Case 3), but the largest part of the thermal resistance is due to the limited surface area.

The thermal simulation of this case showed nicely the differences between FR4 and ceramic PCB. Using a ceramic PCB, the heat was spread by the substrate while on FR4 PCB heat was only spread by copper layers.

It is clear through the simulation results (Fig. 2.8) that heat is spread much more evenly compared with previous cases. The thermal resistance dropped to 36.5 K/W.

The thermal resistance from the LED junction to housing surface was decreased by chip on board technology. The decreased thermal resistance comes from the removal of the solder joint. With thermal paste, volume of air gap decreased between LED dies to substrate.

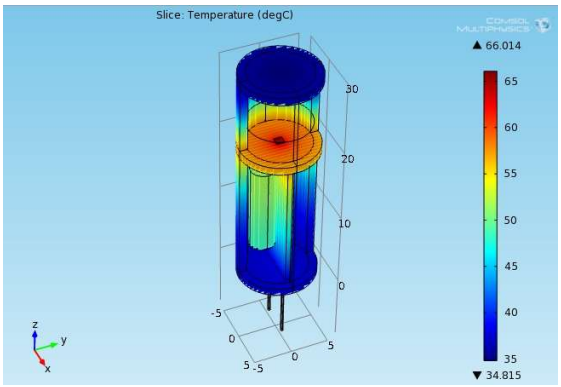

Fig. 2.8 Calculated surface temperature of Case 4 (with half housing)

With this packaging technology, it is possible to push the total power from 1W to 1.5 W, with junction temperature controlled under 85 °C (Fig. 2.9). It is estimated that the lumen output can increase to 100 lumen This indicates that different packaging technologies can lead to different lumen output.

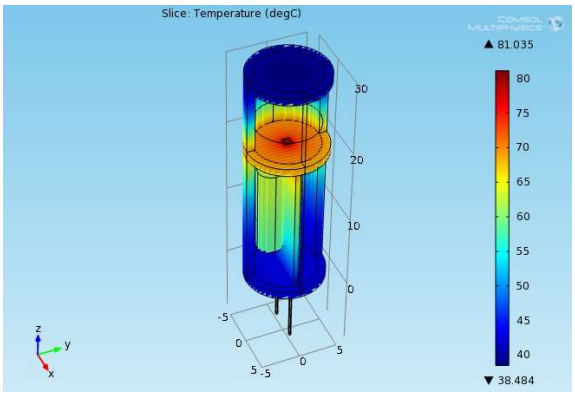

Fig. 2.9 Calculated surface temperature of Case 4 with 1.5W total electrical input power (with half housing)

2.4.5 Case 5. COH High Power LED on an Aluminum Substrate

When looking at the thermal conductivities of various materials, aluminum of 235W/mK appears to be a large thermal conductivity. To maximize the thermal performance gain, it is possible to glue LEDs on the metal substrate with no dielectric layer in between. To test such a package, a simulation was carried on based on the model developed in Case 1.

It is clear from the simulation results (Fig. 2.10) that the junction temperature further drops and the heat spread almost even from the LED junction to the edge of the substrate. Thermal resistance (junction to ambient) was only 33.9 K/W from the junction to temperature in this case.

With this design methodology, the total power was again pushed to 1.5W to simulate the junction temperature (Fig. 2.11). The junction temperature for a total power of 1.5W was around 72 °C. It indicates that even higher power can be applied under this design methodology.

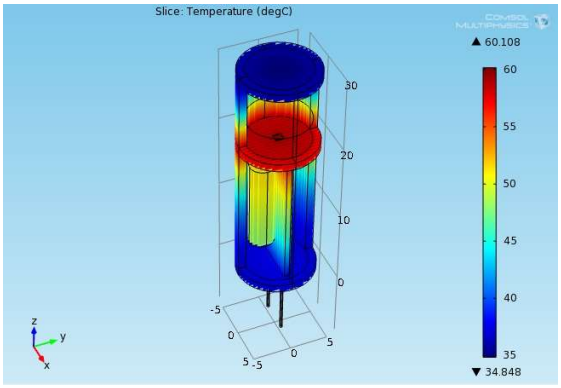

Fig. 2.10 Calculated surface temperature of Case 5 (with half housing)

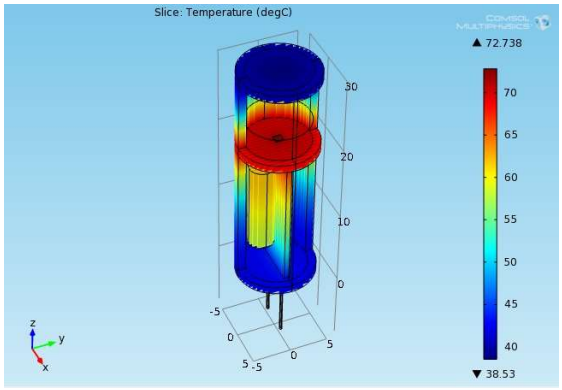

Fig. 2.11 Calculated surface temperature of Case 5 with 1.5W total electrical input power (with half housing)

It is worth to mention here that the heatsink can be further improved to decrease junction temperature. Since the original G4 LED product does not have any heatsink with fins, the model developed here also does not have the heatsink with fins either. It is well-demonstrated by many works that the fins of the heatsink can further improve heat management [12]. However, how to successfully attached the dies on heatsink without causing shortage circuit is still a vital challenge for manufacturers. Besides, the reliability of COB and COH technologies still cannot compete with SMD technology.

Comparing all the above cases, as mentioned in Fig. 2.12, LED chip on the aluminum heat sink (Case 5) has the best performance, regarding junction temperature and thermal resistance. It is worth to mention here that the substrate itself is not always the limiting factor by to spread temperature homogeneously over the whole substrate. To enlarge the substrate size is also a possible way to enhance heat dissipation.

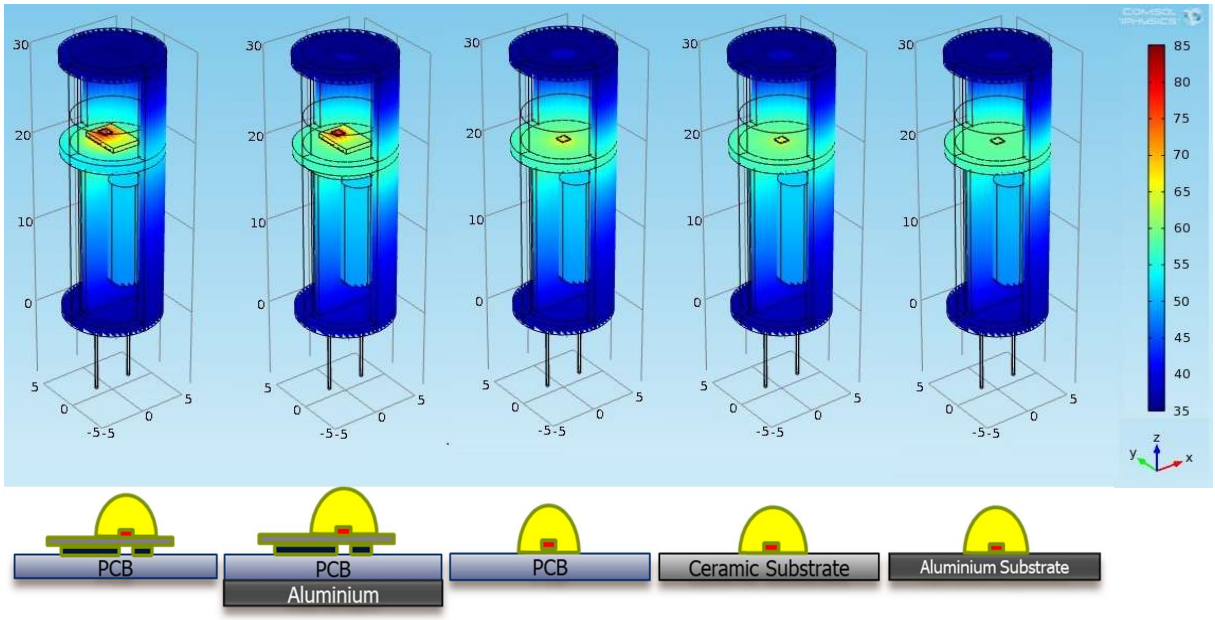

Fig. 2.12 Calculated surface temperature comparison of Case 1-5 (with half housing)

The cases above have shown the most common of the various possibilities of LED packaging technologies. Each of them has been optimized for its application. Based on the model developed in Case 1-5, the junction temperature and thermal resistance of different packaging methodologies were compared, as Fig. 2.13 shows below.

It is obvious that junction temperature increases with higher thermal resistance. Then how to reduce total thermal resistance becomes very important for designers. COH has the lowest thermal resistance and thus the lowest junction temperature compares to other cases. Compared with the original design of SMD, COH gives a decrease in junction temperature and a 50% decrease in total thermal resistance. It is also clear that the thermal resistance of COB and SMD with heatsink are lower than Case 1, which indicates that the design methodology gives better heat management properties than the current product on the market. However, SMD technology is still the most widely used technology by most manufacturers at this moment. COB and COH technologies still need to be further improved regarding cost and technology availability issues. It also worth to mention here that with a proper cooler design (e.g. active cooling) or choosing better packaging materials, the junction temperature still has the potential to drop further.

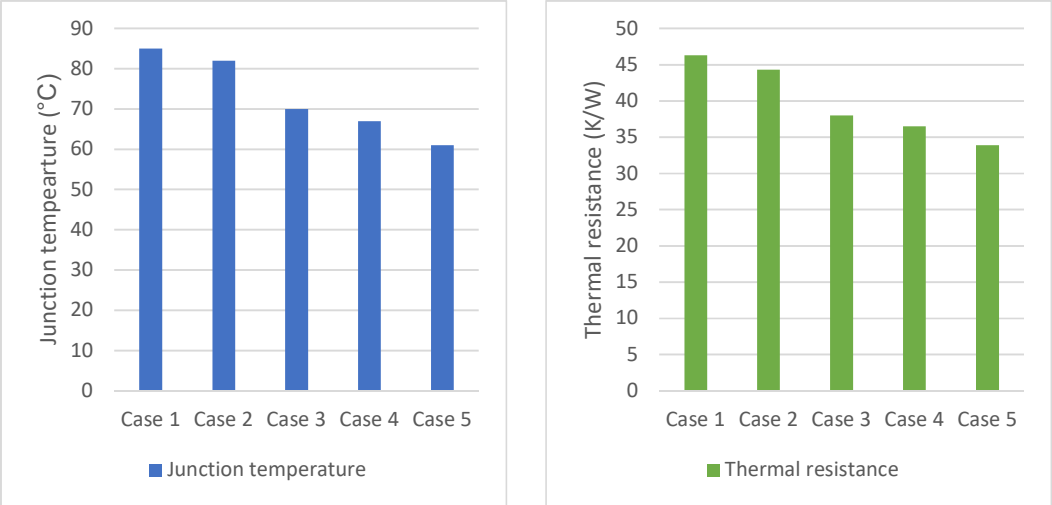

Fig 2.13 Comparison of Case 1 to Case 5 for junction temperature and thermal resistance.

For better understand the relationship between different packaging methods and thermal resistance, a theoretical analysis of total thermal resistance is carried below. Total thermal resistance of LED lamp of Case 1 can be written as:

$$\frac{1}{R_{th}} = \frac{1}{R_{j\text{-}h}} + \frac{1}{R_{d\text{-}h}} = \frac{1}{R_{j\text{-}sol} + R_{sol\text{-}sub} + R_{sub\text{-}h}} + \frac{1}{R_{d\text{-}h}}$$

where R_{th} is the total thermal resistance of the LED lamp, $R_{j\text{-}h}$ is the thermal resistance of junction to housing, $R_{d\text{-}h}$ is the thermal resistance of driver to housing. For Case 1, $R_{j\text{-}h}$ can be rewritten to the sum of thermal resistance from junction to solder joint, from solder joint to the substrate, and from the substrate to housing.

For chip on board technology (Case 3 and Case 4), thermal resistance can be simplified to:

$$\frac{1}{R_{th}} = \frac{1}{R_{j\text{-}sub} + R_{sub\text{-}h}} + \frac{1}{R_{d\text{-}h}}$$

where $R_{j\text{-}h}$ is regarded as thermal resistance of junction to substrate plus thermal resistance of substrate to housing.

For chip on heatsink technology (Case 5), thermal resistance would be written as:

$$\frac{1}{R_{th}} = \frac{1}{R_{j\text{-}hs} + R_{hs\text{-}h}} + \frac{1}{R_{d\text{-}h}}$$

where $R_{j\text{-}hs}$ is thermal resistance from junction to the heatsink, and $R_{hs\text{-}h}$ is thermal resistance from heatsink to housing.

Through theoretical analyse, it indicates that Case 5 would have the lowest value of total thermal resistance, which corresponds to the thermal resistance trend in Fig. 2.12 based on simulation. Case 5 COH also leads to cost reduction by the removal of thermal interface materials. However, Case 5 COH in practical suffered from low yield. The author believes that with further improvement of the LED die design together with the heatsink, the chip on heatsink yield can be further improved and widely applied in SSL applications in the coming future.

2.5 Conclusion

In this chapter, the thermal analysis of LED retrofit products based on different integration methods was conducted. One retrofit G4 LED product on market was chosen as a representative to analyze, focusing on Surface Mounted Devices (SMD), Chip on Board (COB), and Chip on Heatsink (COH) technologies. Both Simulation and measurement techniques were used to thermally characterize the LED product. The measurement of thermal behavior was used to calibrate the simulation models since the model was build up based on several simplifications. It has been demonstrated that integration technologies can enhance the thermal behavior, thus the performance of LED lamps. The best thermally designed LED retrofit lamp (Case 5 with COH technology) exhibited a 30% decrease in junction temperature (°C) compared with current product on the market and a 27% drop of the total thermal resistance, which is defined as temperature difference of back side of heat spreader and ambient temperature divided by thermal input power. Furthermore, it still has the potential to bring the junction temperature even lower by using more advanced heatsinks. The total power from LED with the chip on board or chip on heatsink technology can thereby be pushed from 1W to 1.5W or even higher within the limited volume.

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Chapter 3 Driver Integration for Miniaturized Solid State Lighting Applications

After thermal analysis of different packaging methods of LED dies, it worth to take a closer look into the driver electronics to power up the LED dies. LEDs are constant voltage loads with low equivalent series resistance. Most of the LEDs are powered by DC source. For general lighting, it becomes essential to convert AC main supply voltage to regulated DC voltage using rectifiers and filters. Based on the topology of the connected LEDs i.e. series or parallel, a constant voltage regulated driver or current regulated driver is used in [1]. Especially for G4 retrofit LED, the driver system is analyzed in detail. Different modes of driver control are introduced in this chapter, with both advantages and disadvantages analysis.

After driver topology investigation, the question then comes to how to minimize the system volume with these necessary components. For system miniaturization, it is preferred to have a complete SSL G4 retrofit system with all electronic components integrated on a single wafer with both the electrical power conversion block and optical blocks consisting of LEDs. The process integration of the electronics and passive components by monolithically or wafer level integration can significantly bring down the initial cost of the SSL system. Since SSL is based on semiconductor technology, it can be integrated with standard CMOS process to create a complete multifunctional miniaturized module.

However, due to current technology limitation, silicon integrated capacitor fabricated in-house cannot meet the requirement of the system. Therefore, selection methodology was carried on for on-chip and off-chip components. For low voltage applications, silicon as substrate material offers a great potential for monolithic integration of rectifiers and drivers. But passive components such as capacitors, inductors and high watt resistors provide huge challenges to be integrated on-chip. These components have to be off-chip components in this work.

3.1 G4 Retrofit LED Driver Analysis

A breakout of the G4 capsule is shown in Fig. 3.1 [3]. The PCB consists of discrete components such as diodes, electrolytic capacitor and driver IC. The research focus of the thesis project is to build an integrated rectifier and driver on-chip to reduce system cost and PCB space.

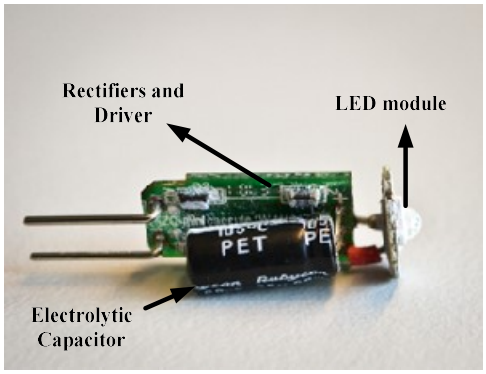

Fig. 3.1 G4 LED Capsule excluding housing

The G4 LED capsule is a 2.5W luminaire which can provide an output of 100 lumen. The input voltage requirement of G4 LED capsule is 12V AC. The G4 module uses a single LED for light output. Considering this specification for a low power LED system, the basic block diagram of this system is shown in Fig. 3.2. The input 12V AC is first converted into DC by a bridge rectifier. The bridge rectifier uses Schottky diodes due to their low forward voltage drop and high current conduction.

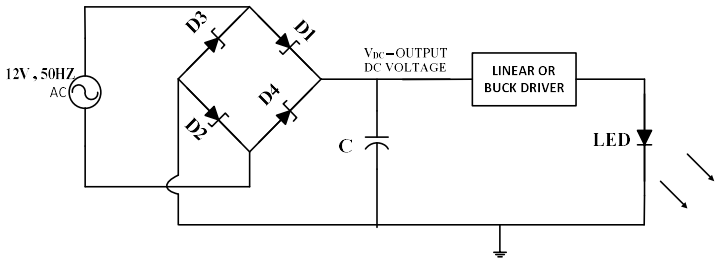

Fig. 3.2 Schematic of a low power 12V LED system

There are two methods to maintain constant current in LED driver systems: a linear driver or a switch mode driver.

3.1.1 Linear Driver

The linear current driver is cost-effective but usually suffers poor efficiency [4], therefore lead to thermal management problems. A basic circuit for a linear constant current driver for LED is shown in Fig. 3.3 and Fig. 3.4 [5].

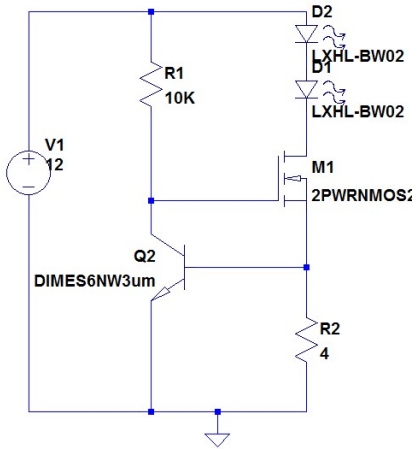

Fig. 3.3 Linear driver circuit example

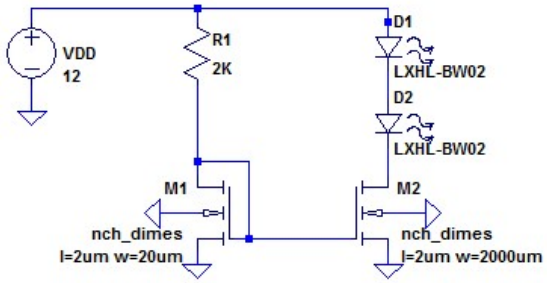

Fig. 3.4 Current mirror linear driver

The current in the circuit in Fig. 3.3 is set by the resistor R2. The NMOS is on when the voltage at R1 is greater than the threshold voltage of the NMOS. The transistor Q2 turns on with base-emitter voltage Vbe of the transistor set by the voltage drop across R2 that should be less than 600mV. The transistor Q2 turns on it pulls down the voltage at the gate of the NMOS causing the MOSFET to go into the linear region and limits the current in the circuit. In the Fig. 3.4, the circuit for the linear driver is a constant current mirror of NMOS devices. The current through the LEDs is set by the resistor R1. The current in the LED branch is set by the ratios of the width of the NMOS M1 and M2.

Based on the requirement of miniaturization, the linear driver is investigated in this work because it can use a current mirror to make the driver inductor free. The Schottky diode, NMOS and resistors are able to integrate on silicon wafer based on in-house design knowledge. The components can then be fabricated all in BiCMOS process to achieve a fully integrated driver.

3.1.2 Switch Mode Driver

In a switch mode regulator configuration, the switch basically MOSFETs takes a small portion of energy for a given time from the input voltage source and transfers it to the driven load [6]. The switch mode driver is more efficient in power conversion than linear drivers. One of the simplest switching LED drivers is the buck converter. The buck converter is well-known as a step-down converter where the load voltage is lower than the supply voltage, as shown in Fig. 3.5 [7]. The inductor in such design is essential since it not only stores energy but also acts as a low-pass filter to control the current in the LEDs. It worth to mention that the higher the inductance value is, the lower the current ripple is. However, for too high inductor value it may lead to problems that the current does not fall enough to the control IC. Therefore, how to select the inductor value is important for such a design.

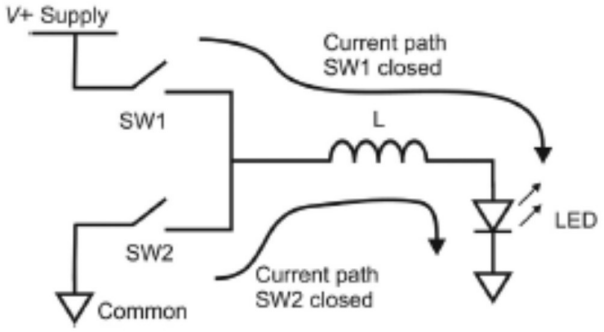

Fig. 3.5 Basic Buck LED Driver [7]

The switch mode driver can achieve higher efficiency when compared to the linear driver. A buck driver is a step-down DC converter. This driver configuration is used if the output load voltage is less than the input voltage. The buck driver requires inductor and capacitor components for energy storage. In Fig. 3.6, it gives an example of a switch mode driver with Schottky diodes to drive LEDs. With such configuration, it also can be easily extended to smart sensors connections.

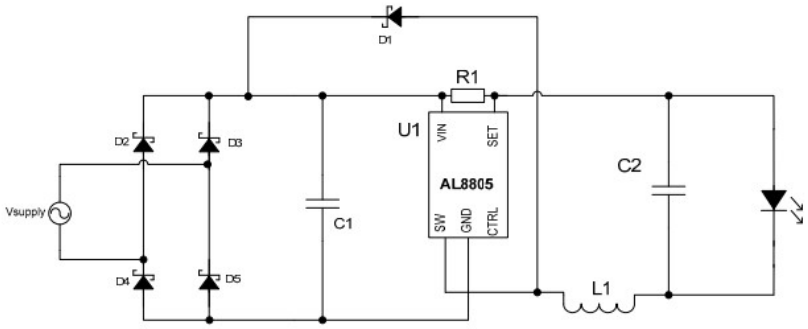

Fig. 3.6 Switch mode Buck Driver with rectifiers using Schottky diodes.

In this circuit design, an inductor is necessary. Therefore, the total size of the driver electronics cannot be as small as the linear driver mentioned before. Based on in-house knowledge, inductors are difficult to integrate on the same wafer with Schottky diode. Therefore, heterogeneous integration is needed for this driver topology.

3.2 Design Methodology for Driver Integration

Based on the two driver topology discussed above, it is then necessary to decide which components can be monolithically integrated, and which components should be left off-chip.

3.2.1 On-chip Components

Wafer level packaging offers the advantage of the reduction in the total cost of the LED system. Since designing an SSL system is similar to designing a microelectronic system, for an in-depth design analysis, it becomes essential to know the concepts from device processing to circuit analysis and packaging and integration for the system development.

In order to guarantee the light output quality (e.g. no flicker), it is necessary to generate the spice model of the in-house fabricated on-chip components. Take an example of a Schottky diode, an analytical model in the in-house standard BiCMOS process should be first established. Such a model is essential for process understanding and layout design for achieving the required high current conduction and high breakdown voltage for G4 retrofit applications. In the next step, this analytical model is verified by simulations using TCAD software TSUPREM4 and MEDICI. This provides guidance for simulating the process and device models that allow us to predict the process parameters that would be required during fabrication of the devices in EKL cleanroom 100. The next step is the electrical characterization of the Schottky diodes. The measurements are done using cascade probe station with ICCAP software. A spice model is then extracted from the measurement data for circuit analysis. In the same measurement procedure, characterization of BJT and NMOS devices of the various wafers are done to extract the spice parameters.

Using the spice models extracted from the software, electrical circuit analysis is done for the basic linear and buck driver circuits. This design step allows us to check at each step to optimize the design for future process. Firstly, an Analytical model for Schottky diodes was set for devices fabricated in the standard BiCMOS process, for achieving high current and high breakdown voltage. Secondly, a set of design parameters can be extracted from the model of Schottky diodes. Moreover, NPN bipolar transistors and MOS devices were also analyzed at the same time to provide a complete methodology for electrical characterization and modeling. Therefore, a design for integrated driver circuit on silicon substrate is set analyzed, and characterized.

A robust process and device modeling of the devices intended for integration on chip must be done. The devices are then fabricated and characterized. With the device models extracted from the measurement data, circuit analysis is done for integrating higher level circuits. The design concepts will be tested for reliability and optimized in the next development cycle when the system electrical connections are finished. In the following table, on-chip components investigated in this work are listed. The selection criteria is mainly based on whether the technology knowhow in house is sufficient enough to support the design, fabrication, characterization, and spice model distraction.

Table 3.1 On chip components characteristics

Component
Schottky diodes
Temperature sensor
Light sensor
NMOS
Resistors

3.2.2 Off-chip Components

Off-chip components in this work are IC chips provided by the supplier, capacitors, resistors, inductors, etc. The power converters and driver electrical circuit for the LED require large storage capacitors. These are used as discrete components on PCB. The electrolytic capacitors are mainly used as the storage capacitors. They are bulky and occupy a lot of space. It is considered as off-chip components in this work since it is a challenge with the lab infrastructure to create capacitors based on a silicon substrate with the desired capacitance and breakdown voltage.

The characteristics of the components applied in this SSL system are listed in the following table. The components are either too challenge for wafer level integration based on current lab situation, or with better performance than the in-house fabricated devices. For instance, a trenched capacitor based on wafer level process was explored and fabricated. However, due to the equipment limitation, it is not possible to guarantee the yield. Also, the size of in-house device is even bigger than the off-chip components in the market. Therefore, the capacitor was decided to be an off-chip component.

Table 3.2 Off chip components characteristics

Component	Supplier	Characteristics
High-efficiency Buck LED driver	Diodes	AL8805, 30V, 1A
Capacitor	Panasonic	150uF, Aluminum Electrolytic Capacitors, 50V, 6.3x11.2mm2
Inductor	Wurth Electronik	39uH, 1kHz/250mV
Rectifier (As a comparison for Schottky diodes fabricated by BiCMOS process)	Taiwan Semiconductor	SS14M, 40V Breakdown voltage
Temperature sensor (As comparison for Schottky diodes fabricated by BiCMOS process	Texas Instruments	LMT70, Power supply 2.0-5.5V
Resistor	Panasonic	Anti-surge thick film chip Resistors, 0805, 20 ohms, 500mW
Capacitor	Vishay	Aluminum Capacitors, 220uF, 6.5x18mm2
LED die	CREE	TR5050, 0.5x0.5mm2, 5V, 230mA
SMD LED	Sharp	GM2BB30BM0C, 300mA, 5V

3.3 Conclusion

In this chapter, we first analyzed a representative G4 LED driver circuit. Based on this, two modes of the driver were selected: linear driver and switch mode driver. The linear driver can be inductor free, thus fit in to the desired small form factor. However, linear drivers usually suffered by low efficiency. Moreover, it is a challenge to integrate smart sensor control systems into linear driver without introducing inductors. Switch mode driver needs inductors, but it is more energy efficient, and easier to add smart sensor control with the help of the control IC.

Components mentioned in these two modes of the LED driver were then analyzed for system integration. Off-chip components and on-chip components were first selected based on criteria such as thermal management, the yield of production, and technology in-house. In this driver integration for miniaturized SSL smart lighting applications, the on-chip components include monolithically integrated rectifiers, drivers related components (e.g. small resistors, transistors), and sensors. The off-chip components include capacitors, inductors, and control IC chips. How to fabricate these on-chip components and how to arrange these off-chip components to fit in the small form factor is then a challenge that will be addressed in the following chapter.

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Chapter 4 Monolithic Wafer Level Integration

It has been demonstrated in Chapter 2 that advanced packaging technologies can greatly reduce total thermal resistance, thus improve the performance of LED lamps. Advanced miniaturized and multifunctional packages are one of the critical challenges for not only SSL systems but in general the whole semiconductor industry. In the semiconductor packaging industry, wafer level packaging (WLP) is one of the fastest growing research direction, with offering small form factor and low packaging cost. As mentioned in Chapter 1, solid state lighting (SSL) is on track to replace traditional lighting sources. However, the cost is still a key issue for the market [1]. Therefore, creative packaging solutions are necessary to bring the costs down. Wafer level packaging is one of the main trends for cost reduction. The main advantage of wafer level packaging (WLP) is the possibility to package many LED chips on a wafer, not every chip individually. Cost reduction using WLP can be up to 30%. [2,3] The packaging cost per wafer in WLP can become more cost-effective when decreasing die size or increasing wafer size. [1]

There are mainly two WLP packaging concepts, namely system on chip (SOC) and system in a package (SIP). In SOC technology, all necessary electronic components are placed on a single integrated circuit (IC). For instance, monolithic integration of the power circuitry of rectifiers, passive components and sensors is a significant challenge to reduce system space and create smaller products. SIP integration, on the other hand, allows chips or other components from different suppliers to be combined into highly functional products in their own respective technology flows. [2] Heterogeneous wafer level system integration and packaging is a key driving technology for the multifunctional system in a package (SiP) microelectronic systems for reducing cost, size and improving performance. The main aspect of the system in a package technology is to combine semiconductor technology with other technologies in an electronic packaging dimension. This includes integration of heterogeneous functions like electrical, optical, mechanical to create high value single miniaturized system package at low cost [3].

Driven by the demand for higher power density devices, numerous technology is rapidly evolved in the electronics market. In Ricky Lee's work [4], a WLP solution with LED chip mounting on a silicon sub-mount wafer was presented, in order to deliver a silicon-based manufacturing solution which is low-cost, fast throughput and high yield. Furthermore, electronics integration based on WLP have been emerging to expand the technology into System-in-Package (SiP) applications. In In-Soo Kang's work [5], a wafer level embedded system in a package was developed to optimize structure and materials.

For miniaturized LED applications, electronic components included need to fulfill more critical requirements such as limited volume, high working temperature, high sensitivity, etc. Since the SSL system is essentially a microelectronic system with semiconductor components like diodes, SOC strategy was chosen for system space reduction. A silicon platform was then selected which brings in wafer level integration. Silicon wafer level packaging for LED offers great advantages for integrating both optical function and electrical function on the same substrate, with the benefits of space and cost reduction. The main challenge using silicon as the substrate material for integration is that the breakdown voltage for silicon is less than 100V [2,6]. Hence, silicon as substrate material cannot be used for the high power lighting application. Since G4 retrofit systems are usually aiming at low voltages such as 12V, therefore silicon-based substrate was chosen in this work.

To start with, we focus on the rectifier composed of four Schottky diodes, since they are usually at a high temperature in G4 LED driver systems when just lighting up, as mentioned in Chapter 1. For better control of the electrical efficiency, a robust spice model of Schottky diode was extracted from the measurement data using the ICCAP tool. Based on this model, two types of driver IC can be tested to drive LEDs. Capacitors were then investigated for heterogeneous integration, since it is one of the most essential components in G4 LED driver system. Flexible connections were developed for capacitor self-align integration, however, the contact resistance is too high compared with traditional wire bonding connection. Therefore, this capacitor integration will not be further addressed in this work.

Furthermore, smart sensors were investigated. The priority goes first to the temperature sensor, since it directly links to the lifetime of retrofit G4. It is well-known that a relatively high operating temperature may adversely affect the lumen output. The relatively high operating temperature may increase the rate of light output degradation experienced by LEDs, which may shorten the lifetime, decrease and degrade the light output. Accordingly, there is a need for monitoring the operating temperature of SSL applications, especially miniaturized LED lamps such as G4 LEDs, for reliability considerations. [7]

Besides temperature sensors, other smart sensors are also drawing widely interests in general lighting applications, such as light sensors and presence sensors. Lighting systems based on LED luminaires can be easily and flexibly controlled. Daylight lighting control can realize energy-efficient systems, by producing illumination in accordance with daylight conditions. [8] Presence sensors are also helpful for energy saving, by switches off the light automatically when no movement is detected. By combining light sensors and presence sensors, light control can be easily realized, especially in consuming lighting. It worth to mention, that presence sensor using mmW technology was developed by the author using Kapton film for cost reduction. However, due to the transmission line, the total size of the presence sensor does not fit into the scope of this work due to the size limitation. Therefore, in this chapter, only the work for temperature sensing and light sensing will be illustrated in detail.

4.1 Monolithic Integrated Rectifier

Conventional Schottky diodes and junction barrier power Schottky diode are fabricated as a vertical structure with top anode contact and bottom cathode contact. These are the generally packaged diodes available as commercial off the shelf components. The disadvantage of such power Schottky diodes having vertical structure is that it cannot be integrated monolithically with other integrated circuit components in a standard BiCMOS process. In this work, the requirement of a Schottky diode with a breakdown voltage of 40V is desired. The Schottky diodes fabricated in standard CMOS process forms the fundamental component of integrated low voltage full wave bridge rectifier circuit for powering the driver and LED.

4.1.1 Design and Fabrication

In the fabrication of planar Schottky diodes in a standard BiCMOS process, the choice of metal for the Schottky contact is limited. In this process, aluminum is the metal used for the Schottky contact. In the planar process, the Schottky metal is in contact with moderately doped n-type layer obtained by N-Well diffusion process. The anode contact of the Schottky diode is made with the n-well region, and the cathode ohmic contact is with a heavily doped n+ layer [9, 10]. A cross-section of the planar Schottky diode is shown in Fig 4.1.

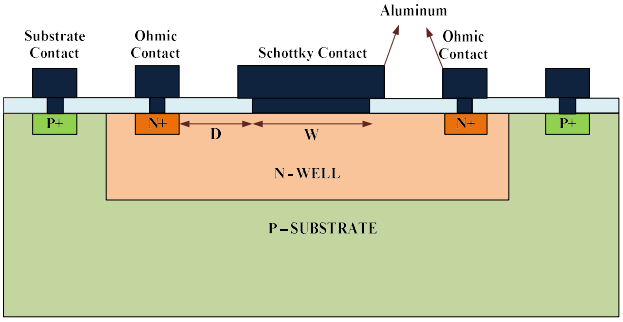


Fig. 4.1 Cross section of Planar Schottky Diode device

The Schottky contact area shown in Fig 4.1 is given as (W x L) where width W is the width of the Schottky diode and L is the length of the Schottky diode. The distance between the Schottky contact and ohmic contact is defined with D. The drift region, in this case, is the lightly doped N-Well region. The current conduction in planar Schottky diode is in the lateral direction from anode Schottky contact to the cathode ohmic contact. When the anode terminal of the Schottky diode is forward biased by applying a negative bias voltage, the electrons cross over the Schottky barrier by thermionic emission move towards the cathode ohmic contact through the n-well region. The current under forward bias is given by the general Schottky diode current equation as [11],

$$I = AA^{*}T^{2}\mathrm{e}^{-(q\phi_{bn}/kT)}[\mathrm{e}^{(qV_a/kT)} - 1] \tag{4.1}$$

where :

A = Schottky contact area defined by (W x L)

The total specific series on-resistance R_{ON} modeled by resistor components for the planar Schottky diode is shown in Fig 4.2 [12]. It is given as,

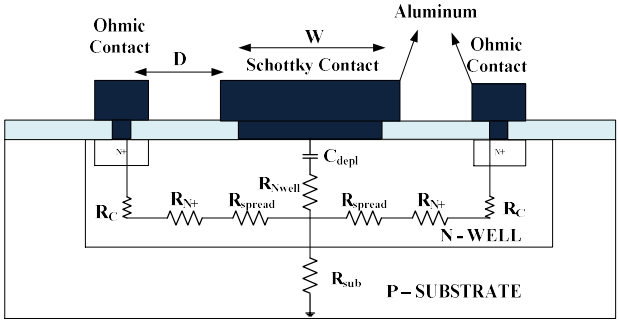


Fig. 4.2 Components of series resistance in Planar Schottky Diode

$$R_{ON}=R_{nwell}+R_{Spread}+R_{N+}+R_C \tag{4.2}$$

$$=\frac{1}{WL}\rho_{nwell}T_{nwell}+\frac{1}{3}\frac{W}{4}\frac{1}{L}\rho_{nwell}T_{nwell}+\frac{1}{2}\frac{D}{L}\frac{\rho_{n+}}{T_{n+}}+\frac{1}{2L}\sqrt{\rho_C\frac{\rho_{n+}}{T_{n+}}}$$

where: W = Width of the Schottky contact, L = Length of the Schottky contact, ρ_{nwell} = resistivity of n-well layer, T_{nwell} = Thickness of un-depleted N-well layer, D = Separation between Schottky contact and ohmic contact, L = Length of the Schottky contact, ρ_{n+} = resistivity of n+ layer, T_{n+} = Thickness of n+ layer, ρ_C = specific contact resistivity.

The resistance components in Eq. 4.2 is discussed and analyzed. R_{nwell} is the n-well resistance. This resistance is taken at 0V bias since the n-well will be un-depleted and the resistance at this bias maximum. R_{Spread} is the spreading resistance defined as the resistance due to the current spreading under and around the anode metal contact of the Schottky diode. These resistances are inversely proportional to length L of the Schottky diode. These resistances can be minimized by increasing the length L of the Schottky diode and keeping the width W as small as possible. The resistivity of n-well is inversely proportional to doping concentration. A higher doping concentration and a thinner n-well layer defined in the process can also contribute to reduce these resistances.

R_{N+} is defined as the resistance in the current path due to the distance between the ohmic contact and the Schottky contact. The reduction of R_{N+} can be achieved by decreasing the separation between the Schottky contact D to as minimum as possible. This is layout dependent parameter limited by the lithography limit of the process. R_C is the contact resistance due to the ohmic contact. The specific contact resistivity of Al /Si ohmic contacts [10] is in the range of $10^{-6}\ \Omega cm^2$. Hence, the R_C can be reduced by increasing L.

From the above analysis of series resistance components, it is clear that the total series specific on resistance R_{ON} can be reduced by increasing the length of the Schottky contact L and decreasing the Schottky width W with same diode area (long diode instead of a square diode). This would provide us a lower on-state voltage drop V_F for the Schottky diode under forward bias condition.

In the Schottky diode current equation Eq. 4.1, the forward current conduction of Schottky diode is directly proportional to the Schottky contact area A. For higher current conduction, the Schottky contact area must be increased without increasing the series resistance. From the analysis of series resistance, it is evident that if we increase the area we need to design Schottky diodes having long contacts and shorter width. The method for increasing Schottky contact area keeping series resistance minimum is by designing the layout of the Schottky and ohmic contacts in a finger structure [11]. The finger structure of Schottky and ohmic contacts are placed alternately to each other as shown in Fig. 4.3. With finger configuration of the layout the minimum distance between the Schottky and ohmic contact will be the same. The Schottky contact area can be increased by increasing the length of the Schottky contact and the number of fingers. The total resistance in the finger design structure is the parallel combination of the total specific on resistance R_{ON}. This further reduces the series resistance of the device and increases the diode current conduction.

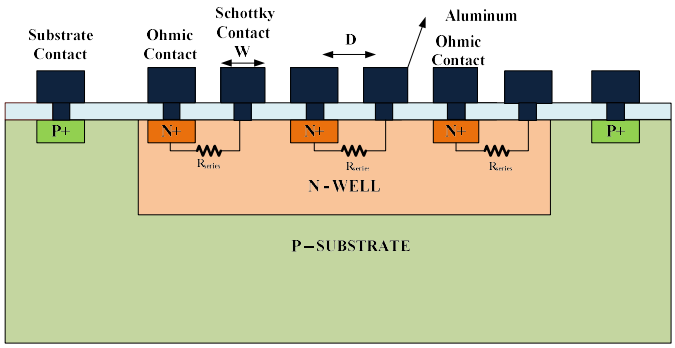


Fig. 4.3 Planar finger structure Schottky diode device cross section

The factor that also affects the breakdown voltage of the planar Schottky diode is the doping concentration of the n-well. In planar Schottky diodes, the drift layer is described by the n-well layer. It is governed by the same equation as described before for the vertical Schottky diodes. It is given by [9],

$$BV_{Si} = 5.34\text{x}10^{12} N_D^{-3/4} \qquad (4.3)$$

where :

N_D = Doping concentration of n-well layer

A graph of the above relation obtained using Matlab is shown in Fig. 4.4. From this graph, it is evident that for Si Schottky diodes the n-well doping concentration of about 5 x 10^{15} - 10^{17} cm^{-3}, the breakdown obtained will be in the range of 10 – 100V.

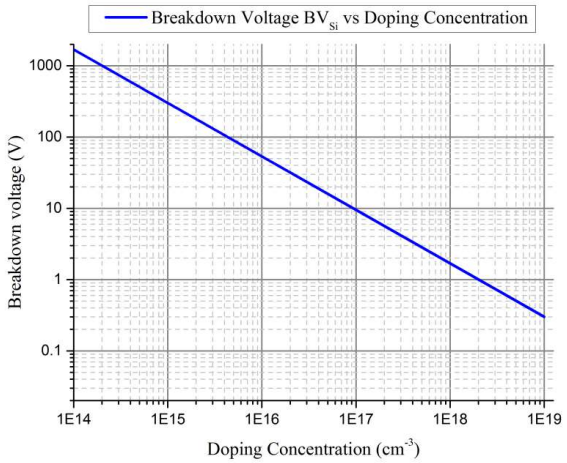


Fig. 4.4 Breakdown voltage v/s Doping concentrations for Si Schottky diode

Two commonly used methods for enhancing breakdown voltage are discussed below: layout modification and P+Guard rings.

(A) Layout modification:

The Schottky junctions are usually made by using the rectangular window in the contact opening mask. Metal is then deposited and patterned on these openings to form the Schottky junction. The depletion region formed expands laterally under the oxide in the reverse bias condition. In the rectangular finger mask layout design shown in Fig. 4.5. In this layout, a cylindrical junction is formed at the finger edges and a spherical junction formed at the corner of these fingers. There is a large increase in the electric field due to the presence of sharp corners and formation of the spherical junction in the layout. The breakdown voltage at these junctions is lower than the edges of the finger. The analysis of both the cylindrical and spherical junction has shown that the cylindrical junction has a lower breakdown voltage than spherical junction [11]. The decrease of breakdown due to the edges can be eliminated by using a curved mask layout at the contact openings without edges. This design will reduce the large electric field build up at the spherical junction formed at the edges of the finger layout design [8]. An example design is shown in Fig. 4.6.

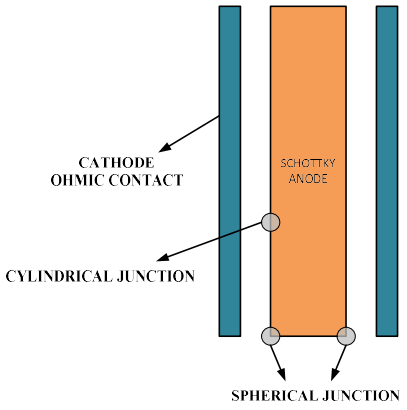


Fig. 4.5 Layout rectangular masks

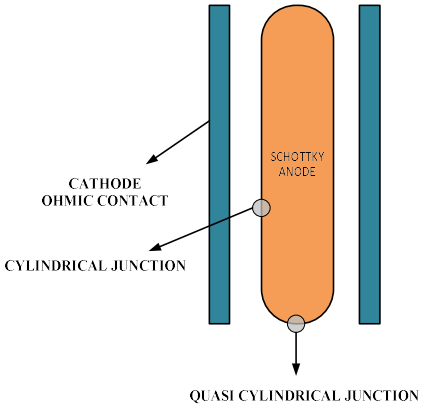


Fig. 4.6 Layout cylindrical masks

(B) P+ Guard rings

The most commonly used method for increasing the breakdown voltage is the incorporation of p+ guard rings in the Schottky edge interface. The guard rings will overlap the edges of the Schottky anode contact and reduce the large build-up of the electric fields. This is a similar technique that is discussed earlier in vertical Junction Barrier Schottky diodes. The guard rings create a p-n junction in parallel with the Schottky diode. The on state voltage drop is determined by the Schottky contact and the breakdown is determined by the presence of PN junction as the Schottky junction breakdown at a lower voltage [9]. The P+ guard ring for the Schottky diodes can be made using the same process mask as that of the PMOS and PNP bipolar transistor so there is no additional mask cost. The design of a p+ guard rings around the Schottky junction is shown in Fig. 4.7. A combination of cylindrical mask termination and guard ring is used to design a Schottky diode in this process to reduce the electric field and enhance the breakdown voltage.

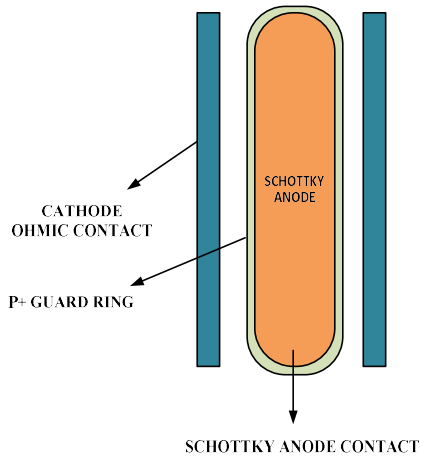


Fig. 4.7 Layout P+Guard rings

After discussing the factors affecting forward conduction and breakdown of Schottky diodes in the standard BiCMOS process, we deduce the design parameters required for the fabrication of Schottky diodes related to process technology and layout considerations.

1. Process technology design parameters:
    a) The main process technology parameter that affects both the forward voltage drop and breakdown voltage is the doping concentration and thickness of the n-well region. From the analytical analysis, a breakdown voltage in the range of 10-100V n-well doping concentration needs to be in a proper range.
    b) The next consideration is barrier metal used for the Schottky junction. The barrier metal in the DIMES BiCMOS process used is aluminum.
    c) The Schottky diodes and the Schottky barrier height are very sensitive to silicon surface in contact. This quality of the Schottky contact depends on the pre-metallization process step. The native oxide residues on the surface of the Schottky contact before the deposition of Al/1%Si can increase the Schottky barrier height. In standard IC step, an HF dip is done before the metallization process to remove the native oxide and surface passivation. A good control of this step can result in a good metal-silicon interface before the deposition of Al/1%Si [10].

2. Layout design parameters :
    a) A finger design structure of cathode and anode layout is preferred than a square cathode layout design as this reduces the series resistance. The distance between Schottky contact and ohmic contact must be placed as close as possible. A good variation in these distances must be chosen, keeping in mind that the Schottky contact which is too close to the ohmic contact will have a lower breakdown due to the high electric field at the edges. To have a large area diode alternate finger structure layout of Schottky (anode) and ohmic (contacts) can be made instead of a large width of the Schottky contact.
    b) A curved layout at the edges of the Schottky metal contact should be used to eliminate the effects of spherical junction formation and high electric field at the edges.
    c) A p+ guard ring surrounding the Schottky metal contacts must be defined to reduce the reverse saturation current and increase the breakdown voltage.

Using the above guidelines for designing the Schottky diodes a variety of Schottky diodes structure can be made and measured. Based on such design parameters, the process starts with a p-type low resistivity wafer. A monolithically integrated rectifier composed of four Schottky diodes were processed using an in-house 7 mask level BiCMOS process (BiCMOS7), as shown below in Table 4.1. The fabricated chip in this process with rectifiers using Schottky diode is shown in Fig. 4.8.

Tabel 4.1 BiCMOS Processing steps

Mask no.	Step title	BiCMOS Processing step
	Start substrate	p-type processing wafer with 3µm Epi implantation
1	NW: N-well	n-type area
	N-well drive in	Annealing step at 1150˚C with 8 hrs for deeper n-well
2	SN: Shallow N	n-type source-drain for the NMOS transistor and cathode ohmic contact for Schottky diode
3	SP: Shallow P	p-type for source and drain for PMOS transistor, guard ring and substrate contact for Schottky diodes
	Vt adjust	Threshold voltage adjust by implanting boron into channel regions
4	CO: Contact	Contact openings
5	M1: Metal 1	Interconnect and gate material formation
6	Via	
7	M2: Metal 2	

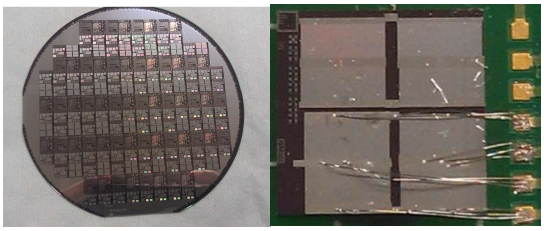


Fig. 4.8 Rectifier wafer and diced rectifier chip (3 by 3 mm) with BiCMOS7 process.

The full wave rectifier configuration as per the circuit configuration was integrated as above design in Fig. 4.9. In order to check if the modeled Schottky diode with parallel finger configuration is suitable diode for the rectifier circuit, the diode model parameters were extracted from the IV characteristics. This was done by detailed IV characteristic simulation of the parallel finger Schottky diode at different temperatures ranging from 20°C to 100°C. The parameter extraction model was used to build a model of the Schottky device. The next step to simulate this was to obtain the model parameters from the Schottky diode simulated. Important parameters were reverse saturation current (Is) and breakdown voltage. Which served as input parameters for the electric circuit simulation in the AC/DC module of the circuit simulation in COMSOL. The spice circuit was then simulated for the diode parameters obtained from the simulated Schottky diode in full wave rectifier configuration and the output was obtained as shown in Fig. 4.9. The output DC voltage is used to power the driver circuit components and the LED module.

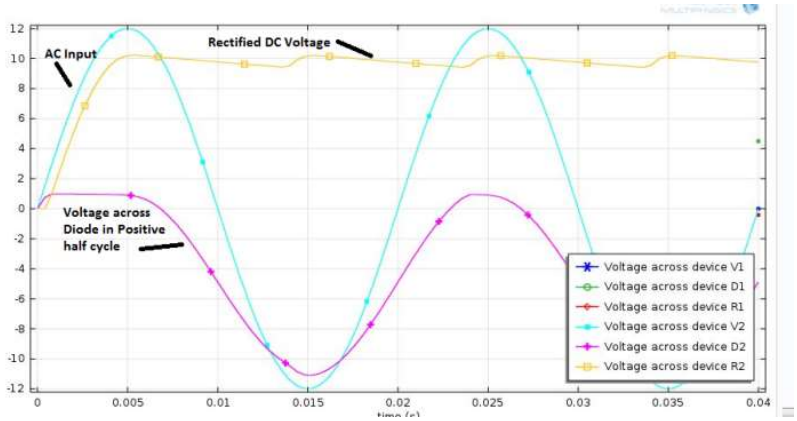


Fig. 4.9 AC simulation of Full wave rectifier with Schottky diode.

4.1.2 Test and Characterization

The measurement for the low current Schottky diodes is done by choosing three wafers having different NW dose. The wafers chosen are with phosphorus implant dose of 3 x 10^{12} cm^{-3}, 6 x 10^{12} $cm^{-3}$and 9 x 10^{12} cm^{-3} (3e12,6e12,and 9e12, respectively). In each wafer the Schottky length is fixed as L = 250 µm. In the structures, the width (W) of the Schottky contact and the distance (D) between the Schottky and ohmic contact are varied. The different layout structure fabricated in the process are Schottky contacts with a rectangular mask, Schottky contact with cylindrical mask and Schottky contact with cylindrical mask and guard rings. An example mask layout is shown in Fig. 4.10.

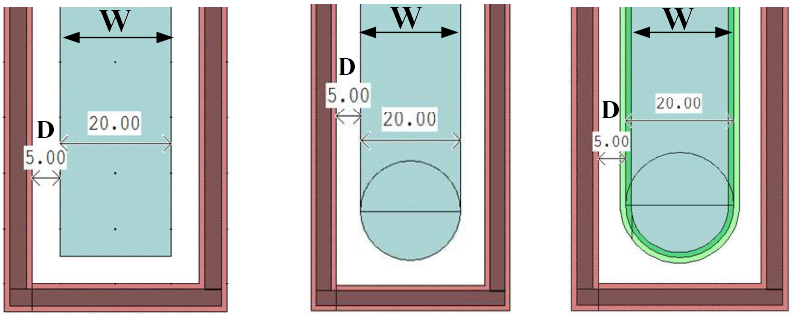


Fig. 4.10 Schottky diode structures for measurements rectangular, cylindrical and cylindrical with guard rings (from left to right)

For the low current Schottky diodes, 5 samples in each wafer for the various structures are measured. The following points can be deduced from the measurement data of IV characteristics. The parameters that mainly influence the forward current are the N-Well doping concentration, the Schottky contact width (W) and the distance between Schottky contact and ohmic contact D. With higher doping concentration; the current conduction is high at low forward bias as shown in Fig. 4.11 considering the example of a Schottky diode with W = 20µm and D = 5µm. The average V_F at I_F = 100mA for n-well 3e12 is 1.1V, for 6e12 it is 1V and for 9e12 it is 0.96V.

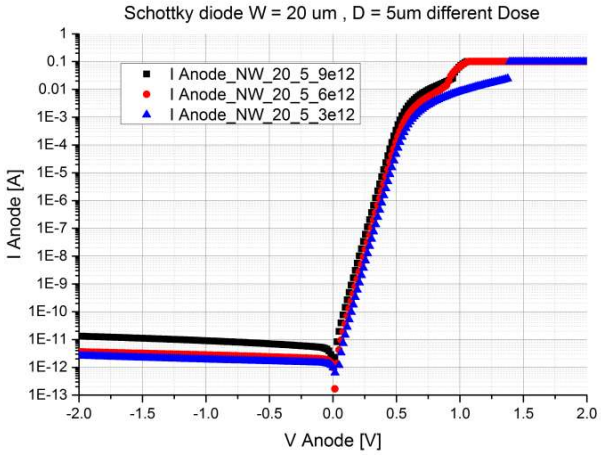


Fig. 4.11 Schottky diodes W = 20µm, D = 5µm for different NW dose

The Schottky contact mask with guard ring structure has a lower reverse current than Schottky contact mask with the rectangular or cylindrical structure as shown in Fig. 4.12. But the current at low bias for Schottky diode with guard ring is lower than the Schottky diodes without guard ring due to the influence of the p+ junction as discussed before. The influence of the Schottky contact width (W) on the forward current is shown in Fig. 4.13. The larger the width W the lower the current at a low bias voltage. With increasing Schottky contact width W the resistance in the n well region plays a role to reduce the current conduction. As seen the current at same bias for Schottky contact width W = 70µm is less than the current for the Schottky diode with W = 5µm.

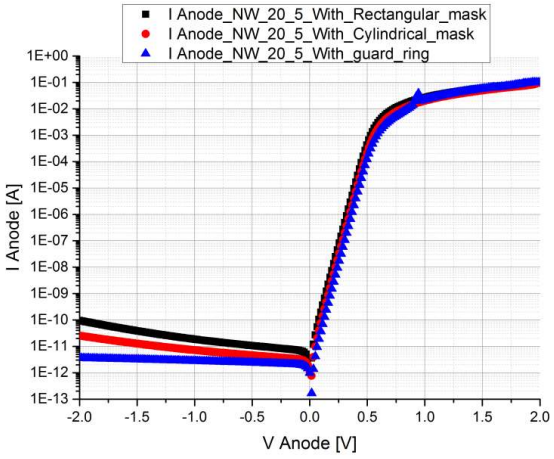


Fig. 4.12 Schottky diodes W = 20µm, D = 5µm for different layout design

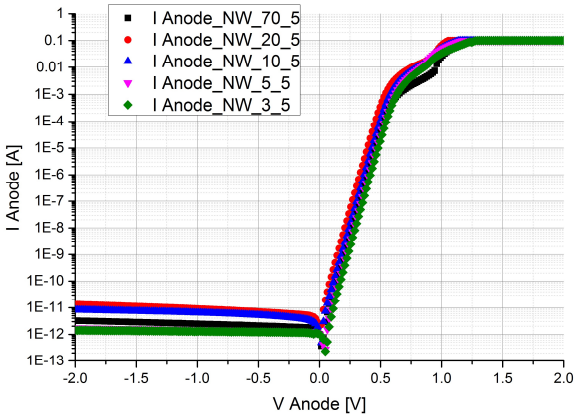


Fig. 4.13 Schottky diodes with different Schottky contact width W

In summary of the above points, the forward conduction of the Schottky diode is highly dependent on the doping concentration of the n-well, Schottky contact width (W) and distance (D). Using higher doping of n-well, with reduced distance between Schottky and ohmic contact (D) yields higher current.

Next the analysis of breakdown voltage of the Schottky diode from the data in the table is discussed in the following points below,

1. The analytical analysis yields that the breakdown voltage is highly dependent on the doping concentration of the n-well. Lower the doping concentration, lower the reverse current and higher the breakdown voltage. By controlling the dose of the n-well we can achieve lower doping in the n-well region as verified previously. The lower n-well dose is, the higher breakdown voltage is. The average breakdown voltage for n-well dose of 3e12 is about 21V, for 6e12 it was 20V and for 9e12 it is around 15V for rectangular Schottky contact mask. The Schottky layout with cylindrical contacts showed a slightly higher breakdown of about 5%. This is not too large when compared to the rectangular layout. The average value is 21V for 3e12, 22V for 6e12 and 16V for 9e12. For Schottky diode with guard ring, there is a large increase in breakdown voltage and a large decrease in the reverse saturation current for n well dose of 6e12 and 9e12. The average value of the breakdown voltage is 29V for 6e12 and 24V for 9e12. For 3e12 the breakdown voltage with guard ring did not show significant improvement, which punches through might occur due to the lower thickness of n-well.

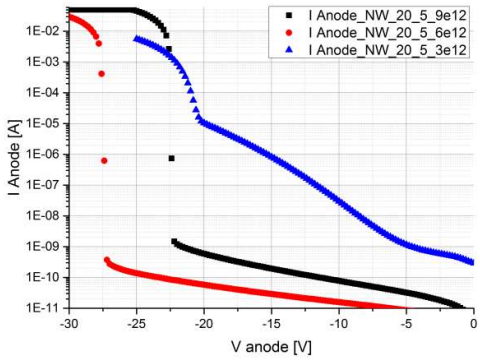


Fig. 4.14 Breakdown Voltage for W = 20µm, D = 5µm for different NW dose – Cylindrical Schottky contact mask with a guard ring

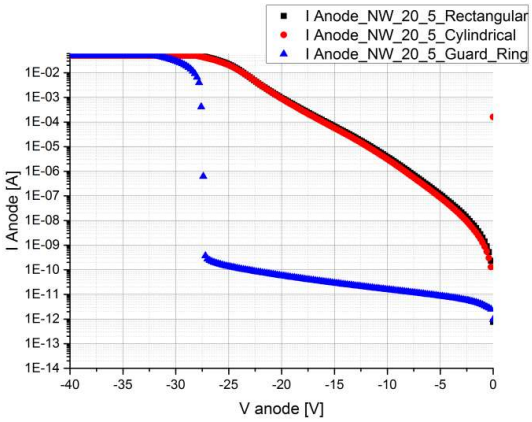


Fig. 4.15 Breakdown Voltage for W = 20µm, D = 5µm for different layouts

2. The cylindrical layout structure for the Schottky contact did have a small effect on the breakdown voltage. The breakdown voltage increases to about 5%. But the predominant effect on the breakdown voltage can be seen with the addition of guard ring structure. The breakdown voltage increases to about 30% when compared to breakdown voltage without guard ring structure.

3. The variation of breakdown voltage for guard ring structure with a different width of the Schottky contact is shown in Figures as follows. The increase in width of the Schottky contact does not influence breakdown voltage. The reverse current is lower but for lower width W of the Schottky contact.

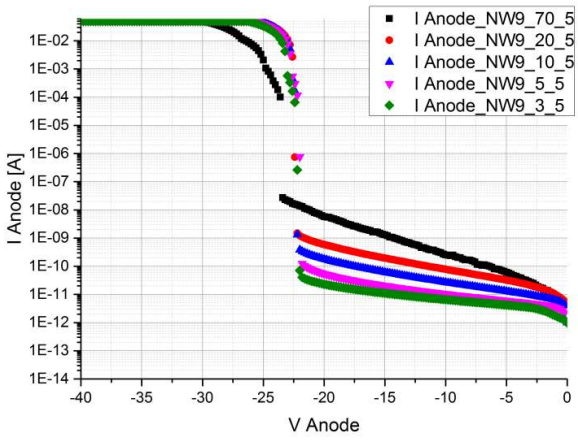


Fig. 4.16 Breakdown Voltage for different Schottky contact width W - NW9e12

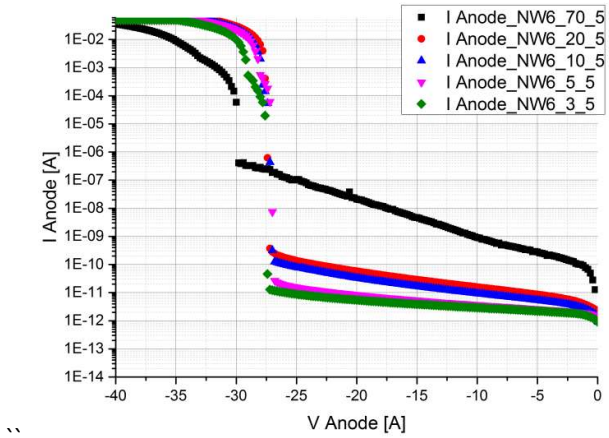


Fig. 4.17 Breakdown Voltage for different Schottky contact width W - NW6e12

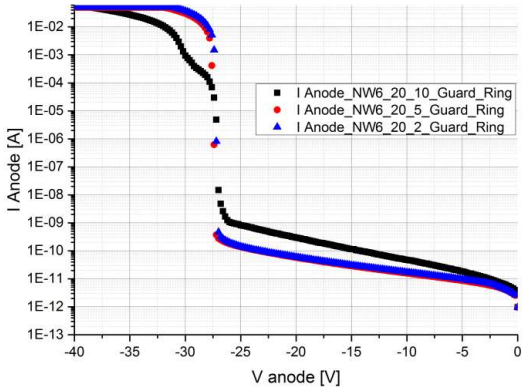


Fig. 4.18 Breakdown Voltage for different distance D - NW6e12

4. The influence of the separation between Schottky contact and ohmic contact (D) is shown in Fig. 4.18. The variation in the breakdown voltage with decreasing D is large for Schottky diodes without guard ring structure. The breakdown voltage is similar for the range of D between 5µm and 10µm. But with lowering of D to about 2µm, the diodes' breakdown as low as 1V. But with the addition of guard ring structure, a higher breakdown is achieved by the structure with D = 5µm.

In summary of breakdown analysis from the measurement data, the breakdown voltage is increased to about 30% by the addition of p+ guard ring to the edge of the Schottky contact. The distance 'D' between the Schottky contact and ohmic contact should be kept at a minimum of 5 µm to achieve the higher breakdown of the devices. The highest breakdown was achieved for n well dose of 6e12 with p+ guard ring in the range of 26-29V. The Schottky diodes fabricated in this planar process have a breakdown of about 27V.

From the measurement of forward and reverse characteristics, in order to achieve high current and high breakdown in this process:

1. Schottky diode must have a p+ guard ring structure doped with n-well dose of 6e12-9e12 (with the depth of 3µm from the drive-in time of 8hrs).
2. The minimum separation D between the Schottky contact and ohmic contact should be 5µm to achieve reliable breakdown with p+ guard rings.

3. The width of the Schottky contact (W) should be in the range of 5 µm -20 µm.

4.2 Spice Model of Schottky Diodes

The spice model of Schottky diodes consists of mathematical equations, parameters, and all the variables which are derived in such a way that they can simulate the complete device as accurately as possible in a simulator supporting spice models of semiconductor devices. The accuracy in which the parameters are extracted depends on the extraction methodology. The large signal equivalent circuit of a Schottky diode is shown in Fig. 4.19. The circuit consists of an ideal diode with a forward voltage drop of V_F in series with a resistor R_S. This is the resistance of the diode is in saturated forward bias condition. G_{MIN} is the shunt conductance across the junction.

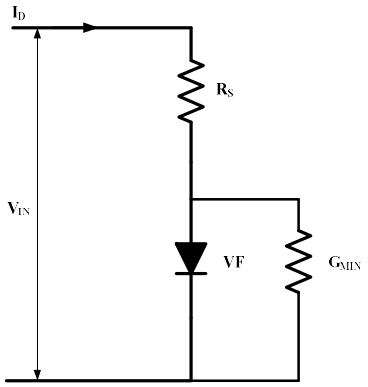


Fig. 4.19 Equivalent circuit of Schottky diode

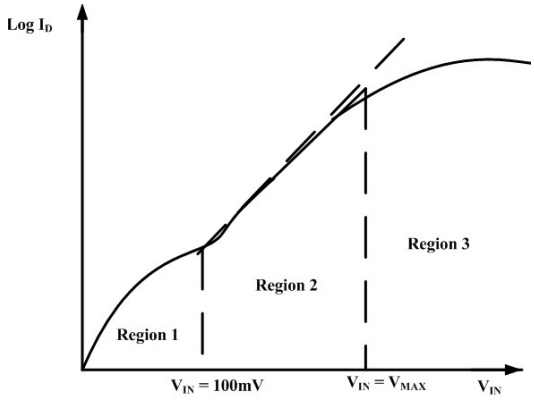


Fig. 4.20 Regions in forward IV characteristics

Table 4.2 Measurements of Schottky diodes and extracted model parameter

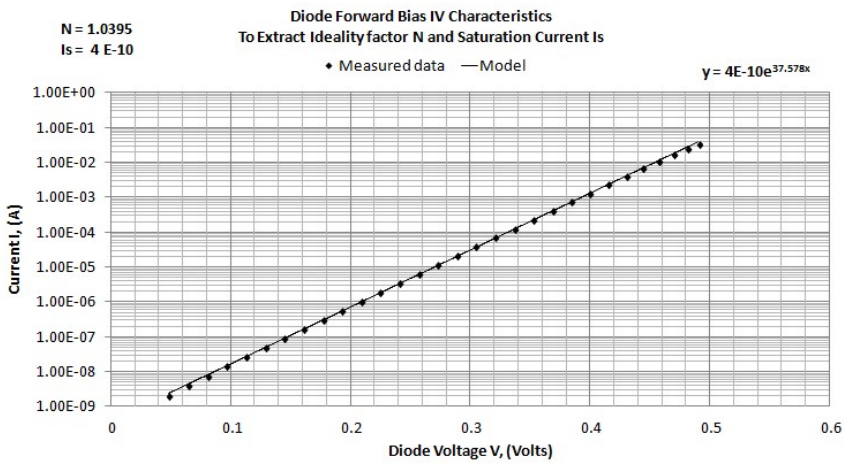
Measurement	**Extracted Model parameter**
Forward IV measurements	IS,RS,N
CV measurements	CJO,VJ,M
Breakdown	BV, IBV

As shown in Fig. 4.20, Region 1 is the region at low forward voltage bias under 100mV caused due to extremely low-level injection of carriers across the junction. Region 2 operated in low-level injection and the diode is almost ideal. The current increases rapidly for low changes in voltage. This happens until the maximum value of V_{IN} is reached where the series resistance of the diode comes into effect and it is the Region 3. The slope of the line in Region 2 gives the ideality factor of the diode. The main measurements that are made to extract the dc parameters for the spice model of the diode are forward IV measurements, reverse IV measurements and Capacitance- Voltage measurements. The main parameters extracted for each measurement data is shown in Table 4.2.

4.2.1 Forward IV Measurement

The measurements were done on cascade probe station and ICCAP software. The forward bias was increased from -2V to 2V. For extraction of ideality factor N, the region 2 of the IV curve in Fig. 4.21 (a) is used for parameter extraction. The slope of this line gives the ideality factor N. The extractions of N for Schottky diode W = 20µm and D = 5µm having 50 fingers is shown. The parameter Rs is extracted from the high bias region using the method in as shown in Fig. 4.21 (b).

(a)



(b)

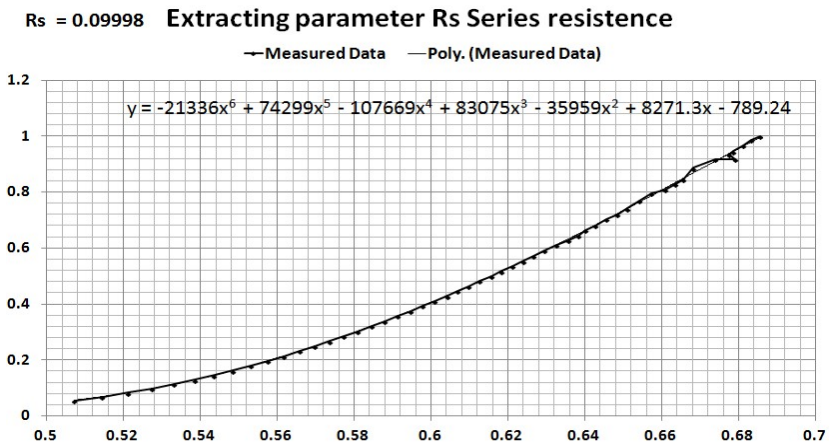


Fig. 4.21 (a) Extracting Ideality factor N for N-well dose=9e12. (b) Extracting factor Rs for N-well dose =9e12.

4.2.2 Capacitance Measurement

The capacitance measurements were by reverse biasing the Schottky diode from 0 to -3V. The CV characteristics obtained is shown in Fig. 4.22. The capacitance for large area Schottky diode is in the range of 600pF to 800pF.

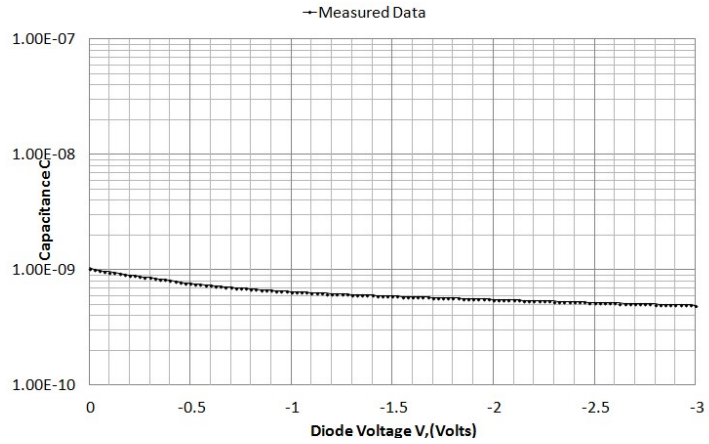


Fig. 4.22 Capacitance-Voltage characteristics of Schottky diode

The capacitance parameters have a strong dependency on the area of the Schottky diode. As the area increases the capacitance also increase. Hence, one of the disadvantages of large area Schottky diode is the increase in capacitance of the device. A comparison of Schottky diodes with area 1.23 sq mm and 0.23 sq.mm is shown in Fig. 4.23. The capacitance of a large diode is in the order of 800pF whereas the capacitance of the small diode is in the range of 200pF.

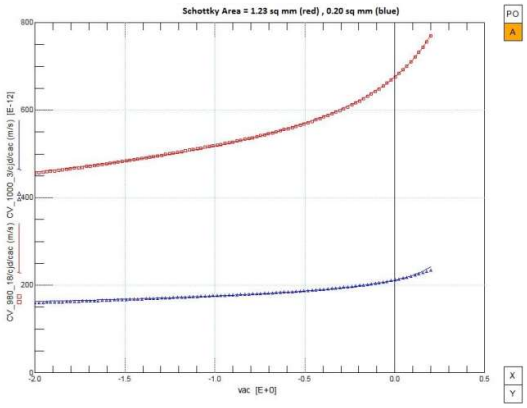


Fig. 4.23 Capacitance-Voltage characteristics different area

4.2.3 Breakdown Voltage Measurement

The reverse characteristics are done using the same approach as previously in the measurement of high current Schottky diodes. From the

Table discussed before, the breakdown voltage and the current at breakdown IBV is derived.

In order to extract the transit time and the reverse recovery time is parameter special setup is needed. The reverse recovery time of the diode is defined as the time that the current becomes negative and recovers to a value to about 10% of the peak reverse saturation current during the switching from forward bias to reverse bias. A JEDEC test circuit is required for the extraction of this parameter. The parameters EG – energy gap, XTI – Is temperature co-efficient are considered as default values. The above spice model is used for the LT spice circuit analysis.

Table 4.3 Spice model extracted parameters of high current Schottky diode

Parameter	Name	NW9e12	NW6e12	NW3e12
IS	Saturation current	4E-10	2E-10	IS
RS	Ohmic resistance	0.09968	0.101	0.09
N	Ideality factor	1.03	1.02	1.0395
CJO	Zero bias junction capacitance	890pF	733pF	633pF
VJ	Contact potential	0.4298	0.26	0.13
M	Junction capacitance grading	0.277	**0.23**	0.2278
BV	Reverse breakdown	22.5	26.4	11.2
IBV	Current at reverse breakdown	1.35E-06	2.9E-07	1.85E-9

4.3 Simulation of Rectifiers Using DIMES BiCMOS7 Schottky Diode Model

The rectifier configuration used in the conversion of AC to DC is a bridge rectifier circuit. The bridge rectifier consists of four Schottky diodes connected as shown in Fig. .The diodes are connected in such a way that during the positive half cycle of the ac input signal diodes D1 and D2 are in forward bias and conduct. During the negative half cycle, the diodes D3 and D4 will be conducting and D1 and D2 are reverse biased. In both the cases the current flowing through the storage capacitor C and the load is in the same direction. The output DC voltage obtained will be equal to the peak AC input minus the twice the forward voltage drop across the Schottky diode. The input AC voltage is 12V with frequency 50 Hz. The output DC voltage is in the range of 11V with the voltage drop across the Schottky diodes are around 0.4V.

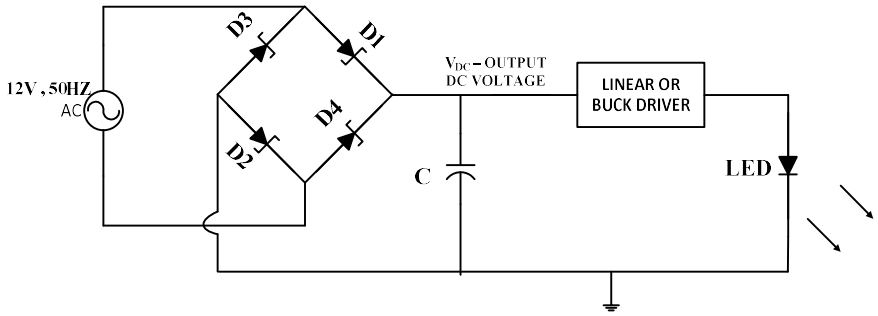
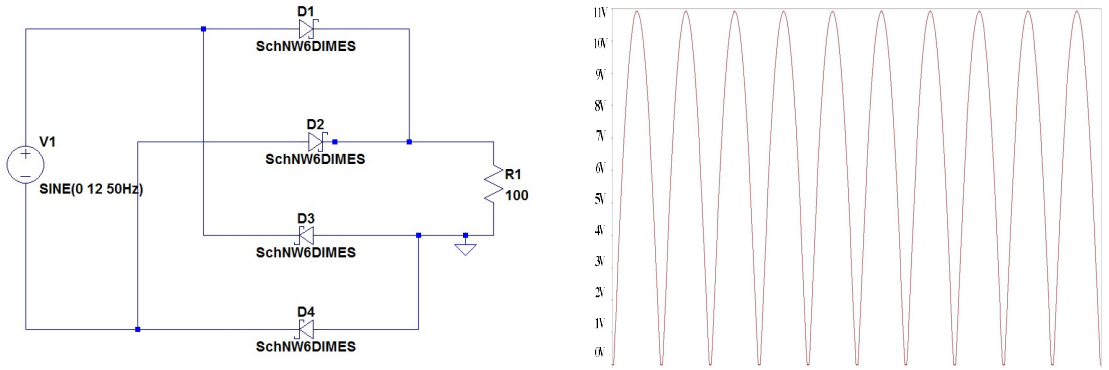


Fig. 4.24 Schematic of Rectifier circuit with Schottky diodes

A schematic of full wave bridge rectifier in LTspice considering a small load of 100 Ω is shown in Fig. 4.25. The circuit is simulated for an AC input voltage of 12V, 50Hz. The spice models used are the Schottky diode models derived from the previous chapter. The Output voltage waveforms obtained are shown as well.



(a) (b)

Fig. 4.25 (a) Schematic of Rectifier circuit with schottky diodes. (b) Output voltage at resistor

From the above simulations, it can be seen that the output voltage at the individual diode terminals is about 11.4 to 11.5V. This means the forward voltage drop across the schottky diode is about 0.5-0.6V. The output voltage from Fig. 4.25(b) is about 11V. The output ripple is due to the absence of storage elements in the schematic. To minimize the ripple, a storage capacitor is used to filter the output voltage and provide a constant dc voltage. The storage capacitor C charges during the positive cycle of the output DC voltage. As the diode voltage drop goes low due to the AC input signal, the capacitor discharges slowly across the resistor, thus providing a lesser ripple than a circuit without the capacitor. The capacitor charges again during the next positive cycle of the output DC voltage thus trying to maintain a constant output DC voltage across the load. The discharge time of the capacitor is dependent the RC time constant of the filter circuit. A schematic of LTSpice simulation with the storage capacitor and LED as the load is shown in Fig. 4.26 and the output voltage and current obtained in the circuit is shown in as follows.

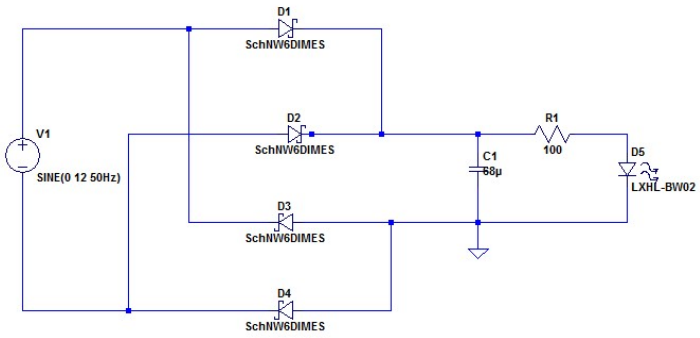


Fig. 4.26 LTspice schematic of Rectifier circuit with resistor as linear driver

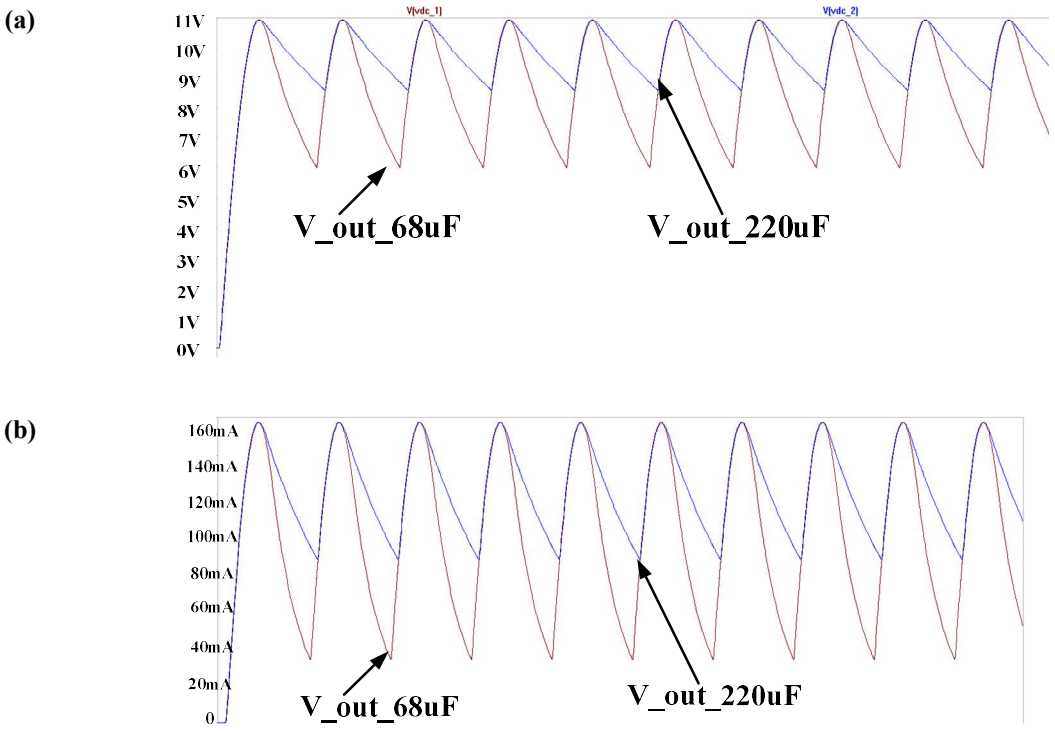


Fig. 4.27 Simulation of the integrated rectifier circuit with Schottky diodes fabricated in BiCMOS7 process. (a) output voltage with capacitors of 68 µF and 220 µF. (b) output current with capacitors of 68 µF and 220 µF.

The output current ripple is about 35% for a capacitor with 220 µF with maximum current at 160 mA and it is about 70% for a capacitor with 68 µF. Hence a resistor based LED driver is highly inefficient as a constant current driver. In the following sections, two modes of LED driver based on such rectifier is investigated and tested.

4.4 Characterization of Integrated Rectifier Fabricated in BiCMOS7 Process

A characterization setup for testing the rectifier as shown in Fig. 4.28 is used. The terminals of the rectifier chip are probed using the cascade probe station. The terminals of the cascade station are then connected to an oscilloscope and a function generator to study the electrical characteristics of the rectifier chip.

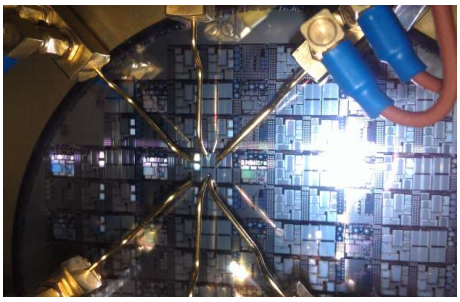


Fig. 4.28 On-wafer testing of the rectifiers using cascade probe station

Similar measurements are made as the simulation of the rectifier in LTspice. The input voltage was set at 11V due to the limitation of the frequency generator. The frequency is set as 50Hz. The output at the diode D1 in the rectifier circuit in Fig. 4.29 obtained is shown below,

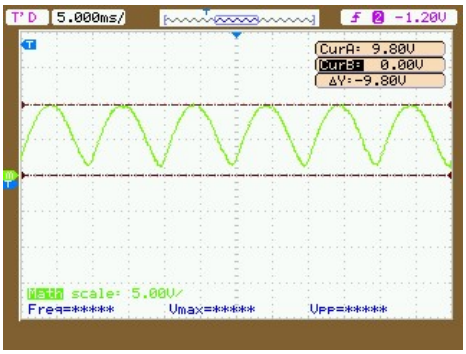
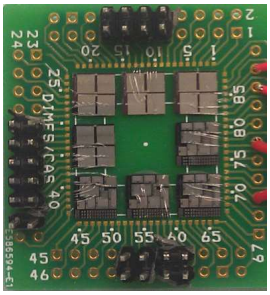


Fig. 4.29 Output voltage at the load of the integrated rectifier

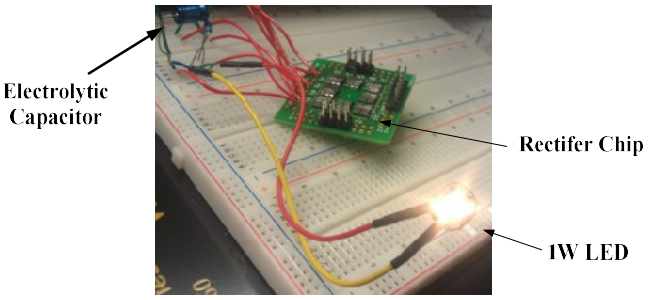
The diode D1 conducts only in the positive half of the cycle whereas the diode D4 conducts only during the negative half of the cycle. The maximum DC voltage obtained for an input of 11V is 10.4V. The drop across the Schottky diode and the probe connector resistor is about 0.6V. The output at the load of the bridge rectifier is shown in Fig. 4.29. The output across the load resistor is about 9.8V. There is a drop of 1.2V across the rectifiers and the probes.

Next, a circuit was built up for rectifier chip with a filter capacitor of 220 µF. The capacitor along with a load resistor of 100 Ω forms the circuit of a linear driver for powering the LED. The setup is shown in Fig. 4.30. The storage capacitor provides a constant dc voltage and the resistor limits the current to 100mA in the LED.

Therefore, a fully integrated rectifier using Schottky diode in BiCMOS7 process was modeled and experimentally verified. The measured output closely matches the simulated output in LTspice.



(a)



(b)

Fig. 4.30 (a) Integrated rectifier wire-bonded to PCB. (b) Integrated rectifiers and linear driver for the G4 LED

The final fabricated devices on wafer after metallization process is shown in Fig. 4.31. The wafer consists of 3 dies with different Schottky mask design. Each design is fabricated on a 6mm x 6mm die in a 4-inch wafer. The rectifier has a dimension of 3mm x 3mm. There are also NPN transistors fabricated together. In this work, monolithic integrated of bridge rectifiers using Schottky diodes are designed, fabricated in BiCMOS7 process. BiCMOS7 is a semiconductor fabrication process in which diodes, transistors, and MOSFETs are

fabricated in a planar process on a single substrate. The DIMES BiCMOS7 process is simple, low cost 7 mask process to fabricate the devices. The Schottky diodes fabricated in the standard planar process have a breakdown of about 27V. The fabricated chip in this process with rectifiers using Schottky diode is shown in Fig. 4.32.

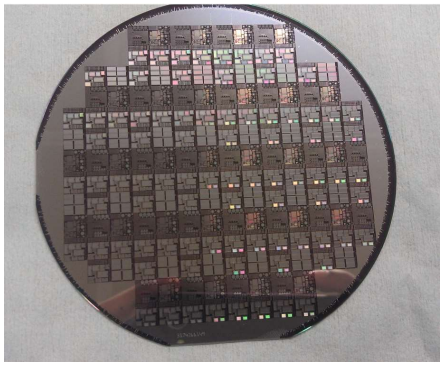


Fig. 4.31 Wafer after metallization and alloying step

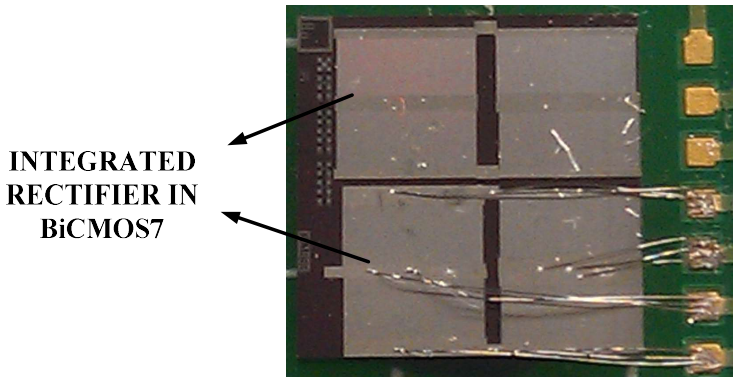


Fig. 4.32 Fabricated Integrated rectifiers chip in BiCMOS7

The integrated rectifier has a dimension of 3mm by 3mm. The Schottky diodes are optimized for high breakdown and high current conduction for retrofit G4 driver requirements. However, to gain more lumen output, more LEDs need to be connected. Therefore, a new WLP silicon-based substrate will be introduced in the following chapter. Such substrate enables the rectifier to be integrated on silicon, while shrinking the total size and bringing uniform light distribution. In the next chapter, a basic linear driver and buck driver circuit based on the integrated rectifiers will be further analyzed.

4.5 Temperature Sensor

All temperature sensors can be divided into two categories: the absolute sensors and the relative sensors. An absolute temperature sensor measures temperature which is based on the absolute zero or any other point on a temperature scale, such as thermistors and resistance temperature detectors (RTDs). A relative sensor measures the temperature difference between two objects which one object is used as a reference, for instance, thermocouple sensors. [4] A comparison of temperature sensors are listed as follows:

Table 4.4 Advantage and disadvantages of popular temperature sensors [14]

	Advantages	Disadvantages
Thermistor	High output	Non-linear output
	Fast	Limited temperature range
	Two-wire ohms measurement	Fragile
		Current source required
		Self-heating
RTD	Most stable	Expensive, slow
	Accurate	Current source required
	More linear than thermocouple	Small resistance change
		Four wire measurement is needed.
Thermocouple	Self-powered	Non-linear
	Simple and inexpensive	Low voltage
	Wide variety of physical forms	Reference required
	Wide temperature range	Least stable and least sensitive
Semiconductor sensors (Schottky diodes, PN junction diodes, etc.)	Most linear	Power supply required
	Highest output	Slow
	Inexpensive	Self-heating
		Limited configurations

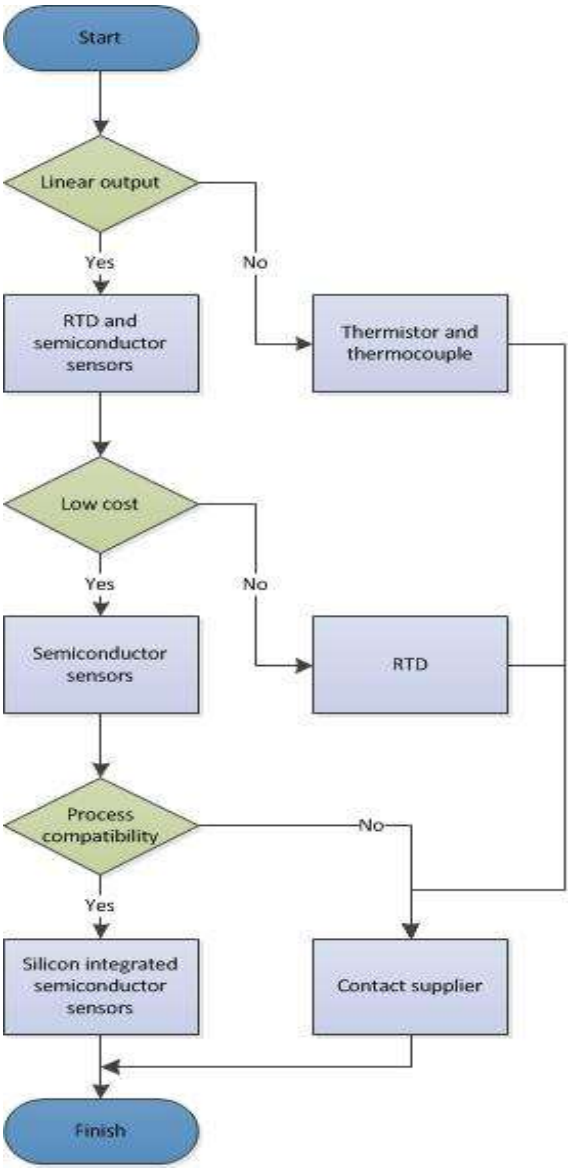


Fig. 4.33 How to choose temperature sensor for miniaturized solid state lighting applications

Reviewing a few key design aspects, an optimum choice of semiconductor sensors were chosen for miniaturized solid state lighting applications, such as G4 LEDs, as shown in Fig. 4.33. Based on the flex/rigid substrate mentioned in previous chapters, the silicon-based temperature sensor is preferable, taken into consideration of fabrication process compatibility. A semiconductor p-n junction in a diode exhibits strong thermal dependence. If the forward-biased junction is connected to a constant-current generator, the resulting voltage becomes a measure of the junction temperature. Such sensor exhibits a high degree of linearity, which allows simple calibration using just two points to define the slope (sensitivity). [7] The current-to-voltage equation of a diode can be expressed as:

$$I = I_0 \exp\left(\frac{qV}{2kT}\right) \quad (4.4)$$

Where I_0 is the saturation current.

In this work, taken into consideration of the process compatibility and integrated driver electronics, Schottky diode mentioned in previous of this chapter is chosen in this work to replace traditional PN junction diode as a temperature sensor.

In normal p-n junction diode, the junction is formed between p type semiconductor to n type semiconductor. Whereas in Schottky diode, the junction is in between N type semiconductor to metal plate. As a result of that, the Schottky diode is a unipolar device since Schottky diode has electrons as majority carriers on both sides of the junction. Current conduction is happening due to movement of electrons only. Therefore, the forward voltage drop is less compared to normal p-n junction diodes due to no depletion layer formed near the junction. Moreover, since there is no holes movement in Schottky diodes, the leakage current is negligible.

The linear operation voltage of such a sensor can be easily tuned by connecting a resistor in series, to meet the control window. The effect on the forward bias characteristics under different temperature conditions is shown in Fig. 4.34.

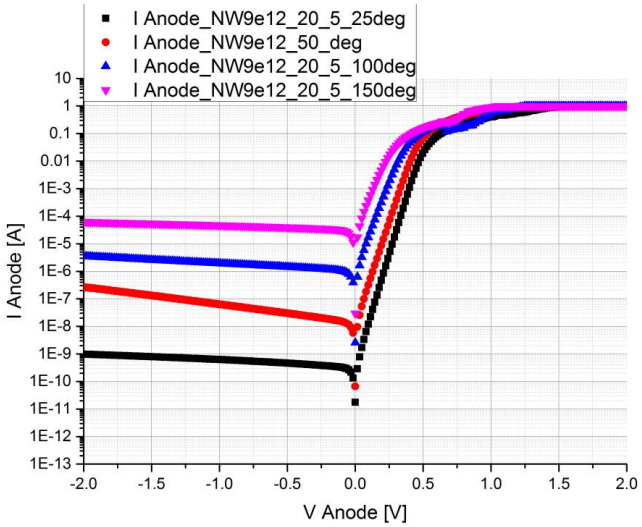


Fig. 4.34 High current Schottky diodes temperature characteristics forward IV

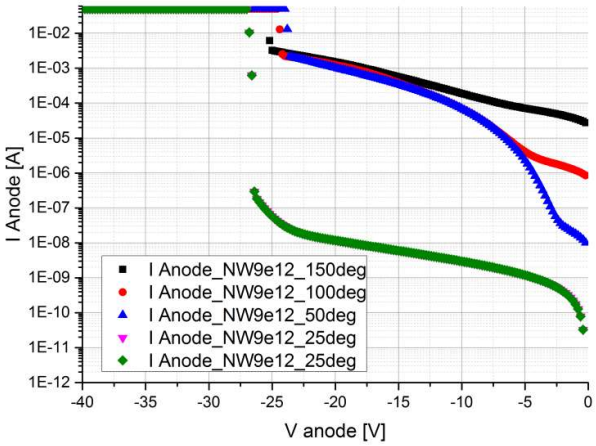


Fig. 4.35 High current Schottky diodes temperature characteristics reverse IV

Reverse biased characteristics were correspondingly measured as Fig. 4.35 shows. It is clear that reverse current increases as temperature increases. It worth to mention here that Schottky diodes break down much faster at higher temperatures. Therefore, thermal management needs to be further investigated for applying such sensor in miniaturized SSL applications, though silicon provides already quite good thermal conductivity for heat dissipation.

For better understand such Schottky diodes for temperature sensing, spice model of such Schottky diodes were derived to simulate as accurately as possible. More details will be explained in Chapter 4.

4.6 Light Sensor

A device which can detect electromagnetic radiation in the spectral range from ultraviolet to far infrared is called light sensor, or light detector. [15] Light sensors can be divided into two major groups: quantum and thermal, depends on the sensing material result either in a quantum or thermal response after photons absorption. Light sensors range from a photomultiplier tube which gives a large voltage pulse for every photon it detests, to cooled thermopiles that absorb kilowatts of power providing a thermocouple voltage proportional to the optical power absorbed. Some light sensor characteristics are summarized in the following table [16].

Taken into consideration of design rules mentioned in Fig. 4.36, photodiodes were chosen as light sensors in this work. Photodiodes are essential for energy saving, since they perform as light sensors. Several technics were developed for light sensing. In the work of R. Stojanovic and D. Karadaglic [16], one or two KEDs are used as a photodetector to detect sunlight intensity. Reverse biased LEDs can generate photocurrent by the incident light, even possible to apply without amplification. In the work of A. Pandharipande and S. Li [13], the use of LED as an emitter and sensor for daylight were described. An array of 6 surface mounted LEDs were connected in parallel. Such type of light detector is highly power efficient but with a logic output. Taken into consideration of the size of microcontroller, analog sensors were chosen in this work for miniaturized solid state lighting applications.

A blue light silicon-based detector designed by Zahra Kolahdouz from TU Delft was chosen, as shown in Fig. [17]. It is composed of a silicon stripe-shape photodiode designed and implemented in a BiCMOS process with 5 masks and 2 µm gate length. Since it is CMOS compatible, the final device can be easily integrated together with the integrated driver circuit.

Table 4.5 Comparison of light sensor characteristics [16]

Electrical Characteristics	Photo-diodes	Photo-transistors	CdS Photocells	Other Photo-conductors	Integrated Circuits	Hybrids	Sensor Electronic Assembly
Available Wavelengths (μm)	0.2-2.0	0.4-1.1	0.4-0.7	2-15	0.2-1.1	0.2-15.0	0.2-15.0
Linearity	Excellent	Good	Good	Good	Good	Good	Good
Ambient Noise Performance	Very Good	Very Good	Very Good	Very Good	Excellent	Excellent	Excellent
Dynamic Range	Excellent	Very Good	Good	Good	Very Good	Very Good	Very Good
Stability	Very Good	Good	Poor	Fair	Very Good	Very Good	Very Good
Reproducibility	Excellent	Fair	Poor	Fair	Very Good	Very Good	Very Good
Cost	Low	Very Low	Very Low	High	Medium	High	Medium
Ruggedness	Excellent	Excellent	Excellent	Good	Excellent	Very Good	Excellent
Physical Size	Small	Small	Small	Small	Small	Medium	Medium
Ease of Customization	Easy	Fair	Fair	Poor	Poor	Poor	Fair
Cost of Customization	Low	Medium	Low	High	Very High	High	Medium

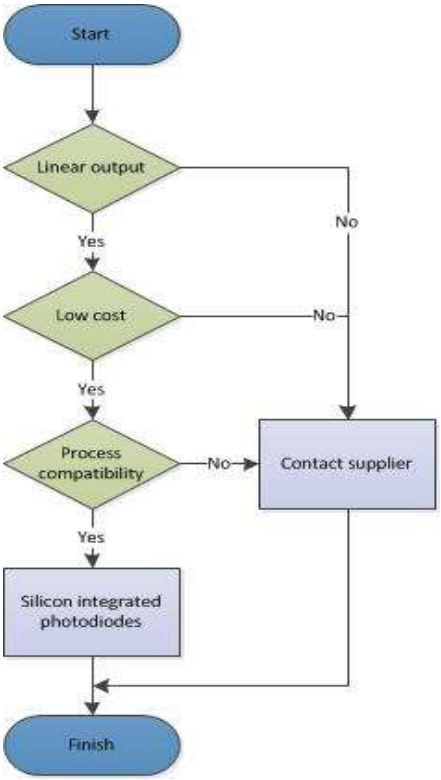


Fig. 4.36 How to choose a light sensor for miniaturized solid state lighting applications

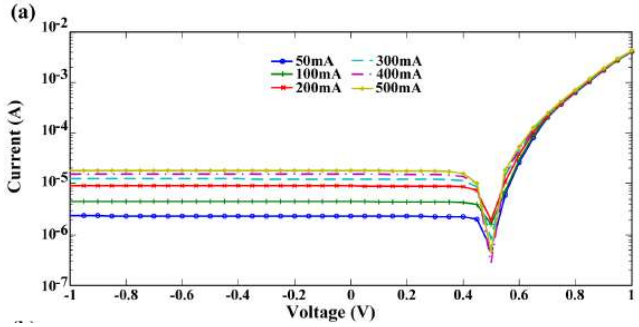


Fig. 4.37 Photodiode output IV curve at different LED driving current [17]

However, the current output of such diode was too low for applications in this work. In order to amplify the output voltage to 2.5V, a 50kX resistor was connected in series with the diode. 3 orders of magnitude increase of light were controlled and tested for such photodiodes (0.1A, 0.35A, 0.7A). As shown in Fig. 4.38, a linear output was reached for IV measurement. It worth to mention that for such device can barely be influenced by ambient light, due to its blue light selectivity. If the application is aiming for daylight response, further adjustment is needed for such photodiode for daylight selection. The sensed light intensity by a photodiode for high current input is slightly lower than the LED specification. This is probably due to high temperature under high current input.

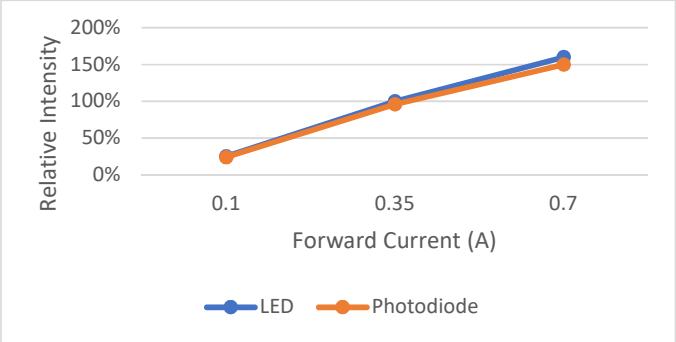


Fig. 4.38 Photodiode vs LED at different LED forward current

4.7 Conclusion

The main goal of this work is to design, fabricate, and test wafer level integrated electronics for solid state lighting applications. By monolithically integrating rectifiers, drivers along with wafer level packaging of LED on silicon offers better reliability at a reduced cost. In this work, low power rectifiers in DIMES BiCMOS7 process was successfully designed, fabricated and characterized. The large area Schottky diodes fabricated in this process achieved an average breakdown of 27V with forward current conduction of 1A at a forward voltage drop of 0.65-0.7V. Spice model of such Schottky diodes, together with NMOS devices fabricated in-house were also generated and calibrated by characterization.

Not only monolithic integration, silicon integrated sensors were also discussed, which are temperature sensor and light sensor. Miniaturized solid state lighting systems required sensors which can operate under a critical environment such as limited volume, low power supply, and ability to work under high temperature. For each kind of sensor, a selection methodology was introduced. Such choices were mainly based on considerations of the existing technology, cost, limited volume, process compatibility, etc. Schottky diode was chosen as temperature sensing based on the same manufacturing process mentioned for driver integration, and linear output for easy control. The photodiode was chosen based on compatibility of BiCMOS process, and linear output as well. In the next Chapter, such sensor integration with control IC will be further discussed. In conclusion, studies conducted on these monolithic wafer level integrated devices make silicon a promising substrate for smart and miniaturized lighting applications.

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Chapter 5 Wafer Level Packaging with Flex/Rigid Substrate

5.1 3D Wafer level Packaging

Since a silicon wafer is part of the package, LED dies need to be placed on the surface or in etched cavities. This means that the packages are essentially flat, only as thick as the substrate wafer. Such a layout is not optimal for a light source, since it reduces the uniformity and can only be applied to unidirectional sources, whereas a general purpose light source needs to emit light in multiple directions. Therefore, 3D WLP integration is necessary for further miniaturization and performance enhancement.

One basic reason for 3D WLP is the system-size reduction. Traditional assembly technologies are based on 2D planar architectures. Additional spacing between components on the board is typically required, further increasing the area-packaging density. Another reason for 3D WLP integration is performance driven. Interconnects in a 3D assembly are potentially shorter than in a 2D configuration, allowing for less power consumption. Furthermore, and maybe the most important reason is to enable hetero-integration, which allows a large variety of functional blocks becomes easier to achieve. [1] As shown in Figure 5.1, Functional tiles on the die are rearranged in multiple dies that are vertically interconnected, resulting in much shorter global interconnect lines.

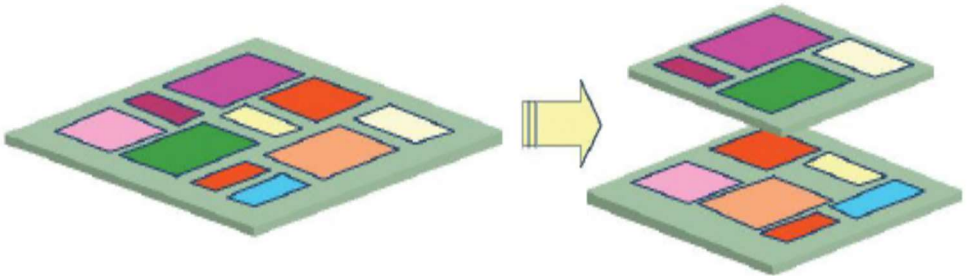


Figure 5.1 Conceptual view of a 3D stacked SOC. [1] Functional "tiles" on the die are rearranged to be vertically interconnected for shortening interconnect lines.

However, such a solution could not solve the light uniformity problem for SSL applications. To gain better light uniformity for WLP packages, flex/rigid substrate were introduced, as presented as follows. The presented package could be used for luminaires that resemble conventional retrofit designs and for volume reduction of current products. The proposed design deals with problems of light uniformity in wafer level packaged devices. By connecting the packaged LED chips with flexible interconnects, rigid-flexible-rigid structures are formed (Figure 5.2). The flexible hinges are bent to angles up to 90° to form 3D shapes with rigid parts acting as side walls. Additionally, the package can be automatically assembled with a designed fixture, to accurately align and wrap into 3D shape. The symmetry of flexible hinges also helps the device to survive from thermal shock.

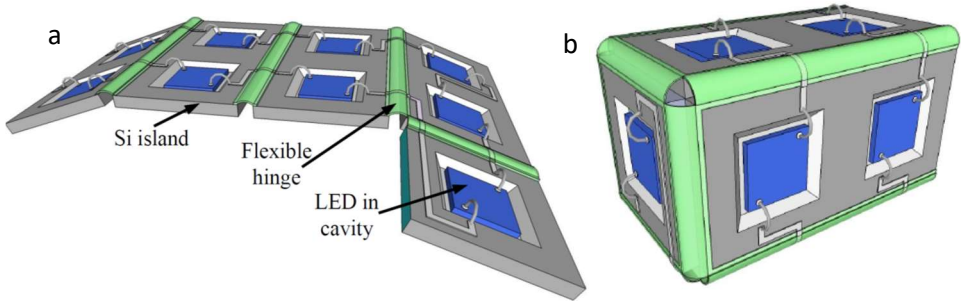


Figure 5.2 Silicon based flexible WLP package concept (a: unfold; b: folded to form a cuboid) [2]

Considering the G4 form factor and performance requirements, Wafer Level Packaging (WLP) can provide solutions to integrate components in limited space and manage heat to dissipate more efficiently. Therefore, a G4 LED prototype (Fig. 5.3) based on WLP was introduced at the end. Furthermore, other technologies like MEMS, CMOS, and other wafer level based technologies can be easily combined with such WLP platform.

Fig. 5.3 Proposed G4 retrofit LED prototype (Schematic drawing)

The main requirements for such fabrication are:

1. possibility to implement LED dies
2. flexible interconnection
3. standard wire bonding and flip-chipping technologies
4. ease of handling and mounting devices in and around the substrate
5. flexible interconnects

Therefore, a flex-rigid substrate which fulfills such requirements were designed, fabricated and tested with implemented LED dies, as described in the following sessions.

5.2 Flex/Rigid Substrate

A 3D wafer level package (WLP) includes silicon substrate with Polyimide/Aluminium flexible interconnect and cavities covered with aluminum to reflect light is designed for miniaturized Solid State Lighting (SSL) Applications such as e.g. G4 capsule. It is an advantage that the package can be easily mass-manufactured in 2D and subsequently assembled to 3D WLP by flexible interconnects. The designed flexible hinges enable the device to endure high thermal stress. An automatic assembly method is also designed for such packages. Light emitting diode (LED) dies are placed in cavities covered with aluminum for optical management. With such packages, it improves light uniformity and reduces volume for solid state lighting applications.

5.2.1 Polyimide

In Benjamin's work[3], such interconnects were designed for medical applications. A generic IC-based fabrication platform combining with complex sensing functionalities were created. Polyimide is spin-coated on a substrate and are desired to be converted into a film form eventually.

Thermal imidization is the most commonly used way to achieve this process. There are mainly two ways to complete this thermal imidization [4-6]. One way is to heat up gradually to the desired temperature which depends on the characteristics of the polyimide and keeps this temperature for normally 2 or 3 hours. Take Durimide 115A from Fujifilm for example, its curing requires 400 °C for 2 hours [7]. Another way is to heat up to a certain temperature and keeps it for 1 hour, then rise to a higher temperature and

keep for 1 hour, another more round if necessary. For CT4112 from KYOCERA, it requires 1 hour at 80 °C, then 1 hour at 120 °C and 180 °C for 1 hour in the end. The product of the cross-linking reaction, water, is evaporated during the processing, which enhances the reaction as stated before.

However, time and temperature are not the only key parameters. The imidization is more preferably to react in more concentrated solutions, especially during the first and internal stages and it is promoted by the residual solvent in the later stage. The residual solvent provides more chain mobility by plasticizing the film. It also allows the favorable conformation for cyclization of the amic acid group.

5.2.2 Polyimide Process

Polyimides (PI) are chosen in this project as flexible substrates and insulator for interconnects. In the process, polyimide was coated on the wafer firstly as a flexible substrate. Interconnects were then fabricated on polyimide and transferred by wafer bonding technology.

(A) Process with Durimide 115A

Durimide 115A is a self-priming, non-photosensitive poly amic acid formulation which needs a curing step to become the polyimide. Fig.5.4 shows the molecular structure of the poly amic acid. The cured polyimide film has a relatively high tensile strength at break (260 MPa) and high Young's modulus (3.3 GPa), which shows a reliable property to be the package of the interconnects.

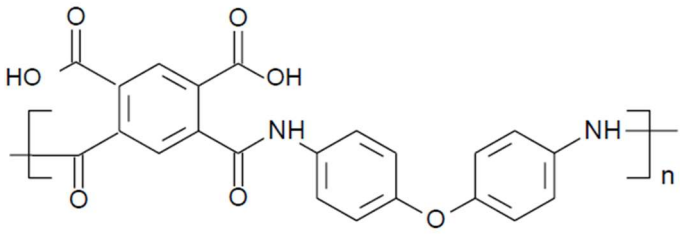


Fig. 5.4 Molecular structure of poly amic acid (PI) Durimide 112A

To process Durimide 112A, it is usually spin-coated on the wafer first. The thickness of the film is related to the spin speed, the uniformity and flatness are affected by the spinning time. Fujifilm has provided the spin speed curves as shown in Fig. 5.5, The uncured polyimide can be patterned with positive photoresist. The positive photoresist is coated on the softly baked polyimide and exposed with the expected pattern after prebake. Then a developer contains TMAH is used to develop photoresist and etch polyimide in the meantime. After the patterning, the photoresist is stripped with a solvent rinse, such as NMP or ethanol. Last, the polyimide is cured in a vacuum oven at 400 °C under the protection of Nitrogen [7]. This process is developed in-house.

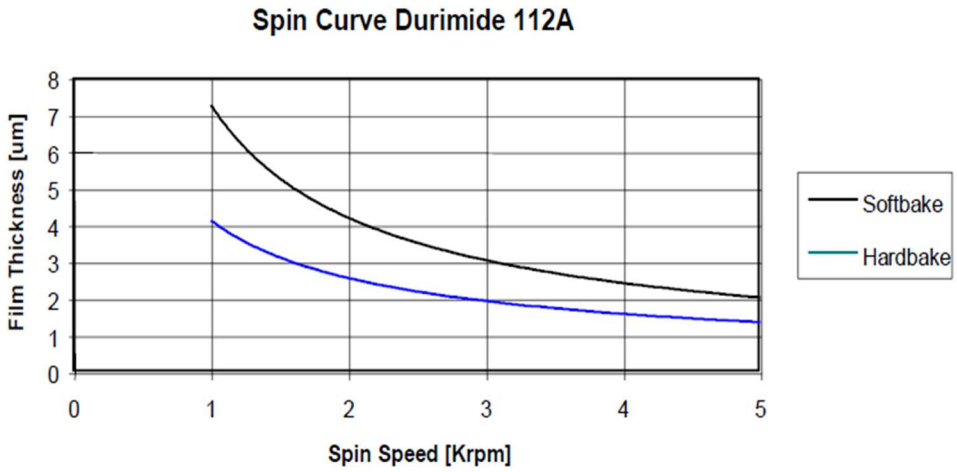


Fig. 5.5 Durimide 112A spin speed curves [7]

Due to the property and disadvantage of this polyimide, more attention has to be paid to under etch and surface adhesion. An under etch of 20 µm per side of the structure has been observed after developed by 1.5% TMAH for 1 min 20 s (film thickness 2.4 µm). Therefore, the under-etch problem should be taken into consideration during designing and more proper developer should be tested. The solvent for photoresist stripping should also be carefully chosen. Acetone, for example, will damage the uncured polyimide, resulting in severe damage of the uncured polyimide and increase the roughness of the surface.

In combination for these works, a flex/rigid wafer level package was designed for G4 LED retrofit. In this work, silicon was chosen to be the solid substrate, linked together by flexible hinges made of Polyimide. Durimide 100 Series 115A PI from Fujifilm is preferred. The fabrication process of such flexible interconnect is as follows:

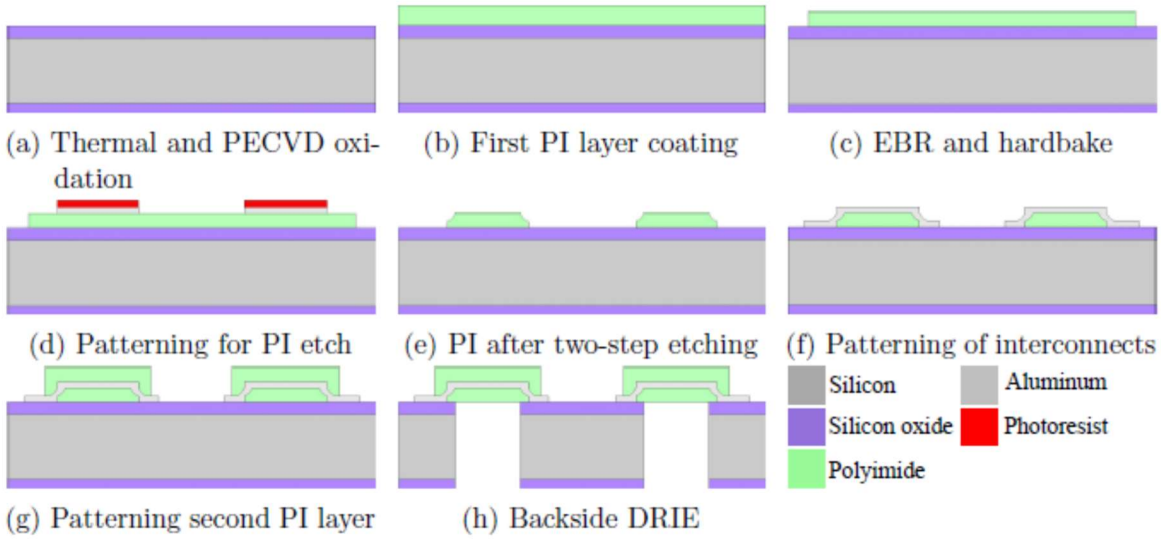


Fig. 5.6 Processing flow of flexible interconnect

a) Thermal silicon oxide is grown on double-side polished silicon wafers (approx. 1 µm thick). The backside is patterned for through wafer etching using thermal and PECVD oxide as masking layer. Further backside protection treatment.

b) First polyimide layer (PI) is spin coated on the front side of a wafer,

c) PI was cured in a vacuum furnace at 400°C. The thickness of the layer can be modified by varying the spinning speed.

d) Pattern the photoresist for PI layer etching

e) PI layer was etched via 2 steps etching: 2.5% TMAOH etch and photoresist stripping using acetone and IPA. After this, polyimide layer lands on silicon

f) A metal layer is sputtered at room temperature and interconnect is patterned.

g) The second layer of polyimide spin coated, matching the first in thickness. Such PI layer is to protect metal interconnects. Both layers of polyimide are patterned to encapsulate the metal where the bending plane will be. Additionally, polyimide strips, designed to keep the silicon islands attached to the wafer, are patterned.

h) Backside through wafer etching is done by either wet or DRIE etching.

(B)Design parameters for flexible hinges: polyimide

Flexible hinges have a typical width (= distance between said solid substrates) between 0.5mm and 3mm, preferably between 0.8 and 1.2mm, most preferably about 0.9mm. The minimum PI length is 735µm for 90° bending, when using 520 µm substrates (as shown in Fig. 5.7). In this design, the PI length is controlled to be the minimum value for easy self-assembly. When bending up to 90°, the flexible cross-section is shown as follows:

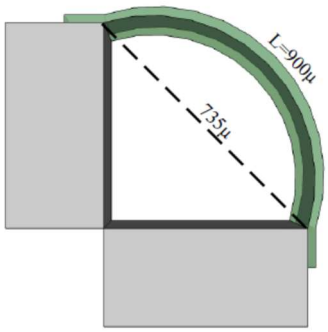


Fig. 5.7 Schematic representation of right angle bend with arc-shaped polyimide hinge

Flexible hinges have a thickness between 3µm and 22µm, most preferably about 18µm. This is according to the PI 115A datasheet spin curve (Fig. 5.8).

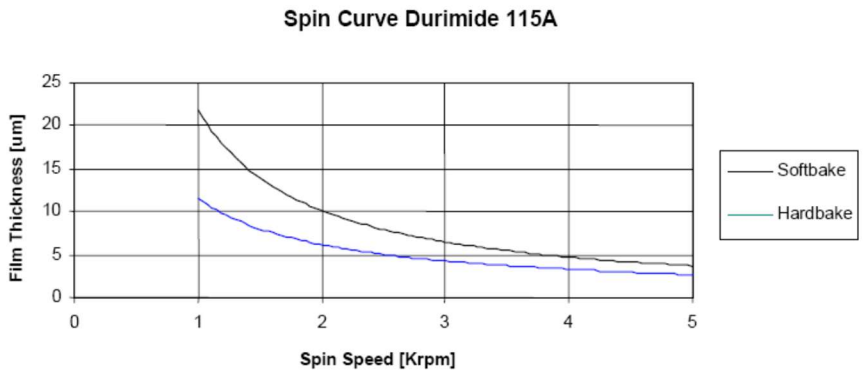


Fig. 5.8 spin curve durimide 115A [7]

(C)Design parameters for flexible hinges: Aluminum tracks

Flexible hinges also comprise Aluminum (Al) tracks for electrical interconnection to drive said LEDs. Typical thickness said aluminum varies between 1µm up to 5 µm, with PI covers from both sides. The ratio of Polyimide top layer thickness vs bottom layer thickness is controlled to be 1, hence the Aluminium track is positioned in a neutral plane, where tensile and compressive forces are canceling each other out.

In order to assemble high power LED dies to the foldable package, the current flow is estimated up to 700 mA. The design parameters of interconnects are influenced by Mean Time to Failure (MTTF), maximum package operating temperature, and bending angles (as shown in Fig. 5.9). The design rule to meet MTTF>25000h, Tmax<85°C, with a bending angle of 90°, the interconnect ratio L/t_hW is less than 2. In the current design, this ratio of 1.5 is chosen, with a dimension of 900µm*300µm*2µm (L by W by t_h).

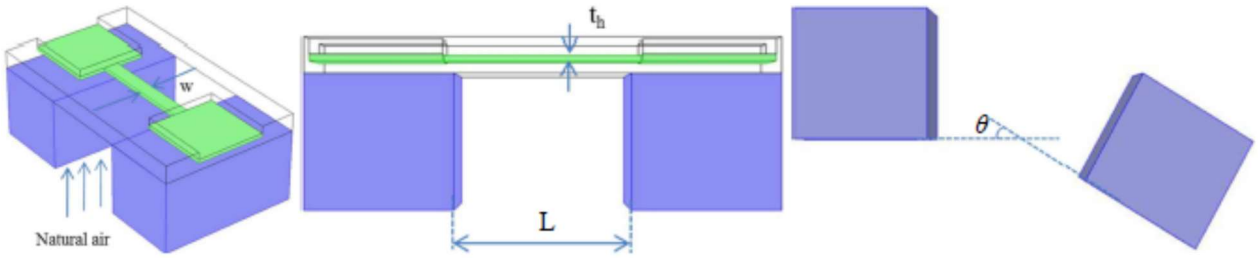


Fig. 5.9 Geometry for FEM simulations of flexible interconnect

FEM simulations were performed in COMSOL Multiphysics 4.2 with modules of Joule heating, electric current, heat transfer, and solid mechanics. All materials properties adopted in this study are listed in Table 5.1.

Table 5.1: Materials Properties input in the model

	Si	Al	PI
Electrical conductivity [Sm-1]	1×10-12	3.8×107	1×10-12
Coefficient of thermal expansion [K-1]	4.2×10-6	2.3×10-5	5.5×10-5
Heat capacity [Jkg-1K-1]	703	900	1100
Density [kgm-3]	2330	2700	1300
Thermal conductivity [Wm-1K-1]	163	160	0.15
Young's modulus [GPa]	131	70	3.1
Poisson's ratio	0.27	0.33	0.34

Joule heating is the only heat source which considered in this work, and expressed in Joule's laws [8]:

$$Q = I^2Rt \quad (5.1)$$

Where I is the current passing in the Al trace, t is the current-on time, and R is the electrical resistance of the Al trace, which can be further expanded as shown in Eq. 5.2.

$$R = \frac{\rho L}{w \cdot t_h} = \rho L/S \quad (5.2)$$

Where ρ is the resistivity of the material, and L/S is an equivalent aspect ratio of the conductive media along the current direction. Therefore, to discuss the geometric effects of Al line on the thermal performance of the RFR substrate, it is rational to treat L/S as one geometric parameter rather than consider L and S separately.

The applied boundary conditions are joule heating due to current flow in aluminum interconnect with natural convection and radiation. The backside of silicon is fixed at 25°C (ambient temperature).

The convective cooling was modeled as [9]:

$$-k \cdot \nabla T = h(T\text{-}T_\infty) \quad (5.3)$$

where $k \cdot \nabla T$ is the surface heat flux, h is the heat transfer coefficient, and $T\text{-}T_\infty$ is the temperature difference between surface and ambient respectively. In the simulations, external natural convection existed with vertical direction from one side of the silicon substrate to the other side, perpendicular with interconnect.

The heat dissipated by radiation to ambient was defined as [9]:

$$-k \cdot \nabla T = \varepsilon\sigma(T^4\text{-}T_\infty^4) \quad (5.4)$$

where ε is surface emissivity and σ is Stefan-Boltzmann constant (5.67×10-8 W/m2K4)

Joule heat generated can be mainly dissipated through silicon. Hence, the middle part of the trace is most likely to be the hottest spot. Furthermore, this spot can be even hotter with larger bending degrees. Due to this evaluated temperature in the spot, the risk of a trace failure because of electromigration significantly increases. This type of failure occurred in a single interconnect is predicted by J.R. Black by Eq. 5.5 [10]:

$$MTTF = AJ^{-n}e^{\frac{E_a}{kT}} \quad (5.5)$$

Where $MTTF$ is the Mean Time To Failure in hours; A is a constant based on a cross-sectional area of the interconnect; J is current density in A/cm2 ($J = \frac{I}{S}$); E_a is Activation energy in eV; k is Boltzmann constant (8.617×10-5 eV/K); T is temperature in Kelvin; n is scaling factor (usually set to 2 according to Black). It is

clear that the geometry of the trace, current level, and temperature are the most relevant parameters to be considered.

According to Black's study, MTTF of sputtered aluminum can be further developed to the formula below [20]:

$$\mathrm{MTTF} = \frac{\mathrm{S}\cdot\exp\left(\frac{\mathrm{Ea}}{\mathrm{kT}}\right)}{5\times10^{-13}\cdot\mathrm{J}^2} \qquad (5.6)$$

Since LED lighting products usually required lifetime longer than 25000 hours, in this study, MTTF larger than 25000 hours was considered as the threshold value to check the feasibility of RFR substrate with certain geometry and bending angle to be adopted in SSL products.

Firstly, the current was set to a constant value for easier comparison. In the following discussion, the current was set to be 100 mA, which is the current for most mid-power LEDs. A temperature difference of maximum temperature point of the system compared with ambient as a function of L/S was determined by 24 simulation runs at zero bending angles, as Fig. 5.10 demonstrated. It shows that the temperature difference $\Delta\mathrm{T}$ between the maximum temperature and the room temperature (25 °C) strictly follows the 2nd order of polynomial trend with $\mathrm{L/S}$, when there are no bends of the interconnect.

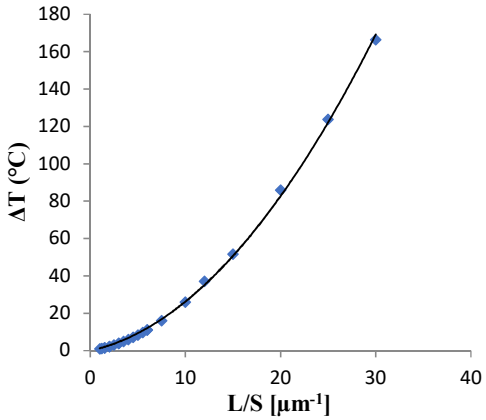


Fig. 5.10: Temperature difference in different L/S value with no bending

Therefore, for the mentioned scenario, the relation between $\Delta\mathrm{T}$ and $\frac{\mathrm{L}}{\mathrm{S}}$ is derived in Eq. 5.7 based on simulation results.

$$\Delta\mathrm{T} = 0.1658(\frac{\mathrm{L}}{\mathrm{S}})^2 + 0.9862\frac{\mathrm{L}}{\mathrm{S}} \qquad (5.7)$$

Since bending angles also influence the maximum temperature of the RFR system, L/S was kept as a constant while the bending angle changes from 0 to 90 degree. Five scenarios with different L/S inputs were simulated. In all scenarios, the function of $\Delta\mathrm{T}$ and θ was found to be quite linear, as in Fig. 5.11 illustrated. The higher the value of the bending angle, the greater temperature difference it is. This relation is shown in Eq. 3.8.

$$\Delta\mathrm{T} = \mathrm{k}\theta + \mathrm{c} \qquad (5.8)$$

Where slope k and intercept c vary with different scenarios. With this equation, $\Delta\mathrm{T} = \mathrm{f}(\theta)$ was obtained.

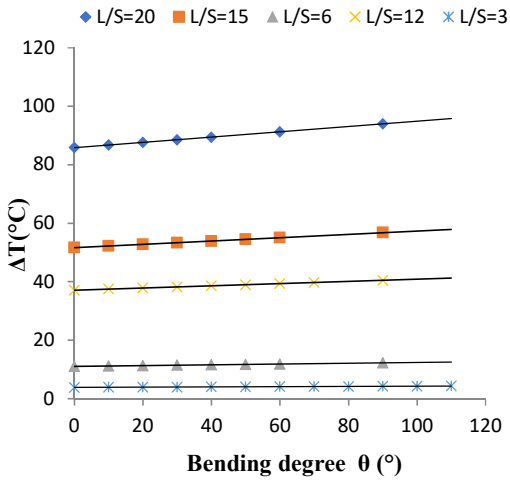


Fig. 5.11: Temperature difference at different bending angles under different L/S scenarios.

In order to derive the relation of ΔT as a function of L/S and θ, the values of slope k and intercept c at different L/S value were found out. As indicated in Fig. 5.12, both k and c follow the 2nd order of polynomial trend very strictly with L/S by:

$$k = 0.0002\left(\frac{L}{S}\right)^2 + 0.0012\left(\frac{L}{S}\right) \quad (5.9)$$

$$c = 0.1658\left(\frac{L}{S}\right)^2 + 0.9862\left(\frac{L}{S}\right) \quad (5.10)$$

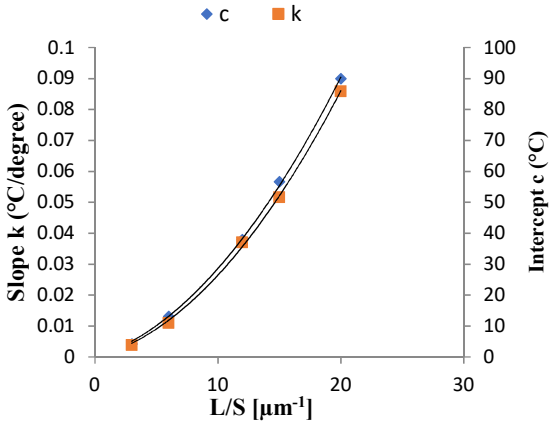


Fig. 5.12: Slope k and intercept c under different L/S scenarios

Therefore, based on Eq. 5.8-5.10, ΔT as a function of both $\frac{L}{S}$ and θ can be written as Eq. 5.11:

$$\Delta T = \left[a_1 \cdot \left(\frac{L}{S}\right)^2 + a_2 \cdot \frac{L}{S}\right] \cdot \theta + a_3 \cdot \left(\frac{L}{S}\right)^2 + a_4 \cdot \left(\frac{L}{S}\right) \quad (5.11)$$

where a_1-a_4 are constants, which are related to current level passing through the Al trace. This equation is also verified by Equation 7 when the bending angle is 0°.

The a_1-a_4 constants obtained at different current levels (0.1 A, 0.35 A, and 0.7 A) are listed in Table 5.2 derived based on the method demonstrated above. With these equations, the maximum temperatures in the RFR substrate can be fast estimated with different bending angles and interconnect geometric dimensions. Fig. 5.13 (a1), (b1) and (c1) illustrated the temperature difference trend when changing the

bending angle and geometric input, with 0.1A, 0.35A, and 0.7A respectively. Threshold value for temperature difference is 65, in order to keep the whole system working under about 90°C. All applicable L/S and bending angles were marked as the shadow area.

Table 5.2 Constants in Eq. 11 at 3 current levels

	I=0.1A	I=0.35A	I=0.7A
a_1	2.0e-4	1.1e-1	1.7e-1
a_2	1.2e-3	1.3e-2	1.9e-2
a_3	1.6e-1	1.6e-1	2.4e-1
a_4	9.9e-1	9.9e-1	1.5e-1

It is observed that the maximum temperature of the system increases with higher bending angle and higher L/S value. This can be attributed to the electrical resistance increase in the Al trace. It is also shown that at a small current level, maximum temperature less depends on bending angles. It can be explained by the fact that heat generated by resistance increase due to bending of the trace is more pronounced when the current level is higher. This leads to design rules of smaller L/S value should be adopted when the bending angle increases. It is also clear that with higher current input, the available L/S range is narrower. Another design rule is then concluded that L/S value less than 2 should be taken when a large current is expected in order to allow the substrate to bend from 0° up to 90°. With the help of the contour plots shown in Fig. 5.13, it could save a lot of time for designers to find the suitable range of L/S value at typical current levels in LED packages at different bending angles.

Furthermore, with the derived $\Delta T = f(L/S, \theta)$ relations and the model presented in Eq. 5.6, the effects of trace cross-section area S and bending angle θ on the Mean Time To Failure (MTTF) at a constant trace length 200 μm caused by electromigration were investigated. The resultant equation is shown in Eq. 5.12.

$$MTTF = \frac{S \cdot \exp[\frac{E_a}{k(\Delta T+25)}]}{5\times10^{-13}\cdot(\frac{I}{S})^2} \qquad (5.12)$$

Fig. 5.13 (a2), (b2) and (c2) demonstrated three contour plots shown the effects of S and θ on MTTF at 3 different current levels (0.1 A, 0.35 A, and 0.7 A). It is illustrated in the figure that at larger current level, the effect of cross-section area S on MTTF is stronger. It is due to the fact that large current level will generally result in larger temperature increase in the trace, which is more efficient to reduce the time to failure as a result of electromigration. Similarly, the effect of bending angle on MTTF is more pronounced when the current level is larger as well.

Similar patterns and relations were also found between contour plots of ΔT and MTTF as a function of geometric parameters and bending angles at the same current level. That indicates the importance of the impact of ΔTon the electromigration behaviors of interconnects. In addition, the safe zones of Fig. 5.13 (b1) and (c1) are quite comparable in size, while the safe zones of Fig. 5.13 (b2) and (c2) have deviated from each other a lot. It is evidence of the higher sensitivity that MTTF has to geometry changes and bending angle modification.

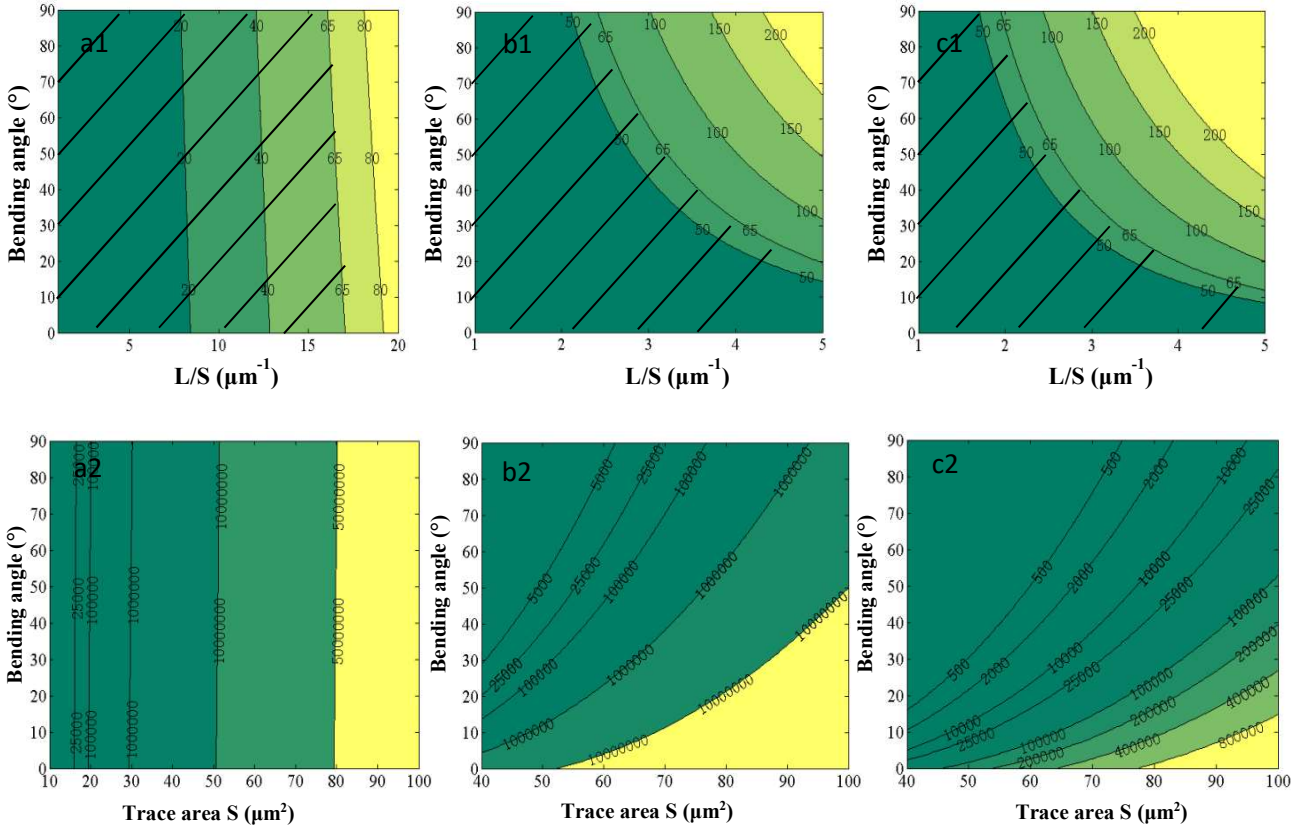


Fig. 5.12: Contour plot of temperature difference at current inputs of 0.1A (a1), 0.35A (b1), and 0.7A (c1) with different L/S geometric inputs. Contour plot of MTTF difference at current inputs of 0.1A (a2), 0.35A (b2), and 0.7A (c2) with different bending angles.

For this analysis, a threshold value of 25000 hours was adopted, which is commonly accepted as a minimum expected lifetime of an SSL package. In order to compare the safe zone under different current levels, L/S values were recalculated according to the S value in the x-axis for contour plots in Fig. 5.12 (a2,b2 and c2). Although the patterns are similar between two contour plots at the same current level, the safe zones in the contour plots are not exactly the same. It seems that in order to fulfill the lifetime requirement, less possible combinations of L/S and bending angle can be utilized than those derived according to maximum temperature allowed. Therefore, to determine the optimized geometry and possible bending angles of the RFR substrate in SSL application, it is suggested that MTTF criterion is checked first.

As already indicated in the previous paragraphs, this study delivered a fast and reliable way for designers to check if the new design meets the main requirements which are commonly need to be fulfilled in the SSL industry. For instance, when the bending angle is 90 degree, in applications of mid-power LEDs (100mA), the ratio of Aluminium thickness vs total Polyimide thickness is most preferably 0.14. In applications of high-power LEDs (350mA), the ratio is most preferably 0.3.

5.3 Rigid/Flex Package Design

Based on the flexible interconnects, a wafer level package of LED system package was designed. The total size is 9 by 24 mm, which follows the volume limitation of traditional G4 halogen lamps. The LED chips are placed inside the etched cavities on silicon islands and can be wire bonded or flip-chipped to the designed interconnect. The cavities are covered with aluminum to optimize the optical properties of the foldable package. The package proposed has five silicon islands, four acting as sidewalls and top cover with cavities to place LED dies, connecting by Polyimide/Aluminium flexible hinges. Two handling tiles are designed for the convenience of assembly.

Substrates comprise cavities covered with a reflective coating and LED dies in the middle. We found it to be an advantage to make a slope in the range between 30 and 60 degrees (for improved optical emission). Light emitting diode (LED) dies are placed in cavities covered with aluminum for optical management. With such packages, it improves light uniformity and reduces volume for solid state lighting applications.

The dimension of package interconnects and LED cavities in detail is shown in Fig. 5.13 and 5.14.

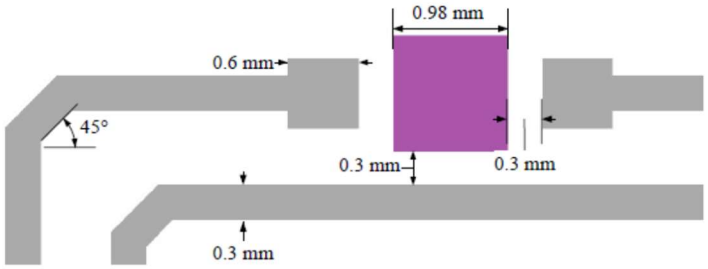


Fig. 5.13 Dimensions of package interconnects and LED cavities

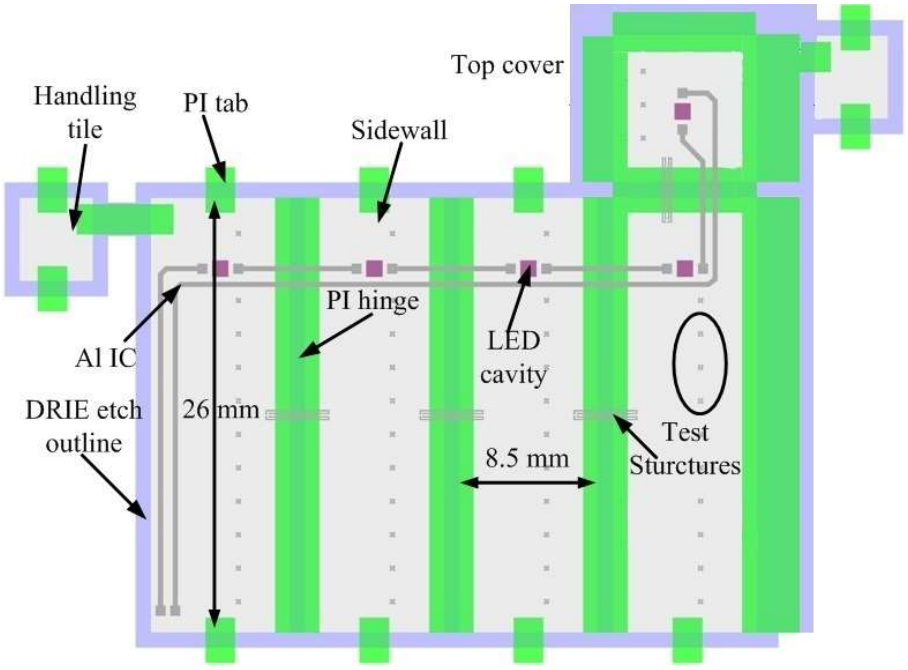


Fig. 5.14 Front-side layout of proposed WLP design

The WLP processed in 2D is compatible with traditional IC processing. Flexible interconnects are fabricated using flex-to-rigid technology, in which metal films are encapsulated between two layers of polyimide material of equal thickness, therefore the metal is in the neutral bending plane, where tensile and compressive forces are cancelling each other out.

The fabrication process of the package is shown in Fig. 5.15.

1. Flexible interconnect fabrication mentioned above.
2. Reflector cavities are etched for LED die placement. The sidewalls are covered in light reflective layer (e.g. aluminum).
3. LED dies are placed in cavities, connected through wire-bonding process or flipchip, and encapsulated.

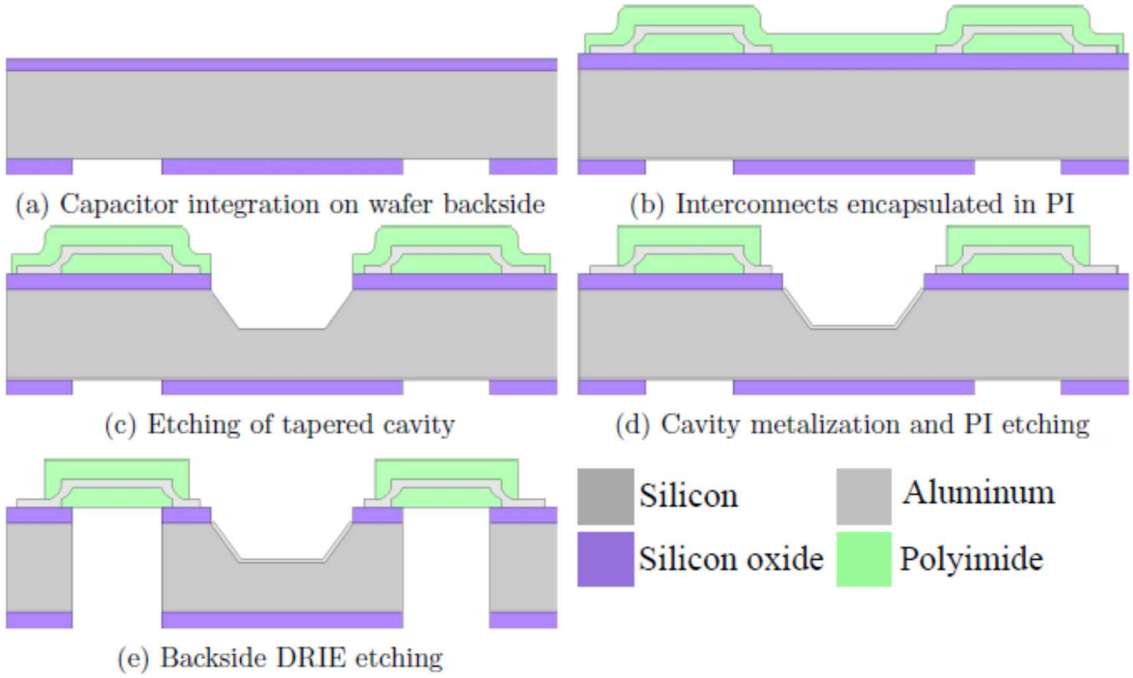


Fig. 5.15 Processing flow of 3D WLP package

5 LEDs with phosphor were then connected by wire bonding, covered with silicone and measured lumen output, as shown in Fig. 5.16. The phosphor is to convert blue light into white, but not optimized specifically. The prototype was released from a silicon wafer and then bent. We have demonstrated the assembly process according to the invention for a 26mm*8.5mm*8.5mm (H x W x L) package, the input power is up to 2W with 90 lumen output. All processes are compatible with traditional IC and MEMS processing, which means it has great potential for sensors and other electronics integration. The backside of islands is used for passive component integration to be used with driver circuitry thereby eliminating bulky discrete components. The critical working temperature of such package is up to 150°C.

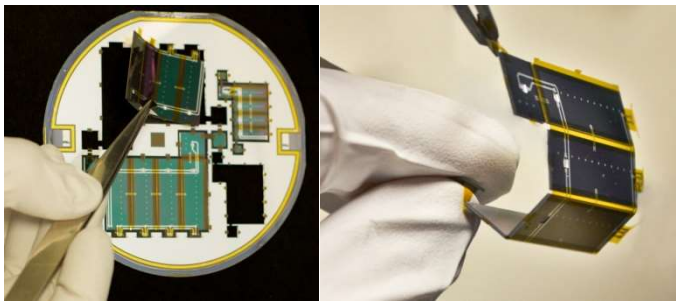


Fig. 5.16 Release and folding of the prototype.

A fixture with 26mm x 8.5mm x 8.5mm (H x W x L) as shown in Fig. 5.17 is designed for self-alignment of assembly. With such flexible package, it is important to accurate assembly it to 3D accurately. A vacuum clamping structure is designed to aid the folding procedure for automatic assembly. Such fixture enables the assembly procedure to be automatic. With such structure, LED packages can be processed in 2D and assembled to 3D with a various number of silicon islands (4 silicon islands in this specific case). With vacuum pipes inside the fixture, the assembly from 2D to 3D can be automated. Two vacuum inlets, with 5 vacuum holes on every sideway are designed for accurate alignment.

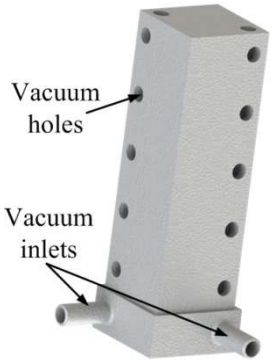


Fig. 5.17 3D rendering of the folding structure

The assembly process is demonstrated in Fig. 5.18:

a) Structures are released from the substrate wafers, by shallow dicing of polyimide strips.

b) Devices are folded to make 3D shapes around a heat dissipation structure (e.g. heat sink).

c) Put Polyimide on areas marked by A, B, C, and D. Then glue with areas marked by a, b, c and d, respectively. Devices are glued by polyimide and then cure in 400°C for 3 hours. (shown in Fig. 5.19)

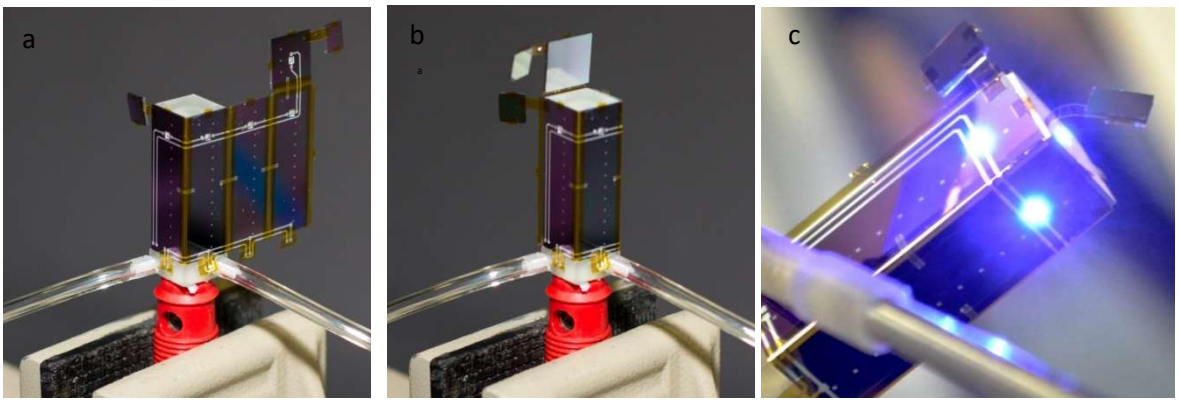


Fig. 5.18 Package folding around heat dissipation structure

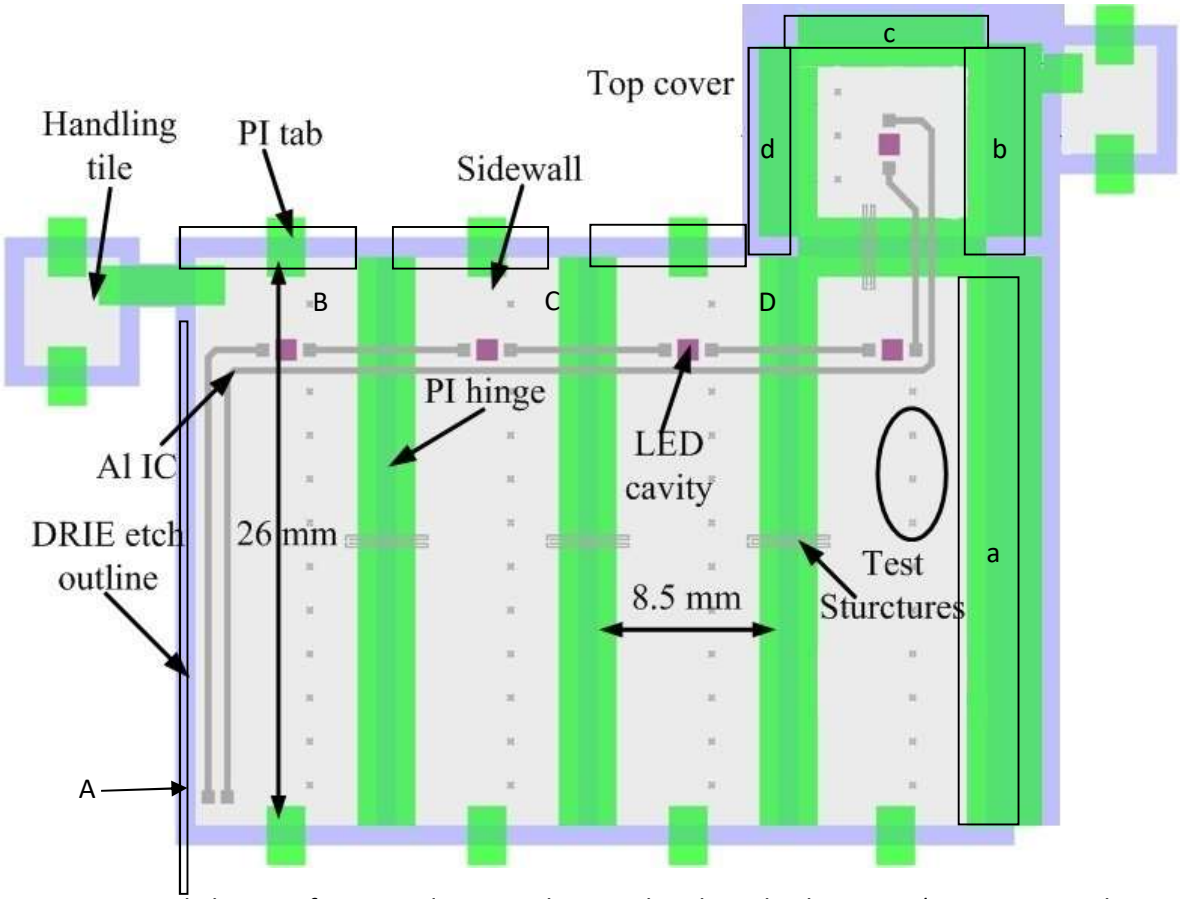


Fig. 5.19 Front-side layout of proposed WLP package with polyimide glue areas (A, B, C, D to a, b, c, and d, respectively)

Vacuum clamping was used to aid with the folding procedure. After folding, the package was still operational. The package can be finally released after gluing by polyimide by turning off the vacuum.

With the above-mentioned process, a novel WLP flexible package is fabricated (as shown in Fig. 5.20). Since flexible hinges have different thermal expansion coefficient with the silicon substrate, such packages will have the "breeze" effect when heated up. The flexible hinges made with mainly Polyimide will help to reduce the thermal shock effect since it can absorb some tension caused by thermal

expansion (as shown in Fig. 5.21). This will greatly increase the reliability for such packages, especially for solid state lighting applications.

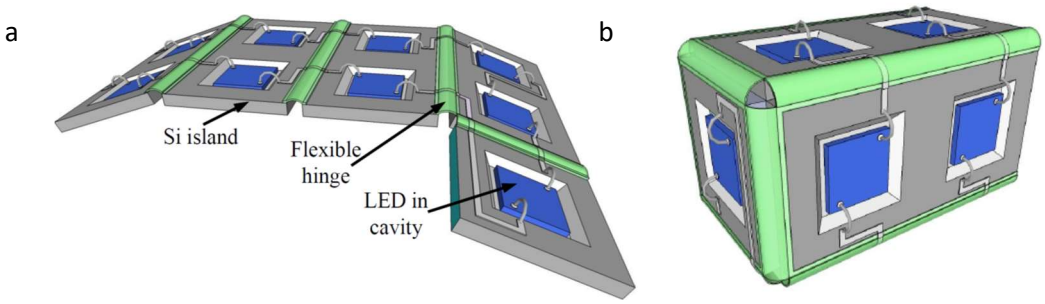
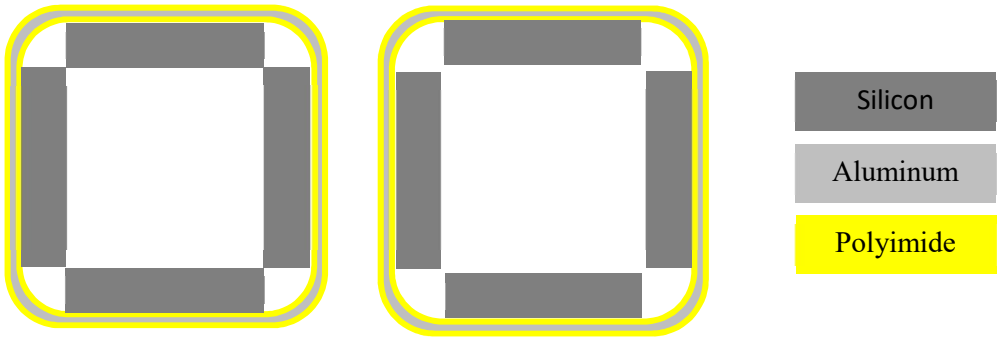


Fig. 5.20 Silicon based flexible WLP package concept (a: unfold; b: folded to form a cuboid)



a: room temperature b: high working temperature

Fig. 5.21 Cross-section of the flexible WLP package working under room temperature (a) and high working temperature (b). The flexible hinges expand more than silicon substrate under high working temperatures.

The final prototype has LED located in cavities with a light reflection layer, and flexible hinges connecting silicon islands with embedded Aluminium interconnects. The flexible interconnect was designed to handle current that is needed for the mid-power LEDs. Silicon-based integration can be easily merged with such flexible hinges. In this prototype, more than 80% substrate area is available for further integration.

The main application of the designed WLP package is in general for miniaturized SSL, such as LED retrofit G4/G9, automotive LED lamps, or decorative LED lamps. With the 3D folding interconnections, it can reach better light uniformity. With embedded electronics, the volume of the package can be further decreased. The silicon substrate can also be utilized for combining cooling structures, such as heat pipes. The auto-assembly structure enables such package for mass production. The lumen output and input power can be further tuned by replacing the current LED die with others, or a different driver circuit design.

5.4 Package Characterization

5.4.1 Flex/Rigid Package Characterization

With such design, the Rth of the package is 2.3K/W. Silicon substrate possesses superior thermal conductivity comparable to certain metals 148W/mK (Al – 160W/mK). Therefore it can efficiently dissipate heat away from the LED chip. Thermal distribution was measured using IR imaging (Fig. 5.22). It was first measured by placing the packages on a steel chuck. To demonstrate heat dissipation at elevated temperatures a piece of cardboard was placed under the package, which reduces conductive heat transfer.

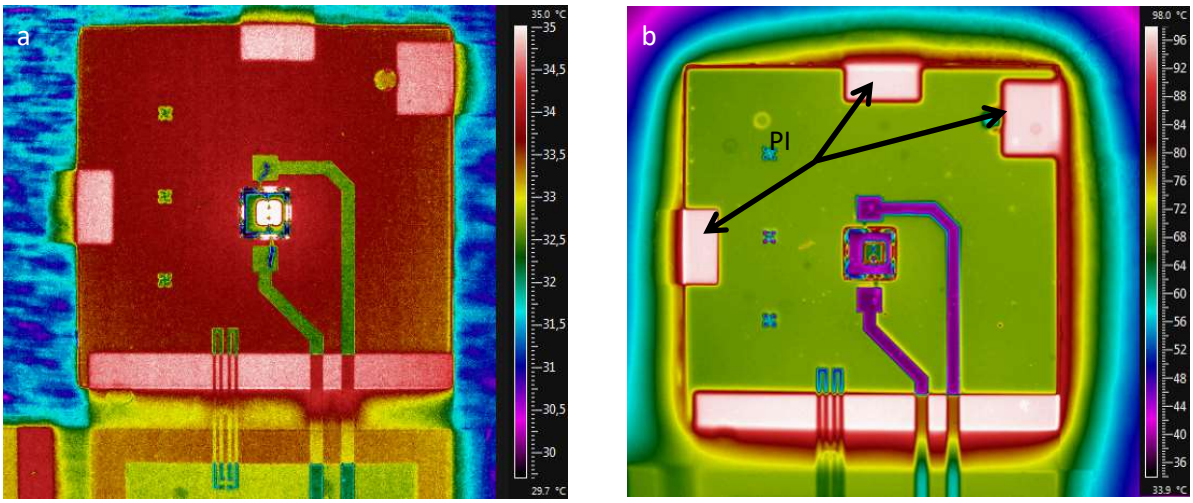


Fig. 5.22 thermal image of WLP (a: on metal chuck after 20 min; b: on cardboard as a thermal insulator after 20 min)

The metal appears colder due to different emissivity values than Si, for the same reason PI seems to be hotter, however uniform heat spreading across the surface of the package is evident.

With LED dies (CREE TR5050), the luminous flux of the device varies as a function of temperature is shown in Fig. 5.23 (a). The influence of the luminous flux of the device caused by input power has also been measured. Since 85°C is generally considered to be a critical temperature of SSL applications, the package can work with 2W input to reach 85lm output.

As seen from Fig. 5.23 (b), the final lumen output of such device was greatly influenced by temperature, thus thermal management is crucial for high lumen output. For instance, microchannels or other MEMS heat dissipation structures can be further integrated on a silicon substrate, for a better performance.

The main application of such designed WLP package is in general for miniaturized SSL, such as LED retrofit G4/G9, automotive LED lamps, or decorative LED lamps. With the 3D folding interconnections, it can reach better light uniformity. With embedded electronics, the volume of the package can be further decreased. The silicon substrate can also be utilized for combining cooling structures, such as heat pipes. The auto-assembly structure enables such package for mass production. The lumen output and input power can be further tuned by replacing the current LED die with others, or a different driver circuit design, as discussed as follows.

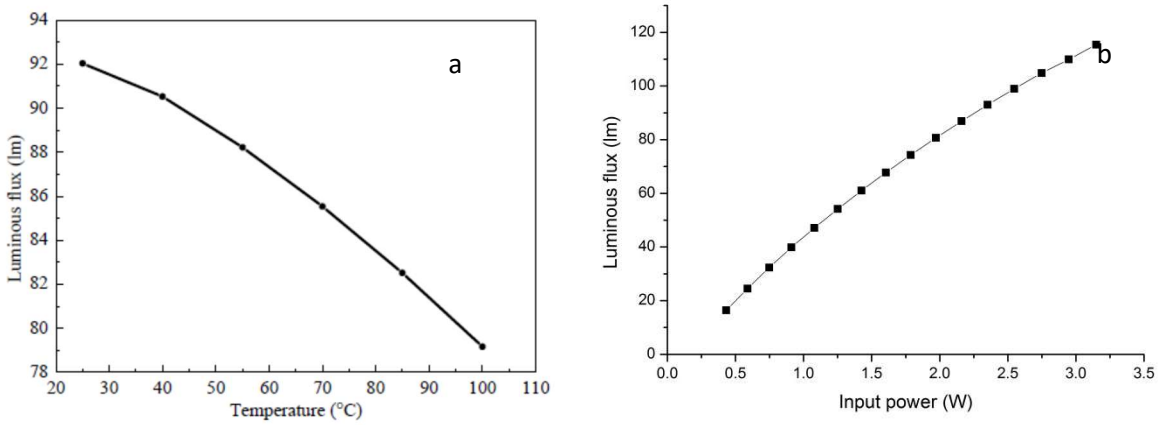


Fig. 5.23 Luminous flux of the device vs: a) temperature; b: input power

5.4.2 Flex/Rigid Package Characterization with integrated driver circuit

By incorporating flexible interconnects a 3D form factor of the SSL module can be achieved. The flexible interconnects consists of aluminum encapsulated in polyimide. The flexible interconnect allows a 3D form factor design and integration of more than one LED chip. This offers advantage of both monolithic integration of devices and 3D wafer level packaging of LED module using silicon as the substrate. Using the BiCMOS7 process in which the Schottky diodes and rectifiers are fabricated, a design proposal for integrating both rectifiers and driver related electronics on a rigid to flex substrate is proposed. A 3D illustration of retrofit G4 module is shown in Fig. 5.24. The proposed integrated and rectifier a flex to rigid substrate is shown. In the integration with flex to rigid substrate, the BiCMOS7 fabrication process step as discussed in the previous chapter is done to integrate the rectifiers and drive using Schottky diodes.

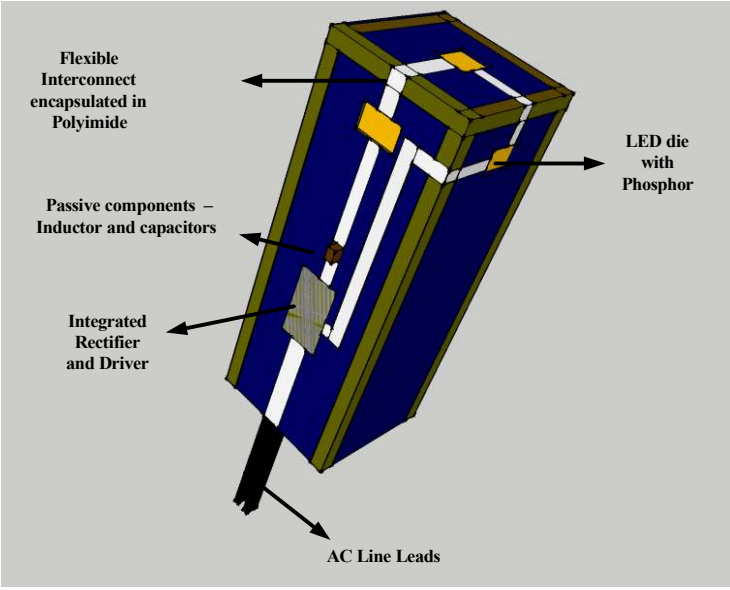


Fig. 5.24 3D model of monolithically integrated rectifiers and drivers on to Flex-to-rigid substrate

The great advantage of such wafer level integrated package is the small form factor due to folding. Meanwhile, it keeps the freedom from silicon integration, which allows the system to be easily tuned by different application purposes. However, to make the best use of a silicon substrate, an optimized design is still in need. With the integration of more and more on-chip devices, aluminum interconnects need to be further optimized, according to the design rule mentioned in Chapter 3.

The flex/rigid substrate with integrated LED blue dies as discussed in Chapter 3 were applied in the characterization of the integrated driver circuit. 2 designs of such package were fabricated, as shown in Fig. 5.25. Package B is the same size of the G4 LED design as mentioned at the beginning of the previous chapter (Fig. 4.1), with 4 long panels. Each panel size is 26x9mm^2. Package A was designed to be 50% smaller physical dimensions compared with Package B. For each design, the rectifier was off-chip integrated. This is aimed for easy check each component during characterization.

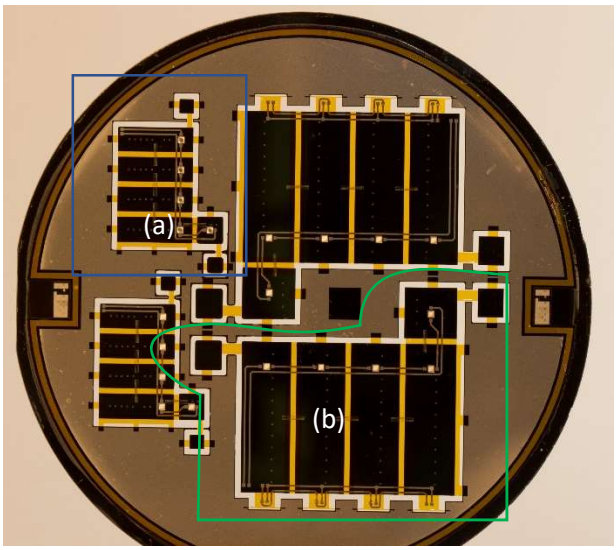


Fig. 5.25 Designs of 2 sizes of flex/rigid substrate (a: 11x5mm2 per panel; b: 26x9mm2 per panel).

To combine such fabrication process with flex/rigid substrate, the rectifiers, NPN, MOS devices and related driver circuit need to be firstly processed in the BiCMOS7 process up to the metal 2 - M2 layer. This layer of aluminum can be combined with the aluminum layer of the flexible interconnect. Secondly, a thermal oxide need to be grown on the back of the processed wafer, to pattern at the regions required for interconnect bending. Next, the 2 polyimide layers and the Aluminium is then patterned. Finally, back etch of the silicon is done to release the polyimide hinges. A detailed analysis and fabrication process is not included in this thesis. Only a design proposal is made. It is intended for future processing. Using flexible interconnect gives the advantage of integrating more LED dies on a single package.

(A) Inductor-free Linear Driver

This no inductor-wafer level integrated linear driver is using current mirror based on two NMOS devices. In the current mirror the drain current across the transistor M1 is mirrored to the drain of M2. The current across the M2 is set by the width ratio of M1 and M2. In this example the current across R1 is 2mA. The ratio of widths of M2 and M1 is 200. The current is multiplied by this factor and the current across the LED is about 200mA. The circuit simulation of this current mirror is shown in Fig. 5.27 (a). The

current is about 180mA. The circuit provided uses all the components that can be fabricated in BiCMOS process to achieve a fully integrated rectifier and driver.

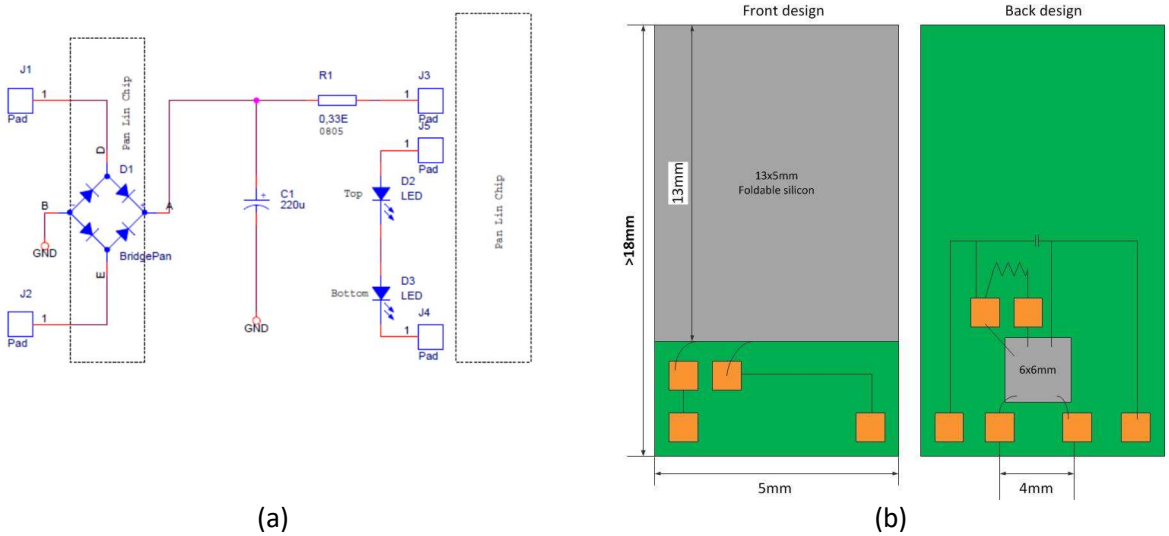
In the process, we designed different M2 for 120mA, 180mA, and 350mA corresponds to the layout dimensions of 2 by 1400, 2 by 2000 and 2 by 4000. Such device was fabricated by BiCMOS process together with the rectifier in-house on wafer level.

The disadvantage of the linear driver is that they are inefficient and consume more power and dissipate a lot of heat. The switch mode driver can achieve higher efficiency when compared to linear driver.

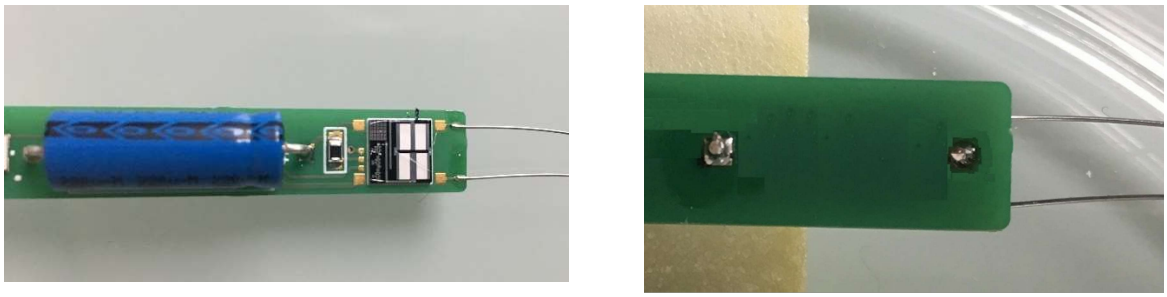
It worth to mention here that high dielectric materials and trench capacitors were studied in this work. However, the experimental results did not meet our expect due to fabrication condition limitations. In the end, capacitors from IPDiA company were chosen. Such wafer level capacitors can provide high capacitance density, and connected through wire bonding.

Since the capacitor is most bucky component in the system. One of the design rules is to reduce the required capacitance by the circuit design. The key issue for such approach is to tackle the I/O power imbalance, e.g. modulate the line input current, pulsating current with relatively large ripple, or adopt other energy storage elements such as inductors to handle the power difference, as shown in (B) Switch mode Buck driver.

For easy characterization, the rectifier fabricated in Chapter 4 was wire-bonded on a PCB together with other off-chip components. The basic layout is shown in Fig. 5.27. The substrate chosen for this driver is 11x5 mm^2. Since no inductor was needed in this circuit layout, the volume is miniaturized by 50%, compared with the original G4 design mentioned in Fig. 3.1.



(a) (b)



(c) (d)

Fig. 5.27 (a) Circuit layout of Linear driver; (b) PCB layout for design A; (c) PCB front side; (d) PCB backside.

The lumen output, compared to the results mentioned in Chapter 3, is shown in Fig. 5.27, given the input of 12V AC provided by an electronic dimmable transformer. The transformer applied in this test was model ET105D of Eterna. The silicon-based flex/rigid substrate lumen output was measured directly under DC with a constant input current of 120mA, as a comparison. The higher the temperature is, the lower lumen output it suffers. As a result of that, no heatsink/dissipation designed for such a prototype. Since silicon substrate is integrated in this design, passive heat dissipation methods, such as heat sink can be further designed. Also, active heat dissipation methods such as microchannels with cooling liquid are also promising. It worth to mention here that the heat dissipation based on a silicon substrate is out of the research scope of this work.

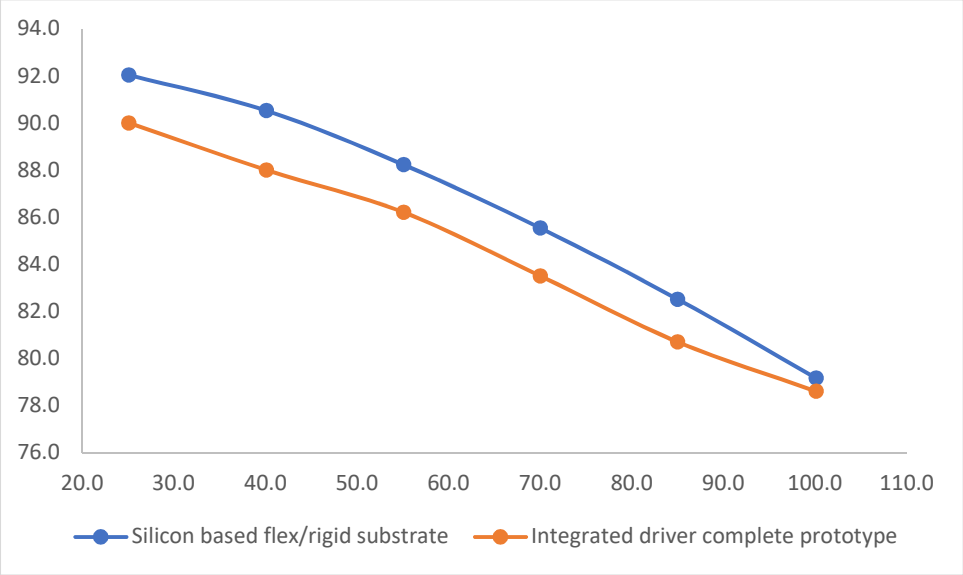


Fig. 5.27 Lumen output comparison of silicon-based flex/rigid substrate and prototype with full integrated driver

(B) Switch Mode Buck Driver

The other wafer level integrated driver is switch mode buck LED driver, as shown in Fig. 5.29. The switch mode driver can achieve higher efficiency when compared to linear driver. A buck driver is a step down DC converter. This driver configuration is used if the output load voltage is less than the input voltage. The buck driver requires inductor and capacitor components for energy storage.

Control IC AL8805 was supplied by diode cooperate and D1 ss14M was supplied by Taiwan Semiconductor. With such configuration, it also can be easily extended to smart sensors connections, as shown in Fig. 5.29.

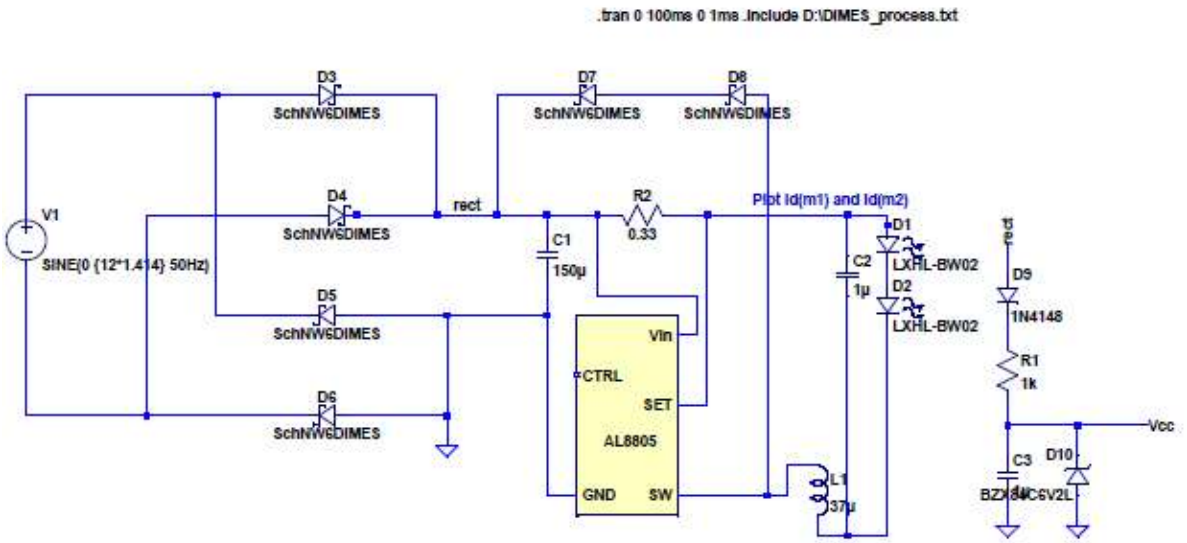


Fig. 5.29 Switch mode Buck LED driver with rectifiers using Schottky diodes and smart sensor connections

In this circuit design, an inductor is necessary. Therefore, the flex/rigid substrate of 26x9mm^2 per panel was chosen, to provide enough space for inductors, sensors, etc. For easy characterization, the rectifier is still wire-bonded to PCB substrate. The temperature sensor was integrated also off-chip, to characterize the temperature of PCB substrate. The volume of such circuit design is the same compared with the design mentioned in Fig. 3.1. The circuit layout and the PCB design for silicon panels to be wrapped were shown in Fig. 5.30.

Lumen output was also measured, with the same method mentioned for linear driver prototype. Since buck driver circuit is more energy efficient, the lumen output is higher than linear driver for lower temperature conditions. However, due to more components were involved in this circuit design, the heat is more difficult to dissipate. Therefore, the lumen output of 70 and 80 degree is lower than the linear driver, as shown in Fig. 5.31. Smart sensor control was also integrated in this buck driver prototype. The set up was to lower the current input when the temperature is higher than 80 degrees. As a result of that, a sharp drop in lumen output was observed when the system reached 100 degrees.

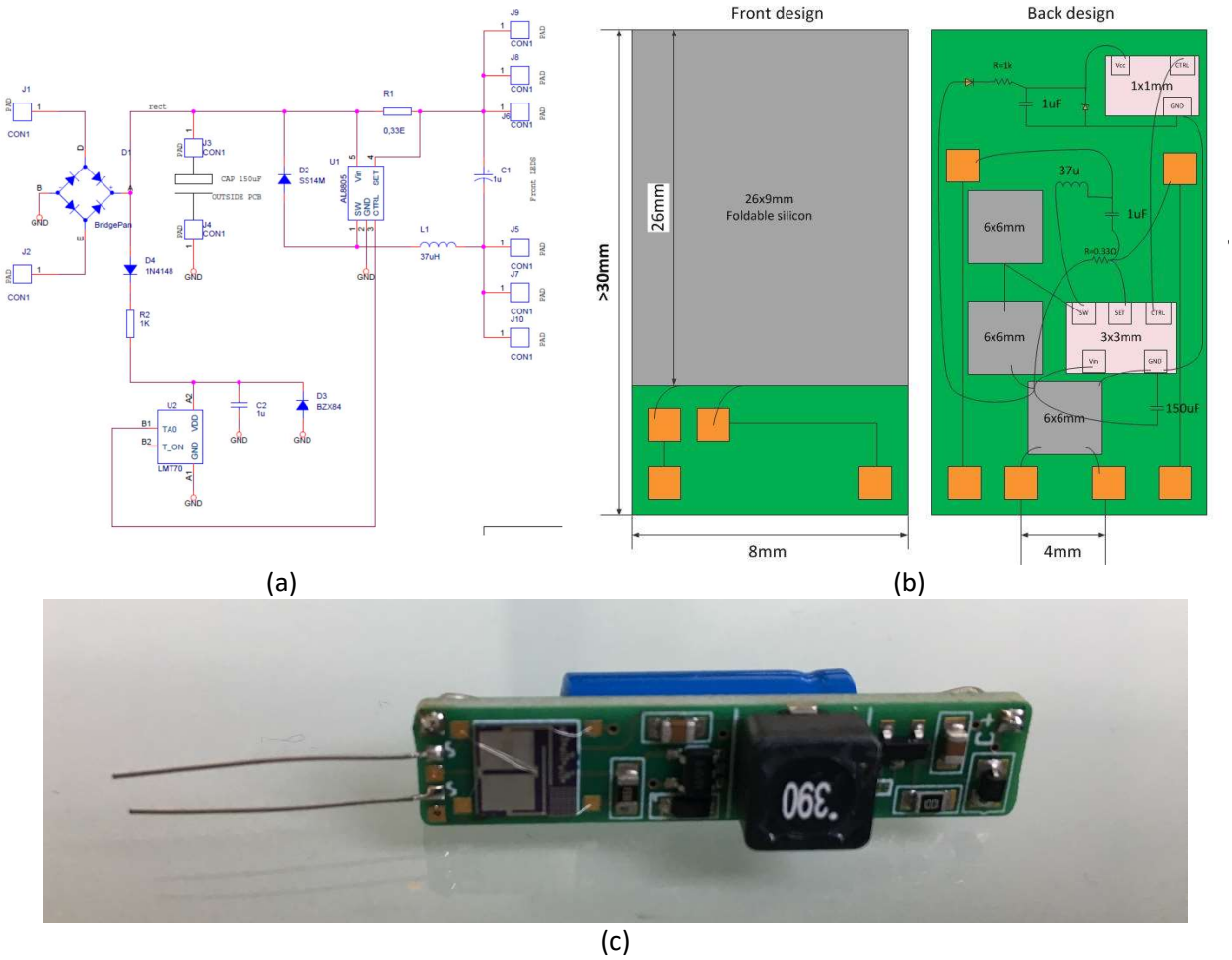


Fig. 5.30 (a) Circuit layout of Buck driver. (b) PCB layout for connecting foldable silicon substrate of design B; (c) PCB prototype

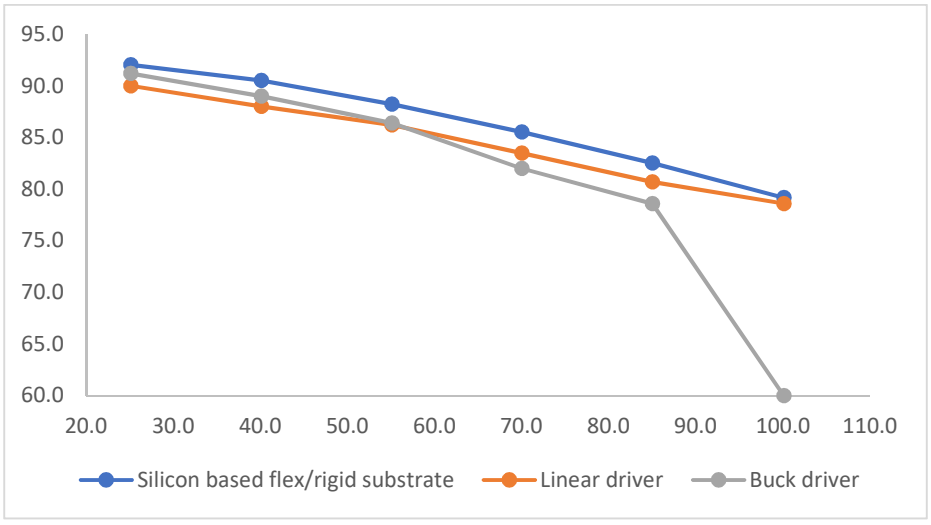


Fig. 5.31 Lumen output comparison of silicon-based flex/rigid substrate and prototype linear driver and buck driver layout.

It is worth to mention here that these two prototypes are tested without proper heatsink/heat pipes. There are plenty technologies already developed for silicon-based heat transfer techniques. With proper integrated thermal management devices, the lumen output can be further optimized.

5.5 Conclusion

In this chapter, A 3D wafer level package (WLP) includes silicon substrate with Polyimide/Aluminium flexible interconnects and cavities covered with aluminum to reflect light is designed for miniaturized Solid State Lighting (SSL) Applications such as e.g. G4 capsule. It is an advantage that the package can be easily mass-manufactured in 2D and subsequently assembled to 3D WLP by flexible interconnects. The designed flexible hinges enable the device to endure high thermal stress. This work describes a number of critical technical details such as ranges of geometrical dimensions, aspect ratios, and material choices. On one hand, a LED light emitting device was designed and tested. On the other hand, the related manufacturing method was also taken into consideration. Therefore, an automatic assembly method is also designed for such packages. Light emitting diode (LED) dies are placed in cavities covered with aluminum for optical management. With such packages, it improves light uniformity and reduces volume for solid state lighting applications.

Based on the physical dimension limitation, desired power input and expected lumen output, two drivers were designed based on this 3D wafer level package with flexible interconnects with on-chip components such as a rectifier, and off-chip components such as capacitors. One is a linear driver with advantages of fewer components, inductor free, and volume saving. The other is buck driver with advantages of higher power efficiency and the ability of smart control. Prototypes were build based on such topologies, and characterized for the lumen output. The rigid/flex substrate has shown the potential for device integration, and connection to external components. It is promising to further develop such platform to reach higher lumen output and smart control of miniaturized solid state lighting applications with proper thermal management methods such as heat pipes.

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Chapter 6 Flexible Substrate Based Presence Sensing Antenna

6.1 Flexible Substrate

Flexible electronics industry is expected to reach around $17.2billion by 2024 [1]. The interest in flexible electronics arises with merging the advantages of silicon-based technologies with low-cost manufacturing processes. The market is primarily driven by strong demand for consumer electronics, such as wearable electronics, smartphones, tablets, e-readers, etc. Sensors are one of the areas where flexible electronics are emerging in more commercial and industrial areas, from medical, automotive and aerospace to cosmetics and packaging and much more. Flexible substrate based sensors enable the sensors to be wearable, therefore attract increasing attention.

Based on the flex/rigid package developed in the previous chapter, it opens the door of polyimide (PI) based electronics integration. Therefore, PI-based presence sensor was selected in this work.

6.2 Presence Sensor

Presence sensors work according to a similar principle as motion detectors: thermal radiation is detected in the detection area. Presence sensors convert the thermal radiation of human beings into a measurable electric signal to switch on the luminaires. Since a significant part of thermal radiation energy ranges in the infrared region, infrared detectors have been widely used to identify the emitted radiation and consequently the temperature. However, infrared detectors suffer from high attenuation in presence of obstructions while their operation is strongly dependent on human's movement and influenced by environmental conditions. Therefore, a new technology is introduced based on radio frequency (RF) sensors instead of infrared for presence detection applications, as shown in Fig. 6.1

This technology is capable of detecting real human's presence based on the Doppler principle and the long wavelength can penetrate possible obstructions such as clothing, smoke etc. Among the RF frequencies, research on millimeter wave (mmW) is drawing increasing attention for presence sensing. MmW is a narrow frequency range (30-300 GHz) at the upper edge of radio frequency which provides wavelengths in a scale from 1mm to 1cm, as shown in Fig. 6.2. Fundamentally, this wavelength allows mmW to travel through clothing, glass, smoke etc with negligible attenuation. The importance of this property leads to high detection accuracy even under no light conditions or during winter that over layered clothing is required. As a matter of fact, mmW sensors have the advantage of detecting real human's presence regardless of the environmental conditions.

Passive mmw detection systems use thermal radiation emitted in millimeter wave range (30GHz-300GHz) by objects in the area. Their function requires a temperature difference between the body and the surroundings. This can result either from the difference in temperature, with the object having a higher temperature than the surroundings but similar emissivity or from the difference in emissivity with the object having higher emissivity but similar temperatures.

The radiation emitted by a human body is defined by its emissivity. In general, the emissivity depends on the dielectric constant of the skin and the subcutaneous layers. It increases with decreasing wavelength. Human's skin has an average emissivity of $\varepsilon = 60$ in the millimeter wave region [2]. At an average temperature of $T_0 = 310K$, the surface (brightness) radiometric temperature of the body is obtained by: $T = \varepsilon \cdot T_0$, which is the temperature that a blackbody must be in order to produce a certain amount of power.

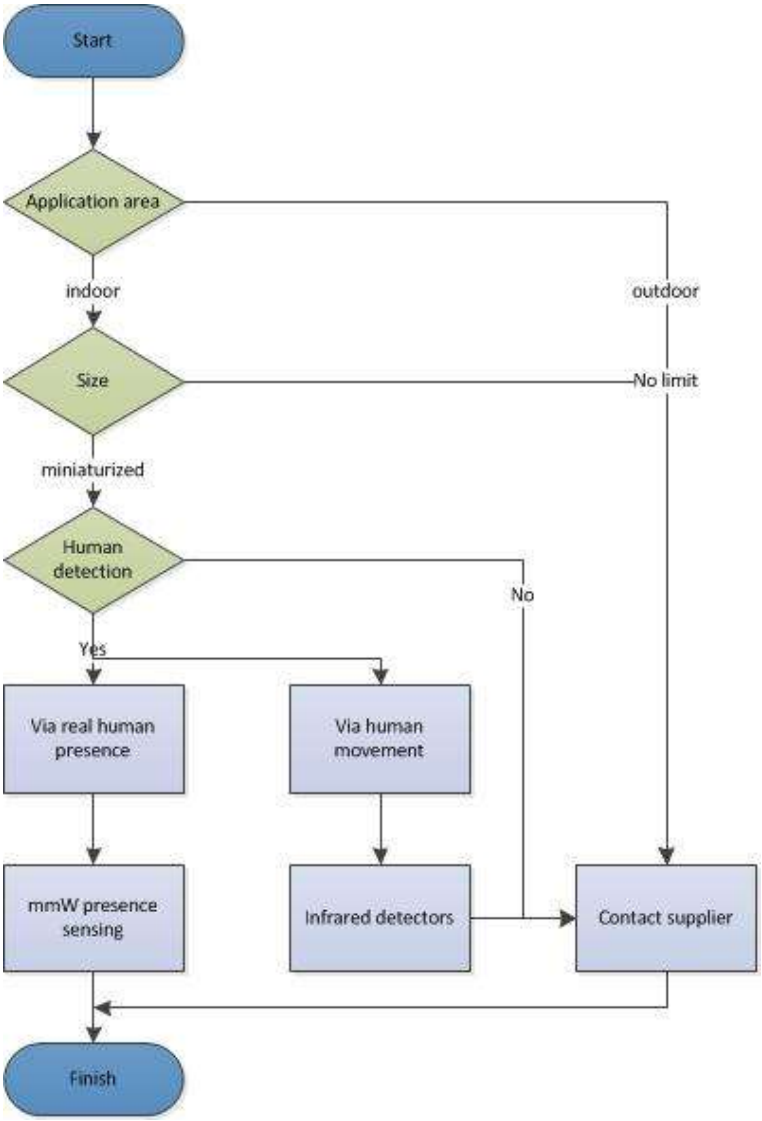


Fig. 6.1 How to choose a presence sensor for miniaturized solid state lighting applications

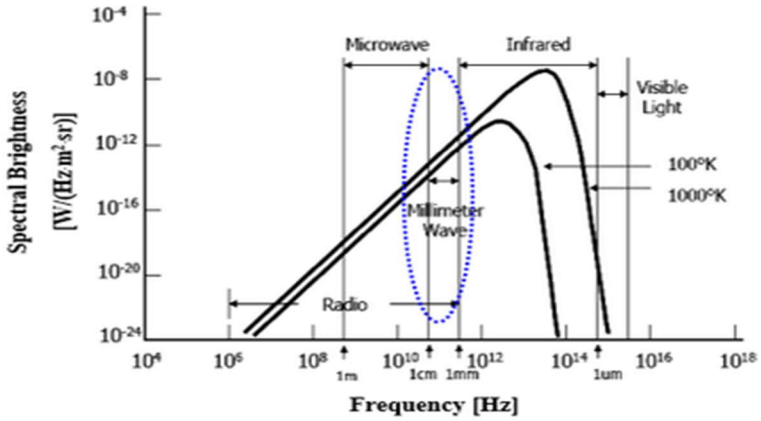


Fig. 6.2 Spectral brightness as a function of the frequency (the dashed line indicates the mmw region).

Considering a human body temperature of $310K$ and a frequency of $27GHz$, Planck's black body radiation can be approximately described by Rayleigh-jeans Law for a grey body:

$$I_f = \frac{2f^2}{c^2} kT \qquad (Eq. 6.1)$$

Where I_f is the spectral radiance in $[Wm^{-2}Hz^{-1}sr^{-1}]$, f the frequency in Hz, c the light speed in ms-1, k the Boltzmann's constant in JK-1 and T the radiometric temperature in K.

For a narrow bandwidth the spectral radiance is given by:

$$I \approx \frac{2f^2}{c^2} kT\Delta f \quad [Wm^{-2}sr] \qquad (Eq. 6.2)$$

Taking into account the effective aperture transmitted by the human body At the power received by the antenna terminals of effective aperture Ar is given by:

$$P = \frac{1}{2} I A_r \frac{A_t}{R^2} - \frac{A_r A_t f^2}{R^2 c^2} kT\Delta f \qquad (Eq. 6.3)$$

Where R indicates the distance between the radiating source and the receiver and the term $1/2$ results from the antennas responding to only one component of polarization.[3]

The main challenge in the mmw frequency sensors design is the perturbation caused by signals generated by other devices. The system must isolate the human body signal. Human body is a self heat generation object resulting in a coherent radiation signal, on the contrary objects do not generate their own heat and consequently their radiation is a combination of a scattering reflection and thermal emission solar heat. The differentiation comes to the emissivity. A human body has a much higher emissivity in mmw region compared to that of other objects. This makes human body appear warmer than the surroundings. [3]

Human body exhibit higher temperature as the surroundings resulting in an increase of the emitted radiation intensity. The corresponding increase in temperature can be sensed by the passive mmw detector. This is achieved by the contribution of two main effects: the radiative transfer of electromagnetic waves and the bio-heat transfer. The latter is a combination of heat conduction and the heat transferred through blood. Both effects are important in detecting human's presence in both mmw and infrared region. Nonetheless dilution due to coarse spatial resolution makes mmw sensors more preferable.

6.2.1 Choice of Antenna Substrate

Most mmW sensors are usually fabricated on expensive substrates, e.g. Quartz substrate, or ceramic type of substrates (LTCC, Alumina) due to low loss [4,5]. These materials and the associated processing are typically expensive and can not transform to various surfaces. Therefore, this work focuses on the design and fabrication of a flexible, low profile sensor in the millimeter wave frequency region consisted of a coupled antenna.

Flexible substrates (i.e. papers, textiles, and plastics) make flexible electronics an appealing candidate for the next generation of consumer electronics. Needless to say, the nature of flexible wireless technologies requires the integration of flexible, lightweight, compact, and low profile antennas. At the same time, these antennas need to be mechanically robust, efficient with a reasonably wide bandwidth and desirable radiation characteristics. [6]

In this work, Kapton® polyimide film with a thickness of 127 µm was first chosen and then characterized to extract its relative permittivity, from transmission lines measurements. Transmission lines were realized on Kapton® film using photolithography. Coplanar waveguide (CPW) is the most preferable type of transmission line (TRL) because of its easy integration with microwave circuitry and low losses. Operating as a transducer between a free space wave and a guided wave, it is used as a feeding technique for transmitting the microwave signals. The patch antenna, the TRL and the ground plane are made of high conductivity metal.

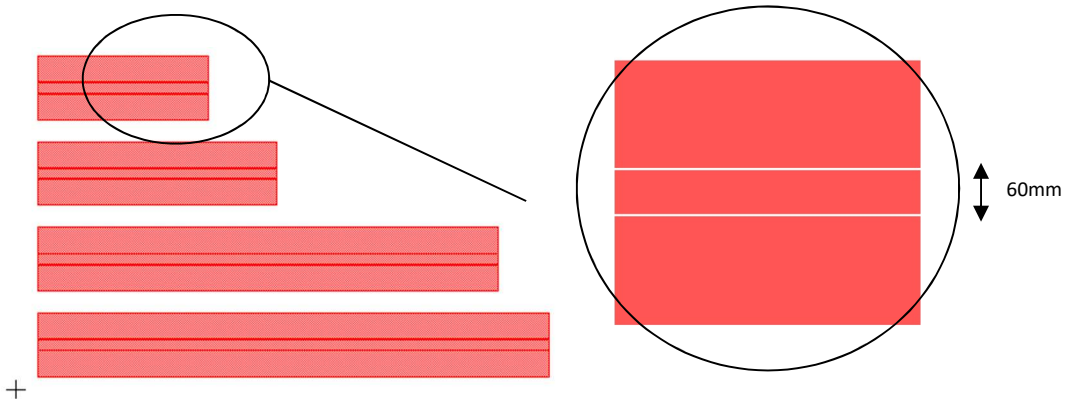


Fig. 6.3TRL structures for 1mm, 1.4mm, 2.7mm 3mm

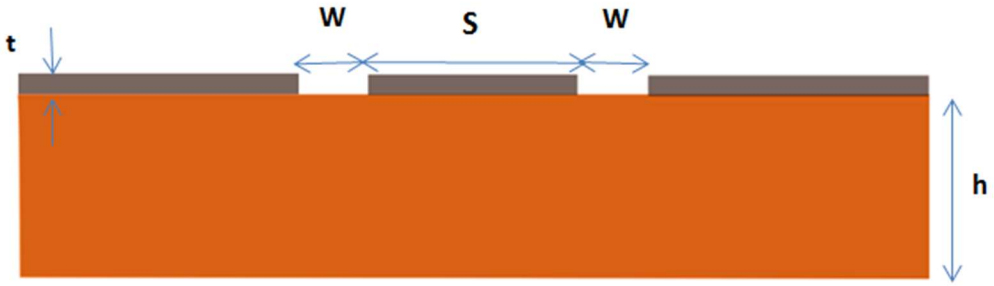


Fig. 6.4 Coplanar waveguide structure (CPW) on a polyimide substrate (PI)

As shown in Fig. 6.4, the CPW consists of, at least one, thin conductive strip and conductive ground planes sitting on top of a dielectric substrate with a permittivity ε_r, each one operating as a conductor. [7] Antennas can both transmit and receive microwave signals. The radiation of a transmitting antenna relies on the transition of a guided wave fed by the transmission line to a free space wave. On the other hand, receiving antennas rely on the exact opposite operation; the received space wave is led into the transmission line. Any radiating object can produce a signal which can be detected by passive antennas.

Based on such structure, transmission lines were realized on Kapton® film using photolithography. Measurements on Kapton® flexible substrate were carried out employing probes and using an Anritsu network analyzer operating at frequencies 20-60 GHz. The relative permittivity extracted from the data is illustrated in Fig. 6.5.

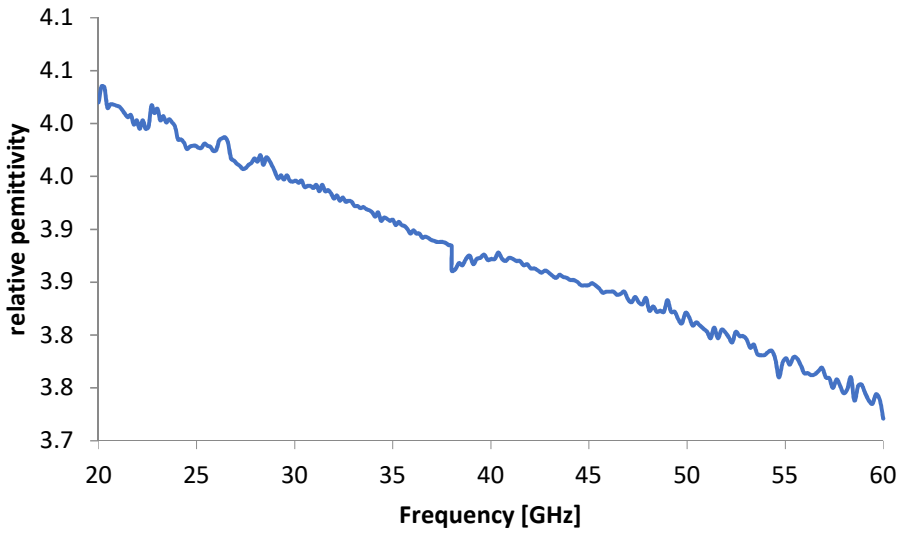
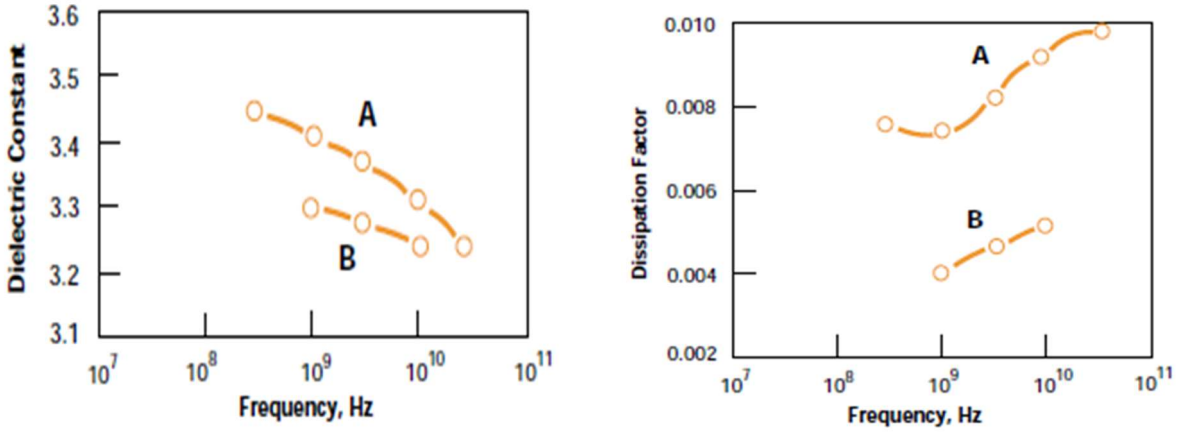


Fig. 6.5 Extracted relative permittivity of Kapton® film in the frequency range 20-60 GHz.

The dielectric constant and loss factor extracted by measurements were also verified with the values over frequency range of 20-60 GHz, according to datasheet of Kapton film. The nominal characteristics of Kapton® film were provided in data sheets and are illustrated in Fig. 6.6. Curve A represents the measured properties as received at 250C while curve B represents the measurements after conditioning the film at 1000C for 48h [13].



(a) (b)

Fig. 6.6 (a) Dielectric constant related to frequency; (b) Dissipation factor related to frequency, as given in the datasheet [8]

It worth to mention here that there are several techniques for substrate characterization. However, the most popular method is based on transmission lines together with the substrate material over a broad frequency range.

6.2.2 Choice of Operate Frequency

The main idea is the fabrication of a completely flexible sensor based on a $127um$ Kapton® polyimide substrate consisting of a coupled antenna with low directivity for wia der detection range. The device will be able to roll, stretch and bend according to the application needs. The system was selected to be

operated at a nominal frequency of $60GHz$. The extracted values for the relative dielectric constant as derived from Fig. vary from 3.7 to 3.75. These values are close to the nominal one derived from the data sheet. The estimated value of 3.7 will be assumed in the following as the relative permittivity of Kapton® substrate at 60GHz.

The atmosphere can be transparent at that frequency in millimeter region causing an attenuation peak ($0.016dB/m$) at around $60GHz$ due to the oxygen resonant absorption. In addition, this frequency allows the design and connection of low cost and small sized components, available in the market. The device is elaborated in details in the following chapters.

6.2.3 Choice of Antenna Type

Micro strip patch antennas are narrow band antennas consisted of a metallic patch on a ground substrate. Their technology has rapidly attracted the attention of academic, industrial engineers and researchers. Their low cost and low complexity mass production has made them suitable for variable wireless applications [9]. In addition, the transmission line and all the radiating elements can be implemented in the same substrate. From the market point of view, micro strip patch antennas have developed their own commercial target regarding the microwave systems such as mobile devices, intelligent vehicle highway systems, satellite communications etc.

Micro strip antennas have broadened the already existed field of antennas technology. Compared to other types of antennas, the micro strip patch ones appear to have a low profile (only a few mm thick) and low weight while their ability to conform and the fact that can be printed directly onto the circuit board makes them increasingly useful. In addition they do not require any via holes or shorting pins while their design allows the printing of both radiating element and ground plane on the same side of the substrate. [10] Last but not least, depending on the fabrication process and the material selection, micro strip patch antennas can be a low-cost technology.

On the other hand, their technology suffers from some serious drawbacks. When it comes to electrical performance the micro strip antennas are not the most preferable. Their narrow bandwidth (≤3%), the high feed network losses and the low power handling capacity have set a new research target. [11] To surpass those drawbacks researchers continuously come up with innovative designs and configurations.

The narrow bandwidth of micro strip patch antennas does not allow their use in applications where wide frequency ranges but small structures are required. There are variable broad banding techniques which increase the bandwidth by tuning the impedance value of the antenna. This can be achieved by varying the slot geometries or tuning stubs. Multilayer structure or stacked patches employs several layers of different dielectric constants between the upper patch, the lower patch and the micro strip line. This technique can efficiently increase the BW but results in thicker structure and more complex fabrication process. Another way to increase BW is by using coupled coplanar patches but this also leads to complex structure. The simplest broad banding technique is tuning the impedance by etching a slot on the patch. There are several slot shapes as shown in Fig. 6.7[10]. In this project a U-shaped slot antenna as described in [12] is being investigated.

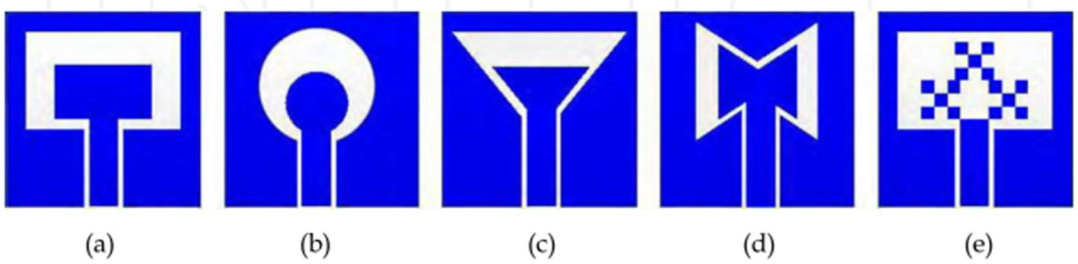


Fig. 6.7 CPW fed slots geometries and tuning stubs

A micro strip device can simply consist of a ground plane and a conducting layer in parallel separated by a dielectric substrate.[9] The ground plane is necessary to obtain unidirectional radiation since a slot antenna operates as a bidirectional radiator. The properties of the most suitable substrate are elaborated in the following section. In the field of interest, micro strip antennas had been developed to operate in mm-wave band at frequency up to 38GHz and their promising technology extended their performance up to 60 GHz. [9].

6.3 Antenna Design and Characterization

A rectangular, U-slot microstrip patch antenna was designed and simulated in HFSS 13.0. The design and the dimensions of the simulated structure are reported in Fig. 6.8 and Table 6.1. The structure was based on a 127µm thick Kapton® polyimide substrate using a 2um thick layer of Aluminum for the metal layers. Ground plane was implemented at the bottom side of the substrate to avoid radiation losses.

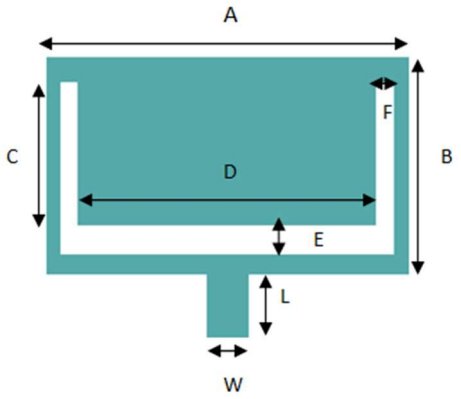


Fig. 6.8 Dimensions of the proposed antenna

Table 6.1 Dimensions of the designed antenna

Dimension	[mm]
A(width)	2.4
B(length)	1.44
C	1.16
D	2.15
E	0.2
F	0.125
W	0.275
L	14

A single rectangular microstrip coplanar waveguide fed antenna was then simulated, fabricated and characterized at 60 GHz. The passive components were based on a 127µm thick Kapton® polyimide substrate using a 2 µm thick layer of Aluminum for the metal layers and fabricated using lithography technology. Kapton® film itself is a rather tricky material to process and needs caution. Polypropylene carbonate (PPC) was found the most suitable material to attach the film on the wafer achieving strong adhesion and easy delamination after process completion. High attention is needed in the attachment of the film since partial adhesion hampers the upcoming etching step. Overheating of the film during dry etching results in photoresist damage and partial pattern of the structure. As a matter of fact partial dry etching followed by short time (1min) wet etching finalizes the structure. The process is as follows: (a) primer/PPC spin coating and Kapton® film adhesion, (b) aluminum evaporation (2um), (c) 3um positive photoresist layer, (d) UV exposure, (e) photoresist development, (f) etching process, (g) resist stripping, (h) film separation. Detailed process was also illustrated in Fig. 6.9.

The reflection coefficient in dB as a function of the frequency is illustrated in Fig. 6.10. In blue the simulated data for the Kapton® is shown while in red is the simulated data for quartz as described in [13]. The antenna implemented on Kapton® has a maximum value of the reflection coefficient lower than -18dB at around 62GHz but the simulated -10dB matching bandwidth is smaller(<4dB) than the one derived from the simulation on quartz. Although the two substrates have similar permittivities the thickness of Kapton® film is much less resulting in a smaller BW. For a broader BW a much bigger patch width is required which would result in an undesired size of the overall structure. The specifications of the device investigated in this project can be satisfied by the derived matching bandwidth.

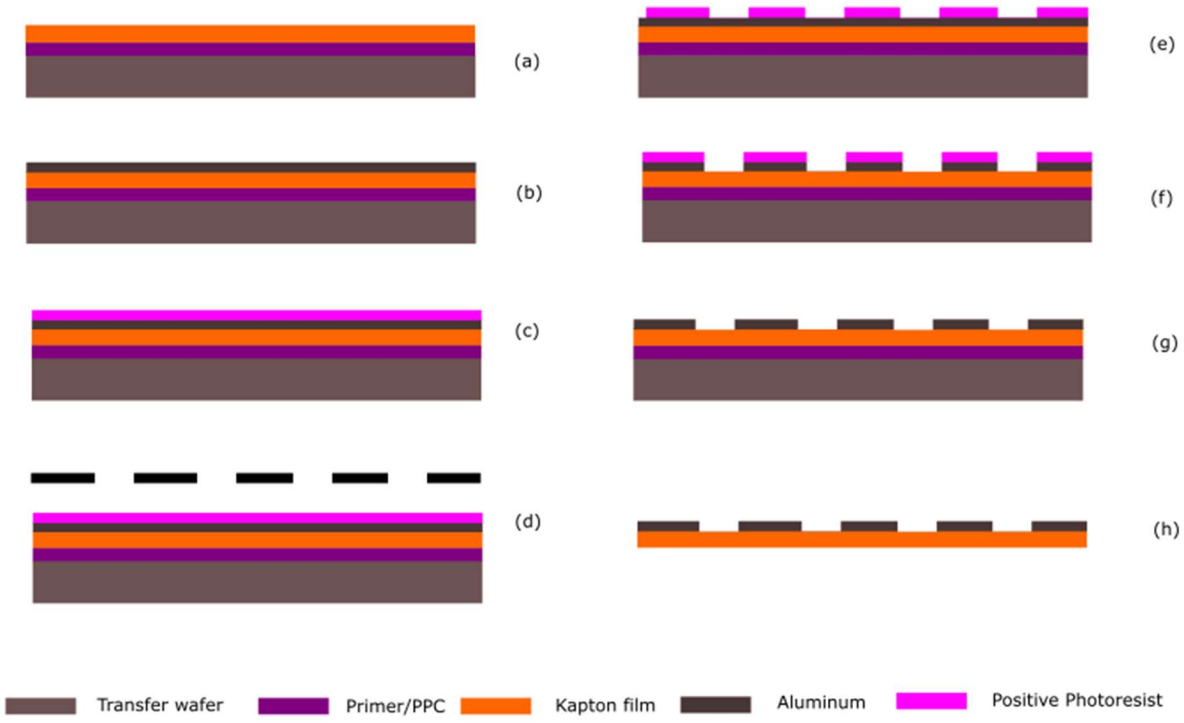


Fig. 6.9 Flowchart of the process followed for Kapton® film adhesion with PPC/primer

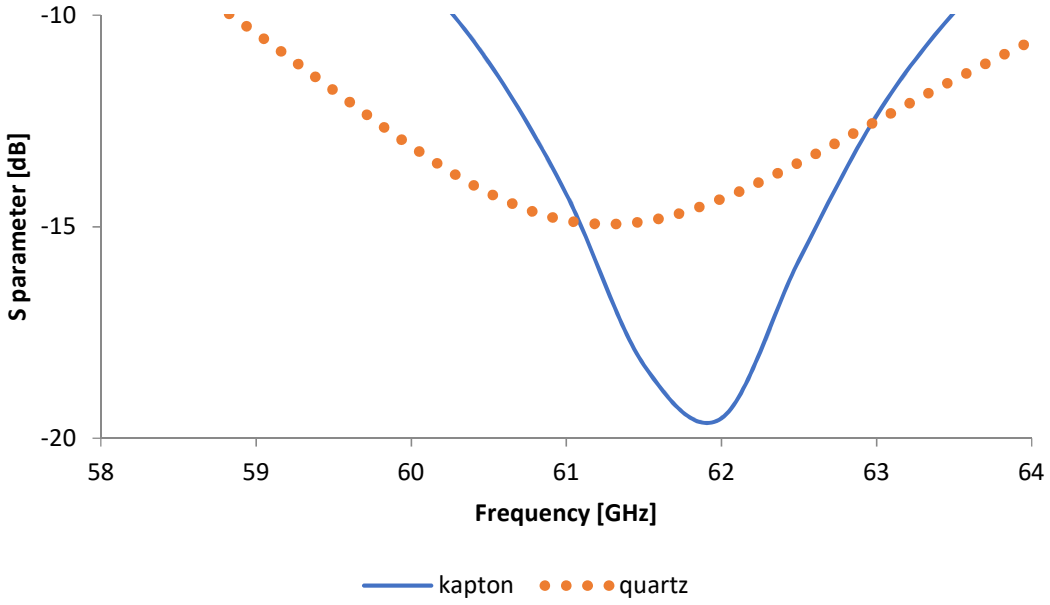


Fig. 6.10 Reflection coefficient in dB of the antenna as a function of frequency. In dash red the simulated data for quartz and in blue the simulated data for Kapton®

In Fig. 6.11, the gain of the antenna in the plane $\phi=90^{o}$ is illustrated. The derived simulated data for Kapton®, in blue line is compared to the one on quartz, red dash line. In this graph the main lobe is more clear. Patch antennas are directional antennas explaining the fact of one main lobe and several minor

lobes in the figure. The beamwidth of the patch implemented on Kapton® appears narrower that the one on quartz. Generally, antennas with wide beamwidth tend to have lower gain. Since gain is a measure of how much power is radiated in a given direction, a narrow beamwidth antenna radiating most of its energy in a specific direction will exhibit higher gain. In fig.18, though, both antennas reach a gain value of 5dB at their main lobe differentiating in the beamwidth. This could be due to the lower thickness of the substrate regarding Kapton® film (0.127mm) compared to the quartz substrate (0.200mm). In addition, changes in radiation pattern of the patch can be caused by any cavities of the film tuning the directivity of the antenna but this is more clearly elaborated in the following chapters where the film treatment is described along with the experimentally derived data.

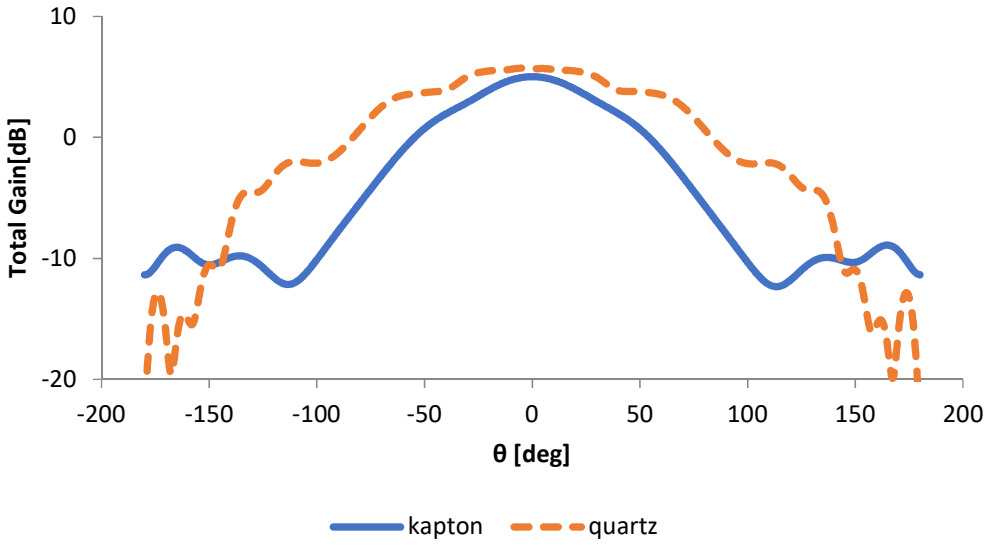


Fig. 6.11Total Gain of the antenna as a function of θ in the plane ϕ=90o at 62GHz. Red dash line the simulated data for quartz and in blue the simulated data for Kapton®

6.4 CPW Vertical Transition

Additionally, the vertical transition between microstrip and CPW lines was investigated to enhance the electromagnetic coupling of the antenna components and the integration with external subsystems. Since Polyimide substrate is difficult to connect to IC control chips via wire bond, the vertical transition could help to transfer the signal. The performance of the device was finally tested in terms of electromagnetic performance. The test results indicated that the system resonated at a lower frequency than 60GHz.

The final device consists of two coupled patterned layers as designed and simulated. The bottom side is patterned with the CPW as shown in Fig. 6.12 while the top side was patterned with the microstrip patch antenna design coupling the bottom part as shown in Fig. 6.13. Initially, the two layers were processed individually with the method elaborated in Fig. 6.9. The coupling was achieved under a microscope by means of alignment marks designed in each one of the structures. The purpose of that was to be able to exploit all the good structures individually while discarding the fault ones.

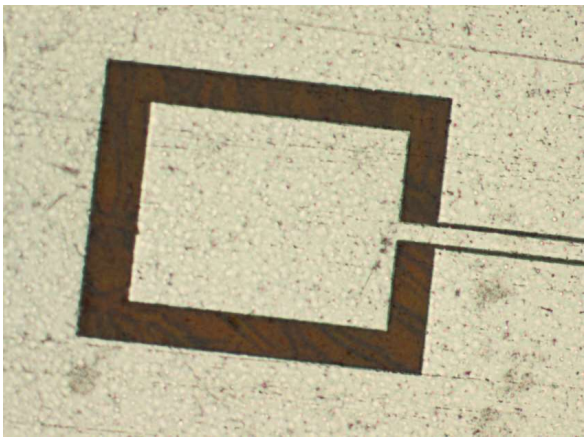


Figure 6.12: CPW as patterned on the bottom side of the device

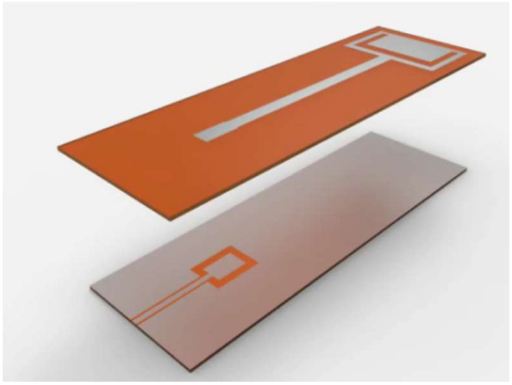


Fig. 6.13 Schematic drawing of the final device with CPW vertical transition

In order to attach the two layers, liquid polyimide, primer and PPC were tested respectively as bonding glue. A small drop of each was applied on the bottom structure in order to glue the top part. The glue layer should be thin enough so as not to change the overall thickness. That would result in a partial disorder of the device performance. The top film was initially attached and aligned manually under a microscope and in sequence employing AML aligner wafer bonder. The alignment of the two layers was quite challenging since the coupling region is of great importance and needed to be particularly precise. Any deviation from the designed structure would lead to an increase in radiation losses. Another issue worth mentioning is the attaching method. Since it is not always easy to control the amount of the adhesion media added, sometimes the adhesion liquid might exceed the defined region and proceed in covering part of the CPW which hampers the forthcoming measurement of the device. This has been the case when PPC and liquid polyimide were used as adhesion materials while primer has exhibited more stable behavior. Even a small drop of those materials could exceed the region of the antenna when pressure is applied during bonding. To deal with this problem PPC and polyimide needed to be cured in vacuum for higher stabilization of the polymer. This way the polymer becomes more viscous and stable while better adhesion is achieved. Right after the manual alignment of the coupling region the sample is driven in the bonding machine where the attachment is finalized.

The two Kapton® layers were bonded under pressure and temperature. The fundamental of the bonding between the two layers is based on Wan der Waals attractive force due to interaction of the molecules of the polymers. For primer and liquid polyimide 5000N were applied at 350°C for 3min resulting in fine adhesion. On the other hand PPC cannot tolerate such high temperature and the bonding was held at

60oC. The best adhesion was achieved with primer requiring less time and cure, the top layer was immediately attached and exhibited the most stable behavior. In Fig. 6.14 the coupling region of the final device is illustrated as observed under microscope.

The final device as fabricated is shown in Fig. 6.15. The two layers are coupled and sufficiently attached to each other with the CPW patterned on bottom layer providing the ground plane for the antenna printed on the top layer. The provided device can potentially achieve high flexibility and durability in respect to Kapton®film properties while the small thickness of the aluminum structures and the material's high adhesion on the polymer allows the device to bend and roll in different configurations without causing any damages in the metalized pattern.

The final structure was sustained in via on-wafer measurement to determine the reflection coefficient of the antenna by means of a Suss semi-automatic probe station and an Anritsu network analyzer in the band 50-65 GHz. The film had to be flat enough so that no damage would be caused in the probes and high accuracy measurements could be extracted. The scattering parameter for the antenna is illustrated in Fig. 6.16 The simulated device is shown in green line while the red line represents the experimental measurement for the device. As shown in the graph there is a differentiation in the resonance between the simulated device and the experimental ones.

Figure 6.14: The microstrip line as couples the CPW completing the device

Fig. 6.15: The final device attached with primer, alinged by self designed alignment marks

The system was designed to resonate at 60 GHz while in experimental case resonates at lower frequency, around 53 GHz. Such Frequency drop can be caused by multiple reasons:

Starting with fabrication faults, such systems based on vertical transitions are extremely sensitive in fabrication; a small misalignment in the coupling process can result in lower performance and higher loss. In addition dimension of the device holds an important role in the overall system behavior. The importance of short time chemical etching also needs to be highlighted. Over etched slots can tune the resonance of the system and influence its performance.

Another factor affecting the experimental performance of the device is the length of the microstrip line. In general, the dimension of the final device should be the same as in simulation. The microstrip line though appears to be shorter in the designed simulation since bigger size mesh is extremely time consuming and sometimes not accurate. Nonetheless, a parametrical simulation of the microstrip showed not much influence on the resonance of the system.

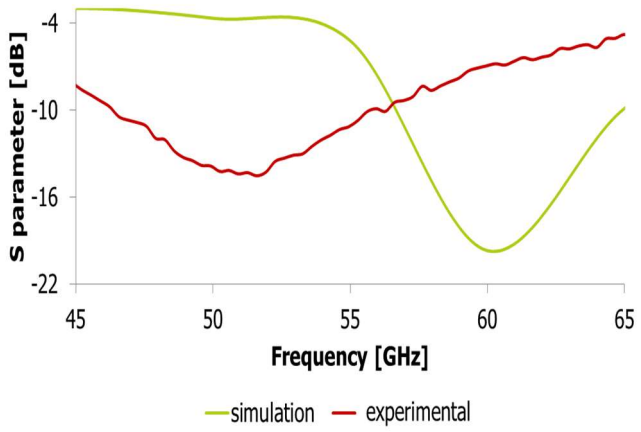


Fig. 6.16 Reflection coefficient of the final device as derived from the simulation and the experimental measurements using polyimide

A factor of major importance which has a high influence on the overall system performance, is the permittivity of the Kapton® film. Kapton® itself has a rather low permittivity as derived from data sheets. Depending on its fabrication process it is considered as a polymer of high porosity, exhibiting a low dielectric constant suitable for electronic applications. On the other hand, its high porosity can be really detrimental for the final device performance. During the fabrication process, the film undergoes high temperature and pressure, aluminum evaporation, chemical etching etc. The high porous material can absorb and trap any kind of liquid they come in contact with. In our case, it is likely that the permittivity of Kapton® film increases due to water or Al impurities. Water has a high permittivity, that means that any kind of traces or moisture trapped, automatically result in ε rising. In addition, during Al evaporation, it was observed that polyimide reacts with Al and it was rather hard to delaminate it from the film. That could also explain a possible rise in permittivity.

The influence of permittivity in the resonance of the system was tested by setting a simulation and altering gradually the dielectric constant of the substrate, varies from 3.7 to 4.5. The S parameters illustrated in this graph represent the investigation of the antenna individually where the resonance

dependence on permittivity becomes clear. The higher the dielectric constant, the lower the frequency at which the system resonates. As shown in Fig. 6.17, comparing the simulated data for an increased permittivity reaching a value of 4.5 with the measurements results, the graph approaches more the experimental results for the sample using polyimide as glue material between the two films. This can be explained by the fact that polyimide has similar properties with Kapton® film. That means that any change in properties will occur concomitantly on both polymers. On the contrary, primer might exhibit a different behavior throughout the process affecting the permittivity and lowering even more the frequency.

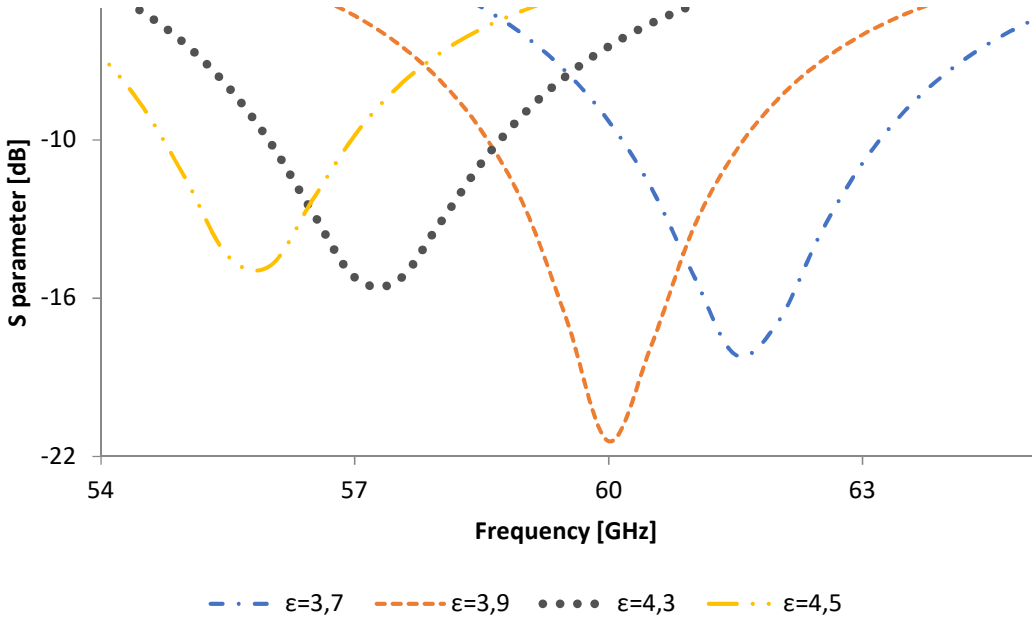


Fig. 6.17: Effect of permittivity increase on the antenna reflection coefficient as studied individually

Besides choosing high permittivity substrate, substrate thickness, the size of the patch could also be tuned for improved system performance. The parameters were checked by simulation. However, due to the cooperated chip was not ready at that moment, the presence sensing was not possible to test. With proper chip design, the antenna fabricated in this work could be functional. Such work also opens the door for flexible sensor integration. The process developed in this chapter can also be extended to other sensors applications. Moreover, such a process is complete CMOS compatible, therefore, it can be integrated together with the monolithic wafer level integration process.

6.5 Conclusion

In this work, a mmW presence sensor were chosen base on human actual presence sensing. In this work, flexible substrate Polyimide Kapton film was investigated for antenna fabrication for lower cost and easy integration in the flex/rigid substrate. Combining the photolithography process with metal deposition, such antenna has great potential for presence sensing, especially for miniaturized systems. In order to avoid wire bonding issues on flexible substrates, vertical signal transition through CPW lines was investigated, makes it promising to connect to IC chips to test. In conclusion, studies conducted on these sensors based on flex/rigid substrate make it promising for smart lighting applications.

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Chapter 7 Conclusions

In this thesis, a rigid/flex silicon-based platform was made to develop a system integrated package for solid state lighting (SSL) with multi-functions and miniaturized size. The high working temperature within miniaturized SSL applications leads to a silicon-based substrate regarding high thermal conductivity and ability for passive/active cooling. A 2D wafer level process was developed, together with devices that are compatible with such a manufacturing process. The device can be easily fabricated in 2D and assembled into 3D to provide uniform light distribution. Moreover, monolithic and heterogeneous device integration and smart sensors integration were also extended based on such a platform.

The main conclusions of this thesis are as follows:

- LED packaging and electronics are crucial for SSL systems in the reduction of total system size, cost, and risks of breakdown. With multiple layers and different thermal coefficients of expansion, the SSL system suffers from delamination, corrosion, and degradation. Therefore, chip on heatsink (COH) technology brings better thermal behavior for miniaturized systems, compared with standard surface mounted devices (SMD), and chip on board (COB). The best thermally designed LED retrofit lamp (Case 5 with COH technology) exhibited a 30% decrease in junction temperature (°C) compared with current product on the market and a 27% drop of the total thermal resistance, which is defined as temperature difference of back side of heat spreader and ambient temperature divided by thermal input power. For further lower the junction temperature, silicon was chosen as the platform for the multifunctional and miniaturized system, due to its high thermal conductivity, easy for device integration, available sensors technologies, and the possibility for microchannels for active cooling. Such silicon-based platform also has the potential for cost saving.

- Based on such an LED package, related electronics for G4 LED were investigated. In order to guarantee the LEDs are powered efficiently, different driver topology was studied. Both linear driver and switch mode driver were selected and analyzed. Components needed in G4 LED drivers were separated to on-chip components and off-chip components according to the system requirements.

- Considering the retrofit G4 LED form factor and performance requirements, wafer level packaging (WLP) can provide solutions for not only components integration but also heat dissipation in limited space. Monolithic wafer level integrated driver were fabricated and tested. Rectifier composed of 4 Schottky diodes were designed and characterized as a monolithically integrated component. Such Schottky diodes with guard ring structures processed under a standard BiCMOS process can reach a breakdown voltage of 27V. The breakdown voltage mainly depends on n-well doping concentration. In order to bring high quality LED lumen output, spice model of Schottky diode, rectifier, NPN transistors, and resistors were derived from the in-house fabricated chip and then tested.

- Wafer level integrated smart sensors were also introduced within the limited dimension. Two kinds of sensors were chosen and tested: temperature sensor, and light sensor. The

methodology of how to choose such sensors in miniaturized SSL systems was illustrated. Schottky diodes fabricated in Chapter 3 was chosen as a temperature sensor. A silicon-based light detector designed by Zahra Kolahdouz and fabricated in BiCMOS process was selected as light sensor.

- When more than 2 LED dies are needed for the system, planar WLP meets difficulty for thermal management as well as light uniformity. The main research focus is to combine the rigid/flex LED package with semiconductor IC technology or other technologies to create a miniaturized system package. As a result of that, 3D WLP provides even more possibility than 2D planar wafers, in terms of size reduction, high performance, and the possibility for monolithic/hetero-integration. In the application of SSL, 3D WLP also enables the uniform light distribution. Therefore, a rigid/flex platform was designed, tested, and applied for the miniaturized multifunctional LED package in this work. The LED chips located in the silicon cavity covered by a light reflection layer were connected by flexible aluminum interconnects encapsulated by polyimide. The flexible hinges bent to angles up to 90° to form 3D shapes with rigid silicon acting as side walls. A design rule for flexible aluminum interconnects was investigated to reach a lifetime of 25000 hours, taken into consideration of Mean Time To Failure (MTTF). Such an LED package based on a rigid/flex platform improves light uniformity, reduces volume, and brings more possibility for cooling structures such as heat pipes, sensors for smart lighting control, etc. It worth to mention that such a rigid/flex substrate manufacturing process is CMOS compatible thus can be easily implemented together with driver WLP.

- In order to test such flex/rigid LED package for miniaturized SSL applications, two prototypes aiming for G4 LED were built up. The simulated circuit was designed based on the simulated Schottky diode model derived from devices fabricated in Chapter 4. Therefore, two kinds of driver were designed. One is inductor free linear driver. The total size is only half of the original G4 LED. However, the driver efficiency is limited, as well as smart control applications. The other driver is switch mode buck driver. With such design, the total size is the same as the original G4 LED. A temperature sensor was integrated and successfully controlled the light output when reaching high working temperatures (>85˚C). Therefore, the advantage of such a buck driver is higher power efficiency and the ability of smart control.

- With the introducing of flexible hinges, the flexible substrate was invested for electronics integration., A mmW presence sensor was chosen to be fabricated on polyimide Kapton film for lower cost. Such mmW presence sensors based on human actual presence sensing, are more accurate and consume less power compared with traditional IR sensors. Moreover, the size of such a flexible antenna can be shrinked to fit in the G4 rigid/flex LED package. The process of antenna fabrication can also be easily integrated into the flex/rigid substrate or monolithic wafer level processing. Combining the photolithography process with metal deposition, such antenna has great potential for presence sensing, especially for miniaturized systems. In order to avoid wire bonding issues on flexible substrates, vertical signal transition through CPW lines

was investigated, makes it promising to connect to IC chips to test. In conclusion, studies conducted on these sensors based on flex/rigid substrate make it promising for smart lighting applications.

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Curriculum Vitæ

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2005-2009	Bachelor of Materials Science and Engineering, China Beijing University of Aeronautics and Astronautics(Beihang University) Thesis: Electrodeposition Preparation of Ni/Ppy bi-layer nanowire arrays
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Work

2016-2017	UL Transaction Security BV, the Netherlands Analyst
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Awards

2009-2011	Faculty Scholarship of TU Delft
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