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Synchronization of Bloch oscillations by gate voltage modulation

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We propose to synchronize Bloch oscillations in a double phase-slip junction by modulating the gate voltage rather than the bias voltage. We show this is advantageous, and the relatively small ac modulation of the gate voltage gives rise to the pronounced plateaus of quantized current of the width of the order of Coulomb blockade threshold. We theoretically investigate the setup distinguishing three regimes of strong, weak, and intermediate coupling, defined by the ratio of the gate capacitance C and the effective capacitance of the phase-slip junctions. An important feature of the intermediate-coupling regime is the occurrence of the fractional plateaus of the quantized current. We investigate the finite temperature effects, finding an empirical scaling for the smoothing of integer plateaus.

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I. INTRODUCTION

An elementary process giving rise to resistance in a quasi-one-dimensional superconducting wire is a phase-slip: an event where the magnitude of the superconducting order parameter locally and momentarily reaches zero, allowing the phase difference of the superconducting order parameters on the left and on the right to slip by 2π ([1,2], see [3] for review). This corresponds to a magnetic flux quantum Φ_0 moving across the wire, or, equivalently, a voltage pulse with $\int dtV(t) = \Phi_0$. The phase slips due to thermal and quantum fluctuations have been observed and identified in the course of thorough and difficult experiments [4–6].

The quantum coherence between individual phase-slip events results in modification of the ground state of superconducting systems that become a superposition of the states [7] that differ in flux quanta. Quantum coherent phase-slip states have been observed in superconducting nanowires [8,9] and the chains of Josephson junctions that in many respects are similar to the superconducting nanowires [10]. There is a remarkable duality between the coherent tunneling of flux quanta due to the phase slips and the coherent tunneling of Cooper pairs transferring charge $2e$ that is the base of the Josephson effect [11], so that each Josephson electronic circuit has a dual counterpart made from phase-slip junctions, and vice versa. This has given rise to many theoretical suggestions and experimental work [3,12–21].

A phase-slip junction in a high-impedance environment [where the typical resistance R exceeds G_Q^{-1}, $G_Q \equiv e^2/(\pi\hbar)$] gives rise to a Coulomb blockade of the current up to a voltage threshold that is dual to a zero-voltage state up to a current threshold in a standard Josephson junction. A phase-slip junction can be realized in a nanowire [11] as well as on the basis of a Josephson junction embedded in a highly resistive environment [12].

It has been predicted [22–24] that this should give rise to synchronization of Bloch oscillations, an effect that is potentially useful for metrological applications and irreplaceable in this context. Modern metrology defines the ampere as a product of the electron charge by frequency. There is need of a practical high-accuracy current standard exploiting this principle. This is crucial for the realization of a so-called quantum metrology triangle [25] that enables important fundamental consistency tests on the validity of commonly assumed relations between fundamental constants of nature and the quantum electrical effects. The triangle combines three standards: the voltage standard that is based on Josephson effect and relates volt and frequency, the resistance standard based on the quantum Hall effect, and, to close the triangle, a current standard that provides a transfer of integer number of electrons per a period of a control signal. The most advanced realization of such a current standard is a single-electron pump, where the electrons are transferred through a semiconducting quantum dot [26]. This design, however, is limited to small currents/frequencies not exceeding 1 nA.

The alternative realization exploits the synchronization of Bloch oscillations. Biasing a phase-slip junction with combination of dc and ac bias should give rise to current plateaus with the value corresponding to the ac frequency ω: $I = (e/\pi)\omega$. This may enable a high-precision current standard that is dual to the Josephson voltage standard [11]. The Josephson voltage standard [27,28] exhibits Shapiro steps: the voltage plateaus at the values of voltage matching the Josephson frequency. So the current plateaus can be regarded as dual Shapiro steps. A low-impedance environment is required for Josephson voltage standard, while a high-impedance environment is needed for the phase-slip current standard.

It has to be noted that it is much more difficult to realize a high-impedance environment than the low-impedance one, and prevent overheating of such environment by power dissipation in the course of operation. Although the phase-slip Coulomb blockade feature has been reliably observed (e.g., [29,30]), the attempts to achieve the synchronization of Bloch oscillations [18,31–33] have not demonstrated a decent pre-

cision during the three decades. The breakthrough has been reported [34] only very recently, after the completion of this manuscript.

In recent years, much experimental and theoretical interest was received by a double phase-slip junction [14,35,36]. The total phase-slip amplitude there is a result of interference of the phase slips in constituent junctions, this interference being affected by a gate voltage supplied via a capacitive coupling. The gate charge dependence has been successfully demonstrated in spectroscopy measurements of the phase-slip qubit-level positions [37] and in the measurements of the Coulomb blockade threshold [35,37,38].

In this article we propose synchronization of Bloch oscillations in a double phase-slip junction by the ac gate voltage and theoretically investigate this phenomenon in a variety of regimes. Let us explain here why, in our opinion, the gate voltage synchronization is advantageous in comparison with the standard bias synchronization. The reason is general although rather technical, at least from a theoretical point of view. A phase-slip junction should be embedded to a high-impedance environment with substantial capacitance. While this capacitance is irrelevant for dc bias, there is an overwhelming *RC* filtering of the ac signal. To get a substantial ac signal at the junction, one needs to increase ac bias by orders of magnitude to compensate for the filtering. This ac bias leads to substantial dissipation in the environment, its overheating, and destruction of the synchronization by the thermal noise generated by this overheating. This is the likely explanation of the fact that a prominent Coulomb blockade feature at dc bias does not give rise to high-quality synchronization if ac bias is applied. In contrast to this, the ac gate voltage signal propagates in a low-resistance environment and should provide much less dissipation.

In this article we systematically analyze the phenomenon in the quasiclassical limit corresponding to the limit of high impedance, mostly concentrating on the peculiarities of current plateaus. We distinguish three regimes. (i) A strong-coupling regime corresponds to the limit of small gate capacitance C as compared to effective phase-slip junction capacitances. Most experimental setups are in this regime [35,37,38]. The harmonic gate voltage modulation gives rise to multiple *integer* plateaus. We show that in this regime the width of the plateau can be made comparable with the Coulomb blockade threshold voltage even for very asymmetric junctions at sufficiently large modulation amplitudes. (ii) An intermediate-coupling regime where the effects of finite gate capacitance are essential. We demonstrate the appearance of *fractional* plateaus with the width $\propto C$. This is a dual of half-integer Shapiro steps observed in Josephson superconducting quantum interference devices (SQUIDS) [39]. (iii) A weak-coupling regime of big C_g where the gate capacitor plays the role of an effective dc voltage source and efficiently decouples.

For all three regimes, we analyze the effect of the thermal noise on the plateaus. We demonstrate that that integer plateau vanishes at the temperature $k_BT \approx 0.06e\Delta V$, ΔV being the plateau width in the absence of noise.

The paper is organized as follows. In Sec. II we give the description of the setup and the system of equations governing its dynamics. We address the stationary regime in Sec. III. We discuss the emergence of current plateaus in strong (Sec. IV), intermediate (Sec. V), and weak (Sec. VI) coupling regimes. In Sec. VII we address the finite temperature effects in all three regimes. We conclude in Sec. VIII.

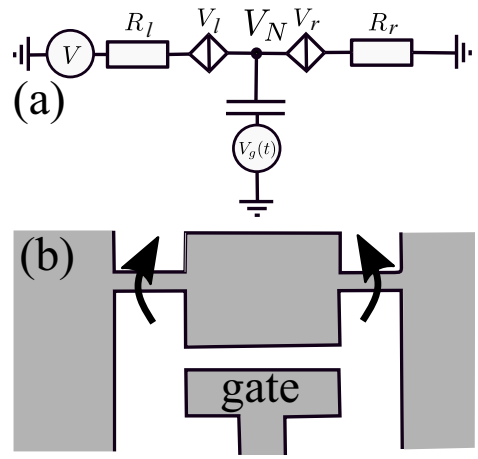

FIG. 1. Two phase-slip junctions in series in a resistive environment coupled to a capacitor in between where the gate voltage is applied.

II. THE SETUP

In this article we address a double phase-slip junction setup (Fig. 1). We require two phase-slip junctions in series: those can be realized lithographically as short nanowire-type constrictions in a superconducting film of a high normal-state resistance [8] [Fig. 1(b)]. We do not have to impose any stringent conditions on homogeneity and regularity of the materials in use: we only need the phase-slip tunneling amplitudes via the narrow parts of the setup. The tunneling amplitudes may be due to phase slips arising uniformly in the wires, or they can be dominated by the slips in the most narrow place of the wire, or even occur in a tunnel-type Josephson junction that is formed in the wire; this is not important, as explained in [12] in more detail. Eventually the nanowire could be a Josephson junction chain with the phase slip occurring at the weakest junction. Experimentally, the amplitude in a single junction, either the left or right one, is determined from the observation of the Coulomb blockade threshold voltage, $V_{l,r}$ being the threshold voltages for the junctions of the setup. The junctions are embedded in the high-impedance environment. We took the simplest and most frequently used model of such an environment: the frequency-independent resistors $R_{l,r}$ on both sides of the double junction. The important part of the setup is the gate electrode coupled via the capacitance C to the node between the junctions.

We consider here the quasiclassical limit that is justified when the resistance exceeds by far the quantum unit, $R_{l,r}G_Q \gg 1$. In this case the charge passed though a junction is a good classical variable subject to few quantum fluctuations. We will use a dimensionless charge $q = Q\pi/e$. In these notations, each junction can be regarded as a nonlinear capacitor with the voltage drop depending on q, $V(q) = V_{l,r}\sin q_{l,r}$.

The voltage drops at the resistors are given by corresponding currents, $\frac{e}{\pi}R_{l,r}\dot{q}_{l,r}$. We assume the system is biased from

the left with the voltage V. Introducing the voltage $V_N(t)$ at the node between the junctions, we equate the voltage drops as follows:

$$V_N(t) = V_r \sin q_r + \frac{e}{\pi} R_r \dot{q}_r, \tag{1}$$

$$V - V_N(t) = V_l \sin q_l + \frac{e}{\pi} R_l \dot{q}_l. \tag{2}$$

Each of these two equations is equivalent to a standard voltage-biased single-junction equation. The coupling between the junctions comes about the fact that the voltage at the node $V_N(t)$ also depends on the charge accumulated at the capacitor C. It is also contributed by the gate voltage,

$$V_N(t) = \frac{e}{\pi} \frac{q_l - q_r}{C} + V_g(t). \tag{3}$$

In the weak-coupling limit $C \to \infty$ the capacitor efficiently uncouples the phase-slip junctions VI. In the opposite limit of strong coupling (IV), the two phase-slip junctions effectively work as one with an amplitude that is the sum of the two. The interference of two amplitudes can be tuned by gate voltage.

Now we can account for the voltage noise coming from the thermal fluctuations in the large resistors. The noise gives a stochastic addition $\xi(t)$ to the voltage drop at a resistor satisfying $\langle \xi(t)\xi(t')\rangle = 2k_BTR\delta(t-t')$, $\langle \xi(t)\rangle = 0$. We define noises in both resistors such as $\langle \xi_r(t)\xi_r(t')\rangle = 2k_BTR_r\delta(t-t')$, $\langle \xi_l(t)\xi_l(t')\rangle = 2k_BTR_l\delta(t-t')$, $\langle \xi_l(t)\xi_r(t')\rangle = 0$. The resulting system of equations which we analyze in this article thus reads

$$\begin{cases} \frac{e}{\pi} R_l \dot{q}_l = V - V_l \sin q_l - V_N(t) + \xi_l(t) \\ \frac{e}{\pi} R_r \dot{q}_r = V_N(t) - V_r \sin q_r + \xi_r(t) \\ V_N(t) = \frac{e}{\pi} \frac{q_l - q_r}{C} + V_g(t). \end{cases} \tag{4}$$

These are the stochastic evolution equations for two variables q_r, q_l.

Owing to the duality mentioned, a similar set of equations describes a Josephson junction system in a low-impedance environment. This system is a dc current–biased, two-junction SQUID with an extra inductance in the loop subject to a time-dependent flux penetrating the loop (a dual of the time-dependent gate voltage). Such Josephson circuits have been studied in [39,40] but, to our knowledge, have not been put into practice.

III. STATIONARY REGIME

In this section we shortly describe and illustrate the stationary regime where both bias and gate voltage do not depend on time. Let us start with a Coulomb blockade when (in the absence of noise) no current is flowing until the bias voltage V reaches a certain threshold value $V_{\rm th}$. In the Coulomb blockade regime, $V = V_l \sin q_l + V_r \sin q_r$, and the charges $q_{l,r}$ are related by

$$q_l - q_r = -q_g + \frac{\pi C V_r}{e} \sin q_r, \tag{5}$$

where we have introduced the gate-induced charge $q_g \equiv \pi C V_g/e$. The periodicity of $\sin q_{l,r}$ implies the periodicity of the results for $V_{\rm th}$ in q_g, that is, in gate voltage.

These results also depend on the ratio between the gate capacitance and effective capacitance of the phase-slip junctions. We will use the dimensionless parameter

$$C_d = \frac{\pi C(V_l + V_r)}{2e} \tag{6}$$

to characterize the ratio and distinguish the regimes.

The strong-coupling regime corresponds to small C_d. In this case, two phase-slip junctions are equivalent to a single junction. The difference $q_r - q_l$ is set to q_g, and the overall phase-slip amplitude is a sum of two amplitudes corresponding to tunneling in the junctions,

$$\mathcal{A} = V_l e^{iq_l} + V_R e^{iq_l + iq_g}. \tag{7}$$

The gate voltage controls the relative phase shift and thus the interference of two amplitudes. The threshold voltage is determined by the maximum modulus of this amplitude,

$$V_{\rm th} = \sqrt{V_r^2 + V_l^2 + 2V_rV_l \cos q_g}. \tag{8}$$

The threshold vanishes at $V_l = V_r$, $q_g \mod 2\pi = \pi$ as the result of destructive interference.

The large capacitance effectively decouples the phase slips in the junctions, so in the opposite regime of weak coupling $C_d \gg 1$ the threshold voltage is thus a sum of two thresholds plus a a small periodic correction:

$$\frac{V_{\rm th}}{V_l + V_r} = 1 - \frac{\bar{q}_g}{2C_d}, \tag{9}$$

$\bar{q}_g \equiv (\pi C V_r/e - q_g) \mod 2\pi$.

If the bias voltage exceeds the threshold, a dc current I flows in the circuit. It is accompanied by ac (Bloch) oscillations with the frequency $\omega_B = \pi I/e$ corresponding to the dc current. We obtain the I-V characteristics by solving the system 4 at given V, V_g at a long time interval $(0, t)$ and calculating the time-averaged current from $I = (q_{l,r}(t) - q_{l,r}(0))/t$. The characteristics evaluated are shown in the Fig. 2.

We see that I-V curves qualitatively follow the same shape typical for a single junction: a sharp square-root rise immediately after threshold and Ohmic behavior $I = V/(R_r + R_l)$ at $V \gg V_{l,r}$. The threshold is, however, modulated by the gate voltage. We measure the current in units of $2e\omega_0$, ω_0 being the frequency scale determined by the phase slips,

$$\omega_0 = \frac{\pi}{e} \frac{V_l + V_r}{R_l + R_r}, \tag{10}$$

and change the definition of q_g to compensate for the average V_N in the Ohmic regime,

$$q_0 = \frac{\pi C}{e} \left(\frac{R_r}{R_l + R_r} V - V_g \right). \tag{11}$$

In the left panel of Fig. 2 we plot the I-V characteristics for the intermediate coupling C_d at several q_0. The threshold is modulated by the gate voltage but does not vanish even for the symmetric case considered, since the finite capacitance effects suppress the destructive interference, its minimum value being $\approx 0.2(V_l + V_r)$. In the right panel of Fig. 2, we plot the I-V curves at various C_d at $q_0 = 0, \pi$. At $q_0 = 0$ maximizing the threshold all characteristics are the same; this is a peculiarity of the symmetric case. At $q_0 = \pi$ the threshold changes from

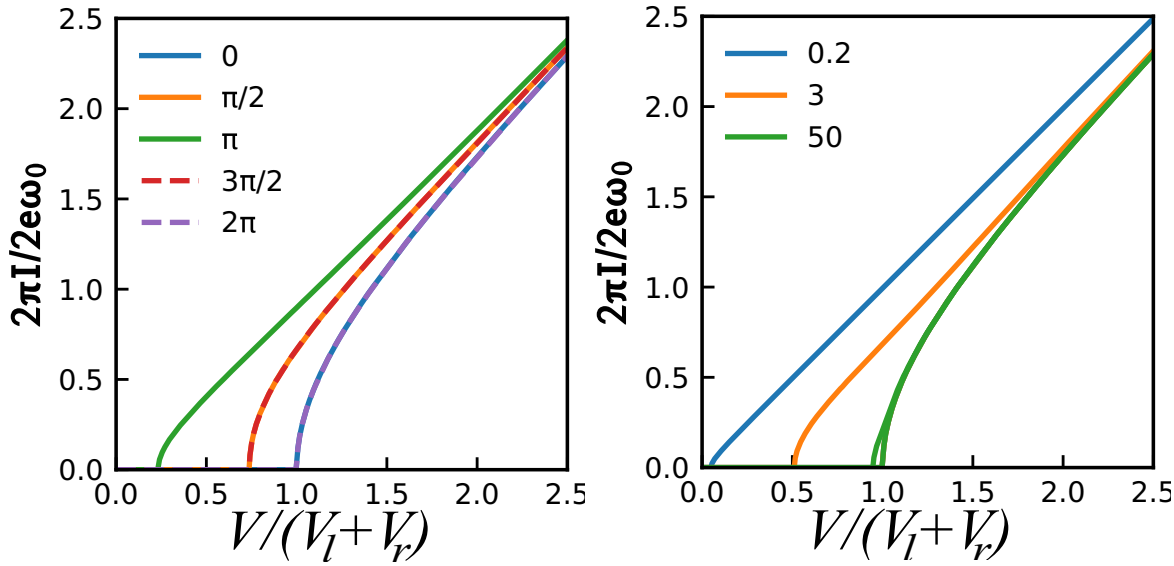

FIG. 2. I-V characteristics in stationary regime. Symmetric setup, $R_l = R_r$, $V_l = V_r$. Left: Intermediate coupling, $C_d = 1$. The labels give the gate-induced charge q_0. The Coulomb blockade threshold is modulated by q_0 but does not vanish at $q_0 = \pi$ owing to finite C_d. Right: I-V characteristics for $q_0 = 0, \pi$, and three different C_d shown in the labels. The curves collapse at q_0, which is the peculiarity of the symmetric setup. The minimum threshold approaches the maximum one upon increasing C_d manifesting the weak-coupling regime.

an almost zero to almost maximum value upon decreasing the capacitance and thus decoupling the junctions.

IV. PLATEAUX IN STRONG-COUPLING REGIME

The most important application of the circuit is the synchronization of Bloch oscillations with an extra external ac signal of frequency ω. Without such a signal, the solutions of the dynamical equations are degenerate with respect to the phase of the oscillations owing to time translation symmetry. The ac signal breaks the symmetry, and the phase locks with that of the signal. In the dc measurement this is manifested as a current plateau; the dc current does not depend on the bias voltage in a certain interval of the voltages of the width ΔV, and the value of the current is determined by the frequency only. In this section and the two following ones we explore the current plateaus in the strong-, intermediate-, and weak-coupling regimes, respectively. We consider the periodic modulation of the gate voltage, concentrating on the harmonic one: $q_g(t) = q_0 + A\sin(\omega t)$.

Some examples of I-V characteristics are shown in Fig. 3. We observe the current plateaus at multiples of the modulation frequency $I_k = ke\omega/\pi$. The width of the plateau $\simeq (V_l + V_r)$ at $A \simeq 1$. At small A, the width of the kth plateau scales as A^k. The width is a nonmonotonous function of A.

Let us derive an analytical expression for the width of the plateau in the limit of $k\omega \gg V_{l,r}/R_\Sigma e$. It follows from Eq. (3) that the limit $C \to 0$ $q_r = q_l + q_g(t)$. Let us separate q_g into a time-independent and oscillating part, $q_g(t) = q_0 + \tilde{q}_g(t)$. Let us introduce a convenient variable

$$q = r_l q_l + r_r q_r + q_0(r_r - r_l - 1/2), \tag{12}$$

where $r^{r,l} = R_{r,l}/R_\Sigma$. Summing up Eq. (1), we obtain a convenient equation for this variable,

$$\frac{e}{\pi} R_\Sigma \dot{q} + \mathrm{Im}[e^{iq}\mathcal{A}(t)] = V, \tag{13}$$

where the effective phase-slip amplitude $\mathcal{A}(t)$ reads

$$V_l e^{-iq_0/2} e^{-i\tilde{q}^R(t)} + V_r e^{iq_0/2} e^{i\tilde{q}^L(t)}, \tag{14}$$

where $\tilde{q}_g^{r,l} \equiv r_{r,l}\tilde{q}_g$.

We concentrate on $V \gg (V_l + V_r)$ and $\pi V/eR_\Sigma$ close to $k\omega$. We will search for the solution in the form (see, e.g., [41])

$$q = k\omega t + \psi(t), \tag{15}$$

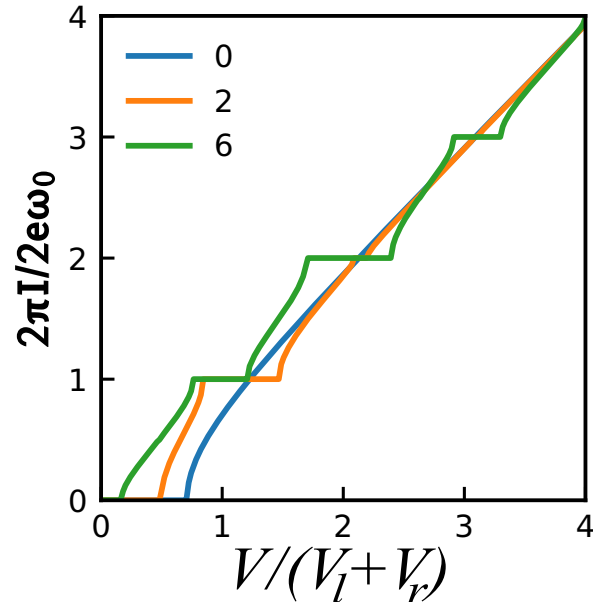

FIG. 3. I-V characteristics in the strong-coupling regime, $C_d = 0.2$, for the different gate voltage amplitudes A shown in the labels. The setup is symmetric, $q_0 = \pi/2$, and $\omega = \omega_0$. Upon increasing the amplitude, the current plateaus develop at the multiples of the modulation frequency $I_k = ke\omega/\pi$.

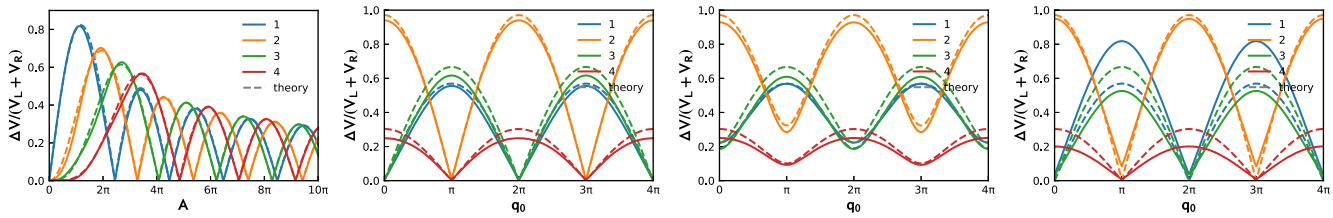

FIG. 4. Strong-coupling limit. The width of the current plateaus at $\omega = 2\omega_0$. (a, b, d) are for symmetric setup, and for (a, b, c) $C_d = 0.05$. The high-frequency Bessel approximation [Eqs. (18) and (19)] given by dashed lines. (a) Width of several integer plateaus in symmetric case vs the driving amplitude at $q_0 = \pi/2$. The curves are close to the high-frequency Bessel approximation. (b) The widths vs q_0 for the constant amplitude $A = 2\pi$. The destructive interference in the symmetric setup manifests as zero width and a cusp at the values $q_0 = 0, \pi$ for odd and even plateaus, respectively. (c) Same as in (b), for a slightly asymmetric setup, $V_r = 2V_l$. (d) Same as in (b), the capacitance is increased to $C_d = 1$.

assuming the separation of timescales (see, e.g., [41]), that is, the phase ψ to change slowly on the scale of ω. Substituting Eq. (15) to Eq. (13) and averaging over the short timescale, we obtain an evolution equation for this slow phase,

$$\frac{e}{\pi} R_\Sigma \dot{\psi} + \mathrm{Im}[e^{i\psi}\overline{\mathcal{A}}_k] = \delta V, \tag{16}$$

where $\delta V = V - (e/\pi)R_\Sigma k\omega$, and $\overline{\mathcal{A}}_k$ is the result of averaging the amplitude over the oscillation period,

$$\overline{\mathcal{A}}_k = \int_0^{2\pi/\omega} dt\, \mathcal{A}(t) e^{ik\omega t}. \tag{17}$$

Equation (16) has a stationary solution for ψ provided $|\delta V| < |\overline{\mathcal{A}}_k|$. This implies that the frequency of the oscillations in this voltage interval does not change being locked to $k\omega$. The width of the plateau is thus given by

$$\Delta V_k = 2|\overline{\mathcal{A}}_k| = 2|V_l e^{-iq_0/2} J_k(A_r) + V_r e^{iq_0/2} J_k(-A_l)|, \tag{18}$$

where in the last equation we have specified to the harmonic gate voltage signal, $A_{r,l} \equiv r^{r,l}A$, J_k being the Bessel function of order k. For the symmetric case $R_r = R_l$, $V_l = V_r = V_\Sigma/2$, this becomes

$$\Delta V_k = 2V_\Sigma J_k(A/2) \begin{cases} |\cos(q_0/2)|, & \text{if } k \text{ is even} \\ |\sin(q_0/2)|, & \text{if } k \text{ is odd.} \end{cases} \tag{19}$$

We thus have selection rules in this case: no odd plateaus at q_0, no even plateaus at $q_0 = \pi$.

Although the expression (18) is formally valid only in the limit $k\omega \gg \omega_0$, we find numerically that it gives qualitatively good estimations for all $\omega \simeq \omega_0$. We extract the plateau widths from numerical data, finding the voltages at which the relative deviation of the current from the quantized value amounts to 10^{-3} and associating those with the endpoints of the locking interval.

We present the numerical results for $\omega = 2\omega_0$ in Fig. 4 in comparison with Eqs. (19) and (18). Figure 4(a) gives the widths versus the driving amplitude A for the symmetric setup at $q_0 = \pi/2$ so that the plateaus of both parities are developed. As we see, the actual widths coincide with Bessel function prediction with the accuracy of several percent. In Fig. 4(b) we plot the widths versus q_0 at constant driving amplitudes. We observe the selection rules mentioned: the width drops to 0 with the plotting accuracy for $q = 0$ and odd plateaus, and for $q_0 = \pi$ and even plateaus, manifesting the destructive interference of the phase slips. The curves make a cusp at these values of q. As we see in Fig. 4(c), the curves are smooth and do not reach 0 if we depart from the symmetric case ($V_l/V_r = 2$ in this figure). It is interesting to note that if we decrease the capacitance moving towards the intermediate-coupling regime [$C_d = 1.0$ for Fig. 4(d)], the cusps in the symmetric case do not disappear but visibly depart from 0. Thus the small decoupling of the phase slips suppresses the destructive interference. This is consistent with the results for the Coulomb blockade threshold voltage described in the previous section.

The analytical expressions for widths given by Eqs. (18) and (19) do not depend on frequency. This should not be valid for sufficiently small frequency. Indeed, we see that the plateaus disappear in the limit of $\omega \ll \omega_0$, in the limit of small frequency (Fig. 5). We also see that the high-frequency limit is achieved already at $\omega \approx \omega_0$ for all plateaus and the frequency dependence is generally nonmonotonous, resembling a Bessel-like dependence on the amplitude.

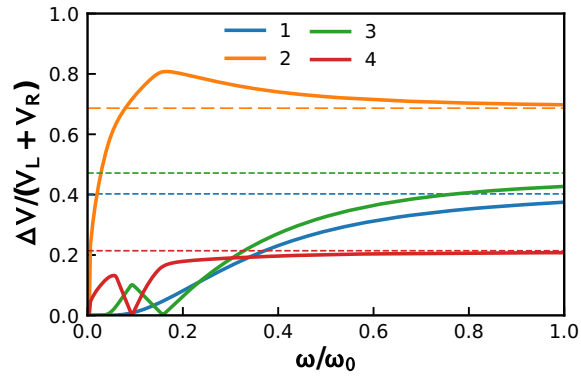

FIG. 5. The frequency dependence of the plateau width for several integer platueas (see the labels). Strong-coupling regime $C_d = 0.2$, $q_0 = \pi/2$, symmetric setup, the gate charge amplitude $A = 2\pi$. The high-frequency limits [Eqs. (18) and (19)] are given by dashed lines. The high-frequency approximation given [formula (18)] is given by dashed lines. We see that the limit is achieved at $\omega \approx \omega_0$ for all plateaus. The width is the high-frequency approximation and is valid for all steps. The width decreases to zero at lower frequencies, with some nonmonotonous Bessel-like dependence.

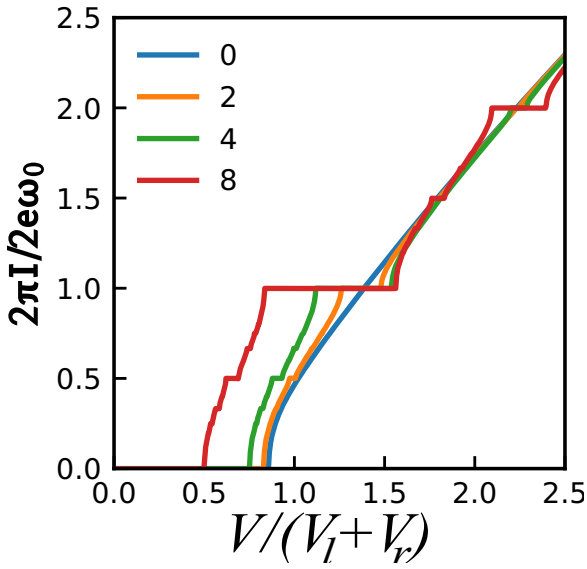

FIG. 6. Intermediate-coupling regime $C_d = 5$. Symmetric setup. I-V characteristics for $q_0 = \pi/2$ and several different driving amplitudes A given in the labels. In addition to the integer plateaus, we see the emergence of smaller fractional plateaus at $I_{MN} = (e/\pi)\omega\frac{M}{N}$.

V. FRACTIONAL PLATEAUS IN INTERMEDIATE-COUPLING REGIME

In this section we will discuss the intermediate-coupling regime $C_d \simeq 1$. Typical I-V characteristics with driving are presented in Fig. 6. A striking difference from the strong-coupling regime is the appearance of smaller current plateaus at integer fractions of $e\omega/\pi$. In principle, we expect a plateau at any rational fraction $I_{MN} = (e\omega/\pi)M/N$, M, N being an integer, so that the actual I-V characteristics resemble Cantor function and are an example of a devil's staircase [42]. In practice, the plateau widths become exponentially small upon increasing N so only several fractional plateaus are visible. In our numerics, we were able to detect the features up to $N = 7$. The fractional plateaus are best visible for $C_d \simeq 5 - 10$ and will gradually disappear upon further increase of capacitance, see the next section.

To understand the emergence of fractional plateaus analytically, we will develop a perturbation theory in terms of small C_d. To simplify the derivations, we resort to the fully symmetric setup ($R_l = R_r = R_\Sigma/2$, $V_l = V_r = V_\Sigma/2$).

It follows from Eqs. (3) and (1) that the first-order correction in C_d to Eq. (13) can be presented as a small change of the gate charge:

$$q_g(t) \to q_g(t) - \frac{\pi C}{2e}\left(\frac{e}{2\pi}R_\Sigma \dot{q}_g(t) + V_\Sigma \sin\frac{q_g(t)}{2}\cos q\right). \tag{20}$$

The first term in the addition is an insignificant modification of the signal, while the second term brings higher harmonics of e^{iq} into Eq. (13), which becomes

$$\frac{e}{\pi}R_\Sigma \dot{q} = V - V_\Sigma \cos\frac{q_g(t)}{2}\sin q - V_F \sin^2\frac{q_g(t)}{2}\sin 2q. \tag{21}$$

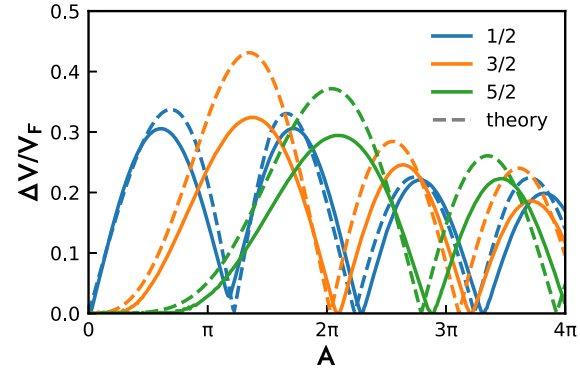

FIG. 7. The widths of the half-integer plateaus 1/2, 3/2, and 5/2 vs the driving amplitude. Symmetric setup, $\omega = 2\omega_0$, $q_0 = \pi/2$, $C_d = 0.2$. The numerical results (solid lines) are in good correspondence with the semianalytical prediction [Eq. (30), dashed lines].

Here $V_F \equiv \pi C V_\Sigma^2/8e$, $V_F \ll V_\Sigma$, and the third term represents a relevant correction responsible for emergence of the half-integer plateaus. A similar equation has been studied in the context of fractional Shapiro steps [39]. Further orders in C_d would provide the terms $\propto e^{iNq}$ with $N > 2$ that will account for the plateaus at higher fractions.

We analyze this in the limit of high frequencies, searching for the solutions in the form [cf. Eq. (15)]

$$q = (k + 1/2)\omega + \psi(t), \tag{22}$$

with $\psi(t)$ being the slow-varying phase. We can neglect the second term in Eq. (21), since it averages out over the period. The resulting equation for this phase is contributed by the third term,

$$\frac{e}{\pi}R_\Sigma \dot{\psi} + \mathrm{Im}\left[e^{2i\psi}\overline{\mathcal{A}}_k^{(2)}\right] = \delta V, \tag{23}$$

where

$$\overline{\mathcal{A}}_k^{(2)} \equiv \frac{V_F\omega}{2\pi}\int_0^{\frac{2\pi}{\omega}} dt \sin^2\frac{q_g(t)}{2} e^{i(2k+1)\omega t}. \tag{24}$$

This gives the width of the half-integer plateau,

$$\Delta V_{k+1/2} = V_F |J_{2k+1}(A)||\sin q_0|, \tag{25}$$

which is parametrically smaller than V_Σ in the limit $C_d \to 0$ and is of the order of V_F in the intermediate-coupling regime.

This gives an accurate prediction at high frequencies $\omega \gg \omega_0$. To investigate the half-integer phase slips at lower frequencies, we build up a more complex perturbation theory in C_d. This relies on a heuristic assumption; however, it accurately and adequately describes complex numerical data (see Fig. 7).

To start with the low-frequency perturbation theory, we would need to solve the unperturbed equation

$$\frac{e}{\pi}R_\Sigma \dot{q} = V - V_\Sigma \cos\frac{q_g(t)}{2}\sin q. \tag{26}$$

We cannot find an explicit analytical solution. Instead, we use a solution $q_\star(t)$ of an *autonomous* equation obtained by the averaging of $\cos(q_g(t)/2)$ over the period

$$\frac{e}{\pi}R_\Sigma \dot{q}_\star = V - V_\Sigma \bar{f}\sin q_\star, \tag{27}$$

$\bar{f} = J_0(A/2)\cos(q_0/2)$. This equation can eventually be solved [41], and we write the solution in the form

$$\frac{dt}{dq_\star} = \frac{V - V_\Sigma \cos(\Omega t + \psi)}{\Omega^2 \pi R/e}, \tag{28}$$

where the frequency of autonomous oscillations

$$\Omega = \pi \frac{\sqrt{V^2 - V_\Sigma^2 \bar{f}^2}}{eR}. \tag{29}$$

We are interested in Ω close to $M\omega/2$, M being odd. We substitute the expression (28) to Eq. (21) and derive an equation for the slowly varying phase that is similar to Eq. (23). This finally gives a semianalytical expression for the plateau width:

$$\begin{aligned}\frac{\Delta V_{M/2}}{V_F} = {} & \frac{(\pi R/e)M^2}{V\omega_0 \bar{f}^2}(\max_\phi - \min_\phi) \\ & \times \left\{ M\frac{\omega}{\omega_0}\sin\frac{q_0}{2}\sum_{kM\in odd} J_{kM}(A)\left(\frac{\bar{f}}{y}\right)^{2k}\sin(2k\phi) \right. \\ & - M\frac{\omega}{\omega_0}\cos\frac{q_0}{2}\sum_{kM\in even} J_{kM}(A)\left(\frac{\bar{f}}{y}\right)^{2k}\cos(2k\phi) \\ & \left. - \frac{\kappa}{2}\left[1 - J_0(A)\cos\frac{q_0}{2}\right]J_M(A)\cos\frac{q_0}{4}\sin\phi \right\},\end{aligned} \tag{30}$$

where

$$y = \sqrt{V/V_\Sigma - \bar{f}^2} + V/V_\Sigma;\ w = \Omega/\omega_0;\ v = V/V_\Sigma$$

$$\kappa = \bar{f}\left(\frac{v^2}{w^3} - 4\frac{w}{y^2}\right) - \bar{f}^3\left(\frac{2v}{3y^2 w} + \frac{v(w+y)}{w^3 y^2}\right).$$

This coincides with Eq. (25) in the limit of high frequencies and diverges at $\omega \to 0$, invalidating the perturbation theory in this limit.

In Fig. 7 we plot the widths of the half-integer plateaus for a small capacitance $C_d = 0.1$ so we can compare them with the semianalytical prediction obtained, Eq. (30). The deviations such as the shift of position of the cusps, the finite width at the cusp, and the heights of maxima, arise from the higher-order terms in C_d. More details about the width of the half-integer plateaus illustrating the effects of junction asymmetry and q_0 are presented in Fig. 8.

VI. PLATEAUS IN THE WEAK-COUPLING REGIME

The weak-coupling regime occurs at sufficiently big capacitances, $C_d \gg 1$. In this limit the capacitor can be regarded as a voltage source that completely decouples the junctions with respect to ac voltage. Of course, the dc coupling still persists, so the same dc current flows through the junctions, but all interference effects characterized by q_0 dependence eventually disappear in this limit, as well as the fractional current plateaus. Perhaps unexpectedly, the absence of q_0 dependence does not suppress the synchronization of Bloch oscillations by the gate voltage; we see in Fig. 9 well-developed integer current plateaus.

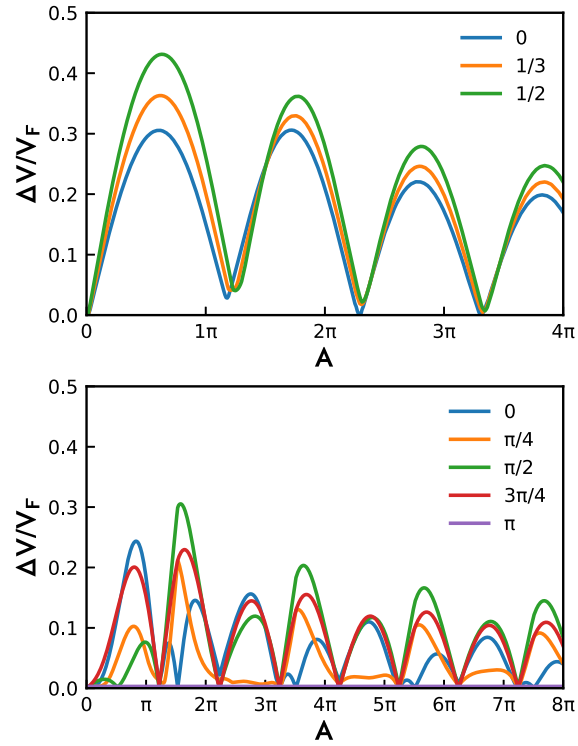

FIG. 8. The widths of 1/2 plateau in dependence on asymmetry of the junctions and q_0, $\omega = 2\omega_0$, $C_d = 0.2$. Upper panel: The width at $q_0 = \pi/2$ vs the driving amplitude for several values of the asymmetry parameter $(V_l - V_r)/(V_l + V_r)$ shown in the labels. Lower panel: The width at $\omega = \omega_0$ vs the driving amplitude for several values of q_0 given in the labels. The setup is symmetric. We observe a rather complex dependence coming from the contributions of various Bessel functions. The data are obtained from Eq. (30). No plateaus persist at $q_0 = \pi$.

To obtain the dynamical equations in this regime, we notice that the big capacitors effectively shortcuts $V_N(t)$ except zero frequency. So in this limit $V_N(t) = \tilde{V}_g(t) + \bar{V}$, $\bar{V}$ not depending on time, $\tilde{V}_g(t)$ has no dc component. With this, Eq. (1) becomes

$$\bar{V} + \tilde{V}_g(t) = V_r \sin q_r + \frac{e}{\pi} R_r \dot{q}_r, \tag{31}$$

$$V - \bar{V} - \tilde{V}_g(t) = V_l \sin q_l + \frac{e}{\pi} R_l \dot{q}_l. \tag{32}$$

So the equations for left and right junctions separate, and each is for a single junction biased by a dc and ac voltage. The only coupling is provided by $\bar{V}$, which is determined from the dc current conservation:

$$\bar{I}_l(V - \bar{V}) = \bar{I}_r(\bar{V}). \tag{33}$$

In the general situation, the solution $\bar{V}$ of this equation is formally ambiguous right at a current plateau, since at the plateau the currents do not depend on voltages. This ambiguity, however, is readily resolved if voltage noise is taken into account. As we discuss in the next section, this results in finite differential conductance at the plateaus and unambiguous solution. In any case, the total width of a plateau is just the sum

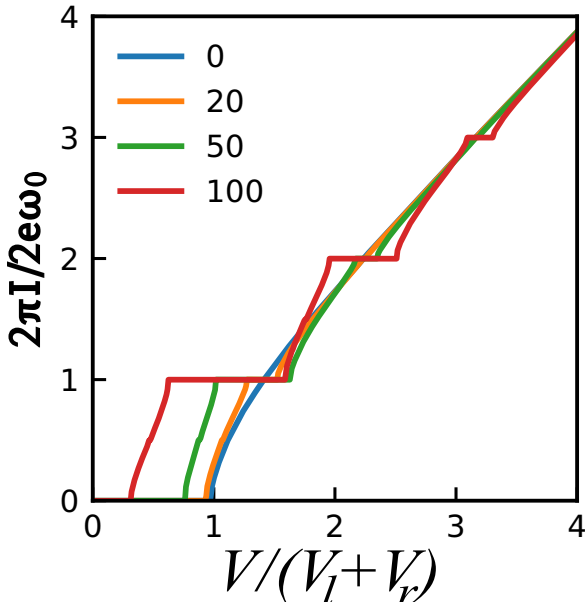

FIG. 9. Plateaus in the weak-coupling regime. Symmetric setup, $C_d = 50$, $\omega = \omega_0$, $q_0 = \pi/2$. The fractional plateaus are hardly visible for such values of C_d, while the integer plateaus remain pronounced. The labels give the induced charge modulation amplitude A as in the previous sSections. We see, however, the change of the scaling: the plateaus become of the order of $V_L + V_R$ at $A \simeq C_d^{-1}$, that is, at the gate voltage modulation amplitude $\tilde{V}_g \simeq V_L + V_R$. In distinction from the strong-coupling regime, the plateau width at a given amplitude is decreasing upon increasing frequency or voltage, $\Delta V \propto \omega^{-1}$.

of the widths for constituent junctions,

$$\Delta V = \Delta V^L + \Delta V^R. \tag{34}$$

For a symmetric setup, this gives $\bar{V} = V/2$, and the I-V characteristic is the same as for a single junction at half voltage and $\tilde{V}_g$ added to the bias voltage,

$$I(V) = I_{\text{single}}(V/2). \tag{35}$$

Let us obtain the analytical prediction for the plateau width in the limit of big frequency. We concentrate on the left junction and chose a harmonic drive:

$$\frac{e}{\pi} R_l \dot{q} = V - \bar{V} - V_l \sin q - \tilde{V}_g \sin(\omega t). \tag{36}$$

Near the kth integer plateau, we neglect V_l and search the solution in the form

$$q(t) = k\omega + \frac{\pi \tilde{V}_g}{eR_l} \cos \omega t + \psi(t). \tag{37}$$

The resulting equation for the slow phase is very similar to Eq. (16),

$$\frac{e}{\pi} R_\Sigma \dot{\psi} + \text{Im}[e^{i\psi} \overline{\mathcal{A}}_k] = \delta V, \tag{38}$$

where

$$\overline{\mathcal{A}}_k = \frac{V_l \omega}{2\pi} \int_0^{\frac{2\pi}{\omega}} dt \exp\left(ik\omega t + i \frac{\pi \tilde{V}_g}{eR_l} \cos \omega t \right). \tag{39}$$

This gives the plateau width for the left junction,

$$\Delta V^L = 2V_l \left| J_k\left(\frac{\pi \tilde{V}_g}{e\omega R_l} \right) \right|, \tag{40}$$

and the overall width

$$\Delta V^L = 2V_l \left| J_k\left(\frac{\tilde{V}_g}{e\omega R_l} \right) \right| + 2V_r \left| J_k\left(\frac{\tilde{V}_g}{e\omega R_r} \right) \right|. \tag{41}$$

This result is somewhat similar to that for the strong-coupling regime [Eq. (41)]: the maximum width is restricted by $V_l + V_r$ and exhibit the Bessel-like dependence on the driving amplitude. We note, however, the disappearance of interference and renormalization of the arguments in the Bessel functions. The arguments are inversely proportional to ω, and this reduces the widths upon increasing ω. However, much smaller amplitudes $\tilde{V}_g$ are required for the argument of the Bessel functions to be of the order of 1: if $\omega \simeq \omega_0$, $\tilde{V}_g \simeq V_{l,r}$ as opposed to $\tilde{V}_g \simeq V_{l,r}/C_d \gg V_{l,r}$ in the strong-coupling regime.

The weak-coupling limit described corresponds to $C_d \to \infty$, and at any finite capacitance up to $C_d \simeq 10^2$ there are still noticeable deviations. We illustrate this in Fig. 10. In the left panel we plot I-V characteristics at different q_0 for $C_d = 10$. The q_0 dependence should be absent in the weak-coupling limit, and the curves should collapse on the single-junction I-V characteristic. We see, however, sizable deviations and even small fractional plateaus. In the right panel we plot the widths of the integer plateaus at fixed gate voltage modulation amplitude $\tilde{V}_g$ (since $A \propto C_d$, the widths vanish at $C_d \to 0$). The widths should saturate in the weak-coupling limit. We see that the saturation is slow and also different for different plateaus.

VII. FINITE-TEMPERATURE EFFECTS

In the previous sections we neglected the finite temperature that in our semiclassical model is manifested as a white voltage noise. This permitted us to concentrate on ideal synchronization, sharp Coulomb blockades, and plateau features. In this section we investigate how the synchronization is gradually destroyed by noise. This is manifested as gradual smoothing and eventual disappearance of blockade and plateau features. This study is especially relevant in the setups including large resistors in view of the dissipation and resulting overheating of the resistors. We numerically solve Eqs. (4) to obtain the I-V characteristics with and without modulation. We use standard modules (Julia language, DifferentialEquations.jl) and consider the solutions for large time intervals to assure the averaging of the results. To achieve the uniform accuracy throughout the parameter space, we found it convenient to use the fixed time step that is commensurate with the (expected) modulation period being a small integer fraction of it. The main goal of this study is to come up with approximate but practical estimations of the temperatures at which the plateaus are still observable. With this, we can also draw semiquantitative predictions beyond semiclassics using the correspondence between the thermal and quantum noise at a plateau developed by modulation with the frequency ω [15] : $k_B T = \hbar\omega$.

We present first the finite temperature effect on the Coulomb blockade feature in the absence of the ac modulation

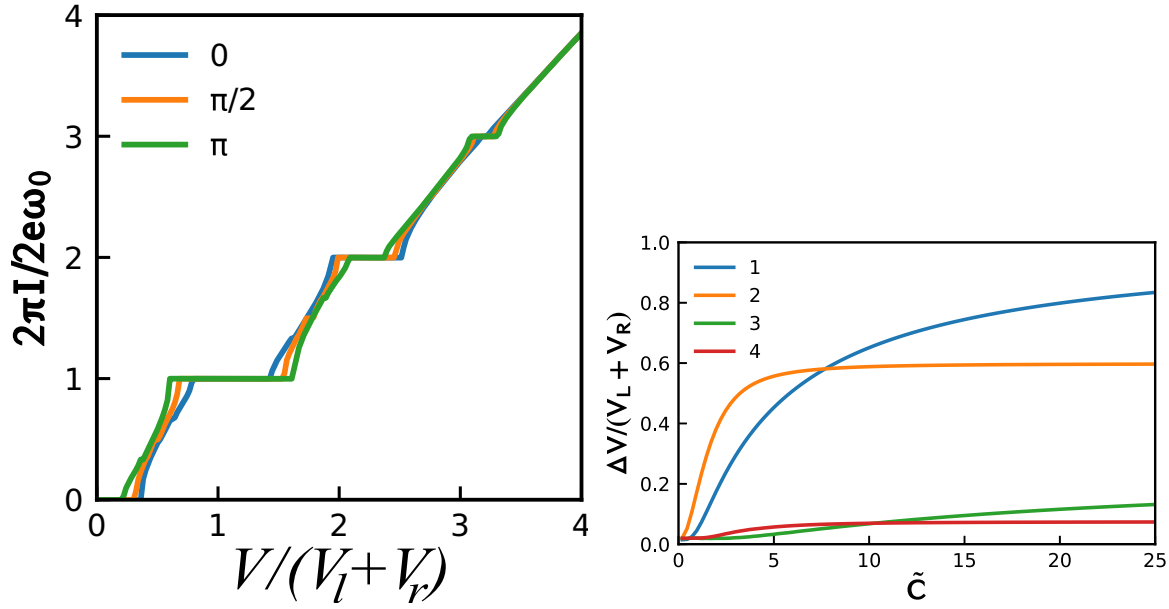

FIG. 10. Approaching the weak-coupling regime. Symmetric setup. Left: I-V characteristics at $C_d = 10$, $A = 20$ and several values of q_0 given in the labels compared with the I-V characteristic of the single junction with $\tilde{V}_g$ added to bias voltage [Eq. (35)]. All these curves should coincide in the limit $C_d \to \infty$. For finite C_d, we see some residual deviations modulated by q_0 and even small fractional plateaus. Right: The plateau width (in units of $V_l + V_r$) of several integer plateaus at fixed ac amplitude $\tilde{V}_g$ (same as that on the left) vs the capacitance C_d. The saturation indicates the weak-coupling regime and occurs at different C_d for different plateaus.

(Fig. 11). The temperature scale at which Coulomb blockade deteriorates should correspond to the Coulomb energy eV_Σ. We incorporate this by introducing a dimensionless temperature $T_d \equiv 8\pi k_B T/eV_\Sigma$. The smoothing of the Coulomb blockade for our setup is qualitatively similar to the smoothing of I-V characteristics in a common Coulomb blockade: at low temperatures, the sharp corner at the threshold is rounded at the scale of this low temperature while the differential conductance remains strongly suppressed; at medium temperatures, the low-voltage conductance becomes a fraction of R^{-1}; at higher temperatures, the Coulomb blockade feature disappears and the I-V characteristics are almost linear. In Fig. 11 we compare the results for strong- and weak-coupling regimes, choosing $q_0 = 0$ where the

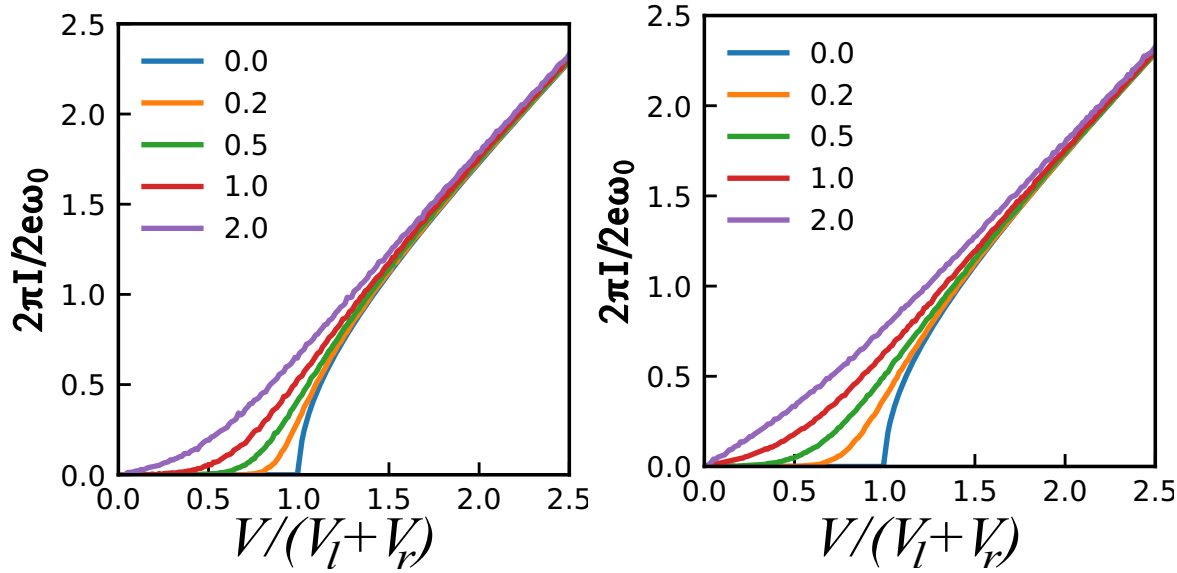

FIG. 11. Smoothing of the Coulomb blockade feature by finite temperature. I-V characteristics for several dimensionless temperatures $T_d = 8\pi k_B T/eV_\Sigma$. Symmetric setup, $q_0 = 0$. Left: $C_d = 0.1$, strong-coupling regime. Right: $C_d = 50$, weak-coupling regime. Upon increasing the temperature, we see first the rounding of the sharp feature at the threshold, then finite conductance at zero voltage, and finally a linear I-V characteristic. The same degree of smoothing in the weak-coupling regime occurs at approximately half of the temperature at which it occurs in the strong-coupling regime.

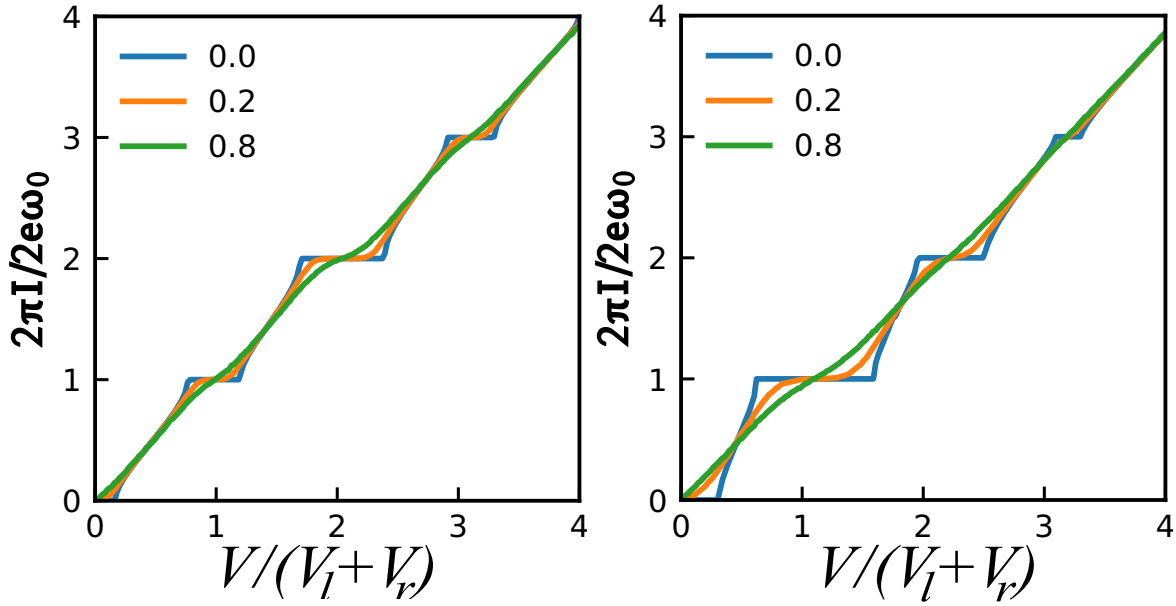

FIG. 12. Smoothing of current plateaus at finite temperature. I-V characteristics of symmetric setup under gate voltage modulation with $\omega = \omega_0$ at dimensionless temperatures T_d shown in the labels. Left: Strong-coupling regime, $C_d = 0.2$, $q_0 = \pi/2$, the induced charge modulation $A = 6$. Left: Weak-coupling regime, $C_d = 50$, the voltage gate modulation $A = 100$ with $q_0 = \pi/2$. At the same temperature, the degree of smoothing is bigger for the plateaus of smaller width. The same degree of smoothing in the weak-coupling regime occurs at twice smaller temperature as compared with the strong-coupling regime.

Coulomb blockade thresholds are maximized and equal in both limits. We see that for the symmetric setup the same degree of smoothing in the weak-coupling regime requires twice smaller temperature as compared to the strong-coupling regime. This is explained by the fact that the height of the Coulomb barrier is twice smaller in the weak-coupling regime. Indeed, since the junctions are uncoupled, the Coulomb barriers are determined by $eV_{l,r}$ as compared to $e(V_l + V_r)$ in the strong-coupling regime.

The smoothing of the well-developed integer plateaus with $\Delta V \simeq V_\Sigma$ follows the same pattern (Fig. 12). Also here the same degree of smoothing occurs at approximately twice smaller temperature in the weak-coupling regime. One can see it, for instance, for the second plateau that is slightly wider in the weak-coupling regime but is more smoothed at the same temperature. We also see that the smaller plateaus are smoother at the same temperature. This leads us to a simple scaling hypothesis: for each plateau, the degree of smoothing is defined by the temperature relative to the plateau width (c.f. [41]). To check the hypothesis, we need to choose a measure of smoothing.

To do this we note that a common experimental signature of imperfect plateaus is the peaks in differential resistance. Typical current dependences of the differential resistance for various temperatures are plotted in Fig. 13. There, we see the peaks at the quantized values of the current that diverge at vanishing temperature, take finite value at finite temperatures, and eventually merge with the background $\approx R_\Sigma$ at higher temperatures. We define the width of the plateaus at finite temperature as the length of the voltage interval where the differential conductance exceeds the background resistance at least by a factor of Q, and choose $Q = 3$. With this definition, the plateau widths becomes zero at some critical temperature where the peak differential resistance is thrice the background. Despite the arbitrariness of this definition, it seems to be a reasonable practical compromise. To extract the so-defined width numerically, we change voltage in small steps near the quantized values of the current, checking the differential conductance at each step.

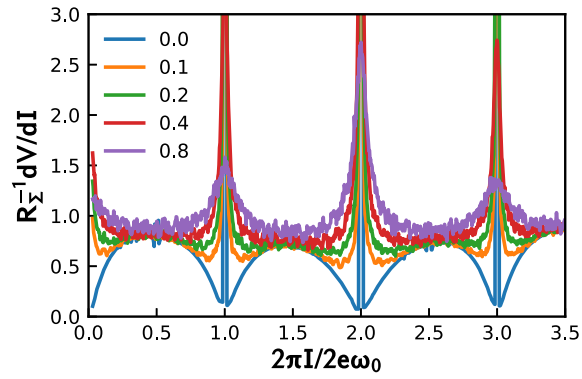

FIG. 13. The differential resistance vs current. Symmetric setup, $C_d = 0.2$, ac voltage modulation at $\omega = \omega_0$, $A = 6$, the dimensionless temperature T_d is given in the labels. The resistance is obtained numerically from I-V characteristics taken at discrete values of voltage with the current step $0.03\frac{2e\omega_0}{2\pi}$. The noise in the data comes from the actual noise: To obtain I-V curves, we average the current over a finite time interval picking up its fluctuations. The smoothed plateaus are manifested as the peaks of differential resistance. The height of the peaks decreases with increasing temperature. We define the "width" of the plateau at finite temperature as the length of the voltage interval where the differential resistance exceeds the background differential resistance $\simeq R$ by at least a factor of 3.

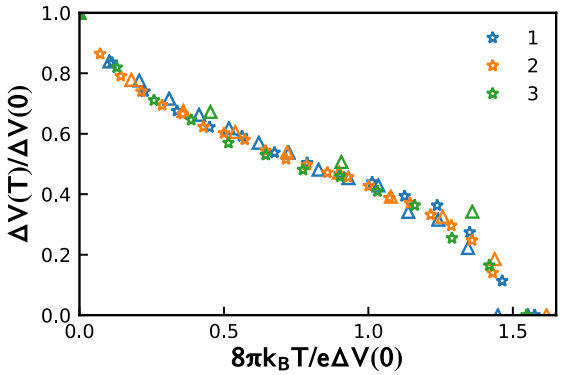

FIG. 14. The scaling of the integer plateau smoothing with temperature. We check a simple scaling hypothesis $\Delta V(T)/\Delta V(0) = f(k_BT/eV(0))$ and see the data collapsing into the same universal curve for both weak- and strong-coupling regimes and various plateaus. For the weak-coupling regime, we correct the temperature by a factor of 2. The data for the strong-coupling regime ($C_d = 0.2$, $A = 6$, $q_0 = \pi/2$) are plotted with stars, those for the weak-coupling regime ($C_d = 50$, $A = 100$) are plotted with triangles, the color of the star/triangle corresponds to first, second, and third plateaus as shown in the labels, $\omega = \omega_0$ for all situations.

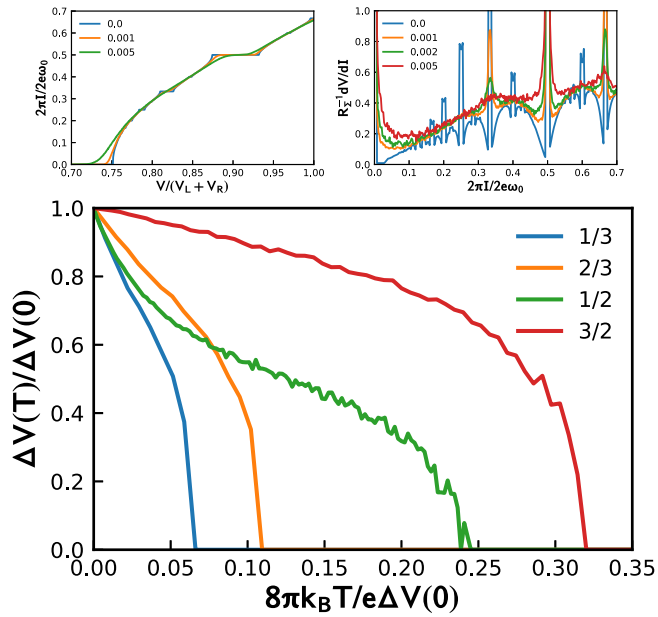

FIG. 15. Failure of the simple scaling hypothesis for fractional plateaus. The data are for symmetric setup, $\omega = \omega_0$, $A = 4$, $q_0 = \pi/2$, $C = 5$. Upper panel left: The I-V characteristics for various dimensionless temperatures T_d marked in the labels. Lower panel: Temperature-dependent plateau width for a set of fractional plateaus vs the temperature in units of the width obtained at current step $\Delta I = 0.01\frac{2e\omega_0}{2\pi}$. In contrast to Fig. 14, the curves are different for different fractions; there is no universal scaling.

The simple scaling hypothesis would imply that the temperature-dependent width in units of zero-temperature width is a universal function of temperature in units of the zero-temperature width:

$$\frac{\Delta V(T)}{\Delta V(0)} = f\left(\frac{k_BT}{e\Delta V(0)}\right). \tag{42}$$

To check the hypothesis, we plot (Fig. 14) the evaluated widths of several plateaus in coordinates $\Delta V(T)/\Delta V(0)$, $T_dV_\Sigma/\Delta V(0)$. We plot the data for both the strong- and weak-coupling regimes, correcting the temperature by a factor of 2 in the latter case. We see a good collapse of the data into a single curve despite significantly different widths of the plateaus. We conclude that the width of a plateau is halved at $k_BT \approx 0.03e\Delta V(0)$ and vanishes at

$$k_BT_c \approx 0.06e\Delta V(0). \tag{43}$$

The suggested scaling is not exact in any obvious limit; in fact, since we have to correct the weak-coupling regime data, it would not work in between the regimes at $C_d \simeq 1$, albeit it seems to work empirically.

To convert it into a quantum noise estimation, we substitute $k_BT_c = \hbar\omega$ and $\omega = \omega_0$. This gives a minimum value of the resistance R_Σ at which the plateau is still observable,

$$R_c \approx 16\frac{\pi\hbar}{e^2}\frac{V_\Sigma}{\Delta V(0)}. \tag{44}$$

Being encouraged with the success of the simple scaling hypothesis for the integer plateaus, we analyze the effect of finite temperature on the fractional plateaus in the intermediate regime $C_d \simeq 1$. The results are presented in Fig. 15. We observe there pronounced fractional plateaus at vanishing temperature, with the width up to $\simeq 0.1V_\Sigma$. However, they vanish rather quickly, at temperatures of two orders of magnitude lower than the integer ones. One could think that this is due to the smaller widths of the plateaus, so we check the simple scaling hypothesis plotting the temperature-dependent width in coordinates $\Delta V(T)/\Delta V(0)$, $T_dV_\Sigma/\Delta V(0)$. We do not find a correspondence with the scaling of integer plateaus: the critical temperatures in units of width are at least a factor of 5 lower and decrease with increasing denominator. There is no scaling for different fractions, even for those with the same denominators. This may be explained by the fact that the shape of the effective energy barrier for fractional plateaus is different from that for integer plateaus and is different from fraction to fraction. In conclusion, the fractional plateaus can only be observed at temperatures two orders of magnitude lower than the integer ones.

VIII. CONCLUSIONS

In conclusion, we propose to synchronize Bloch oscillations in a double-phase-slip junction by modulating the gate voltage. This is advantageous in comparison with the bias voltage modulation, since the ac signal does not produce extra dissipation that may kill the synchronization by overheating. We show that ac modulation gives rise to the pronounced plateaus of quantized current of width V_Σ corresponding to optimistic estimations for bias voltage modulation.

We distinguish and investigate in detail three regimes corresponding to the ratio of the gate capacitance C and effective junction capacitance V_Σ/e. The strong-coupling regime $C \ll V_\Sigma/e$ is characterized by strong interference of the phase slips that is tuned by q_0, the charge induced by the dc part of the gate voltage. Well-developed plateaus are achieved at

ac-induced charge $\tilde{q}_g \simeq e$ corresponding to ac modulations. The interference is suppressed in the opposite regime of weak coupling, $C \ll V_\Sigma/e$. The well-developed plateaus require bigger induced charge amplitudes $\tilde{q}_g \simeq CV_\Sigma$ but smaller gate voltage amplitudes $\tilde{V}_g \simeq V_\Sigma$. Interestingly, well-developed fractional plateaus are developed in the intermediate regime of $C \simeq V_\Sigma/e$.

We investigate the effect of finite temperature on the smoothing of plateaus in all three regimes. The smoothing of integer plateaus is found to obey an empirical scaling law: the degree of smoothing is determined by the temperature in units of the plateau width. No such scaling was found for fractional plateaus that are only observable at temperatures two orders of magnitude lower than the integer ones.

To support open science and open software initiatives and to comply with institutional policies, we have published all relevant code and instructions for running it on the Zenodo repository [43].

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