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***Abstract*— In this article, a novel fan-out panel-level printed circuit board (PCB)-embedded package for phase-leg silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) power module is presented. Electro-thermo-mechanical co-design was conducted, and the maximum package parasitic inductance was found to be about 1.24 nH at 100 kHz. Compared with wire-bonded packages, the parasitic inductances of the PCB-embedded package decreased at least by 87.6%. Compared with blind via structure, the thermal resistance of the proposed blind block structure reduced at most by about 26%, and the stress of the SiC MOSFETs decreased by about 45.2%. Then, a novel PCB-embedded packaging process was developed, and three key packaging processes were analyzed. Furthermore, effect of PCB-embedded package on static characterization of SiC MOSFET was analyzed, and it was found that: 1) Output current of PCB-embedded package was decreased under a certain gate–source voltage compared to SiC die; 2) Miller capacitance of SiC MOSFET was increased thanks to parasitic capacitance induced by package; and 3) compared with SiC die, nonflat miller plateau of the PCB-embedded package extends, and as drain–source voltage increases, the nonflat miller plateau extends. Lastly, switching characteristics of the PCB-embedded package and TO-247 package were compared. The results show that the PCB-embedded package has smaller parasitic inductances.**

***Index Terms*— Electro-thermo-mechanical codesign, printed circuit board (PCB)-embedded package, phase-leg silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) power module, static characterization, switching characterization.**

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I. Introduction

SILICON carbide (SiC) is a promising semiconductor material under high operating temperature, high blocking voltage, and high switching frequency applications due to its excellent electrical and thermal properties. Compared with Si counterparts, wide bandgap energy and low intrinsic carrier concentration of 4H-SiC enable SiC devices to operate at much higher temperature (approximately five times higher than Si) [1]–[5]. 4H-SiC also possess a higher breakdown field strength (ten times of Si), which allows SiC power devices to have a much thinner drift region and higher doping concentration for a given voltage rating than their Si counterparts. The thinner and higher doping drift region greatly reduces specific on-resistance of the SiC devices, facilitating the use of unipolar SiC power metal-oxide-semiconductor field-effect transistor (MOSFET) device. The SiC MOSFETs reported to date already significantly outperform any available Si counterparts at the same voltage rating in terms of reduced switching losses and at least 5–10 times higher switching frequencies [6]. Compared with Si counterparts, SiC MOSFET has a smaller chip size, resulting in significantly reduced internal parasitic capacitances, hence a much faster intrinsic switching speed [7]. Therefore, SiC MOSFET has the potential to revolutionize the industry of power electronics.

In a power module, the superior properties of a SiC MOSFET cannot be exploited if it is used simply as a direct drop-in replacement of Si device [8]. Owing to the fast switching speed capability, the switching characteristics of SiC MOSFET are more susceptible to parasitic elements, such as the parasitic inductances of interconnections and parasitic capacitances [9]. The high dv/dt at turn-on transient easily leads to the arm crosstalk due to the miller capacitance and the high di/dt at turn-off transient easily induces voltage overshoot thanks to the parasitic inductance [10].

Up to now, conventional wire-bonded interconnection is still the most preferred technology for packaging SiC MOSFET. However, wire-bonds have an inherent parasitic inductance that can exceed 10 nH [11], an excessive voltage overshoot of a wire-bonded SiC MOSFET package is easily produced at high speed switching transients. The large voltage overshoot may damage the SiC MOSFET by exceeding its absolute maximum ratings, increasing power losses, introducing substantial electromagnetic interference (EMI) noise, thereby affecting

the reliability of the MOSFET [11], [12]. In order to avoid the large overshoot, low inductance design of SiC MOSFET package is needed.

Moreover, power density of SiC MOSFET is higher than those of Si counterparts due to the smaller size. And power loss generated by SiC MOSFET increases with frequency, most of it is only dissipated through the bottom side of the wire-bond package. A cooling system that can remove the heat through dual sides will be much more efficient.

Besides, with the wire-bonded interconnection structure, under high ambient temperature or high operating temperature, thermally induced stress/strain resulting from the coefficient of thermal expansion (CTE) mismatch among the constituent materials could lead to wire failure, die attach (DA)/die crack, package warpage, etc. [13].

New packaging interconnection techniques need to be developed to push the development of SiC power module. So far, several wire-bondless interconnection packages for SiC MOSFET module have been developed, e.g., planar packaging, press-pack, and 3-D packaging.

As a wire-bondless interconnection technology, printed circuit board (PCB) embedded SiC MOSFET package is a potential solution with small form factor, lightweight, and simple process technology. PCB-embedded package, also called "Chip in Polymer" technology, was first introduced by Fraunhofer IZM and TU Berlin. The ultrathin semiconductor chips were embedded into the build-up layers of PCB together with integrated passive components. Electrical interconnection between chip and outer-layer footprints were realized by laser-drilled and metallized microvias [14]–[16].

In recent years, PCB-embedded packaging technology has been applied to power module. This mainly includes two types of process flows: face-up and face-down processes [17]. The DA materials used in the two processes are different. For face-down process, it is a nonconductive adhesive, whereas for face-up technology, except for nonconductive adhesive, it can also be solder, sintered Cu/Ag, etc. The latter is more suitable for high power-density vertical dies, such as insulator gate bipolar transistor (IGBT), power diode, power MOSFET, etc.

There have been some developments in the PCB-embedded power module. Leadframe-based PCB-embedded packaging technology is one of the major representatives [18], [19]. The power dies are soldered or sintered onto a Cu leadframe, and the resulting assembly is then fully embedded in a prepreg or resin-coated copper (RCC) material. Electrical interconnection of the dies with outer layers is realized through PCB vias and redistribution layers (RDLs). Besides, Pascal *et al.* [20] proposed an innovative PCB-embedded packaging technology. They used a piece of nickel foam to create a pressed contact between the top side of a PCB-embedded power die and the rest of the circuit. AT&S developed a panel-level PCB-embedded technology known as embedded component packaging (ECP) [21]. Yang *et al.* [22] presented a PCB-embedded power MOSFET. The power MOSFETs were soldered onto a Cu foil with a solder resist pattern and embedded in an RCC foil. However, all these package structures are asymmetrical in the thickness direction, which could easily cause larger stress and strain under harsh environments.

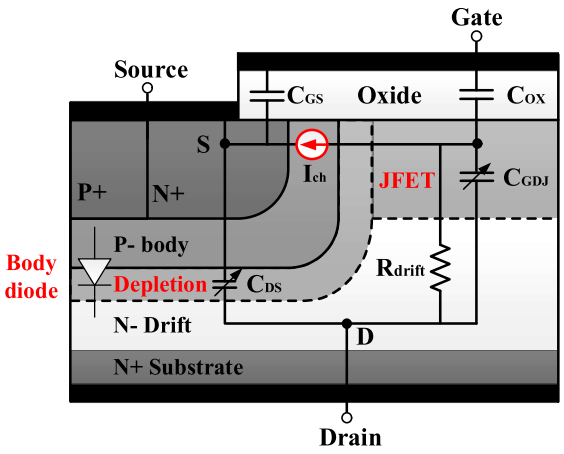


Fig. 1. Typical structure of half SiC DMOSFET cell with equivalent parasitic capacitances.

Besides, heat generated by power devices is mainly dissipated into the ambient only through bottom side. Symmetry package structure with double-sided cooling can relieve the thermally induced stress and improve the heat dissipation performance of the PCB-embedded power module.

Up to now, there are few reports on PCB-embedded SiC MOSFET power module. Scientific challenges in the design and implementation of PCB-embedded SiC MOSFETs packaging, e.g., heat dissipation, thermo-mechanical reliability, and packaging process, have not been well dealt with. After packaging, accurate characterization of the custom module is also a challenge. These issues must be handled more carefully in the development of SiC MOSFET power module packaging.

In Section II of this article, SiC MOSFET and phase-leg power module were introduced. In Section III, a novel fan-out panel-level PCB-embedded packaging technique for SiC MOSFET power module was proposed. In Section IV, electro-thermo-mechanical co-design of the PCB-embedded SiC MOSFETs package was conducted. In Section V, a brief description of process flow of the PCB-embedded package was given, key PCB-embedded packaging process and failure analysis were performed, and improved package process was suggested. In Section VI, the static characteristics of SiC MOSFET and PCB-embedded package were analyzed and compared. The effects of PCB-embedded package on $I-V$, $C-V$, and gate charge characteristics of SiC MOSFET were investigated, respectively. In Section VII, the switching characteristics of SiC MOSFET in the PCB-embedded phase-leg power module and the TO-247 discrete package were analyzed and compared.

II. SiC MOSFET And Phase-Leg Power Module

SiC MOSFET comprises more than 10 000 small parallel-connected N-Channel enhancement mode MOSFET cells. A cross section of half DMOSFET cell with equivalent parasitic capacitances is illustrated in Fig. 1 [23]. The SiC MOSFET device is fabricated by beginning with an N-drift layer grown on a heavily doped N+ substrate. The drift layer is sandwiched between N+ substrate and p-body, creating a

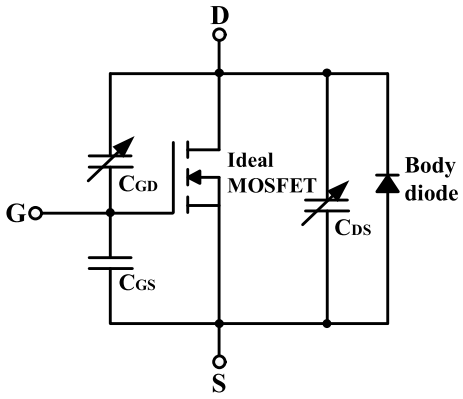


Fig. 2. Equivalent circuit model of the SiC MOSFET.

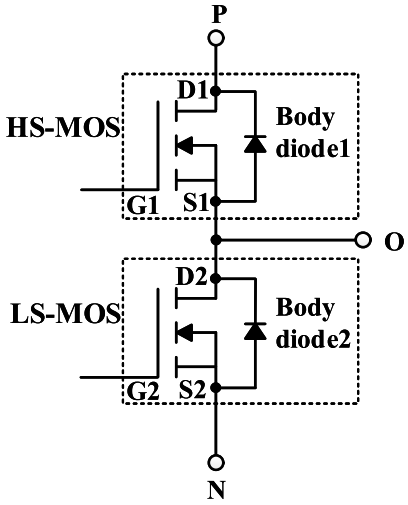


Fig. 3. Circuit diagram of phase-leg SiC MOSFET power module.

vertical body diode. The body diode is a PiN diode and is anti-parallel with the SiC MOSFET channel. The foremost characteristic of PiN diode is in the turn-off transient where reverse recovery can be observed as a result of minority carrier extraction from the drift layer [24], [25].

Fig. 2 shows the equivalent circuit model of the SiC MOSFET. It is composed of an ideal MOSFET which is described as a voltage-controlled current source, three parasitic capacitances, and an anti-parallel body diode. Parasitic capacitances of SiC MOSFET include gate–source capacitance (C_{GS}), drain–source capacitance (C_{DS}), and gate–drain capacitance (C_{GD}) [9], [10], [23]. C_{GS} consists of a constant overlap oxide capacitance between gate and source and a constant capacitance between gate and source metallization, which are in parallel. C_{DS} is the bias-dependent depletion capacitance of P-body/N-drift junction and is given by

$$C_{DS} = C_{DS0}\left(\frac{V_{bi}}{V_{bi} + V_{DS}}\right)^{M} \tag{1}$$

where C_{DS0} is a constant, V_{bi} is the built-in potential between P-body and N-drift junction, and M is a fitting parameter.

Fig. 3 shows a circuit diagram of phase-leg SiC MOSFET module, which consists of a high-side SiC MOSFET (HS-MOS) and a low-side SiC MOSFET (LS-MOS). Body diode in the SiC MOSFET is utilized to replace external freewheeling diode. Unlike traditional Si devices, SiC MOSFET has shorter lifetime of minority carriers so that not a large reverse recovery current is estimated, which enables the body diode of the SiC MOSFET to be a brilliant diode with almost no reverse recovery charge and forward recovery voltage [24].

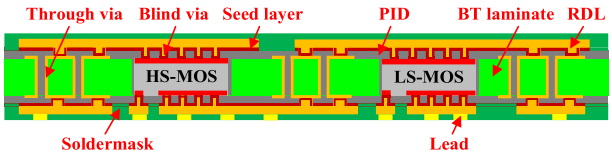


Fig. 4. Structure schematic of the PCB-embedded SiC MOSFETs package.

TABLE I
GEOMETRY STRUCTURE SIZE OF EACH COMPONENT

Component	Size (mm)
Chip	3.36×3.10×0.186
Soldermask	15×15×0.04
PID	15×15×0.04
Chip pitch	6
BT laminate	15×15×0.186
Through via	Diameter = 0.15, Pitch = 0.4
Blind via	Diameter = 0.1, Pitch = 0.2
RDL thickness	0.025

III. FAN-OUT PANEL-LEVEL PCB-EMBEDDED PACKAGING

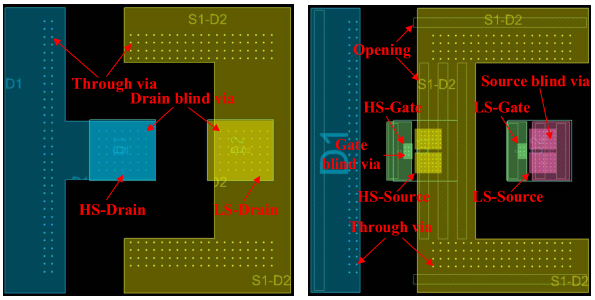
A. Packaging Structure

Fig. 4 shows the structure schematic of the fan-out panel-level PCB-embedded package for phase-leg SiC MOSFET power module. The package mainly consists of a pair of SiC dies (HS-MOS and LS-MOS), PCB-embedded material (BT laminate), photo imageable dielectric (PID), electrical interconnection (seed layers, RDLs, blind vias, and through vias), and lead. Geometry size of each component is listed in Table I.

The SiC MOSFETs are embedded in the PCB. Electrical interconnection between SiC MOSFETs and out-layer footprint is realized by PCB vias and RDLs. Compared with conventional wire-bonded interconnections, the PCB-embedded technology eliminates Al wire-bonds, direct bond ceramic (DBC) substrate, DA, and encapsulation structure, manufacturing processes are, accordingly, simplified. The PCB-embedded SiC MOSFET power module has merits of lightweight, thin profile, low parasitic inductances, structure symmetry, double-sided cooling, etc.

B. Packaging Materials

In order to withstand high-temperatures beyond 175 °C and high-voltages over 1200 V, and improve thermo-mechanical reliability of the PCB-embedded SiC MOSFETs,



(a) (b)

Fig. 5. Packaging layout of the PCB-embedded SiC MOSFETs. (a) Front-side. (b) Backside.

copper clad laminate (CCL-HL832NSF) and prepreg (GHPL-830NSF) from Mitsubishi Gas Chemical were selected. CCL-HL832NSF was a double-sided copper-clad BT laminate (E-glass fiber-reinforced BT resin) with high Tg and low CTE. And GHPL-830NSF was a sheet of BT prepreg (E-glass fiber-reinforced uncured BT resin). In order to obtain the BT laminate with almost the same thickness as the SiC die, BT prepreg was used. In our previous work [27], characterization of the PCB-embedded package materials for SiC MOSFETs were performed. The experimental results showed that the PCB-embedded materials could withstand high temperatures beyond 200 °C and high voltages above 1200 V. Tg was as high as over 260 °C and CTE matched well with SiC. Besides, a novel PID film was used as a laminating dielectric material.

C. Packaging Layout

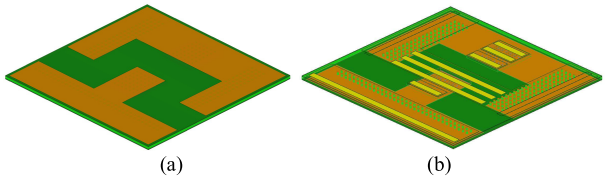
Fig. 5 displays front-side and backside of the PCB-embedded SiC MOSFETs packaging layout. The package has a size of 15 × 15 × 0.36 mm^3. The Cu coverage of front-side and backside RDL is about 63% and 57%, respectively, so the package will take on a "smile" shape when cooling down from stress-free high temperature.

IV. Electro-Thermo-Mechanical Codesign

In order to evaluate the electrical, thermal, and mechanical performances of the PCB-embedded SiC MOSFETs, the electro-thermo-mechanical co-design was performed. Parasitic inductances of the PCB-embedded SiC MOSFETs package were first extracted, and the effects of switching frequency on parasitic inductances were analyzed. Then, thermal modeling was conducted to verify the heat dissipation performance of the package. Thirdly, thermo-mechanical virtual prototyping was applied to analyze the mechanical behavior of the package.

A. Package Parasitic Inductances Extraction

Parasitic inductances induced by package structure are especially critical for fast switching of SiC MOSFETs. The ANSYS Q3D Extractor was used to extract parasitic inductances of the PCB-embedded SiC MOSFETs. Fig. 6(a) and (b) shows the extraction model of the PCB-embedded SiC MOSFETs package. Table II lists the definitions, sources, and sinks of the package parasitic inductances.



(a) (b)

Fig. 6. Extraction model of the PCB-embedded SiC MOSFETs package. (a) Front-side. (b) Backside.

TABLE II
Definitions, Sources, and Sinks of Package Parasitic Inductances

Parasitic inductance	Definition	Source	Sink
L_{D1}	HS-MOS drain inductance	Interfaces between blind vias and HS-MOS drain	P terminal
L_{G1}	HS-MOS gate inductance	Interfaces between blind vias and HS-MOS gate	GD1 terminal
$L_{S1\text{-}O}$	HS-MOS source inductance	Interfaces between blind vias and HS-MOS source	O terminal
$L_{O\text{-}D2}$	LS-MOS drain inductance	Interfaces between blind vias and LS-MOS drain	O terminal
L_{G2}	LS-MOS gate inductance	Interfaces between blind vias and LS-MOS gate	GD2 terminal
L_{S2}	LS-MOS source inductance	Interfaces between blind vias and LS-MOS source	N terminal

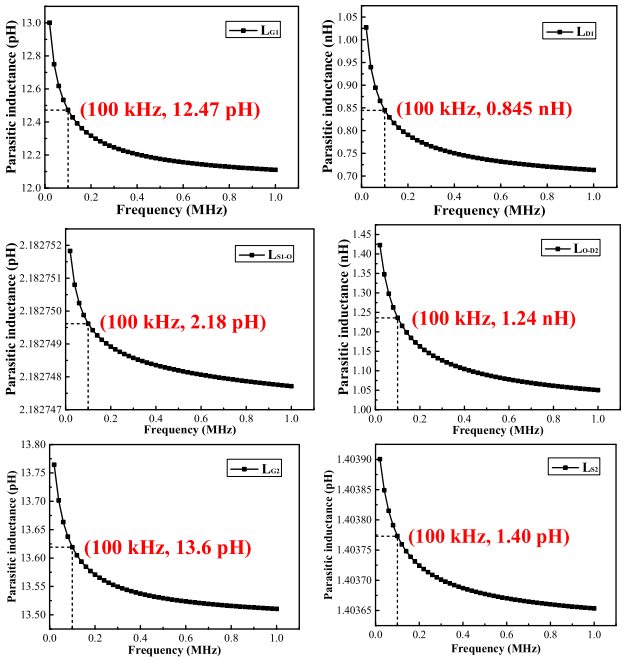


Fig. 7. Parasitic inductances of the PCB-embedded SiC MOSFETs package dependent on switching frequency.

Fig. 7 shows the parasitic inductances of the PCB-embedded SiC MOSFETs package dependent on frequency. The sweep frequency range was 20 kHz–1 MHz. As shown in the figures, the parasitic inductances of the PCB-embedded package decreased with the frequency due to the skin and proximity effect. From 20 to 200 kHz, the parasitic inductances dropped evidently. When the frequency kept on increasing

from 200 kHz to 1 MHz, the parasitic inductances decreased slowly and leveled off.

From Fig. 4, it can be seen that the drains of the two MOSFETs are connected to the package terminals by blind vias, front-side RDLs, through vias, and backside RDLs, whereas the sources and gates are connected to the package terminals through blind vias and backside RDLs, so the drain inductances are much higher than the source/gate inductances. As shown in Fig. 7, the HS-MOS drain inductance L_{D1} is about 0.845 nH at 100 kHz, and LS-MOS drain inductance L_{O-D2} is about 1.24 nH at 100 kHz which is the largest in the package. Other parasitic inductances in the package are lower than 15 pH. Compared with conventional wire-bonded packages, in which parasitic inductances exceed 10 nH, Therefore, the parasitic inductances of the PCB-embedded package decreased by 87.6% at least.

B. Thermal Modeling Analysis

Thermal conductivities of PCB-embedded materials are relatively low. Furthermore, heat flux of SiC MOSFET is higher than those of Si counterparts with the same voltage rating due to smaller size and higher switching frequency, so more efficient cooling solution for PCB-embedded SiC MOSFETs package is required. Conventional single-sided cooling design is difficult to achieve the heat dissipation requirement. A cooling method that could remove the heat through double-side will be much more efficient.

As shown in Fig. 4, SiC MOSFETs are communicated with outer interconnection layers through blind vias in the PID film. The blind vias are filled with Cu through sputtering and plating. However, because the diameter of blind via is only 100 μm, Cu coverage above the pads of SiC MOSFETs is relatively low, which is only about 3.2%. In order to improve the heat dissipation of the PCB-embedded SiC MOSFETs package, it is necessary to increase the Cu coverage above the die pads. However, if only increasing the amount or diameter of blind via, the increase of Cu coverage above the chip pads is limited.

In this article, blind block was proposed to increase the Cu coverage above the die pads, thus improving the heat dissipation capability of the PCB-embedded SiC MOSFETs. The blind block can be formed by PID exposure and development, panel-level physical vapor deposition (PVD), and RDL interconnection techniques. The structure diagram of blind block above the SiC MOSFET pads is shown in Fig. 8(a) and (b), respectively.

Fig. 9 shows a compact thermal resistance network model of the PCB-embedded SiC MOSFETs. The model includes junction-to-case thermal resistance (θ_{JC}) and junction-to-board thermal resistance (θ_{JB}) of the PCB-embedded package.

θ_{JB} and θ_{JC} of the PCB-embedded package were analyzed through ANSYS ICEPAK. Table III compares the thermal resistances of the blind via and blind block structures. From the table, it can be calculated that the thermal resistance of the proposed structure reduced by about 26% at most.

C. Thermo-Mechanical Virtual Prototyping

Prior to PCB-embedded SiC MOSFETs packaging process, thermo-mechanical simulation was carried out using ANSYS Mechanical APDL to provide guidelines. Effect of Cu coverage above the chip pads on von Mises stress was optimized.

Table IV lists thermo-mechanical properties of the packaging materials. The storage modulus, loss modulus, and tan delta of the BT laminate dependent on temperature are shown in Fig. 10. As shown in the figure, Tg of the laminate was up to 275 °C, which was much higher than most other PCB materials. For other materials, SiC was considered as isotropic and elastic. Cu RDL and electroplated blind vias were assumed

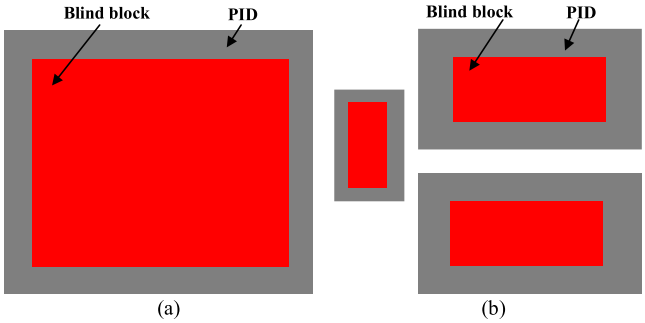


Fig. 8. Structure diagram of blind block above the MOSFET pads. (a) Drain. (b) Gate and source.

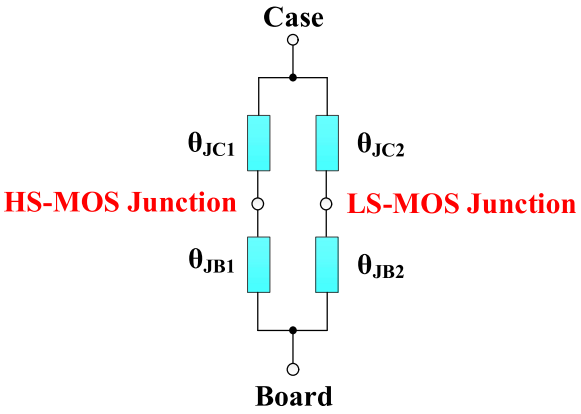


Fig. 9. Compact thermal resistance network model of the PCB-embedded SiC MOSFETs package.

TABLE III
COMPARISON OF THERMAL RESISTANCE BETWEEN THE BLIND VIA AND THE BLIND BLOCK STRUCTURE

Structure above pads	θ_{JC1} (K/W)	θ_{JC2} (K/W)	θ_{JB1} (K/W)	θ_{JB2} (K/W)
Blind via	0.502	0.522	0.262	0.558
Blind block	0.386	0.386	0.256	0.455

TABLE IV
THERMO-MECHANICAL PROPERTIES OF THE PACKAGING MATERIALS

Component	Material	Tg (°C)	E (GPa)	CTE (ppm/°C)	υ
MOSFET	4H-SiC		400	5.1	0.14
BT laminate	832NSF	275 °C	See Fig. 10	α1=5.3; α2=3	0.18
PID	PVI-3 HR100S	160-165	3.5	α1=45; α2=120	0.3
RDL	Cu		129	17.3	0.34
PCB via	Cu		129	17.3	0.34

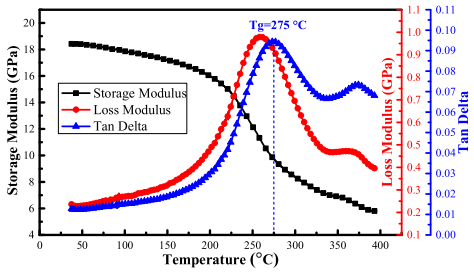


Fig. 10. Storage modulus, loss modulus, and tan delta of the BT laminate dependent on temperature.

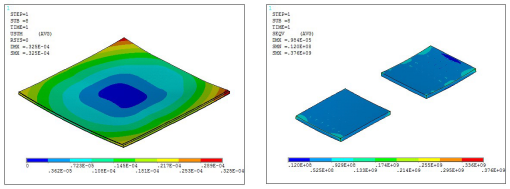


Fig. 11. Simulation results. (a) Warpage of PCB-embedded package. (b) von Mises stress of SiC MOSFETs.

as elastoplastic. The material properties of PID and soldermask were taken from the vendors' datasheets.

When conducting thermo-mechanical simulation of the PCB-embedded package, the initial reference temperature of the finite element model was set to be baking temperature of 175 °C, the final room temperature was 25 °C, and the bottom center point of the model was fixed. Besides, perfect adhesion was assumed between all material interfaces, manufacturing tolerances of dimensions were not considered [29]–[31].

Fig. 11(a) shows the warpage of the PCB-embedded SiC MOSFETs after high-temperature baking. The package takes on an approximately isotropic "smile face" shape due to asymmetrical chip layout, which is consistent with the previous analysis. The maximum warpage is about 32.5 μm, which is lower than 0.5% of the package diagonal length. Fig. 11(b) illustrates the von Mises stress distribution of SiC MOSFETs. From the figure, it can be seen that the maximum von Mises stress is 376 MPa, which occurs at the corner of the MOSFET.

From Table IV, it can be seen that CTE of PID is relatively higher than that of SiC and Cu, CTE mismatch between the SiC MOSFET and the PID film could lead to higher stress. In this article, effect of blind slit and blind block structures on von Mises stress of SiC MOSFET were analyzed and compared. The structure diagram of blind slit and block above the drain are shown in Fig. 12(a) and (b), respectively.

Fig. 13(a) and (d) shows the von Mises stress of the HS-MOS and LS-MOS in different structures. Compared with blind via structure, the proposed blind block structures relieved the von Mises stress of SiC MOSFETs, and von Mises stress of the SiC MOSFETs decreased by about 45.2%.

V. PCB-Embedded Packaging Process

The detailed packaging process flow of the PCB-embedded SiC MOSFETs is depicted in Fig. 14. The key techniques

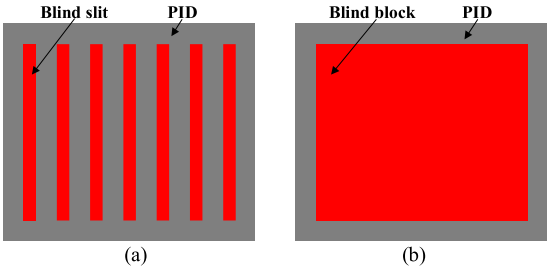


Fig. 12. Structure diagram of (a) blind slit and (b) blind block above the MOSFET drain.

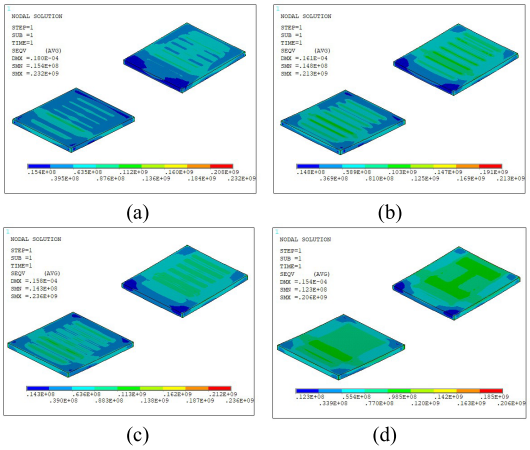


Fig. 13. Effect of Cu coverage above the chip pads on von Mises stress of SiC MOSFETs. (a) Blind slit width: 100 μm. (b) Blind slit width: 200 μm. (c) Blind slit width: 300 μm. (d) Blind block.

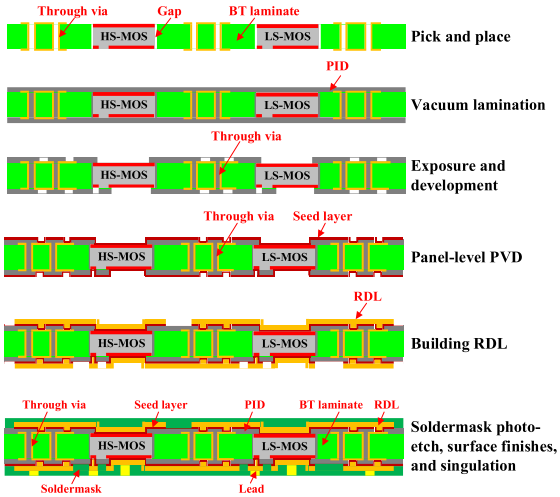
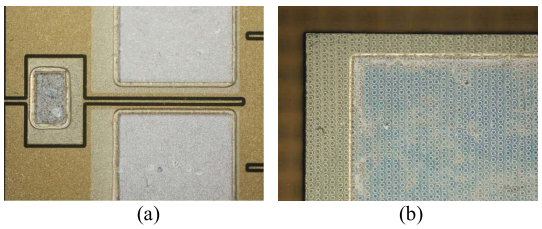


Fig. 14. Process flow of the PCB-embedded SiC MOSFETs.

of the packaging process mainly include PID exposure and development, panel-level double-sided PVD, and double-sided RDL interconnection techniques.

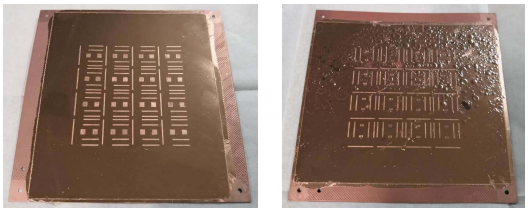
A. PID Exposure and Development Technique

At present, commercially available SiC power devices are designed for front-side Al wire bonding. Hence, metallization layers of front-side pads on these devices are Al, which is



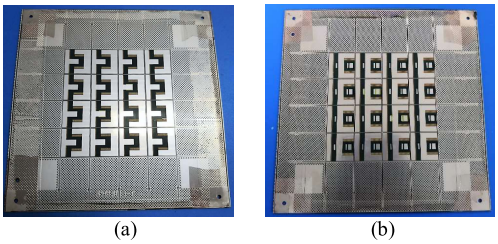
(a) (b)

Fig. 15. Terminal pads of SiC MOSFET after exposure, development, and cure. (a) Source and gate. (b) Drain.



(a) (b)

Fig. 16. Cu layers on the PID. (a) Successful sputtering. (b) Failed sputtering.



(a) (b)

Fig. 17. Double-sided RDLs of the panel-level PCB-embedded package. (a) Front side. (b) Backside.

not compatible with PCB-embedded package and an additional metallization layer is required on the front-side source and gate pads [17], [32]. Dies that had extra metallization layers are then embedded in the PCB, followed by blind vias that are usually formed by laser drilling and Cu plating, thus realizing the interconnection between dies and outer layers [14], [18], [19], [22]. However, if energy is not properly controlled, the terminal metallization pads could be damaged by laser drilling. For very thin pad of power device, laser drilling is not allowed. Therefore, new alternative laser drilling needs to be developed.

In this work, SiC MOSFET bare dies were picked and placed in the grooves of BT laminate with almost the same thickness and were laminated by double-side PID films through a vacuum laminator. Because of flow ability of PID in this process, gaps between SiC MOSFETs and BT laminate and through vias of the BT laminate were filled with PID. Chip pads and inner interconnection layers covered by PID films were then opened through exposure and development process. Fig. 15(a) and (b) shows the terminal pads of SiC MOSFET after exposure, development, and cure. It is noted that the PID film is a transparent material. It is difficult to distinguish whether the die pads and inner RDLs are exposed after development, which easily leads to final package failure. If exposure and development conditions are not well controlled or dies are tipped or thicker BT laminate is chosen, die pads and interconnection layers cannot be opened. Therefore, laminate should not be thicker than die, and die placement should be well controlled as well as the process condition.

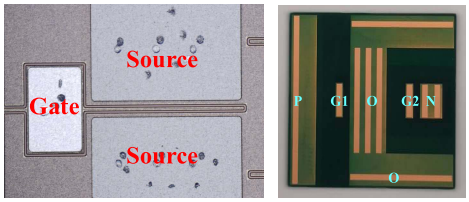
B. Panel-Level PVD Technique

In the PCB-embedded SiC MOSFET packaging, if Al pads are not modified, they will be damaged in the follow-up Cu plating process because of high reactivity of Al in the PCB-embedded package. Therefore, re-metallization of Al pad on the power devices is a key process for the development of PCB-embedded SiC MOSFET package. In [22], 5-μm-thick Cu was added to the MOSFET pads at wafer level. For SiC power MOSFET, however, the cost and risk of pad re-metallization at wafer level are high. Kearney *et al.* [19] developed a 1.2-kV PCB-embedded IGBT inverter module. For IGBT and diode front-side re-metallization, the original Al metallization of emitter, gate, and anode contact was modified by sputtering of Cr/Cu (5 nm/8 μm) layers, whereas dielectric region on the top surface of the IGBT was protected with a shadow mask. However, the size of SiC MOSFET is relatively small compared to IGBT, and it is difficult to realize the re-metallization of pads at such a small bare die. Besides, SiC MOSFET is a vertical power device; with the gate and source on front-side and drain on backside, chip-level PVD easily contaminates the other side when sputtering one side. Therefore, exploration of new re-metallization technique for SiC MOSFET in the PCB-embedded package is essential.

In this work, after PID exposure, development, and cure, panel-level double-sided PVD process was carried out. In order to improve the adhesive force between the PID film and the additional metal, a very thin layer of Ti (50 nm) was deposited on the surface as seed layer, followed by the deposition of a layer of thick Cu (500 nm), thus the original Al metallization of front-side gate and source contacts and Ag metallization of backside drain contact were modified. Fig. 16(a) illustrates the successful sputtering on the PID. Compared with wafer- and chip-level PVD, any kind of chip pad metallization can be performed at panel-level. It is noted that, if sputtering condition is not well controlled and panel sample is not dry, some bubbles could be generated. Fig. 16(b) illustrates the Cu bubbles arising due to high-power sputtering and relatively high vacuum environment. Therefore, a fully dry sample should be prepared and panel-level PVD process should be performed under the low-power and ultralow vacuum environment.

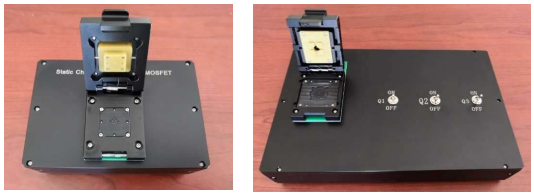
C. Double-Sided RDL Interconnection Technique

After PVD process, front-side and backside RDL layers of the PCB-embedded package were built by exposing, developing, plating, etc. Cu and Ti on the nonconductive areas were removed by flash etch and hydrofluoric acid solution, respectively. Fig. 17(a) and (b) shows the front-side and backside RDLs of the panel-level PCB-embedded package, respectively. The double-sided RDLs replaced wire-bonds and interconnection structure related to DBC substrate, the physical length of the commutation loop was shortened, and thus parasitic inductances of the PCB-embedded package were largely reduced.



(a) (b)

Fig. 18. Experimental samples. (a) SiC MOSFET bare die. (b) PCB-embedded phase-leg SiC MOSFET power module.



(a) (b)

Fig. 19. Custom fixtures for static characterization of (a) SiC MOSFET bare die and (b) PCB-embedded package.

VI. Static Characterization

A. Experimental Sample

Fig. 18(a) and (b) shows the experimental sample of SiC MOSFET bare die and PCB-embedded phase-leg power module, respectively. The SiC MOSFET bare die embedded in the PCB is the SiC DMOSFET from CREE (CPM2-1200-0080B). The backside drain metallization is Ni (0.8 μm) and Ag (0.6 μm) and front-side source and gate metallization are Al with 4 μm thickness [26]. The leads of the PCB embedded package correspond to the terminals of phase-leg power module in Fig. 3.

B. Experimental Setup

In this article, static characteristics of SiC MOSFET bare die and PCB-embedded package were measured using Power Device Analyzer (Keysight B1505A). For bare dies and custom packages, additional custom fixtures are needed. In order to accurately analyze and investigate the effect of PCB-embedded package on the $I-V$, $C-V$, and gate charge characteristics of SiC MOSFET, two custom fixtures were developed, respectively, as shown in Fig. 19(a) and (b). Electrical interconnection of device under test (DUT) was realized via probes on the fixtures. In order to avoid damage of devices or probes due to excessive current, the current limiting in the experiments was set to 20 A.

C. I–V Characterization

Fig. 20 shows the test circuit for $I-V$ characteristics of SiC MOSFET and PCB-embedded package. The gate and drain of SiC MOSFET were connected to its source through two voltage sources. The drain–source voltage V_{DS} was swept from 0 to 4 V under the gate–source voltage V_{GS} from 10 to 20 V at the step of 2 V.

Fig. 21 shows the effect of PCB-embedded package on output characteristics of SiC MOSFET. It can be observed

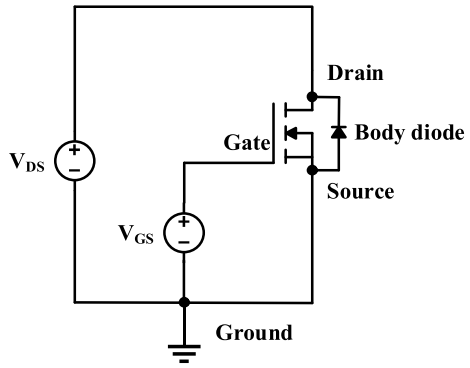


Fig. 20. Test circuit for $I-V$ characteristics of SiC MOSFET and PCB-embedded package.

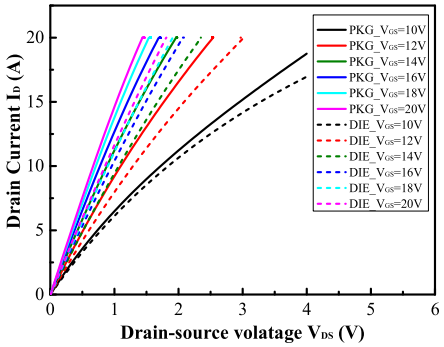


Fig. 21. Effect of PCB-embedded package on output characteristics.

from the figure, there was no evident boundary between linear and saturation regions of SiC MOSFET. As drain–source voltage V_{DS} increased, drain current I_D did not have the trend of saturation. Output current (I_D) of PCB-embedded package was decreased under a certain gate–source voltage V_{GS} compared to SiC MOSFET bare die. To realize the same output current, higher gate–source voltage V_{GS} is needed due to existence of parasitic resistance.

D. C-V Characterization

Dynamic characteristics of SiC MOSFET are dominated by charging and discharging of parasitic capacitances, which include gate–source capacitance C_{GS}, drain–source capacitance C_{DS}, and gate–drain capacitance (miller capacitance) C_{GD} [9], [10], [23].

Nonlinear miller capacitance C_{GD} is the most important and complicated parasitic capacitance, it provides a feedback loop between output and input of MOSFET. As shown in Fig. 1, the miller capacitance C_{GD} is composed of a constant gate oxide capacitance C_{OX} and a nonlinear SiC depletion layer capacitance C_{GDJ}.

Fig. 22 shows the test circuit for $C-V$ characteristics of SiC MOSFET and PCB-embedded package. The gate of SiC MOSFET was short-connected to its source. The drain was connected to its source through one voltage source. The drain–source voltage V_{DS} was swept from 0 to 200 V at a frequency of 100 kHz.

Fig. 23 shows the effects of PCB-embedded package on input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitances

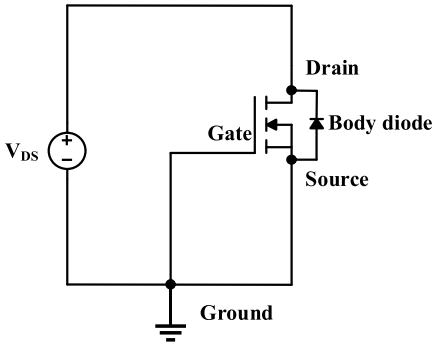


Fig. 22. Test circuit for C–V characteristics of SiC MOSFET and PCB-embedded package.

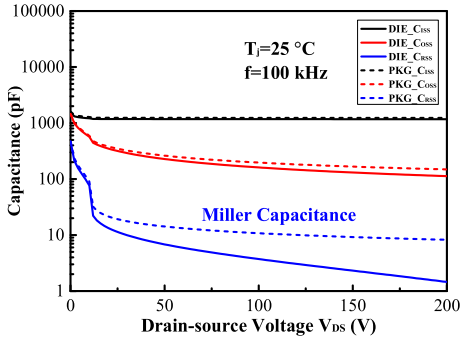


Fig. 23. Effect of PCB-embedded package on input–output, and reverse capacitances of SiC MOSFET.

of SiC MOSFET. The parasitic inductances of SiC MOSFET are related to the terminal capacitances as

$$C_{GD} = C_{RSS} \tag{2}$$

$$C_{GS} = C_{ISS} - C_{GD} \tag{3}$$

$$C_{DS} = C_{OSS} - C_{GD}. \tag{4}$$

It can be seen from the figure, the PCB-embedded package had a great impact on reverse capacitance (miller capacitance) of SiC MOSFET, had a certain effect on output capacitance, and influence of PCB-embedded package on input capacitance was little. Miller capacitance of SiC MOSFET was increased thanks to parasitic capacitance brought from package. As drain–source voltage V_{GS} increased, the difference of miller capacitance between the package and the bare die increased. According to (3) and (4), gate–source capacitance C_{GS} and drain–source capacitance C_{DS} were decreased.

E. Gate Charge Characterization

SiC MOSFET has much lower output capacitances and gate charge, and they can switch at much higher dv/dt and di/dt. High switching speed enables low switching loss and high switching frequency, which can improve the power density and efficiency of power module.

Gate charge (Qg) is the total amount of charge to turn on/off a power device. It is one of the key parameters of MOSFETs and IGBTs [33], and especially important for high-frequency

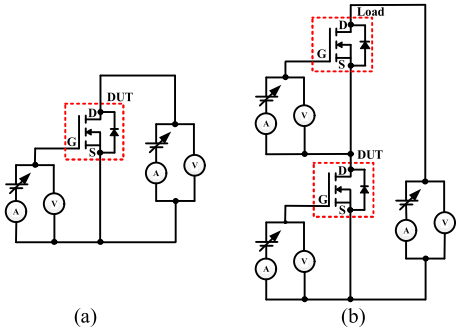


Fig. 24. Test circuit for gate charge characterization of SiC MOSFET and PCB-embedded package. (a) High-voltage measurement circuit. (b) High-current measurement circuit.

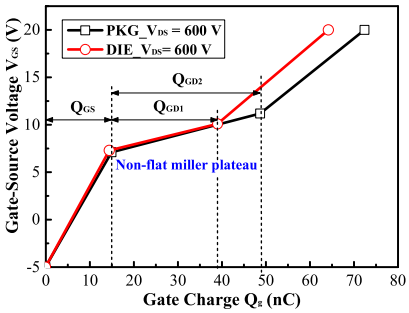


Fig. 25. Effect of PCB-embedded package on gate charge.

wide bandgap devices, e.g., SiC MOSFET and GaN HEMT. Qg can be used to assess the switching performance, e.g., gate driving loss, switching time, and miller capacitance.

To measure Qg, a test circuit with a constant current source, or a resistive load, or an inductive load is often shown in a datasheet. Conventional measurement methods require power suppliers that can simultaneously deliver high voltage and high current. The test cost and operational risk are relatively high. Furthermore, when high voltage and high current are applied to the DUT simultaneously, the power dissipation is enormous [33]. In this work, high-voltage/low-current and high-current/low-voltage measurements were performed, respectively. The test circuits are shown in Fig. 24(a) and (b). Different from the former, the high-current measurement circuit is a phase-leg structure. High side is a constant current load. A TO247 Si IGBT with the same power rating was used in this experiment.

The high-voltage measurement was performed at the OFF-state, whereas the high-current measurement was conducted from initial OFF-state to fully ON-state. The two Qg curves were merged to form a total Qg curve.

As shown in Figs. 25 and 26, gate charge curve consists of three segments with different slopes. In the first segment, C_{ISS} was charged by gate current I_G from OFF-state, because C_{GS} is much larger than C_{GD}, the gate charge in the segment is named as Q_{GS}. Gate–source voltage V_{GS} in the segment was increased until drain current of SiC MOSFET reached a load current of 20 A. Different from IGBT, drain current I_D of SiC MOSFET in the saturation region increases with drain–source voltage V_{DS} due to its short-channel effect and modest transconductance [34], [35].

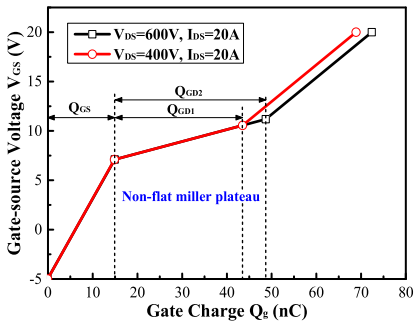


Fig. 26. Effect of drain–source voltage on gate charge.

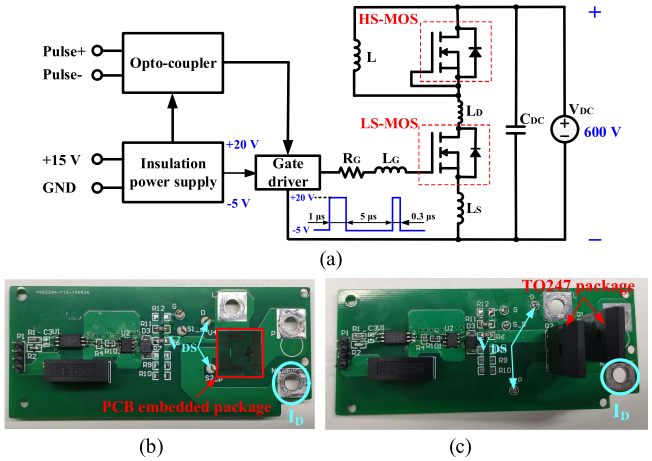


Fig. 27. Switching characteristics test for SiC MOSFET. (a) DPT equivalent circuit. DPT boards of (b) PCB-embedded package, and (c) TO-247 package.

In the second segment, where SiC MOSFET was changing from ON-state to fully ON-state. Because gate current I_G flows into the C_{RSS} and drain current does not saturate, gate–source voltage increases slowly, the gate charge in the segment is called as Q_{GD}. In the last segment, the SiC MOSFET was fully turned on.

As shown in Fig. 25, under the same drain–source voltage V_{DS} of 600 V, drain current I_D of DUT increased quickly with gate–source voltage V_{GS}. Once the drain current I_D reached the load current, it would stop increasing and keep the value. Drain–source voltage V_{DS} began to decrease. With the decline of drain–source voltage V_{DS}, gate–source voltage V_{GS} slowly increased due to unsaturation of drain current I_D. Therefore, miller plateau of SiC MOSFET was nonflat. From the figure, it can be found that Q_{GS} was almost the same before and after packaging, nonflat miller plateau of PCB-embedded package extended compared to SiC MOSFET bare die. Q_{GD} increased by 10 nC.

For the PCB-embedded SiC MOSFETs package, effect of drain–source voltage V_{DS} on Qg was also investigated, as shown in Fig. 26. It is found that as drain–source voltage V_{DS} increased, the nonflat miller plateau extended.

VII. Switching Characterization

Double pulse test (DPT) is widely used for evaluating the switching characteristics of power devices, e.g., MOSFET and

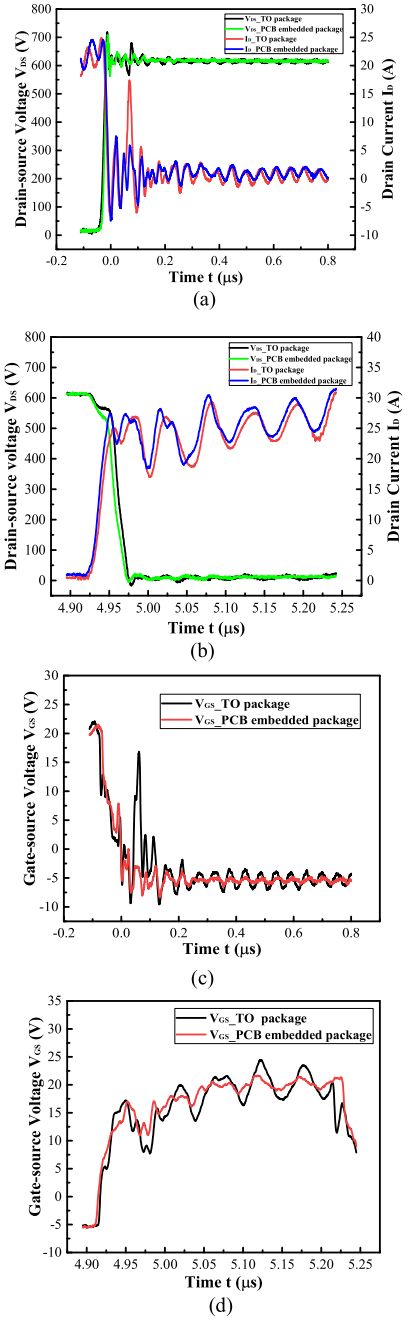


Fig. 28. Comparison of switching characteristics and driver waveforms between the PCB-embedded package and the TO-247 package. (a) Turn-off. (b) Turn-on. (c) Driver signal transition from high-to-low voltage. (d) Driver signal transition from low-to-high voltage.

IGBT. It is an inductive load double-pulse test setup and primarily consists of a dc power supply, a load inductor, a dc capacitor, and a gate driver.

In this work, DPT was used to evaluate and compare the switching characteristics of SiC MOSFET in the PCB-embedded phase-leg power module and the conventional TO-247 discrete package. The equivalent circuit schematic of DPT is shown in Fig. 27(a). The dc bus voltage was 600 V. The gate of the HS-MOS was connected to its source and its body-diode was used for the reverse recovery. The LS-MOS was controlled by a double-pulse gate signal,

as shown in the figure. The time of the first and second pulse was 1 μs and 0.3 μs, respectively. The duration between the two pulses was 5 μs. Fig. 27(b) and (c) displays DPT board of the PCB-embedded phase-leg power module and the TO-247 package, respectively. Because the PCB-embedded package is a surface mount device, it is difficult to test real switching waveforms of the package. In this experiment, switching waveforms of test points on the DPT boards of the PCB-embedded package and the TO-247 package were measured and compared. Test points on the DPT boards were designed as close as possible to the leads of the PCB-embedded package and TO-247 package, as shown in Fig. 27(b) and (c), respectively. In order to ensure the equality of comparison, the distance and width of the power loop and driver loop of the two packages were nearly the same, respectively.

Fig. 28 compares the switching characteristics and the driver signal waveforms between the PCB-embedded package and the TO-247 discrete package. As can be seen from Fig. 28(a) and (b), the PCB-embedded package had smaller voltage overshoot and current oscillation at turn-off and smaller voltage oscillation and current overshoot at turn-on than TO-247 package. The results indicated that the PCB-embedded package had smaller parasitic inductances and capacitances than TO-247 package, making SiC MOSFET more suitable for high voltage and high frequency applications.

As can be seen from Fig. 28(c) and (d), the driver signals of the PCB-embedded power module had significantly smaller oscillation than TO discrete package. Because the power and driver loops were connected through source terminal of LS-MOS, larger parasitic inductances of the power loop connected to the TO-247 package would affect the driver loop, leading to larger oscillation of the driver signal. When the oscillation amplitude exceeds threshold voltage of SiC MOSFET, it could falsely turn on the device, thereby affecting the normal operation of the circuit. The PCB-embedded package module proposed in this article had smaller parasitic inductances, which could reduce the oscillation of the driver signal and avoid false turn-on in high frequency applications.

VIII. Conclusion

In this article, a novel fan-out panel-level PCB-embedded package for phase-leg SiC MOSFET power module was developed. Electro-thermo-mechanical co-design of the PCB-embedded SiC MOSFETs package was conducted. Three key PCB-embedded packaging process, including PID exposure and development, panel-level PVD, and double-sided RDL interconnection techniques, were proposed to replace conventional laser drilling, chip/wafer-level PVD, and wire bonding techniques. To accurately characterize the PCB-embedded package and analyze the effect of PCB-embedded package on SiC MOSFET bare die, two custom fixtures were developed. $I-V$, $C-V$, and gate charge characteristics of SiC MOSFET and PCB-embedded package were analyzed and compared. DPT was used to evaluate and compare the switching characteristics of SiC MOSFET in the PCB-embedded phase-leg power module and TO-247 discrete package. Some conclusions are drawn as follows.

1) The maximum parasitic inductance of the PCB-embedded SiC MOSFETs is about 1.24 nH at 100 kHz. Compared with conventional wire-bonded package, the parasitic inductances of the PCB-embedded package decrease by 87.6% at least.
2) Compared with blind via structure, thermal resistance of the proposed structure reduces by about 26% at most, and von Mises stress of the SiC MOSFET decreases by about 45.2%.
3) When performing PID exposure and development process, laminate should not be thicker than die, die placement should be well controlled and also the process condition. Panel-level PVD process should be performed under the low-power sputtering and ultralow vacuum environment.
4) Output current of PCB-embedded package is decreased under a certain gate–source voltage compared to SiC die. To realize the same output current, higher gate–source voltage is needed due to existence of parasitic resistance.
5) The PCB-embedded package has a great impact on miller capacitance of SiC MOSFET, which is increased thanks to parasitic capacitance brought from package. As drain–source voltage increases, the difference of miller capacitance between the package and the bare die increased.
6) Only nonflat miller plateau of SiC MOSFET before and after packaging is different. Compared with SiC MOSFET bare die, the nonflat miller plateau of PCB-embedded package extends, and Q_{GD} increases by 10 nC. As drain–source voltage increases, the nonflat miller plateau extends.
7) The PCB-embedded package module has smaller parasitic inductances, which can reduce the oscillation of the driver signal and avoid false turn-on in high frequency applications.

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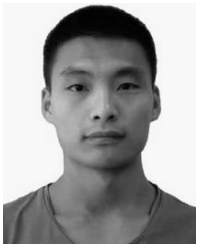

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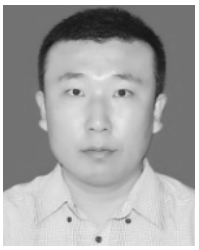

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