A new experimental approach to investigate the physics-of-failure of wirebond interconnects

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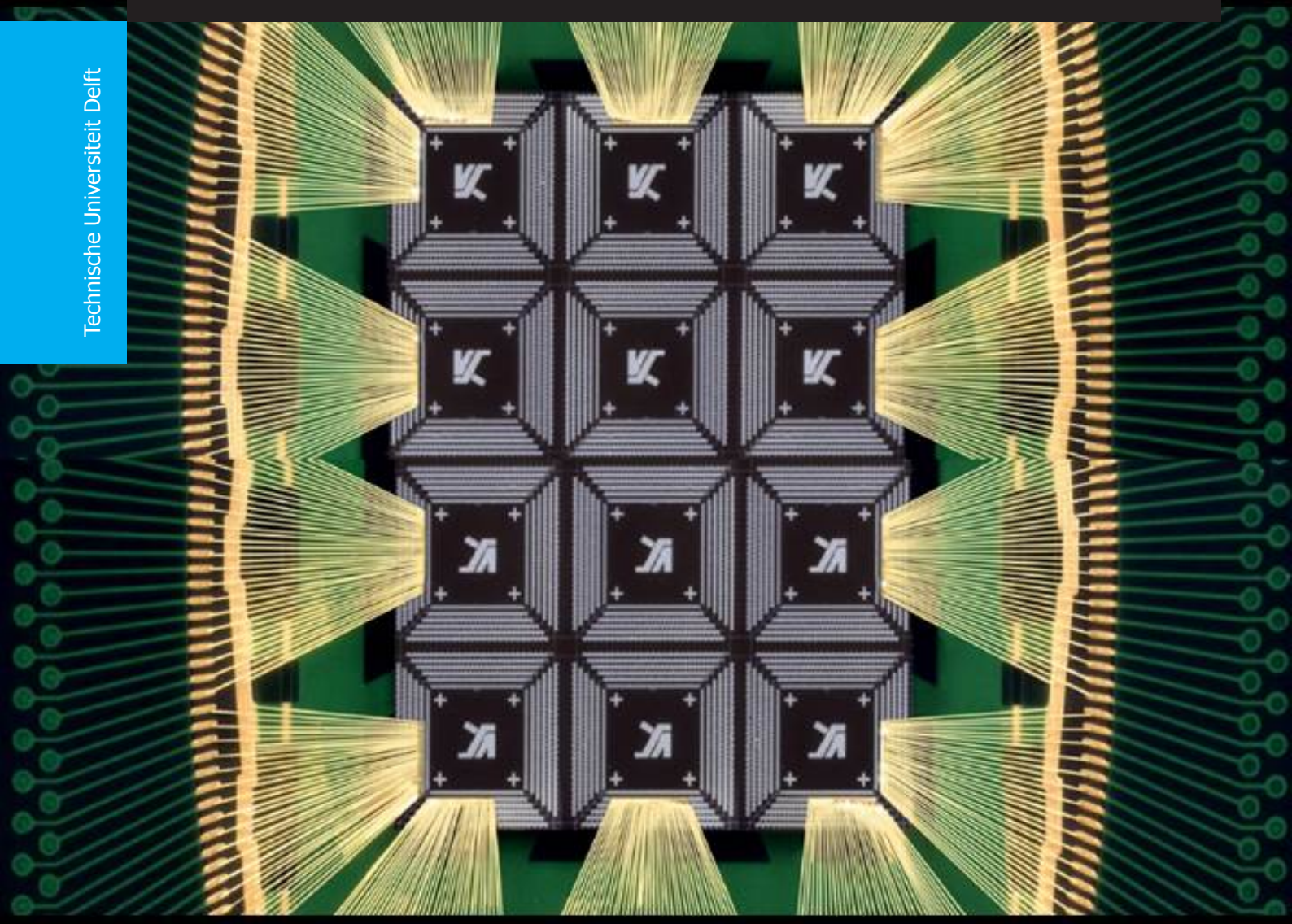

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Challenge the future

A new experimental approach to investigate the physics-of-failure of wirebond interconnects

by

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Abstract

Wirebonding is an interconnection technology used to connect a chip to its LED package. It is currently not well understood which wirebond characteristics are best to tailor to prevent the failure of wirebonds. The focus of this thesis is to understand the physics-of-failure of wirebonds via an experimental approach. Therefore, an experimental setup is designed which can accurately measure the resistance of the wirebond samples by four-wire resistance measurements. Furthermore, Finite Element simulations are done to understand the physical nature of wirebond failure better.

Gold wirebonds with different loop geometries have been designed and made which are then subjected to temperature cycling. It is found through 4-wire experimental resistance setup that when a significant increase in resistance is reported, wirebond fatigue is imminent. Coffin-Manson based Finite Element simulations show that stresses at the neck are higher than at the heel. In retrospect, when the wirebond samples are encapsulated in Silicone, there is an increase in the stresses at the heel.

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List of Symbols

ϵ	Hook position
φ	Angle from the normal to the bonding surfaces and in the plane which includes the two bonds, that the probe is pulled in the pull test
Θ	Contact angles
ρ	Resistivity
α	Resistance Temperature Coefficient
R	Resistance
T	Temperature
ϵ_p	Effective plastic strain
σ	Stress
ϵ_f	Fracture stress of the material
ϵ_c	Creep rate
σ_e	Effective stress
σ_n	Material constant

Abbreviations

L0	Level 0
L1	Level 1
L2	Level 2
L3	Level 3
L4	Level 4
L5	Level 5
PCB	Printed Circuit Board
I/O	Input/Output
TAB	Tape-Automated Bonding
IC	Integrated Circuit
LED	Light Emitting Diode
IGBT	Insulated-Gate Bipolar Transistor
RF LDMOS	Radio Frequency Laterally Diffused MOSFET
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
CD	Critical Dimension
IMC	Intermetallic Compound
EFO	Electric-Flame Off
HAZ	Heat Affected Zone
SOSB	Stand-Off Stitch Ball
PCC	Palladium Coated Copper
FAB	Free Air Ball
MIL-STD	Military Standard
FE	Finite Element
LCF	Low Cycle Fatigue
CTE	Coefficient of Thermal Expansion
COB	Chip-On-Board
APC	Advanced Packaging Center
DIL	Dual-In-Line
BSOB	Bump Stitch On Bump
US energy	Ultrasonic energy
DMM	Digital Multimeter
SP	Set Point
GPIB	General Purpose Interface Bus
JST	Japan Solderless Terminal
DAQ	Data Acquisition
RTD	Resistance Thermometer
EKL	Else Kooi Laboratory
Cpk	Process Capability Index

CHEMICAL ELEMENTS

Al	Aluminium
Au	Gold
Cu	Copper
Si	Silicon
Ag	Silver
N_2	Nitrogen
H_2	Hydrogen
Pd	Palladium
PdCu	Palladium coated Copper

1

INTRODUCTION

Section 1.1 gives a brief history of wire bonding and its importance in interconnect technology. Section 1.2 explains the motivation behind this thesis along with the main objective of this project and section 1.3 lists the intended outcomes of the thesis. Section 1.4 outlines the structure of each chapter included, giving a basic overview of what can be expected.

1.1. History

Wire bonding is an interconnect technology that integrates several fields of study like mechanics, materials, electronics, and chemistry. Wire bonding is also the lowest cost technology and has kept up with the pace of Moore's law w.r.t scaling [24] [25]. Interconnect hierarchy has about six levels, starting from the gate level at level 0 (L0), chip to package connections at L1, component-to-component connections on a PCB at L2, PCB-PCB connections at L3, sub-assembly connections at L4, and finally, physically separate system connections at L5 [2]. Wire bonding is an interconnect technology used on a level where chips are connected to package-level IO's (L1).

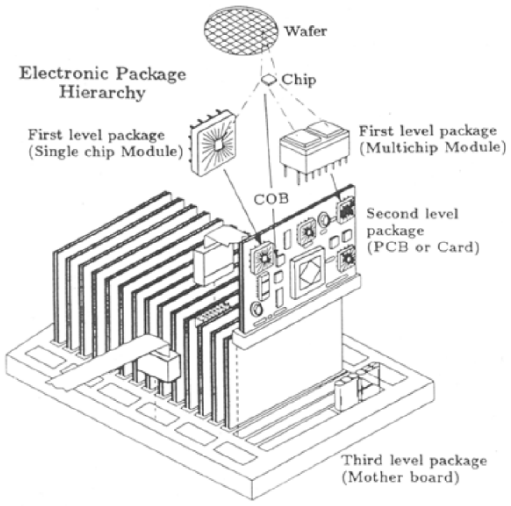

Figure 1.1: Interconnect hierarchy

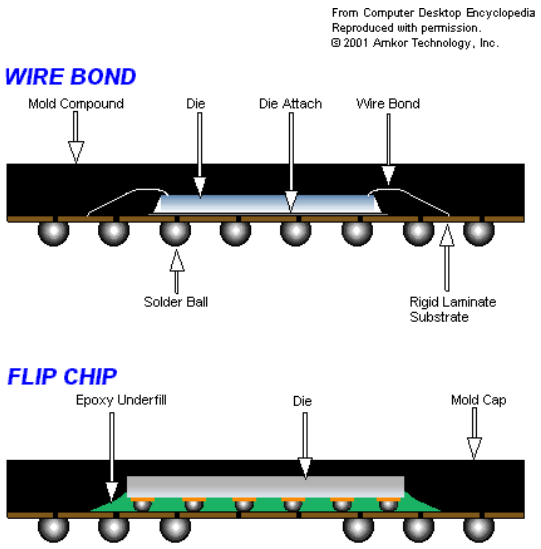

Figure 1.2: Wire bond and flip chip interconnect technology

Thermocompression wire bonding was the first of the three processes found until other processes were required for thermally sensitive devices [26]. This type of interconnect technology is suitable for low number of I/O's. As the number of I/O's increases, the number of bonds becomes proportional to the die area, causing a power distribution problem. Other interconnect technologies include flip chip

bonding and tape automated bonding (TAB) [25]. Flip chip bonding involves the deposition of solder bumps on die pads, using up all of the die area. Furthermore, it is claimed to be an advantage for high number of I/O's since the connection length has reduced and there is a significant decrease in the signal inductance [27]; which can be major contributing factors as a choice of interconnect technology for high-frequency applications. The difference between wire bonding and flipchip bonding can be seen in Figure 1.2.

Tape-Automated Bonding (TAB) involves placing mounting bumped chips on metallized polymer tapes or films [28] as seen in Figure 1.3. This method of interconnect technology allows dynamic testing and burn-in tests before assembly. In retrospect, though flip chip bonding and TAB provide advantages, wire bonding is still a popular choice of interconnect technique for small number of I/O's (<200 I/O's) because of the flexibility it offers, no chip modifications that need to be included and a well researched and established infrastructure leading to low cost, good yield and reliability.

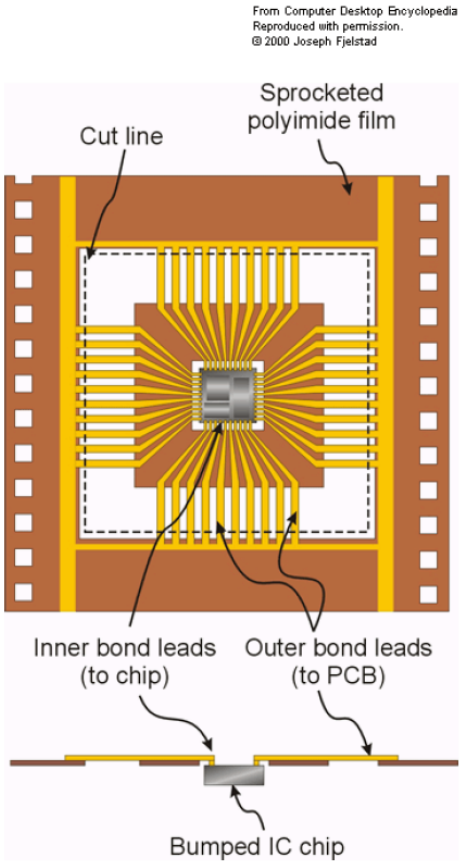

Figure 1.3: Tape-Automated Bonding

1.2. Objective

The main objective of this thesis is to study the physics-of-failure of wirebonds as an interconnect technology and to design an experimental setup to accurately measure the resistance of wirebonds. There are several variable parameters w.r.t wirebond loop geometry that controls the yield and reliability of wirebonds. It is currently not well understood which wirebond characteristics are best to tailor to reduce the failure rate or fatigue of these interconnects. By a combination of Finite Element calculations and experiments this thesis aims to increase the understanding of the problem.

1.3. Outcomes of the thesis

The outcomes of this thesis are highlighted as:

- Experimental method to be able to detect crack growth in metal interconnects, more specifically wirebonds.
- Understanding the physics-of-failure of wirebond fatigue.
- Design recommendations for wirebond fatigue reduction.

1.4. Layout

This report will explore into various parameters contributing to wirebond fatigue. This chapter gives a brief introduction about wire bonding, the main objective, outcomes and the layout of the entire report. It talks about the various factors that contribute to wirebond fatigue via a fishbone diagram that will be explored in detail in chapter 2.

Chapter 2 begins by describing the different ways of making wirebonds along with the bonding processes that are involved in this technique. Following this the fishbond diagram for wirebond fatigue is introduced. It allows to inspect the characterization of wirebonds, materials, and lifetime evaluation via FE simulations reported in the literature of wire bonding. This section ends with a detailed description about testing the quality of wirebonds. This literature survey will be referred to accordingly throughout the report.

Chapter 3 explains the experiment conducted by describing the materials and components used, how the setup is connected, and how data can be logged. It also gives a description of how the samples are made and illustrates it with necessary images. The geometric and technical specifications of these samples are not conventional but have been designed to suit this project. This chapter also includes quality and reliability testing: thermal cycling and pull test, both of which are explained in detail.

Chapter 4 describes how the wirebond samples are modelled using COMSOL Multiphysics™ v. 5.2. The physics and studies that have been implemented in the finite element simulations are also discussed here.

Chapter 5 This chapter reports the results obtained from the experiments described in chapters 3 as well as from the simulations described in chapter 4. A comparison is made to cater to the reliability of wirebonds.

Chapter 6 talks about the conclusions made in this research. It also talks about the future recommendations for this research.

2

LITERATURE SURVEY

2.1. Wirebond processes

Wire bonding makes interconnections between the IC and the leadframe or the package. The material used is generally Al, Au or Cu with a wire diameter range between 15 microns and several hundred microns depending on the power required in applications. This technology broadly falls under two classes: Ball-wedge bonding and Wedge-wedge bonding. Furthermore, these two technologies have two kinds of processes namely, thermo compression and ultrasonic bonding. Thermo-compression bonding, developed in Bell Laboratories [29] [30] makes use of three process parameters: temperature, pressure and time. This process occurs at high temperatures and does not use any ultrasonic power. Ball wedge bonds with Au wires are made using this method. Ultrasonic bonding, as the name suggests makes use of ultrasonic power, pressure and time. This process occurs at room temperature because of the use of ultrasonic power. Usually wedge-wedge bonds with Al, or Al with 1% Si wires are made using this method and they find application in devices with high current.

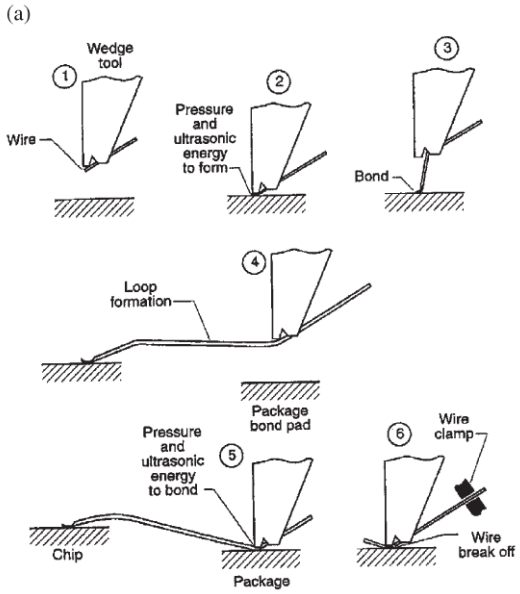

Figure 2.1: Ultrasonic wire bond with a wedge tool [1]

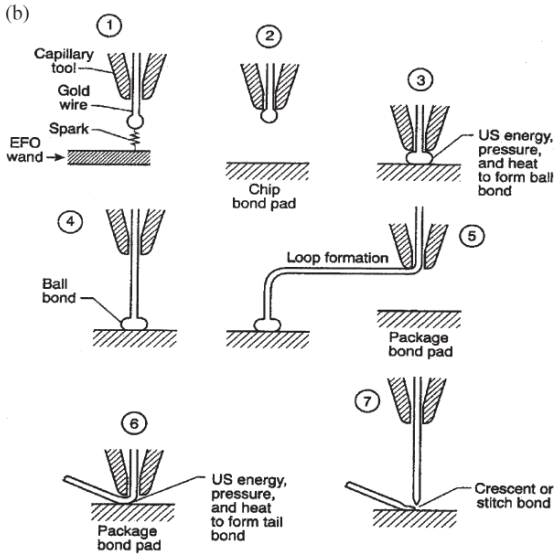

Figure 2.2: Ball stitch wire bonding procedure with a capillary tool [1]

A third kind of process, called Thermosonic bonding is a combination of the first two, i.e., it uses ultrasonic power as well as temperature along with pressure and time in order to make the bond. Here, both ball-wedge and wedge-wedge bonds are made with Au and Al wires. Figures 2.2 and 2.1 portray

simplified procedures of making a ball-stitch wire interconnection with a capillary tool and an ultrasonic wirebond using a wedge tool.

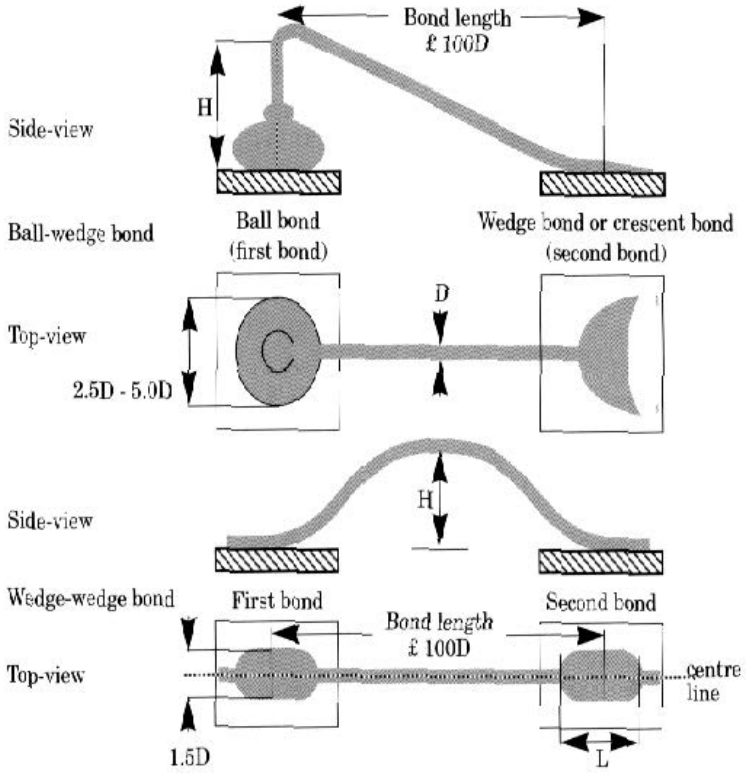

Figure 2.3: Side view and Top view for Ball-wedge and Wedge-wedge bond [2]

Wirebonds undergo fatigue, which is a serious issue in LEDs due to crack growth in them. While the reasons for crack growth can be several, the failure is mainly due to two consecutive processes: viscoplastic deformation ultimately leading to crack initiation and crack propagation that leads to final catastrophic failure [31]. Several factors are associated to wirebond fatigue like wire material and its properties, assembly process, bonding temperature, diameter of the wirebond, loop geometry, breaking load, bond to bond spacing, loop height, and bond loop movement. These factors are listed in the fish bone diagram in Figure 2.4 and will be discussed in detail in the following sections.

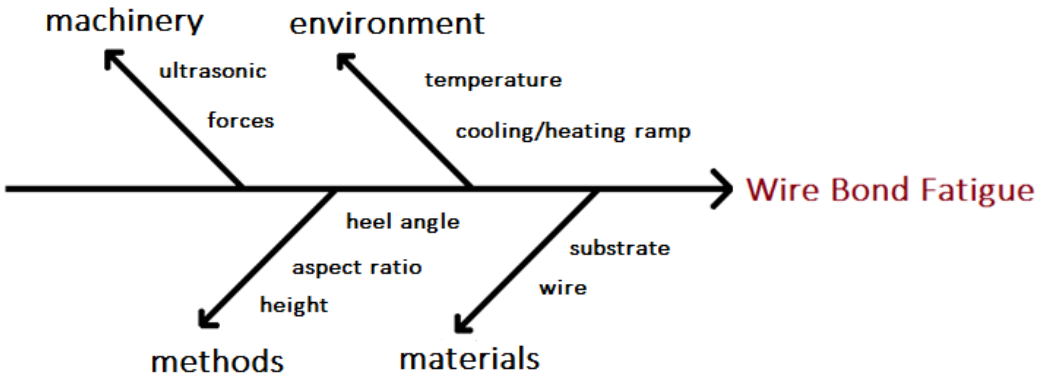

Figure 2.4: Fishbone diagram for wirebond fatigue

In an LED package, there is a silicone encapsulant surrounding gold wirebonds, and this encapsulant has a higher thermal coefficient of expansion than Au. Silicone reacts to temperature i.e. elastic modulus of silicone is higher at low temperatures than higher temperatures. And this low temperature condition causes plastic strain in the wire, leading to fatigue.

Thermal fatigue of wirebonds have been studied for various applications like for IGBT modules, power modules, RF LDMOS and silicon power semiconductors through the years. For high power IGBT modules, [32] it was noted that wirebond lift off was a major failure mechanism caused by low-cycle fatigue. The IGBT modules were approached analytically as well as using Finite Element calculations in [13]. In the paper, Al wire bonding is used with a wire diameter of 350μm and a Coffin Manson approach is used to predict the wirebond's lifetime. Al wirebonds are also used in power MOSFETs like LDMOS (Laterally Diffused MOSFET).These wires also experience fatigue as they go through temperature and power cycling where the required field conditions were between 10^4 and 10^{10} cycles to failure. LED package failure falls under low-cycle fatigue failure [33] as opposed to other electronic packages whose failure attributes to high-cycle fatigue failure. Low cycle fatigue is a concern that is often also seen in Aluminium wirebonds. The characteristics of low cycle fatigue include plastic deformation and low cycle phenomenon. Plastic or permanent deformation is observed if the load exceeds the elastic limit of the material. Nevertheless, this deformation doesn't have a linear relationship with applied stress. Wirebond failure rates have been the cause of up to 30% of electronic packaging failures [34] 49% of all failure modes in LEDs are due to cracking of the wirebonds [35].

2.2. Characterization of wirebonds

There are several factors contributing to wirebond fatigue. A wirebond's profile influences its reliability the most, as well as how the wirebond is fabricated during the wire bonding process because of the influence of the residual stress in the wirebond [36]. Some of these factors that characterize a wirebond's profile is explained in detail in the following sections.

2.2.1. Geometry and looping

The diameter of wirebonds vary between 15 - 75μm [37] based on the applications. A larger diameter of the wire helps it withstand more tensile strength, in case of applications that require large power or larger currents. Currently ball bonding upto 76μm or 3 mil. is also offered. Here, the shape of the ball bond decides how strong the bond is; usually a larger diameter translates to a stronger bond. But to cater to finer pad-pitch applications, the wire diameter size is decreasing [3]. And the thinner the diameter gets, new challenges arise. Typical wirebond dimensions are listed in Table 2.1.

Table 2.1: Typical wirebond dimensions [2]

Description	**Typical values D=25um**	**Typical values D=18um**
Wire length (min)	1 mm	760 micron
Wire length (max)	2.5 mm	2 mm
Loop height	400 mm	400 mm
Die pad size: ball (min)	100 um	80 um
Die pad size: wedge (min)	65 um	50 um
Substrate pad 1	250 x 200 um	250 x 200 um
Substrate pad 2	250 x 250 um	250 x 250 um

There are several looping issues because of an increase in the wire length and decrease in the wire diameter. The wire bends at the tip of the bonding tool, and how it bends affects the characteristics of the loop made. This can be determinded by the radius of the bend. If the bend is too large, there will be contact with the substrate causing a hump after bonding the wire. This hump is an excess and does not fit into the desired specification of the package. Another consequence of the radius being too large is that the wire may sway, leading to contact with other wirebonds in the package. The tolerance

for wire sway depends on the pad pitch, diameter and length of the wire [3].

If the radius of the bend is too small, there may be a laydown condition where there is not enough tension in the wire to hold up. These issues can be eliminated with programming suitable parameters in the bonding tool or to take up alternative looping mechanisms. Wire loops or bends have two advantages: they extend the wire functionality and they also avoid obstacles in the packages. They also maintain loop height consistency. Difference between a large and small bend radius can be seen in Figure 2.5.

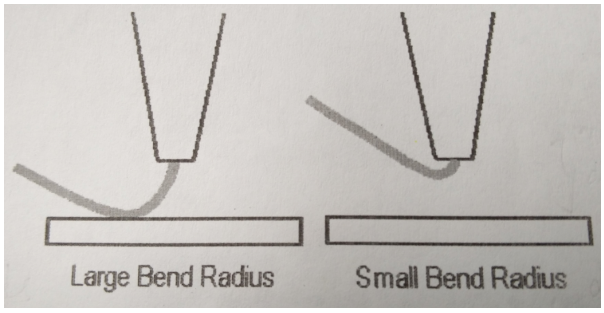

Figure 2.5: Wire radius [3]

Loop shapes can be of four types based on the number of bends. The simplest type is the kink over bonded ball observed in Figure 2.6 which is a preferred choice if speed is the priority of the bonding process. The second type is the horizontal directional bend, also known as lateral wire shaping [3]. It should be noted that as the bends are farther from the initial bond, the control over the loop reduces. The ideal results are obtained for loop shaping when it is done within the first 60% of the wire span [3]. "Each bend adds 10% to 20% to the overall wirebond cycle time of the device [3]."

The third and fourth types of loop shaping are loops with two kinks. These are used for special specifications where longer wires are needed. The use of double kinks depends on the amount and the direction of loop shaping. The uses can be seen in table 2.2.

Table 2.2: Two-bend loops applications [3]

Bend 1	Bend 2	Application
-	+	M-loop, for long-low loops.
+	-	CSP, to conform loop shape to chip.
+	+	Cavity-down, up-bonded loops.

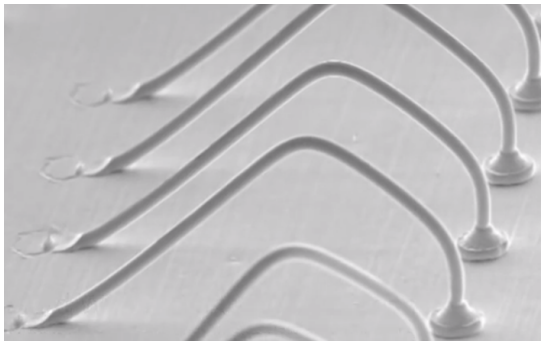

Figure 2.6: Kink over bonded ball [3]

Figure 2.7: M-loop [3]

The M loops consist of two kinks, seen in Figure 2.7, allow low loops to be made and the shape itself is known to provide [3] a natural resistance to thermal expansion and contraction that occurs to some

wire loops in certain packages. This type of loop shaping is also a solution to wire sway as it is less likely to experience it. The fourth type of looping is the one with a tail kink, which is apparently the the most complex type of shaping. The approach here is a high angle approach for the second bond, so it makes it difficult to make a kink that does not affect the rest of the wire itself.

There is no perfect wire geometry, nor is there a single optimal wire geometry to prevent fatigue. Different wire shapes work well for different applications. In retrospect, the bonding tool chosen also plays a role in the quality of the wirebond. Normally, a standard bonding tool does the job but in case of a requirement of low loops or more bends, a bonding tool with smooth edges might shape better quality wires. A bonding tool with a large hole (H) and critical dimension (CD) is preferred, and a suggestion is made to choose a tool with a hole-wire dimension of 0.4 mils [3]. Increasing the bond force and reducing the ultrasonic energy will also contribute to shaping wires of better quality. Figure 2.8 shows the critical dimensions of the bonding tool's capillary. A new capillary design [38] with a larger chamfer diamter and a smaller chamfer angle improved the bond bondability and smaller ball size control for ultra-fine pitch wire bonding. It was claimed that by using this new type of capillary design it produced a higher perccentage of IMC than the standar capillary; resulting in 0% ball lift failure after 300 hrs of aging.

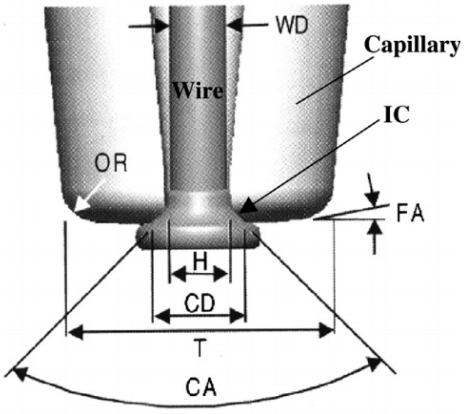

Figure 2.8: Critical dimensions of the bonding tool's capillary [4]

Due to scaling down, there has been a decrease in the bond pad pitch which directly influences the die size and the paddle size; both arising the need for long wire loops [3]. The looping methods affect the bondability of wires, especially low-loop bonds. The reason for increasing low-looped bonds or bonds with a low height is the development in the multiple level stacked die packages. The trajectory of the capillary, the electric-flame off process (EFO) and wire's properties influence the wire loop and the loop height [39].

The two types of looping methods are forward and reverse looping [6]. It was found in [6] that forward looping is suitable for heights equal to or greater than 110μm and if used for heights below 90μm, the Au wire is affected by the HAZ effect and cracks may be formed. Non standard wire looping techniques include stand-off stitch bonding or looping with non-conventional trajectories. The former is also known as reverse bonding. The forward loop is conventional and usually has a failure at the neck if forming low-height loops. In such a situation, reverse bonding plays a key role in preventing wire sway. This method is also known as Stand-Off Stitch (SSB) or Stitch-on-Ball. Here, a gold bump is made on the 1st bond bap and then a ball bond is made. After this, the gold wire is pulled up and looped to stitch with the bump made on the 1st bond pad. Since the second bond is at a lower height as seen in Figure 2.9 and 2.10 than the first bond, the HAZ effect does not effect the wirebond to form cracks.

2.2.2. Materials

Wirebonds are typically made of Aluminium (Al), Copper (Cu), Silver (Ag), or Gold (Au). Due to the rise in the cost of Au, Cu is seen as an option again because of its material properties. Cu has better mechanical, electrical and thermal properties [40]. It is known for its ball neck strength after

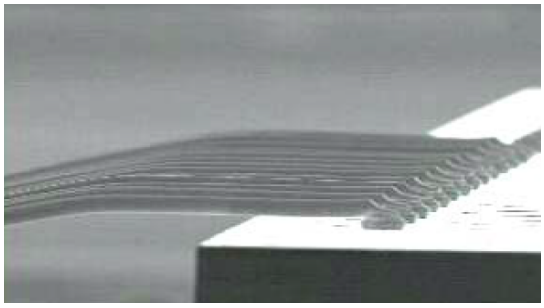

Figure 2.9: Low loops formed by reverse ball bonding [5]

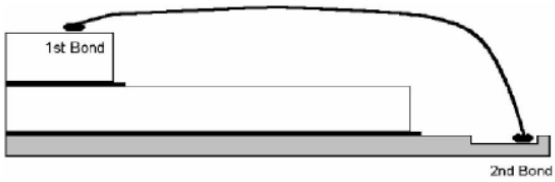

Figure 2.10: Stand-off Stitch Bonding profile [6]

the ball formation process [1], and its stiffness helps in making longer and low loops for high I/O applications[41] that also prevents wire short. But its disadvantages include oxidation, even at low temperatures. So during FAB (Free Air Ball) formation, 95% N_2 and 5% H_2 forming gas is a required condition in order to prevent Cu oxidation [8]. These properties/characteristics can lead to a contradiction because though Cu can be used to make low loops, there's a trade off because of possible surface oxidation. The possibility of cratering due to use of more ultrasonic power. Table 2.3 presents the differences in properties of Cu, Au and Ag.

Table 2.3: Pure metal properties [8]

Bonding wire	**Cu**	**Au**	**Ag**
Density (g/cm^3)	8.9	19	10.5
Atomic weight (g/mol)	64	197	108
Electrical resistivity (ohm.m)	1.68E-8	2.21E-8	1.63E-8
Anti-oxidation (V)	0.52	1.42	0.79
Thermal conductivity (W/m.K)	401	318	429
Melting point	1085°C	1064°C	961°C
Vickers hardness (Mpa)	369	216	251
Young modulus (GPd)	130	78	83

If an alloy is used to make the bond wire, homogeneity should be maintained; in order to prevent voiding problems (Kirkendall effect). It has already been stated that due to Au's high cost, Cu is the most economical substitute that has suitable electrical, mechanical, and thermal properties. But, Cu has a tendency to oxidise even at a low temperature. Another disadvantage for Cu is that it needs more power and force for ultrasonic bonding that might lead to cracking of the bond pad. Al-coated Cu wires for room-temperature wedge–wedge bonding have been shown to suppress oxidation and have better pull strength, better metallic contact formation, and better storage capabilities than bare Cu wires [21]. Several coatings applied on Cu prevents oxidation, but Pd turns out to be of low cost, and also has a higher tensile strength than Cu when bonded on Al pads.

Apart from Cu, other alternatives for wirebonds include palladium coated copper (PCC) and silver (Ag) alloys. Amongst these, Ag-alloys have properties most similar to Au, while its cost is comparatively much lower than Au, as can be seen in Figure 2.11 according to the datasheet provided by Amkor Technology.

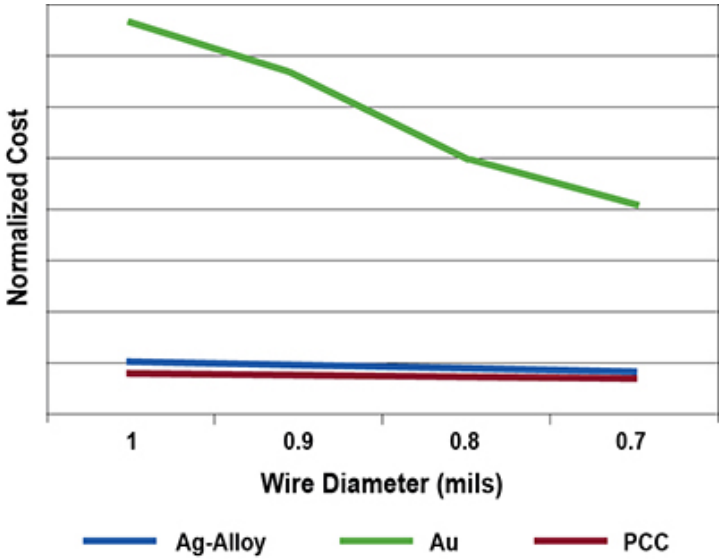

Figure 2.11: Wire cost comparison [7]

Table 2.4 gives a comparison for different wire bonding materials with respect to different factors that influence the reliability of the bond.

Table 2.4: Wire bonding material comparison [21]

	Au	**Cu**	**PdCu**
Cost	High	Low	Low (higher than Cu)
Cover gas	No need	Forming gas	Forming gas or N^2
FAB hardness	Compatible to Al	~40% harder than Au	~10% harder than Cu
First bond process	Good process window	Narrower than Au	Same or slightly narrower than Cu
Second bond process	Same	Same	Same
Portability requirement	Moderate	High	High
Reliability	Good	Good; more stringent mold compound than that for Au	Same or slightly better than Cu

Other alloys like, alloyed Al wire (Al 1%Si) are also preferred to pure Al wire except in high-current devices because of greater drawing ease to fine sizes and higher pull-strengths in finished devices. Ag is known to have reliable electrical and thermal conductivities especially better than Au, and Ag's price is also $1/20^{th}$ that of Au [42].

In the tests performed in the reliability study [42], it was noticed that Ag wire with an Al bond pad showed cracks after 300hrs of aging, whereas with a noble metal bond pad, a solid solution was formed with no cracks noticed even after 800hrs of aging. It might be interesting to look at Figure 2.12 for IMC growth comparison in the same reliability test. There is a significant increase in the IMC growth of Au when compared to Ag or Cu. For instance, at 48hr, IMC growth for Au-Al is more than that for Ag-Al and definitely more than Cu-Al. The Au-Al is seen to be more uniform as well as stable at 175°C than for Ag-Al or Cu-Al IMC growth. No Al splash or squeeze out for Au and Ag can be observed in Figure 2.12 unlike for Cu since Cu is a harder material.

Table 2.5 compares different wire materials and but has an addition of the Ag-alloy and compares various parameters of the Ag-alloy with Au and PCC. This table also presents the impact each of the

Table 2.5: Wire material comparison based on impact on application requirement

	Ag-alloy	Au	PCC	Impact
Wire cost	Lower cost	Expensive	Lowest cost	PCC and Ag-alloys are significantly cheaper than Au wire
FAB hardness	Soft	Soft	Hard	Harder materials cause cratering and bond pad crack
Process window (Force, Power, Time)	Wide	Wide	Narrow	Wider process window improves manufacturability for devices with fragile bond pad structures
Al splash	Minimal	Minimal	More	Less Al splash is better for fine pitch and small BPO
Ultra-low loop capability	Excellent	Excellent	Limited	Ultra-low loop capability allows thinner packages
Resistivity	Good	Better	Best	Low resistivity is better for current carrying applications

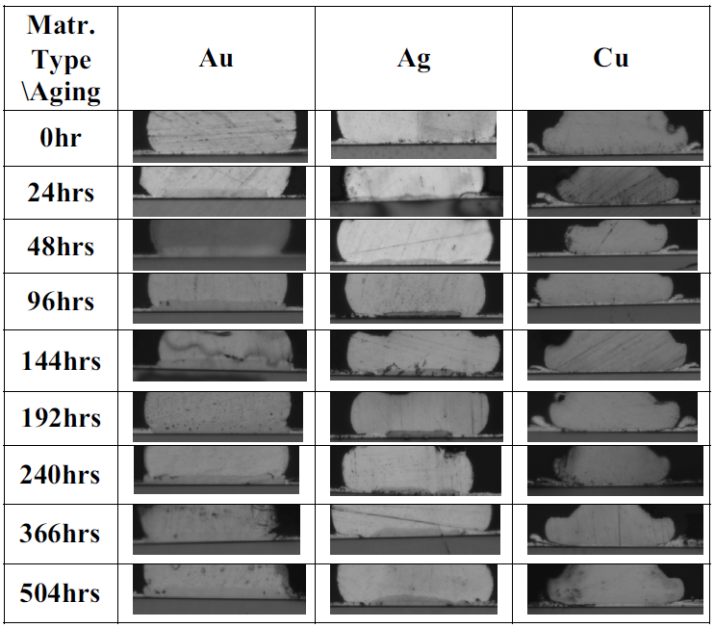

Figure 2.12: IMC growth comparison for Au, Ag annd Cu at 175°C between 0hr and 504hrs [8]

wire material choices has on specific application requirements. Au is a reliable wire material choice as it does not need cover gas and has a wide process window with the capability of making ultra-low loops. Ag-alloy is quite similar to Au but is cheaper and has a slightly higher resistivity than Au, making Au better for current carrying applications.

Different metallizations behave differently on the bond pad's material. Ball bonds made to Al or Al/Si showed an extrusion of metallization [9] as seen in Figure 2.13, whereas when mixed with Cu, as in Al/Cu or Al-Cu/Si, there was almost no extrusion noticed. The probable reasons for no extrusion could be that Cu provides hardness to the bond and tends to precipitate into the Al matrix [9] due to which extrusion is not seen. Mostly an almost unnoticable spotty intermetallic layer is formed, due to no

reaction between the ball and the pad, and thus eventually turning into bond failure on exposure to temperature [43]. It was said in [9] that proper bond schedules would have a uniform intermetallic layer for bond pads with copper as seen in Figure 2.14 as opposed to spotty or non-uniform intermetallic layers with older bonding schedules that would lead to bond failure.

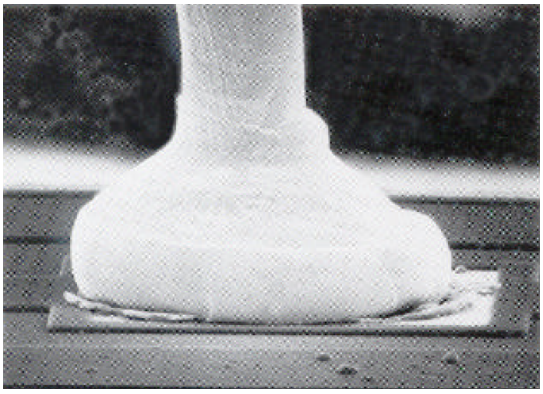

Figure 2.13: Al Extrusion noticed when wirebonded to Al or Al/Si metallization [9]

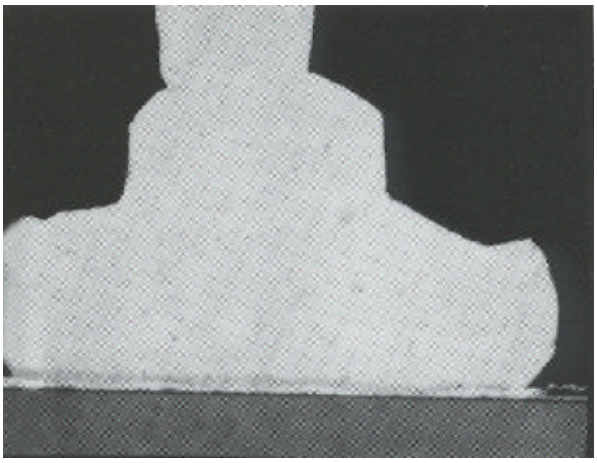

Figure 2.14: Uniform IMC formed for AL/Si/Cu metallization with revised bonding schedule [9]

2.2.3. Quality testing

The quality of wirebonds affects their reliability too. And there are several methods to test the bond quality. Popular mechanical tests are the pull test and the bond shear test. The pull test is one of the most famous ones that has been in practice for years. The military standard MIL-STD-883 Method 2011.7 is a destructive bond pull test [44] that measures bond strengths and compares with the required bond strengths. [22]. The bond pull involves an upward force when a hook is placed under the wirebond. Furthermore, it is pulled until it fails [10] and can be seen in Figure 2.15 and 2.16.

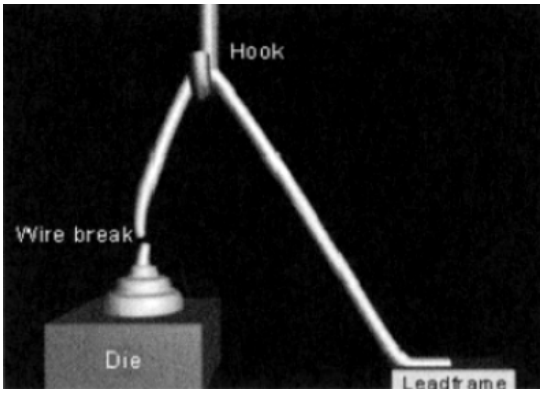

Figure 2.15: Wirebond pull test [10]

Figure 2.16: Pull test [2]

The pull forces in MIL-STD-883 can be seen in the Table 2.6. Figure 2.17 shows the geometric variables for a bond pull test.

Table 2.6: Pull forces in Al and Au [22]

Al and Au wire diameter (inches)	Pull force (gf) Al	Pull force (gf) Au
0.0007	1.2	1.6
0.0010	2.0	2.4
0.00125	2.5	3.2
0.0013	2.5	3.2
0.0015	3.0	4.0
0.0030	9.5	12.0

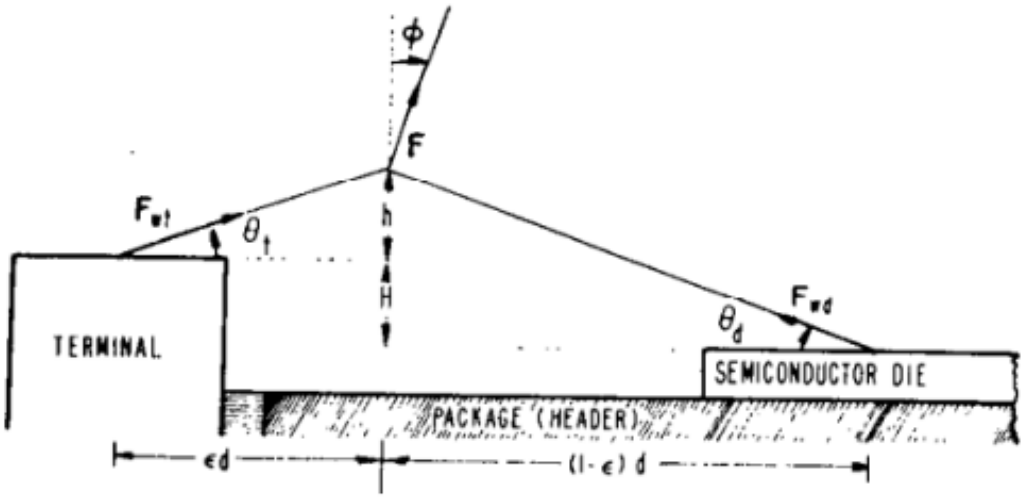

Figure 2.17: Geometric variable for a bond pull test [1]

$$F_{wt} = F[\frac{(h^2 + \epsilon^2 d^2)^{1/2}((1-\epsilon)cos\varphi + \frac{(h+H)}{d}sin\varphi)}{h + \epsilon H}] \tag{2.1}$$

$$F_{wd} = F[\frac{(1 + \frac{(1+\epsilon)^2 d^2}{H+h^2})^{1/2}(h+H)\epsilon cos\varphi - \frac{h}{d}sin\varphi}{h + \epsilon H}] \tag{2.2}$$

A more recognizable equation is when both bonds are on the same level (H=0) and the loop is pulled at the center (ϵ= 0.5) and φ=0:

$$F_{wt} = F_{wd} = \frac{F}{2}\sqrt{1 + (\frac{d}{2h})^2} = \frac{F}{2sin\varphi} \tag{2.3}$$

For a given strength, larger values of h/d will result in higher pull force value [1]. Due to the possibility of a bent hook wire, the loop height (h) will vary as a different angle (θ) is being introduced. In order to calculate the corrected loop height h1, h must be substituted in 2.1 and 2.2 and h1 is given as:

$$h1 = \sqrt{\frac{(h^2 + \frac{\epsilon d^2}{2})^2}{h^2 + \frac{d^2}{4}} - \epsilon^2 d^2} \tag{2.4}$$

For smaller stand-off ratios (h/d), the pull force increases since the hook's position is shifted from the center. Retrospect, for larger ratios, the pull force decreases. When epoxy is applied in such scenarios,

even if the hook moves away from the center, pull force applied increases but the wire would refrain from breaking. Thus, epoxy is a solution to prevent breakage, though it translates to an increase in the cost.

Since a pull test does not entirely confirm the strength or quality of a ball bond, a shear test was also developed. The bond shear test uses a shear tool to push the ball bond with a certain amount of force. It is critical that the tool is placed according to the requirement of the shear test. Else, there is a probability for the tool to drag on the substrate [10]. Figure 2.18 illustrates a comparison of ball shear mode at 175°C between 0hr and 504hrs in the reliability test performed in [8]. Figure 2.18 shows that there was no Ag remains at 0hr during the ball shearing test. But a bulk of Ag remains can be seen between 96-504hrs. It was seen that the ball shear (force) measurements from the ball shear test were higher for Ag than Au or Cu as the ageing increased between 48 to 504hrs [8]. The reason why a circular shape is seen for Au and not Ag after the shear test is because of the uniform IMC growth in Au-Al and uneven IMC growth in Ag-Al with longer ageing time.

Figure 2.19 shows a systematic movement of the shear tool and respective failure modes. These tests are for certain failure modes like ball lift, ball neck break, mid span break, heel break, weld lift, lift off, cratering, ball shear and bond pad lift.

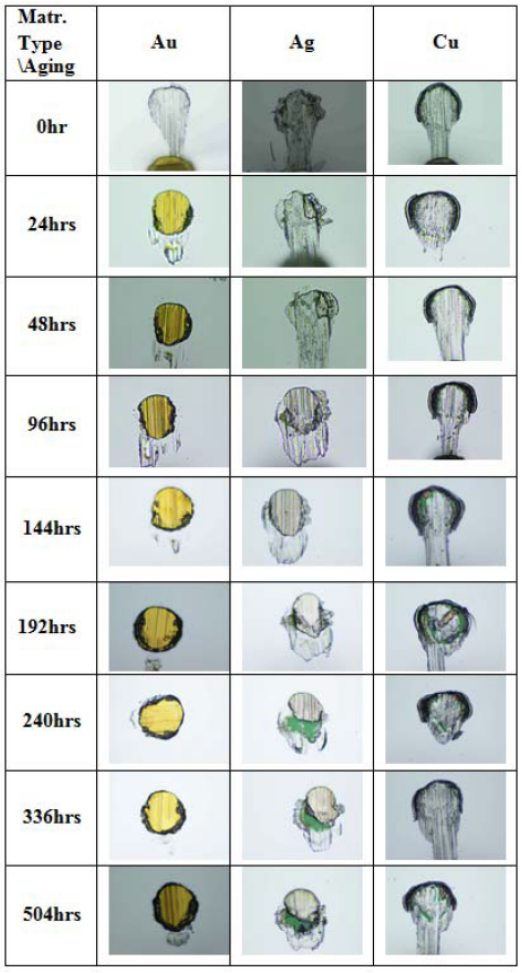

Figure 2.18: Comparison of Au, Ag and Cu wires for ball shear at 175°C between 0hr and 504hr [8]

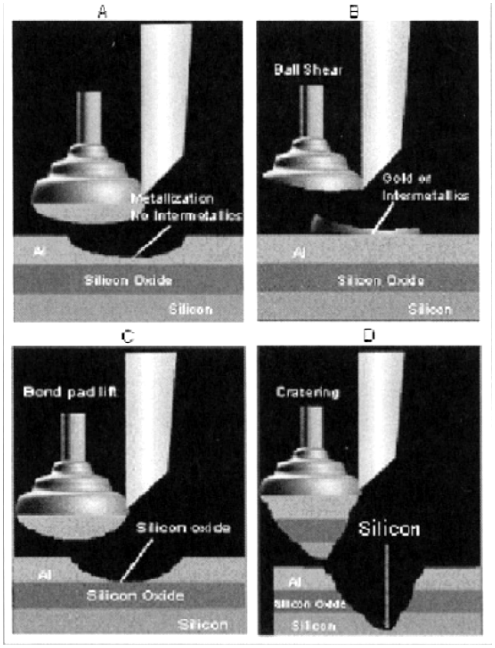

Figure 2.19: Failure modes for shear test. (A) Ball lift (B)Ball shear (C) Bond pad lift (D) Cratering [10]

2.3. Failure locations

Some failure modes are representative of their failure locations like mid-span break (when bond strength exceeds wire tensile strength), neck break at Heat Affected Zone (HAZ), heel break, lifted stitch and lifted ball. The locations where these failures occur are illustrated in Figure 2.20.

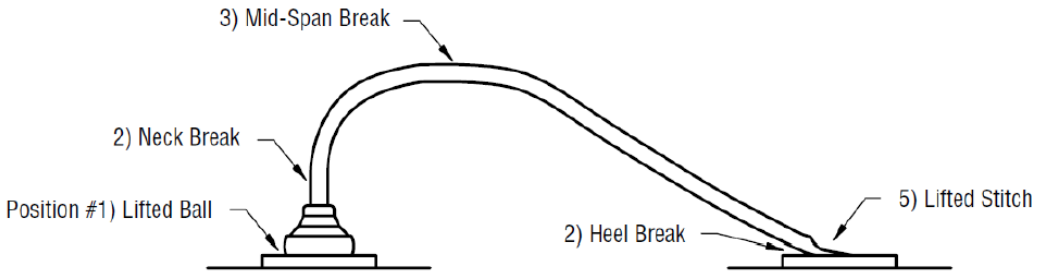

Figure 2.20: Failure modes [2]

2.3.1. Ball Lift

When the interface between the bond pad and the ball bond is weak, this failure may occur. The reasons for this varies and can be because of bond pad surface contamination or poor bonder set-up [10]. In this failure mode, no intermetallic formation is seen.

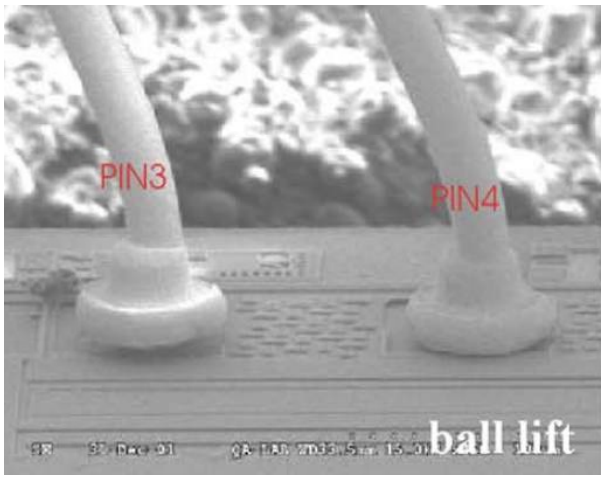

Figure 2.21: Ball lift [11]

2.3.2. Midspan Break

This failure is usually due to ductile fracture and plastic deformation and it's different from the failure at the neck or the heel as that is caused by brittle fracture [10].

2.3.3. Ball neck failure

This failure occurs above the neck of the bond at the interface between the rest of the wire and the ball bond. This is one of the preferred failure modes that occurs near the HAZ. The failure is usually due to incorrect parameter settings for the bonder or if the tools are worn-out or contaminated [10].

2.3.4. Heel Break

The heel is the location where the wire narrows into the bond, when the wire breaks off from its wedge, the failure mode is a heel break. This is often seen in wedge-wedge Al bonding. Furthermore, the

reason for this failure is due to crack propagation at the heel, which may be due to use of abundant amount of ultrasonic energy and force while bonding.

2.3.5. Weld Lift

This failure mode is similar to bond lift and is one of the undesired failure modes and indicates an improper process optimization [10] and might occur due to lead frame contamination, improper ultrasonic coupling, or hard metallization.

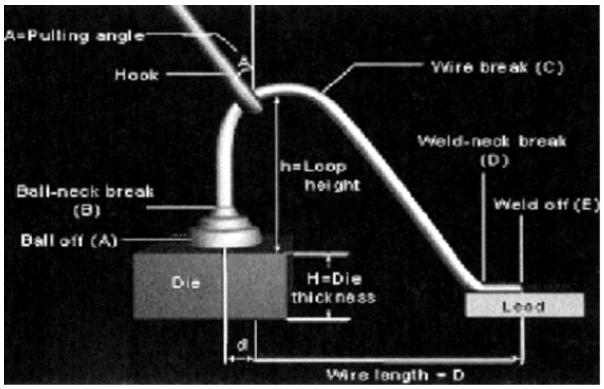

Figure 2.22: Different failure modes [10]

2.3.6. Ball Shear

When there is significant intermetallic formation on the bond pad, and the entire ball is sheared, this failure mode is observed.

2.3.7. Cratering

When a chunk of the wirebond including the ball/wedge wears off due to mechanical damage such as crack formation and impairs the underlying bond pad, this failure mode occurs.

2.3.8. Bond pad Lift

When the bond tears off and Silicon dioxide is exposed the failure mode is that of a bond pad lift.

The above failure modes can be seen in Figures 2.19 and 2.22. Other examples of wirebond failure are stitch break, wire sweep, and wire break, shown in Figures 2.23, 2.24 and 2.25.

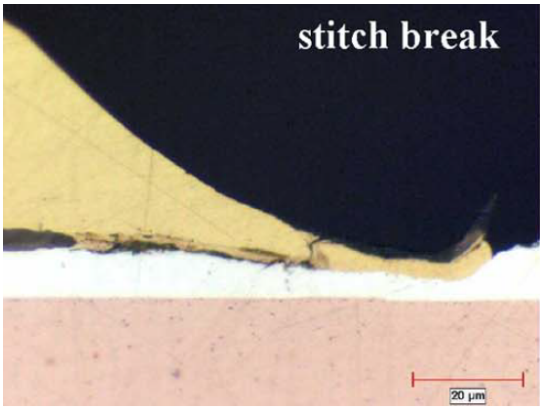

Figure 2.23: Stitch Break [11]

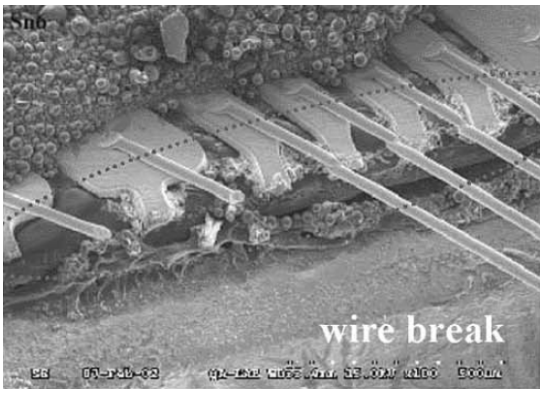

Figure 2.24: Wire Break [11]

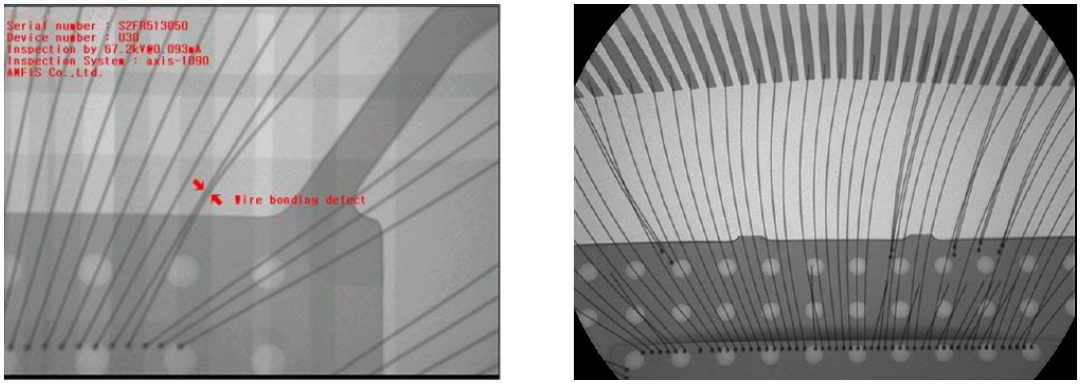

Figure 2.25: Wire Sweep [2]

2.4. Multi-physics FE modelling

The failure of solder joints is primarily because of two processes which occur in three stages: viscoplastic deformation followed by crack initiation and crack propagation that leads to a failure [31]. Figure 2.26 illustrates the failure process of solder joints during a drop test, where stage 1 represents crack initiation. Here, the static and dynamic resistance increases eventually as the number of drops also increase. Stage 2 is the crack propagation where the peaks observed mean that the crack is quickly propagating and stage 3 represents the crack opening.

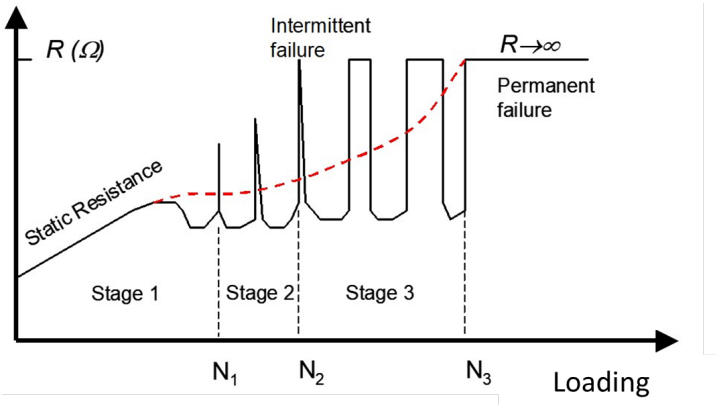

Figure 2.26: Geometric variable for a bond pull test [12]

A similar trend may be observed for wirebonds in a scenario wherein the wirebonds are subjected to thermal shocks or thermal cycling until failure is observed. The thermal cycling affects the wirebonds by changing their resistance over time. The resistance of the wire is given as:

$$R_w = \frac{\rho l}{A} \tag{2.5}$$

where ρ is the resistivity, l is the length, and A is the area of cross-section. The relationship between temperature and resistivity does not have a simple mathematical relationship but can be understood by quantum mechanics. As the temperature rises, the number of phonons also increase [45], which is the source of the resistance. So, technically, as the temperature increases the resistance also increases in conductors. There are two equations; one is a linear function of temperature 2.6 and the other is a power relationship 2.7, for materials like Tungsten.

$$\rho = \rho_0(1 + \alpha(T - T_0)) \tag{2.6}$$

$$\rho = \rho_0(T/T_0)^{\mu} \tag{2.7}$$

where T-T_0 is the temperature difference and α is the resistance temperature coefficient. In retrospect, as the wirebonds undergo thermal cycling, there shall be fatigue growth after a certain period of time which inevitably leads to an increase in the resistance of the wirebonds. Furthermore, how this can be carried out will be explained in detail in Chapter 3.

Several models have been made for wirebonds to mimic fatigue and their failure by using finite element calculations. But the first simulation for wirebond looping was reported in [46]. In this paper, a quasi-static analysis was performed but as an improvement to their simulations, the same group later reported wire-tensioning and the kick-up effect in their simulation for wedge bonds [36] where they used the FE software ABAQUS ver 6.1. and further reported dynamic effects for ball-wedge wire bonding in [47]. A linkage-spring model with multiple degrees of freedom is designed in [48]. In this paper, springs are used to simulate the forces acting on a section of the wirebond. The elastic-plastic deformation is simulated with the help of the bending angle of two linkages. A number of looping profiles for gold are simulated and it's claimed that necking and fracturing during the bonding process can be prevented by the method used in [48].

To model stress in FE models, accelerated testing is a common practice. One such example is in [13]. The lifetime of Aluminium wirebonds in IGBT (Insulated Gate Bipolar Transistors) modules is predicted using accelerated test results and the Coffin Manson model approach. This approach is often used to model crack growth via temperature cycling [49]. The Coffin-Manson equation for low cycle fatigue (LCF) is:

$$N_f = A(\epsilon_P)^B \tag{2.8}$$

where N_f is the number of cycles to failure, ϵ_P is the effective plastic strain, and A and B are Coffin Manson parameters, that can be determined by calibration. In [13], for calibration, the fatigue data is obtained from the temperature cycling tests of wedge-wedge Al bonds, with 2 hrs cycle time, ramping between -55°C and 150°C. Other experiments with different temperature ranges were also carried out. A 3D FE model see in Figure 2.27 was made for the Al bond using TED-ISE [50] tensor grid editor and simulations were performed with SOLIDIS-ISE.

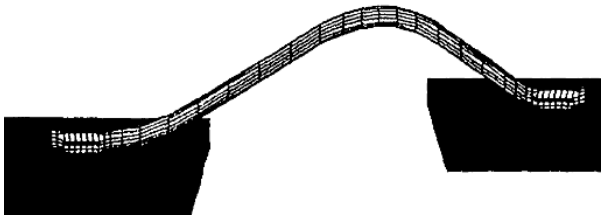

Figure 2.27: Initial 3D finite element model of the Al wirebond and the bond pad [13]

Here, it was concluded through experimental and numerical calculations [51] that the bond heel is a critical location for crack initiation and growth. In the FE simulations, the elasto-plastic stress-strain law was applied that influenced the calibration in Coffin-Manson law and resulted in predicting the lifetime. For the analytical calculations, a linear relationship was assumed between plastic strain and temperature swing and results in lifetime between the results obtained by FE simulations.

Similarly, another model was made in [14] for Al wires in the ceramic air cavity package for LDMOS. Here, FEM was used to calculate the stress in the heel as a function of loop shape, current and pulse time. The multi-physics coupling involved electro-thermo-mechanical simulations to derive S-N curves (Basquin relation) where S is the stress i.e. iterative load and N is the number of cycles to failure. Though the second bonding angle is of importance, it was found in this paper that the first bond was where failure always occurred as seen in Figure 2.28. Low cycle fatigue is usually described by the Coffin-Manson model that uses the strain-life approach but high cycle fatigue is generally described by the Basquin equation 2.9.

$$N_f = C_1(\Delta\sigma)^{-C_2} = \left(\frac{\Delta\epsilon_P}{2\epsilon_f}\right)^{-C_2} \tag{2.9}$$

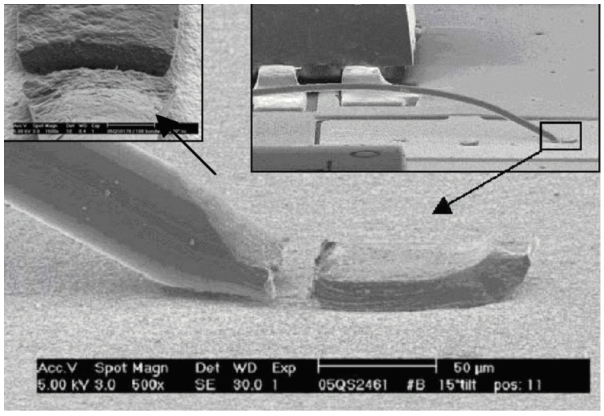

Figure 2.28: Failure at the heel after 10^7 cycles [14]

where ϵ_f represents fracture stress of the material, C_1, and C_2 represent material dependent constants. [14] concentrates on high-cycle fatigue because it cannot be detected by the standard qualification tests; a transition was found from low to high cycle fatigue between N_f=1-10K cycles that can be observed in the changing exponent in the power law relationship between relating strain and N_f. Two FE models are made using Ansys^{TM}9.0, a 2D model to simulate the bonding process and a 3D model which a electro-thermo-mechanical model used to calculate the stress amplitude in the heel of the wire.

The wirebonds are usually surrounded by an encapsulant material. Due to different CTEs (co-efficient of thermal expansion) between materials, thermo-mechanical stresses play a role in the failure due to cracks and fractures [52] [53] [54]. Models with thermo-mechanical stresses and strains on the wirebond in a chip-on-board (COB) package with temperature cycling was simulated in [55]. Other such models including thermo-mechanical analysis can be found in [11] and [56].

3

EXPERIMENTS

3.1. Samples

The most important part of the experimental setup in this thesis is the wirebond samples. An automatic wirebonder is used to make gold wirebonds of different heights. These wirebonds are made at APC (Advanced Packaging Center). The need for an automatic wirebonder is so that there is consistency maintained in the heights of these wirebonds. The Au wirebonds have a diameter of 1 mil or 25μm and are bonded on an Au coated ceramic DIL 24-pin package, the schematic of which can be seen in Figure 3.1 and the specifications of the package can be found in the Appendix **??**. It is important to note that the scope of this thesis is to study the wirebonds itself but not its interface to the package. Hence, a package with any number of pins could have been chosen, and 24-pin DIL package was chosen because of its availability. Figure 3.2 gives a realistic depiction of how the packages look.

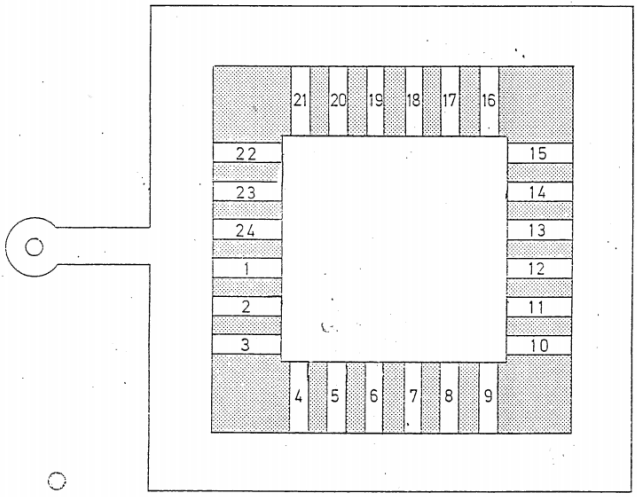

Figure 3.1: DIL 24 pin package schematic from Spectrum-semi

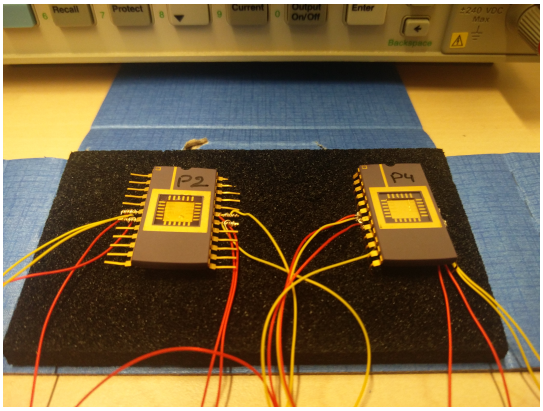

Figure 3.2: 24-pin DIL packages used for the experiment

3.1.1. Sample Specifications

Three sets of samples have been made and all the samples are made on the 24-pin DIL packages. One set of samples consists of two packages and each package has 16 wirebonds bonded on it; eight on the left side of Figure 3.1 and eight on the right side of it. The bondpads used on the left are 22, 23, 24 and 1, and 15, 14, 13 and 12 on the right. Each bondpad has two wires bonded to the base of the package which also has an Au coating. This is depicted in Figures 3.3 and 3.4.

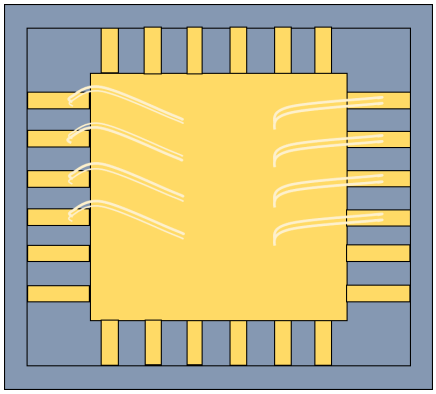

Figure 3.3: Top view of wirebonds on 24-pin DIL package

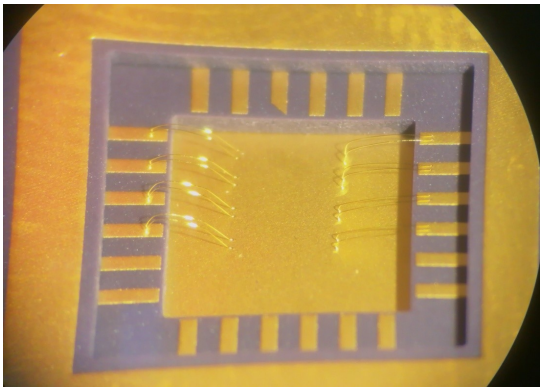

Figure 3.4: Wirebond samples

The machine settings are same for each package. Though, on the left the machine bonds in the high-low-high direction and on the right, low-high-low. This automatically gives a different angle to the wedge. These wires also have a bump under the wedge. This method of wire bonding is called Bump Stitch On Bump (BSOB) and the different steps involved in the process is shown in Figure 3.5.

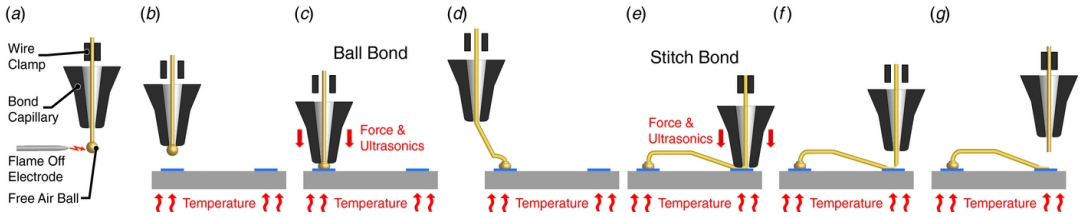

Figure 3.5: Process steps involved in Ball Stitch On Bump technique [15]

Ball Stitch on Bump is a process method for wire bonding that is flexible and has a high degree of freedom for different loop shapes and directions [57], [25] [1]. This process is a preferred choice for low cost and high volume production for applications, and has high reliability and throughput. Figure 3.5(a) shows how gold is fed through the capillary and an EFO causes the gold to melt to form a FAB (Free Air Ball) at the end of the wire which is then pulled towards the tip of the capillary which is then positioned above the bond pad Figure 3.5(b) where the first bond is to be made. The bond pad is placed on a heated piece holder. Figure 3.5(c) illustrates the tool pressing against the bond pad with a certain amount of force, and with ultrasonic (US) energy acting simultaneously the bond is formed. The tool now moves towards forming its second bond on the second bond pad Figure 3.5(d) and the stitch bond is formed with US energy and forces acting on it, seen in Figure 3.5(e). The tool now moves straight up, after the wire clamp is closed, thus tearing off the wire, see Figure 3.5(f) and Figure 3.5(g).

This method, that involves a ball bond provides quite a bit of flexibility as the circular shape of the ball bond offers a 360° freedom to loop and bend [15]. In contrast, if it were a wedge bond, the direction parameter is constrained as it is already pre-determined [1]. Common loop shapes in packaging is illustrated in Figure 3.6. Figure 3.7 shows the top view of the wirebond sample. All the samples look similar when seen from the top view. Figures 3.8, 3.9, 3.10 and 3.11 show the shapes of the wirebonds highlighting the kinks for samples PRD3 and PRD4. Both the samples have one loop, the former with a loop height of 200μm and the latter with a loop height of 400μm. The tool parameters for the samples are listed in tables 3.1 and 3.2.

Table 3.1: Pull forces for PRD3

Sample: PRD1 and PRD2		
Parameters	Left	Right
USG	80 mA	50 mA
Time	15 ms	15 ms
Force	120 g	100 g

Table 3.2: Pull forces for PRD4

Sample: PRD3 and PRD4		
Parameters	**Left**	**Right**
USG	40 mA	20 mA
Time	15 ms	15 ms
Force	140 g	110 g

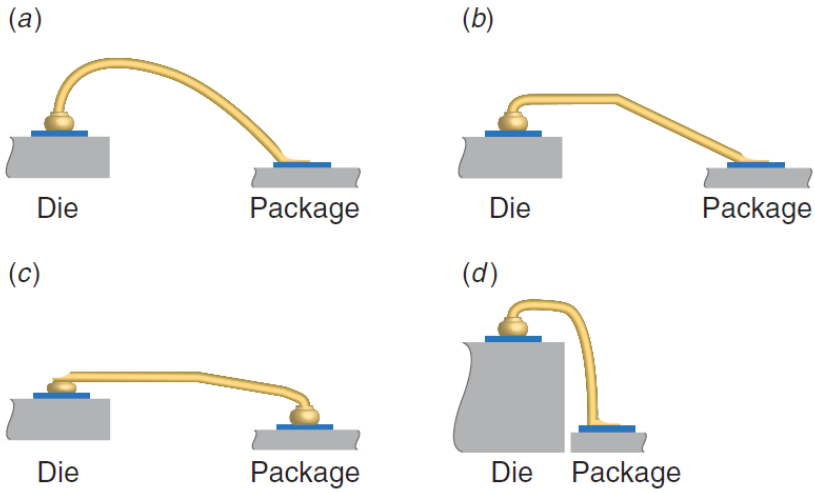

Figure 3.6: Loop shapes: (a) Standard forward loop (b) Flat forward loop (c) Reverse loop (d) Chip scale package (CSP) loop [15]

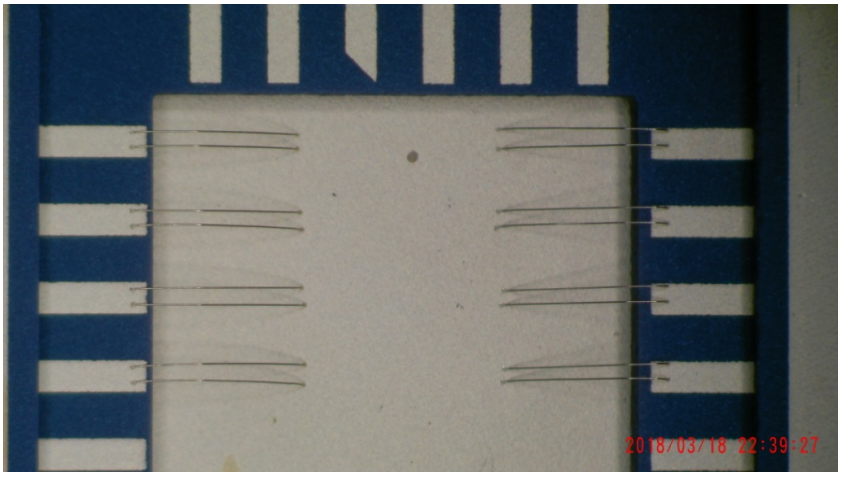

Figure 3.7: Sample PRD3 top view

Figures 3.8, 3.9, 3.10 and 3.11 portray the wirebond shape with one kink from the side view. Another set of samples are made with the same settings, and the cavity of the package is filled with standard Silicone [58], so that it behaves as an encapsulant like in an LED. Figure 3.12 shows the cross-sectional view of a high power LED package with the Au wirebond and the placement of the Silicone encapsulant. The Silicone is mixed and then manually added to DIL 24-pin package's cavity where the wirebonds are already present. This is placed inside the oven at 50°C for 24 hours so that the Silicone is cured properly before temperature cycling these samples. Figure 3.14 illustrates how the package appears with the mixed silicone 3.13 in its cavity.

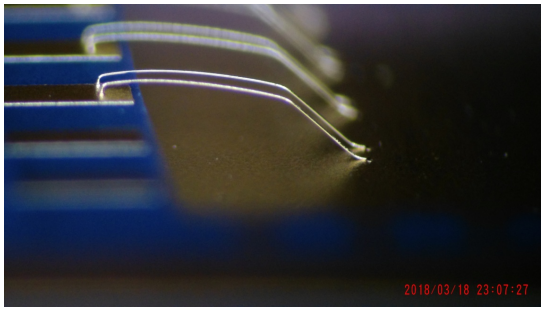

Figure 3.8: Left sample PRD3

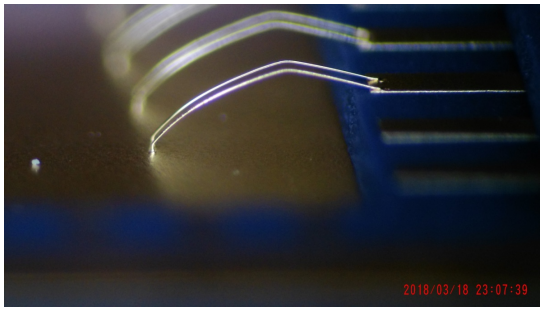

Figure 3.9: Right sample PRD3

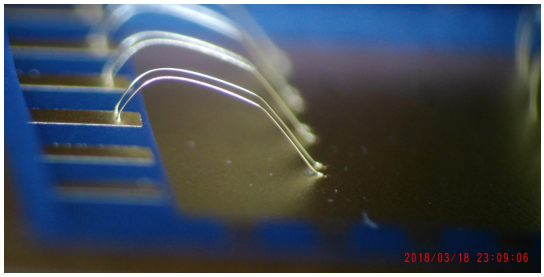

Figure 3.10: Left sample PRD4

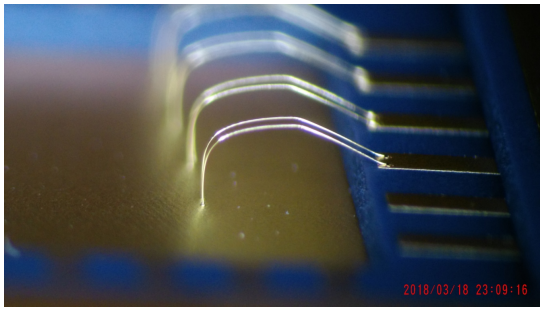

Figure 3.11: Right sample PRD4

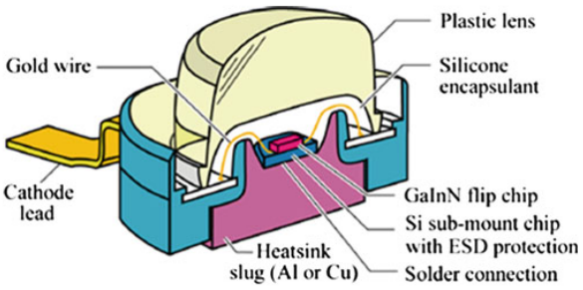

Figure 3.12: Cross-sectional view of an LED with various components inside [16]

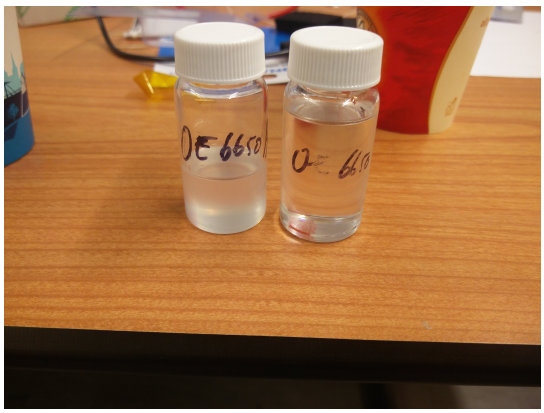

Figure 3.13: Silicone

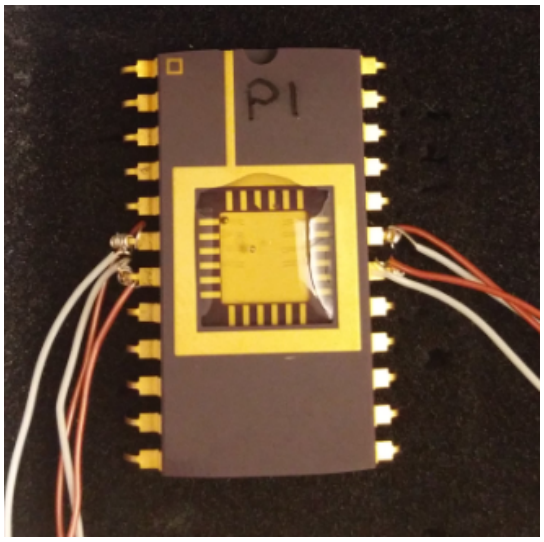

Figure 3.14: PRD1 with Silicone encapsulant

3.2. Experimental Setup

The experimental setup consists of designing the 4-wire resistance measurements setup and the wire-pull test setup. Section 3.2.1 reports all the components and materials that have been used in the experimental setup. It gives an explanation of how the component works and its functions that are relevant to this setup. Section 3.2.2 explains in detail how the four-wire resistance measurements setup is made using the components mentioned in the previous section. Furthermore, section 3.2.3 explains the temperature profile that has been selected for thermal cycling of the wirebonds. The following section 3.3 describes the data logging code written in LabVIEW. Section 3.4 explains the operation and principle involved in the four wire resistance measurements. Finally, section 3.5 explains the wire pull-test setup.

3.2.1. Components and materials

Components:

- Agilent 34970A Data Acquisition/Switch unit
- Agilent 34420A 7 $\frac{1}{2}$ digit Nano Volmeter/Ohm meter
- TPS Tenney oven
- WATLOW Ramping controller
- LEMO FVN-1S connector cable
- Resistors (1KΩ and 1Ω)
- A couple of RTDs (Resistance thermometers)
- Wire wrapping tools and wire
- Headers
- DIL 24-pin packages
- Automatic (programmable) wirebonder
- Soldering machine
- Digital multimeter
- Computer with LabVIEW or any data logging software compatible with the Data acquisition Switch Unit

Materials:

- Au wire (25μm)
- Silicone

Agilent 34970A Data Acquisition/Switch Unit

This instrument allows you to scan data by combining the DMM and the multiplexer channels. For a scan to occur, the instrument connects a digital multimeter to a multiplexer channel, and makes measurements for one channel at a time [59]. The DMM can be internal or external. The scan can include any channel that can be 'read' by Agilent 34970A, which includes voltage, temperature, resistance, frequency, current or period measurements or a combination of any of them on the multiplexer channels. For the scan to take place, the 34908A 40-channel single-ended multiplexer was used.

Scanning method: A scan list can be prepared for the instrument to scan only specific channels, by default the instrument scans all the channels from slot 100 to 300 and if a channel is skipped if not mentioned in the scan list. The * annunciator is turned on for each measurement. Up to 50,000 readings can be stored in the non-volatile memory, in retrospect, if there is a memory overflow the MEM

annunciator turns on.

The scan list can be activated by pressing the 'Measure' button followed by selecting the function, range and resolution. By choosing the 'Step' option, it allows the instrument to sequentially step through the scan list and make a measurement at each channel. If a channel needs to be removed from the scan list, the 'Channel Off' option can be selected. In order to stop a scan, the 'Scan' button should be pressed and held. In this case, since this instrument is being used to make 4-wire resistance measurements, after pressing the 'Measure' button, the knob on the right end can be rotated to select the 4 wire mode and pressing 'Measure' again. This instrument is connected to a computer that runs a LabVIEW code which helps in logging data, in this case resistance values of wirebond samples that are placed inside the cycling test chamber.

The 34901A Multiplexer module has two banks of 10 channels with two additional two channels for direct measurements with the DMM. Each of these channels switch both HI and LO components and during 4-wire resistance measurements, channel n is automatically paired with n+10 to provide the source and sense connections as well [59]. Figure 3.16 illustrates the internal parts of the module.

Figure 3.15: Agilent 34970A Data Acquisition/Switch Unit

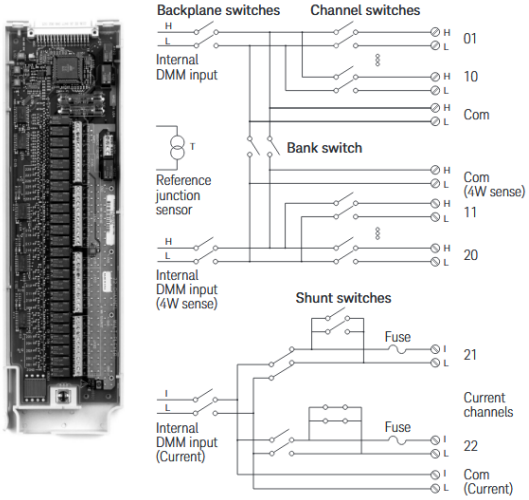

Figure 3.16: Agilent 34901A 20-channel multiplexer schematic

Agilent 34420A 7 $\frac{1}{2}$ digit Nano Volmeter/Ohm meter

The Agilent 34420A performs low-level measurements and in this thesis, this instrument is used as an ohm meter. The HI and LO connections from the switch unit is made to this module via the LEMO FVN-1S cable for 4-wire resistance measurements. The wires from the switch unit are soldered inside the cable and then connected to the source and sense channel on the ohm meter. This instrument reads the resistance values of the samples and the measurements can be logged into an Excel sheet via a code written in LabVIEW.

TPS Tenney Cycling Test Chamber

This cycling test chamber seen in Figure 3.18 is used as an oven for the temperature cycling of wirebond samples. The standard temperature range of this oven is -70°C and 200°C.

WATLOW Ramping Controller

The F4 1/4 DIN industrial ramping controller is used to program the ramp and soak processing of the thermal oven application for this experiment. The ramp allows a programmed change from one temperature set point to another. Figure 3.19 gives a self-explanatory description of different functions that can be viewed on the ramp controller. Several profiles can be setup using this ramping controller with the steps available, up to a total of 256 steps that is stored in the F4's non-volatile memory. This

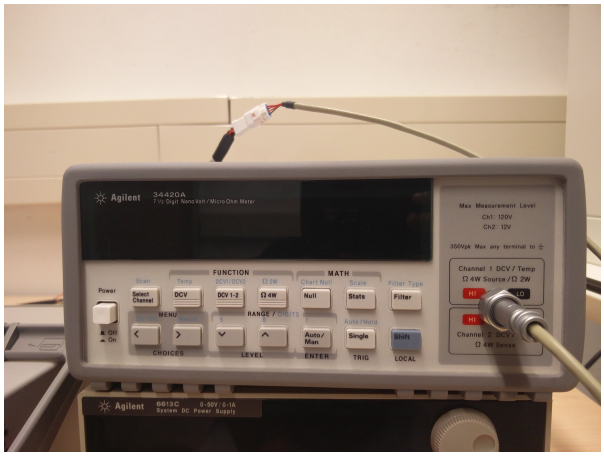

Figure 3.17: Agilent 34420A 7 $\frac{1}{2}$ digit Nano Volmeter/Ohm meter

Figure 3.18: TPS Tenney Cycling Test Chamber

also translates to the fact that a maximum of 40 different profiles can be setup, totaling 256 steps overall. While programming the profiles, steps can be added, edited or deleted accordingly and the profiles can be named/renamed at convenience. The different types of steps available are:

- **Autostart:** This allows a profile to start at a specific time and date and can be activated in the profile settings.
- **Ramp Time:** The ramp time shifts the Set Point (SP) temperature to a new value in a given period of time. If an event is programmed in the setup page, then the first step of Ramp time is to wait for that event's output. Following this, the time period is set, which decides the time involved to reach the set point temperature. The, the Set Point temperature (SP1) is decided for Channel 1 (if dual channel SP2 is also programmed). Post this, one of the PID settings (heat/cool parameters programmed in the Operations page) is chosen. The last decision to be made in this step is Guaranteed Soak is required or not; this allows the actual process value to remain in the Soak Band as decided in the System menu.
- **Ramp Rate:** This is similar to Ramp Time but it changes the SP temperature value at a given rate and is valid for single channel only. This step can be defined by waiting for an event similar

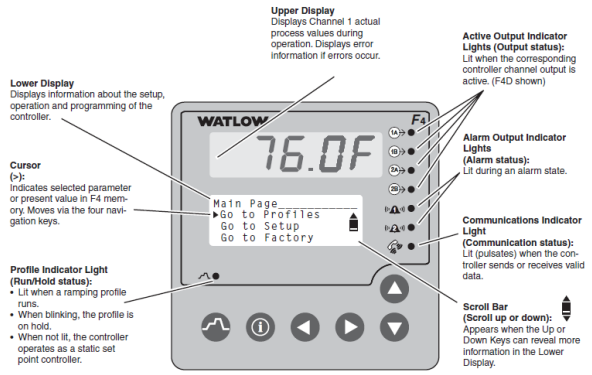

Figure 3.19: Button functions on WATLOW ramping controller [17]

to the previous step followed by defining the rate in terms of units per minute and set the SP value. The PID setting and guaranteed soak option is available again like in Ramp Time.

- **Soak:** This option allows the SP temperature to be maintained as it was set in the previous steps (Ramp Time or Ramp Rate). This also lets the temperature value to be maintained for a specified period of time that can be programmed. The way of defining this is similar to the Ramp steps.

- **Jump:** Like the name suggests, this step initiates a jump to another programmed profile or another step of the same profile. The Jump step can be defined by pointing to the profile that contains the step to which the program has to jump. Followed by pointing to the step and mentioning the number of repeats. The number of repeats allows the oven to thermal cycle several times through the same steps that have been programmed.

- **End:** That which is common in every profile programmed is the End step. This terminates the profile after the last step before End. The End step can be defined by ending with Hold, Control Off, All Off or Idle state.

3.2.2. Four-wire resistance measurement setup

This experimental setup connects the Agilent 34970A switch unit 3.15 and the Agilent 34420A micro ohmmeter 3.17 via a General Purpose Interface Bus (GPIB). The switch unit has an interface of two multiplexer modules fit inside it. HI and LO connections of Source and Sense leads inside the multiplexer module are wired via cables to the outside. Each of these cables has four wires that are orange (HI Source), red (HI Sense), brown (LO Sense) and black (LO Source). These wires are connected to a JST U-A connector. A similar cable consisting the four wires is used to connect the ohmmeter to the same JST U-A connector via the LEMO FVN-1S connector cableto enable 4-wire resistance measurement. The JST U-A connector connects to and AMP 1229 connector via four other wires: red, blue, white and yellow.

- Orange = Red
- Red = Blue
- Brown = White
- Black = Yellow

There is one channel connection between the switch unit and the ohmmeter via the JST U-A cable for interfacing. The rest of the multiplexer channel connections are wired to only a JST U-A connector which is linked to an AMP 1229 connector (Figure 3.20). This is connected to the header which has connections from the wirebond sample whose resistance needs to be measured. These wirebond samples are next placed inside the cycling test chamber for temperature cycling. Meanwhile, the ohm meter is connected to a computer for data acquisition (DAQ) of the resistance values. This setup is illustrated in Figure 3.21.

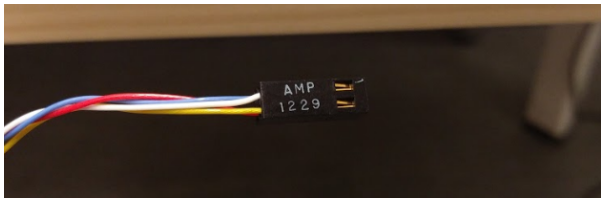

Figure 3.20: AMP 1229 connector

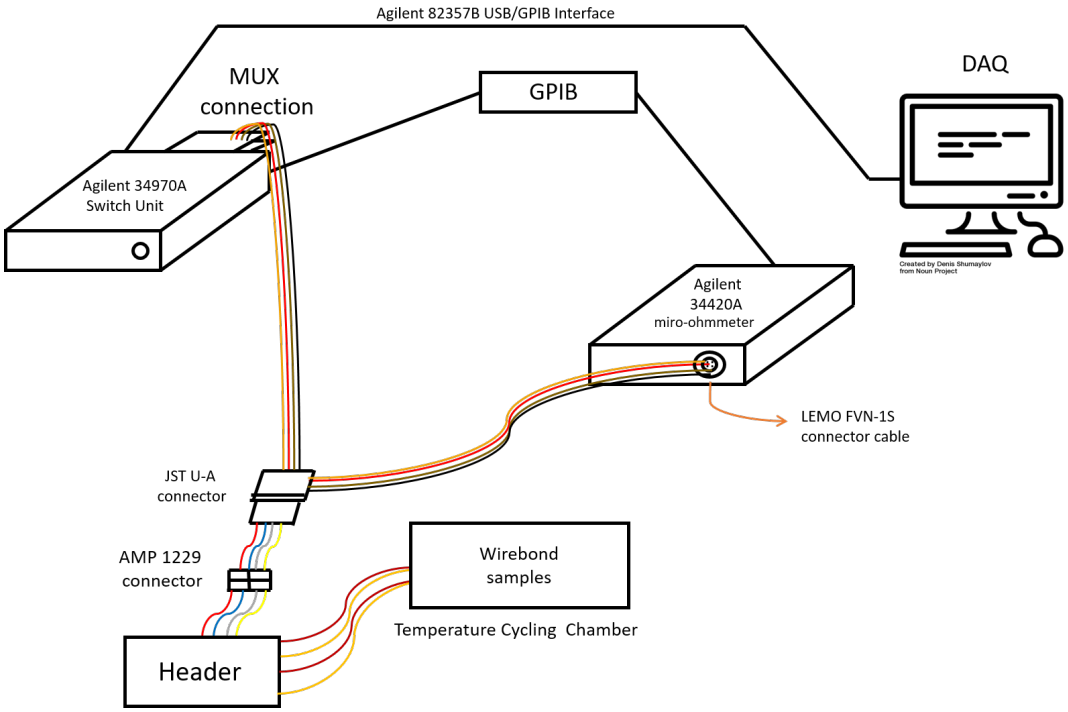

Figure 3.21: 4-wire resistance measurement experimental setup

3.2.3. Cycling Test Chamber Temperature profile

The TPS Tenney oven offers several options to setup a profile for temperature cycling. In this oven, 256 steps can be programmed from options like: ramp rate, ramp time, soak, jump and end. The profile programmed for the experiment-in-question's thermal cycling is called 'RUNN' and has 7 steps:

Step 1: Ramp Rate = 4°C/min
SP temp = 117°C

Step 2: Soak
time = 15min

Step 3: Ramp Rate = 4°C/min
SP temp = -50°C

Step 4: Soak
time = 15min

Step 5: Ramp Rate = 4°C/min
SP temp=24°C

Step 6: Jump to Step 1 of RUNN
No. of repeats = 25 repeats

(if thermal cycling needs to run for two days, the number of repeats can be edited for longer or shorted periods of thermal cycling)

Step 7: End-All off

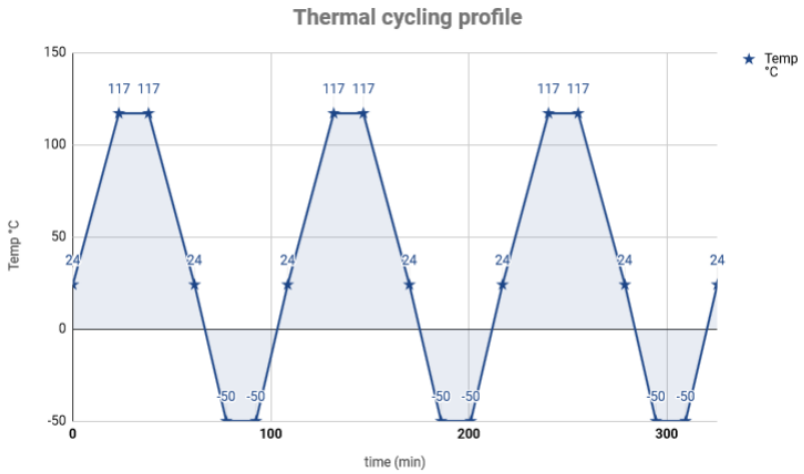

Figure 3.22: Thermal cycling Load conditions

A visual plot can be seen in Figure 3.22. The SP temperature in step 1 was set at 117°C instead of 120°C because during the Soak step, the temperature tends to overshoot and it was observed that, it reached 120°C in retrospect when the SP temp was set at 117°C. The reason for not exceeding °C is that, some of the samples are filled with Silicone as an encapsulant. And silicone tends to crack above 120°C which would be unfavourable to our experimental setup.

3.3. Data Acquisition

The measurements read from the ohmmeter can be simultaneously stored in a computer by data acquisition or data logging. The code for DAQ has been written in LabVIEW ver. 2017, a system design platform for visual programming. There are three critical steps for the resistances to be read and stored during temperature cycling: initialization of the switch unit and the ohmmeter, switching between channels, and data logging in an MS EXCEL sheet.

3.3.1. Initialization

A software called Keysight IO Library Suite (former Agilent Measurement Suite) can be installed in order to detect the devices connected to the computer; the code functions according to the requirement when the devices, switch unit and the ohmmeter are detected in the Keysight IO Library Suite software. Figure 3.23 shows that part of the code where the drivers for the switch unit and the ohmmeter are initialized in the LabVIEW code.

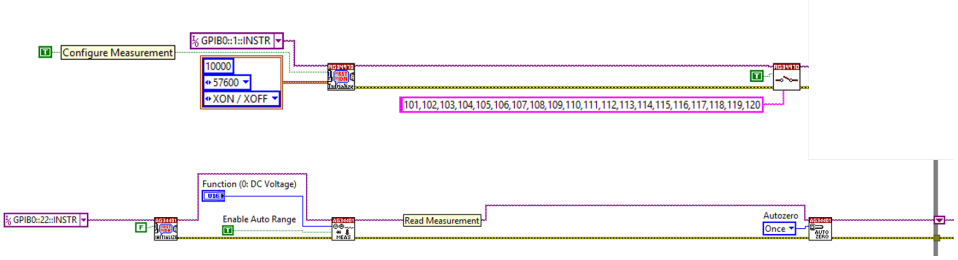

Figure 3.23: LabVIEW block diagram: Initialization

3.3.2. Looping

Figure 3.24 depictes the switching of channels in the multiplexer. The loop works in a way such that only the channels from the scan list programmed in the switch unit will be scanned, while the rest of the channels will be skipped.

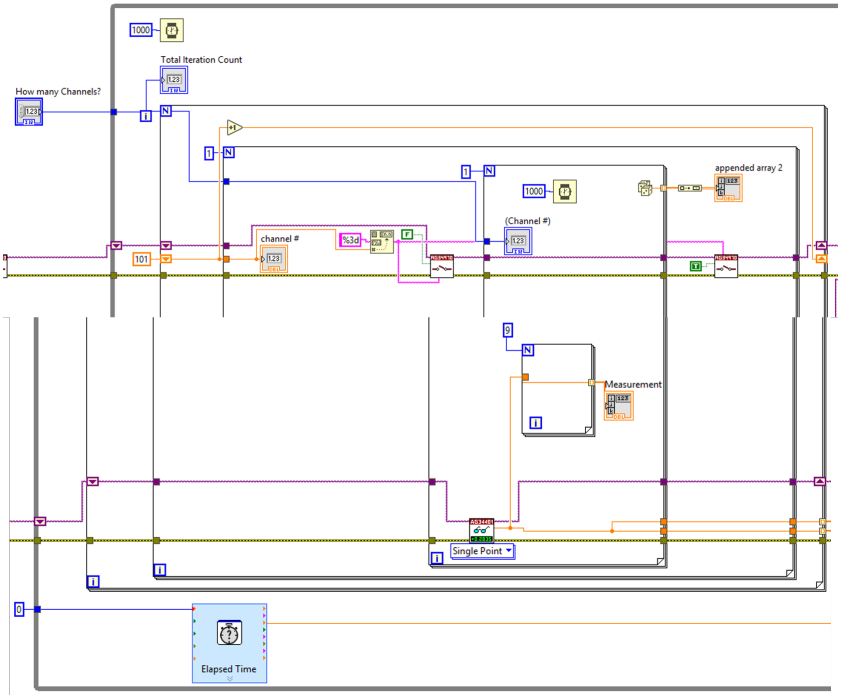

Figure 3.24: LabVIEW block diagram: Switching between multiplexer channels

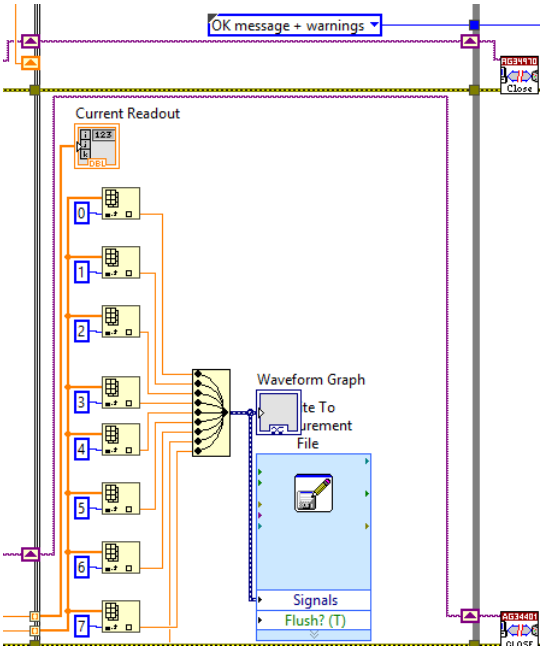

Figure 3.25: LabVIEW block diagram: Data logging

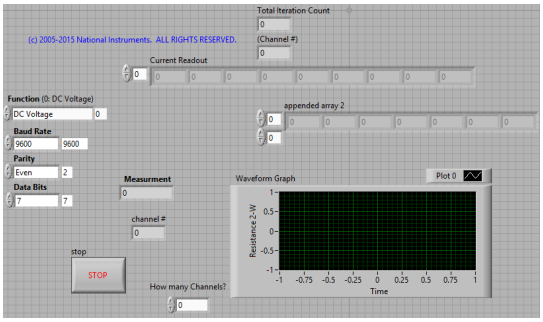

Figure 3.26: LabVIEW Front Panel

3.3.3. Data Logging

Seven channels were arbitrarily picked to store the resistance values of the wirebond samples, which may be converted into a waveform graph. The last channel is a resistance thermometer (RTD) connection that measures the temperature at which the resistance was measured. Figure 3.25 and 3.26 show the block diagram for data logging and the front panel of the LabVIEW code. It was previously set to store the data in an Excel sheet.

3.4. Operation and Principle

The setup is based on four terminal sensing or also known as four wire resistance measurements. The ohm meter 3.2.1 is used to measure the dc resistance of a circuit connected to its input. This operation is based on Ohm's law. This method of measuring resistance has separate current and voltage electrodes connected to the sample-under-test. This enables to eliminate the lead and contact resistances as opposed to two wire measurement, that gives a resistance value including the lead and contact resistances.

3.4.1. Four-wire resistance measurement

The internal DMM can measure the resistance of a circuit in two ways: 2-wire or 4-wire ohms. For the former method, the voltage drop of the resistance under test is sensed internal to the DMM. Hence, the test lead resistance is also calculated in the resistance value measured. Meanwhile, for 4-wire measurement, sense connections are required which are separate and because of this no current flows through the sense leads and so the resistance for this does not include test lead resistance values and does not give a measurement error. For both the methods, the test current flows from the input HI terminal through the resistance under test [59].

This method of measuring resistances is most accurate for small resistances especially below a 10Ω and is used in high-accuracy applications like RTD temperature transducers [59]. The added resistance from test leads, multiplexer and contact resistances are reduced by using the 4-wire ohms method. Current is passed through the current leads (source wires) from the switch unit. This causes a voltage drop to occur across the sample-under-test (wirebonds). A pair of voltage leads (sense wires) are also present along the sample-under-test but the voltage drop across them is negligible as current almost does not flow through the voltage leads. The value read on the ohmmeter is the accurate four-wire resistance measurement. The mechanism is seen in Figure 3.30.

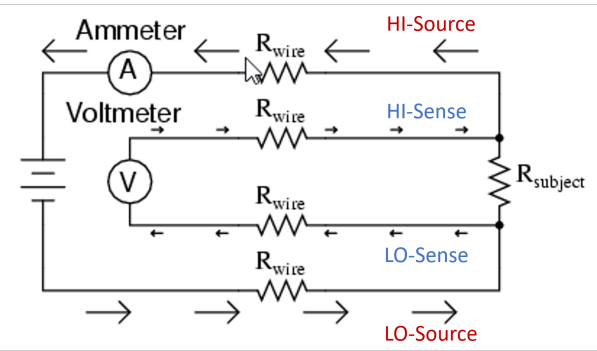

Figure 3.27: 4-wire resistance measurement setup

To measure the resistance of a wirebond on the package, the wires on two bond pads are considered, with two wires on each bond pad. The equivalent circuit of the wirebonds is illustrated in Figure 3.29 where the resistance of each wirebond is assumed to be R. The resistance of the samples taken before temperature cycling are reported in table 3.3. These values in Table 3.3 are those of the samples pointed in Figure 3.28. In retrospect, it was found that the resistances of all the wirebonds on one side of the package are confirmed to be the same and hence, the equivalent circuit works well to measure accurate resistances of the wires. A disadvantage of this method obviously stands as using twice as many wires and switches but the accurate resistance measurement compensates for this. It should

be noted that the four-wire resistance measurement is made by connecting the package leads to a header; and the header is connected to the ohm meter via four wires (source high, source low, sense high and sense low).

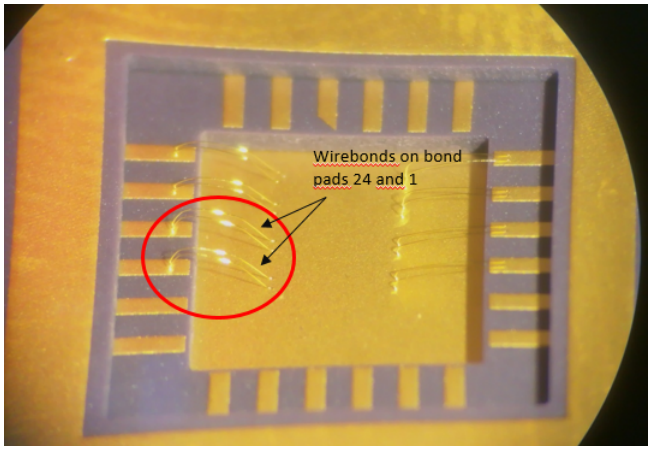

Figure 3.28: Wirebond samples in a package used for resistance measurements

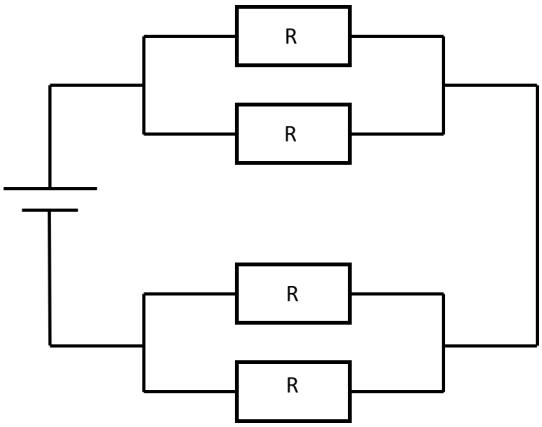

Figure 3.29: Resistance circuit for wirebond samples

Table 3.3: Resistance measurements of wirebond samples

Sample	Resistance (Ω)
PRD3	0.222
PRD4	0.255

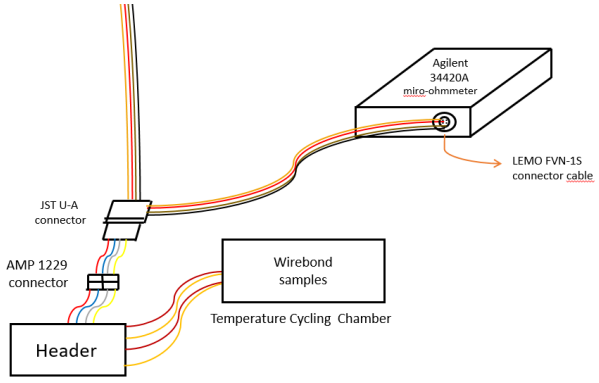

Figure 3.30: Experimental set up zoomed in to show the connection: wirebond-header-ohm meter

3.5. Pull test setup

The third set of samples are used to perform the wire pull test. The wire pull test tool used is Xyztec. For this test, a test type needs to be chosen with settings that gives the most failure modes. If the desired failure modes are not feasible, a test type needs to be chosen with a load synonymous to the real loading condition. The settings need to be such that it produces the highest force. The settings from the pull test can be seen in Figure 3.31 and 3.32.

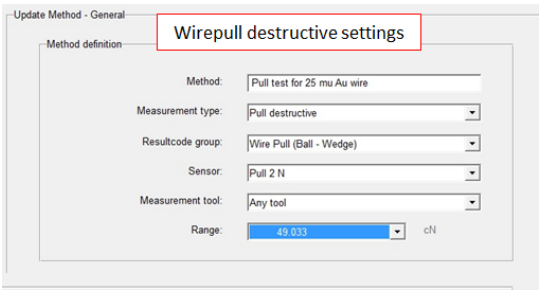

Figure 3.31: Xyztec pull test tool settings

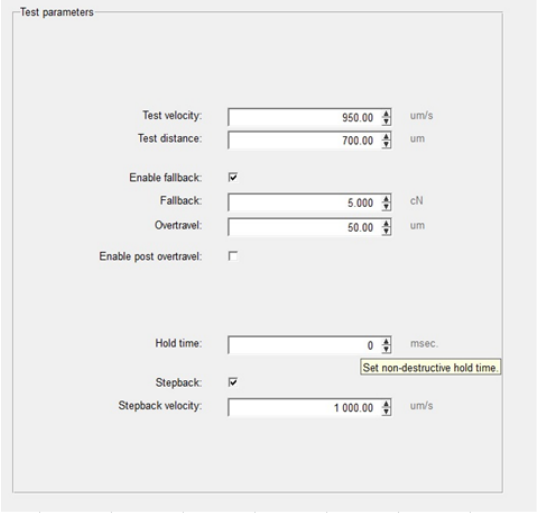

Figure 3.32: Settings contd.

The standard test hook used here has a shaft diameter of 50μm, foot length of 30mm, foot diameter of 150μm.

4

SIMULATIONS

Chapter 4 introduces stress and its effects which is an important parameter in the COMSOL™ model simulations. This is followed by section 4.2 that describes the modelling procedure of the 2D model geometry for finite element calculations. Section 4.3 discusses a 3D model made in COMSOL™ that replicates the four-wire resistance measurement and explains how the simulation is capable of giving accurate resistance measurements of wirebonds.

4.1. Stress

When a certain amount of stress is applied to a material, it experiences a respective strain which is elastic in nature. During initial deformation, stress and strain have a linear relationship as seen in Figure 4.1 which means that there is recoverable deformation. When the load is removed, elastic strain is recovered. But, when plastic strain plays a role, there is a non-linear relationship between stress and strain and results in plastic deformation. This occurs over the lifetime of a wirebond due to ageing. One of the common failure modes in wirebonds is wire fatigue which is directly related to the loop geometry of the wirebonds. This thesis makes an attempt to model the most important geometric aspects of these bonds and simulate their stress behavior using the Finite Element Package: COMSOL™ Multiphysics v. 5.2.

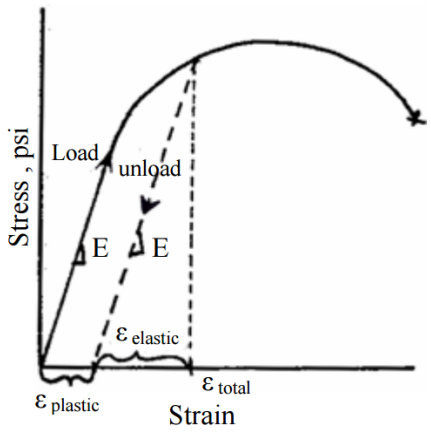

Figure 4.1: Stress and strain relationship

Fatigue testing of materials is a time consuming process. One of the ways to approach this issue is to reduce the time duration of the experiment or simulation while simultaneously increase the severity of the boundary conditions of the model [23]. In wirebonds, one of the major reasons for failure is the difference in the coefficients of thermal expansion of materials. The uneven thermal expansion leads to

a stress concentration in several areas of the loop geometry (stress is inversely proportional to area of cross-section of the geometry). By temperature cycling i.e. over cycles of heating and cooling (120°C and -50°C), this stress concentration continuously changes and exceeds the limiting value which leads to failure of the sample.

4.2. 2D modelling

Samples PRD3 and PRD4 are modelled in COMSOL™ Multiphysics v. 5.2 with the same geometry as those of the real samples. These wirebonds are made of gold with a diameter of 25μm. Both the wirebonds have one loop but apart from that, the latter has a span of 60%. The loop height of PRD3 is 200μm and that of PRD4 is 400μm, from the base where the first bond was made (left bond pad). The loop height is measured with the help of the Keyence optical microscope from TU Delft's EKL. The wirebond samples PRD3 and PRD4 are illustrated in Figure 4.2 and 4.3.

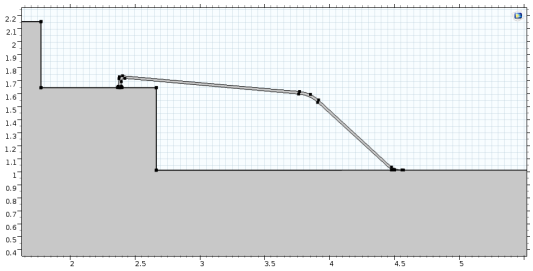

Figure 4.2: Geometry of wirebond sample PRD3

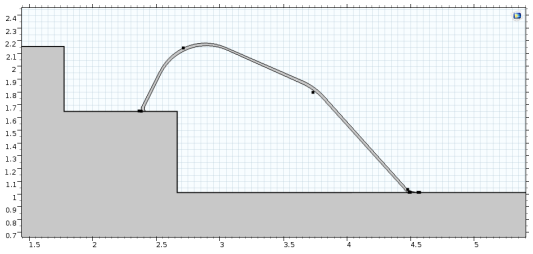

Figure 4.3: Geometry of wirebond sample PRD4

There are primarily four domains in the model. The wirebond is made of gold, and the package is made of alumina with a thin coating of nickel and another thin layer of gold on top. The size of the package is 30.48 x 15.49mm^2. The material properties of gold, nickel and alumina are listed in Table 4.1 and are taken from the in-built material properties of COMSOL™ Multiphysics v. 5.2. Figure 4.4 shows where these materials are used in the 2D model.

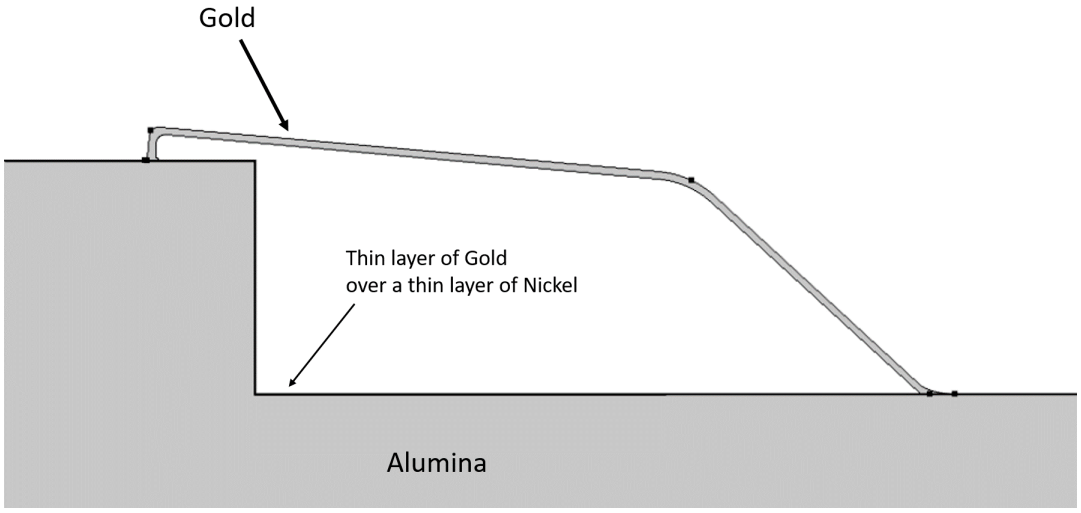

Figure 4.4: Material domains in the wirebond model

Each of these 2D models uses solid mechanics and fatigue and both the models use free triangular meshing. Solid mechanics helps in modelling creep formation in the wirebond sample and fatigue helps in calculating the cycles to failure. Initially, a transient study computed for a time period of 3600s results in plots of stress obtained in the wirebond model. Following this, the fatigue study is enabled in which the Coffin-Manson criteria is selected and a strain type of effective creep strain is selected. Solid

Table 4.1: Domain material properties for gold, nickel and alumina

Property	Gold	Nickel	Alumina
Coefficient of thermal expansion	14.2E-6 [1/K]	13.4E-6 [I/K]	8E-6 [I/K]
Heat capacity at constant pressure	129 [J/(kg*K)]	445 [J/(kg*K)]	900 [J/(kg*K)]
Density	19300 [kg/m^3]	8900 [kg/m^3]	3900 [kg/m^3]
Thermal conductivity	317 [W/(m*K)]	90.7 [W/(m*K)]	27 [W/(m*K)]
Young's modulus	70E9 [Pa]	219E9 [Pa]	300E9 [Pa]
Poisson's ratio	0.44	0.31	0.222

mechanics is interfaced with fatigue and the model is computed. These computations result in stress plots along with effective creep strain plots that are presented in the results chapter. Now, the fatigue study is added and the time dependent study is interfaced to the solutions and the last few cycles are selected in order to calculate the number of cycles to failure because including the initial cycles would lead to a biased fatigue assessment.

A stationary study of the 2D model of sample PRD4 is also performed wherein, a point load is applied at the heel of the wirebond and an upward force is applied to model the pull test results which will be discussed in chapter 5. Furthermore, this 2D model is also simulated to observe the displacement at the temperature when the bond is made.

4.2.1. Creep in Solid Mechanics

When there is finite amount of stress applied at temperature T, there is say, 'x' deformation that is observed. This process plays out well until the yield strength of the material (Au) after which, there is plastic strain in the material and at temperature T, the deformation is always going to be a summation of deformation 'x' and residual plastic strain. Hence, creep is considered in the modelling and is an important factor at higher temperatures. Wire bonding failure mechanism is generally creep [60] and this phenomena becomes essential at higher temperatures. In creep even though deformation changes over time, stress remains constant. Creep is encompassed by plastic deformation, but not visa-versa. Creep is a type of plastic deformation, whereby deformation occurs below the yield stress limit of the material. Of the three creep mechanisms seen in Figure 4.5 we only consider secondary creep in which the creep rate is constant. This secondary creep can then be represented by a double Norton law represented by equation 4.1.

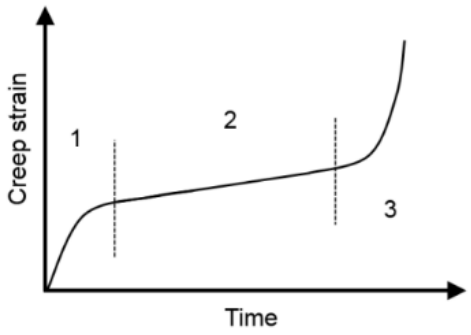

Figure 4.5: Creep strain mechanisms

$$Creeprate, \epsilon_c = A_I(\frac{\sigma_e}{\sigma_n})^{n1} + A_{II}(\frac{\sigma_e}{\sigma_n})^{n2} \tag{4.1}$$

where ϵ_c is the creep rate, σ_e is the effective stress, and A_I, A_{II}, σ_n, n_I and n_{II} are material constants that are listed in Table 4.2. Two terms exist, because one factor A_I describes creep at low stresses and is 12 times higher in orders of magnitude compared to A_{II} which describes creep at higher stresses. The two terms in the double Norton law helps to compute creep due to each individual contribution.

Table 4.2: Creep material constants [23]

Material constant	value
A_I	8.03E-12 [1/s]
A_{II}	1.96E-23 [1/s]
n_I	3
n_{II}	12
σ_n	1 [MPa]

4.2.2. Fatigue

Fatigue is a failure mode that occurs by repeated application of stress as depicted in Figure 4.6. And fatigue can be low cycle (<10E3 cycles) or high cycle (>10E3) as seen in Figure 4.7. Fatigue testing helps in determining the number of cycles to failure. Here, the load type plays an important role while modelling for fatigue and analysing it. It decides whether the fatigue model should be stress-life, strain-life or an energy-based one. An algorithm is presented in Figure 4.8, which is devised by Altasim technologies.

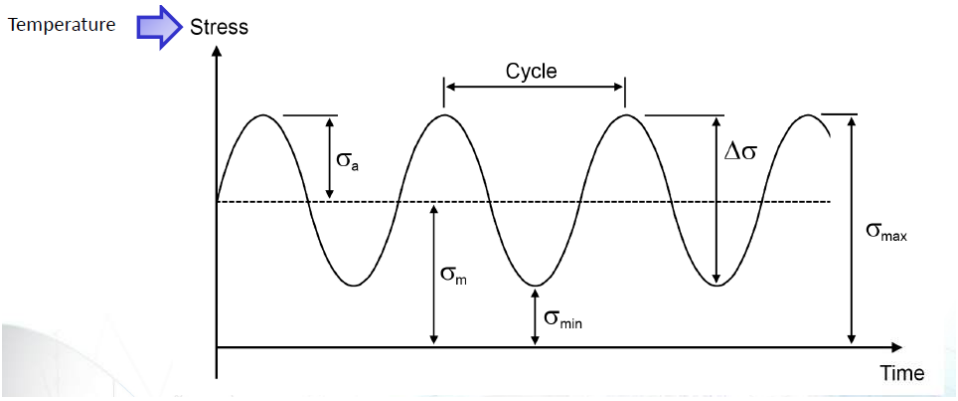

Figure 4.6: Fatigue [18]

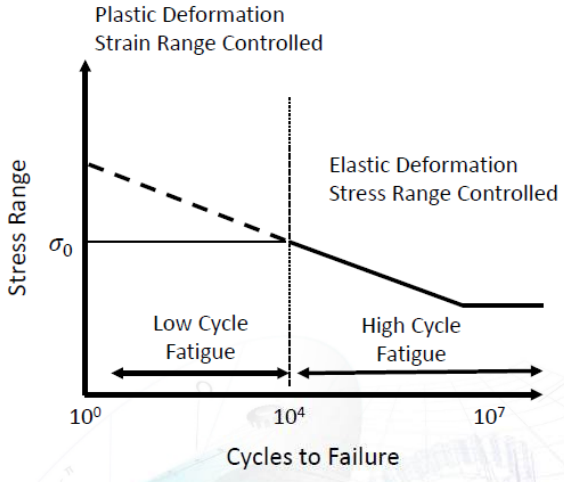

Figure 4.7: Low cycle and High cycle fatigue [18]

Fatigue modelling can be done with several types of models. A lot of these models share the same mathematical model, for instance the Coffin-Manson and the Morrow model [23]. The only difference in these models is whether it is energy driven or not. In this thesis, the Coffin-Manson approach strain-life based fatigue is used where the effective creep strain plot is computed.

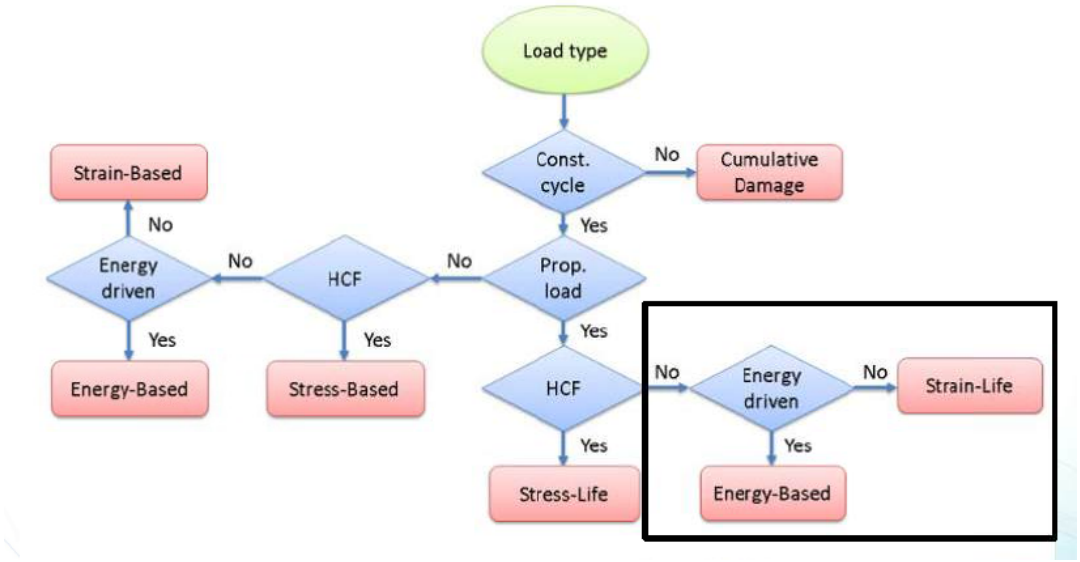

Figure 4.8: Fatigue assessment algorithm [18]

It should be noted that in the transient analysis, temperature is a function of time. The thermal load cycle reads the temperature and causes thermal strains. In all the plots from COMSOL™ there is acolour legend on the right which gives a range of either stress values or cycles to failure. In the stress plots, there is an additional legend that represents the effective creep strain.

4.3. 3D model

A 3D model of samples PRD3 and PRD4 is also simulated in COMSOL™ Multiphysics v. 5.2. This model is extruded from the 2D model and is further modelled to illustrate the wirebond sample in the DIL package used for the four-wire resistance experiment. This can be seen in Figure 4.9.

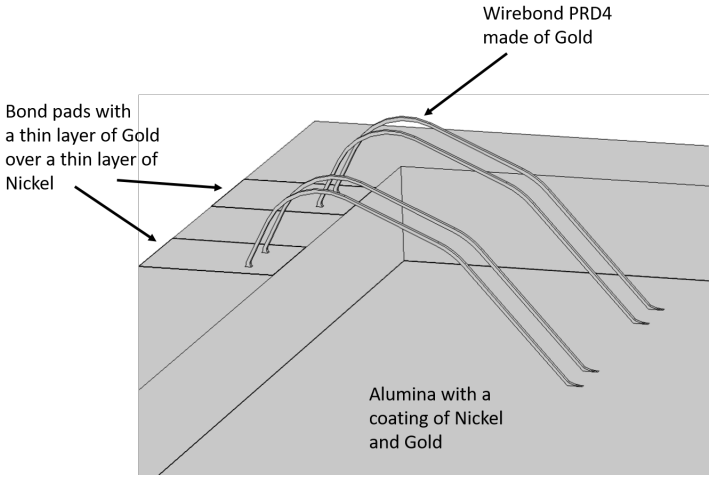

Figure 4.9: 3D model geometry of PRD4

This geometry is modelled with the Electric currents. The model is used to model the four-wire resistance setup. For this, the boundary conditions involve selecting four boundaries for the four-probe resistance measurement. This is illustrated in Figures 4.10, 4.11, 4.12 and 4.13.

The model is based on four terminal sensing or four-probe resistance measurements. An electric current of 1mA is passed through the Source high terminal and the Source low is considered as ground. A

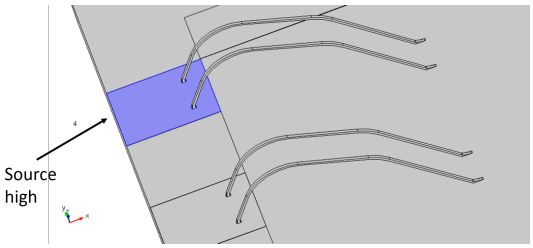

Figure 4.10: Source high in the 4-probe setup

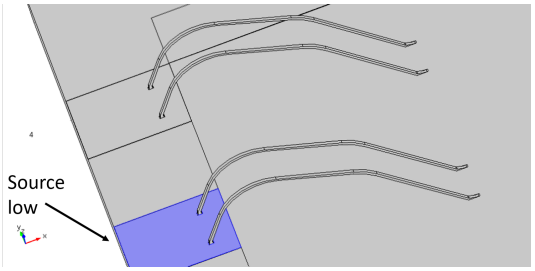

Figure 4.11: Source low in the 4-probe setup

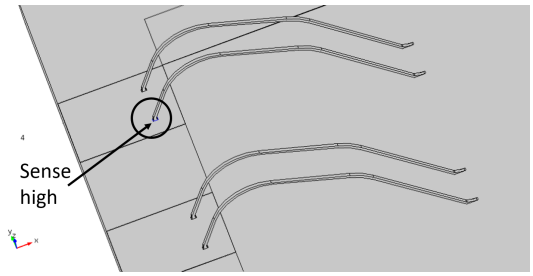

Figure 4.12: Sense high in the 4-probe setup

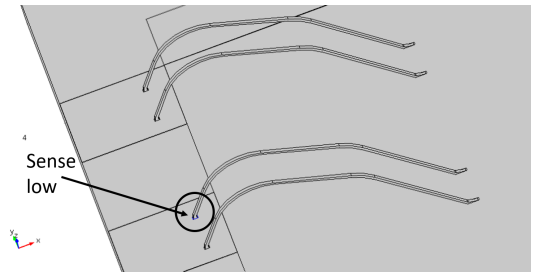

Figure 4.13: Sense low in the 4-probe setup

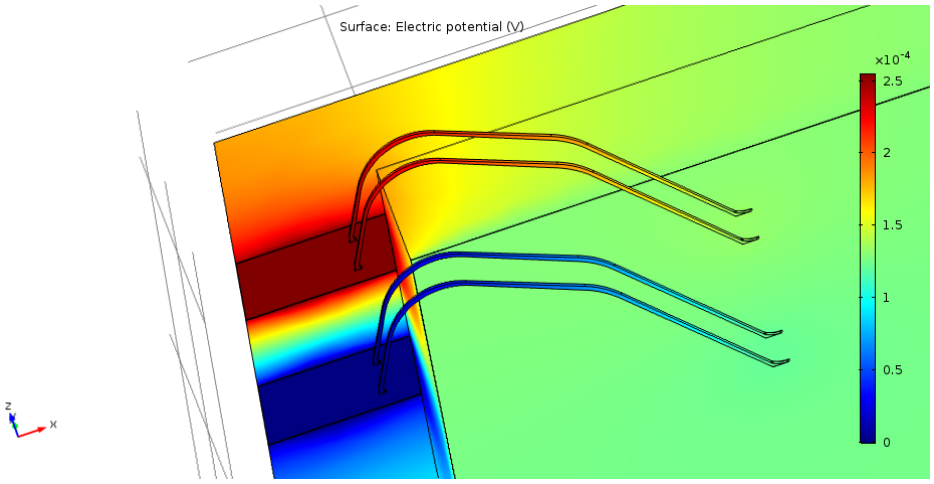

Figure 4.14: Electric potential plot simulation

stationary study computes the electric potential calculated through the wire seen in 4.14 and a global evaluation allows the accurate resistance measurement. This enables to eliminate the lead and contact resistances as opposed to two wire measurement, that gives a resistance value including the lead and contact resistances.

5

RESULTS

This chapter is divided into three sections. Section 5.1 reports the results from the pull-test performed on the wirebond samples. In this section, the pull-test results are compared with the 2D simulation results. In the following section 5.2, the experimental resistance results obtained are discussed. It also compares it to a 3D model simulated that replicates the 4-wire setup in COMSOL™. Finally, section 5.3 describes the stress results from the finite element simulations of the wirebond samples.

5.1. Pull-test results

The criteria for failure modes during wire pull are wire break (mid-span), neck (HAZ) break, wedge (heel) break. These criteria are illustrated in Figures 5.1, 5.2 and 5.3. Due to the melting process, looping and ultrasonic power used to attach the wire, the neck and the heel are the most sensitive parts. Usually, the thinner the wire, it is more flexible and is less susceptible to break. But, this too depends on the loop height. In retrospect, the results from the pull tests for samples PRD3 and PRD4 are listed in tables 5.1 and 5.2.

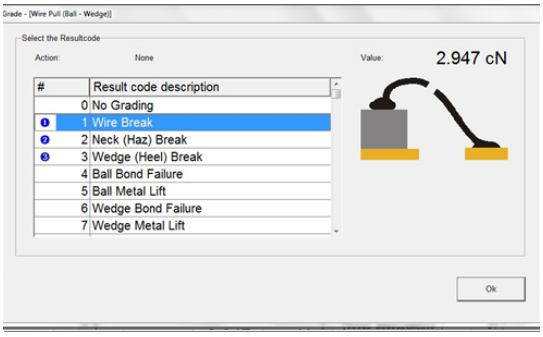

Figure 5.1: Failure mode: Wire break

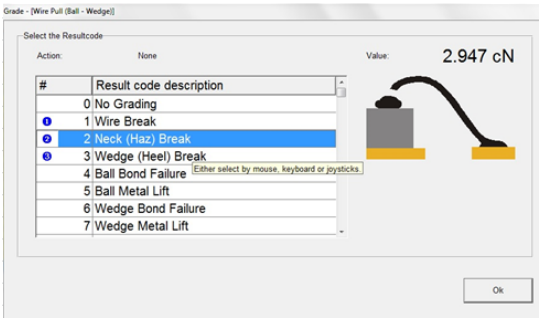

Figure 5.2: Failure mode: Neck (HAZ) break

The maximum and minimum forces are 13.4cN and 6.1cN (including the pull rest results for samples PRD1 nd PRD2) with an average of 9cN. The standard deviation is 1.5 and the Cpk is 1.26. The Cpk is the process capability index which represents quality.

5.1.1. Comparison with COMSOL™ simulation results

The pull-test is modelled in COMSOL™ Multiphysics v. 5.2. software for the PRD4 wirebond sample. A point load is modelled at the heel of the wirebond where the failure mode is expected to occur. A force of around 11cN is applied at the heel and the stress output is plotted which can be seen in Figure 5.4 with a stress of 250MPa. This value of stress was assumed as the Ultimate Tensile Strength (UTS)

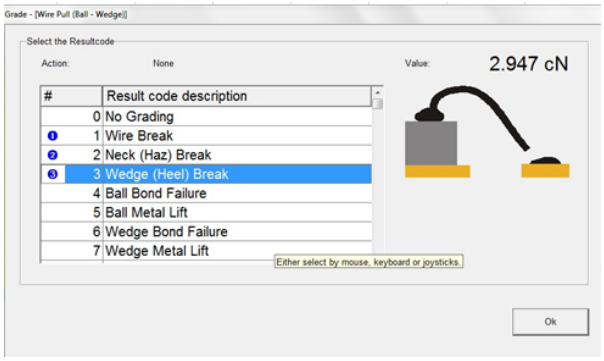

Figure 5.3: Failure mode: Wedge (Heel) break

Table 5.1: Pull forces for PRD3

	Left Wire pull [cN]	Right Wire pull [cN]
PRD3	9.172	7.548
PRD3	9.511	7.731
PRD3	8.562	9.213
PRD3	9.576	9.090
PRD3	9.137	8.426
PRD3	9.321	13.369
PRD3	8.963	7.564
PRD3	8.629	9.207

Table 5.2: Pull forces for PRD4

	Left Wire pull [cN]	Right Wire pull [cN]
PRD4	11.034	8.927
PRD4	10.950	7.532
PRD4	10.688	8.729
PRD4	11.073	7.408
PRD4	10.970	9.239
PRD4	11.177	8.908
PRD4	11.323	8.768
PRD4	11.067	9.580

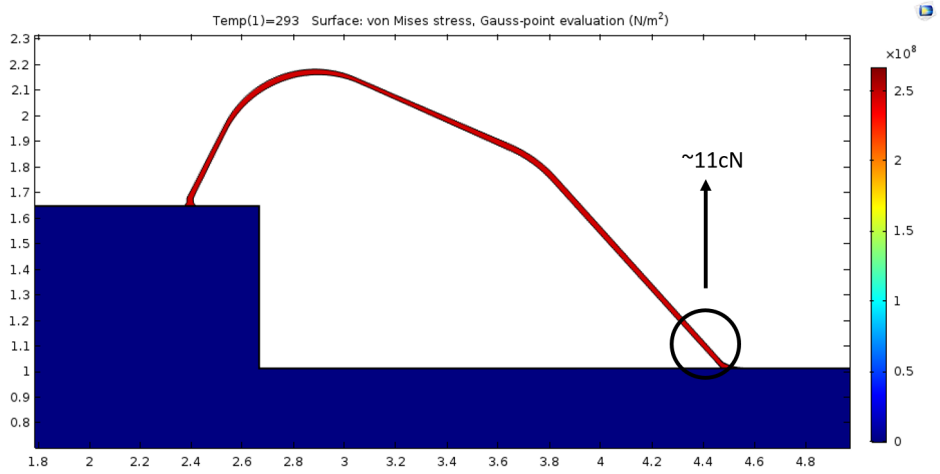

Figure 5.4: PRD4 pull test: stress plots

of gold seen in Figure 5.5 by Weimar et al. in [19]. In that paper, a similar range of temperatures were considered for thermal loading and a similar tensile fatigue test was performed. This comparison matches and shows that the wirebond breaks; hence the model is validated.

Thus, the COMSOL™ model stress output matches those of the pull-test experimental results. These results are validated due to a similar stress of 250MPa that is obtained.

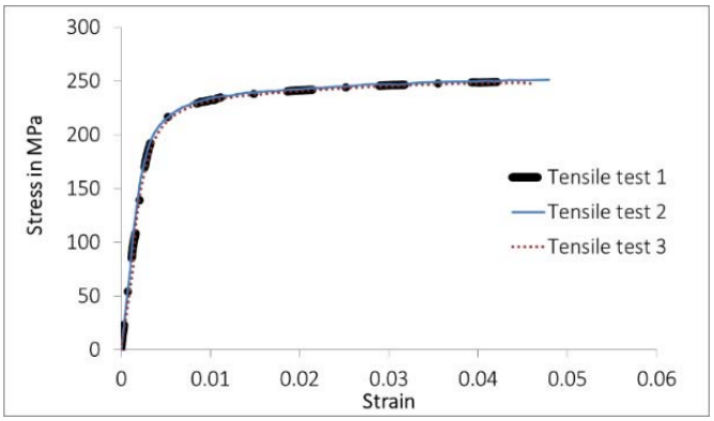

Figure 5.5: Stress-strain plots from tensile tests for gold wire [19]

5.2. Resistance results

As described in chapter 3, an experimental setup was made that enabled the measurement of wire-bond resistances using four-wire method. Table 5.3 lists the resistance values logged after temperature cycling. It is important to note that the resistance of PRD3 was 0.222Ω and that of PRD4 was 0.255Ω before temperature cycling.

Table 5.3: Resistance values of wirebond samples PRD3 and PRD4 before and after temperature cycling

Time	**PRD3 resistance (Ω)**		**PRD4 resistance (Ω)**	
	without Silicone	with Silicone	without Silicone	with Silicone
Before temp. cycling	0.222	0.241	0.255	0.263
After temp. cycling	0.225 (after ~255 cycles)	0.447 (after ~95 cycles)	0.258 (after ~255 cycles)	0.462 (after ~80 cycles)
		O.C. (after ~115 cycles)		O.C. (after ~100 cycles)

As the number of thermal cycles increased, an increase in the resistance of the wirebonds was observed. A common observation was that the samples with the encapsulant failed i.e. PRD3 failed between 95 and 115 cycles and PRD4 failed between 80 and 200 cycles after which the resistance could not be measured. The significant increase in the resistance values of 0.447Ω and 0.462Ω shows that the wirebond is close to the end of its lifetime.

5.2.1. Comparison with COMSOL™ simulation results

A 3D model was simulated in COMSOL™ that mimics the setup of wirebonds on the DIL package. This representation can be seen in Figure 5.6. The model was simulated with an electric currents physics with a current of 1mA passing through the wires. Through a stationary study, the simulation output shows an electric potential plot illustrated in Figure 5.7 for PRD3.

The electrical conductivity of Au is 30.30 S/m [61] and the reference diameter is 25um. The diameter of the Au wire is varied by $\pm 2u$m. Tables 5.4 and 5.5 present the resistance values while varying the diameter of the wire. The simulation resistance values differ from the experimental resistance values because the diameter of the wire might not be uniform throughout the bond, which would cause an increase or decrease in the resistance. It is to show this trend that Tables 5.4 and 5.5 show resistances for varying diameter values. Another reason might be because of the extrusion of the 2D model into 3D, which does not have a cylindrical shape for the wire. Furthermore, as the diameter is increased the resistance also decreases.

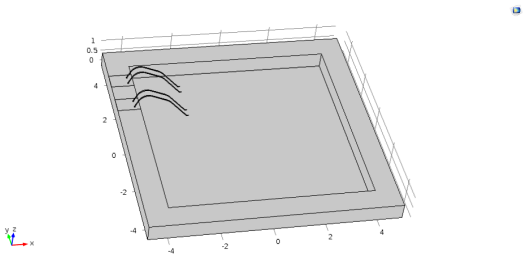

Figure 5.6: 3D model geometry of PRD4

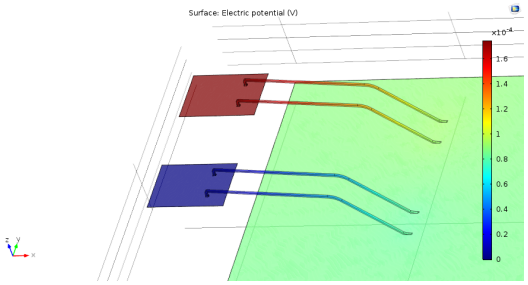

Figure 5.7: PRD3 electric potential plot

Table 5.4: Comparison of resistances for different PRD3 diameters

Sample PRD3			
Resistance method	Diameter (um)		
	23	25	27
2-wire resistance measurement (Ω)	0.18914	0.17474	0.16261
4-wire resistance measurement (Ω)	0.18900	0.17457	0.16247

Table 5.5: Comparison of resistances for different PRD4 diameters

Sample PRD4			
Resistance method	Diameter (um)		
	23	25	27
2-wire resistance measurement (Ω)	0.20597	0.19042	0.17656
4-wire resistance measurement (Ω)	0.20589	0.19036	0.17649

This shows the sensitivity of the wirebond's resistance w.r.t diameter of Au wire.

5.3. Finite element COMSOL™ simulation results

Two different geometries observed in PRD3 and PRD4 are modelled as seen in chapter 3 in COMSOL™ Multiphysics v. 5.2. Sample PRD3 has a low loop height and PRD4 has a higher loop height of 200μm and 400μm respectively. These samples are made at a high temperature 120°C. It is with the assumption that the initial stresses or intrinsic stresses are unknown when the wirebond is made and hence these stresses are not considered in the simulation, which makes 120°C a stress-free temperature. Therefore, the wirebond does not experience any displacement and the computed output is seen in Figure 5.8 for PRD4.

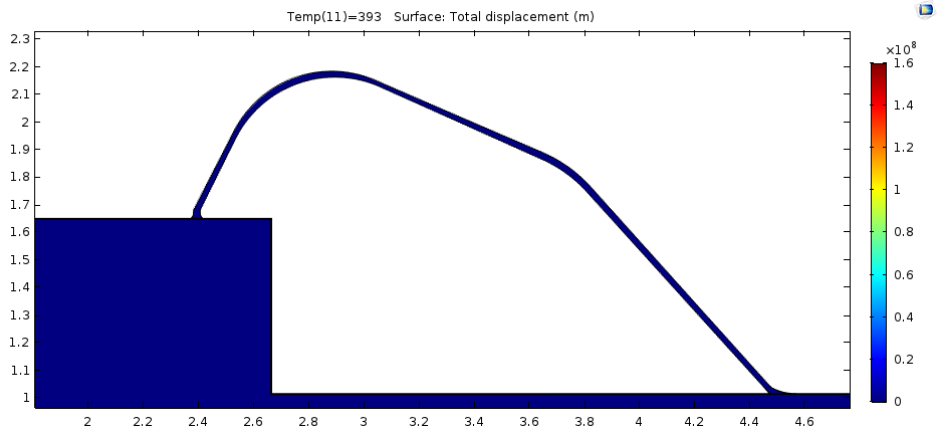

Figure 5.8: No displacement observed at 120°C

5.3.1. Stress results for sample PRD3 and PRD4

The COMSOL™ simulations were thermal cycled according to the temperatures seen in Figure 5.9 between -50°C to 120°C. This translates to the fact that each cycle was 60 seconds long and the time-dependent study was run for 3600s or an hour's equivalent which is 60 cycles. Figures 5.10 and 5.11 show the stresses observed at PRD3's neck and heel and figures 5.12 and 5.13 show the stresses observed for PRD4's neck and heel respectively at 3600s, which is at a temperature of 20°C. It should be noted that all the stress plots in this section are made using the same scaling.

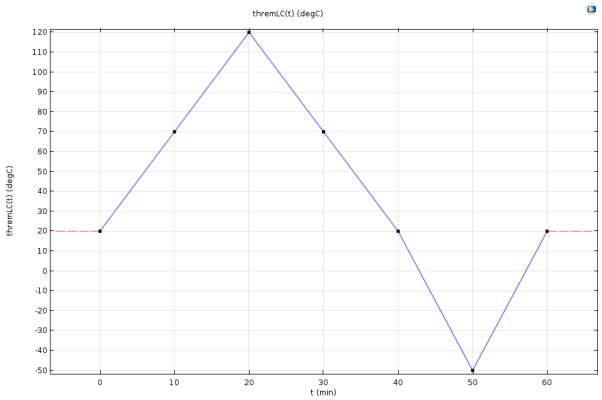

Figure 5.9: Thermal loading

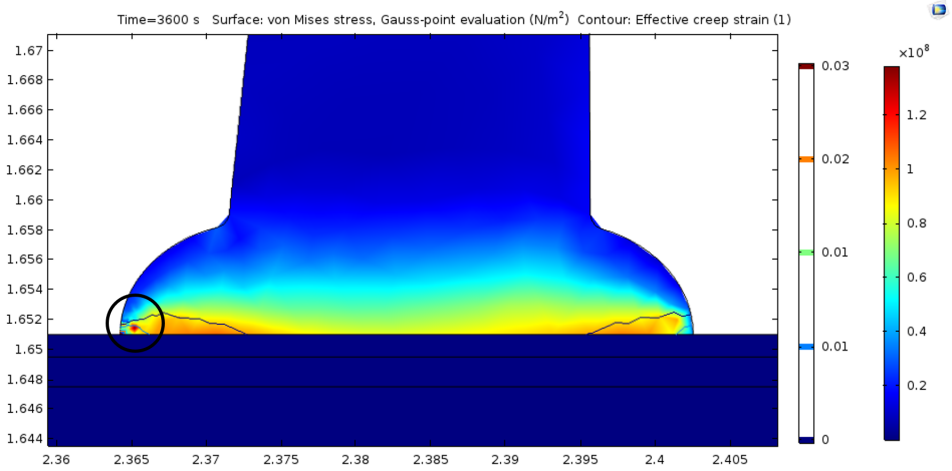

Figure 5.10: Stress plots at PRD3 neck

Table 5.6: Stress comparison between PRD3 and PRD4 w.r.t time and critical areas

Sample (height)	**Stress (MPa)**			
	t=3000s		t=3600s	
	Neck	Heel	Neck	Heel
PRD3 (200um)	267	255	121	63
PRD4 (400um)	307	78	139	90

Stresses vary with time due to temperature cycling. Table 5.6 compares the stresses obtained for PRD3 and PRD4 with loop heights 200μm and 400μm respectively, at two instances of time i.e. t1=3000s and t2=3600s which are at -50°C and 20°C respectively. The stresses presented were at the neck and the heel based on the contour line of the effective creep strength. These critical points are circled in figures 5.10, 5.11, 5.12 and 5.13. The above results show there are higher stresses in the neck w.r.t

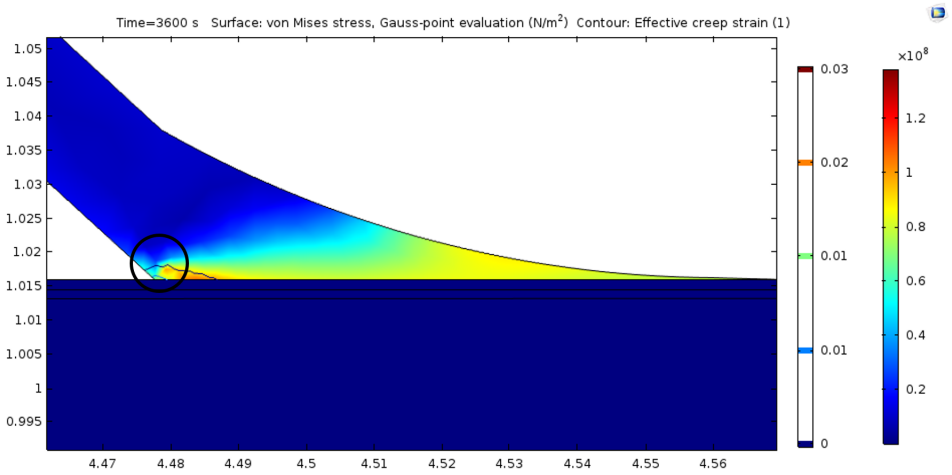

Figure 5.11: Stress plots at PRD3 heel

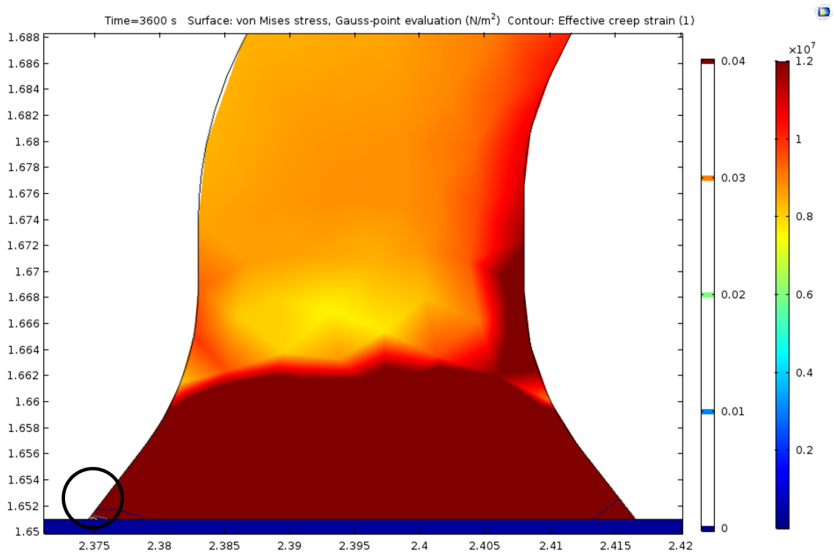

Figure 5.12: Stress plots at PRD4 neck

the heel. It also shows that a shift in the radius of the loop (which is dependent on the loop height) influences the stresses of the wirebond. The effective creep strain plot for PRD3 and PRD4 is seen in Figure 5.14 and 5.15. This plot shows how the creep strain spreads in the wirebond with time.

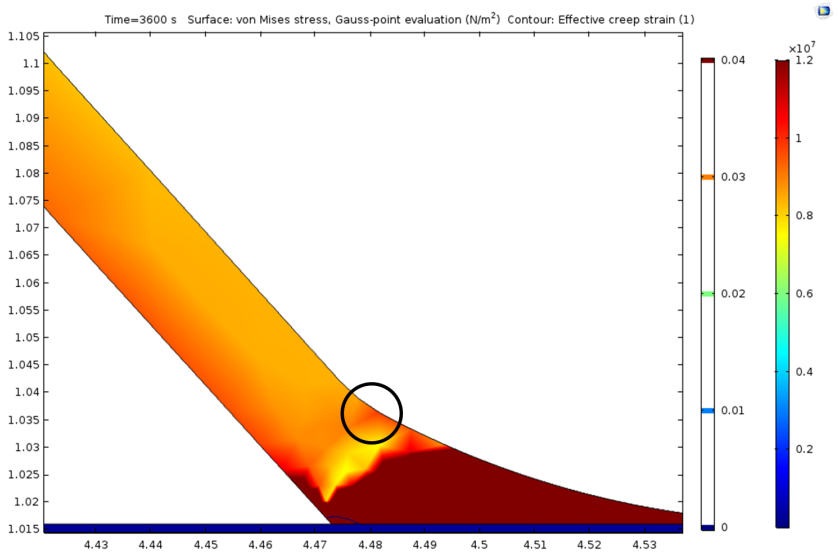

Figure 5.13: Stress plots at PRD4 heel

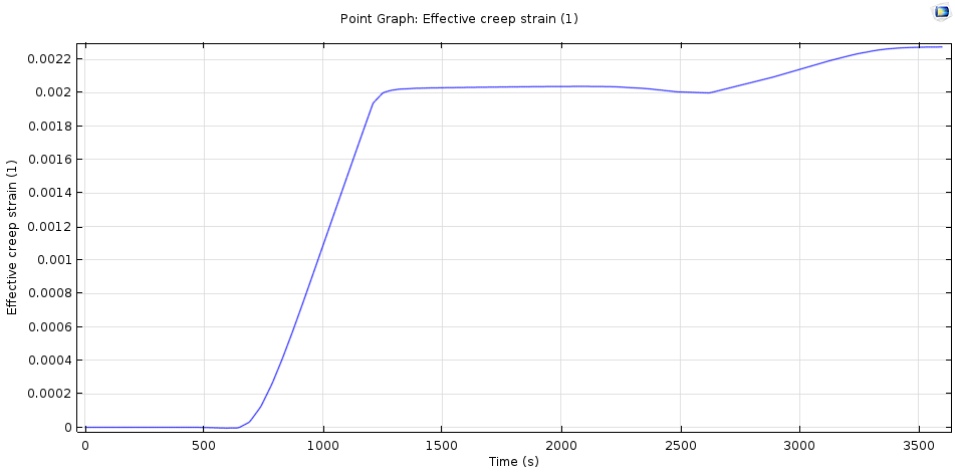

Figure 5.14: Effective creep strain plot for PRD3

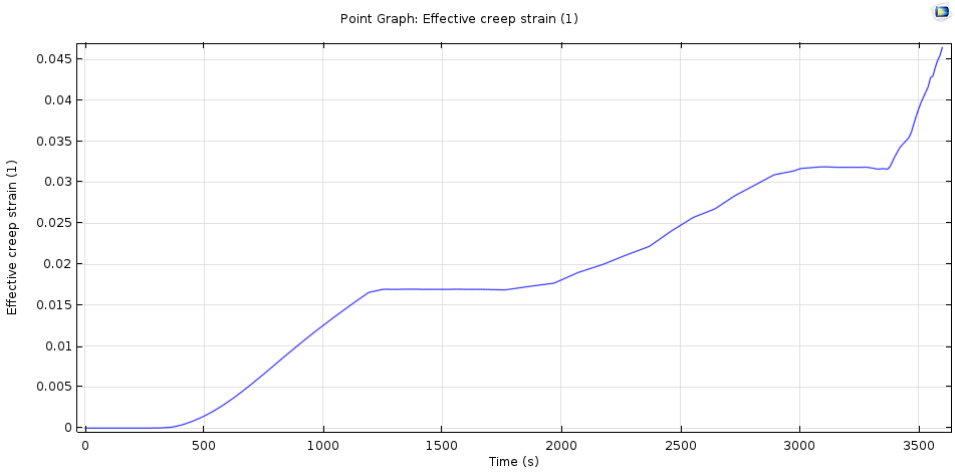

Figure 5.15: Effective creep strain plot for PRD4

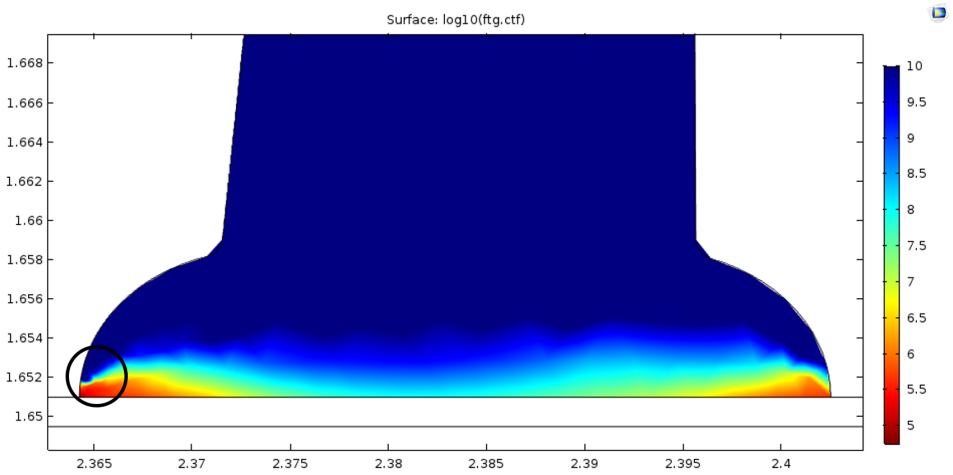

Figure 5.16: PRD3 neck cycles to failure

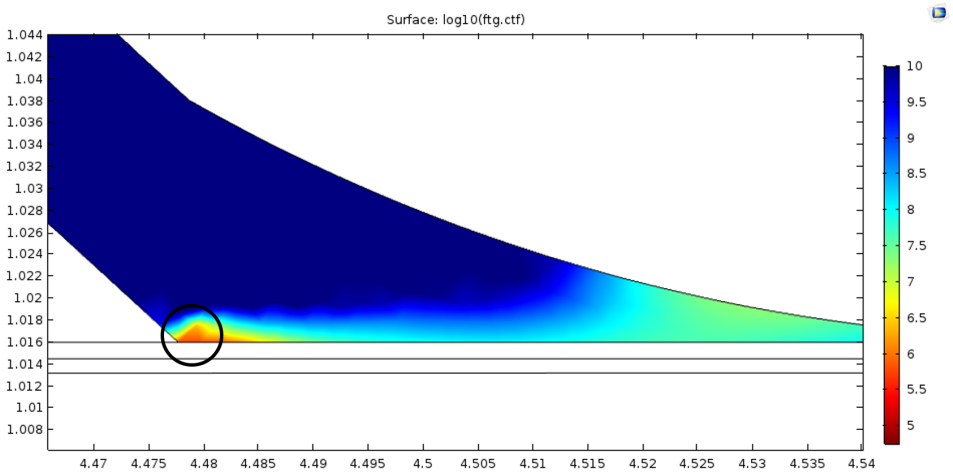

Figure 5.17: PRD3 heel cycles to failure

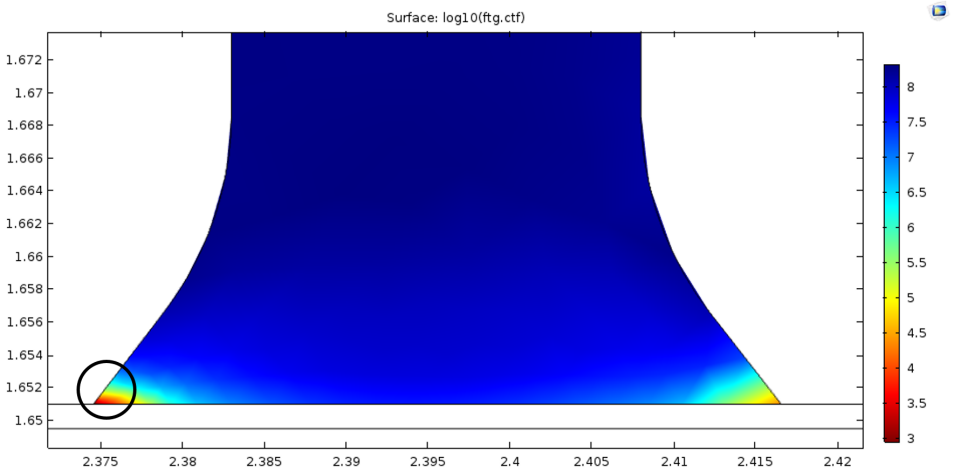

Figure 5.18: PRD4 neck cycles to failure

The cycles to failure observed at the neck and heel of PRD3 and PRD4 are presented in Figures 5.16, 5.17, 5.18 and 5.19. It should be noted that in PRD3, there wasn't any failure observed in the first 10^5 cycles which matches the results provided in [62] that within the first 10^5 cycles no specimens failed.

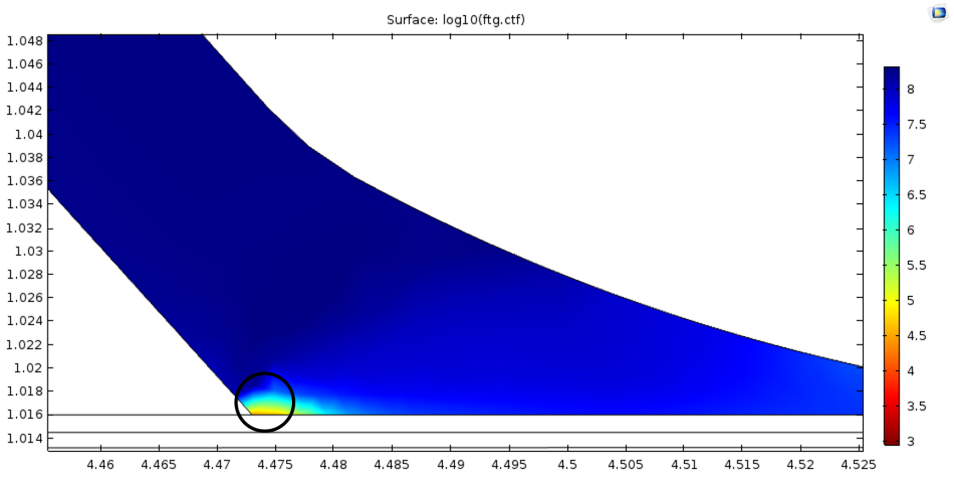

Figure 5.19: PRD4 neck cycles to failure

Meanwhile, for PRD4, there seems to be a possibility of failure before 10^5 cycles which is the influence of the loop geometry i.e. when the loop height is high, the wirebond's neck (HAZ) becomes a critical area for fatigue.

5.3.2. Stresses with Silicone encapsulant

One set of wirebond samples are now filled with Silicone encapsulant and simulated by thermal cycling just like in section 5.3.1. But, the time period for which the models were simulated is 600s. This is done to observe the stress that accumulated with time, that would eventually lead to failure. The colour legends give a reference to the amount of stress through the wire. Figures 5.20, 5.21, 5.22 and 5.23 show the neck and heel stresses observed for PRD3 and PRD4 respectively.

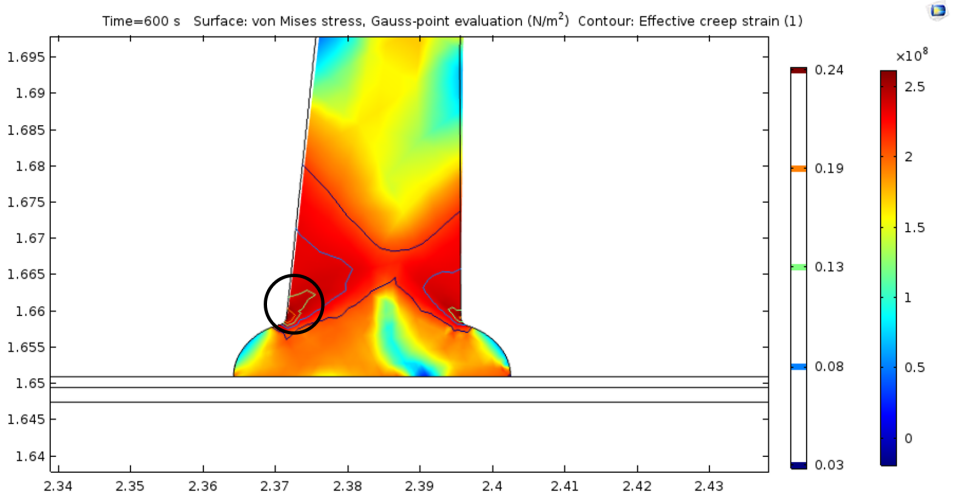

Figure 5.20: PRD3 neck stress with Silicone as encapsulant

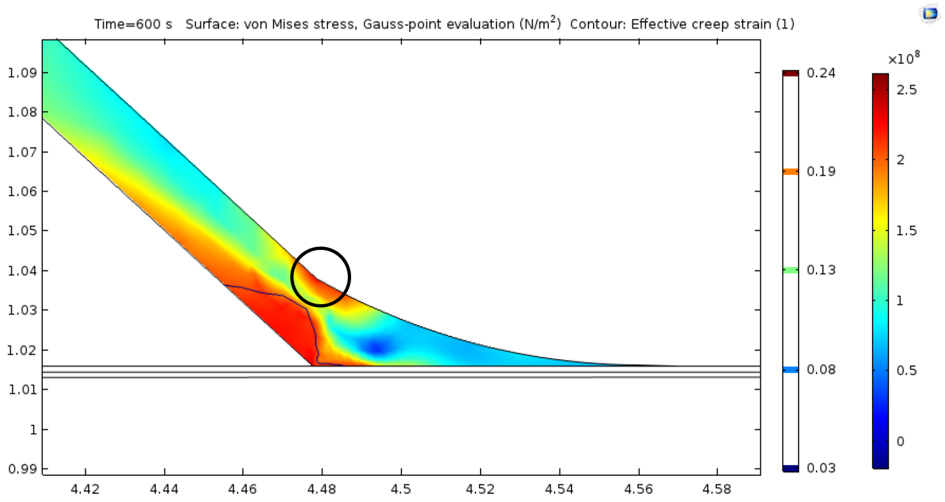

Figure 5.21: PRD3 heel stress with Silicone as encapsulant

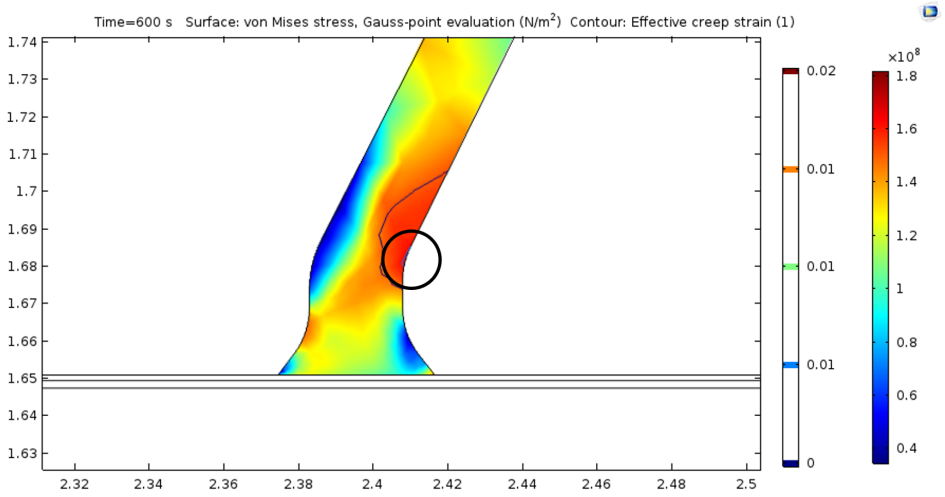

Figure 5.22: PRD4 neck stress with Silicone as encapsulant

Table 5.7: Stress comparison between Silicone encapsulated PRD3 and PRD4 w.r.t time and critical areas

Sample with silicone	**Stress (MPa)**			
	t=500s		t=600s	
	Neck	Heel	Neck	Heel
PRD3	206	188	234	216
PRD4	158	168	163	145

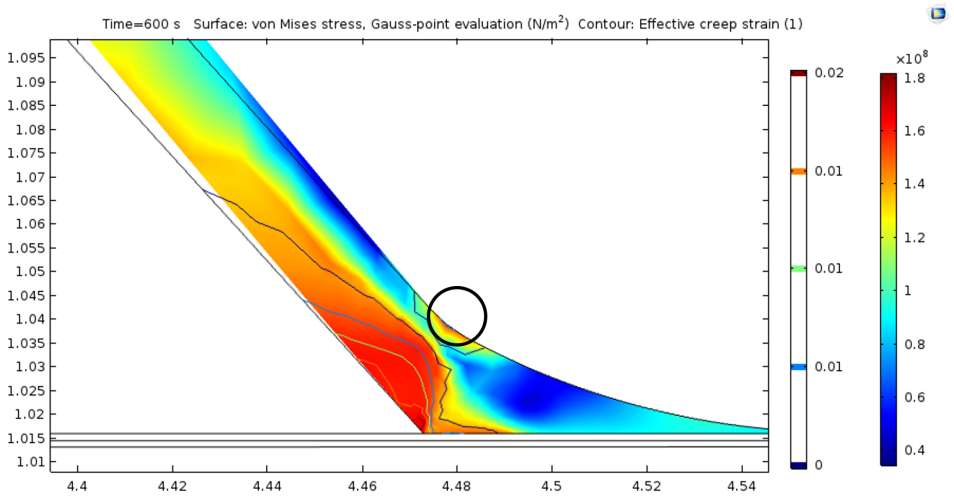

Figure 5.23: PRD4 heel stress with Silicone as encapsulant

Table 5.7 compares the stresses for PRD3 and PRD4 which have a loop height of 200μm and 400μm respectively at critical locations of the neck and the heel based on where the failure may occur as known from the literature survey.

Here, it is noticed that the simulation results have a higher scaling for stress values. Also, when Silicone is added to the model, the heel stress increases; indicating that the Silicone adds force to this area predominantly.

6

CONCLUSIONS AND RECOMMENDATIONS

6.1. Conclusions

The primary focus of this thesis was to understand the physics-of-failure of wirebond interconnects. This has been successful by performing experiments, running simulations, and performing tests.

The outcomes match with the research questions that were initially formed. The conclusions of this thesis are:

- The ultimate tensile strength of gold used in the pull-test is 250MPa; and the 2D COMSOL™ modelling is validated as the simulation provides matching stress results.
- One of the outcomes of this thesis includes a working experimental approach to detect crack growth in wirebonds using accurate resistance methods. Because of this resistance method, it is concluded that when a significant increase in resistance is reported, wirebond fatigue is imminent.
- When the stress results are compared between wirebond samples without Silicone and samples with Silicone, it is observed that the heel stress increases in the latter as Silicone adds forces to this area predominantly. This is further observed by a higher scaling in the stress plots.
- Finally, it is observed that in the wirebond samples without Silicone, during thermal cycling, the neck area experiences more forces than the heel area.

6.2. Recommendations

Future recommendations of this research include:

6.2.1. Design recommendations

- Optimize the loop heights to reduce the stresses to failure.
- Optimize the loop radius to reduce the stresses to failure.

6.2.2. Future work

- Continuation of the tests to a higher number of cycles i.e. more test time.
- Increase in the number of samples that are being tests.
- The understanding of accumulated strain, crack growth and fatigue can improve the reliability of wirebonds.
- Automation of the experimental setup, for data logging.
- Use other materials like Ag-alloy to compare results with Au wirebonds.

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A

DIL 24 pin package details(Spectrum semi)

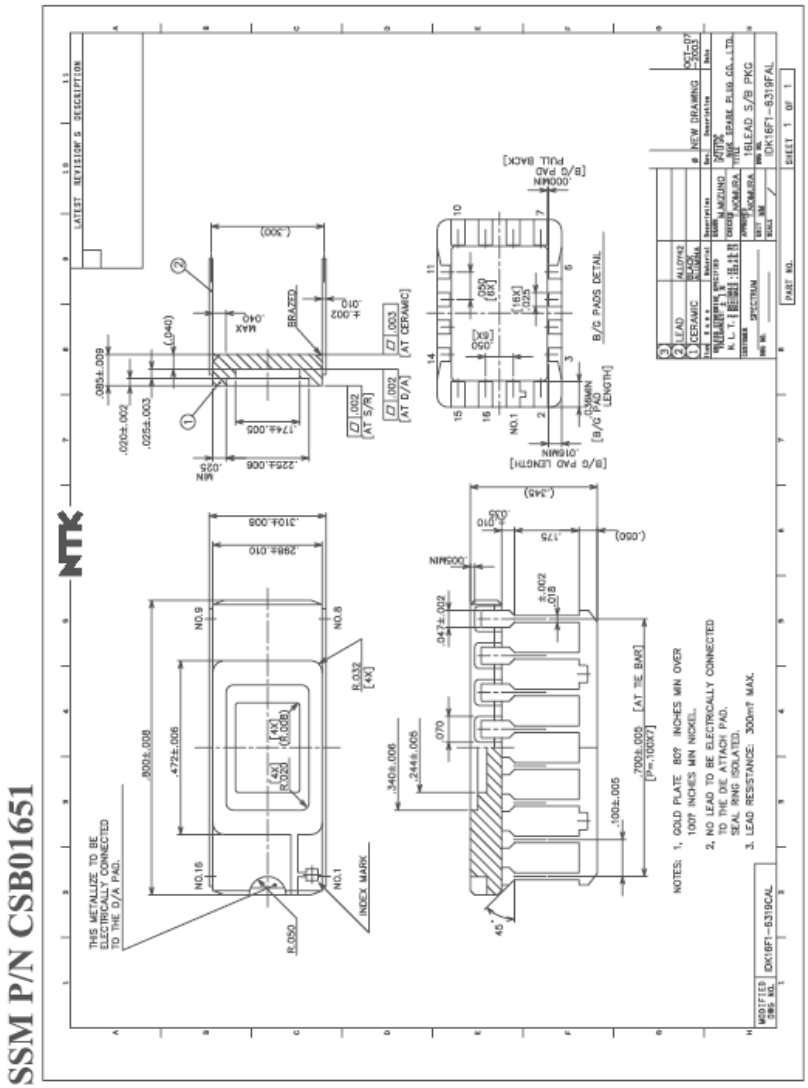

Figure A.1: DIL 24 pin package details

B

Parts of a ball-stitch wirebond

F_{wd} = F_{wt} = tensile force in the wire on the die and on the terminal side of the wire bond, respectively

F = pull force applied by the pulling probe in a pull test or the pull strength of the wire bond

h = height of the apex of the wire loop above the terminal bonding surface

ϵ = hook position

d = diameter of the wire

H = height difference between the die and the terminal bonding surfaces

φ = angle from the normal to the bonding surfaces and in the plane which includes the two bonds, that the probe is pulled in the pull test

Θ = contact angles

$\frac{h}{d}$ = Stand Off ratio

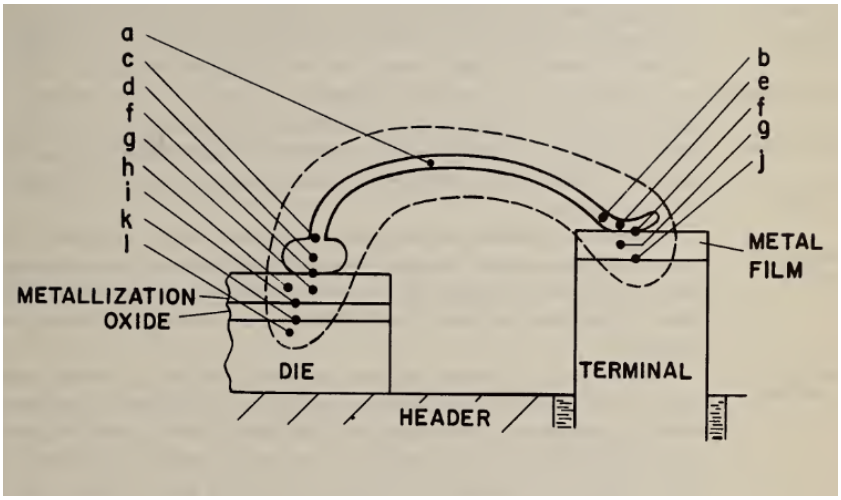

Figure B.1: Sketch of a thermocompression ball-stitch wire bond (enclosed by the dashed line) with the various elements of the wire bond indicated where failure can occur [20]

(a) Wire

(b) Heel of the bond.

(c) Wire emerging out of the top of the wire material melted to form a ball prior to being deformed in the process of making the ball bond.

(d) Wire material melted to form a ball and deformed in the process of making the ball bond.

(e) Wire material deformed in the process of making the bond and located over the bond between the wire and the bonding surface.

(f) Bond interface between the wire and the bonding surface.

(g) Metal-filmed bonding surface. It may be multi-layered.

(h) Metal film (metallization) at the perimeter of the bond interface.

(i) Interface between the metal-film bonding surface and an underlying insulating layer, usually a silicon oxide.

(j) Interface between the metal-film bonding surface and the terminal.

(k) Interface between the insulating layer and the silicon substrate.

(l) Silicon substrate.

C

Samples PRD1 and PRD2

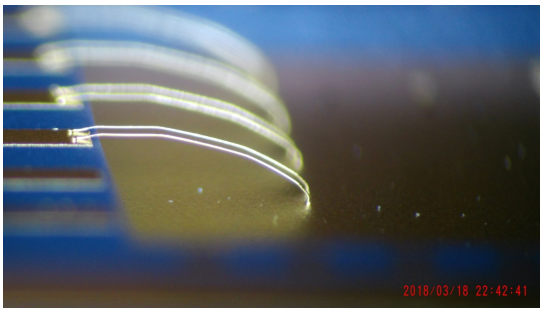

Figure C.1: Left sample PRD1

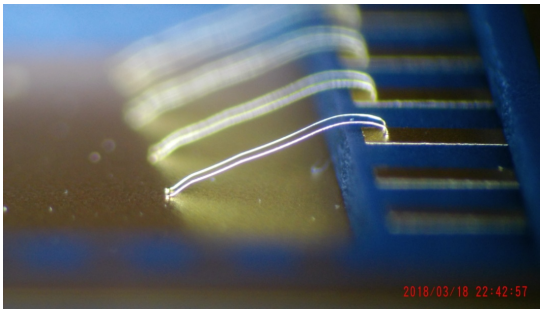

Figure C.2: Right sample PRD1

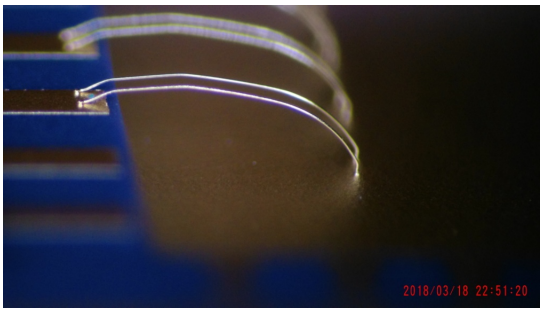

Figure C.3: Left sample PRD2

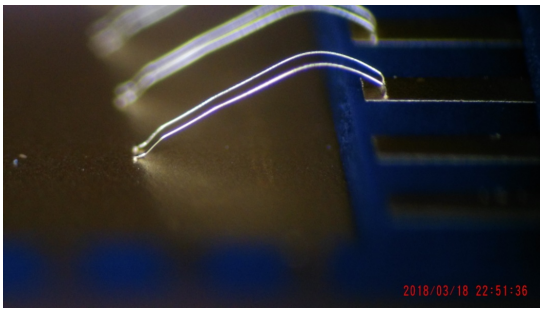

Figure C.4: Right sample PRD2

D

Pull test results of PRD1 and PRD2

Table D.1: Pull forces for PRD1

	Left Wire pull [cN]	Right Wire pull [cN]
PRD1	7.922	8.358
PRD1	7.762	8.089
PRD1	7.892	8.312
PRD1	7.924	7.762
PRD1	8.271	8.379
PRD1	8.096	7.523
PRD1	8.369	8.872
PRD1	8.670	8.759

Table D.2: Pull forces for PRD2

	Left Wire pull [cN]	Right Wire pull [cN]
PRD2	7.264	6.055
PRD2	7.138	6.546
PRD2	6.828	7.030
PRD2	7.106	6.438
PRD2	7.438	6.364
PRD2	6.364	6.690
PRD2	7.654	7.927
PRD2	8.459	6.388

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