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Radio-Frequency Reflectometry in Silicon-Based Quantum Dots

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Radio-frequency (rf) reflectometry offers a fast and sensitive method for charge sensing and spin readout in gated quantum dots. We focus in this work on the implementation of rf readout in accumulation-mode gate-defined quantum dots, where the large parasitic capacitance poses a challenge. We describe and test two methods for mitigating the effect of the parasitic capacitance, one by on-chip modifications and a second by off-chip changes. We demonstrate that on-chip modifications enable high-performance charge readout in Si/Si_xGe_{1-x} quantum dots, achieving a fidelity of 99.9% for a measurement time of 1 μs.

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I. INTRODUCTION

Quantum computing promises a significant speedup of computational tasks that are practically impossible to solve on conventional computers [1–4]. Of the physical platforms available, spin-based quantum bits (qubits) in semiconductors are particularly promising [5,6]. Single-qubit gates with fidelities above 99.9% [7] and two-qubit gate fidelities up to 98% [8,9] have been demonstrated. Spin qubits in silicon are considered a strong candidate for realizing a large-scale quantum processor due to the small qubit dimensions, the localized nature of the control, the CMOS compatibility, the long coherence times [10], and the possibility of operating beyond 1 K [11,12].

Charge sensing is an important technique for measuring spin qubits, as their long-lived spin states can be converted into detectable charge states [13,14]. To detect a charge state, a sensing dot (SD) is placed in close proximity ($d <\sim 300$ nm) to the qubit, as shown in Fig. 1(a). The resistance of the SD is strongly dependent on the charge state. However, measuring this resistance in dc with an amplifier at room temperature requires an integration time on the order of 30 μs–1 ms, due to the presence of noise and the *RC* time constant from the line capacitance and the amplifier input impedance [11,13]. This slow readout forms a bottleneck when performing spin-qubit experiments, since initialization and manipulation can be performed on the nanosecond or microsecond scale [15–17].

Radio-frequency (rf) reflectometry [18] has been successfully applied to depletion-mode GaAs quantum dots and has enabled single-shot readout with only a few microseconds of integration time [19]. However, in accumulation-mode devices, the large parasitic capacitance of the accumulation gates to the two-dimensional electron gas (2DEG) below provides a low-impedance leakage pathway to ground for the rf signal, complicating rf-reflectometry measurements. Previous works have addressed this problem by the use of circuit-board elements [20] and careful gate design [21,22].

In this work, we further develop the theoretical model of the leakage pathway introduced by this parasitic capacitance and apply it to two methods of circumventing the impact of the parasitic capacitance. We first apply this model in the "Ohmic-style" implementation, similar to GaAs, where the signal is sent through an Ohmic contact. For this approach, we mitigate the effects of the capacitance by optimizing the on-board elements and the device design. Second, we present the "split-gate style," where the rf signal is carried by a gate that is capacitively coupled to the 2DEG [20]. By an adaptation of the sample design, the leakage pathway to the Ohmic contact is blocked by a highly resistive channel.

II. RADIO-FREQUENCY REFLECTOMETRY

When performing rf readout, a fixed frequency signal is applied to a SD [Fig. 1(c)]. The reflectance of the applied

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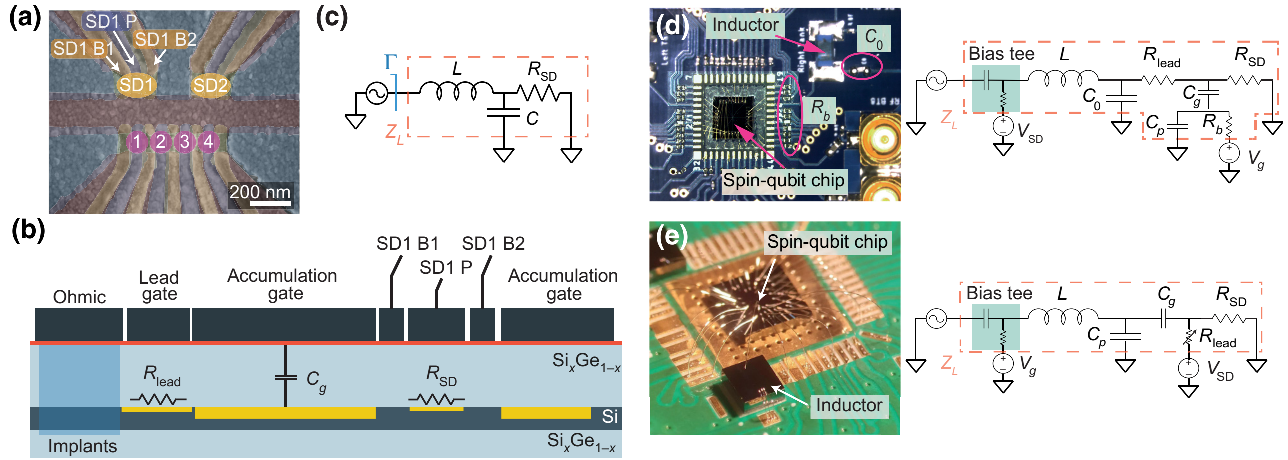

FIG. 1. (a) A false-colored SEM image of a Si/Si_xGe_{1-x} device, similar to the one used in this work. (b) A schematic cross section of the sample, showing the Si/Si_xGe_{1-x} quantum well and the gate stack on top. The yellow regions indicate a finite electron density in the quantum well. The three gates SD1 are used as plunger and barrier gates of the SD, with resistance R_{SD}. The accumulation gate induces a 2DEG connecting the quantum dot to the Ohmic contact, via a smaller area controlled by the lead gate. We use the lead gate to set the resistance R_{lead}. The path between the bond wire to the Ohmic contact and the quantum dot also contains a contact resistance and the resistance of the 2DEG below the accumulation gate, both of which we absorb into R_{lead}, for simplicity. The capacitance between the 2DEG and the gates is dominated by C_g. (c) The circuit diagram, showing an *LCR* circuit containing R_{SD}. (d) An optical image (left) and the circuit diagram (right) of the wire-bonded sample on the printed circuit board (PCB) used for the Ohmic approach. The rf signal is applied to the Ohmic contact. C_0 is a capacitor on the PCB. The R_b are resistors on the PCB to prevent leakage of the rf signal into the dc lines (e.g., the accumulation-gate electrode). The bias tee ($R = 5$ kΩ, $C = 100$ nF) is implemented on the PCB to combine dc (V_{SD}) and rf signals. C_p is the parasitic capacitance of the bond wire and accumulation gate to the ground plane of the PCB. (e) An optical image (left) and the circuit diagram (right) of a wire-bonded sample and inductors on the PCB used for the split-gate approach. The rf signal is applied to the accumulation gate.

signal is measured. It can be expressed as

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0), \tag{1}$$

where here Z_L represents the load impedance of the entire circuit (including matching networks and bias tees, as applicable) and Z_0 is the input impedance, equal to the output impedance of the rf source ($Z_0 = 50$ Ω). A maximal power transfer occurs when $\Gamma = 0$, which is called the matching condition ($Z_0 \approx Z_L$). Given the resistive load from the SD, R_{SD}, we can reach a matching condition by adding a matching network consisting of an inductor and a capacitor, as in Fig. 1(c) [19]. The impedance of this *LCR* circuit is given by

$$Z_L = i2\pi fL + \frac{1}{(1/R_{SD}) + i2\pi fC}. \tag{2}$$

For this simple *LCR* network, matching occurs when $f_{res} = 1/(2\pi\sqrt{LC_0})$ and $R_{SD} = L/C_0Z_0$. In general, we denote the frequency and SD resistance for the matching condition as f_M and R_M throughout. Ideally, matching occurs where R_M is reached at the flank of the SD Coulomb-blockade peak, where the SD resistance is most sensitive to the charge occupation of the qubit dot, typically in the range of 50–500 kΩ.

In Si/Si_xGe_{1-x} quantum dots, the large parasitic capacitance from the 2DEG to the accumulation gate [C_g in Fig. 1(b)] makes it hard to find a practical matching condition. The large C_g (approximately 1 pF) can be compensated by increasing the inductance of the inductor but this causes the resonance frequency to drop to a regime where most cryogenic amplifiers do not perform well (below 50–100 MHz). We solve these problems by slightly altering the circuit. We consider two approaches, which we explain in more detail below:

(a) The Ohmic approach—the rf signal is sent through the Ohmic contact. The effect of C_g is mitigated by optimizing the circuit board and sample design [Fig. 1(d)].

(b) The split-gate approach—the accumulation gate is split into two parts. The rf signal is carried to the SD using the large C_g between the accumulation gate and the 2DEG below [Figs. 1(b) and 1(e)]. The lead gate (R_{lead}) is used to create a high-impedance path to the Ohmic.

These two approaches are tested on quadruple quantum dot devices on a Si/Si_xGe_{1-x} heterostructure. Figure 1(a) shows a SEM image of a typical device. Four quantum dots are formed with the lower set of gates of the device and two sensors are formed with the upper set of gates. Large accumulation gates control the electron density from

the quantum dots to the Ohmic contacts, approximately 50 μm away.

III. OHMIC APPROACH

The Ohmic approach is shown in Fig. 1(d) and introduces the rf signal to the lead of the SD through the Ohmic contact. The large C_g and R_{lead} prohibit application of the simple *RLC* model to accumulation-mode $\text{Si}_x\text{Ge}_{1-x}$ devices. The gates are connected to ground by two channels: the line resistance R_b to the input lines for the gate voltages V_g, which serves as rf ground, and the parasitic capacitance C_p to ground from all the metal on the sample side of R_b (gate, bond wire, bond pad, PCB trace). We will begin by exploring how the tank-circuit parameters (R_b, C_p, C_0, and L) and the device parameters (R_{lead} and C_g) affect the matching conditions (f_M and R_M). This understanding will then be applied to demonstrate several key strategies that allow for Ohmic-style rf reflectometry in $\text{Si}/\text{Si}_x\text{Ge}_{1-x}$ accumulation-mode devices. The goal is to achieve R_M and f_M values that are experimentally achievable and to ensure that the majority of the power is dissipated in R_{SD}, resulting in a usable signal-to-noise ratio (SNR). For that, we aim at a $R_M \sim 50$–500 kΩ and $f_M \sim 100$–300 MHz.

A. Prevent shunting to ground through C_g

The rf signal in the lead 2DEG has a low impedance path to the accumulation gates through C_g [20]. In order to block this pathway, we design the printed circuit board (PCB) to have surface-mount resistors to increase R_b between the sample bond pads and input lines for gate voltages V_g. C_p is in parallel to R_b and limits the ability to decrease the impact of C_g by just increasing R_b. We place the blocking resistors close to the bond pads to minimize the amount of metal on the sample side and thereby reduce C_p. In the end, we find a minimum $C_p = 0.2$ pF. At $f > 10$ MHz, this would be a leakage path with a resistance smaller than 80 kΩ. The role of C_g, R_b, and C_p together can be represented by one effective gate capacitor $C_g^* = C_pC_g/(C_p + C_g) = 0.2$ pF for any $R_b > 100$ kΩ at our target frequency range, because C_p is the more dominant leak channel compared to R_b.

B. Solution of lumped-element model

The simple *LCR* model always has a physically meaningful solution of f_M and R_M for the impedance-matching condition. However, device simulations and experiments demonstrate that large values of R_{lead} and C_g^* can prevent there being a R_M and f_M and therefore the ability to use the tank circuit for charge detection. In Fig. 2, we explore the dependence of the matching conditions on C_0, L, C_g^*, and R_{lead}. Simulations are performed by solving for R_{SD} and f such that the circuit impedance Z matches $Z_0 = 50$ Ω, giving R_M and f_M, respectively. The constraints that f_M is real and that R_M is real and positive result in there being conditions where no matching can be achieved, which are shown as white regions in Figs. 2(a)–2(d).

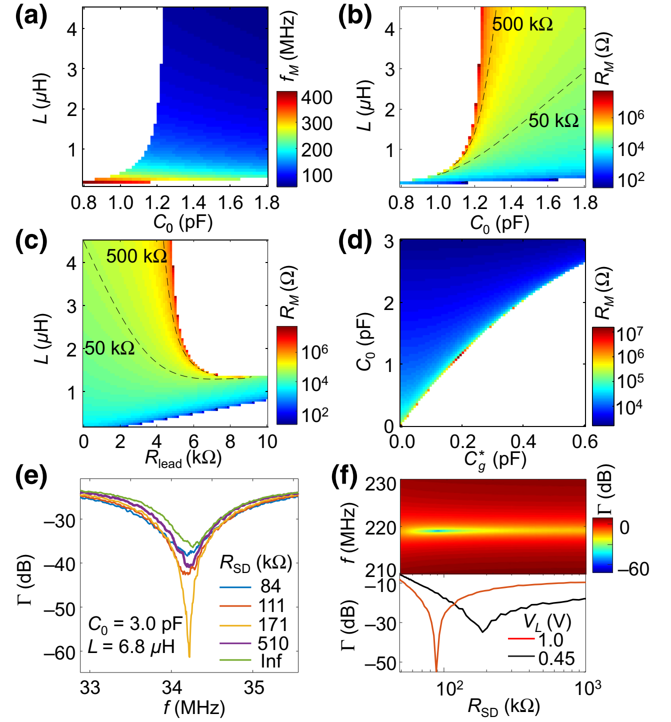

FIG. 2. (a),(b) Simulations of f_M and R_M as a function of C_0 and L with fixed parameters of $C_g^* = 0.2$ pF and $R_{\text{lead}} = 3$ kΩ. The white regions are where no matching can be achieved. (c) A simulation of R_M as a function of R_{lead} and L with fixed $C_g^* = 0.2$ pF, and $C_0 = 1.6$ pF. (d) A simulation of R_M as a function of C_0 and C_g^* with $L = 1$ μH and $R_{\text{lead}} = 3$ kΩ. (e) An experimental demonstration of best matching with $f_M = 34$ MHz and $R_M = 170$ kΩ. (f) The upper panel shows Γ measured as a function of R_{SD} and f for an optimized device and circuit board, while the lower panel shows Γ at f_M (red and black) as a function of R_{SD} when $V_L = 1$ V, 0.45 V, respectively.

C. Control matching with C_0 and L

When a sample is fabricated, C_g and R_{lead} are roughly fixed, meaning that the only way to change R_M and f_M is through the tank-circuit parameters L and C_0. We present solutions of f_M in Fig. 2(a) and R_M in Fig. 2(b) as a function of L and C_0, with $C_g^* = 0.2$ pF and $R_{\text{lead}} = 3$ kΩ. We note that far from the nonmatching regions, the behavior is approximately that of the standard *LCR* model. Under these conditions, $C_0 \gg C_g$, which means that C_0 dominates the capacitance of the loaded tank circuit. When C_0 is comparable to or smaller than C_g^*, R_M diverges.

In order to tune C_0 and L, our PCB is designed with solder pads for a surface-mount inductor, L, and a surface-mount capacitor to control C_0. The board

parasitic capacitance also provides a significant contribution (approximately 1 pF) to C_0 and sets a lower bound for possible values of C_0. The ground plane near the tank circuit should be minimized to reduce this board parasitic capacitance, ensuring the tunability of the tank circuit by C_0 and L. Following the prediction of the model, we test lumped elements with $L = 6.8\ \mu$H and $C_0 = 3.0$ pF for a device with an estimated $R_{\mathrm{lead}} = 4$ kΩ and $C_g = 0.5$ pF ($C_g^* = 0.2$ pF). The result in Fig. 2(e) demonstrates impedance-matching behavior with a usable R_M. However, it comes at the cost of a very low and unusable f_M. In practice, we need C_0 to be as low as allowed by C_g^* to guarantee a f_M that is above 100 MHz. For this reason, it is important to reduce C_g and thus C_g^*.

D. Balancing C_g and R_{lead} in sample design

The dependence of the matching conditions is strongly dependent on R_{lead}, as shown in Fig. 2(c). At $R_{\mathrm{lead}} = 0$, the model is reduced to the standard *LCR* model with an effective $C_0^* = C_0 + C_g$. The range of L that can achieve matching is drastically reduced as R_{lead} increases, since more rf power would be dissipated by R_{lead} before R_{SD}. Reducing R_{lead} is therefore key to achieving rf reflectometry. To capture the impact of C_g, we present a simulation of the dependence of R_M on C_g^* and C_0 in Fig. 2(d). We again observe that matching is only achieved when C_0 is large enough compared to C_g.

The sample design impacts both C_g and R_{lead}, both of which we want to minimize, through the length l and width w of the accumulation gate. The knowledge that $C_g \propto lw$ and $R_{\mathrm{lead}} \propto l/w$ reveals that decreasing l is ideal for both parameters, while decreasing w to improve C_g comes at the cost of increasing R_{lead}, and vice versa. We find that $w = 5\ \mu$m is sufficient to achieve consistent accumulation for usable R_{lead} without increasing C_g drastically. In the future, we will place the Ohmics as close to the SD as possible to limit l as in Ref. [21]. The optimized result is demonstrated in Fig. 2(f), where we plot the reflected power Γ in the upper panel as a function of f and R_{SD}. We apply $V_L = 1$ V on the lead gate to fully turn it on and thus minimize R_{lead}. With this, we achieve both a usable $R_M \sim 100$ kΩ and $f_M = 220$ MHz.

E. Tuning R_{lead}

To experimentally confirm the dependence of R_M on R_{lead}, we make use of the lead gate. When V_L is small, the lead gate is partially turned on and thus leads to a larger R_{lead}. The lower panel in Fig. 2(f) shows Γ at f_M as a function of R_{SD} when $V_L = 1$ V and 0.45 V. The best matching is achieved with 67 kΩ for the minimized R_{lead} and 200 kΩ for a larger R_{lead}, which agrees with the simulation in Fig. 2(c). This tunability also allows the use of fixed C_0 and L for general devices, as the matching condition of the device can be tuned *in situ*. This tunability, however, is not ideal, since the larger R_{lead} gets, more energy is lost before the sensor dot, resulting in a reduced SNR.

IV. SPLIT-GATE APPROACH

In this approach, the rf signal is sent to the SD via the accumulation gate instead of via the Ohmic contact [Fig. 1(b)] [20]. The capacitance C_g between the accumulation gate and the 2DEG allows the rf signal to couple in to the 2DEG, as shown in Fig. 1(e). The lead gate is used to generate a high-impedance channel to the Ohmic contact, preventing leakage of the rf signal.

We aim for similar design specifications for this method as for the Ohmic method: a matching resistance (R_M) ranging from 200 kΩ to 600 kΩ and a matching frequency (f_M) larger than 100 MHz. We simulate f_M and R_M for different circuit configurations. We estimate C_g to be 280 fF from the sample design and $R_{\mathrm{lead}} = 10$ MΩ. We vary the parasitic capacitance C_p (from the bond wires and the accumulation gate to the ground plane of the PCB) and the inductance L, as these are parameters that are controllable by the device design and inductor choice. From the simulation results in Fig. 3, we find a large parameter space that achieves the desired matching condition for practical values of L up to about 5 μH as long as $C_p < 0.3$ pF. In this case, the circuit reduces to the standard *LCR* model [23], given that the reactance of C_g, $\chi_g = (1/2\pi f C_g) \ll R_{\mathrm{SD}}$ and $R_{\mathrm{lead}} \gg R_{\mathrm{SD}}$ [see Fig. 1(e)]. We also simulate the expected measurement bandwidth at the matching condition of this circuit. We only see a weak dependence of the bandwidth on L and C_p. The bandwidth of the circuit ranges from 0.5 to 1 MHz.

For the devices used to demonstrate the split-accumulation-gate approach, we estimate by simulation the total parasitic capacitance to be around $C_p \sim 250$ fF. The parasitic capacitance is kept low using a compact gate layout and high-kinetic-inductance resonators as inductors [24]. We aim for an inductor value of $L \sim 3.4\ \mu$H, which

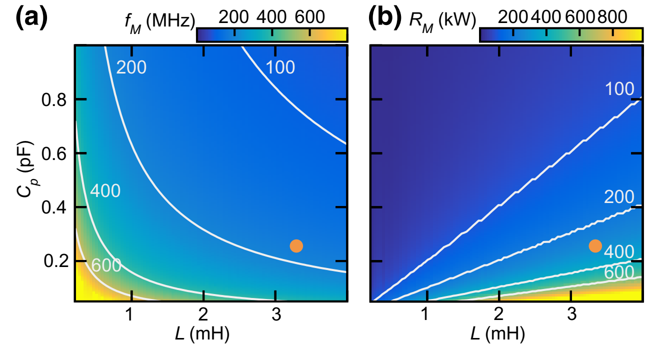

FIG. 3. Simulation results for (a) f_M and (b) R_M as a function of C_p and L for the split-accumulation-gate circuit when $R_{\mathrm{lead}} = 10$ MΩ and $C_g = 280$ fF. The orange dot indicates the parameters for the device and circuit used in the experiment.

is expected to lead to a resonance frequency of approximately 180 MHz and a matching resistance of 300 kΩ for the SD. When operating the device, leakage to the Ohmic contact is cut off by tuning R_{Lead} above 10 MΩ.

Figure 4(a) shows the response of the resonator versus the frequency for several values of R_{SD}. We see that f_M is slightly below 170 MHz. In Fig. 4(b), we find $R_M = 275$ kΩ. The circuit bandwidth can be extracted from the full width at half maximum (FWHM) of the resonance line. For R_{SD} equal to R_M, the bandwidth is 0.8 MHz, which means that we can measure signals up to time scales as short as approximately 600 ns, provided that the SNR is sufficiently high. Two sensitive regions where the reflected signal depends strongly on R_{SD} are visible in Fig. 4(b), as indicated by the red and green shaded areas. The inset shows the expected response of the circuit in the I-Q plane around R_M. The red and green regions can be differentiated by a phase π in the measured signal. In practice, the coax line between the sample and the measurement circuit adds an unknown phase. In order to maximize the SNR, we record both I and Q and convert the result to a scalar.

In practice, we find that the resistance range for R_{SD} that gives the largest charge sensing signal is roughly 0.4–1.0 MΩ, just above $R_M = 275$ kΩ. This implies that we can improve the SNR by a factor of 2 by matching within this range (e.g., 600 kΩ). This can be done by reducing C_p from 250 fF to 150 fF (smaller gate footprint) or by increasing the inductance L (see Fig. 3).

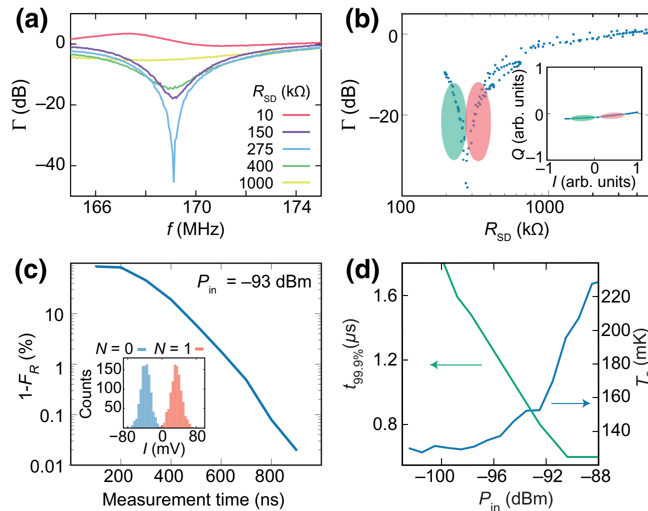

FIG. 4. The characteristics obtained with the split-accumulation-gate approach. (a) The measured reflection coefficient as a function of f for several values of R_{SD}. (b) The reflection coefficient Γ at f_M as a function of R_{SD}. $R_M = 275$ kΩ. The sensitive regions are marked in red and green, respectively. The inset plots the theoretical response in the I-Q plane. (c) The infidelity of charge detection versus measurement time for an interdot transition. The inset shows an example histogram for calculating the fidelity. (d) $t_{99.9\%}$ and T_e as a function of P_{in}.

To characterize the readout performance experimentally, we measure the charge-readout fidelity (F_R). This fidelity is defined as the probability of correctly determining whether a quantum dot is occupied with no ($N = 0$) or one ($N = 1$) electron. To estimate F_R, we send a train of 10 000 square pulses to the target quantum dot. The dot-reservoir tunnel time is several orders of magnitude shorter than the periods used in the experiment, which means that the quantum dot charge state tracks the square pulse. We sample the I-Q signal for each half period of the square pulse and plot the distribution for both half periods as shown in the inset of Fig. 4(c). The overlap of the two signals is the reported infidelity ($1 - F_R$). For these measurements, we use a digital filter (finite impulse response type) with a pass band between 100 kHz and 2.5 MHz. The lower frequency of the pass band is determined by the slowest signal that we want to detect (5 μs in this case). The upper frequency is taken to be larger than the bandwidth of the matching circuit, so as not to limit the measurement speed.

Figure 4(c) plots the readout infidelity $1 - F_R$ versus the measurement time when we apply an input signal power (P_{in}) of −93 dBm to the readout circuit (estimated from the output power at the source and the specified losses of the transmission line). We find a minimum measurement time of $t_{99.9\%} = 780$ ns in order to achieve $F_R > 99.9\%$. We see that $t_{99.9\%}$ strongly depends on the input power of the rf-readout circuit [Fig. 4(d)]. The SNR is improved by larger P_{in} until the bandwidth limit of the circuit is reached (0.8 MHz). On the other hand, larger P_{in} also affects the effective electron temperature of the quantum dots. To characterize the trade-off, we measure T_e by measuring the polarization line of an interdot transition [25] and plot the result as a function of P_{in} in Fig. 4(d). We note that T_e starts to increase dramatically once $P_{\text{in}} > -93$ dBm. We recommend that power should only be supplied to the rf-readout circuit while the readout is being done, to prevent the readout from affecting the qubit operations.

V. CONCLUSION

In this work, we demonstrate two methods that can be used to achieve a reasonable matching condition for rf-reflectometry measurements in accumulation-mode devices. For the Ohmic method, we demonstrate that a series resistance can be used to reduce leakage through the parasitic capacitance. Additionally, a careful sample design is necessary in order to obtain both a workable frequency and matching resistance. With further design changes, such as moving the Ohmic contact closer to the quantum dot and drastically reducing the accumulation-gate capacitance, the Ohmic method can perform as well as the split-accumulation-gate method [21,22]. For the split-accumulation-gate method, the rf source is directed to the accumulation gate of the SD and the addition of

the lead gate allows us to efficiently cut off the leakage path to the Ohmic contact. The charge state of a qubit dot can be read out within 1 μs with a $> 99.9\%$ fidelity, which matches the state-of-the-art readout performance. The split-accumulation-gate method is useful when it is difficult to achieve a very low C_g and/or to keep R_{2DEG} sufficiently low.

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