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## REVIEW ARTICLE OPEN

## Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent

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Semiconductor spins are one of the few qubit realizations that remain a serious candidate for the implementation of large-scale quantum circuits. Excellent scalability is often argued for spin qubits defined by lithography and controlled via electrical signals, based on the success of conventional semiconductor integrated circuits. However, the wiring and interconnect requirements for quantum circuits are completely different from those for classical circuits, as individual direct current, pulsed and in some cases microwave control signals need to be routed from external sources to every qubit. This is further complicated by the requirement that these spin qubits currently operate at temperatures below 100 mK. Here, we review several strategies that are considered to address this crucial challenge in scaling quantum circuits based on electron spin qubits. Key assets of spin qubits include the potential to operate at 1 to 4 K, the high density of quantum dots or donors combined with possibilities to space them apart as needed, the extremely long-spin coherence times, and the rich options for integration with classical electronics based on the same technology.

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## INTRODUCTION

The quantum devices in which quantum bits are stored and processed will form the lowest layer of a complex multi-layer system.<sup>1–3</sup> The system also includes classical electronics to measure and control the qubits, and a conventional computer to control and program these electronics. Increasingly, some of the important challenges involved in these intermediate layers and how they interact have become clear, and there is a strong need for forming a picture of how these challenges can be addressed.

Focusing on the interface between the two lowest layers of a quantum computer, each of the quantum bits must receive a long sequence of externally generated control signals that translate to the steps in the computation. Furthermore, given the fragile nature of quantum states, large numbers of quantum bits must be read out periodically to check whether errors occurred along the way, and to correct them.<sup>4</sup> Such error correction is possible provided the probability of error per operation is below the accuracy threshold, which is around 1% for the so-called surface code, a scheme which can be operated on two-dimensional (2D) qubit arrays with nearest-neighbor couplings.<sup>5, 6</sup> The read-out data must be processed rapidly and fed back to the qubits in the form of control signals. Since each qubit must separately interface with the outside world, the classical control system must scale along with the number of qubits, and so must the interface between qubits and classical control.

The estimated number of physical qubits required for solving relevant problems in quantum chemistry or code breaking is in the  $10^6$ – $10^8$  range, using currently known quantum algorithms and quantum error correction methods.<sup>7, 8</sup> For comparison, state-

of-the-art processors contain more than one billion transistors (<http://www.intel.com/pressroom/kits/quickreffam.htm>). Furthermore, the structure of these transistors bears a lot of resemblance with that of promising semiconductor-based qubits.<sup>9, 10</sup> However, an important difference is that conventional processor chips have only  $\approx 10^3$  input-output connections (IO's), for instance Intel's land grid array 2011 socket has 2011 pins that contact the backside of the processor (<http://www.intel.nl/content/www/nl/nl/processors/core/core-i7-lga-2011-datasheet-vol-1.html>). This brings the transistor-to-IO ratio over  $10^6$ . This scaling of the number of pins with the number of devices is empirically described by Rent's rule.<sup>11, 12</sup> In the absence of multiplexing or on-chip control logic, the limit for the qubit count is probably similar to the pin-limit of the package, which is currently around  $10^3$  (<http://www.intel.nl/content/www/nl/nl/processors/core/core-i7-lga-2011-datasheet-vol-1.html>).

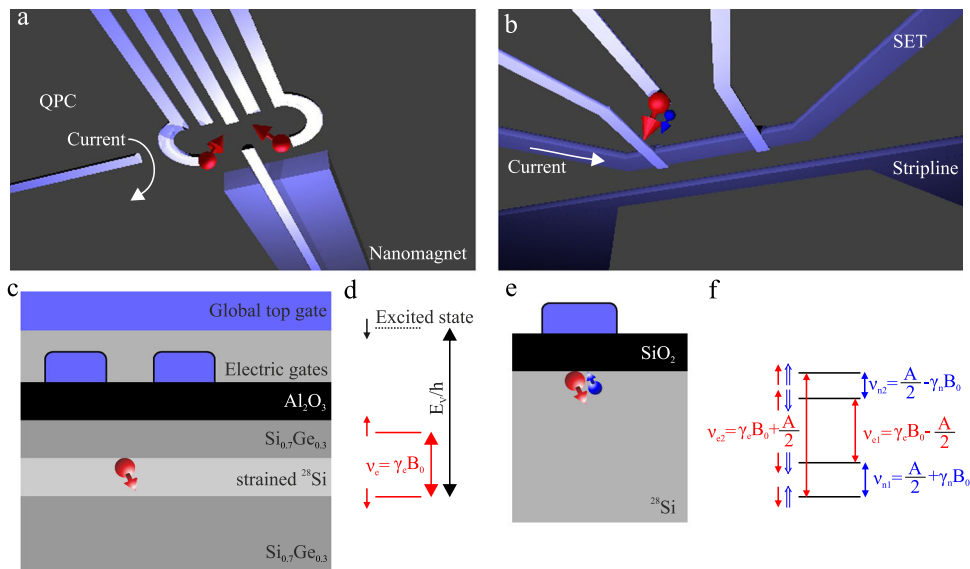
Therefore, the notion that semiconductor quantum bits that are manufactured by complementary-metal-oxide-semiconductor (CMOS)-compatible technology are easily scalable, is too simplistic. While many qubit architectures and strategies for scaling have been proposed,<sup>13–40</sup> a completely worked out pathway to create qubit systems that can be expanded to a large-scale quantum processor yet has to be defined and a key step is the design of a scalable classical-quantum interface.

Here, we focus on the quantum-classical interface requirements and possible solutions for qubits encoded in electron spins in semiconductor quantum dots and donors.<sup>9, 10</sup> We thereby consider specifically quantum dots that are probed and controlled using electrical signals, referring to ref. 1 for a discussion of optically addressed quantum dots. Electrically controlled quantum

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**Fig. 1** Schematic diagram of typical electrically measured spin qubit devices. Red (blue) spins and energy levels refer to electron (nuclear) spins. **a** A double quantum dot device defined in a Si/SiGe quantum well. Quantum dots can be defined either in accumulation mode with a global top gate as depicted in panel **c**, or in depletion mode using a doping layer. **b** Donor qubit system in depletion mode and fabricated by silicon metal-oxide-semiconductor technology (material stack in **e**). The spin states of a single electron are split in a magnetic field and qubit operation is obtained via an ac magnetic field that matches the associated resonance frequency  $\nu_e$  as represented in **d** for dots and **f** for donors. An ac magnetic field can be realized directly by sending an ac current through a strip-line **b**. Alternatively, the motion of a quantum dot due to an ac electric field created by driving a nearby gate results in an effective magnetic field due to the field gradient of a nearby nanomagnet **a**. The donor system forms an effective two-qubit device due to the presence of a nuclear spin, that is coupled to the electron through the hyperfine interaction with strength  $A$ . The gyromagnetic ratio  $\gamma$  of both the quantum dot and donor system are affected by the electric field from the nearby electrostatic gates and nearby charged defects, which causes a non-uniformity between the qubits, but can also be exploited for addressability. For high-fidelity operation it is important that the qubit states are well isolated from excited states. Particularly in silicon quantum dots, a low-energy excited state can appear due to valley degeneracy, which can be lifted in energy via a large vertical electric field.<sup>98</sup> The quantum-point-contact (QPC) or single-electron-transistor (SET) is used to probe the number of charges on the dots. They could potentially be avoided via gate-based dispersive read-out<sup>57</sup>

dots and donors are two promising qubit realizations that have much in common both conceptually and in terms of qubit specifications and hardware requirements. There is significant scope to make these realizations compatible with industrial CMOS technology, which is optimized for high-yield, reproducibility and cleanliness. Indeed, there is a lot of effort in this direction and qubits that are partly fabricated with industrial technology have already been realized.<sup>41</sup>

We begin with a brief summary of electron spin qubits in quantum dots and donors, then derive the control signal requirements and challenges, and next present possible solutions to overcome these challenges. These focus on dense 2D tunnel coupled spin qubit arrays, sparse arrays with coherent links between them, and on the possibility of operating spin qubits at 1 or 4 K, allowing for more complex electronics to be integrated with the qubits.

### ELECTRON SPIN QUBITS IN QUANTUM DOTS OR DONORS

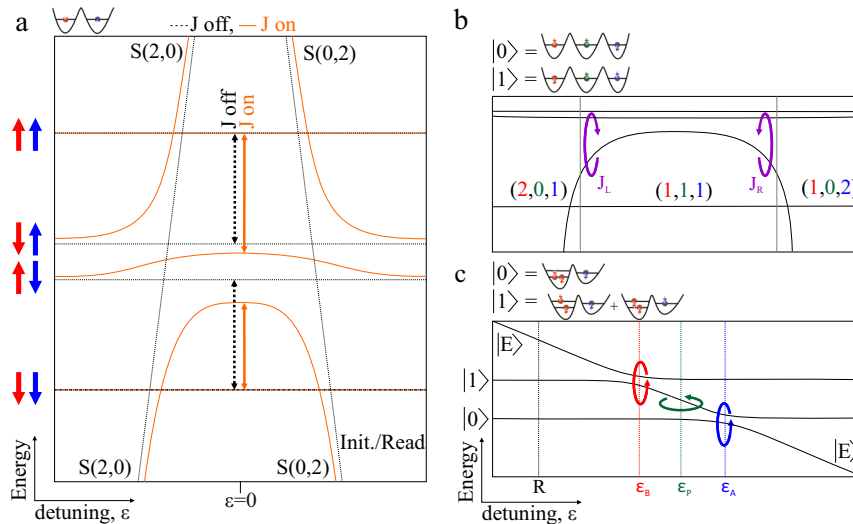
We first briefly introduce electron spin qubits in electrically detected quantum dots and donors as a starting point for discussing the control and interfacing requirements (for more extensive reviews, see refs 9, 10).

A schematic of a prototypical quantum dot device is shown in Fig. 1a. A combination of bandgap offsets and electrostatic gates are used to confine one or more free electrons (or holes<sup>41–43</sup>; for brevity we will refer to electrons throughout the text) in a small space in a semiconductor, typically a few tens of nm in diameter. For qubit experiments, the gate voltages are usually tuned so the quantum dots contain exactly one electron each, although for certain initialization and read-out protocols, an electron is pushed

off a dot or onto a neighboring dot. Figure 1b shows a schematic of a donor-based device. Donor atoms such as phosphorous in silicon have one excess electron compared to the atoms in the surrounding lattice, and at low temperatures this electron is bound to the donor atom (acceptors with one excess hole can be used as well; we will just refer to donors for brevity). With a gate voltage, this electron can be pushed off the donor or a second electron can be bound to the donor, provided the required electric fields are below values that result in population of the silicon conduction band (or valence band in case of acceptors). In both cases, an additional gate can be placed in between or close to adjacent sites in order to control the tunneling of electrons between the sites via a gate voltage, a crucial ingredient of most electron spin qubit proposals.<sup>13, 14</sup> Qubit experiments with such systems have been performed so far with the sample attached to the mixing chamber of a dilution refrigerator, at operating temperatures of 10–100 mK.

The canonical encoding of a qubit in these systems is in the spin split levels,  $|\uparrow\rangle$  and  $|\downarrow\rangle$ , of the electron on each site, in the presence of a static magnetic field.<sup>13, 14</sup> However, alternative encodings have been proposed theoretically and explored experimentally, whereby specific collective spin states of two or three electrons in two or three quantum dots are used to represent  $|0\rangle$  and  $|1\rangle$ , see Fig. 2.<sup>44–48</sup> For each of these encodings, direct current (DC) voltages may be used to fine tune qubit transition frequencies. This is immediate for the encodings based on two or three electron spins, where qubit splittings are directly set by gate voltages. Also for single-spin qubits, the spin splitting is typically sensitive to electric fields.<sup>49–51</sup>

Regardless of the chosen qubit encoding, one generally requires the ability to individually rotate every qubit about two



**Fig. 2** Energy level diagram of spin states in quantum dots. **a** Low-energy spectrum of two uncoupled spins (black dotted line) and coupled spins (orange solid line) in two quantum dots as a function of the detuning energy  $\epsilon$ , the relative energy difference between the *left* and *right* dot levels, which is controlled by the corresponding dot gate voltages. The exchange interaction provided by the charge states with double occupancies  $S(2, 0)$  and  $S(0, 2)$  can be used for two-qubit operations between single spin qubits as the exchange interaction  $J$  modifies the qubit resonance frequencies. While in the uncoupled situation the transition  $|\downarrow\downarrow\rangle$  to  $|\uparrow\uparrow\rangle$  has the same energy as the  $|\downarrow\uparrow\rangle$  to  $|\uparrow\downarrow\rangle$  transition, these become different when exchange is on, allowing to drive rotations of one spin conditional on the state of the other.<sup>75</sup> Alternatively, when briefly turning on the exchange, the two spin states will exchange over time, which also constitutes a two-qubit gate. While many experimental works exploit the detuning to control the exchange amplitude, directly controlling the tunnel coupling allows to operate the system at the so-called symmetry point, where the exchange energy is less sensitive to charge noise, dramatically improving the gate fidelity.<sup>104, 105</sup> The joint state of two coupled spins, for instance the spin singlet and one of the triplet states, can also be used as a single qubit.<sup>65</sup> The advantage of such a qubit is that one qubit axis is electrically controlled and two qubits can be coupled capacitively.<sup>23</sup> For universal control, a magnetic field gradient is required, for instance induced by a nearby nanomagnet. All electrical control is possible using more advanced combinations of spins, for example, **b** the so-called exchange-only qubit and **c** hybrid qubit. **b** The encoding in the exchange-only qubit is based on three spins in three adjacent quantum dots and control is provided via the exchange between the outer quantum dots and the central dot,  $J_L$  and  $J_R$ .<sup>46, 77, 78</sup> **c** The hybrid qubit is based on three spins as well, but requires only two quantum dots.<sup>48</sup> Universal qubit control makes use of the anti-crossings between the lowest three energy states to induce rotations about different axes. While these qubit representations are clearly more involved compared to the single-spin qubit, their operation may offer advantages for scaling toward large arrays where not the number of dots per qubit but the number and type of control lines per dot will likely form the largest challenge

different axes in the corresponding qubit Bloch sphere, and to entangle neighboring qubits with each other; see Fig. 2 for rotation axes of different qubit encodings. Altogether, this forms a universal set of quantum gates, which can be used to perform arbitrary logic.<sup>52</sup> Both single-qubit and two-qubit gates can be accomplished in one of two modes: (1) fast gate voltage pulses that rapidly switch the Hamiltonian so that the qubit(s) will start evolving around a new axis (in Hilbert space) or (2) radio-frequency or microwave-frequency electric or magnetic fields resonant with the energy difference between specific single- or two-qubit states. Gate durations vary from sub-ns to microsecond timescales.<sup>9, 10</sup>

Spin states are hard to detect directly, but can be converted to charge states via a sequence whereby a charge movement between dots or from a dot to a nearby electron reservoir is made to be spin state dependent, via “spin-to-charge conversion”.<sup>53, 54</sup> Simultaneous single-charge detection then reveals what the spin state was before the measurement. Real-time single-charge detection can be accomplished in several ways. In the first method, the conductance through a nearby charge detector is probed, either at baseband<sup>55</sup> or via radio frequency (RF) modulation.<sup>56</sup> The charge detector can be a narrow channel called quantum point contact (QPC) or a small island that itself is capacitively coupled to the quantum dot or donor. In either case, the conductance through it directly depends on the charge occupation of the dot or donor (see Fig. 1a, b). Alternatively, the ability of charges to move back and forth in response to an oscillating excitation can be probed. This amounts to an electrical susceptibility measurement, which is commonly implemented by

looking at the reflection of an RF signal applied to one of the quantum dot gates<sup>57</sup> or reservoirs.<sup>58</sup> Single-shot measurement times down to 200 ns have been achieved in specific settings,<sup>59</sup> and read-out fidelities as high as 99.8% have been reported.<sup>60</sup>

Qubit reset or initialization could be achieved by thermalization to the ground state, but that would be very slow given that spin relaxation times are often in the millisecond to second range.<sup>9, 10</sup> Faster approaches include initialization by measurement<sup>52</sup> and spin-selective tunneling from an electron reservoir or dot to a dot or donor.<sup>54, 61, 62</sup>

Finally, we note that microscopic variations in the semiconductor substrate and non-uniformities in the gate patterns lead to substantial variations from site to site in a realistic device. While progress has been made and high-quality double quantum dots have been reported,<sup>63</sup> an attractive but challenging solution would be to reach a uniformity level where a common (set of) DC voltage(s) would suffice to place each of several quantum dots in the desired configuration; for example, systematically having a dot-to-dot variation in required gate voltage for single electron occupancy smaller than the charging energy. Donor fabrication introduces more challenges, but the strong confining potential can have specific advantages here due to the intrinsic large energy scales. Fabrication based on scanning-tunneling-microscopy<sup>54</sup> as compared to ion implantation has the further advantage that uncertainties in donor placement and capacitive coupling to nearby stray donors are significantly reduced. However, a systematic study on the relevant variations for a large array is missing. Furthermore, nominally identical operations currently require DC gate voltages, gate voltage pulses, and

microwave control signals that all differ in amplitude or duration from qubit to qubit.

### CONTROL SIGNAL REQUIREMENTS

The discussion of electron spin qubits in quantum dots or donors leads us to the following commonly recurring requirements for the control signals. As can be seen from Fig. 2, not all requirements apply to each of the encodings, and this can be a criterion for comparing the merits of different encodings with each other.

1. an independently calibrated and tuned DC gate voltage on every site (typically up to  $\pm 1$  V)
2. independently calibrated and tuned gate voltage pulses on every site (typically up to tens of mV and with sub-ns rise times)
3. independently calibrated and tuned microwave magnetic or electric fields at every site (typically  $-40$  to  $-20$  dBm, 1–50 GHz bursts of 10 ns to 1  $\mu$ s duration)
4. a high precision of each of the control signals to achieve error rates comfortably below the 1% accuracy threshold
5. initialization, operations and read-out on timescales short compared to the relevant decoherence time.

We now examine some of these requirements in more detail, and in particular consider which requirements can be relaxed. In the next section, we will present some general guidance for meeting the necessary requirements.

For the pulsed control signals, often only one of the two pulse stages requires precise tuning. For instance, the precise strength of the exchange interaction is important when the exchange is turned “on”, but the exchange strength in the “off” state merely needs to be below some threshold, which is a much more relaxed constraint. The exchange is commonly controlled by changing gate voltages along the so-called detuning axis that controls the relative potential of neighboring dots (see Fig. 2). To reach the “off” state, it suffices to pulse gate voltages to a sufficiently far detuned condition. Similarly, when performing exchange gates at the so-called symmetry point (see the caption of Fig. 2), it suffices to pulse the gate voltages to any condition where the residual exchange is sufficiently suppressed, though this may require larger voltage amplitudes than when pulsing the detuning. Similarly, accurate level alignment is needed during read-out of a single spin based on spin-selective tunneling to a reservoir,<sup>54, 62</sup> but when not reading out it suffices to stay in the regime with one electron per site. Spin read-out of two-electron spin states is typically even more forgiving, as it suffices to pulse from somewhere deep in the regime with one electron on each dot, to somewhere in the so-called pulse triangle with two electrons on one of the dots.<sup>65, 66</sup> Therefore, one could imagine that voltage pulses to, say, control exchange gates or initiate read-out can be made uniform across multiple (all) dots, by fine-tuning the exact qubit operating points via DC bias voltages. The main assumption in these examples is that the qubit is not sensitive to the exact DC gate voltage while in the “off” state. As the qubit transition frequency may in fact vary with DC gate voltage,<sup>49, 50, 67</sup> unintentional single-qubit  $\hat{z}$ -rotations could occur and these must be tracked or corrected separately for every qubit.

For microwave control signals, we need to separately consider the microwave frequency vs. amplitude and duration. The simplest approach is to assume that all qubits will need to be resonant with either a single frequency or a small number of frequencies. This can be achieved by  $g$ -factor control or Stark shifting, through either DC or pulsed control voltages,<sup>49, 50</sup> to bring qubits on specific sites in or out of resonance with the excitation. For conventional electron spin resonance (ESR) whereby a global microwave magnetic field is applied,<sup>49, 68–70</sup> the same microwave can be used to achieve the same angle of

rotation on multiple qubits provided the amplitude variations are sufficiently small and the resonance frequency of all qubits resonant with the excitation is sufficiently uniform. Uncontrollable spin-orbit coupling renormalizing the  $g$ -factor can give qubit-to-qubit variations in the resonance frequency of order 10 to 100 MHz at  $B = 1.5$  T (ref. 67). A possible strategy to overcome such variations is operating at significantly lower magnetic field. Globally applied alternating current (ac) magnetic fields could give rise to excessive dissipation and heating, and the magnetic field profile may suffer from distortions due to all the metal interconnects. A strategy could be to integrate local microwave lines that are close to the qubits and only address subsections of the larger qubit array. Superconducting lines could further reduce dissipation.

For electric-dipole spin resonance, whether based on intrinsic spin-orbit interaction<sup>41, 71</sup> or on local magnetic field gradients to allow electric fields to drive spin transitions,<sup>51, 72, 73</sup> dot-to-dot variations in the confining potential may impose different microwave amplitudes for every qubit. All-electrical control is often argued to be beneficial because of fast and local control. Essential in the design will be the interconnection between the microwave source and the individual qubits. Power dissipation will be significantly reduced compared to ESR, but avoiding cross-talk will be challenging. A solution for cross-talk could include to spatially separate qubits with equal resonance frequency.

The main message from this technical discussion is that even though some requirements can be relaxed, especially if the quantum dot properties are homogeneous, at least a subset of signals (DC, pulsed, or microwave) will need to be independently calibrated and delivered to each and every qubit.

### CONTROL SIGNAL WIRING SOLUTIONS

How can we route qubit-specific classical control signals to a large number of quantum dot or donor qubits? The common understanding in the field is that directly connecting via wires or coax lines say  $10^8$  sub-100 mK qubits to room temperature voltage sources, pulse sources, and microwave sources, is impractical for several reasons. At the qubit chip level, it conflicts with Rent’s rule in classical systems<sup>11, 12</sup> and practical limits to the number of pins on a chip. At the level of the transmission lines from room temperature to the chip, heat transport causes a heat load of a few mW on the 4 K plate. For comparison, cooling powers of currently used pulse tube systems are in the range of a few W at 4 K. Below 4 K, superconducting lines can be used, which are poor thermal conductors and thus minimize heat load, but power dissipated in the attenuators can heat up the coldest parts of the dilution refrigerator. A common view is that instead a combination of two ingredients will be required:

1. Multiplexing strategies
2. A first layer of classical electronics residing next to the qubits and commensurate with the inter-qubit spacing

Other layers of classical electronics may reside farther away from the qubit plane and at higher temperature, as the data rates between layers higher up in the quantum computer architecture are orders of magnitude smaller than those between the physical qubits and the first control layer.

Within this framework, important choices include

1. What qubit density to work with?
2. At what temperature do the qubits reside? Is operation at 1.5 or 4 K possible?
3. What is the functionality of the first electronics layer?
4. What specifications must the electronics meet (clock speed, noise, resolution, frequency range, memory, power dissipation)?

These questions are interrelated, for instance the qubit density and the cooling power (which depends on the temperature) impact the functionality and specifications of the electronics that can be achieved. We next discuss platforms based on a dense qubit array or a sparse qubit array, and an operation temperature ranging from 100 mK to 4 K.

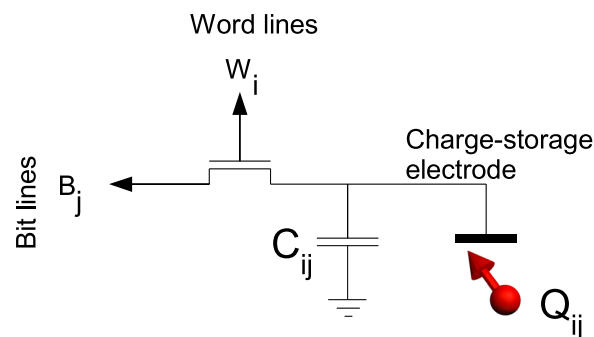
#### Dense qubit array and cross-bar addressing

The most widely used mechanism for two-qubit gates using quantum dots is based on the exchange interaction.<sup>74–76</sup> This interaction couples the spin states of two electrons when their respective wave functions overlap, i.e., when the respective dots are tunnel coupled.<sup>13</sup> The two-qubit exchange gate is very fast: it can be operated on sub-ns timescales, limited in practice by the bandwidth of the control electronics rather than by the underlying physics. In the absence of nuclear spin noise that is mostly relevant in III–V quantum dots,<sup>9</sup> the fidelity is often limited by electrical noise, usually charge noise from the amorphous materials and interfaces, and electrical noise on the gates. Coherent spin exchange between neighboring spins has been extensively realized in double dots as well as in linear arrays of three dots,<sup>9, 39, 77, 78</sup> and scaling up a linear array to larger sizes is relatively straightforward.

Scaling to a large two-dimensional array of tunnel coupled dots presents a great opportunity for realizing highly dense qubit arrays, but also presents practical challenges to wire up all the qubits, given the geometric constraints. To make things concrete, in order to have sufficient tunnel coupling between neighbors in the array, the center-to-center distance between dots must be no more than a few 100 nm in GaAs, <100 nm for qubits defined in silicon (a result of the three times larger effective mass in Si), and <20 nm for donors (due to the strong confinement potential). Taking a 100 nm qubit-to-qubit pitch as an example, a 2D array of 1 mm<sup>2</sup> would allow space for a massive 10<sup>8</sup> qubits. However, with at least one control line per qubit, fan-out of the control lines requires multiple layers of interconnects. If the interconnects and control lines can come from all sides, but have the same width as the quantum dots, a 4 × 4 array requires two layers (the first layer to contact the outer dots, the second to contact the inner dots), five layers are needed for a 10 × 10 array and 50 layers for a 100 × 100 array. There is clearly a practical limit to the size of a monolithic array that can be wired up in this way.

A possible strategy to partly overcome this fan-out problem is to borrow concepts from dynamic random access memory (DRAM). Rather than connecting every gate continuously to a voltage source, an individual gate is connected to a capacitor that stores the desired voltage. The voltages can be set efficiently via a cross-bar addressing scheme<sup>40</sup> (Fig. 3). Given that a single electron charge  $e$  is the smallest amount of charge that can be added to the capacitor, the capacitance required to achieve a gate voltage resolution  $\Delta V$  must be  $C > |e|/\Delta V$ . For  $\Delta V = 1 \mu\text{V}$ , this gives  $C > 160 \text{ fF}$ . Furthermore, thermal noise in the circuit when the switch is closed translates to an uncertainty in the gate voltage given by  $V_{\text{rms}} = \sqrt{k_B T/C}$ , which is a function of the capacitance but independent of the circuit resistance. Reaching an uncertainty  $V_{\text{rms}} = 1 \mu\text{V}$  at a temperature of 50 mK would require a capacitance larger than 800 fF. One challenge with this approach is the chip area required for such relatively large capacitances. Conventional planar approaches with  $10 \text{ fF}/\mu\text{m}^2$  are not compatible with the envisioned small dot spacing so that other solutions such as concentric pillar capacitors will be needed.

These charge-storage electrodes may have to be periodically refreshed, due to leakage or variations in the capacitive coupling to nearby structures. Such refreshing is routinely done in classical electronics. For instance, a typical refreshing interval time of DRAM is 64 ms where a refresh cycle is performed within 30 ns. If the 1% weakest electrodes can be excluded, the interval time can



**Fig. 3** Charge-storage capacitors for biasing quantum dots, in analogy to DRAM. Individual qubit communication can be achieved via a pair of word lines and bit lines. A voltage can be applied to qubit gate  $Q_{ij}$  via  $B_j$  by setting  $W_i$  high and stored on capacitance  $C_{ij}$  by subsequently setting  $W_i$  low. Depending on the pitch and dimensions of transistors and quantum dots, more complex circuits can be constructed based on this method

be extended to a second. While the tolerances of quantum dot voltages are much more stringent, leakage is strongly reduced at a few Kelvin or below, so such an approach might be feasible. Experimental drifts of approximately one Coulomb oscillation per hour  $\approx 8 \text{ mV/h}$  have already been observed in charge-storage electrodes integrated with quantum devices.<sup>79</sup> However, more research is needed to demonstrate these drifts using electrodes that have a size comparable to the quantum dots and to minimize possible leakage pathways.

Globally controlling these floating electrodes could be done via an efficient cross-bar addressing scheme, using horizontal and vertical control lines that each have a spacing corresponding to the dot-to-dot distance. Assuming a dot-to-dot pitch of 50 nm, consistent with requirements for quantum dots, would imply an interconnect pitch of 50 nm, which is similar to what is possible with 14 nm node technology, the most advanced that is commercially available today (<http://www.intel.com/content/www/us/en/silicon-innovations/intel-14nm-technology.html>).

Furthermore, 50 nm is below the 70 nm transistor gate pitch for the 14 nm node. Therefore, unless dot dimensions can be kept slightly larger, integrating a single transistor above every quantum dot requires continued scaling of conventional CMOS devices, dictated by Moore's Law.

A cross-bar approach can also provide a relatively economical avenue for qubit control. For instance, we can apply a voltage pulse on one of the vertical lines (combined with the DC voltage required by that site via a bias-tee) and use the horizontal line to select to which qubit the pulse is applied. As discussed in the section of control signal requirements, it should be possible to allow the same pulse amplitude to induce an exchange gate or initiate read-out across multiple dots. In this case, parallel addressing of multiple dots will be possible, as well as addressing for instance all dots or half of the dots (any combination of dots compatible with cross-bar selectivity is possible). It has indeed been shown that the cross-bar approach can be used to run the surface code, both in donor and dot platforms.<sup>32, 40</sup> It was also shown that surface code variations can be implemented with reduced local control.<sup>37, 38</sup>

Initiating parallel read-out is possible with a cross-bar approach as well, with vertical lines used to select the set of qubits underneath and horizontal lines used to carry the corresponding read-out signals. It may be possible to re-use the same cross-bar that is used for control, also for read-out, for instance using dispersive gate read-out.<sup>57</sup> An RF signal is then applied to a vertical line (again added to a DC gate voltage) and the horizontal lines select the qubit that is read out. This procedure comes at a

cost. In its simplest form, an array of  $N$  qubits requires  $\sqrt{N}$  repetitions of this read-out protocol to measure all the qubits.

This slow-down has two sides. First, it requires that probability of error of a qubit during  $\sqrt{N}$  read-out cycles stays far below the accuracy threshold. Here, the extremely long memory times of spin qubits under dynamical decoupling, of order one second,<sup>49, 69</sup> are crucial. Second, it slows down the net clock cycle of the surface code operation by a factor  $\sqrt{N}$ . Here, we note that it is not clear what the optimal effective clock cycle is. Too slow is not good since it slows down the computation. Too fast is not good either, since then the classical processors cannot keep up processing the massive data streams produced by the surface code syndrome measurements, and this will pose a hard boundary. This flexibility in choosing the clock cycle of the classical computer may turn out to be an important advantage of electron spin qubits over, e.g., superconducting qubits.

As a more sophisticated and efficient read-out variant, it may be possible to combine the cross-bar approach with frequency multiplexing<sup>80</sup> when using RF techniques for read-out.<sup>57, 58</sup> In this case, each horizontal line can carry multiple read-out signals simultaneously. The demonstrated on-chip resonators<sup>80</sup> will be challenging to fit locally into a dense array. However, frequency multiplexing could also be achieved by clever crossbar operation. For example, if the gates that control the interdot tunnel coupling are connected to vertical lines, these can be frequency-modulated so that each vertical line has a different modulation frequency. The resonance frequency of the readout circuits, measured along the horizontal lines, will then shift corresponding to the respective modulation frequency. This frequency multiplexing enables simultaneous read-out along horizontal lines. Global simultaneous read-out is then obtained by connecting each horizontal line to a separate circuit or by frequency multiplexing each horizontal line. If  $k$  frequencies can be simultaneously read out,  $k\sqrt{N}$  qubits can be read out in parallel. This gives further design flexibility and room for optimization.

An important consideration for any of the above uses of cross-bar addressing is whether power dissipation in the switching circuits is compatible with dilution refrigerator temperatures. The desired functionality of the control circuits will determine the number of required active components, the total power dissipation, and the minimum operation temperature. Dynamic power dissipation is a major source of power dissipation in classical electronics, here a single switch contributes  $P = CV^2af$ , with  $C$  is the circuit capacitance,  $V$  the applied voltage, and  $a$  the activity factor relative to clock cycle with frequency  $f$ . For example, if refreshing the voltage on the floating gate would involve compensating a 10  $\mu\text{V}$  drift at 1 V gate voltage and at a conservative refresh rate of 1 MHz per qubit, dissipation would amount to 8 pW for a capacitance of 800 fF, the lowest capacitance that can give 1  $\mu\text{V}$  noise and resolution, as discussed above. The additional power needed to drive the switching of the transistors could be dissipated at higher temperature stages. Large dilution refrigerators are now capable of providing cooling power beyond 1 mW at 100 mK. Therefore, many millions of transistors could potentially operate in combination with floating gates at the lowest temperature stage, provided they can be interconnected to higher temperature stages with dissipationless (superconducting) lines. Simple functionalities such as multiplexing strategies could become compatible with the discussion here and research to find the optimal hybrid, with essential electronics operating at the lowest temperature and all other electronics at higher temperature stages is, therefore, key to scaling spin qubits.

#### Sparse qubit arrays and local electronics

Several alternative spin qubit coupling mechanisms exist besides direct exchange coupling, that allow the building of two-dimensional spin qubit arrays without the need for direct tunnel

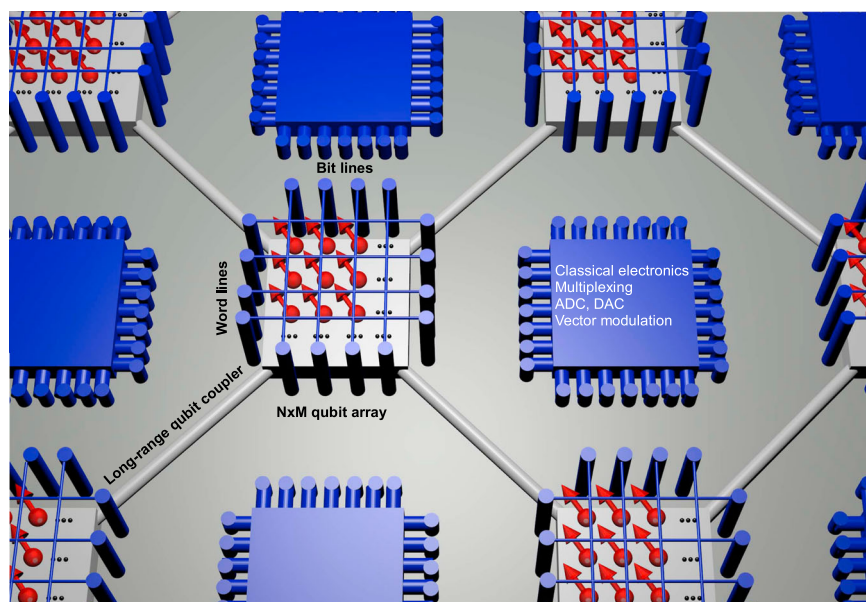
coupling between neighboring qubits in four directions (north, south, east, west). Many of these mechanisms have in common that they allow the separation of the qubits by larger distances, varying from roughly 1  $\mu\text{m}$  to roughly 1 mm. Proposals for coupling spin qubits at a distance rely on the use of superconducting resonators,<sup>15, 18, 26, 29</sup> capacitive coupling,<sup>23, 24, 36</sup> ferromagnets,<sup>28</sup> superconductors,<sup>27, 31</sup> intermediate dots or dot arrays,<sup>19, 20, 33, 34, 39</sup> or surface acoustic wave cavities.<sup>30</sup> An alternative approach consists of shuttling electrons across the chip between distant quantum dots, where the electrons are propelled by surface acoustic waves<sup>21, 22, 81</sup> or time-varying gate voltages.<sup>16, 35, 82, 83</sup> Whereas with enough motivation, any of these platforms could be realized in industry cleanrooms, those that only require additional gate metal are most easily integrated with CMOS technology.

When combining coupling mechanisms at a distance with local registers of tunnel coupled qubits, a modular structure arises as illustrated in Fig. 4. Modular architectures are currently considered across a wide variety of platforms, from trapped ions to superconducting qubits to impurity spins of NV centers in diamond.<sup>84</sup> Quantum error correction schemes such as the surface code can be naturally implemented on modular or distributed quantum computers. For instance by moving two logical qubits onto the same local register, two-qubit logical gates can be performed with known methods.<sup>85</sup>

Widely spaced qubit arrays can alleviate fan-out and wiring problems, simply by allowing more space for routing as also seen in Fig. 4. Yet, even if this allows space to connect each qubit to one or more control lines running off the chip, we mentioned before that connecting individual qubits to sources and generators a large distance away is not viable. Therefore, the more important advantage of space between the qubits may be that it allows a first layer of control electronics that is commensurate with the inter-qubit spacing to be placed directly above or in the qubit layer. If placed above the qubit layer, this classical layer can be interfaced with the qubit layer via an interposer, flip-chip (C4) technology or similar methods. Thermal isolation between the quantum and classical chips could be provided by using superconducting vias for connection. In this way, heating of the qubits by thermal dissipation in the classical circuitry is minimized. When transistors are realized in the same plane as the qubit layer, they could be integrated directly with traditional CMOS fabrication.

Depending on the actual spacing between qubit arrays and on the power budget, the functionality of the classical layer can be more or less advanced.<sup>86</sup> At the lowest level, simple multiplexing strategies based on switches can be implemented. What would have more impact is if analog to digital converters (ADC), digital to analog converters (DAC), and vector modulation could be implemented locally in the first classical layer. In this case, only digital signals must flow between the first classical layer and a second layer higher up in the control structure, potentially even at room temperature, where the digital data is processed. The required bandwidth of the communication channel between the classical layers is then much smaller, as per qubit one or a few bits of information must be transmitted per clock cycle, instead of time traces containing a large number of analog data points. Even then, data rates to room temperature are substantial. For example, if  $10^8$  qubits are repeatedly read out at 1  $\mu\text{s}$  intervals and each qubit measurement provides one bit of information, the data flow amounts to 100 Tb/s. Control will require a few bits and several operations per surface code cycle. Therefore, local error decoding would be highly attractive but also most demanding in terms of circuit complexity.

The feasibility of this approach hinges on a number of questions that each constitute a full research question, for which only an initial analysis has been performed to date. First estimates indicate that footprints on the order of  $(100 \mu\text{m})^2$  and a power budget in the microwatt range per qubit could be sufficient to implement



**Fig. 4** Sparse qubit array with local electronics. Long-distance qubit coupling opens up space for local electronics that can control a small dense qubit array. In the schematic, this electronics is placed in the qubit plane. Alternatively, it could be located on a separate chip and connected to the qubit chip by flip-chip or similar technologies. A crucial aspect is the optimum qubit array size  $N \times M$  and the functionality of the local electronics. Ideally, the local electronics include ADC and DAC converters, as well as vector modulation, such that a minimal number of control lines needs to interface with the outside. Giving the strong dependence of refrigerator cooling power on temperature, power dissipation in the classical electronics integrated with the qubits would likely require the qubits to operate at higher temperatures. Therefore, the demonstration of high-fidelity spin qubit operation at four Kelvin would be a milestone toward extendable structures

DC bias sources, AC control DAC's (operating at 300 MS/s), pulse memory and control logic with currently available 65 nm technology.<sup>87</sup> These would implement the complete set of low level control circuits for baseband controlled qubits. If appropriate low-power microwave modulators can be designed, EDSR control would also be possible. Further optimization, the use of a more advanced technology node, and a reduced functionality could lead to a substantial reduction in the required footprint. The dissipation could potentially be reduced by several orders of magnitude if the transistors are fully optimized for low temperature operation by reducing the supply voltage.<sup>88</sup> Cooling power itself would not be a severe limitation if electronics can be operated at 1.8 K or higher (for comparison, the Large Hadron Collider magnet system has eight cryocoolers that together provide a cooling power of 144 kW at 4.5 K and 20 kW at 1.9 K (ref. 89)), but a key question is whether the resulting temperature gradient between qubits and electronics can be maintained in conjunction with a sufficient interconnect density. Regarding error decoding, it has been shown that the best-performing surface code algorithm lends itself to parallelization,<sup>90</sup> and that it requires about 2  $\mu$ s per round and qubit on a current high performance CPU.<sup>91</sup> Substantial improvement can be hoped for with an application-specific integrated circuit, but it remains to be seen if the resulting circuit complexity and power consumption will be acceptable. Alternatively, other decoders that are less computation-intensive may become an option,<sup>92, 93</sup> including decoders based on neural networks.<sup>94, 95</sup> To put the electronics footprint in perspective, convenient qubit spacings to allow reliable gate operations from the physics perspective range from 1–10  $\mu$ m for capacitive couplers,<sup>23, 24, 36</sup> from 1–100  $\mu$ m for spin shuttles<sup>16, 35, 81–83</sup> and from 100–1000  $\mu$ m for superconducting resonators<sup>15, 18, 26, 29</sup>. A final consideration is that the constraints on power dissipation as well as the interconnects between electronics and qubits would be greatly reduced if spin qubits could be operated at higher temperature, without excessive compromises in the fidelity of initialization, coherent operations,

memory time, and read-out. We explore this attractive possibility in more detail in the next section.

#### Hot qubits

Much would be gained by qubits that can operate at 1 to 4 K. At 4 K, the cooling power of a single commercial pulse tube cooler as used in qubit experiments today is 1–2 W. By comparison, powerful dilution refrigerators offer a cooling power of 1 mW at 100 mK. At  $T < 100$  mK, we, therefore, expect that only very simple functionality can be realized without excessive heat dissipation. Superconducting classical circuits<sup>96</sup> dissipate very little power, but are complex in design, lack the memory function, and have a large footprint. Operating spin qubits at 4 K, with a thousand-fold increase in available cooling power, makes the prospect of electronics commensurate with and right next to the qubit plane more realistic. An integrated quantum-classical structure would have multiple advantages in solving the fan-out problem, would simplify the RF wiring and reduce signal losses.

A major attraction of Si-MOS-based quantum dots and donor-based qubits is that they can have energy scales that are compatible with 1 to 4 K operation. Proper operation requires that the relevant energy scales are about five times larger than the thermal energy, which is 340  $\mu$ eV at 4 K. Charging energies of donors and small quantum dots are easily in excess of 10 meV and orbital energies can be of order 10 meV as well,<sup>97</sup> satisfying this requirement. However, in silicon there is also a valley degree of freedom. Silicon has a sixfold degeneracy due to crystal symmetry, which is broken at the interface leaving two relevant valley states. These lowest-energy valley states can be split via a sharp confinement potential, e.g., the silicon-SiO<sub>2</sub> or Si/SiGe interface, and a vertical electric field. In Si/SiGe devices, valley splittings are typically no more than 100  $\mu$ eV in current devices.<sup>51</sup> Possibly this energy scale can be significantly increased by reducing dot size or adopting novel growth approaches. Alternatively, the valley could be initialized using advanced methods such as a measurement-based active reset for high-temperature operation. By comparison,



in Si-MOS dots, the valley splitting has reached almost 1 meV,<sup>49, 98</sup> and could also be pushed up further by reducing the device dimensions and increasing the electric field by confinement gates. This would allow initialization in the lowest-energy orbital and valley state.

Spin splittings in all spin qubit measurements to date are far below the thermal energy at 1–4 K. This would pose problems for conventional single-spin initialization and read-out schemes.<sup>54</sup> Simply increasing the magnetic field and hence the spin splitting would imply impracticable qubit operation frequencies of (sub) THz and potentially too short relaxation times. Instead, high-fidelity initialization and read-out of spin states can make use of the single-dot singlet-triplet splitting, which is typically somewhat below the orbital or valley splitting (whichever is lower) due to the exchange interaction.<sup>9</sup> For initialization, two electrons are loaded on the same dot, occupying the ground state valley and orbital state with the spins in a spin singlet configuration. One electron is then moved to the neighboring dot by adjusting the gate voltages, creating a state with one electron on each dot. If the movement is diabatic with respect to the difference in Zeeman energy between the dots, the spins will remain in their spin state and thus be initialized in the singlet state, which is a natural initial state for a  $S - T_0$  qubit.<sup>65, 99</sup> When using  $\{|\uparrow\rangle, |\downarrow\rangle\}$  qubits, the spin singlet can be rotated to  $|\uparrow\rangle|\uparrow\rangle$  via single- and two-qubit gates if desired. If the difference in Zeeman energy is large compared to the exchange energy, diabatic pulsing might not be an option. Instead, adiabatic transfer of one electron to the neighboring dot will directly result in the  $|\uparrow\rangle|\downarrow\rangle$  state<sup>65</sup> (Fig. 2). Spin read-out at temperatures exceeding the spin splitting can be realized based on Pauli spin blockade,<sup>70</sup> whereby two electrons can or cannot come together on the same dot depending on their relative spin states. The (relative) spin state can then be inferred from charge-sensing,<sup>9</sup> as was shown also in recent experiments using Si-MOS quantum dots.<sup>41, 75</sup>

With one well-initialized electron on each dot, qubit splittings can be chosen in a comfortable range, say 5–200  $\mu\text{eV}$ , which corresponds to accessible microwave frequencies of 1–50 GHz. Hence by combining a large energy splitting for initialization and read-out with a lower level splitting during qubit manipulation, the frequencies for driving qubits do not have to be scaled up with the operating temperature.

The spin relaxation time  $T_1$  will be reduced with higher temperature. Below 100 mK,  $T_1$  is typically very long, especially in silicon, with measured  $T_1$  times of over one second<sup>62, 98</sup>; see ref. 100 for a theoretical analysis on the limiting relaxation mechanisms. At low temperature, the temperature dependence of  $T_1$  is dictated by one-phonon (direct) processes, and the relaxation rate will increase roughly linearly with temperature.<sup>9</sup> However, the relaxation rate can have a much stronger temperature dependence at higher temperatures due to two-phonon transitions, such as  $1/T_1 \propto T^{7-9}$  (Raman) and/or  $1/T_1 \propto e^{-\Delta E/k_B T}$  (Orbach), where  $\Delta E$  is the energy to the first orbital state. For donors, the transition to the exponential temperature dependence due to Orbach transitions occurs at 6 K for phosphorus, 11 K for arsenic, 4 K for antimony, and 26 K for bismuth, all at a magnetic field of 0.3 T. The measured  $T_1$  is above one second at 4 K in all cases.<sup>101</sup> For silicon quantum dots, there are few experimental reports on the temperature dependence of  $T_1$ .<sup>102</sup> Based on the large orbital splitting of order 10 meV that can be realized in silicon quantum dots,<sup>37</sup> one would expect the transitions to two-phonon processes to occur at relatively high temperatures as well. However, imperfect interfaces give rise to spin-orbit coupling between the valley states, and this opens a new channel for relaxation as observed in experiment,<sup>98</sup> which will have a strong sample-to-sample dependence. Nevertheless, long  $T_1$  times have been achieved even in systems with very small valley splitting.<sup>51</sup> This suggests that at least in this temperature range, multi-phonon processes do not dominate and more research on the

temperature dependence is needed. Nonetheless, the long relaxation times leave a lot of margin, and we anticipate that it is possible to substantially increase the operating temperature of silicon spin qubits.

Decoherence from hyperfine interaction with nuclear spins in the substrate will be approximately temperature independent. An important question is to what extent both low-frequency and high-frequency charge noise will be enhanced by thermal excitations. Charge noise affects spin states most strongly during gates based on exchange or capacitive coupling (Fig. 2), but also a single spin is sensitive to electric fields through the Stark effect, and this sensitivity is higher if local magnetic field gradients are present. Established models indicate that low-frequency charge noise increases linearly with  $T$ , and such signatures are seen in recent experiments on SiGe and SiMOS dots.<sup>103</sup> In GaAs, a quadratic dependence of high-frequency charge noise was observed between 50 and 250 mK. If silicon devices exhibit similar behavior, this would strongly impact two-qubit gate fidelities. Significant improvements in the quality of exchange oscillations (the basis for most two-qubit gates, and for single-qubit gates in some qubit representations) were recently obtained by keeping the qubits at all times at the so-called symmetry point (Fig. 2a).<sup>104, 105</sup> At this operating point, the spin states are to first order insensitive to the energy detuning between neighboring dots. This detuning is typically the main channel through which charge noise affects the qubit splitting. Even coupling spin qubits via resonators may be possible at 4 K, despite the fact that the resonator will be thermally populated.<sup>106</sup> Altogether, we believe that potential 4 K operation of spin qubits is an attractive possibility.

## CONCLUSIONS

Wiring up large qubit arrays is a common, central challenge across all qubit platforms. From the above discussion, we see that electron spin qubits in quantum dots or donors offer several particularly attractive features for overcoming this challenge. First, the sub-100 nm lateral dimensions of quantum dots or donors allow for highly dense qubit registers that nevertheless can be wired up with multiplexing and cross-bar approaches with charge-storage electrodes. The feasibility of such approaches strongly benefits from the extremely long coherence times of electron spins in nuclear-spin-free host materials such as isotopically purified  $^{28}\text{Si}$ ,<sup>49, 69, 107</sup> which relax the requirements of parallel read-out and control that short-lived qubits must meet. Second, multiple ideas have been proposed for interconnecting qubit arrays over micron to mm distances. This leaves flexible space for interconnects and integrated electronics. Third, spin qubits on dots or donors may be operated at temperatures of 1–4 K, where the available cooling power is about 1000 times larger than below 100 mK, the typical operating temperature today. This would greatly simplify the integration of a first layer of classical control electronics right next to the qubits, again strongly relaxing the interfacing challenges.

These proposed solutions and approaches are not mutually exclusive. For instance, charge-storage electrodes can be beneficial also in sparse arrays, and a classical layer with (very) limited functionality could be incorporated with dense arrays. Furthermore, it is clear that there is still a big step to take from formulating general ideas as done here, to a complete proposal for an actual device, including device lay-outs, dimensions, power budgets, and so forth. Nevertheless, it is clear that spin qubits offer several particularly attractive possibilities in this direction. Finally, the continuous development of semiconductor technology provides further perspective that the wiring challenges can in fact be overcome, paving the way for the construction of a large-scale universal quantum computer.

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## AUTHOR CONTRIBUTIONS

L.M.K.V. and M.V. wrote the manuscript. All authors discussed the work together and commented on the manuscript.

## ADDITIONAL INFORMATION

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