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Menicucci, Alessandra; Malatesta, Fabio; Di Capua, Francesco; Campajola, Luigi; Casolaro, Pierluigi; Furano, Gianluca; Di Mascio, Stefano; Ottavi, Marco

**DOI**

[10.1109/NSREC.2018.8584279](https://doi.org/10.1109/NSREC.2018.8584279)

**Publication date**

2018

**Document Version**

Accepted author manuscript

**Published in**

2018 IEEE Nuclear and Space Radiation Effects Conference, NSREC 2018

**Citation (APA)**

Menicucci, A., Malatesta, F., Di Capua, F., Campajola, L., Casolaro, P., Furano, G., Di Mascio, S., & Ottavi, M. (2018). Simplified Procedures for COTS TID Testing: A Comparison between  $^{90}\text{Sr}$  and  $^{60}\text{Co}$ . In *2018 IEEE Nuclear and Space Radiation Effects Conference, NSREC 2018* Article 8584279 IEEE. <https://doi.org/10.1109/NSREC.2018.8584279>

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# Simplified procedures for COTS TID testing: a comparison between $^{90}\text{Sr}$ and $^{60}\text{Co}$

1<sup>st</sup> Alessandra Menicucci  
Department of Space Engineering  
TU Delft  
Delft, The Netherlands  
a.menicucci@tudelft.nl

2<sup>st</sup> Fabio Malatesta  
Cobham Gaisler  
Göteborg, Sweden  
fabio.malatesta@gaisler.com

3<sup>st</sup> Francesco Di Capua  
Dept. of Physics  
University of Naples Federico II and INFN  
Naples, Italy  
dicapua@na.infn.it

4<sup>st</sup> Luigi Campajola  
Dept. of Physics  
University of Naples Federico II and INFN  
Naples, Italy  
luigi.campajola@na.infn.it

5<sup>st</sup> Pierluigi Casolaro  
Dept. of Physics  
University of Naples Federico II and INFN  
Naples, Italy  
pierluigi.casolaro@na.infn.it

6<sup>st</sup> Gianluca Furano  
Data Systems and Microelectronics Division  
European Space Technology Centre - ESTEC  
Noordwijk, The Netherlands  
gianluca.furano@esa.int

7<sup>st</sup> Stefano Di Mascio  
Department of Space Engineering  
TU Delft  
Delft, The Netherlands  
s.dimascio@tudelft.nl

8<sup>st</sup> Marco Ottavi  
Department of Electronic Engineering  
University of Rome Tor Vergata  
Rome, Italy  
ottavi@ing.uniroma2.it

**Abstract**—The tolerance to the cumulative effects of ionizing radiation is one of the most important parameters to keep in account when selecting an EEE component for space applications. TID sensitivity is normally investigated measuring changes induced by gamma rays from  $^{60}\text{Co}$  sources to nominal parameters of a component or to its expected functional behavior. In this work we propose an on-chip  $^{90}\text{Sr}/^{90}\text{Y}$  electron source as an alternative methodology for TID tests.  $^{60}\text{Co}$  and  $^{90}\text{Sr}/^{90}\text{Y}$  TID test setups for a complex SoC are compared in terms of complexity and of experimental results, investigating the use of a  $^{90}\text{Sr}/^{90}\text{Y}$  as well as the established  $^{60}\text{Co}$ . We show that  $^{90}\text{Sr}$  allows a simpler test setup, manages to reproduce specific modes of failure obtained with  $^{60}\text{Co}$  and causes failures at comparable total doses. This makes  $^{90}\text{Sr}$  an interesting alternative to  $^{60}\text{Co}$  qualification and the use of untested components, to be further investigated especially for complex COTS SoCs.

**Index Terms**—component, total dose, Cobalt

## I. INTRODUCTION

The use of System-on-Chip (SoC) solutions in the design of space-borne data handling systems is an important step towards further miniaturization in space. In cubesats and in many aggressive commercial missions, use of Commercial Off-The-Shelf components is becoming the rule, rather than the exception and many of those are complex SoC, MPSoC (multiprocessor system-on-chip), SiP (System in package) or AMS-SoC (Analog/Mixed Signal SoC) [1]. It is well known that the possible sources of failure of these devices are Single Event Effects (SEE) [2], [3] and Total Ionizing Dose (TID) [4], [5]. In particular the TID characterization of these complex devices presents new challenges that are either not

fully addressed by current testing guidelines or may result in cumbersome test configurations. In this activity we aim to study test set-up, procedures and achieve some sample results for TID testing of miniaturized complex devices. This is a starting point to build knowledge and set guidelines to be applicable to all devices for which classical  $^{60}\text{Co}$  tests is too cumbersome or expensive to be viable.

During standard tests using high intensity  $^{60}\text{Co}$  sources, all sensitive parts except the Device Under Test (DUT) must be shielded. One commonly used method is to deploy heavy lead blocks of sheets to shield the sensitive components in order to avoid the risk to invalidate the test. This is sometime impossible given the fact that ancillary circuits are often on the same test board and, even with bespoke designs, the maximum possible distance is limited. These difficulties in a standard  $^{60}\text{Co}$  irradiation room, could be overcome only with the development of complex and expensive test setup. A more confined radiation field could avoid such problems and the need for ad-hoc designed boards, allowing the use of typical SoCs modular evaluation boards which provide cheaper and faster solutions.

Furthermore, physical distance between the DUT and the measurement equipment needed is often on the order of 10 meters or more, depending on the facility. For this reason, testing at realistic clock speeds, comparable with real applications, is very cumbersome if using the traditional approach which relies on the usage of long cables [6]: if fast clocks or analogue signals need to be monitored on the DUT, complex set-up is needed. In this work we used the solution addressed by [7]



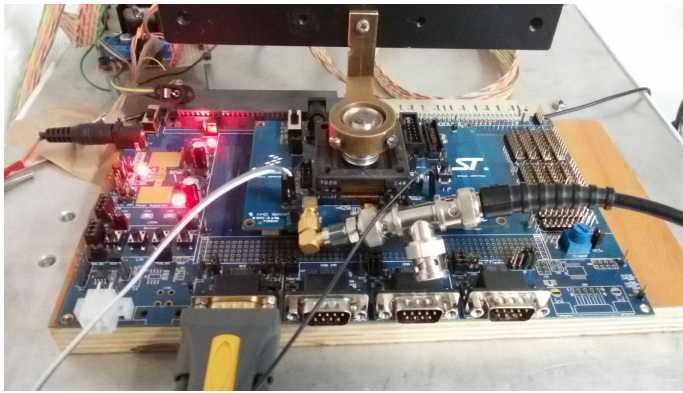


Fig. 2. Test Setup for  $^{90}\text{Sr}$  test

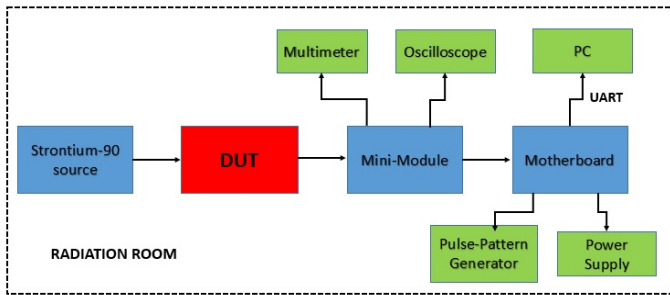


Fig. 3. Diagram of the test setup for  $^{90}\text{Sr}$  test

different test procedures have been employed:

**Procedure A:** this test has been performed in the same conditions as the  $^{60}\text{Co}$  test, described in [11]. For this reason the procedure is the same as in [11], and it is reported here:

- 1) Flash the DUT with the ADC program and read ADC value.
- 2) Flash the DUT with the "Test as you fly" program and place it for irradiation.
- 3) Irradiate the device to the dose required, according to the current irradiation step (see Table III-A).
- 4) Stop the irradiation and execute intermediate operations:
  - Monitor FCCU outputs with the oscilloscope to check correct activity of the device, voltage levels and frequency.
  - Measure current absorption without clock using the power analyzer.
  - Measure  $V_{\text{core}}$  voltage with a multimeter (DUT unlocked)
  - Reprogram the DUT with the ADC program (using additional motherboard) and measure ADC value.
  - Go to step 2 if other irradiation steps are required (see Table III-A)
- 5) Test again the DUT after several annealing conditions with the procedure described in step 4

**Procedure B:** the goal of this procedure is to find out

TABLE I  
 $^{90}\text{Sr}$  TEST: IRRADIATION SCHEDULE FOR PROCEDURE A

Step	Dose Rate [rad/h]	Duration [h]	Total dose [krad(Si)]
1	538	24	12.9
2	538	24	25.8
3	538	24	38.7
4	538	24	51.6

TABLE II  
 $^{90}\text{Sr}$  TEST: RESULTS FOR PROCEDURE A

Step	0 krad(Si)	12.9 krad(Si)	25.8 krad(Si)
Current (clocked) [A]	0.18	0.18	0.18
Current (unclocked) [A]	0.09	0.09	0.09
$V_{\text{core}}$ (clocked) [V]	1.268	1.277	1.278
$V_{\text{core}}$ (unclocked)[V]	1.250	1.251	1.251
FCCU (J16) [V]	3.68	3.68	3.68
FCCU (J18) [V]	3.52	3.52	3.52
FCCU [KHz]	7.87	7.88	7.88
ADC value	663	66B	-
Reprogramming	yes	yes	no

what is the maximum total dose that the DUT can tolerate. Therefore, the DUT has been placed under radiation with no interruption until it showed an unrecoverable failure. During the test time the device was running the "Test-as-you-fly" program, and its behavior was constantly monitored with the laptop. Moreover, the following parameters have been monitored:

- Supply Current absorption
- FCCU outputs: voltage levels and frequency
- $V_{\text{core}}$  voltage

For annealing, after irradiation, the device rested at room temperature for 1 day and then for 1 week at  $100^\circ\text{C}$ , inside a thermal chamber. Both anneals have been performed in the same electrical bias condition as the irradiations, but without providing the clock signal. During the annealing the board supply current was constantly monitored and electrical measurements have been made following each anneal increment.

**1) Test results for Procedure A:** The test results for procedure A are showed in table II. The device failed reprogramming at 25.8 krad(Si). After the annealing procedure the device was unable to recover its functionality and no contact through the JTAG was possible. We can conclude that the DUT reported a permanent failure on the flash controller. In fact, as described in [12], the on-chip charge pump is the first part of the flash memory to fail, although flash memories will continue to work - in read-only mode - at much higher radiation levels. During the 48 hours of irradiation the device experienced a total of 10 automatic resets, probably caused by the FCCU. The results showed a correlation with what happened in the  $^{60}\text{Co}$  test, performed in [11]: also with the  $^{60}\text{Co}$  the device failed reprogramming at approximately 30 krad(Si). This result shows a remarkable alignment between  $^{60}\text{Co}$  and  $^{90}\text{Sr}$  tests.

**2) Test results for Procedure B:** The device was continuously working under radiation for 247 hours, receiving a total dose of 133 krad(Si). After 247 hours the micro-controller

TABLE III  
<sup>90</sup>Sr TEST: RESULTS FOR PROCEDURE B

Total Dose [krad(Si)]	0	13	39	65	91	117	133
Board supply current [mA]	180	179	181	180	180	180	190
V <sub>core</sub> [V]	1,258	1,259	1,260	1,262	1,264	1,266	1,268
FCCU (J16) [V]	3,5	3,5	3,5	3,5	3,5	3,5	3,7
FCCU (J18) [V]	3,6	3,6	3,6	3,6	3,6	3,6	3,8
FCCU [KHz]	7,81	7,81	7,81	7,82	7,82	7,82	7,82

froze and needed a power supply reset, but the FCCU never showed any fault signal. After the reset the processor got stuck again after a few seconds. Since the device was unable to work continuously for more than 5 seconds, this was considered an unrecoverable fault: irradiation was stopped. After the annealing procedure the device did not recover its functionality: it was still unable to work continuously and, once locked, the FCCU still didn't show any fault signal. None of the tested parameters showed any significant variation, except for the V<sub>core</sub> voltage, whose behavior is showed in figure 4. The test results for procedure B are showed in table III. During the test the device experienced a total of 51 automatic resets.

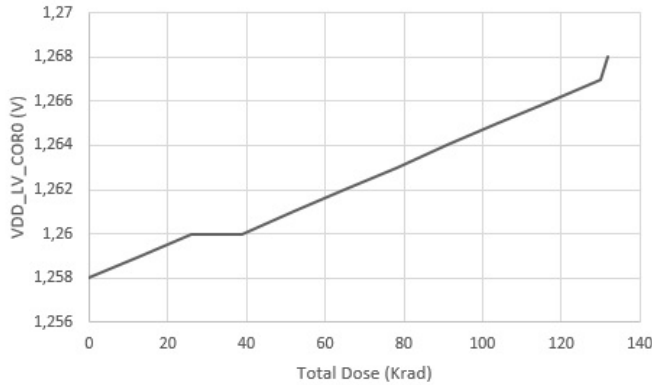


Fig. 4. <sup>90</sup>Sr TEST: Behavior of the V<sub>core</sub> voltage

### B. <sup>60</sup>Co test

This test has been carried out in the ESA-ESTEC <sup>60</sup>Co facility. As stated in [13], in ESTEC the Co-60 source consists of multiple small rods about 50 mm long held around the periphery of a 30mm diameter container. Once the source is raised to the irradiation position, the gamma beam produced by the Co-60 decay exits the irradiator unit through a collimator window into the radiation cell. The facility consists of the radiation cell and a large external control room with cable feed-throughs that enable the remote monitoring and controlling of experiments. For this reason, all the cables used for the measures and for the signaling needed to be long about 6 meters.

The dose rate used for the test has been of 830 rad/h. The test setup contained the following equipment:

- An oscilloscope, to monitor the FCCU pins on the minimodule
- A Pulse-Pattern Generator to provide the clock signal to the device. The clock signal provided was a square wave with 50% duty cycle, 40 MHz frequency, 1.3 V peak to peak with a 0.65 V offset.
- A Current Probe, to monitor the core's DC supply current.
- An Adjustable Output Stabilized Power Supply, to provide power to the board (12 V DC) and monitor the current drain.
- A laptop in the control room to log the program flow signaled from the DUT via UART.

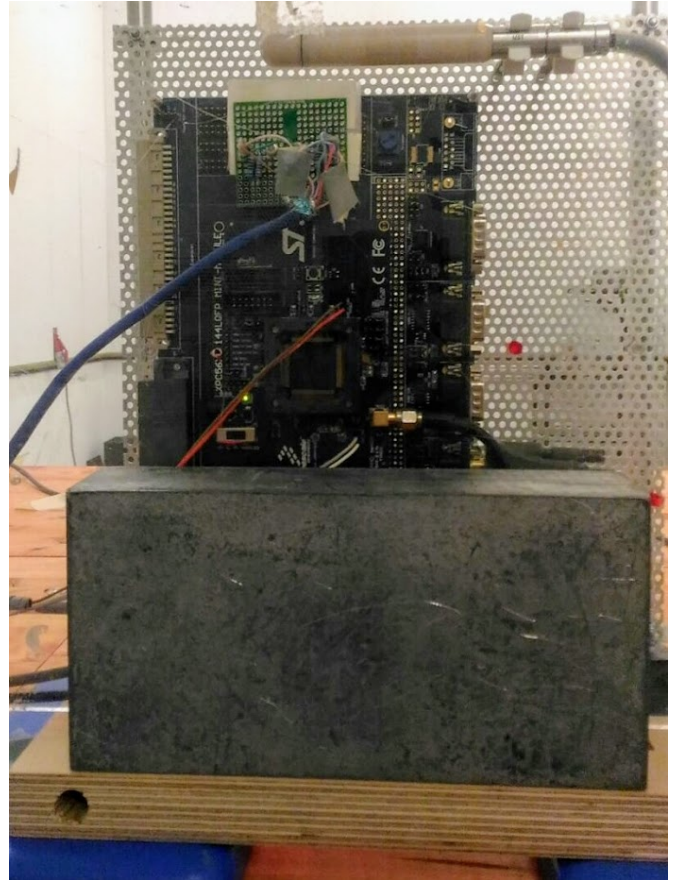


Fig. 5. Test Setup for <sup>60</sup>Co test

As shown in figure 6, only the board was stored in the radiation room. Moreover, shielding was necessary to ensure that no peripheral circuitry was interested by the irradiation. To ensure this condition, a lead brick has been arranged in front of all the used ancillary electronics on the board. All the remaining equipment was stored in the control room. As in procedure B of the <sup>90</sup>Sr test, the goal of this test is to find out what is the maximum total dose that the DUT can tolerate. Therefore, the DUT has been placed under radiation until it would had showed an unrecoverable failure. During the test

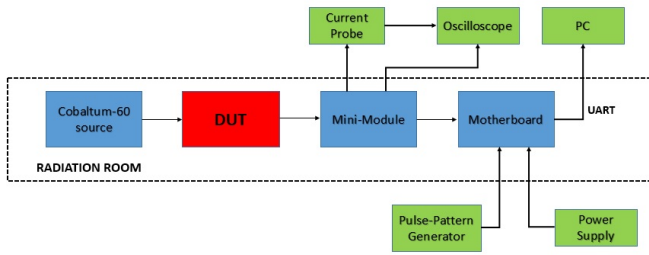


Fig. 6. Diagram of the test setup for  $^{60}\text{Co}$  test

time the device was running the "Test-as-you-fly" program, and was constantly signaling its behavior via UART. After the end of the irradiation procedure, the DUT has undergone the annealing procedure described in III-A.

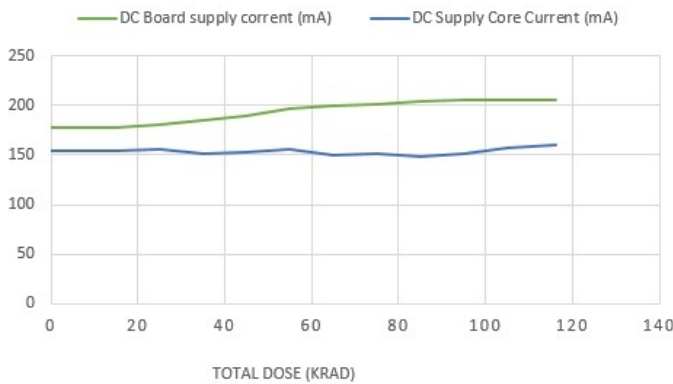


Fig. 7.  $^{60}\text{Co}$  TEST: Monitored currents

1) **Test results:** when the total dose reached 95 krad(Si) the DC Supply Core Current, while maintaining a stable average value, showed a wave shape very irregular comparing to the one at the test start (see figure 8). After 140 hours of irradiation (with a total dose of 116 krad) the device froze. After some power resets, the device was still unable to work continuously for more than 10 seconds. This was considered an unrecoverable failure and the start of the annealing procedure. Moreover, the FCCU signaling was damaged and the J18 pin experienced a 90% decrease of the peak to peak voltage. During the irradiation time, the DUT experienced a total of 3 automatic resets. The measures are reported here in table IV. After the annealing procedure the FCCU J18 pin recovered its normal behavior and the tested parameters returned to their original values. Nevertheless, the device kept freezing every 10 seconds and the Core Current kept its irregular shape. This results are very similar to those obtained to the procedure B of the  $^{90}\text{Sr}$  test. This is a further suggestion about the using of  $^{90}\text{Sr}$  as a valid alternative to the  $^{60}\text{Co}$ .

#### IV. CONCLUSION

This paper showed results from two different test procedures run both under  $^{60}\text{Co}$  and  $^{90}\text{Sr}$  irradiation. The results show

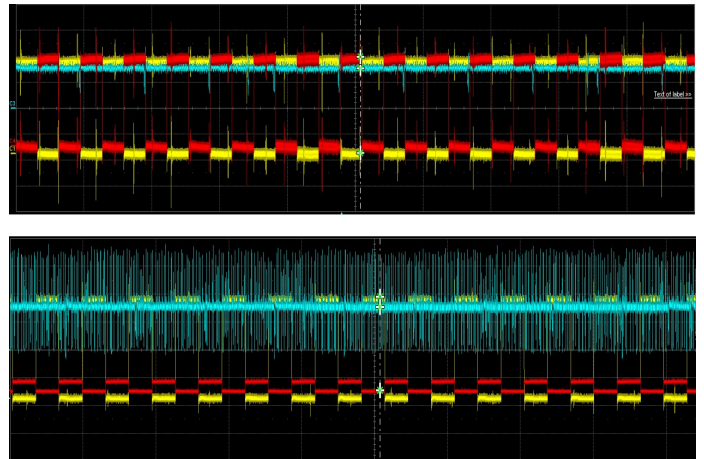


Fig. 8.  $^{60}\text{Co}$  TEST: Oscilloscope at test start (top) and at total dose equal to 116 krad(Si) (bottom). In red FCCU J18, in yellow FCCU J16, in cyan Supply Core Current.

Total Dose [krad(Si)]	0	15	45	75	95	105	116
Board supply current [mA]	177	177	190	201	205	206	206
Supply Core Current [mA]	154	154	153	151	151	157	160
FCCU (J16) [V]	3,5	3,5	3,5	3,5	3,6	3,6	3,6
FCCU (J18) [V]	3,4	3,4	3,4	3,4	3,5	3,5	0,3
FCCU [KHz]	7,84	7,84	7,84	7,84	7,84	7,84	7,84

TABLE IV  
 $^{60}\text{Co}$  TEST: MONITORED PARAMETERS

remarkable alignment. Procedure A showed that the maximum dose rate before flash reprogramming failure is about 30 krad for  $^{60}\text{Co}$  and 25.8 krad(Si) for  $^{90}\text{Sr}$ . Procedure B showed that the maximum (lethal) dose rate before the chip stops operating is about 116 krad for  $^{60}\text{Co}$  and 133 krad(Si) for  $^{90}\text{Sr}$ .

For complex SoCs it is crucial to irradiate the DUT without degrading the performances of the auxiliary circuits, which was much easier to be obtained with a directional source like  $^{90}\text{Sr}$ .

In addition, for COTS devices, the radiation qualification is often seriously compromised by the fact that samples with the same component identification may potentially have significantly different radiation hardness characteristics. Testing with  $^{90}\text{Sr}$  can then be exploited for the study of lot-to-lot variations.

These results suggest that electron irradiation with  $^{90}\text{Sr}/^{90}\text{Y}$  source could represent in future a viable, low-cost and suitable solution for screening of components to be used in space applications.

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