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An Ultracompact 9.4–14.8-GHz Transformer-Based Fractional-N All-Digital PLL in 40-nm CMOS

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***Abstract*— In this paper, we apply various area reduction techniques on an inductor–capacitor (*LC*)-tank oscillator in order to make its size comparable to that of ring oscillators (ROs), while still retaining its salient features of excellent phase noise and low sensitivity to supply variations. The resulting oscillator employs a proposed ultracompact split transformer topology that provides a 1:2 passive voltage gain and is less susceptible to common-mode electromagnetic interference than are regular high-quality-factor *LC* tanks, thus making it desirable in system-on-a-chip environments. The oscillator, together with a proposed dc-coupled buffer, is incorporated within an all-digital phase-locked loop (ADPLL) intended for wireline, digital clocking, and less stringent wireless systems. The ADPLL architecture introduces a look-ahead time-to-digital converter that exploits a deterministic phase prediction to reduce power consumption and phase detection complexity. The ADPLL is realized in 40-nm CMOS and has the smallest reported area of 0.0625 mm^2 among *LC*-tank oscillators while providing fractional-N operation, wide tuning range of 45% (from 9.4 to 14.8 GHz), very low voltage supply sensitivity of 80 MHz/V, and integrated figure-of-merit jitter (FoM$_{\text{jitter}}$) better than −230 dB. A separate identical ADPLL was implemented using an RO instead, for completeness and systematic comparisons.**

***Index Terms*— All-digital phase-locked loop (ADPLL), digitally controlled oscillator (DCO), inductor-capacitor (*LC*)-tank oscillator, ring oscillator (RO), time-to-digital converter (TDC), transformer.**

I. Introduction

MONOLITHIC frequency synthesizers have been used as key building blocks in a wide range of applications. In digital data communications, they are responsible for generating GHz-level frequency carriers either through an inductor–capacitor (*LC*)-tank oscillator or a ring oscillator (RO), depending on the application's set of requirements and IC implementation tradeoffs.

Due to their small silicon area, wide tuning range and performance improvements with scaling, ROs are widely adopted in wireline systems. However, their intrinsically poor phase noise (PN) and strong frequency pushing, i.e., sensitivity to supply voltage variations, impede their use in high performance applications, such as wireless communication. ROs often require either a very complex calibration [1] or high-power-supply rejection ratio (PSRR) LDOs [2] that employ large capacitors, thus effectively worsening their area advantage as well as their power efficiency.

On the contrary, *LC*-tank oscillators inherently feature much lower PN and higher power efficiency than ROs, due to the higher quality (Q)-factor of the *LC*-tank. Furthermore, some classes of *LC*-tank oscillators, such as class-F [3] or class-C, with inductor [4] or transformer [5], exhibit low frequency pushing (mostly related to a voltage dependence of their active devices' parasitic capacitance) since their active devices require gate biasing networks of zero dc current, thus promoting an effective RC filtering.

The typical drawbacks of *LC*-tank oscillators are their large size and narrow tuning range. Various inductor-area minimization efforts have been reported in literature to address the area disadvantage of *LC* oscillators. In [6], stacking of metal layers in a vertical solenoid fashion is employed, resulting in extremely small area, yet a very small tuning range of 5%–10%, which can be deemed insufficient in face of PVT variations. In [7], planar shrinking requires a large number of turns to compensate for the lower Q-factor, resulting in a high parallel capacitance [and consecutively low self-resonance frequency (SRF)]. Its operation in GHz-range is possible since it is implemented in SOI process (lower parasitic and substrate losses) and uses analog varactors as tuning elements. In advanced CMOS technologies, analog varactors are highly sensitive to voltage perturbations and might require large charge-pump capacitors or robust DAC capacitors when used in a PLL, thus reducing their area competitiveness. Moreover, that special inductor is very sensitive to its surroundings, thus requiring complete metal isolation [7], [8], which might infringe on design rules in advanced CMOS nodes.

A common approach to improve area is to operate the oscillator at higher frequencies than the target (which we also adopt as our work strategy). However, the additional power and area required for the frequency division should be considered. Furthermore, at higher frequencies, the capacitor bank tends to have a lower Q-factor (due to more lossy switches and/or analog varactors) and parasitic capacitance plays a bigger role, ultimately limiting the tuning range. For this reason, that solution has so far been applied mostly to narrowband wireless systems [9].

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Based on the above observations, an optimal oscillator topology would combine the superior PN and frequency pushing performance of an *LC*-tank oscillator with the low area and wide tuning range of an RO. Furthermore, to exploit the scaling of CMOS technology, a digital manner of frequency tuning would be desired.

In this paper, we propose an ultracompact transformer-based digitally controlled oscillator (DCO) with a size comparable to that of a typical RO, while offering much higher power efficiency, wide tuning range, and higher robustness to power supply perturbations. The oscillator is designed to operate at higher frequencies, thus reducing the size of passive elements (i.e., inductor and switched capacitors), while taking advantage of the technology scaling to minimize parasitic capacitance. It is designed using two separate coils that are excited in such a way as to offer common-mode electromagnetic (EM) cancellation, thus reducing sensitivity to external interferences, as well as coupling rejection to nearby circuits. The DCO is then used as a building block in an all-digital phase-locked loop (ADPLL), featuring a proposed look-ahead time-to-digital converter (TDC) that takes advantage of phase prediction to save power and to reduce complexity of the phase detection mechanism. Furthermore, a 3-stage RO is implemented and it is used in an almost identical ADPLL, so direct comparisons can be made.

This paper is organized as follows. In Section II, the proposed transformer-based topology is introduced and its advantages are described. The core DCO design is detailed in Section III. The ADPLL architecture, including the proposed look-ahead TDC, is described in Section IV, while experimental results are shown and compared in Section V.

II. Ultracompact Transformer-Based DCO

Efficiently scaling down an inductive element requires multiple optimizations to deliver the salient features of an RO (i.e., wide tuning range and small area) while keeping high power efficiency (i.e., better PN with less power) [10]. The goal is to pack a sufficient inductance into a small area, without drastically degrading the Q-factor. Moreover, parasitic capacitance of the inductor and of its accompanying g_m stage transistors should be kept low for a reasonable SRF, so that the desired tuning range can be achieved. At the same time, the stringent metal density requirements of advanced CMOS must be fulfilled.

EM coupling between the inductive structure and its surroundings is another point of concern, especially in system-on-a-chip (SoC) environments. A way to relax the inductor sensitivity is to use a quadrupole, as in [11] and [12]. It has been demonstrated that the EM coupling of a quadrupole is much lower than that of a single inductor, allowing a more compact overall design. It is pertinent to notice the superior advantage of a 4-lobe quadrupole [11], which is able to minimize the magnetic field in both symmetric axis, in comparison to the 2-lobe, which is only able to do so in one axis [11], [12]. However, even at the maximum coupling for the 2-lobe, it provides a 16 dB lower magnetic coupling than that of a single spiral [11].

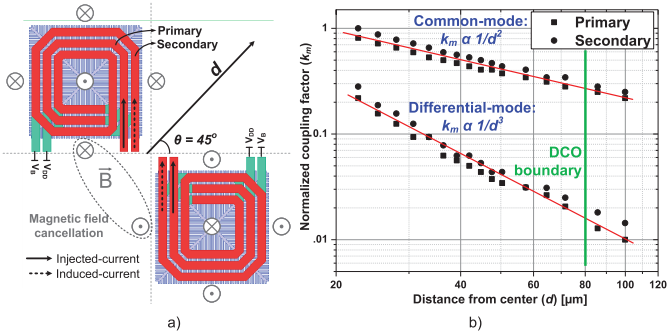

Fig. 1. Magnetic field cancellation. (a) Magnetic field directions. (b) Simulation of coupling factor (k_m) for common-mode and differential mode excitations.

For our proposed split-transformer oscillator, a 2-lobe quadrupole was used, but in a different arrangement and driving configuration. Based on the results of this paper, another version was implemented in 10-nm FinFET technology [13]. In the following section, a more thorough analysis is performed and conclusions are drawn.

A. Electromagnetic Field Cancellation

The large size of high-Q inductors inevitably makes them very sensitive to their surroundings, as they act like antennas. By either picking up noise or inducing currents in nearby circuits, these inductors could potentially lead to various operational issues, such as frequency pulling of two or more close-by oscillators, and noise induction in analog circuits, thereby requiring special countermeasures. Maintaining the inductor isolation and space between the circuits would be expensive due to extra silicon and not always permitted due to the stringent metal density rules.

In literature, solutions are proposed [14], [15] to deal with strong magnetic fields, such as 8-shape inductors. However, they are bulky and thus not very suitable for low-area implementations. On the other hand, transformers can additionally benefit from field cancellation while, at the same time, provide passive voltage gain between drains and gates of the cross-coupled pair of g_m devices, in order to alleviate any startup issues associated with the use of small devices as required for low parasitic capacitance.

In our proposed split topology, shown in Fig. 1(a), the magnetic fields ($\vec{B}$) generated by the coils are in opposite direction to each other (when driven differentially). To quantify this interaction, we analyze the magnetic coupling factor k_m between the transformer and a (probing) single coil. This approach emulates the current induction caused by the transformer in nearby circuits, tested at distance d and direction (θ) of 45°.

Fig. 1(b) shows the normalized k_m under common-mode and differential-mode excitations. The terminology used here is related to the injected current into the coils; i.e., in the common-mode, the injected currents in both coils have the same phase, generating similar magnetic fields, while in the differential-mode, the phases of the injected currents are 180° apart, generating opposite magnetic fields. In a typical

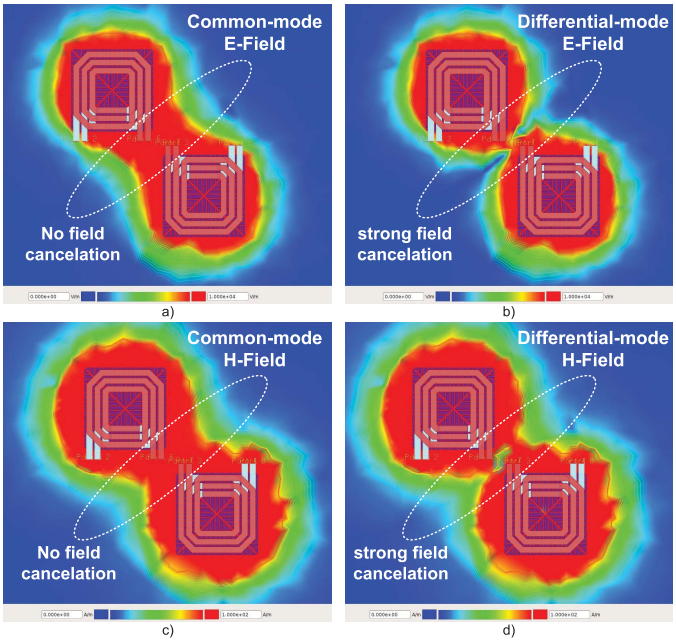

Fig. 2. FEM Simulation. (a) E-field common-mode. (b) E-field differential-mode. (c) H-field in common-mode. (d) H-field in differential-mode.

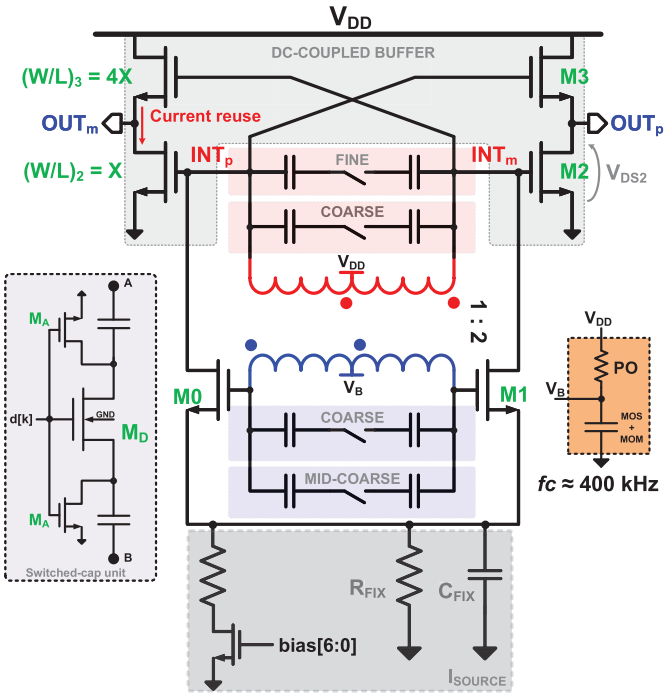

Fig. 3. Simplified ultracompact transformer-based DCO core.

single-inductor solution, only one magnetic field is generated, so it can be related to the common-mode excitation, even though the coil itself is excited differentially. The efficiency of the magnetic field cancellation can be shown firstly by the magnitude of k_m, which is 75% smaller for the differential-mode when compared to the common-mode, and the slope, $1/d^2$ and $1/d^3$, for the common-mode and differential-mode, respectively, according to the theory of dipoles [16].

The electric and magnetic fields can also be evaluated by plotting the magnitude of finite-element method (FEM) 3-D EM simulations under common-mode and differential-mode, as shown in Fig. 2. Both the electric and magnetic fields undergo strong cancellations in the direction (θ) of 45°.

The simulations presented in Figs. 1 and 2 indicate the benefit of exciting the structure in the differential-mode rather than in the common-mode (which would be the case of a single inductor as well), where the near field is beneficially canceled. Moreover, our proposed structure is similar to an 8-shape inductor (with respect to the generated EM fields), where the common-mode magnetic field is rejected and the differential-mode field vanishes for far-field observation (rejection of coupling to nearby signals).

III. Circuit Design

As discussed above, the proposed split transformer needs to be driven differentially, in order to achieve field cancellation. In the following, we describe in detail various aspects of the active and *LC*-tank circuitry that forms the DCO.

A. Transformer-Based DCO

We propose a transformer-based *LC* cross-coupled topology which enjoys a freedom to low-pass filter the gate bias voltage V_B of the active devices. This is to obtain a very low sensitivity of frequency pushing by minimizing gate-source capacitance, C_{GS}, modulation due to the gate-source voltage, V_{GS}. The proposed transformer-based DCO is shown in Fig. 3. The transformer is composed of two independent multiturn single-ended transformers, using top-layer metal conductors (thickness 0.85 μm), in a digital 40-nm CMOS technology without ultrathick metals, while satisfying all restricted metal density design rule check requirements that cannot be waived in advanced CMOS. The two independent transformer units are placed symmetrically to the center of the DCO, in order to obtain magnetic field cancellation.

The transformer is fully custom-designed (see Fig. 4 for more details) including pattern-ground shield in poly and all six thin metals (at the center of the coils) following the same pattern as the poly ground shield. It was simulated using the method of moments. Each coil has a winding width of 2.9 μm and spacing of 1.15 μm, where the outer and inner diameters are 38.9 and 16.9 μm, respectively. The V_{DD} and GND connections are done in Alucap. The transformer has a coupling coefficient $k_m = 0.7$ between the 350-pH primary and 1-nH secondary, peak Q-factor of $Q = 8$ around 13 GHz and SRF at 50 GHz.

The capacitor banks are divided between the transformer's primary and secondary. The coarse banks (6-b binary-weighted) are switched simultaneously, enhancing the overall Q-factor of the transformer over individual inductors [3]. Midcoarse and fine banks are both 14-b unit-weighted, but the effective capacitive weight of the former is $n^2 (= 4$ times) larger than the latter's, since the midcoarse is connected only at the secondary and the fine bank is connected only at the primary. The slight asymmetry caused by that does not degrade the Q-factor of the whole tank. Moreover, it can provide the required frequency range overlap as well as fine resolution.

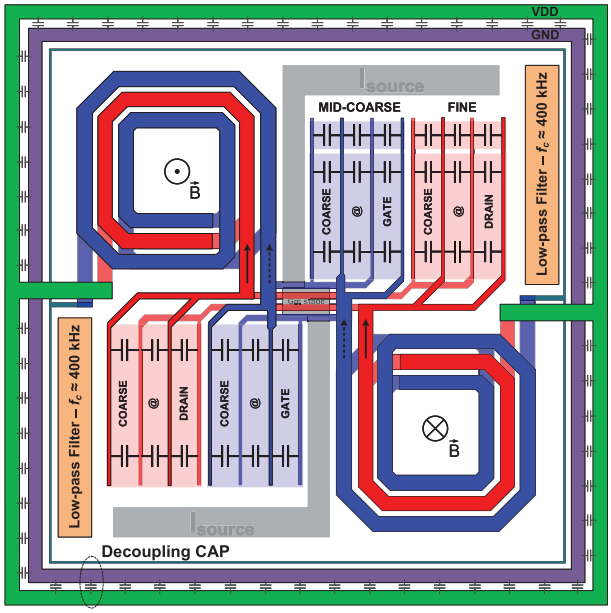

Fig. 4. Details on the layout of the DCO.

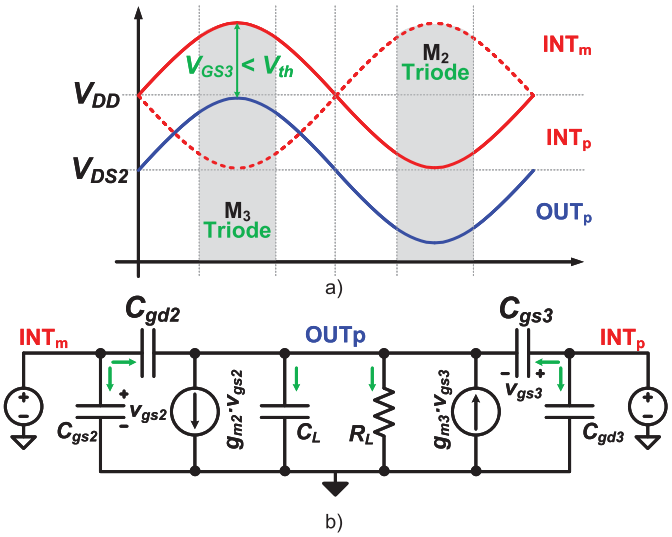

Fig. 5. DC-coupled low-voltage DCO output buffer. (a) Half-circuit large-signal excursions. (b) Half-circuit small-signal simplified model.

In order to improve the effective frequency resolution, a second-order MASH $\Sigma\Delta$ dithering is applied to three unit-weighted bits of the fine bank. It uses a divided version of the DCO output frequency ($\div 32$ or $\div 16$) to modulate capacitance of these three bits, thus effectively obtaining fractions of the minimum capacitance and, consequently, finer frequency resolution.

The switched-capacitor units were designed using the topology shown in Fig. 3. It is a differential metal-oxide-metal (MOM) capacitor with a main differential-mode switch, assisted by two common-mode auxiliary switches. The main nMOS switch (M_D in Fig. 3) turns the capacitor ON and OFF, while two smaller auxiliary nMOS transistors (M_A) provide a weaker dc path to ground for the source and drain of the main switch. Note that even in the OFF-state, the tiny leakage current of the auxiliary transistors ensures a high impedance path to ground, thus avoiding risky forward biasing of the junction diodes of M_D. The capacitor bank design is very critical, especially the connection between the switch and the capacitors, since excessive parasitic capacitance in these lines, due to cross-coupling, would affect the ON-/OFF-state capacitance ratio. To accomplish the desired tuning range, the $C_{\mathrm{ON}}/C_{\mathrm{OFF}}$ ratio was design to be around 3, with Q-factor of 14 and 140 for the ON- and OFF-state, respectively.

B. dc-Coupled Buffer

Besides the DCO optimization for the required PN and power consumption performance, another important concern is the immediate DCO output buffer. A nonlinearity of the driven load (including the buffer's nonlinearity itself) and a supply voltage disturbance could degrade the PN and, consequently, reduce the oscillator power efficiency. Also, the incessant technology node shrink requires voltage supply reduction, while the transistor threshold voltage (V_{th}) is kept roughly the same, thus requiring new buffer topologies to overcome these issues.

Most of the practical high-frequency buffers are connected to the DCO through dc blockers (i.e., ac-coupling capacitors) [3], [17], allowing the buffer bias voltage to be set locally. This helps to alleviate effects from the statistical process variation, especially pMOS and nMOS mismatches. However, these dc blockers add extra load and area to the oscillator tank and, depending on the frequency, they could be prohibitively large. Moreover, thermal noise of the shunt resistor (generally used for self-biasing) is easily coupled back to the oscillator and then up-converted. Some buffers, however, allow direct dc-coupling to the oscillator. The best example is a source follower, which features a wideband frequency response, but offers a voltage gain often well below unity. In order to increase its power efficiency, a combined source follower and common-source topology is proposed. Its schematic is shown in Fig. 3.

The buffer is thus dc-coupled to the DCO while sharing the same V_{DD} supply. It uses only nMOS devices to reduce capacitive loading, noise, and process mismatches. From Fig. 5(a), we can see that V_{GS3} is kept always constant and equal to $(V_{\mathrm{DD}} - V_{\mathrm{DS2}})$, which is chosen to be below the threshold voltage, V_{th}. In this way, M_3 operates in weak inversion and M_2, due to a velocity saturation, operates in strong inversion, since both share the same current and the former is $4\times$ larger than the later. For a short interval of the oscillating period (around 90° and 270° of the cycle), however, either one of the transistors goes into the triode region. Nevertheless, the overall performance of the buffer is not affected since the other transistor is providing an ac gain to the corresponding output. Also, due to a relatively small voltage swing (in our case 250 mV_p), this linear region is reached only for a brief angle duration. Therefore, for this analysis, we can still treat the circuit using a small-signal model.

Fig. 5(b) shows such a simplified small-signal model of the left-half of the circuit. The current reuse is represented by the

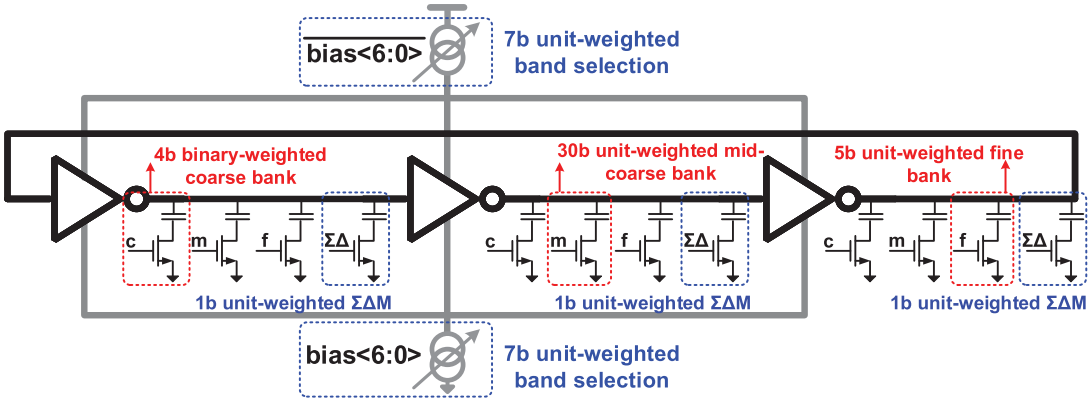

Fig. 6. 3-stage current-starving fully digitally controlled RO.

addition of g_{m2} to the gain, and the architecture provides a compensation for the gate–source capacitance of M_3 (C_{gs3}), contributing to an overall voltage gain enhancement of 20%, in our case, when compared to a simple source follower. The voltage gain enhancement, however, depends on the driven load, where the differential overall gain is given by

$$A_v = \frac{g_{m2} + g_{m3} + s(C_{gs3} - C_{gd2})}{g_{m3} + 1/Z_L + s(C_{gs3} - C_{gd2})} \quad (1)$$

where, Z_L is the output load impedance and includes the output dynamic impedance of the transistors.

The overall transformer-based DCO is packed in a square of 120×120 μm^2, and includes the transformer, capacitor banks, active core, output buffer and decoupling capacitors.

C. Ring Oscillator

The implemented RO is a 3-stage current-starved topology shown in Fig. 6. The frequency tuning is performed exclusively by digital control words, with very coarse steps ("band selection") provided by switched current sources, and finer frequency steps by single-ended switched capacitors. The capacitor bank is divided between 4-b binary-weighted coarse, a 30-b unit-weighted midcoarse and a 15-b unit-weighted fine banks. Also, a 3-b unit-weighted bank for second-order MASH $\Sigma\Delta$ dithering is implemented to enhance the frequency resolution.

To ensure the circuit's symmetry and balance, thus keeping the output load symmetric, consequently lowering the $1/f^3$ PN corner, the coarse and midcoarse banks are switched at the same time at all three DCO stages. For the fine bank and the $\Sigma\Delta$ dithering capacitors, the control is applied in a thermometer manner to only one of the DCO stages at a time so a finer resolution could be achieved with monotonic frequency steps. All capacitors are based on a unit cell, with an nMOS switch and a MOM capacitor that are combined in groups according to the desired bank capacitance. Moreover, a single-ended topology was chosen, since it provides a better FoM when compared to its counterpart (pseudo-) differential topology.

The complete RO is packed in a square of 120×120 μm^2, the same as the transformer-based DCO. The apparently relatively large area of the RO is due to accounting for the decoupling capacitors, which occupy 40% of the whole area (approximately 4 pF as a combination of MOS and MOM capacitors), and the $\Sigma\Delta$ modulator.

IV. Implementation of the Two ADPLLs

The aforementioned oscillators (i.e., RO and transformer-based) are integrated into two ADPLLs, sharing a common architecture. Thanks to the introduction of a "look-ahead" TDC as the fractional phase error detector, the ADPLLs feature low power consumption. Both loops operate with a feedback frequency ranging from 1.2 to 2 GHz, coming either from the RO (divided by 2) or the transformer-based DCO (divided by 8), thus keeping the PLL loop identical. The ADPLL operation and design are detailed in this section.

A. Look-Ahead Action and TDC

Traditional phase-domain (i.e., counter-based) ADPLL implementations [18] are resistant to a deep power consumption reduction because the TDC of fine resolution has to cover at least one variable clock period, T_V. Solutions such as clock-gating of the variable clock at the TDC have been proposed [19], [20]; however, none of them provides an optimal circuitry that would allow only the single necessary clock edge to pass to the TDC.

In this implementation, the deterministic nature of the phase error when the ADPLL is fully settled is taken advantage of to modify the traditional ADPLL architecture. Indeed, it has been shown in [21] that for every frequency reference (FREF) clock cycle, assuming locked type-II loop (both in frequency and phase lock), the deterministic time difference between the rising edge of FREF clock, and the next rising edge of feedback clock (CKV) is given by

$$\Delta_t = (1 - \mathrm{PHR}_F) \cdot T_V \quad (2)$$

where PHR_F is a fractional part of the accumulated frequency command word $\mathrm{FCW} = T_R/T_V$, where T_R is the period of FREF. In other words, FCW is the targeted ADPLL frequency multiplication ratio. Equation (2) suggests that each FREF rising edge can be delayed by a deterministic amount of time so that a delayed version of FREF is created, namely, $\mathrm{FREF}_{\mathrm{dly}}$,

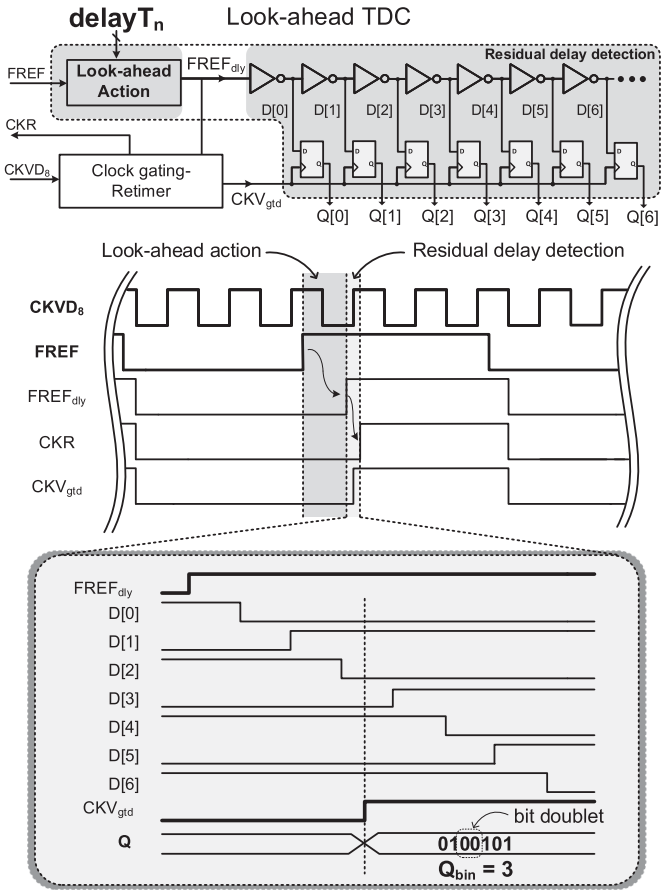

Fig. 7. Look-ahead TDC block diagram with interconnection to clock-gating and retiming circuit along with all the signal waveforms.

which is aligned (to within a small constant offset) to the next CKV rising edge. This predictive effect will be referred to as the look-ahead action.

The advantages of implementing the look-ahead architecture are numerous. First, the delay operation occurs at the FREF rate, which is typically two orders of magnitude lower than the CKV rate. It should be stressed that, even when proper prediction occurs, there is always a nondeterministic component of the FREF-to-CKV delay that renders the use of a TDC to resolve the $\mathrm{FREF_{dly}}$-to-CKV residual delay necessary. Nevertheless, the TDC action is carried out by only a few delay elements. Most importantly, since $\mathrm{FREF_{dly}}$ and CKV are now aligned, $\mathrm{FREF_{dly}}$ can be used to clock-gate the TDC, allowing its operation at the FREF rate. Another key benefit of the look-ahead action is that retiming of FREF to create a digital clock (CKR) for the feedback loop, as in [18], is now a metastability-free operation and, therefore, no significant circuit-level effort and power consumption are required to resolve it. Instead, a conventional re-sampling of $\mathrm{FREF_{dly}}$ by a divided version of CKV suffices as the CKR generation mechanism.

Fig. 7 shows the conceptual block diagram of the look-ahead TDC and its interconnections with the clock-gating and retiming circuitry, as well as the time diagram of all waveforms associated with the look-ahead action. The FREF signal is delayed within the look-ahead TDC to generate $\mathrm{FREF_{dly}}$, which is then used to generate CKR and a clock-gated version of the CKV, called $\mathrm{CKV_{gtd}}$. CKR is used as a *digital* global clock, while $\mathrm{CKV_{gtd}}$ (at the FREF rate) samples the TDC to resolve the residual error between $\mathrm{FREF_{dly}}$ and CKV. Unlike the TDCs in conventional ADPLL implementations [19], where the CKV is propagated through the inverter chain and sampled by FREF, in our case it is much more convenient to propagate $\mathrm{FREF_{dly}}$ instead and sample it with a gated version of CKV, operating at the reference frequency. As seen from Fig. 7, the output of the flip-flops can be converted to an integer number, by identifying the location of two consecutive identical logic values in the output bit stream. This integer number can be normalized to yield a representation of the fractional part of the phase error between FREF and CKV (PHE_F) when the ADPLL is locked. In Fig. 7, the decoded output of the delay is 3, which corresponds to a delay of three inverters ($3 \cdot t_{\mathrm{inv}}$).

A detailed schematic of the look-ahead TDC is shown in Fig. 8. The look-ahead TDC is implemented as a chain of identical controllable delay cells that can be used either as delay elements—for the look-ahead action—or as sampling elements—to resolve the $\mathrm{FRE}F_{\mathrm{dly}}$-to-CKV time delay. Each delay cell consists of an inverter and a pair of set/reset transistors that can pull up or down the corresponding cell input node [22]. Additionally, a compact D flip-flop (DFF) optimized for a minimum input capacitance and small setup and hold times is placed at each intermediate node. The simulated typical delay of the generic cell is 15 ps while the DNL and INL values are 0.5 and 1 LSB, respectively.

The cells located at the beginning of the inverter chain perform the look-ahead action, effectively acting as a digital-to-time converter (DTC). In this case, the DFFs act only as dummy loads (shown in gray in Fig. 8) and the set-reset transistors are active. The intended functionality of the DTC part is the propagation of a single pulse through a desired number of inverter delays. Since the $\mathrm{FREF_{dly}}$ output is fixed, the FREF input has to be dynamically selected every reference cycle, via the control of set/reset transistors. A logic control cell, shown in Fig. 8, converts a thermometer-coded input into the control signals for the pMOS and the nMOS transistors, respectively.

An example of the look-ahead action of the TDC is illustrated in Fig. 9, where a delay equal to two inverter delays is generated. The operating principle can be extended, without loss of generality, over any multiple of the inverter delays (t_{inv}). As shown in Fig. 9, the look-ahead TDC goes through three distinct and consecutive states during every FREF cycle, namely, the *reset* state, the *set* state and the *propagation* state. The reset state occurs when FREF is low and sets the output $\mathrm{FREF_{dly}}$ to a low steady-state, whereby the internal nodes of the look-ahead cells are set accordingly. In the *set* state, upon a rising FREF edge, a disturbance is generated at one specific internal node. The selected node changes progressively at every FREF edge (in a fractional-N operation). In this example, the disturbance starts from two cells away from the output ($\mathrm{FREF_{dly}}$). To achieve this, all nodes from *Start* backward are inverted through the set-reset transistors,

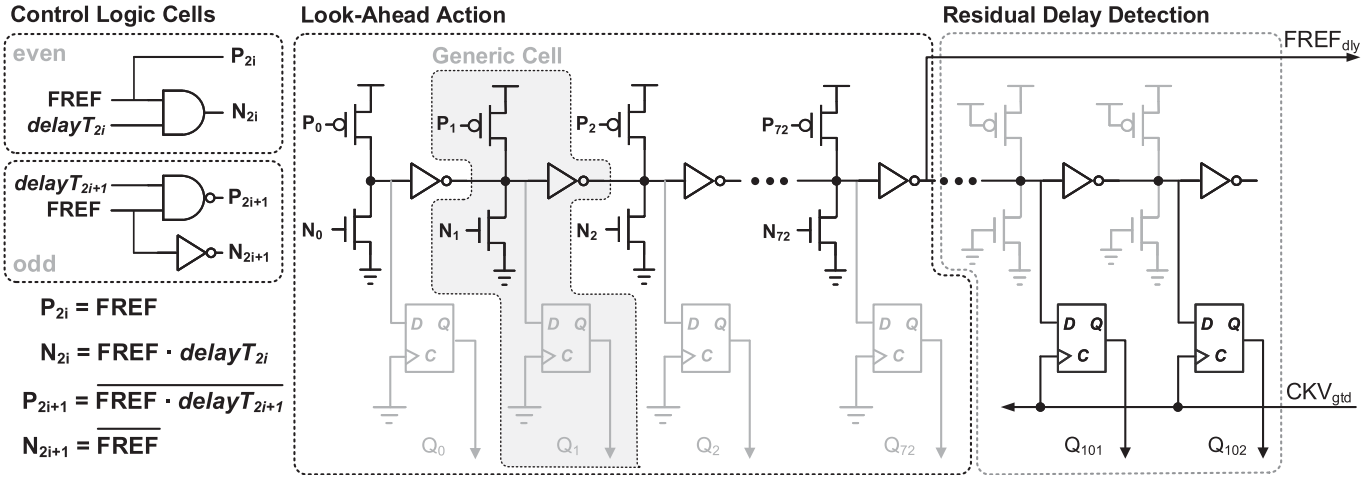

Fig. 8. Look-ahead TDC schematic implemented with identical controllable delay cells.

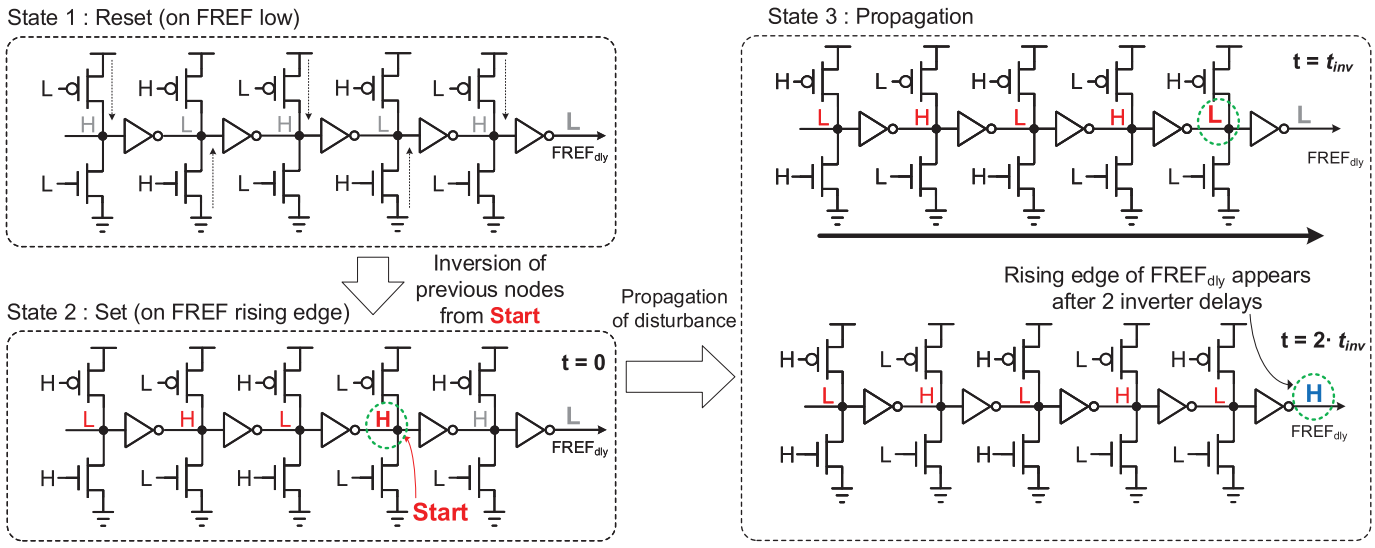

Fig. 9. Transition of the look-ahead part of the TDC through the *reset*, *set* and *propagation* states, for the generation of a delay equal to two inverter delays.

while the rest of the nodes, i.e., up to the end of the delay line, are set as floating by turning OFF their corresponding set–reset transistors. In fact, the disturbance manifests itself as two consecutive identical logic states, i.e., at the input and output of the same inverter. As a result, during the propagation state, the disturbance is propagated through the rest of the delay line and eventually enters the residual detection section, so the time difference between $\mathrm{FREF_{dly}}$ to CKV can be resolved. At the same time, the $\mathrm{FREF_{dly}}$ is used to clock-gate the CKV and for the CKR generation.

Knowing the cell delay t_{inv}, we can calculate the number of cells that the disturbance has to propagate through at each FREF cycle. Defining the gain of the look-ahead TDC as $K_{\mathrm{TDC}} \triangleq t_{\mathrm{inv}}/T_V$ and combining it with (2), we obtain

$$\mathrm{delay_{NR}} = \frac{1 - \mathrm{PHR}_F}{K_{\mathrm{TDC}}}. \tag{3}$$

A pseudo-thermometer coding of $\mathrm{delay_{NR}}$, as a number of the most significant zeros in a bit-stream of ones, is applied as a signal $\mathrm{delayT_n}$ at each logic cell, as shown in Fig 8. Each logic cell needs to convert $\mathrm{delayT_n}$ and FREF signals into the appropriate controls of the set-reset transistors. Based on the example of operation in Fig. 9, we can construct a truth table for each signal P_k and N_k and deduct logic functions as in Fig. 8.

As highlighted in Fig. 7, FREF is propagated through the chain of inverters while the $\mathrm{CKV_{gtd}}$ samples the intermediate node values by means of the DFFs. The flip-flop vector output is decoded as the location of a doublet of high or low logical values and should be then normalized by K_{TDC} to yield a representation of the fractional part of the FREF-to-CKV phase error (PHE_F).

With a single element delay of 15 ps, 64 elements are used to perform the look-ahead action in order to cover the worst case delay of 830 ps (1.2 GHz feedback clock) and account for PVT variations. As far as the fractional phase error detection is concerned, this can be theoretically achieved by one element (equivalent of a bang-bang TDC). However, this could have an

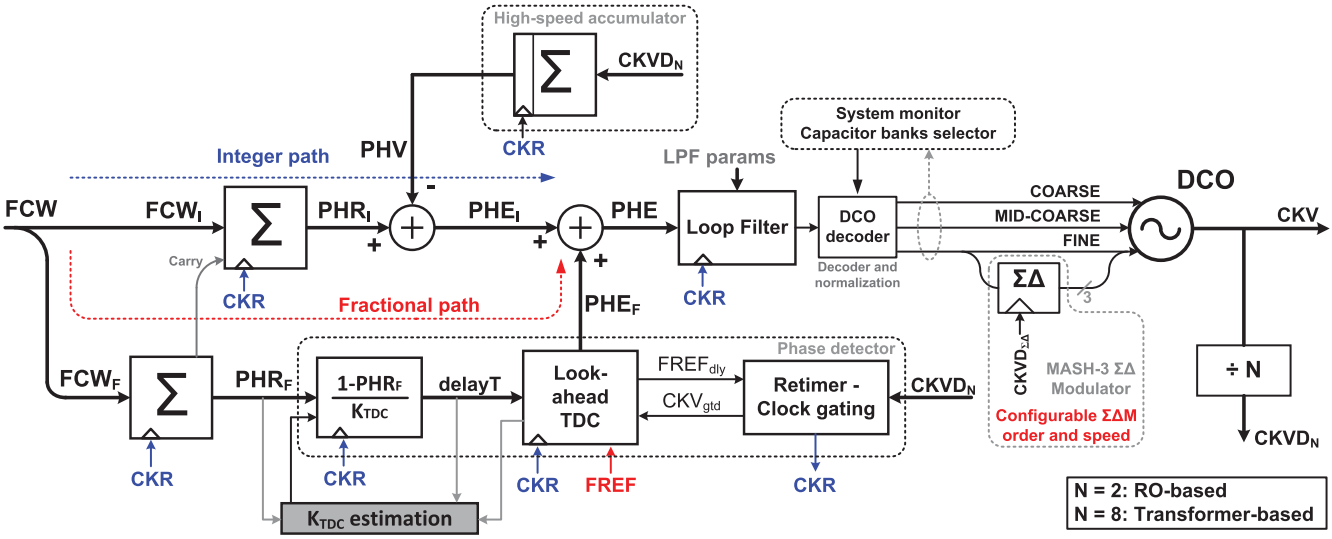

Fig. 10. Block diagram of the accumulator-based phase-prediction ADPLL.

unpredictable impact on the settling time of the phase error, if no additional frequency settling loop is employed. In our implementation, an output word of the eight-delay element FFs is read out, which is equivalent to a 3-b TDC, to ensure fast settling on the order of microseconds.

It should be noted that the "next clock edge prediction" approach has already been widely used in previous ADPLL implementations. In [23], a divider-based ADPLL architecture with a bang-bang detector was implemented. However, it requires a secondary loop with a complex frequency acquisition to ensure proper large frequency step locking. In [24], an accumulator bang-bang phase detector is utilized instead of a small range TDC for fractional error detection. However, it might cause unpredictable or long frequency locking transients. In addition, no advantage is taken of the aligned nature of the FREF_{dly} and CKV clocks resulting in a power-hungry sampler-based counter. Lastly, [25] implements separate DTC and TDC parts, an approach that is more prone to delay mismatches and requires different gain estimation blocks. In this implementation, a single delay element, embedded in the look-ahead TDC is used to ensure identical unit delays of the look-ahead action and the residual error detection. As a result, a single look-ahead TDC gain estimation block suffices for the estimation of the average delay of the elements. Furthermore, a dynamic element matching for the purpose of eliminating close-in fractional spurs can be straightforwardly implemented by employing a rotation of unit cells.

B. ADPLL Architecture

Fig. 10 shows the block diagram of the ADPLL. The frequency command word (FCW) is split into its integer and fractional parts, with separate reference accumulators that generate the integer and fractional part of the reference phase, PHR_I and PHR_F, respectively. In order to properly accumulate the FCW as a whole, a carry-out is transferred to the integer accumulator whenever an overflow of the fractional part occurs. A synchronous 8-b counter serves as the variable accumulator and produces the variable phase PHV which is subtracted from PHR_I to provide the integer part of the phase error PHE_I. PHR_F is used to calculate the TDC delay code, according to (3), which is, in turn, applied to the look-ahead TDC, through a gain. A TDC gain estimation block, based on an iterative adaptation algorithm, is implemented on-chip to dynamically track delay estimation errors due to PVT variations [26]. The digitized output of the TDC represents the fractional part of the phase error, PHE_F that is combined with PHE_I to yield the total fixed-point representation of the phase error, PHE.

The phase error PHE needs to be filtered, in order to properly set the loop dynamics. A reconfigurable proportional-integral controller is followed by a DCO decoder to form the oscillator tuning word. The DCO decoder design varies between the two ADPLLs due to the different capacitor bank configuration of the two oscillators. Both DCOs include switched capacitor banks that are dithered using a second-order MASH $\Sigma\Delta$ modulator in order to achieve a finer equivalent frequency resolution and to push the quantization noise into higher frequency offsets, where they are more easily filtered out and do not contribute significantly to the total jitter [27]. The operation frequency of the $\Sigma\Delta$ modulators can be dynamically selected from different taps of the divider chain in order to meet the required performance as a tradeoff between power consumption and jitter.

For the feasibility of the variable accumulator implementation, the feedback path was chosen to operate at a maximum 2.5 GHz, which means that a divide-by-2 version of the RO output and a divide-by-8 version of the transformer-based DCO output is fed back to the variable accumulator and the look-ahead TDC. Division by 2 in the RO-based ADPLL is achieved by a CMOS digital divider and for the division by 8 in the transformer-based ADPLL, a divider-by-4 (CML) is cascaded with a CMOS digital divider. These dividers are represented in Fig. 10 by the block $[\div N]$. Since in both

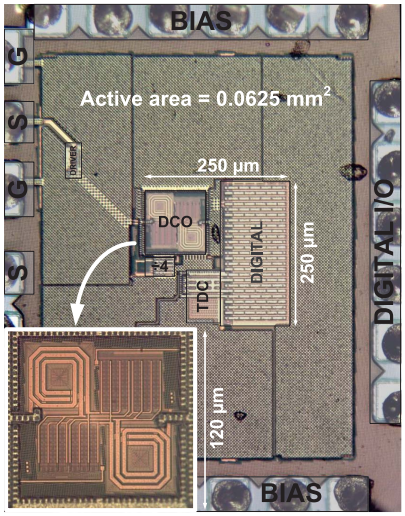

Fig. 11. Transformer-based ADPLL chip micrograph.

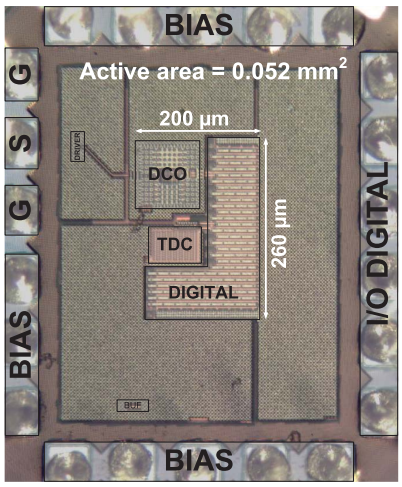

Fig. 12. Ring DCO-based ADPLL chip micrograph.

ADPLLs the loop feedback operates on a divided version of the output, the effective frequency command word has to be adjusted accordingly. Therefore, half of the multiplication ratio is accumulated at the RO-based ADPLL, and one-eighth of it for the transformer-based ADPLL.

As mentioned above, the clock-retimer gating circuit generates the important clock signals for the ADPLL: The CKR clock is used as a global digital clock of the ADPLL loop (at the reference clock rate), to resample the output of the variable accumulator and to generate a gated version of the variable feedback clock, $\mathrm{CKV_{gtd}}$.

V. Experimental Results

Fig. 11 shows the micrograph of the proposed transformer-based ADPLL fabricated in 40-nm TSMC LP CMOS technology, with an active area of 0.0625 $\mathrm{mm^2}$, where the DCO alone occupies 120×120 $\mu\mathrm{m}^2$. For a comparison, Fig. 12 shows the die micrograph of the RO-based ADPLL, in the same technology. The RO-based synthesizer occupies an area of 0.052 $\mathrm{mm^2}$, which is only 20% smaller than the transformer-based ADPLL, with both DCOs occupying roughly the same area.

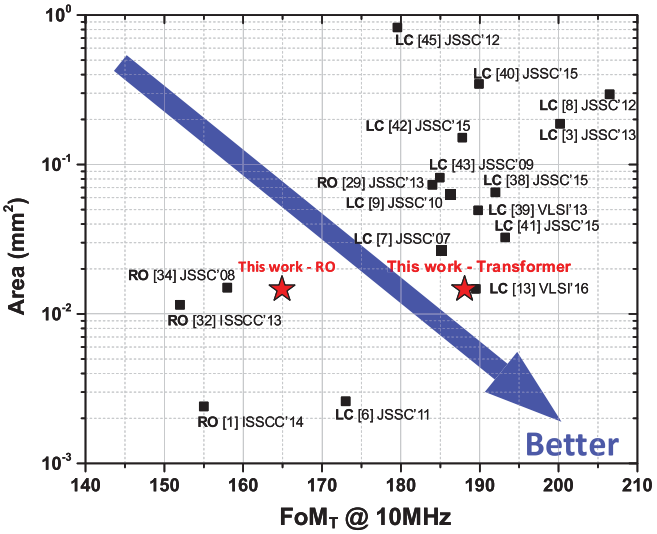

Fig. 13. FoM_T over area for stand alone state-of-the-art oscillators.

For a more coherent analysis, the figure-of-merit (FoM) [28] should be examined. It takes into account the oscillator free-running PN, power consumption (P_{dc}) and operating frequency (f_0). It is widely used and conveniently reproduced here as

$$\mathrm{FoM} = |\mathrm{PN}| \; + \; 20 \cdot \log_{10}\left(\frac{f_0}{\Delta f}\right) - 10 \cdot \log_{10}\left(\frac{P_{\mathrm{dc}}}{1\ \mathrm{mW}}\right). \tag{4}$$

An extension of the FoM is expressed by FoM_T, which includes also the oscillator tuning range, and is defined as

$$\mathrm{FoM}_T = \mathrm{FoM} + 20 \cdot \log_{10}\left(\frac{\mathrm{TR}[\%]}{10}\right). \tag{5}$$

The FoM and FoM_T of the transformer-based DCO are 175 and 188 dB, respectively. Fig. 13 depicts the measured FoM_T along with the occupied chip area and compares it with compact *LC* oscillators and ROs from literature. The FoM_T of the proposed transformer-based DCO is at least 20 dB better than other RO's of comparable size. The performance is still improved even when compared to advanced PN cancellation techniques applied in ROs [29]. As seen in Fig. 13, the proposed DCO occupies comparable area to an RO while retaining an FoM_T equivalent to *LC* oscillators.

Measurement results confirm a high accuracy of the design methodology. Center frequency, frequency step, power consumption and PN were measured within 10% of the simulation predictions. This also indicates the importance of having an accurate metal/oxide stack profile during the design process.

The transformer-based oscillator was designed to operate between 10–16 GHz with FoM of 176 dB and FoM_T of 189.3 dB but due to a slightly higher power consumption and a narrower tuning range (5.4 GHz instead of 6 GHz–10% lower), 1 dB lower FoM and FoM_T were measured. This pre-silicon accuracy appears quite remarkable, especially given the tiny size of the tank, where any extra parasitic capacitance can produce large frequency variations.

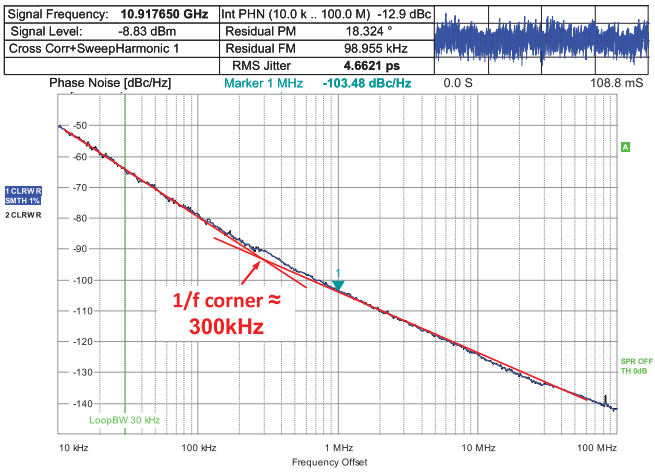

Fig. 14. Transformer-based DCO phase-noise.

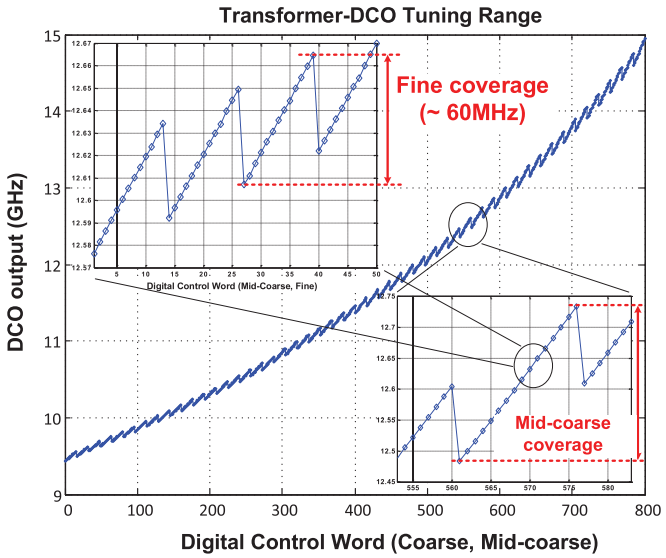

Fig. 15. Transformer-based DCO frequency sweep over coarse, midcoarse, and fine tuning banks.

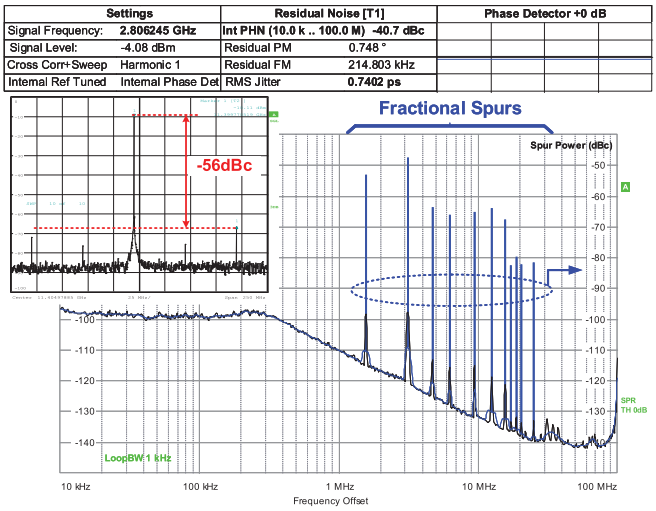

Fig. 16. Phase noise and spectrum closed-loop of transformer-based ADPLL.

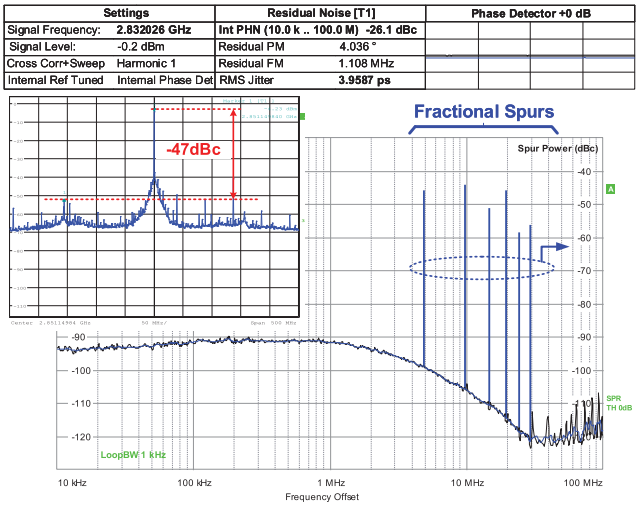

Fig. 17. Phase noise and spectrum closed-loop of RO-based ADPLL.

The Q-factor of the LC-tank (i.e., the transformer and switched capacitor banks) stays relatively constant at around 6 over the tuning range. The open-loop PN at 10.9 GHz is plotted in Fig. 14 and corresponds to the midpoint of the control tuning word. Fig. 15 demonstrates the continuous tuning range coverage of the transformer-based DCO. Sufficient overlap over the different banks (coarse, midcoarse and fine) guarantees the proper ADPLL locking sequence. The coarse bank is binary-weighted for easier implementation, while the midcoarse and fine banks are switched in a thermometer way, guarantying monotonicity and tracking of voltage and temperature variations.

Both ADPLLs operate at a regular 1.1-V supply, while the transformer-based DCO operates at a 1-V supply, in order to optimize its FoM and to allow operating in the lower frequency span. Both ADPLLs can support a wide range of reference frequencies (20–200 MHz), but for the following results, crystals of 100 and 156.25 MHz are used as references, for the transformer-based and RO-based ADPLLs, respectively. Both support the fractional-N operation, using identical feedback loops (look-ahead TDC and divider-by-2), with an exception of the extra divider-by-4 (CML) for the transformer-based configuration. Fig. 16 plots the PN and spectrum of the transformer-based ADPLL, with highlighted spurs and after division-by-4, to relax the measurement buffers. In the inset, the spectrum is also shown and the reference spur could be inferred. For comparison, the PN and spectrum of the RO-based ADPLL are plotted in Fig. 17. The fractional FCW for those cases were set to 14.03125 and 9.0625, which correspond to 112.25 and 18.125 for the transformer-based and RO-based ADPLL, respectively, since the feedback loop effectively operates at CKV/8 and CKV/2.

The above measurements were repeated at various FCW values (both in integer-N and fractional-N). A plot of the integrated RMS jitter and integrated FoM jitter ($\text{FoM}_{\text{jitter}}$) is shown in Fig. 18. The $\text{FoM}_{\text{jitter}}$ characterizes the frequency synthesizers in terms of jitter-power trade-off, which has been

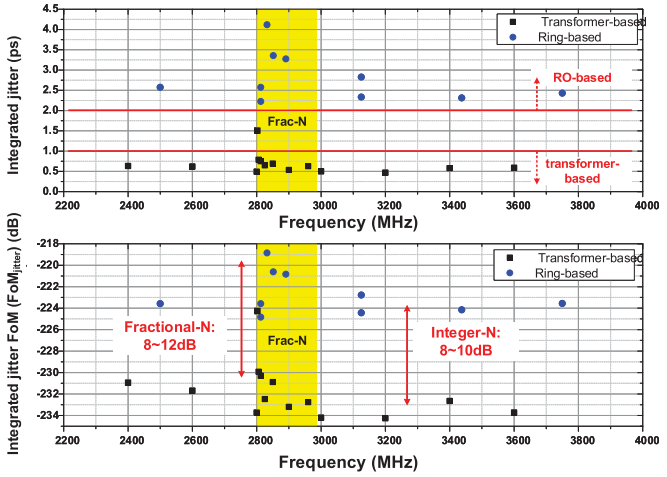

Fig. 18. Integrated RMS jitter and $\text{FoM}_{\text{jitter}}$ comparison for RO (raw CKV) and transformer-based (CKV/4).

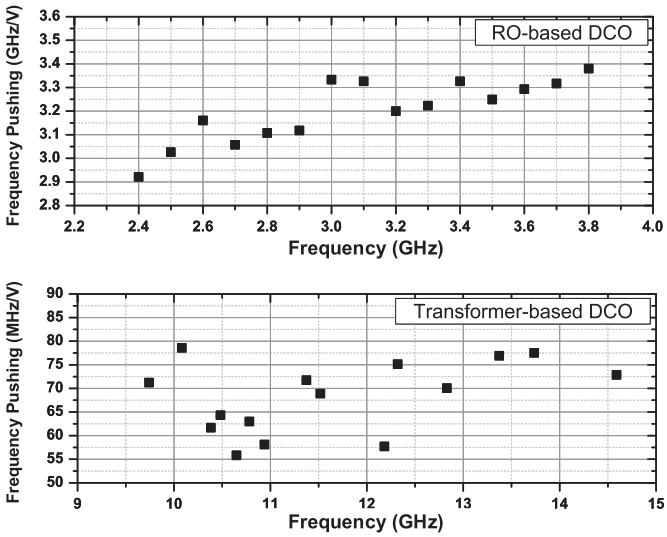

Fig. 19. DCO frequency pushing comparison of RO (top) and transformer-based (bottom).

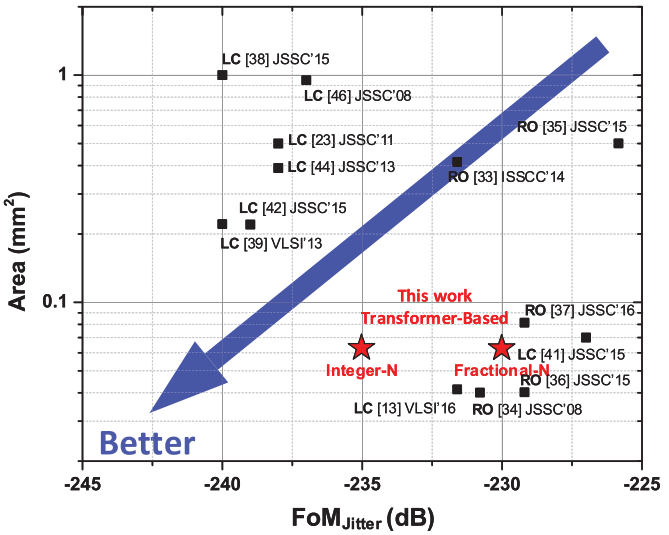

Fig. 20. $\text{FoM}_{\text{jitter}}$ over area for recent state-of-the-art fractional-N PLL.

introduced by [31], as the product of jitter variance σ_t^2 and the power consumption in mW, defined as

$$\text{FoM}_{\text{jitter}} = 20 \cdot \log_{10}\left(\frac{\sigma_t}{1\ \text{s}}\right) + 10 \cdot \log_{10}\left(\frac{P_{\text{dc}}}{1\ \text{mW}}\right). \quad (6)$$

A quick inspection of Fig. 18 reveals a significant performance improvement of the proposed transformer-based ADPLL over the traditional RO-based ADPLL: 8 dB better $\text{FoM}_{\text{jitter}}$ for integer-N channels and 12 dB better for fractional-N channels.

The worst case reference spur was measured at −56 and −47 dBc for the transformer- and RO-based ADPLL, respectively. Since the dominant fractional spurs are caused by the TDC nonlinearity, they experience a regular low-pass filtering by the ADPLL loop filter. However, the fractional spurs falling within the loop bandwidth (e.g., in case of a very small fractional FCW setting) cannot be attenuated so the two ADPLLs report the worst case in-band fractional spur of −35 dBc. When not operating at such very small fractional FCW values, the maximum integrated jitter (from 10 kHz to 100 MHz) was measured at 0.74 and 4 ps_{rms} for the transformer- and RO-based ADPLL, respectively. However, when the in-band fractional spurs are present, the maximum integrated jitter increases to 1.5 ps_{rms} for the transformer-based ADPLL.

A comparison of the $\text{FoM}_{\text{jitter}}$ shows that our RO-based ADPLL is the best in its class and our transformer-based ADPLL provides an additional 11-dB improvement, being comparable in performance to similar-area *LC* PLLs [13], [41] and only 8–10 dB worse $\text{FoM}_{\text{jitter}}$ than the best-in-class, but of large-area, wireless (narrow-band) *LC* PLLs [38], [39]. Moreover, important parameters, such as frequency pushing (not universally reported), which can be translated as frequency sensitivity to its supply, is intrinsically superior in *LC* tank DCOs (and also in our case) than in any RO-based. A high frequency pushing would normally require massive filtering (i.e., large silicon area of LDOs) to compensate for it, thus reducing the area advantage [34]. Fig. 19 shows the measured frequency pushing of both circuits over frequency. The measured frequency pushing of the transformer-based DCO was 80 MHz/V (0.8%/V), which is far more robust than the RO-based, found to be around 3.2 GHz/V (100%/V), being only acceptable if a state-of-the-art LDO is used to supply it [43], which can provide maximum of −54 dB PSRR (at 100 kHz) with area penalty.

The $\text{FoM}_{\text{jitter}}$ performance of the proposed transformer-based ADPLL is compared in Fig. 20 to recent state-of-the-art fractional-N synthesizers. It reports the smallest area among all PLLs (analog or digital alike and wide or narrow tuning range) and a very good $\text{FoM}_{\text{jitter}}$ (<−230 dB). Thus, the proposed miniaturization process proves to be very efficient, with a relatively small impact on $\text{FoM}_{\text{jitter}}$ when compared to high-end PLLs.

Table I provides a comparison between state-of-the-art RO-based frequency synthesizers. Serving simply as a reference, this RO-based PLL offers similar jitter performance as [32] and similar area, with much larger tuning range and

TABLE I
STATE-OF-THE-ART COMPARISON TABLE FOR BOTH ANALOG AND DIGITAL RO-BASED FREQUENCY SYNTHESIZERS

	This Work	Kao [32] ISSCC'13	Marucci [33] ISSCC'14	Tierno [34] JSSC'08	Nandwana [35] JSSC'15	Tsai [36] ISSCC'15	Elkholy [37] JSSC'16
Technology [nm]	40	40	65	65	65	16	65
Architecture	Dig-PLL	Ana-PLL	MDLL	Dig-PLL	Ana-PLL	Dig-PLL	Dig-PLL
Area [mm^2]	**0.052**	**0.055**	**0.4**	**0.03**	**0.48**	**0.029**	**0.084**
Output freq. [GHz]	2.4-3.8	1.9-2	1.6-1.9	0.5-8	4.25-4.75	0.25-4.0	2.0-5.5
Tuning range [%]	45	5.7	17	66	11	67	67
Reference [MHz]	20-200*	26	50	125-500	50	50-200	50
Loop bandwidth [MHz]	0.7-10	2	N/A	1.25-5	12	2	5
Integ. RMS jitter [ps]	2.3 | 4	3.4	1.4	0.7[4]	1.5	1.22 | 3.48	1.9 | 3.6
Power consump. [mW]	6.5-8.5	9.95	3	17.2	11.6	3.9-9.3	1.35-4
DCO Supply Voltage [V]	1.1	2.5	1.2	0.5-1.3	1.0	0.52-0.8	0.7-0.9
$\mathrm{FoM_{jitter}}$ [dB]	**-220 | -218**	**-219**	**-232**	**-231**	**-225.8**	**-228 | -223**	**-229 | -228**
Reference spur [dBc]	-47	N/A	-47	N/A	-60	N/A	-44
Worst fract. spur [dBc]	-35+	-50	-47	N/A	-50	-31.2	-41.6
Freq. pushing [MHz/V]	**3200 (100%/V)**	**N/A**	**N/A**	**8000 (100%/V)**	**N/A**	**N/A**	**N/A**

* Results using 156.25 MHz crystal.
+ In-band spur.

TABLE II
STATE-OF-THE-ART COMPARISON TABLE FOR BOTH ANALOG AND DIGITAL *LC*-BASED FREQUENCY SYNTHESIZERS

	This Work	Raczkowski [38] JSSC'15	Ahmadi [39] VLSI'13	Venerus [40] JSSC'15	Lee [41] JSSC'15	Elkholy[42] JSSC'15	Li [13] VLSI'16
Technology [nm]	40	28	40	65	28	65	10
Architecture	Dig-PLL	Ana-PLL	Ana-PLL	Dig-PLL	Ana-PLL	Dig-PLL	Dig-PLL
Area [mm^2]	**0.0625**	**1**	**0.39**	**0.56**	**0.07**	**0.22**	**0.034**
Output freq. [GHz]	9.4-14.8	9.2-12.7	8-12.4	2.8-3.5	2.7-4.5 / 4-7	4.4-5.2	10.8-19.3
Tuning range [%]	45	32	43	22	50-54	16.7	56
Reference [MHz]	20-200*	40	156.25	26	54	50	150
Loop bandwidth [MHz]	0.7-8	1.8	0.5-4.3	0.04	0.35	0.75-3	2
Integ. RMS jitter [ps]	0.5 | 0.74	0.23 | 0.28	0.29 | 0.46	N/A	1.0	0.45 | 0.5	0.725
Power consump. [mW]	12-20	13	16.9	21	14	3.7	11.9
Supply Voltage [V]	1.0 / 1.1	0.9 / 1.8	1.0	1.0 / 1.2	1.8	1.0	0.8
PN (DCO) @ 10 MHz [dB]	-120	-132	-123	-143	-122	-130	-120
FoM @ 10 MHz [dB]	175	181	176	184	168	183	174
$\mathrm{FoM_T}$ @ 10 MHz [dB]	188	192	189	190	182	187	189
$\mathrm{FoM_{jitter}}$ [dB]	**-234 | -230**	**-242 | -240**	**-238**	**N/A**	**-228**	**-240**	**-232**
Reference spur [dBc]	-56	N/A	N/A	-82	N/A	-69	-74
Worst fract. spur [dBc]	-35+	-43	-57	-43	N/A	-51.5	-30
Freq. pushing [MHz/V]	**80 (0.8%/V)**	**200 (1.8%/V)**	**N/A**	**N/A**	**N/A**	**N/A**	**250 (1.7%/V)**

* Results using 100 MHz crystal.
+ In-band spur.

lower supply voltage. This implementation provides a much smaller area than [33] due to the fully digital approach, in contrast to the use of DACs in [33]. In [34], a more compact ADPLL with a better jitter performance is presented, yet it is implemented in SOI technology and can only provide integer-N channels along with a fixed number of programmable frequency steps.

Table II shows the performance comparison between state-of-the-art *LC*-based frequency synthesizers. Our proposed solution is the smallest, except for [41] which occupies almost the same area. Our solution has moderate jitter performance (in general 10 dB worse than high-end solutions), since it was compromised while trading for the area.

VI. CONCLUSION

This paper offers a very efficient way to tradeoff area with jitter in frequency synthesizers, while keeping power efficiency best-in-class. To do so, the proposed solution picks advantages of both worlds, from the superior *Q*-factors of *LC* tanks to the small size and wide tuning range of ROs. The transformer-based ADPLL is only 20% larger than the

RO-based ADPLL, but provides at least 11 dB better $\text{FoM}_{\text{jitter}}$, while offering much higher robustness to supply variations and to common-mode magnetic field interference, which is highly desirable in SoCs, thus providing a very good frequency synthesizer solution suitable for wireless as well as wireline communication systems. A convenient comparison between the two ADPLLs (i.e., RO and the proposed transformer-based DCO) is possible due to the almost identical digital loops, same input reference frequency range (20–200 MHz), loop bandwidth configuration and output frequency of RO and transformer-based DCO (divided by 4).

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