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***Abstract*—The trend to 3D and heterogeneous integration enable driving multi-functional blocks in one package. Flip-chip integration is currently playing an important role and is based on solder joints. To overcome the limitations of solder joints, all-copper interconnects have been investigated to meet electrical, thermal, and reliability demands in 3D integration. The underfill process is widely applied in flip-chip encapsulation technology. We propose a novel wafer-scale all-Cu interconnect method combining epoxy-based photo-patternable polymer as self-aligned underfill layer with the patterned copper nanoparticles interconnects. The resulting test wafers were able to pattern 20 µm pitch copper nanoparticle-paste interconnects on both substrates with and without photoimageable polymer. The Cu paste was applied to form the interconnects and was sintered after bonding process. Free-standing nanocopper is sintered to obtain mechanical properties with a Young's modulus of 112 GPa. All-Cu interconnects with diameter of 50 µm and 100 µm were measured to achieve the specific contact resistance, ranging from 1.4×10^{-5} Ω·cm^2 to 1.0×10^{-5} Ω·cm^2 at different sintering temperature when epoxy-based underfill existing. And its resistivity was 4.54×10^{-4} Ω·cm, compared to 5.86×10^{-4} Ω·cm for the all-Cu interconnects without underfill.**

Keywords—copper nanoparticles, flip chip, underfill, epoxy-based photoresist, all-Cu interconnects

I. Introduction

3D System in Package (SiP) and heterogeneous integration (HI) technologies enable to integrate more multi-functional blocks to support more-than-moore packaging technologies [1]. The conventional approach for chip-to-wafer and chip-to-chip integration is solder-based flip-chip technology, however, it has disadvantages of restricting height, reflow issues and re-melting at high temperature. Therefore, solder cannot satisfy advanced electronics devices and packaging technologies [2]. To mitigate these issues, silver and copper nanometallic materials have been proposed to replace solder. The metallic nanoparticles have been attracting researchers' attention as the interconnecting material, which has the advantages of better no melting properties and higher thermal conductivity [3]. Compared to silver, Cu has lower electrical conductivity and is less expensive [4]. Copper nanoparticles (nano-Cu) sintering occurs at low temperature and doesn't reflow and melt at high temperature. The nano-Cu joint integration technology is one of the potential solutions to replace solder [5]. Hence, nano-Cu joints showed a high shear strength under 15 MPa at 400 °C [6]. Therefore, enabling all-Cu interconnects with nano-Cu joints and investigating to enhance the fine-pitch interconnections is worthwhile.

Moreover, during processing, the nano-Cu pillars have a nanoporous structure that can be compressed during bonding to provide a uniform standard height. Therefore, it can be used for very precise alignment and integration techniques also for harsh environment applications. To investigate the fabrication process of nano-Cu patterning, the lithographic stencil printing (LSP) process is further investigated to transfer the nano-Cu pattern at wafer-scale, which has the advantages of high throughput and high resolution [5]. The photoresist acts as the stencil mask, and a photoresist lift-off process is applied to remove the photoresist stencil and excess Cu-paste.

Often, flip-chip technology is combined with underfill technology, because it can significantly reduce the CTE mismatch and enhance the reliability of solder joint [7]. Furthermore, underfill has the advantages of improving the adhesion between chip-to-substrate (C2S) and redistributing the thermal stress to reduce the solder strain and enhance the solder joint lifetime [8]. Conventionally, capillary underfill technology is applied after the solder bonding by injecting the underfill materials in the cavity between the chip and the substrate [9]. A no-flow underfill was invented by Wong *et al.* to simplify the conventional underfill technology, when applying specific underfill materials with the properties of reaction latency and flux-ability [10]. Gilleo *et al.* proposed the molded underfill (MUF) to encapsulate the flip-chip and molding compound at the same time [11]. However, the underfill process reduce throughput and requires specialized equipment.

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This report presents a novel wafer-scale all-Cu interconnecting approach using the LSP process for nano-Cu patterning combined with photopatternable polymer underfill. sample A was first applied to form free-standing nano-Cu bumps on dummy wafer for LSP test and nanoindentation test to investigate the mechanical property characterization. Sample B was fabricated using regular LSP process to demonstrate the normal LSP printing capable of pattern 20 μm pitch copper nanoparticle-paste interconnects for heterogeneous integration. For improved integration reliability, sample C proof a concept that an epoxy-based photoresist was applied not only as a lithography stencil mask but also as a permanent underfill material self-aligned with patterned nano-Cu interconnects to combine precise patterning and underfill together.

II. Nano-Cu Joint Patterning and Test Structure

A. Photolithographic Nano-Cu Patterning

To investigate the LSP and sintering procedure for nano-Cu paste, a dummy free-standing nano-Cu pillars were fabricated in the first stage. We prepared the dummy sample A, as illustrated in Fig. 1. The first step is to grow 300 nm of low-stress silicon nitride (SiN_x) as an insulating barrier layer on a silicon wafer by low-pressure chemical vapor deposition (LPCVD), and then sputter-coat a 300 nm Cu interconnect layer as a "substrate wafer".

For sample A, a Ti/TiN (25 nm/2 nm) was sputter-coated on the substrate wafer as adhesive and insulting layers, subsequently, spin-coated by 10 μm AZ®-12XT photoresist. The photoresist was exposed and developed as shown in Fig. 1(a). Next, the nano-Cu paste is distributed by a silicon squeegee manually to fill the gaps between the photoresist (Fig. 1(b)). The nano-Cu paste spread wafer was dried in an oven at 110 °C for 15 minutes. The lift-off process is applied under agitation by N-Methyl-2-pyrrolidone (NMP) to strip the photoresist. This LSP for sample A (Fig. 1(d)) was completed after rinsing by DI water. The resulting wafer after nano-Cu patterning process was diced into 10×10 mm^2 dies. A typical resulting nano-Cu transferring pattern is demonstrated in Fig. 2. After LSP process, the formation of micron sizes ranging from 20 μm to 100 μm was achieved using a silicon squeegee.

B. Nano-Cu Interconnects Test Vehicle Design and Fabrication

Fig. 3(a) shows an overview of the test vehicle in this experiments. We fabricated two types Si wafers, one designed as 10×10 mm^2 dies as bottom wafer, and another one designed

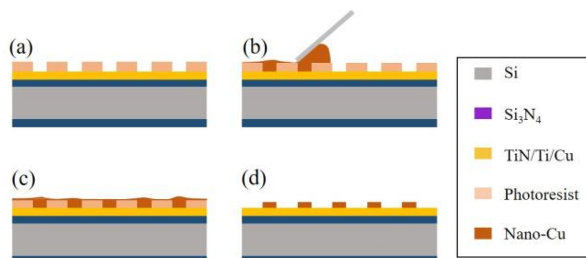

Fig. 2. A overview of the patterns transferring process using photolithography stencil printing for sample A.

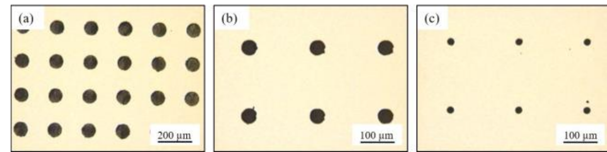

Fig. 1. Microscopy images of test examples of photolithographic pattering under sub-micro size.

as 6×6 mm^2 dies as top wafer, both first following the procedure for "substrate wafers" described in the previous section. Then, the substrate wafers were deposited with 300 nm Cu though sputtering and then patterned through lithography and wet etching process. The etchant solution ($Na_2S_2O_8$ (1 wt%) H_2SO_4 (0.25 wt%) H_2O) was mixed for bulk Cu etching. After nano-Cu patterning procedure, the 6×6 mm^2 chips were flipped and aligned onto 10×10 mm^2 bottom chips to form the test vehicle containing Cu pads, redistribution layer (RDL) and nano-Cu interconnects.

The test vehicle is consisting of daisy chain (DS), cross-bridge kelvin structure (CBKS) and sheet resistance with pressure and without pressure. The patterns of Cu pads are symmetrical on the top and bottom dies. For the DS and CBKS structure, the nano-Cu bumps form rectangles and circles with diameters of 10, 20, 40, 50, 100 μm, and the pitches of DCs are 20, 40, 80, 100 and 200 μm. The sheet resistance can be measured by the Greek cross, a special Van Der Pauw (VDP) structure, in cross area of 50 μm^2. To compare the sheet resistance between the pressureless and pressure-assisted sintering processes, two Greek cross structures were located outside and inside the top chip area, respectively.

C. Free-standing Nano-Cu Joint All-Cu Interconnects

To investigated the LSP process on test vehicle structure, free-standing nano-Cu bumps were first formed on the test bottom wafer, as sample B, and the process flow is illustrated in Fig. 4. The photoresist was spin-coated on the test bottom wafer with the test vehicle pattern and exposed to open the areas on the Cu pads for contact with nano-Cu, as shown in Fig. 4(b). As in the LSP process described previously, on the resulting chip, nano-Cu patterns were in contact with the Cu pad to provide interconnections (Fig. 4(e)). Fig. 5(a) demonstrated the resulting test bottom wafer after nano-Cu pattern formation.

The nano-Cu pattern were defined by the photoresist stencil mask being derived from lithographic reticle. The patterned Greek cross sheet resistance structure is shown in Fig. 5(b) and the finest pitch approach using this method was 20 μm for both rectangular and circular nano-Cu interconnects, as illustrated in Fig. 5(c) and (d) showing 2D and 3D optical images using a 3D profilometer (Keyence VK-X250), respectively. The height of pattern was resulted from the thickness of the applied photoresist. The surface profile of 20 μm DC structure with nano-Cu interconnects was observed by a 3D profilometer, as shown in Fig. 5(e), where the yellow and purple dashed line

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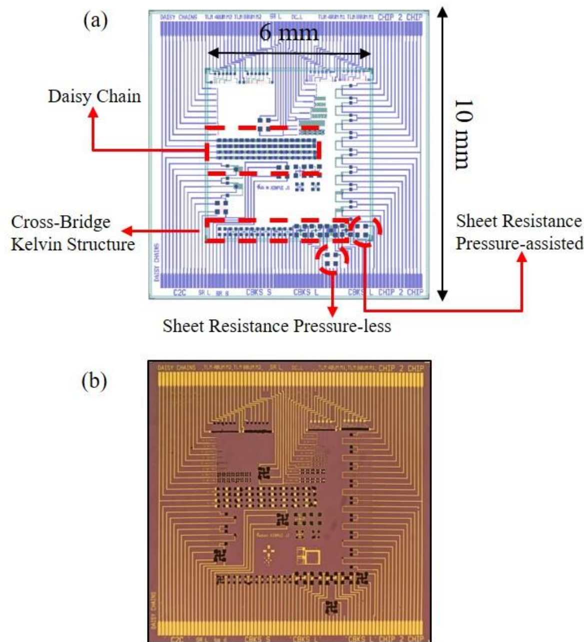

Fig. 5. Layout of test vehicle for (a) screen shot and (b) microscopy image of nano-Cu patterns

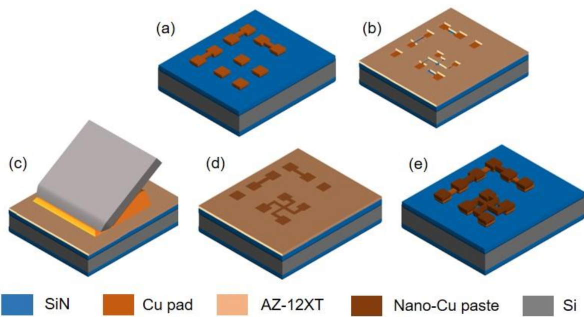

Fig. 4. A overview of the patterns transferring process using photolithography stencil printing for sample B.

represent the horizontal height of Cu pads and wafer substrate, respectively. The height of the nano-Cu pillars was estimated from the height difference between the highest point of the profile and the substrate to be 8.06±0.22 µm.

D. *Photopatternable Underfill Combined All-Cu Interconnects*

Underfill is widely used in packaging technology, and the process is usually performed after the flip-chip pick-and-place step. To alternate the conventional underfill process, we use PermiNex® 2015 purchased from Microresist Technology, which is an epoxy-based photo-patternable photoresist, to combine the interconnect and underfill process. The PermiNex® 2015 is a negative photoresist, hence, its lithography reticle for opening contact area of nano-Cu pattern is inverted from the previous section. According to the previous process, we can estimate the compressed thickness of nano-Cu after sintering and determine the thickness of the photoimageable underfill

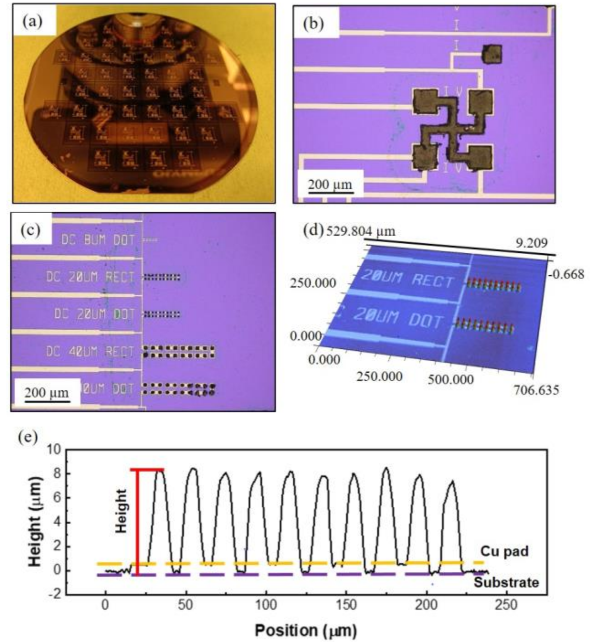

Fig. 3. Test bottom pattern obtained after LSP process. (a) Wafer-scale nano-Cu pattern shown in the dark non-reflected area, (b) Greek cross nano-Cu pattern used for sheet resistance measurements, (c) and (d) representing the resulting 2D and 3D information, and (e) surface profile of the nano-Cu bumps.

layer and photolithographic stencil mask thickness. The process flow combines lithography stencil printing and photoimageable underfill, as shown in Fig. 6. After the Cu pad fabrication step (Fig. 6(a)), the prepared test bottom wafer, containing the 10×10 mm^2 chips, was first spin-coated with PermiNex® at 8000 rpm, followed by photolithography/exposure to obtain the self-aligned underfill layer (Fig. 6(b)), which can be observed under microscopy, as shown in Fig. 7(a) in viewing of 10×10 mm^2. The laser and optical image of the Greek cross on this chip is illustrated in Fig. 7(c), where the red arrow indicates the profile of underfill layer in Fig. 7(e), approximately 12.8 µm. Sequentially, photoresist AZ®-12XT was applied to achieve a second layer as a stencil mask layer on the underfill layer (Fig. 6(c)). Fig. 7(b) demonstrated the optical image of resulting chip after bi-layer photoresist process, where the Greek cross structure is characterized by profliometer, as shown in Fig. 7(d). Fig. 7(f) depicts the opening contact profile of bi-layer photoresist, indicated by blue arrow in Fig. 7(d). The depth of opening contact area for bi-layer process is approximately 19.0 µm. For the wafer with bi-layer photoresist, the steps in the LSP process were repeated in this modified process (Fig. 6(d) - (f)).

Fig. 8 indicates the defined nano-Cu patterns retained on the resulting wafer (sample C) using the Perminex® underfill for sequential bonding process. Fig. 8(a) and (b) show the optical and laser images of specific area of the fine pitch DC structure and CBKS structure, respectively. It can be observed that the background photoresist protrudes at the area of Cu pattern. It is attributed to weak adhesion between bulk-Cu and PermiNex®. Furthermore, there is a corrugated optical reflection outside the dark nano-Cu area under laser inspection due to the transparent

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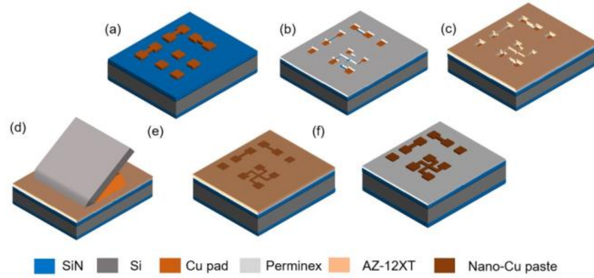

Fig. 6. A overview of the patterns transferring process using photolithography stencil printing and Perminex as underfill for sample C.

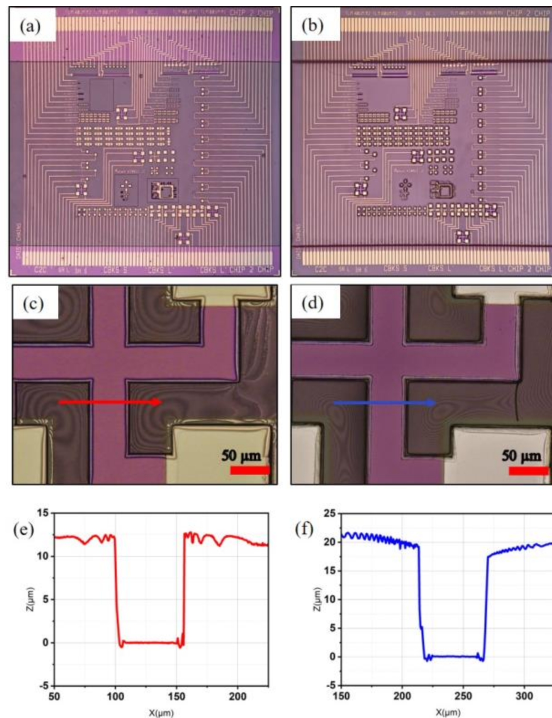

Fig. 7. Microscopy images of (a) and (c) self-aligned underfill pattering process, (b) and (d) bi-layer photoresist patterning. (e) The profile of the thickness of PermiNex® layer indicated at the red arrow in (c) and (f) the profile of the bi-layer thickness indicated at the blue arrow in (d).

photoresist. Hence, Keyence profilometer cannot measure the profile of nano-Cu bumps. We use Dektak surface Profiler to characterize the surface topography of nano-Cu bumps and underfill. The height between surface of underfill and the surface of nano-Cu patterns can be measured and indicated in Fig. 8(c). It can be observed that the side well is higher than the middle of the nano-Cu due the shrinkage of nano-Cu paste during drying. The highest points between the surface of underfill and nano-Cu pillar are ranging from 5.47 to 7.75 µm, hence, the height of nano-Cu pillar using LSP combined with Perminex® is estimated to be 19.41±1.14 µm.

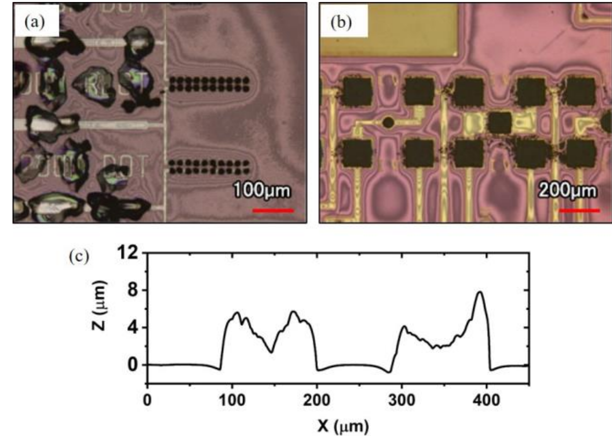

Fig. 8. Optical and laser microscopy images of (a) DCs with 20 µm pitch and (b) the CKBS structure after LSP process with PermiNex®, and (c) the surface profile of the patterned nano-Cu and underfill layer.

III. SINTERING AND INTEGRATION

For flip-chip bonding process, top wafer and dies were fabricated in this step. sample A, B and C required two types of top wafers, the one was bare Si wafer diced into 6×6 mm^2 dies, and another one was patterned with 6×6 mm^2 Cu pad with test vehicle as described in test vehicle design.

Tresky die-Bonder (T-3000-PRO) was applied to align the chip-level flip-chip, and due to the limited pressure available, 1.5 MPa was applied during the bonding process with nitrogen flow. AML waferbonder was used for wafer-level and high pressure bonding, which provided a vacuum environment (below 10^{-3} mbar) to prevent nano-Cu from oxidation.

The sintering parameters of this experiment are demonstrated in Table I. Firstly, the top bare Si die was flipped onto the sample A with nano-Cu bumps without Cu pads and

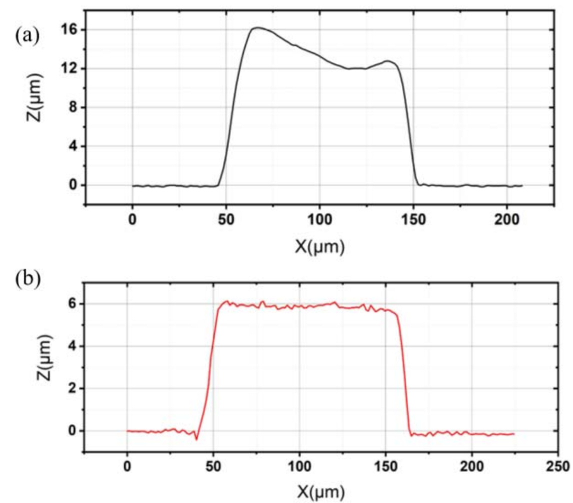

Fig. 9. The profile of the nano-Cu bump (a) before sintering and (b) after sintering.

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RDL interconnects for C2C bonding. After that, the stacked chips were transferred to an AML waferbonder for nano-Cu sintering with a pressure of 20 MPa at 260 °C for 15 mins under vacuum.

Then, the top wafers with Cu pad patterned 6x6 mm^2 sized of chip were flipped and aligned with samples B and C using AML-Bonder and Tresky die-Bonder. The sample B without underfill layer was treated at the temperature of 280 °C under 1.5 MPa for 1 hour. And the stacked sample C with nano-Cu pattern combining with Perminex® layer was bonded with a pressure of 1.5 MPa at 220 °C and 280 °C for 1 hour.

TABLE I. SINTERING PROCESS PARAMETERBLE

Parameter	Process Sample			
	Sample A	*Sample B*	*Sample C*	
Pressure (MPa)	20	1.5	1.5	1.5
Temperature (◦C)	260	280	220	300
Time (min)	15	60	60	60

IV. SINTERED NANO-CU CHARACTERIZATION

A. Mechanical Characterization (Sample A)

The mechanical behavior of sintered nano-Cu is the mechanical deformation, hereby we performs a assessment of the mechanical behavior by nano-indentation measurement. The bonder sample A was applied for the mechanical property investigation. The top Si die on sample A was first peeled off from the bottom die to obtain the sintered nano-Cu for further experiment. Fig. 9(a) and (b) represent the height profile of nano-Cu before and after sintering process, estimated to be 13.57±2.65 µm and 5.86±0.27 µm, respectively. The nano-Cu is compressed and flatten after sintering process. The cross-section of the sintered nano-Cu was obtained by SEM-FIB milling (Helios G4 CX, FEI) to indicate the nanostructure of the sintered nano-Cu pillar, as shown in Fig. 10(b). It can be observed that the sintered nano-Cu have a porous structure and the sintered necks form significantly a network of nanoparticles. The compressed nano-Cu pillar was estimated to be 5.801 µm through the cross-sectional SEM image.

The surface of sintered nano-Cu illustrated in Fig. 10(a) were characterized by a Hitachi Regulus 8230 scanning electron microscope (SEM). A diamond Berkovich tip indenter was loaded onto the surface. The nanoindentation test were conducted in the Nano indenter G200 at the room temperature. We performed the continuous stiffness measurement (CSM) to characterize the continuous change of Young's Modulus with depth [12]. Fig. 11 shows the nanoindentation results of the CSM of the indenter from the sintered nano-Cu surface to 2 µm, and the valid data range was set from 0.5 to 1.8 µm in the equipment system. The elastic modulus of sintered nano-Cu can be calculated from the average value of the valid data and is estimated to be 112 GPa, compared to 128 GPa for bulk Cu [13].

B. Electrical Characterization (sample B and C)

For flip-chip integration, the electrical property plays an important role in nano-Cu joint interconnects. As previous sections described, the contact resistance is the key parameter to nano-Cu joint integration interconnects. In this experiment, the resistance of the sintered nano-Cu was measured by a Cascade Microtech probestation.

The contact resistance is measured on the sample C coated with Perminex® and bonded at 1.5 MPa at 220 °C and 300 °C. After LSP process, the CBKS's were formed to characterize bulk-Cu on the bottom substrate, nano-Cu film and bulk-Cu on the top substrate contact resistances using four-point measurement. The specific contact resistances were calculated by measuring the contact resistance for contact area sizes of 50x50 μm^2 and 100x100 μm^2. The test CBKS structure is indicated in Fig. 8(b). With the increase of sintering temperature from 220 °C to 300 °C, the specific contact resistances of 50×50 μm^2 and 100×100 μm^2 decreased rapidly from 1.4×10^{-5} $\Omega\cdot cm^2$ to 4.6×10^{-6} $\Omega\cdot cm^2$ and 4.6×10^{-5} $\Omega\cdot cm^2$ to 1.0×10^{-5} $\Omega\cdot cm^2$, respectively. For low pressure sintering process, the sintering temperature plays an important role to determine the specific contact resistance.

Greek cross structures were to characterize the sheet resistance and resistivity of sintered Cu nanoporous patterns using LSP methods with underfill and without underfill. The width of Greek cross is designed as 50×50 μm^2 and the nano-Cu thickness of bonded samples with and without underfill were measured to be approximately 8.06 and 19.41 µm, as mentioned in previous sections. There were two Greek crosses on the test structure, one in the area covered by the top die, providing pressure-assisted sintering, and the other in the area without the top die applying pressure, which was pressure-free sintering, as mentioned in Fig. 3(a). Fig. 13 illustrates the average resistivity illustrates the average resistivity during pressure-less and

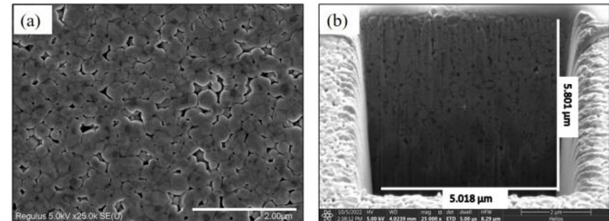

Fig. 10. SEM images of (a) the surface of the sintered nano-Cu bump and the cross-sectional view of the sintered nano-Cu obtained by FIB milling, showing the internal nanostructure.

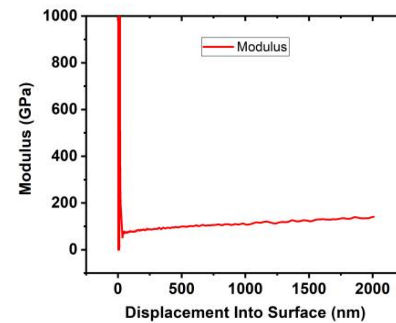

Fig. 11. The elastic modulus of sintered Cu from the surface to a depth of 2 µm.

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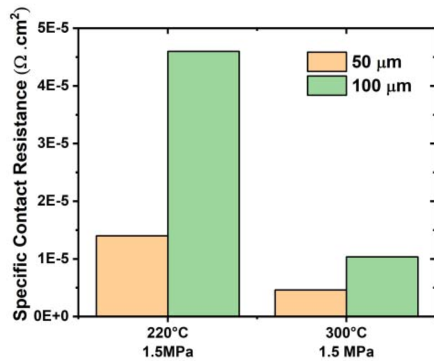

Fig. 13. Specific contact resistance of bulk-Cu/nano-Cu/bulk-Cu sandwich structures at different sintering temperature at bonded pressure of 1.5 MPa.

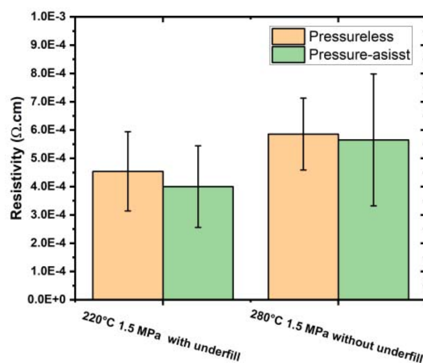

Fig. 12. The resistivity of different process with and without underfill under different sintering parameters.

pressure-assisted processes, indicated by orange and green columns. For the experiments with and without underfill, the resistivity of nano-copper in the pressure-assisted sintering process is significantly lower than that in the pressure-free process, and the pressure aids the sintering process. It can be observed that when sintered at 1.5 MPa, the resistivity of the bonded sample with underfill sintered at 220 °C is 4.54×10^{-4} $\Omega\cdot$cm, which is lower than the resistivity of 5.86×10^{-4} $\Omega\cdot$cm for the bonded sample without underfill at 280 °C. It is attributed to the underfill layer is benefit to planarize the top and bottom substrates and assists in sintering during bonding at lower temperature and pressure. Compared to the resistivity of bulk-Cu of 1.7×10^{-6} $\Omega\cdot$cm, the sintered nano-Cu with underfill is more than 200 times larger.

V. CONCLUSION

In this work, the nano-Cu was applied for the interconnects the patterning process was investigated to enhance the flip chip integration applying for 3D integration. The heights of interconnects are determined by the thickness of applied photoresist. It is feasible to combine epoxy-based photoresist film and LSP process for precise patterning, controllable interconnect height and underfill. The LSP process can provide uniform interconnect heights with different joint sizes.

Mechanical performances were evaluated on sample A using nanoindentation tests to characterize the compressibility of sintered nano-Cu. After sintering, the volume of nano-copper is compressed by 57% compared with that before sintering. The sintered nano-Cu has nanoporous structure with a Young's Modulus of 112 GPa and is more ductile compared to bulk Cu.

The specific resistance of sintered nano-Cu using photoimageable underfill process depends on the sintering temperature, when characterizing sample C. Low specific resistance of bulk-Cu/nano-Cu/bulk-Cu sandwich structure are obtained at sintering temperature 220 °C and 300 °C. The higher sintering temperature results in lower specific resistance at sintering pressure of 1.5 MPa.

The electrical resistivity of sintered nano-Cu is two order larger than that of bulk-Cu, due to oxidation issues and porous structure of sintered nano-Cu. Comparing sample B and C at a sintering temperature of 220-280 °C at a bonding pressure of 1.5 MPa, the underfill combination process facilitates the sintering process to reduce the resistivity. And the resistivity of pressure-less sintered nano-Cu is higher than that of pressure-assisted sintered nano-Cu. The bonding pressure is also a key parameter of sintering process.

Further, the electrical performance need improvement research with focus on the bonding pressure during aligned sintering process and lowering the resistivity. The shear test of flip-chip with and without self-aligned underfill will be investigated to quantify the improvement in flip-chip bonding strength performance by photoimageable underfill combined process. And the oxidization problem will be solved in full-oxidization free environment.

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