

*A FLEXIBLE TRANSPARENT GRAPHENE  
ELECTRODE ARRAY FOR SPINAL CORD  
STIMULATION IN RATS*

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# *A FLEXIBLE TRANSPARENT GRAPHENE ELECTRODE ARRAY FOR SPINAL CORD STIMULATION IN RATS*

By

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## Abstract

Neural interface in the form of microelectrodes is used to monitor and treat spinal cord injury and other neurological disorders by the means of recording and stimulation. Despite the apparent result of these electrical interventions, understanding of the mechanism behind neural stimulation is still inadequate. The use of optical monitoring during implantation is limited due to the use of opaque electrode partially blocking the implantation site. While the use of transparent conductor for an electrode is not uncommon in general electronics where indium tin oxide (ITO) is widely used for displays, however ITO is not suitable for implantation due to its brittle nature[1].

An alternative material to fabricate transparent electrodes is graphene, a single layer of carbon atom forming  $sp^2$  hybridization. Its high charge mobility, flexibility, mechanical strength, and optical transparency make it suitable for various flexible electronics applications including implantable microelectrode arrays. In biomedical fields, graphene has shown potential application as biosensor, stimulation and recording electrode[2].

Although fabrication of graphene microelectrodes has been previously shown[3], graphene had to be transferred manually for each layer. The high temperature needed during graphene deposition makes device fabrication directly on the flexible material impossible. Instead, the fabrication process relies on a transferring process of graphene layer from a growing medium with a high thermal budget to another desired substrate. The manual transfer process of graphene is a skill-dependant process with low scalability.

In this work, a method of fabricating encapsulated graphene electrodes in polydimethylsiloxane (PDMS) with a controlled wafer-scale graphene transfer is proposed. Graphene transfer is done by wafer-assisted PDMS-PDMS bonding. The novel use of PDMS as an encapsulation material for graphene electrode is due to its biocompatibility, flexibility and optical transmittance.

The transferred graphene was patterned on the PDMS by using oxygen plasma. Holes with a diameter of 10  $\mu\text{m}$  was able to be patterned while maintaining the conductivity of the graphene layer. A combination of titanium and aluminium was used as metal contacts, the titanium provides a good contact resistance to graphene layer while aluminium allows wire bonding process to be performed on the contacts.

Difference in material characteristics, such as the thermal expansion coefficient has become one of the challenges during the fabrication process. Despite these challenges, the fabrication process for the electrode array was designed and tested. Conductivity of the patterned graphene layer was tested. The optical transmittance measurement showed up to 77% transmittance was achieved on the graphene encapsulated by PDMS.

# 1. Introduction

## 1.1. Spinal cord injury

A condition when the neural pathways inside the spinal cord are damaged thus disrupting the connection between the brain and the rest of the body can be referred to as Spinal Cord Injury (SCI). This damage can be caused by a trauma or a disease that can cause degeneration of the spinal column (i.e. cancer). Due to the disrupted connection to the brain, a person may lose the sensation and the ability to control their muscle at the area below the point of injury. Depending on the cause and severity of the damage, SCI individuals could experience a partial or complete loss of sensory function or motor control of arms, legs and/or body.

According to the World Health Organization, between 250.000 to 500.000 people suffer SCI every year across the globe, with 40 to 80 cases per million population.[4] Due to the loss of motoric capabilities of SCI patients, the social and economic consequences of this injury is enormous, limiting the patient's ability to contribute in the society in both socially and economically. Patients may lose self-dependency and must rely on caregivers and assistive technology to facilitate mobility, communication and/or self-care. There is also a risk of secondary diseases such as chronic pain, osteoporosis, and urinary tract infection. While SCI is already known for centuries, restorative treatment for SCI is still under development.

Voluntary locomotion normally starts with supraspinal control signals coming from the brain cortex and brainstem. These control signals are descending the spinal tracts and along the way, each tract receives different sensory inputs from all mechanoreceptors and cutaneous receptors. The received sensory information is adapted to the control signal, which allows more effective movements in response to the environment. A Central Pattern Generator (CPG) in the spinal cord converts the non-periodic control signals from the cortex into periodic signals. The periodic control signals propagate to the peripheral nervous system and activate the muscles, which will actuate the locomotion.[5] In patients with SCI, the supraspinal control signals are disrupted or in worst case disconnected. The lack of supraspinal control prevents patients to start the process of voluntary locomotion. However, a study by V.R Edgerton et al. in 2004 suggested that the spinal cord retains its automaticity and plasticity following an injury.[5] Automaticity describes the function of CPG to produce rhythmic outputs in the absence of rhythmic inputs that come from brain cortex[6]. Plasticity refers to the capability of spinal circuitry to regain the voluntary control over muscle through training[7]. Long-term locomotor training has shown the possibility of regaining voluntary locomotion following an incomplete SCI. However, subjects with complete SCI so far were only able to support their partial body weight and unable to perform stepping movement[8]. Stimulation was given to the spinal cord beneath the point of injury. The implant was connected to the dura (protective layer) of the spinal cord. Thus, came the name of Epidural Spinal Cord Stimulation (ESCS).

## 1.2. Epidural Spinal cord stimulation

ESCS was first used as a way to alleviate chronic pain, later its effect to help improving motor functions such as standing and walking was unexpectedly discovered in patients with multiple sclerosis.[9] Unlike ESCS used for pain treatment which is implanted at a varying location depending on the types of pain, ESCS for locomotion recovery is situated more caudally below the point of injury.[10] During ESCS intended for



locomotion recovery, rhythmic electrical signals (typically 25-50 Hz) are induced to the spinal cord. These rhythmic signals have been reported to help activating the spinal cord functionality and generating control signals for locomotion.

Since the process of locomotion is a complex process and given the limitation on direct testing methods on human, little is understood regarding the anatomy spinal tract and the manner of how CPG works. This leads to the lack of understanding of the exact mechanism of ESCS. The mechanism of epidural stimulation recovery is often related to the Hebbian theory similar to the way neurons adapt during the learning process. As the axon of a neural cell is repeatedly communicates with nearby cells, the efficiency of the communication increases due to the growth of new axons or changes in the metabolism. In the case of restoring locomotion after SCI, electrical stimulation provides the necessary signal to activate the CPG function which starts the neural communication. Neuron activities promote axonal regeneration, but despite the fact that synaptic connections to the locomotor network in the lumbosacral region are recovered, the motor capacity is not. [11] Synaptic connections between neurons previously used for locomotion are not enough to regain locomotion. The new synaptic connections with different neurons need to be established to accommodate the difference in the neural circuitry caused by the injury, hence locomotion training is necessary. [12]

Although the exact mechanism of ESCS is not yet well-understood, ESCS has shown positive outcome to recover control of the lost limb. In 2014, Angeli et al. presented a study on four patients with complete motor paralysis for more than 2 years. After attending 80 sessions of locomotor training, voluntary responds were recorded with electromyography (EMG) when patients with epidural stimulation were given a verbal command. Also, they were able to do full flexion and extension of the knee with their own volition. The effect of sensory input in the form of visual and auditory cues were also highlighted when patients were tasked to move a certain part of their bodies such as toe, ankle, and knee in synchrony to the cues[13]. They also managed to match their movement consistently with the cue which signifies the activity of sensory input. In addition, in a long-term study, a patient with complete motor spinal cord injury (AIS B) was observed 18 months following implantation[14]. The patient underwent 170 locomotor training sessions prior to implantation. A 16-electrode array was implanted on L1-S1 spinal cord. After 80 sessions of standing training postimplant, the patient was able to maintain continuous full-weight bearing standing for 4 minutes. Toe, ankle and knee flexion was also possible with epidural stimulation activated. The EMG showed no activity when a similar attempt was performed with the implant deactivated. The patient was reported to regain bladder and sexual function after training and epidural stimulation.

Animal testing has given the community more insight to the study of ESCS due to smaller limitations on treatment paradigms. In animal, the reactivation of CPG through training and epidural stimulation has been proven. Studies performed on rats[15], [16] and cats[17], [18] have shown that spinal animals performed bipedal locomotion on a treadmill with the help of medication, locomotor training, and epidural stimulation.

## 1.3. Electrode Array for Epidural Spinal Cord Stimulation

### 1.3.1. Electrode-electrolyte interface

The idea of inducing an electrical stimulus to the body is the basis of how epidural stimulation works. The process of electrical conduction by definition involves the movement of electrically charged particles called charge carriers. The mechanism of charge transfer depends on the medium in which these are traveling. In metal or semiconductor materials in which stimulation is generated, the charge is carried by electrons. In a physiological medium like that surrounding our nervous system, electrical signals are carried by ions. Positive charges are carried by sodium and potassium ions and negative charges are carried by chlorine ion. In a more general term, a medium that conducts in this manner is called electrolyte.

The transfer of charge from electrons to ions would require an electrochemical process. The apparatus that interface this change of charge carrier is called electrode. In the electrochemical process, there are always at least 2 electrodes to create a circuit, which respectively act as an entry point and return point for the current to flow. Depending on the electrical potential between the electrodes, there are two possible charge transfer mechanisms. When the potential between the two electrodes is relatively small, charge redistribution will occur in the electrolyte with positive ions attracted to the negatively charged electrode and negative ions attracted to the positively charged electrode to maintain net neutrality of the electrode/electrolyte interface. During this process, no electron is transferred from the electrode to the electrolyte. This mechanism is called capacitive/non-faradaic charge transfer. When the potential across the electrodes increases, more charge is transferred. If the net neutrality of the electrode/electrolyte interface cannot be maintained by charge redistribution in electrode/electrolyte interface, the electrolytic cell will be formed. Positively driven electrode causes electrons to be transferred from the electrolyte to the electrode, this process is called oxidation. The reduction is happening at the negatively driven electrode. Electrons are moving from the electrode to the electrolyte, the movement of electrons make up a circuit in which current is flowing from a positively driven electrode to the negatively driven electrode. Due to the transfer of electrons during the reduction and oxidation process, ionization occurs at the electrode. Depending on the electrolyte and the electrode material, irreversible reactions (e.g. corrosion, oxidation, and dissolution) could happen and damage both the electrode and electrolyte (i.e. stimulated tissue). This mechanism is called faradaic charge transfer.[19] The occurrence of non-faradaic and faradaic charge transfer depends on the amplitude of the voltage imposed across the electrodes, the effective surface area of the electrode and electrode material.

### 1.3.2. Requirements for electrodes used in epidural stimulation

There are several requirements that need to be fulfilled during the design process of the electrode. First all there is biocompatibility issue regarding the material involved in the electrode and also during the fabrication process. Biocompatibility relates to the behavior of a living tissue in response to a certain material. A material is said to be biocompatible if it interacts with the host/living system without producing an adverse effect. Biocompatibility tests for medical devices are following a series of standards covered in the ISO 10993. While each individual material used in a certain device may be biocompatible, it does not

necessarily mean that the entire device is biocompatible. Tests according to the standard are needed to be performed to evaluate the possible interaction between materials.

The type of charge transfer happening at the electrode/electrolyte interface is the second important factor as it is related to the long-term reliability of the implant. Capacitive charge transfer is preferred due to the reversibility of the reaction. The irreversible alteration to the electrode and electrolyte during the faradaic charge transfer could change the characteristic of the stimulation and cause harmful effect to the surrounding tissue.[20]

The flexibility of the device is also a concern due to the reliability of the electrodes and comfort of the patient. The electrode array will be exposed to bending movements during surgery and implantation period. Although the damaging movement to the electrodes is minimized, damage to the track can occur which could cause changes to the electrical property. Electrodes need to be flexible in order to avoid hindering the movement of the patient during the implantation period.

### 1.3.3. Neural interface for animal testing

While neurostimulator for a human are readily available in the market, neural interfaces for small animals are harder to find in the market. Due to the difference in anatomy, a neural interface for a human is not compatible for animal testing.

In the past, epidural spinal cord stimulation was performed by using metal wire made of stainless steel coated with Teflon tube as electrodes. The end of the tube would be removed to expose the metal wire to the stimulation site. [16], [21] Although this provides an easy neural interface, better technology was needed to provide more precise and chronic stimulation. The position of the stimulating electrode can only be verified post-mortem[21], thus limiting the accuracy and repeatability of the stimulation.

Multielectrode arrays (MEA) were introduced to replace wire-electrode. MEA provides more flexibility and insight for the stimulation. The location of the stimulation can be adjusted post operation by activating different electrode. The effect on activating different site can also increase the understanding of the response of the spinal cord and locomotion recovery.

## 1.4. State-of-the-art electrode array

### 1.4.1. Fabrication process

Schuetzler et al. proposed the fabrication of microelectrode array using laser-cutting of silicone rubber. The platinum foil was used as tracks, pads, and electrodes.[22] With simple technology, device prototypes can be made inexpensively in a short time with the limitation on feature size of 30  $\mu\text{m}$ . The fabrication process was done on glass carrier with cellophane tape as a sacrificial layer to release the silicone. The silicone layer diluted with n-heptane was spin-coated with approximately 20  $\mu\text{m}$  thickness. 18  $\mu\text{m}$  platinum foil was placed on top of the cured silicone layer. After the patterning process by laser-cutting, another 20  $\mu\text{m}$  thick diluted silicone rubber was spin-coated. The device was released by laser-cutting the perimeter.

Microfabrication is the state-of-the-art fabrication process for electrical devices. In 2011, a parylene-based MEA for spinal cord stimulation in rats was proposed using the microfabrication process.[23] A layer of 5  $\mu\text{m}$  thick parylene-C was deposited on top of a layer of photoresist which was used as a sacrificial layer to release the final structure. A metal layer was deposited on top of the parylene using e-beam evaporation. The metal layer composed of 10 nm of titanium and 200 nm of platinum. Titanium was used as an adhesion layer between platinum and parylene. Patterning on the metal was done using lift-off with photoresist sacrificial layer. Another 5  $\mu\text{m}$  thick parylene was deposited on top to create encapsulation. Openings on the parylene were made using oxygen plasma. Acetone was used to release the device from the substrate. After six weeks of implantation, stress lines were observed on the platinum tracks. Even when the position of the electrodes was fixed to a plate attached to the spine, small movements were enough to damage the tracks. The stress was enough to break the connectivity of the metal tracks, hence causing failure to some of the electrodes.

#### 1.4.2. Challenges

From the fabrication perspective, the main challenge for epidural stimulator is the material used as the electrode and the interconnect. Currently, both electrode and interconnect are predominantly made of metal such as platinum, platinum-iridium and gold[20] As an interconnect, the flexibility of metal depends on the thickness of the material. A sheet of the aluminum plate can be rigid while a sheet of aluminum foil can be bent to a certain degree. Although making a thinner metal layer could solve the flexibility issue of metal interconnect, the conductivity of the interconnect will be reduced as a trade-off.

As an electrode, improvements could be made to facilitate the monitoring of nerves during stimulation through optical means. Currently, the cause and effect relation of epidural stimulation is being monitored electrically using electromyograph (EMG). More insight regarding the mechanism of epidural stimulation can be learned through optical imaging.[3] For this purpose, a transparent electrode is necessary to monitor the stimulation site under the electrode. Although, transparent conductive materials such as indium tin oxide (ITO) can be seen every day in displays and touchscreens, the brittle nature of ITO made it unsuitable for flexible applications such as implantable devices. In addition, the increasing price of ITO due to the high demand encouraged the use of other alternative materials as transparent conductors[1].

#### 1.5. Graphene Potential as a Neural Interface

Graphene is an emerging transparent material made of single/few-layer(s) of a carbon atom. The carbon atoms in graphene are arranged in  $sp^2$  orbital hybridization, with each carbon forming 1  $\pi$ -bond and 3  $\sigma$ -bonds. The most prominent properties of graphene are its mechanical stability due to the  $\sigma$ -bonds and high electrical conductivity due to the  $\pi$ -bonds. As a crystalline structure with only few atoms thick, the graphene possesses a nearly transparent look.

Due to its unique combination of electrical, mechanical and optical properties, interests on using graphene as a neural interface have been shown in the last few years. In the field of biomedical, graphene is being explored for stimulation electrodes, recording electrodes, biosensor, and controlled drug delivery. [2]

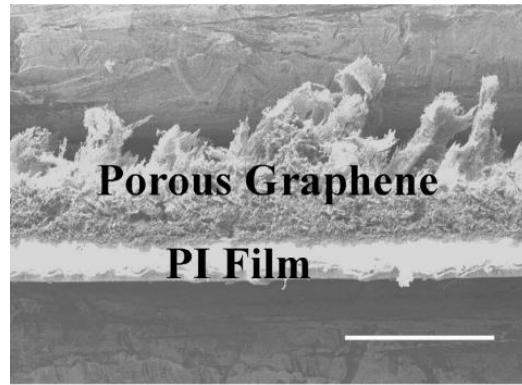
Biocompatibility of graphene and graphene-based materials are still in question. Reviews regarding biocompatibility of graphene-based material have shown evidence of the biological impact caused by graphene-based materials[24], [25], while others suggested that graphene produced by chemical vapor deposition (CVD) did not show any sign of toxicity[26]. Most of the cases of graphene cytotoxicity originate from the biocompatibility study of reduced graphene oxide (rGO). Although rGO and graphene similarly consist of one-atom-thick structure, rGo is comprised of not only carbon but also hydrogen and oxygen atoms. The oxygen content inside rGO caused cells to experience oxidative stress which leads to cells death[25]. Different cells can also react differently towards the oxygen content in rGO. Another study suggested the viability of the usage of graphene-based material including rGo for neural interface coating[27].

The opinions regarding the biocompatibility of graphene and graphene-based materials are still inconclusive and further study is still needed to draw a conclusion. Regardless of the issue of biocompatibility, graphene is still a strong candidate for the future neural interface. While graphene is not ready for long-term implantation, short-term implantation of graphene and other graphene-based materials in animals were already studied[3][27].

## 1.6. State-of-the-art fabrication of graphene electrode array

In 2014, D.W. Park et al. proposed a fabrication process of flexible transparent graphene electrode array using parylene encapsulation[3][28]. This device is intended for neural imaging application on the brain. The fabrication process started with the deposition of parylene-C, gold tracks were deposited and patterned as contact pads and interconnect outside of the recording area. Four layers of graphene were transferred using Poly(methyl methacrylate)(PMMA). Graphene layers were grown using CVD method on the copper catalyst. Finally, another parylene layer was deposited and holes were created using reactive ion etching. In this process, the graphene was transferred layer by layer and stacked on each other. Apart from time consuming, the transfer process using PMMA is prone to contamination of the graphene layer from residual PMMA. The stacking process is also a skill-dependent procedure that can alter the properties of the resulting graphene stack.

Another device was presented by Y. Lu et al. in 2016.[29] The device was used for cortical stimulation and sensing in rats. A porous graphene encapsulated with polyimide was used in this device. The porous graphene is a graphene-like material. Unlike graphene which is considered as two-dimensional material, porous graphene is a three-dimensional material prepared by a laser pyrolysis process (Figure 1). A sheet of polyimide is exposed to CO<sub>2</sub> laser which cause an increase in localized temperature of the polyimide to 2500°C. During this process, the carbon bonds (C=N and C-O) in the polyimide is broken down leaving only carbon bonds. Several electrodes made of porous graphene was then connected by metal interconnect to create an electrode array. While porous graphene provides an easy alternative for depositing graphene-like structure, the nature of the pyrolysis process limits the material that can be used as substrate for the porous graphene.



*Figure 1 Porous graphene on polyimide film[29].*

The study of graphene electrode array fabrication is still underdeveloped. This is logical due to the tender age of graphene discovery. In addition, many fabrication processes still relied on unscalable technique such as transfer method using polymer medium.

### 1.7. The goal and outline of the thesis

The goal of this thesis is to explore the fabrication process of a transparent and flexible electrode array by using graphene as the electrodes and interconnects. The desired electrode array consists of a layer of graphene encapsulated by a polymer as an encapsulation. From the available graphene deposition technique as the starting point, different methods for fabricating the desired device.

The thesis is structured according to the order fabrication process. The designs and its implementations are discussed in chapter 3 and 4. Starting from chapter 5 the fabrication process is discussed. The process started with the graphene deposition which was established before the start of the project. The following chapters will provide the reader with the story and reasoning that lead to the proposed fabrication process. The conclusion of the thesis and recommendation for further study on this project will be provided on chapter 12 and 13.

## 2. Encapsulated Graphene as an Electrode Array

### 2.1. Graphene types

In principle, graphene refers to a single layer of a carbon atom with hexagonal crystal arrangement. While the study of graphene has been dated back as far as 1859 [30], the rise of popularity of graphene was started in 2004 with the study on exfoliated monolayer graphene regarding its extraordinary electrical properties. Graphene was described as a two-dimensional semimetal with zero band gap between valence and conductance band.[31] Atoms in graphene form an  $sp^2$  hybridization, with each atom forms 3  $\sigma$ -bonds and 1  $\pi$ -bond with its neighboring atoms. The  $\sigma$ -bonds are an in-plane covalent bond. The  $\sigma$ -bond is considered the strongest covalent bond with 2 atoms sharing an electron pair with an overlapping atomic orbital. The  $\sigma$ -bonds dominantly contribute to the mechanical properties of graphene. The  $\pi$ -bonds are out-of-plane covalent bonds that form the  $\pi$ -band. In this band, electron flows freely in a phenomenon called surface conduction.

Single layer graphene is the ideal two-dimensional material in terms of electrical and optical performance. A single layer of graphene can have up to  $10,000 \text{ cm}^2/\text{Vs}$  carrier mobility in room temperature[32] with 97.7% optical transparency[33]. Currently, there are still limitations on fabricating uniform and large-scale monolayer graphene, thus multilayer graphene is used instead of monolayer graphene. Kim et al. have studied the electrical properties of multilayer graphene in terms of carrier mobility, density and sheet resistance on different thicknesses of graphene. It has been shown that the thickness does not affect the mobility of the charge carriers, although the charge carrier density is reported to be inversely proportional to a number of the layers due to the fact that charge carriers only generated on the surface of the graphene and only small number of carriers exist in the graphene interlayer. [34] Since density is a measure dependent on volume, the number of graphene layer will increase the volume while the number of charge carrier remains constant.

The simplest way to produce graphene is to use mechanical exfoliation technique. This method was used by Novoselov and Geim in 2004. Graphite consists of layers of graphene bonded to each other by the Van der Waals force. Since the nature of this force is weak, hundreds of graphene layers are delaminated every time graphite is used on the surface of the paper. The idea of mechanical exfoliation is to apply enough force to sever the Van der Waals force between each layer of graphene. In the scotch tape experiment by Novoselov and Geim, the perpendicular force was applied on the surface of graphite. The process was then repeated multiple times on the exfoliated material until a single layer of graphene was obtained. This technique is the simplest way to produce graphene which does not require expensive equipment to produce. Since then, several techniques of exfoliating graphene from graphite was developed involving the use of shear force (ball milling) and sonication in liquid. Although graphene can be produced with this simple method, this process is still far from mass production with low yield, poor repeatability and non-scalable process[35].

Another graphene fabrication process is though epitaxial growth on Silicon carbide. Silicon carbide is a material established by Edward G Acheson in 1890. He was at the time also showed interest on the exfoliation method of graphitic flakes in 1904. Graphene was observed to be forming on the surface of

silicon carbide when exposed to high temperature (up to 2000°C) and low pressure ( $<10^{-10}$  Torr). Due to the extreme environment, the silicon atoms will experience sublimation leaving behind the carbon atoms. The remaining carbon will form a graphene film on the surface, thus the name epitaxial came from. Since this process relies on sublimation of silicon atom due to heat and pressure, strict control over the parameters is necessary to obtain the desired number of graphene stack considering the process is not self-limiting. A uniform distribution of heat is also needed, since gradation of heat over the silicon carbide will cause non-uniform graphene formation and defects such as cracks, folds, and wrinkles. The advantage of using the epitaxial process is the ability to produce a wafer scale process which provides better yield than the exfoliation method. Silicon carbide is also a semiconductor material, hence allowing electronics fabrication on the wafer without the need to switch the substrate. The drawback of the epitaxial growth in the high cost of silicon carbide.

Chemical Vapor Deposition (CVD) graphene is another process of manufacturing graphene. This process starts with a transition metal such as Cu or Ni which will be used as a catalyst. The exact mechanism of this process is different depending on the metal catalyst used. The general idea of the process begins with exposing the metal to a high temperature typically between 800 to 1200°C in vacuum. Gas containing carbon such as methane ( $\text{CH}_4$ ) is then introduced to the metal causing the carbon atoms to be absorbed into the metal bulk or surface. After that, the metal undergoes a rapid cooling which will push the carbon atoms absorbed during exposure to high heat to the surface of the metal. Graphene will be formed on the surface from these expelled carbon atoms.

The CVD process offers more flexibility on the choice of substrate used for graphene deposition compared to epitaxial process. The lower thermal budget is also more desirable giving more freedom on the material allowed during the deposition process. Despite the lower thermal requirement, 800°C is still not compatible with deposition on top of electronics. To incorporate graphene in electronics, methods of transferring graphene to another substrate were explored. These techniques usually involve the removal of the metal catalysts in acids, thus removing the graphene layer from its original substrate. Graphene layers will float on the surface of the acid and the layer then can be scooped out from below by using the substrate which graphene is intended to be on.

A more popular approach of transferring graphene is by using polymers. The polymer is coated on the graphene before removing the metal in acid. Transferring graphene through polymer medium allows more control compared to scooping and opening up possibility to apply graphene without exposing the target substrate to the chemical. The typical polymers used in this process are PMMA and Polydimethylsiloxane (PDMS).

The transfer process starts with graphene layer growth on its metal catalyst. The polymer in uncured condition is coated on the graphene layer, followed by a curing process of the polymer with heat. Covalent bonding occurs between the polymer and the edges of graphene. Later, the entire structure is exposed to acid which etches the metal catalyst. At this moment the graphene layer has two possible interactions with its neighboring layer. The first interaction is Van der Waals bond with the layer underneath the metal



catalyst, typically silicon dioxide. To the layer above, the graphene layer shares covalent and van der Waals bond. Covalent interaction happens at the edges of graphene crystal lattice or grain boundary that occurred due to the imperfection of the CVD process. The nature of covalent bond is stronger compared to the van der Waals force, therefore graphene layers will have the tendency to stay with the polymer medium after the graphene layers are delaminated from the substrate it was grown on. Graphene layer can be applied to a target substrate through stamping (Figure 2), though there is different treatment necessary before the stamping process depending on the type of polymer used. For PDMS, post-curing process before stamping is necessary to weaken the bond to the polymer. PDMS/graphene layer can be put on the intended substrate, and afterwards force can be applied perpendicular to the PDMS surface. This way the PDMS layer can be peeled leaving the graphene layer on the target substrate. For PMMA, an extra chemical step is necessary to remove the PMMA from the graphene because of the stronger bond between graphene and PMMA. Traces of PMMA can remain on the graphene, causing contamination that could lower the conductivity of graphene.[36]

While graphene transfer process can circumvent the limitations on materials contained on the wafer due to high thermal budget necessary for CVD graphene, damage can easily occur during the transfer process which can lower the quality and yield of CVD graphene. Wet chemical processes subjected to the graphene layer have been reported to cause wrinkles and delamination of the graphene layer.[37] External forces applied to the polymer can also cause cracks on the graphene. In addition, damages related to crystal structure can take place during post-curing process because of the thermal stress stemming from thermal expansion difference. The idea of the transfer process, to begin with, is a tug-of-war between forces acting on graphene and its neighboring layers. As mentioned earlier, the force that holds graphene layers together is similar to what occurred to its neighbor which is the Van der Waals force. In the case of multilayer graphene, several layers of graphene might be delaminated from each other due to the interlayer being weaker than the force acting on the original substrate.[37] This could cause non-uniformity of graphene layers after the transferring process.

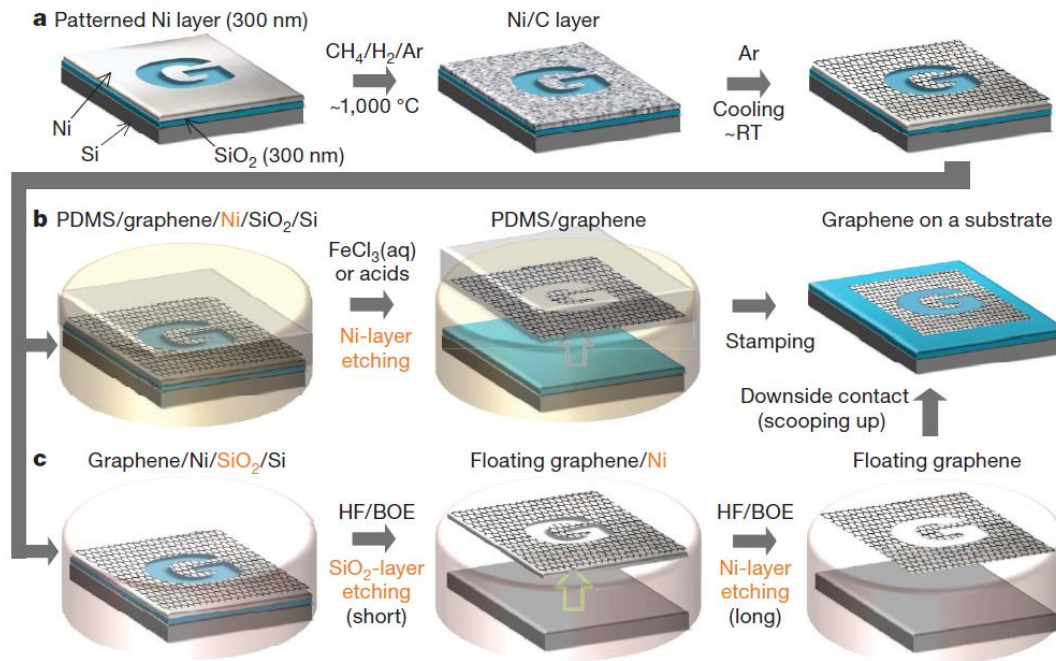


Figure 2 Typical transfer process of patterned CVD graphene[38]

## 2.2. Graphene derivatives

The term 'graphene' is often generalized to refer to other graphitic materials with a structure resembling graphene. Graphene derivatives such as graphene oxide are often referred to as graphene. While these types of material have similar structure based on carbon. The properties of each graphene vary depending on the way it is produced due to possible contamination during the production. Reduced graphene oxide (rGO) is one example of graphene derivatives. The rGO is used as an alternative for mass production of graphene. It is produced from graphite through an electromechanical process called the Hummer's process. The graphite is exposed to strong oxidizer to create graphite oxide and then through sonication, a mechanical exfoliation is performed to create graphene oxide. Graphene oxide in the structure is very much alike to graphene with oxygen atoms connected to the graphene hexagonal crystal structure (Figure 3). These oxygen atoms act as a contaminant to graphene which alters the desirable properties of graphene. Graphene oxide is considered as an electrical insulator due to the disruption of the  $sp^2$  hybridization structure by the oxygen atoms. To reverse the oxidation effect, the reduction is performed to reduce the ratio of oxygen to carbon. The reduction process is typically being done by exposing graphene oxide to a strong reducing agent or hydrogen plasma. Depending on how well the reduction process is performed, the oxygen atom can be completely removed, thus producing pristine graphene. However, this can only be achieved with expensive equipment and only a small amount of pristine graphene can be produced. The rGO has a distinctive form compared to other graphene because the production process of rGO involves strong oxidizer and sonication which results in rGo with smaller grain size compared to graphene produced by CVD and epitaxial growth.

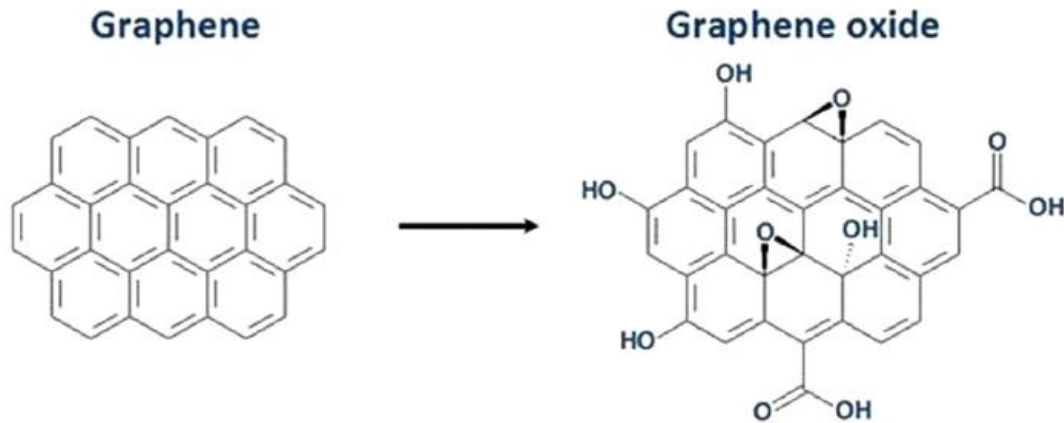


Figure 3 Comparison between graphene and graphene oxide structure[24]

The difference between rGO, CVD, and epitaxial graphene becomes apparent when discussing biocompatibility issues. There are still disagreements regarding the biocompatibility of graphene due to rGO or other graphene-based materials are being related to graphene produced by other means. A biocompatibility study from S. Syama(2016) has shown that rGO produced using Hummer's method was indicating a sign of toxicity because of its high oxygen concentration which produces oxidative stress to the cells.[25] In nanomaterials such as carbon nanotubes (CNT) and graphene, the particle shape is important due to its potential reaction to cells. The size of the nanoparticle is even smaller than the smallest cells, thus small tubular shaped CNT can be seen as a needle that can penetrate the cell membrane and cause toxicity. A similar effect was also observed on rGO with sheets of rGO with smaller mean size having lower cell viability.[25]

A study on graphene produced by the CVD process has indicated that CVD graphene is non-toxic towards L929Fibroblast cells. It was reported to even help the recovery process of damaged tissue.[26] Similar results were reported on a study of cultured human bone cell. The effect of uncovered copper foil to bone cells was compared to a copper foil covered with single-layer graphene and bilayer graphene. Uncovered copper foil showed approximately zero cell viability while foil covered by monolayer and bilayer graphene both showed 100% and 97% cell viability respectively compared to the control group. Toxicity from copper occurred due to corrosion of the copper foil thus causing generation of  $\text{Cu}^{2+}$  ions. The graphene coating was observed to reduce the corrosion effect, therefore it is potentially can be used to prolong the life of metal electrodes. [39]

## 2.3. Polymer for soft encapsulation

### 2.3.1. Soft encapsulation

Similar to CMOS chips, electrode arrays need to be packaged or encapsulated to avoid degradation. From the electronic perspective, the electrode array can be active or passive. In active electrode arrays, encapsulation is important to protect the integrated circuit from being damaged. Although there is no integrated circuit in passive electrode arrays, encapsulation is necessary to prevent damage to the electrode. Corrosion could happen to the metal which typically is used as the electrode. Encapsulation limits the extent of the damage by protecting the area apart from the area that needs to be in contact with the tissue.

The encapsulation allows to do the stimulation selectively. When a certain electrode is activated, only the area corresponds to that electrode is stimulated. Direct contact of the interconnects to the tissue can cause a short circuit between the interconnects, this can also lead to an electrochemical reaction that causes corrosion. A package needs to encapsulate the electrodes from the body, so there is an insulation between each interconnect and electrode.

The spinal cord consists of nervous tissue, extending from the brain stem to the lumbar (abdomen) region along the spinal column. Every motion that involves the movement of the spine will simultaneously impose the movement of the spinal cord. The spinal cord is capable to move with six degrees of freedom, lateral (back and front) bending, side (left and right) bending and side (left and right) rotation. Due to the involvement of the spinal cord during motion, it is imperative that the movement of the spinal cord is unobstructed when a foreign material is implanted on the spinal cord. The electrode array which is used during the ESCS is no exception. As the flexibility requirement of the electrode has been discussed earlier, similarly the encapsulation needs to be made by flexible material to avoid hindering the movement of the spinal cord.

### 2.3.2. Soft encapsulation material

The term soft encapsulation has been used to refer to encapsulation using soft materials. Typically, polymers are used for this purpose. Polymer refers to a chemical structure which consist of a repeating subunit called monomer. The characteristics of a polymer can be completely different from one to another depending on what is the building block that composes it and how long this building blocks is being repeated. For example, polyvinyl chloride (PVC) is a polymer used for making pipes which has opaque color and stiff mechanical characteristic. In contrast, polydimethylsiloxane (PDMS) is a polymer with clear color, it behaves similar to rubber, with low Young's modulus.[40] The polymerization could also affect the properties of a polymer. Polyethylene is a polymer composed of ethylene monomer. Depending on how the monomers are arranged, the density of the formed polymer can be different. Low-density polyethylene (LDPE) is ethylene monomers that were arranged with a lot of branching in the polymer chain with arbitrary length. The resulting molecular structure is more sparsely distributed due to the irregular form of each chain. On the contrary, there is high-density polyethylene (HDPE) which is formed by the same monomer but with less branching and longer straight chains, therefore forming denser molecule groups during crystallization. While LDPE is commonly used in plastic bags, HDPE is often used for an application that requires high tensile strength such as underground pipes and milk containers.

Due to the wide array of properties that polymers could offer, requirements are formulated based on the application. These requirements are used to narrow down which polymer could be used. First and foremost is the biocompatibility issue. The polymer that will be used for encapsulation will be directly in contact with a living tissue during the period of implantation. Flexibility is also one of the main concerns, which is necessary to compensate for the movement of the spinal cord. As mentioned in the Introduction, the use of graphene was partly motivated by the need for transparent electrodes, thus similar optical requirement needs to be fulfilled to encapsulate the graphene electrodes. The encapsulation also needs to be electrically insulating to prevent current leaking from the electrodes.

The use of polymers has been extensively explored for biomedical devices.[41]. As the study of biocompatibility can take years to bear a result, narrowing down the option based on their proven biocompatibility has limited the number of possible polymers. PDMS, polyimide, and parylene-C were commonly used due to biocompatibility reasons. They have been proven to have minimal impact on the body while being implanted.

Compared to parylene-C and PDMS, polyimide is lacking in term of optical transparency. Polyimide typically has a yellow color and optical transparency between 55% to 80% in the visible light spectra compared to 95% of transmittance in the same spectra for PDMS[42] and parylene-C.[43] For flexibility, PDMS has the lowest Young's modulus compared to parylene and polyimide with 0.36- 0.87 MPa. For comparison, Young's modulus of parylene and polyimide are respectively 2760 MPa and 2300 MPa.

PDMS and parylene-C seem to be the suitable candidates for graphene encapsulation. Previous publications suggest that both are suitable to be used with graphene. PDMS has been explored to be used as a medium for graphene transfer process[37], [38] and recently similar attempt on parylene-C has been done to transfer CVD graphene grown on 6-inch wafer.[44] Comparing Young's modulus of both materials, PDMS has an advantage over parylene. The extensive use of PDMS for graphene process provides information regarding PDMS and graphene interaction, hence potentially reducing the time it needs to study the interaction between the graphene and the encapsulation material. With these considerations, the use of PDMS is preferable within this study.

### 3. Design of the electrode array and test structures

The goal of this project is to study the potential application of graphene as a material for realizing electrodes and conductive tracks on an electrode array and to lay a foundation for its fabrication process. The fabrication process starts with the design of the electrode array. This design should be derived from constraints originated from the available fabrication technology and the intended application which in this case is the anatomy and physiology of the implantation subject. The focus of this project is mostly on the fabrication process and not the design of the electrode array. Taking into account the availability of the time and complexity of the project, several considerations to simplify the project were taken with the emphasis on addressing the technological challenges in fabrication. Beside the electrode arrays, some test structures were designed to characterize the device more easily by utilizing unused space available in the 4-inch wafer.

#### 3.1. Electrode array

In ESCS, electrodes are placed in the cavity between the dura mater and the spine referred to as the epidural space. Accordingly, the design of an electrode array for ESCS depends on the anatomy of the spinal cord and spine which influences the available volume in the epidural space. The diameter of the spinal cord will differ depending on several factors such as species, age, health, and even for a particular individual. The diameter is also non-uniform along the spinal cord. In average, the diameter of a human spinal cord varies between 1.1 cm to 1.4 cm along the C4 to C7 region[45]. While in rats, the diameter varies between 3.5 mm to 4 mm between T12 and L1[46]. As far as design is concerned, the location and number of the stimulation sites need to also be taken into consideration. The above specifications for this work were adopted from the previous electrode array design made by V. Giagka[47] who is also involved in this project. The previously reported electrode array was meant to be used for ESCS in rats, and its functionality was verified in *in-vivo* tests (which were implemented using a prototype made from Platinum-iridium electrode and PDMS encapsulation).

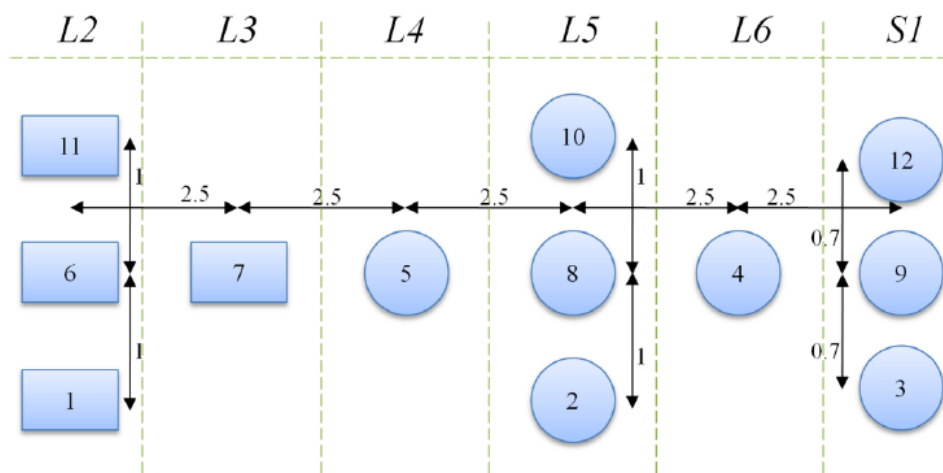


Figure 4 Twelve electrodes configuration. Dimensions are in mm.[47]

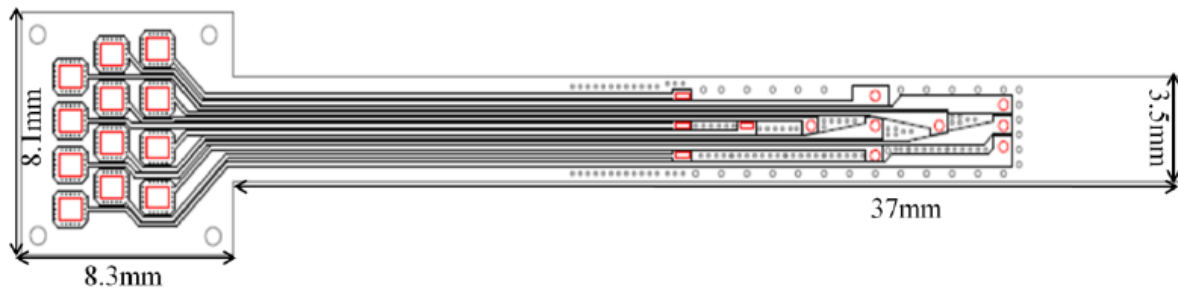


Figure 5 Passive electrode array design by V. Giagka[47]

In the aforementioned previous work, the electrode array fabrication was based on laser cutting technology. The resolution of the pattern created by this technique is limited by the radius of the generated laser beam. In this case, the minimum achievable gap between two structure was 40  $\mu\text{m}$ . However, in the final design, a minimum gap of 100  $\mu\text{m}$  was chosen to allow PDMS encapsulation to bond sufficiently which was assumed to potentially increase the reliability of the device.

The track width was chosen in consideration of the trade-off between device size and the number of electrodes. A width compensation scheme was applied to the interconnects (Figure 5). The width of the interconnects was made to be wider towards the end of the array where there are less interconnects leading to the electrode to prevent stress/strain concentration in the area with less metal. An uneven distribution of stress or strain can lead to broken interconnect when a large amount of force is applied to the electrode array during the implantation procedure.

The electrode array consisted of 12 electrodes each with 0.1  $\text{mm}^2$  exposed surface area. The entire structure consisted of three layers, a layer of metal as electrodes and two layers of PDMS encapsulating the electrode from the top and the bottom. The entire structure can be divided into two areas. The main body where the electrodes were located and the connector area which consists of contact pads. There were two different types of electrode openings, rectangle and circle. Originally it was used to test which performs better as an electrode. In the work presented in this thesis, the above specifications set the basis of the design presented in the paragraphs below. The overall goal was to fabricate an 12-electrode array using a graphene layer to form electrodes and interconnects, sandwiched between two layers of PDMS.

### 3.2. Test structures

Characterization is required to measure the performance of the fabricated graphene electrode array. Some characterization tests cannot be performed directly on the electrode array due to different requirements on the test setups. Test structures were designed to comply with the requirements of each test setup. The test structures were fabricated in the same manner as the electrode array so that it can mimic the performance of the electrode array.

#### 3.2.1. Bending test structure (Kelvin structure)

As mentioned in the Introduction, the electrode array will experience bending motions during the implantation period due to the movements of the spinal cord. The capacity of the electrode array to handle bending movements in terms of electrical properties need to be characterized. The degree of bending applied to the device under test is quantized by the bend radius.

Since the electrodes are used to deliver electrical energy, failure of the device can be measured in terms of electrical conductance or resistance. The easiest way to measure the resistance of a certain material is by utilizing the Ohm's law. A simple structure in form of a line similar to an interconnect is chosen due to simplicity. This structure is usually referred to as Kelvin structure which is used in 4-probe resistance measurement. The current is imposed along the line and the voltage difference between the two points along the line can be measured to obtain the resistance between the two points (Figure 6).

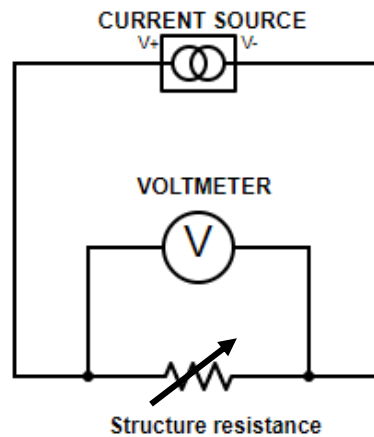


Figure 6 Schematic for the bending test. Structure resistance changes depending on the bending radius.

A device can fail when experiencing a small bending radius (high bending intensity) which leads to the breaking of conductive tracks; which, in this case, is made of graphene. The smallest bending radius that the device can handle is called the minimum bending radius. A device can also fail while experiencing bending higher than its minimum bending radius for several times. Formation of cracks from minor deflections can add up and lead to a device failure. Aside from device failure, the formation of cracks can cause permanent alteration on the electrodes and interconnects properties. The permanent damage caused by cracks can alter the resistance of the structure in unbend state. The amount of bend radius that can cause permanent damage to the device needs to be known to know the limit of deflection that the device can handle without compromising the original characteristics of the device.



Figure 7 Metal rod for controlling the bend radius



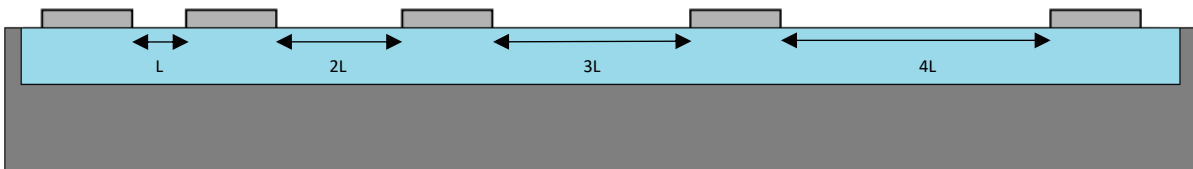
With the available setup, deflection is measured in bend radius controlled by the radius of a metal rod (Figure 7). The use of these rods limits the minimum length of the device under test. The device needs to be longer than half of the circumference of the rod so that the device experiences the correct bend radius as meant by the rod. A test structure with a length of 2 cm was recommended by an experienced user with the test setup.

The tests are to be performed in a destructive manner, in which the bending radius is reduced until the test sample's failure. The device electrical resistance is compared before and after the bending test. The resistance measurements are done three times for each test: before, during, and after the bending test.

### 3.2.2. Transmission Line Measurement

Transmission line measurement (TLM) is used to measure the contact resistance between the graphene and metal layer. The contact resistance is tested to see the effect of holey graphene which can potentially increase the electrical performance when interfacing with the graphene layer. The holey graphene is a structural derivative of graphene. It is a graphene layer that contains repeated hole creating a mesh-like structure [48]. This structural derivative of graphene has shown considerably lower contact resistance compared to a typical planar structure. Through this simple alteration in the structure, the contact resistance of CVD graphene to gold contact was reduced from  $200 \Omega \cdot \mu\text{m}$  to  $23 \Omega \cdot \mu\text{m}$ [48].

TLM structure could alternatively give us an option to extract the sheet resistance of the fabricated graphene layer. The proposed TLM structure has much smaller dimensions compared to the Kelvin structure for the bending test. It is easier to get a small defect-free area, thus a smaller structure could give more accurate result over sheet resistance measurement than larger structure. The advantage of the smaller dimension means that the TLM structure can be distributed easily across the wafer. Different measurements of sheet resistance can be mapped to see which area is more prone to defect during the fabrication process.



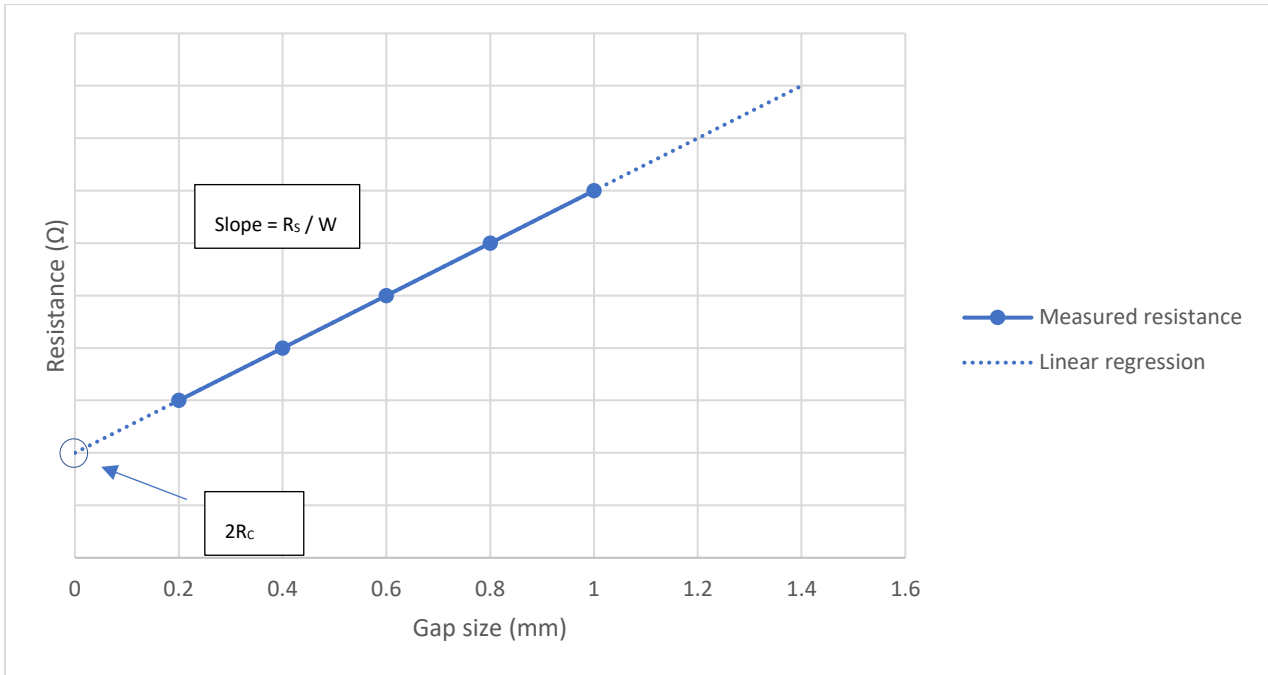


Figure 8 Example of typical TLM measurement result

An example of TLM measurement result can be seen in Figure 8. The measured resistance is drawn with the solid line. The resistance is expected to increase as the gap between the contact pair is increasing, therefore increasing the length of the graphene line. From the measurement of each neighboring pair of contacts, a curve can be made. The sheet resistance can be obtained by calculating the slope of the curve. Through linear regression, the contribution of the graphene layer between the contacts can be eliminated, thus obtaining a value in which represents the contribution of the contact resistance.

### 3.2.3. The optical transmission test structure

One of the reasons behind the novel use of graphene as an electrode is to allow optical monitoring of the spinal cord during the stimulation. Either through unaided visual inspection or through an imaging device, the transparency of the device in visible light spectrum is one of the key parameters that need to be known.

Through the measurement of the device transparency, the actual number of a graphene layer in a sample can be approximated. The use of Raman spectroscopy to measure the thickness of a graphene sheet is limited to identify up to 5 layers of graphene.

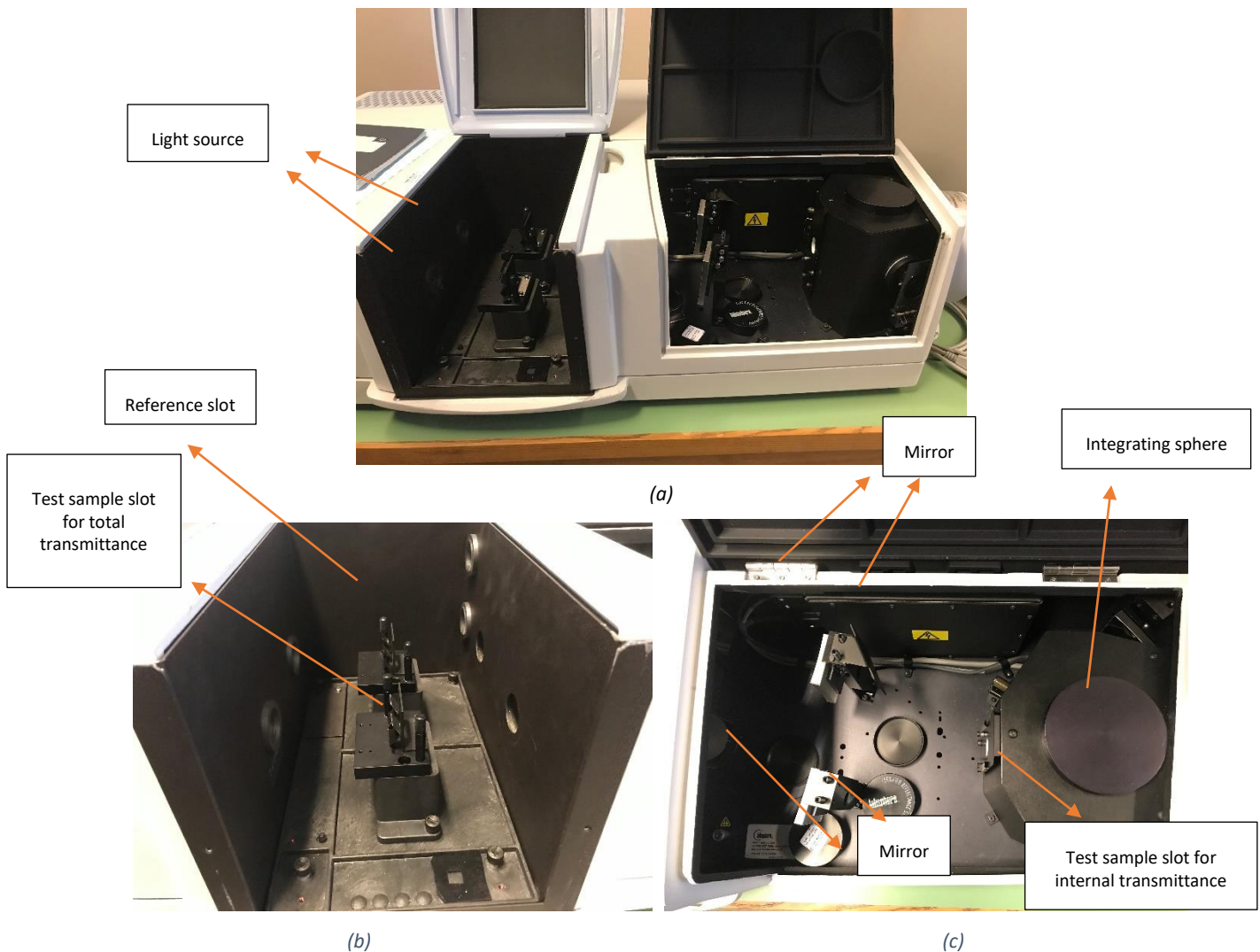


Figure 9 The test setup for optical transmittance using Lambda Arta 950

The degree of transparency, also referred to as optical transmittance is described as the effectiveness of a material to pass radiant energy. It is typically expressed as the percentage of radiant flux leaving the sample compared to the flux entering the sample.

Losses in the sample can be caused by several sources. Depending on this source of energy loss, optical transmittance can be divided into direct transmittance and total transmittance. Direct transmittance or internal transmittance is transmittance that is only taking into account the energy that is absorbed by the sample. Total transmittance on the other hand is considering the energy loss due to the effect of absorption and also scattering by the material.

Measurement of optical transmittance is done by using a spectrophotometer. The machine is capable to measure both internal transmittance and total transmittance depending on where the sample is placed. A sample can be placed in either one of the two fixed slots. One slot is located near the integrating sphere which redirects and average the incoming light to the photoreceiver. Because the sample is placed at the entrance of the integrating sphere, scattered light is measured along with transmitted light. Another slot is located near the light source and it is measuring the total transmittance. The light coming out from the sample is reflected twice through mirrors to reduce the effect of scattered light before it is entering the

integrating sphere. Because these slots are fixed, the spot size of the light beam on the slot positions is constant.

To get an accurate measurement of optical transmittance, the whole light beam needs to pass the sample. Consequently, the test structure needs to be larger than the spot size of the light beam. The spot size tends to be larger the further away it is from the source due to the radiating nature of light. Therefore, the test structure is preferably larger than the spot size in the total transmittance measurement slot. By the recommendation of the tool owner, the dimension of each rectangle is 5 mm x 20 mm. The two rectangles are surrounded by guiding lines to help the dicing process.

### 3.3. Summary

The design of the electrode array was based on the design made by V. Giagka[47]. This was done to focus the project more on the fabrication aspects of the electrode array. Test structures were also designed to measure the electrical and optical characteristics of the fabricated electrode array. These test structures were designed based on the available test setups.

## 4. Implementation

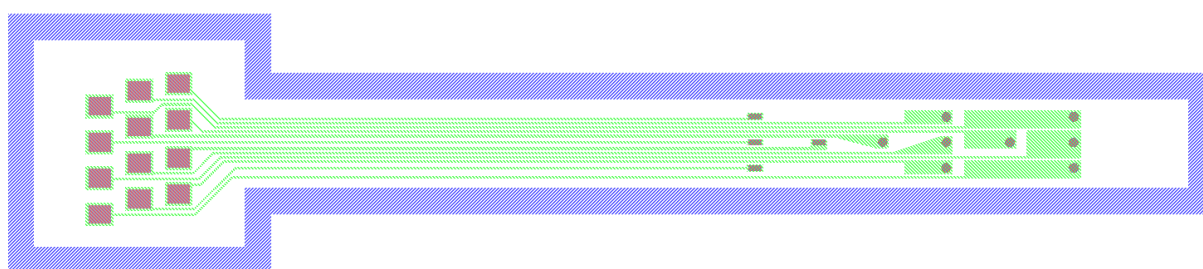
### 4.1. Microfabrication and wafer-scale process

The implementation of the design for the electrode array and the test structures was done by using microfabrication process. The use of microfabrication process to create structure in micrometer scale with high precision is the standard manufacturing process for semiconductor Integrated Circuits (IC). In IC fabrication, electrical components are made on silicon wafers. Because most equipment in the microfabrication process is tailored to be used for IC fabrication on a silicon wafer, the implementation of our design was carried out on a wafer-scale process. The fabrication of the electrode array was done entirely in Else Kooi Lab (EKL) in TU Delft.

The basic principle of the microfabrication process is material addition and subtraction. Materials such as metals are added on top of the wafer. A masking layer is applied on top of the added material. Through a photolithography process, the pattern is transferred from a photomask to the masking layer on the wafer. The photomask contains patterned chrome that blocks incoming light that activates the photochemical process on the masking layer. The previously added material is then removed using plasma or chemicals. The masking layer protects the material underneath thus transferring the pattern to the added material. The masking material can later be removed. This process is then repeated until the desired structure is made.

To implement the designs for the electrode array and test structures in the microfabrication process, photomasks were designed. Every photomask relates to the pattern of a single layer of material. For a structure that consists of several layers of material, multiple photomasks are required.

### 4.2. The layout of the electrode array



*Figure 10 Current electrode array design with width compensation*

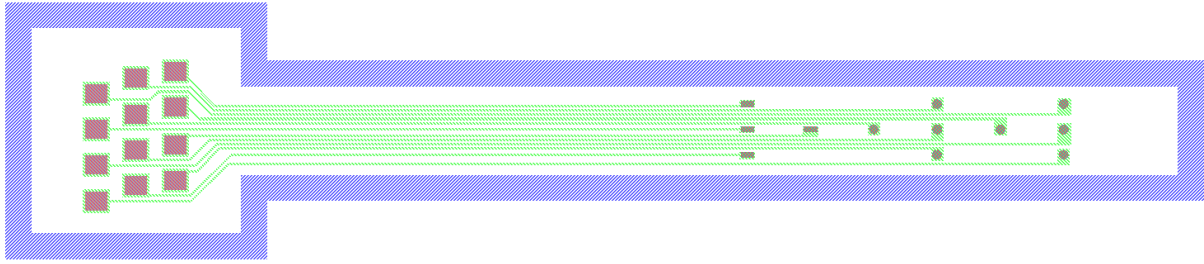
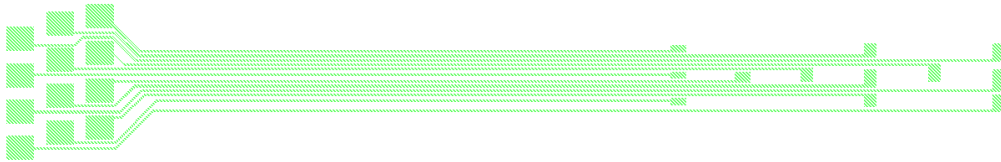
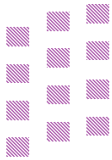


Figure 11 Current electrode design without width compensation

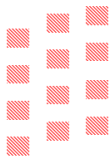
A layout for the photomasks was produced based on the previous electrode array design with several adjustments. The layout for the electrode array can be seen in Figure 10 and Figure 11. The two designs were made to see if the width compensation scheme is still necessary considering graphene possesses the highest measured tensile strength of 130 GPa [49]. This number is significantly higher compared to metal such as titanium (0.65-0.8 GPa[50]) and gold (400 MPa[51]).



(a)



(b)



(c)



(d)

Figure 12 Layers in electrode array layout: (a) Graphene layer, (b) Sacrificial metal layer, (c) Contact metal layer, (d) PDMS opening.

The designs consist of four patterning steps which require four different masks, the graphene layer, the sacrificial metal layer, the contact metal layer and the PDMS openings (Figure 12). The layers are arranged according to the processing order. In Figure 12(a)-(c), the colored area in the layout represents the area covered in chrome in the mask which will block incoming light. While Figure 3(d) was designed for a dark field mask. In this case, the whole mask is covered in chrome except for the colored area.

On the contact pads of the electrode array, wires will be connected through wire bonding to provide the stimulation signal to the electrode array. To avoid damaging the graphene layer during the wire bonding process, contact metal was designed to interface the graphene layer to the wires. The metal that will be used in this process is the combination of aluminum and titanium. Titanium can provide good contact resistance when being interfaced to a graphene layer. However, titanium is not suitable for the wire bonding process, thus aluminum is added on top.

In the final patterning step, openings are made in the top PDMS layer. These openings consist of electrode openings and contact openings. During this process, the dicing lines are also made. Dicing of the device was done manually by using a blade. Dicing lines were created to serve as a guide during the cutting process. Aluminum is typically used as the masking layer due to the long etching process of PDMS.

Sacrificial metal was used as a landing material when creating openings in the PDMS. Landing material was needed for two reasons. First, it is used to protect the graphene layer from plasma exposure during etching which can potentially damage the graphene layer. The second reason is to avoid backscattering of the etched material on the bottom of the openings[52]. Backscattering is deposition of etched material back to the wafer.

During PDMS etching, etched PDMS can be redeposited back on the wafer. The redeposition can happen on top of the mask and at the bottom of the opening that is being etched. J. Garra et al. also reported that the masking material was also redeposited back on the wafer[52]. To ensure that a through hole is made on each opening, sacrificial layer is placed at the bottom of each opening. This allows the etching process to be done for an extended period of time without damaging the graphene layer underneath and also the removal of redeposited material at the bottom of the openings when the sacrificial metal is removed.

The summary of the dimensions in the electrode array can be found in Table 1. Most of the dimensions are based on the previous design. Openings in the PDMS layer are made to be smaller than the graphene layer as overlay margin to mitigate alignment mismatch during each patterning step.

Holes at the edge of the device in the original design were removed to reduce the fabrication complexity. These holes went all the way through the device. It was meant to fix the implant in place during chronic implantation by allowing nearby tissue to grow through the holes.

*Table 1 The summary of the electrode array dimensions*

Connector area	8.3 mm x 8.1 mm
Main body area	37 mm x 3.5 mm
Graphene contact	1.01 mm x 0.91 mm
Contact opening	0.81 mm x 0.71 mm
Interconnect width	70 $\mu\text{m}$
Smallest gap between structures	100 $\mu\text{m}$
Electrode opening area	0.1 $\text{mm}^2$
Rectangular electrode opening	0.5 mm x 0.2 mm
Diameter of circular electrode opening	0.36 mm
Width of the dicing line	1 mm

The current work was done using photolithography technique using contact aligner. Although wafer stepper, a more advanced photolithography technology is available, contact aligner is used as opposed to wafer stepper due maximum device size is limited to 22 mm x 27 mm. Even so, contact aligner is theoretically still capable of producing a structure with up to 1.5  $\mu\text{m}$  resolution, defined by the resolution of the mask reticles. This is already surpassed the resolution achievable by laser cutting technique and it is sufficient to fabricate the electrode array design.

### 4.3. Bending test structure

Due to the limitation of the test setup, the structure needs to be long enough to be fitted into the test setup. A length of 2 cm is chosen based on the information from previous experience with the setup. Failure will most likely occur first on the smallest feature in the electrode array which is the interconnect between the bond pads and the electrode openings. To mimic the performance of the fabricated electrode, the width of the line is set to be 70  $\mu\text{m}$ . Test structures with 100  $\mu\text{m}$  and 200  $\mu\text{m}$  line width were also designed to see the effect of increasing the interconnect width for future reference.





Figure 13 Test structure for bending test. The green color represents the graphene and the red color represents metal layer.

The test will be performed by bending the structure approximately in the middle. The amount of bending applied to the structure is quantized by the bending radius. The radius in which conducting path is completely severed will be addressed as the maximum bending radius. Smaller cracks can also appear when small bending radius is applied, these cracks can increase the electrical resistance thus altering the electrical properties of the wire. Multiple cracks can form and accumulate after repeated bending. Thus, the resistance across the test structure before and after bending will be compared to see when the cracks are starting to form.

#### 4.4. TLM structure

The design for the TLM structure can be seen in Figure 14. Two test structures, the upper structure is a TLM structure with normal contact and the lower one is fitted with holey contact. The structure consists of 2 layers, a graphene layer and a metal layer.

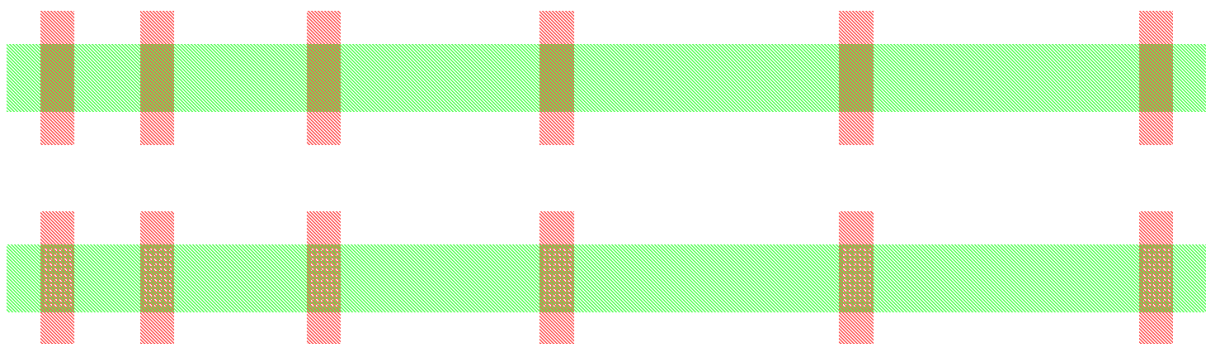


Figure 14 Transmission line test structure. The green color represents the graphene and the red color represents metal layer.

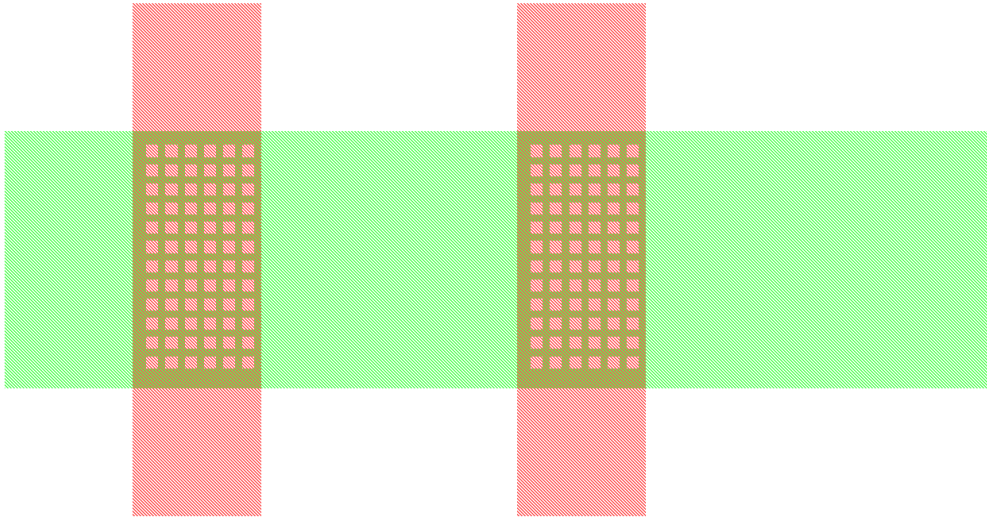


Figure 15 TLM holey contact. The green color represents the graphene and the red color represents metal layer.

Information regarding contact resistance can be obtained through linear regression of repeated resistance measurement between neighboring metal contacts. Resistance is measured using 2-probe setup. The gap between the left-most contacts is 0.2 mm and the distance to the next contact pair is increasing from the left to the right by 0.2 mm. The summary of the test structure dimensions can be seen in Table 2.

Table 2 The summary of TLM structure dimensions.

Graphene layer width	0.2 mm
Graphene layer total length	3.6 mm
Metal contact dimension	0.1 mm x 0.4 mm
Graphene – metal overlap	0.1 mm x 0.2 mm
Graphene hole dimension	0.01 mm x 0.01 mm
Distance between hole	0.005 mm

## 4.5. Optical measurement

Test structure for optical transmittance can be seen in Figure 16. The structure consists of 2 rectangles, one rectangle contains graphene layer while the other is not. The dimensions for the test structure are summarize in Table 3. The rectangle with graphene can measure the optical transmittance of the graphene and PDMS. The rectangle without graphene in it can be used to measure the optical transmittance of the PDMS layers. By using the superposition nature of optical transmittance, the graphene layer transmittance can be calculated. In the case of multilayer graphene, the information regarding optical transmittance can be used to estimate the number of layers inside the fabricated graphene.

Raman spectroscopy has been used to identify the number of layers in multilayer graphene, though it is limited to identify up to 5 layers of graphene. By knowing the absorption rate of a single layer of graphene, the number of layers within a multilayer graphene can be estimated. Some publications suggest that each layer of graphene absorbs approximately 2.3% of incoming light [33][53].

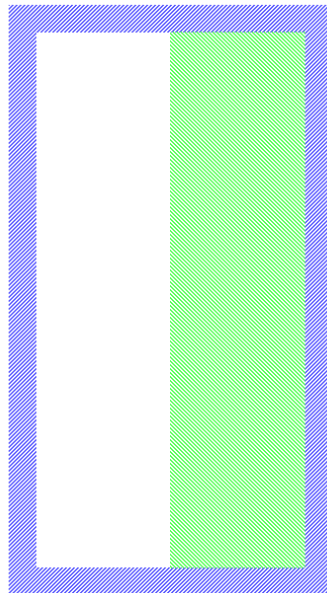


Figure 16 Optical transmittance test structure. The blue color represents hole on the PDMS, the white color represents the PDMS, and the green color represents the graphene.

Table 3 The summary of the optical transmittance test structure.

Graphene layer dimension	5 mm x 20 mm
PDMS hole width	1 mm

## 4.6. Full wafer layout

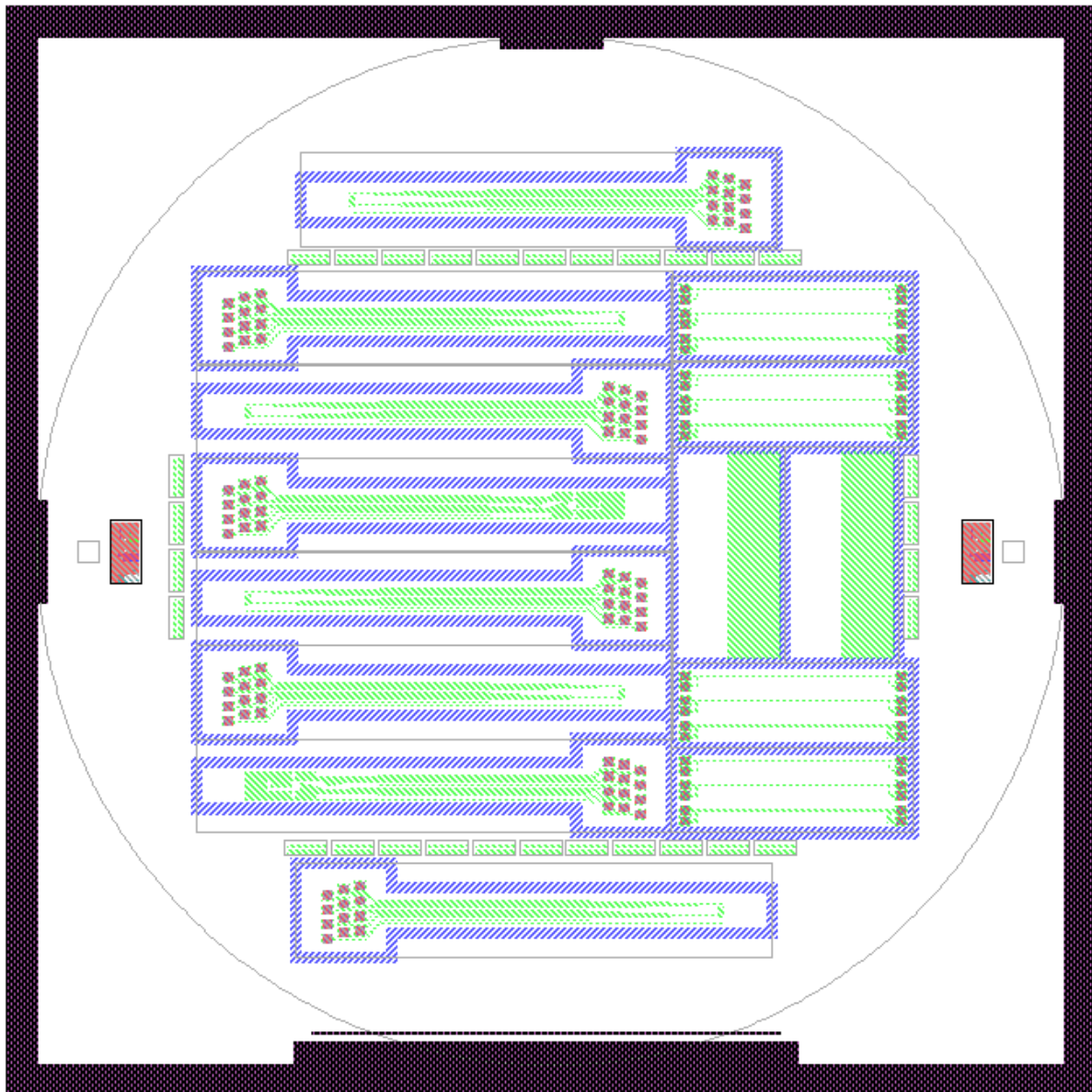


Figure 17 Full wafer layout

Figure 17 shows the layout of the wafer. Eight electrode arrays can be fabricated on a single 4-inch wafer. From eight electrode arrays, two of them are using the width compensation scheme. Damage due to fabrication process is more likely to occur at the edge of the wafer rather than the middle, hence proper placement of devices needs to be considered. Devices with higher importance are placed at the center. An electrode array with width compensation scheme and one without width compensation scheme are placed in the middle to increase the chance that each wafer can produce the two variants of the electrode array to allow comparison between the two designs. Two electrode arrays are placed at the top and bottom part of the wafer as extras, defects are expected to occur in these devices.

Next to the electrode arrays are the test structures. Each test structure is placed with redundancy to lower the risk of defects. The test structures with bigger dimensions have more priority due to less redundancy that can be put on the wafer. More redundancy is allocated for the Kelvin structures. These structures

consist of long and narrow wires which are more susceptible to defects. The small TLM structures are less sensitive towards defects and with plenty of redundancy, it is placed on every side of the wafer.

Apart from the electrode arrays and test structures, a red box at the sides of the wafer are placed. These boxed contain alignment markers for each layer that is used. The alignment markers were not designed in this project.

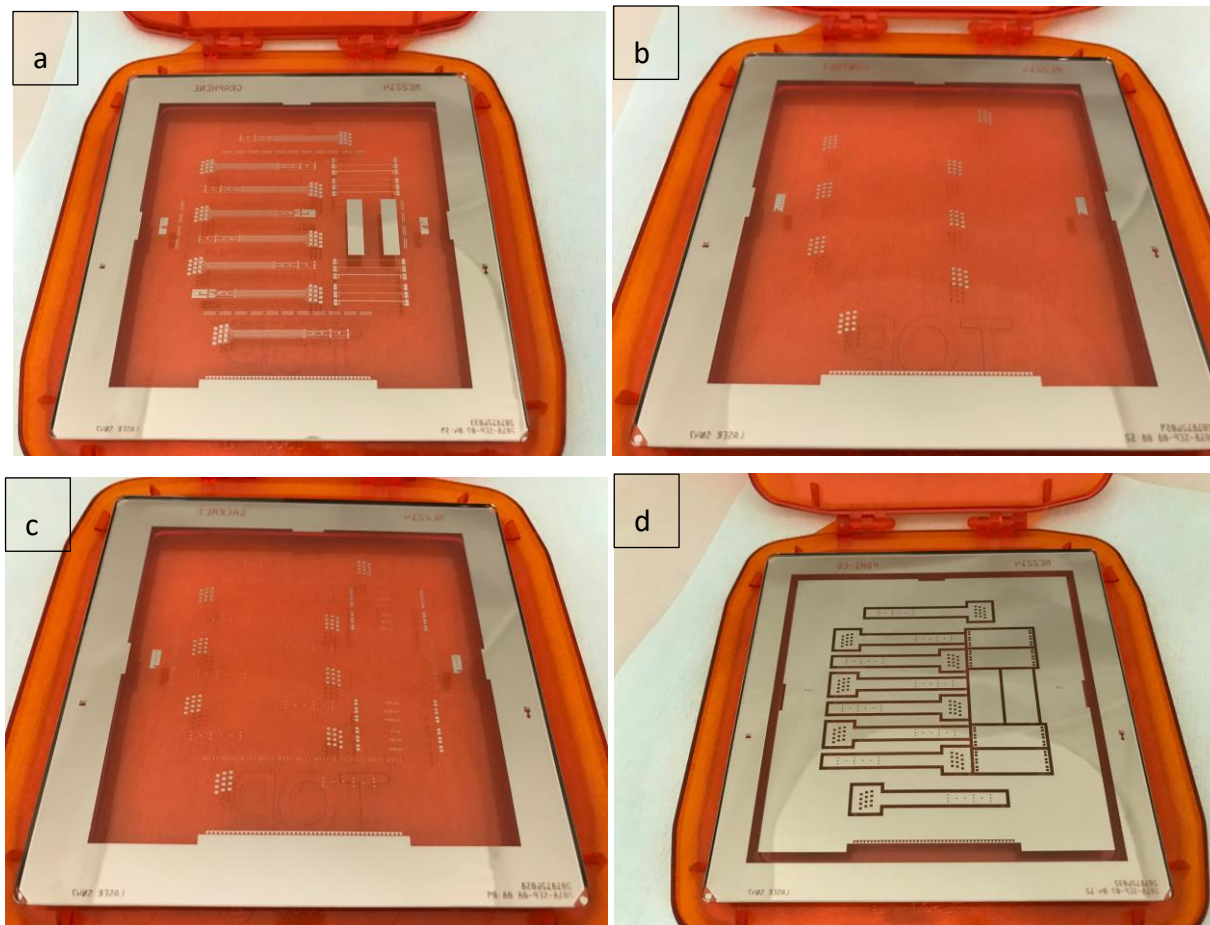


Figure 18 The finished mask. (a) Mask for graphene layer. (b) Mask for contact metal. (c) Mask for sacrificial metal. (d) contact for PDMS opening.

#### 4.7. Summary

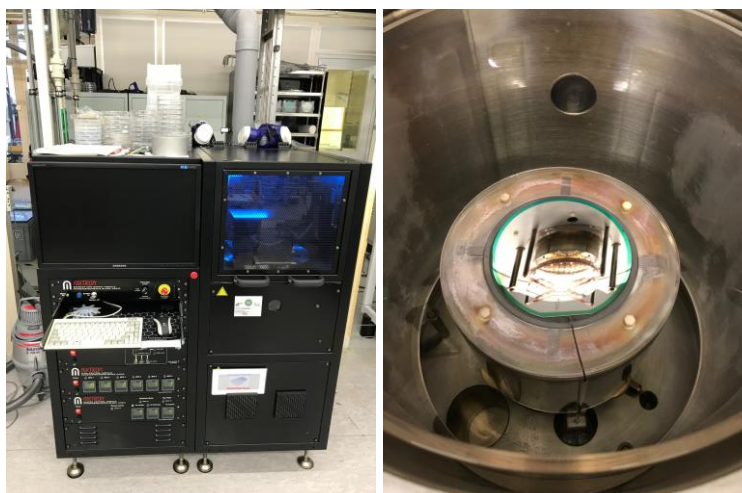
The designs of the electrode array and test structures are implemented as photomask for photolithography process. There are four masks in total, which are used to pattern the graphene layer, the contact metal, the sacrificial metal, and the opening of PDMS. There are two electrode array designs, the first design is using the metal compensation scheme following the original design and the other design is eliminating this scheme to see if this scheme is still necessary for graphene electrode array.

## 5. Graphene Deposition

At the start of this project, building a graphene device on a polymeric substrate has not been done previously in EKL. The fabrication process for this graphene and polymer substrate combination needs to be made from the beginning. Since the use of graphene is the novelty of this project, the fabrication process was built around the deposition of graphene.

As mentioned in previous chapters, there are various ways of obtaining a graphene layer. These methods include the exfoliation of graphene from graphite, epitaxial graphene, and reduced graphene oxide. The use of chemical vapor deposition (CVD) can provide a large area of graphene suitable for a wafer-scale process, hence the use of the CVD process is more desirable than the other process. Here molybdenum is used as catalyst, as it was previously found to give more uniform layers of multi-layered graphene than nickel.

In EKL, the CVD process of graphene is done in a machine called the AIXTRON Black Magic Pro (Figure 19). This machine can deposit a graphene layer on a 4-inch wafer at a time. The use of the CVD process for graphene deposition requires a metal catalyst on the wafer to facilitate the formation of the graphene layer. Metal such as nickel and copper are commonly used as the catalyst.



*Figure 19 The AIXTRON Black magic graphene deposition tool.*

The CVD process begins with a metal catalyst on a wafer as the starting material. Inside the CVD chamber, the wafer is heated up to 915°C. After reaching this temperature, methane gas is introduced to the chamber to provide carbon atoms. With the help of the high temperature, carbon atoms are diffusing into the metal catalyst. The chamber is then cooled down rapidly. The cooling down process forced the diffused carbon to be expelled from the bulk to the surface of the catalyst. At the surface, the expelled carbon atoms create a crystal structure that is referred to as graphene. Figure 20 contains the illustration of graphene CVD process with nickel substrate.

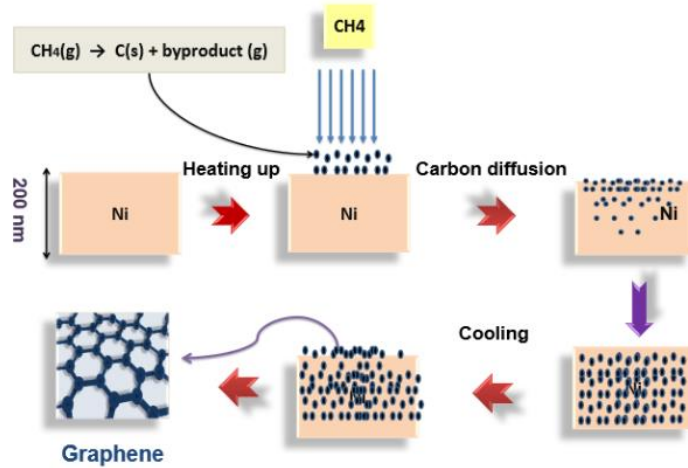


Figure 20 Illustration on CVD graphene process[54].

As a starting point for the graphene electrode array fabrication process, a transfer-free graphene deposition was used[55]. This process used 50 nm of molybdenum deposited on silicon dioxide as the metal catalyst. This molybdenum layer was patterned before the graphene deposition. The patterning process was done using plasma etching and the remaining photoresist from the patterning process was cleaned using N-Methyl-2-pyrrolidone (NMP). In the deposition chamber, the wafer was heated up to 915°C for 20 minutes while it was being exposed to methane gas. After the cooling down process, the graphene layer grew on the metal catalyst. With the catalyst patterned before the deposition of graphene, the pattern was also transferred to the resulting graphene layer. This process eliminates the need of patterning the graphene layer after the deposition. The molybdenum was later removed from the wafer by using hydrogen peroxide ( $\text{H}_2\text{O}_2$ ). When the metal catalyst was etched away, the graphene layer fell and rested on the silicon dioxide underneath the molybdenum (Figure 21).

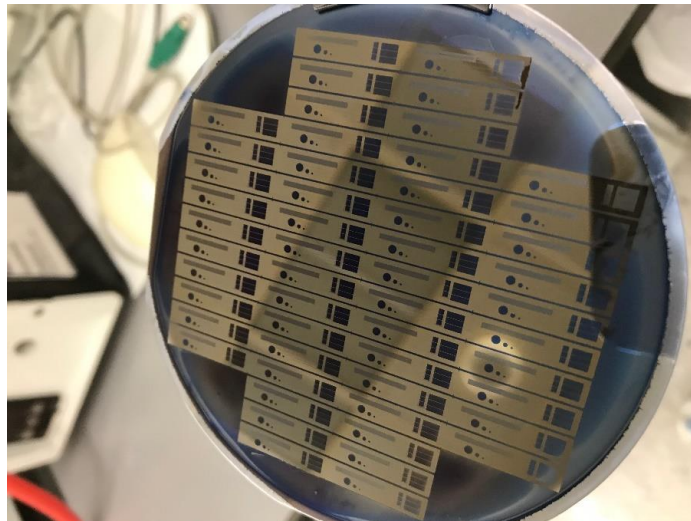


Figure 21 Graphene (blue colored) on silicon dioxide from the transfer-free graphene process.

## 6. Transfer Process of the Graphene Layer

Following the graphene deposition method of transferring the graphene layer to the PDMS layer was explored. Several ideas were investigated over the course of the project. The following chapter explains each of these transfer processes and the reasoning behind it.

### 6.1. The idea of the transfer process

The goal of this project is to have a graphene layer encapsulated by PDMS. This encapsulation can be performed by having PDMS layers from the bottom and the top of the graphene layer. The straightforward way to do it is by putting one side of the encapsulation layer underneath the metal catalyst before the graphene deposition process, but the high temperature during the deposition process makes it impossible for a polymer to survive. It has been reported that PDMS is experiencing thermal degradation in the form of depolymerization starting at 400°C[56].

Since having one part of the encapsulating polymer on the wafer before the graphene deposition was not possible, a transfer process was required to move the graphene layer to a polymeric substrate. The graphene layer was grown on one silicon substrate with a high thermal budget and transferred to another silicon substrate containing PDMS. A silicon substrate is needed on the new substrate so that further processing can be done with the equipment available in the cleanroom.

After the transfer-free graphene process, the graphene layer lands on silicon dioxide. The graphene layer is adhering to the silicon dioxide through weak bonds. By nature, PDMS is sticky and often used as adhesive. The sticky nature of PDMS can provide a better bond strength to graphene compared to the bond strength of graphene and silicon dioxide.

Continuing from the transfer-free graphene process, the wafer was put in contact with another wafer that contains a PDMS layer on the surface. This process was performed using the wafer bonder, where the parameters such as the temperature, pressure, and force applied on the wafer can be controlled. The alignment of the pattern on the graphene in respect to the substrate can also be kept by putting alignment markers on both wafers. Thus, the graphene layer will have the same alignment to the substrate in the target substrate as in its original wafer. This consistency in alignment is important when performing the next photolithography process.



## 6.2. Flowchart for the patterned graphene wafer bonding

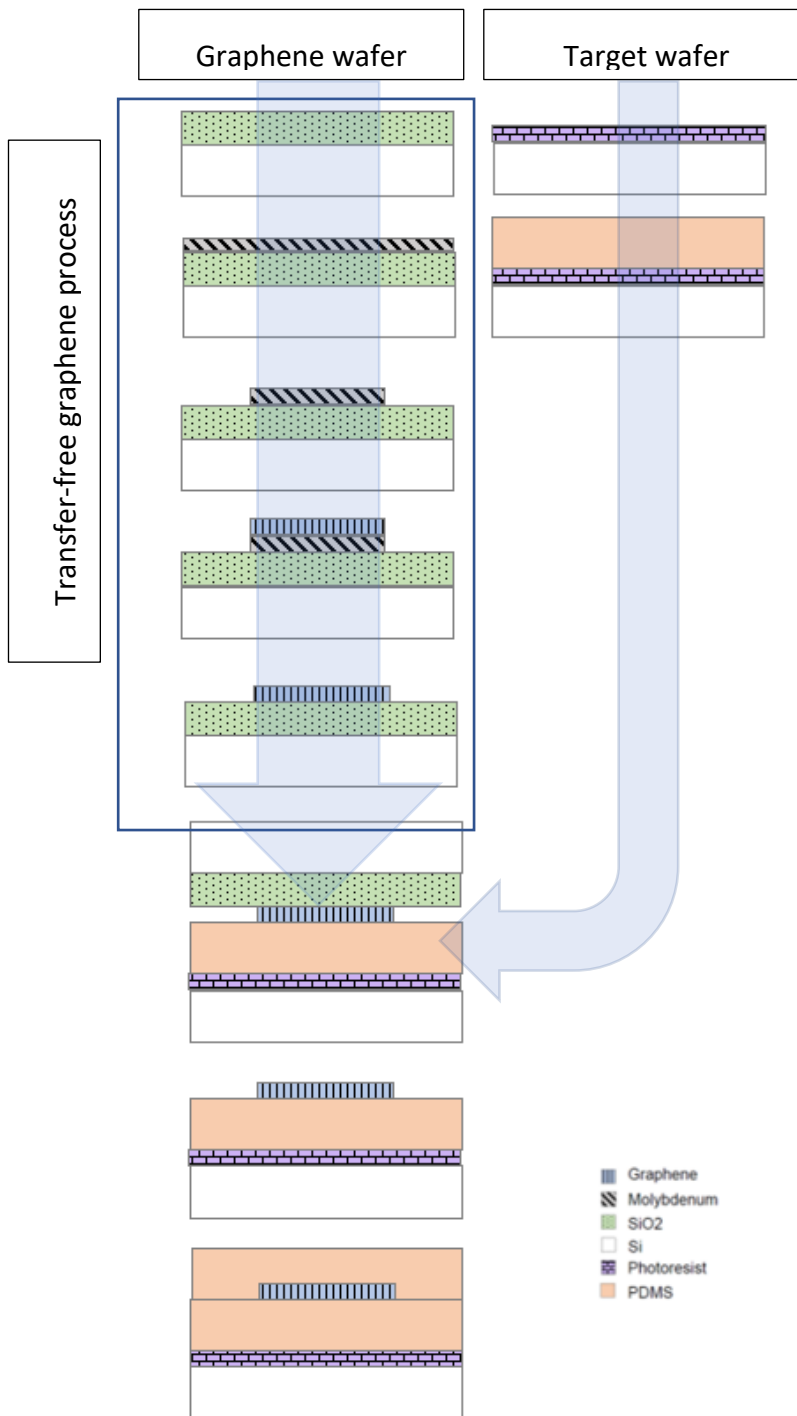


Figure 22 Simplified flowchart for wafer bonding process.

The process starts by preparing two wafers. One wafer will be the wafer for graphene deposition and the other wafer is for performing the encapsulation process. The first wafer to prepare is the graphene wafer. From a blank silicon wafer, 90 nm thermal silicon dioxide is deposited in the furnace. This process is continued with the sputtering of 50 nm molybdenum. A photoresist layer is deposited on top of the molybdenum. After exposure and development of the photoresist, the molybdenum layer is etched using Reactive Ion Etching (RIE)

process. The photoresist layer is removed by using the NMP solution at 50°C. This process is followed by graphene deposition in the Black Magic. During this process, the wafer is exposed to 915°C for 20 minutes. The whole graphene deposition takes about 90 minutes for processing 1 wafer. The molybdenum layer is then removed using hydrogen peroxide for about 5 minutes. At this point, the transfer-free graphene process is finished.

The second wafer is used to do the encapsulation process of the graphene layer. A PDMS layer is chosen as the encapsulation material. In this case, Sylgard 184 from Dow Corning is used as the PDMS layer. This product is chosen for prototyping the electrode array due to its availability in the cleanroom. This PDMS comes in a two-part solution that needs to be mixed in order to start the polymerization process. One part of the solution is a viscous liquid containing the monomer of the PDMS and the other part of the solution is the curing agent that will start the polymerization process. The ratio of monomer to curing agent of 10:1 is used as it is the suggested mixing ratio from the manufacturer. The mixed solution is then applied by spin coating on the wafer. After 1 hour of curing process in the oven for 90°C, the mixed solution on the wafer will solidify as the polymerization process occurs. The PDMS layer is ready for further processing after the curing step.

A layer of photoresist is also added on the second wafer, beneath the PDMS layer. The photoresist is deposited on the wafer by spin coating. This photoresist layer will be used at the end of the process to release the electrode array from the wafer. This process can be done easily by exposing the photoresist to acetone solution.

### 6.3. The result of the bonding process

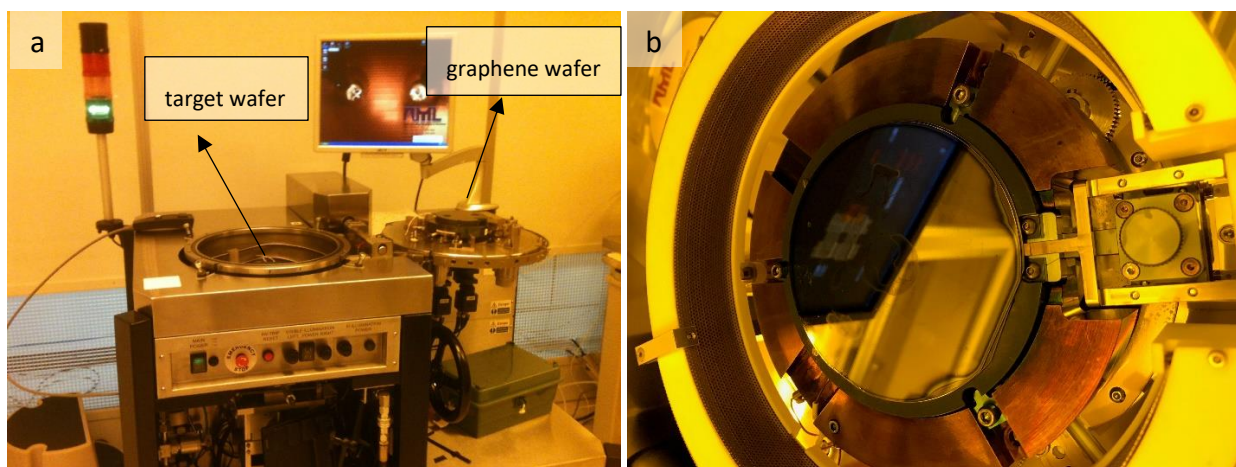


Figure 23 (a) The wafer bonder setup. (b) The finished bonding process, the two wafers are bonded together.

The wafer bonder is typically used for bonding two silicon wafers together to form an irreversible bond. This process is typically done in high temperatures with 6kN force applied on the wafers. However, a reversible bond between the graphene wafer and the target wafer is desired.

As the starting point for the bonding trial, a bonding force of 6kN was used with a chamber temperature of 70°C. The elevated temperature was used to promote adhesion of the PDMS to the graphene. The pressure was applied to the wafers for approximately 1 hour. After the bonding process, the two wafers were pried open using a metal pin. However, this attempt was unsuccessful. The two wafers were not able to be separated.

The later attempts for this process used lower force during the bonding procedure in order to form a reversible bond. A bonding force of 600 N was used for 1 hour. Even with considerably lower bonding force, separation process of the two wafers was still difficult. After being separated, the graphene layer was not transferred to the target wafer.

The failure to transfer the graphene layer to the PDMS indicates that the bonding between the two is not strong enough to overcome the bond between the graphene layer and the silicon dioxide.

#### 6.4. Plasma treatment to improve the adhesion of PDMS

The use of plasma to improve adhesion of PDMS is prominently used in the microfluidic applications. In microfluidics, PDMS is used to create channels for transferring liquid. The channels are made by first patterning the PDMS and then bonding it to another PDMS or other substrates.

Plasma treatment changes the function group of a fully-cured PDMS from methyl (-CH<sub>3</sub>) to hydroxyl (-OH). On PDMS to PDMS bonding, the formation of hydroxyl is bridging the formation of siloxane bond between the two pieces of PDMS. Without any treatment, a fully cured PDMS cannot bond to another PDMS while a plasma treated PDMS can withstand a 0.3 MPa pressure [57]. While this method is commonly used for bonding PDMS to PDMS or another silicon-containing substrate, the effect of plasma treatment on PDMS to graphene bonding is still unknown.

The effect of plasma treatment on the bonding between PDMS and graphene was tested using a similar procedure. The plasma used for the treatment was oxygen plasma and the smallest available power setting on the machine was used. The plasma treatment on the PDMS was performed right before the wafer bonding process. The wafer bonding needs to be performed immediately after the plasma treatment due to the effectiveness of the plasma treatment gradually reducing over time.

A simple test is performed to see the time frame when the bonding process is still acceptable to be performed. The hydrophilicity of the PDMS is a good indication of the effect of plasma treatment. The non-polar methyl function group causes PDMS to be inherently hydrophobic. While plasma treated PDMS has a polar functional group (hydroxyl) which causes the PDMS to be hydrophilic. The PDMS was exposed to 500 W oxygen plasma for 1 minute and contact angle measurements were performed on 30 minutes interval.

Contact angle measurements were performed to measure the degree of hydrophilicity of the PDMS surface. The measurement was performed by measuring the angle formed between the surface of the PDMS and a drop of water. Before the plasma treatment, an angle of 120° was formed between the PDMS and water surface which displayed the hydrophobicity of the PDMS. After the plasma treatment was performed on the PDMS, the water drop was able to form a wider interface with the PDMS (Figure 24a). After 30 minutes, the effect of the plasma treatment was already reduced by 20°. While performing the wafer bonding immediately after the plasma exposure will yield the optimum result, a certain degree of plasma treatment effect still persists After 1 hour. The contact angle of the PDMS returned to 120° when it was measured 18 hours after the exposure.

The bonding process with plasma treatment on the PDMS was performed using the flowchart in Figure 22. Before the bonding process, the PDMS was treated with 500 W plasma for 1 minute. After the separation of the wafers, graphene layer was still remained on the original wafer.

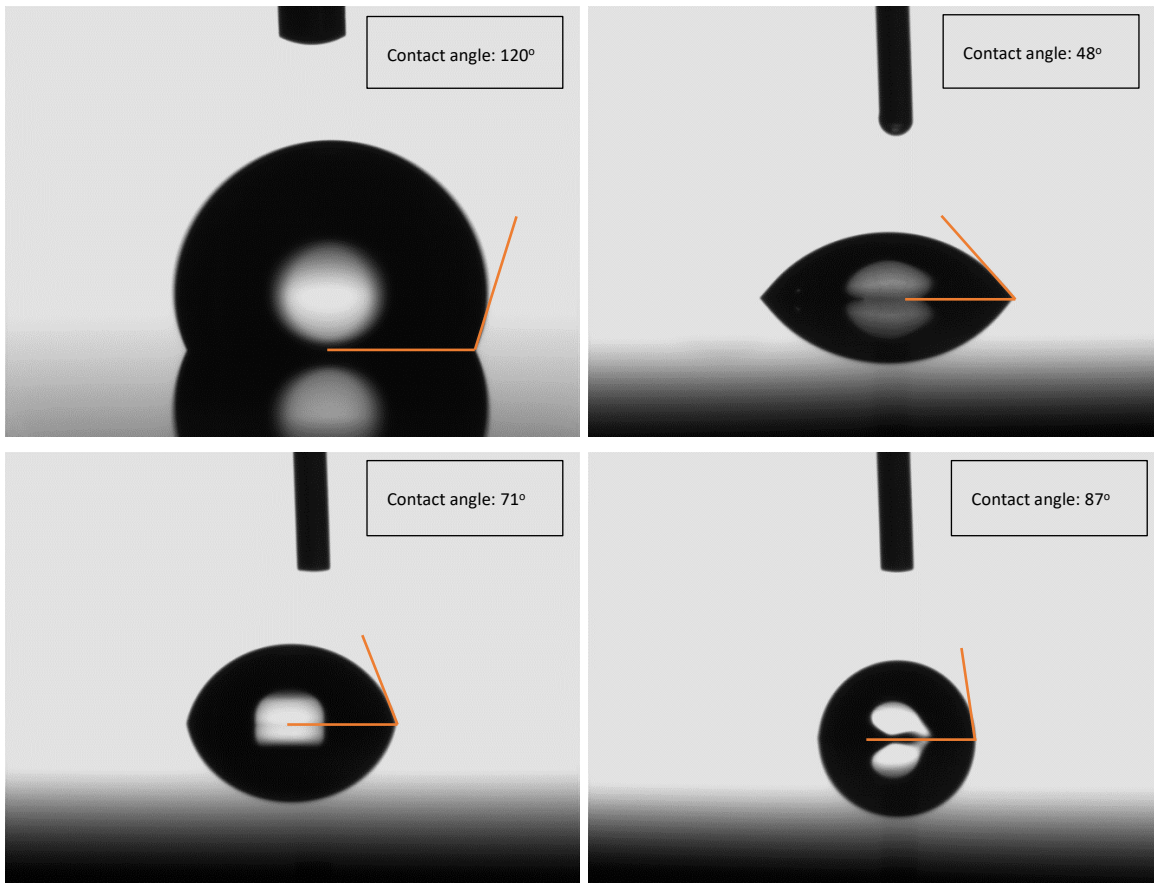


Figure 24 Contact angle measurement of plasma treated PDMS over time. (a) before plasma treatment. (b) immediately after plasma treatment. (c) 30 minutes after plasma treatment. (d) 1 hour after plasma treatment.

## 6.5. The use of different curing scheme of PDMS

The disappointing result of the previous graphene transfer process with the help of plasma treated PDMS indicated that plasma treatment alone cannot produce the necessary bond strength to remove the graphene layer from silicon dioxide. Another scheme to improve the adhesion of PDMS is by changing the curing process of the PDMS. Eddings et al.(2008) has shown different techniques that can increase the bond strength of PDMS[58]. While plasma treatment is one of the most popular technique to improve PDMS adhesion, there are other techniques such as partial curing, varying mixing ratio of monomer to solvent, and the use of uncured PDMS adhesive. From his study, partial curing and the use of uncured PDMS as an adhesive was showing a higher average bonding strength than the effect of plasma treatment.

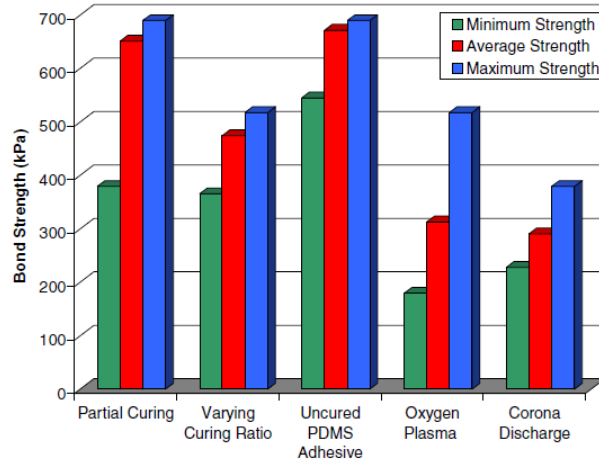


Figure 25 Bonding strength of PDMS-PDMS interface with various bonding techniques[58].

The use of uncured PDMS in the wafer bonder chamber was not preferable due to the possibility of PDMS solution leaking out from the interface of the two wafers. The partial curing approach was better suited to be used in the wafer bonder. The curing process of the PDMS can be continued while performing the bonding process by keeping the chamber temperature at an elevated temperature. Mimicking the result of the study of [58], the PDMS is cured for 30 minutes in an oven at 60°C. During the bonding process the curing of PDMS was continued, the temperature of the chamber was set to 60°C.

Several tests were run with the partially cured PDMS. However, every test has shown an unsuccessful outcome to transfer the graphene layer onto the PDMS. From this result, the outlook of doing a graphene transfer to a PDMS substrate was not promising.

## 6.6. Spin coating of PDMS on graphene

Looking back to the attempt on transferring graphene to a pre-cured PDMS on another wafer, the process was modified to further mimic the transfer process of graphene using a polymer medium. In typical graphene transfer process, polymer such as PMMA or PDMS is molded on the graphene layer in its uncured form. Applying the polymer in an uncured state allows the polymer to coat the graphene conformally. The graphene layer is typically grown on a metal foil made of copper. After the polymer is completely cured, the metal foil is removed by using chemical solution.

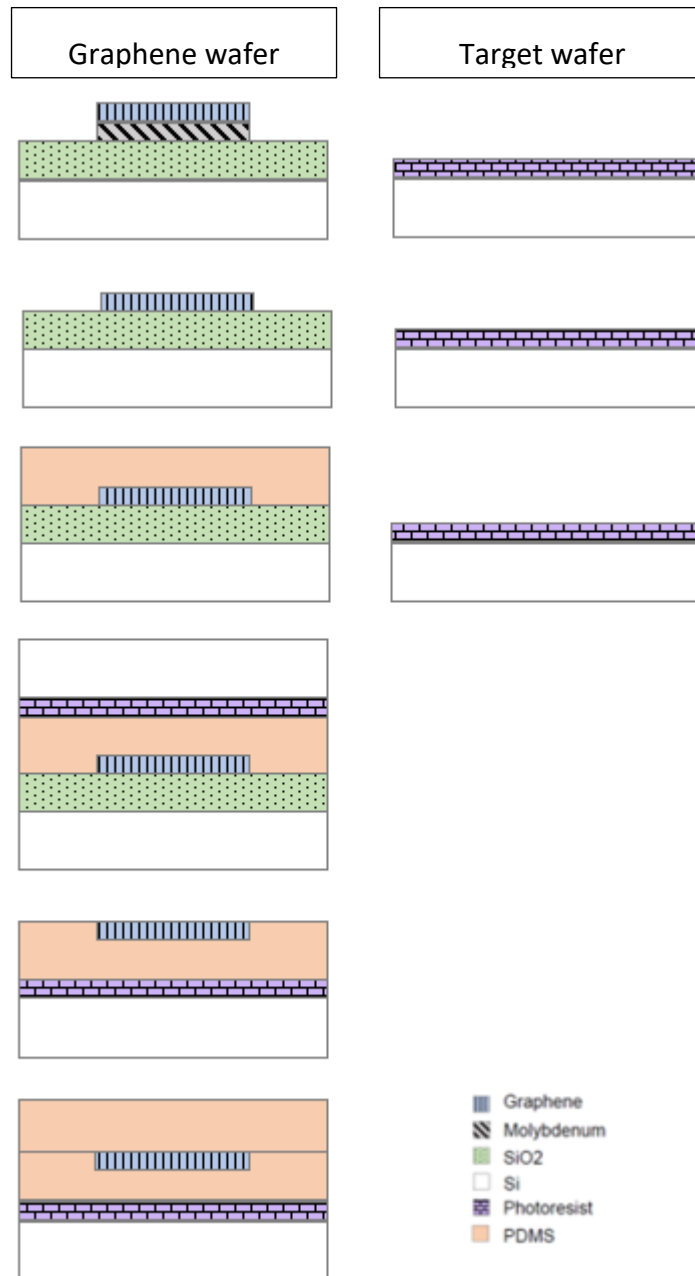


Figure 26 Simplified flowchart for graphene transfer process with PDMS spin coated on graphene

A similar approach was followed in a wafer-scale process. After the molybdenum catalyst is removed in transfer-free graphene process, graphene layer is resting on the silicon dioxide layer. To retain the alignment of the patterned graphene for the next photolithography process, the PDMS cannot be removed from the wafer immediately. To ensure that the alignment of the pattern is kept on the target wafer, the PDMS and graphene layer can only be removed from the original wafer after the bonding process; in which alignment is preserved to the target wafer. On the target wafer, photoresist is applied on the wafer to act as a release mechanism to remove the device from the wafer at the end of the process. Plasma treatment can be done on both the PDMS and the photoresist to increase the bond strength of the two polymers.

After the bonding process, the silicon dioxide layer is removed by using hydrofluoric acid (HF) solution. The removal of the silicon dioxide layer will delaminate the graphene and the PDMS from the original wafer.

Following the procedure in Figure 26, a test was performed. A 50  $\mu\text{m}$  thick PDMS was spin-coated on top of the graphene. Partial curing scheme was performed on the PDMS layer, in combination the photoresist layer was plasma treated to promote the adhesion between the two layers. The two wafers were bonded for 1 hour with 600 N force applied on the wafers. Temperature of the chamber was set to 60°C to continue the curing process.

The delamination process was performed a day after the bonding process to ensure that the curing process of the PDMS was completed. The wafer stack was soaked in a buffered hydrofluoric acid (BHF) 7:1 solution. The wafer stack was soaked until the two wafers can be separated with minimum force. The etch rate of the thermally deposited silicon dioxide in BHF is approximately 2 nm per second in room temperature. The thickness of silicon dioxide on the wafer was 90 nm. The etching process should be finished within 45 seconds. But after the wafer stack had been soaked for approximately 1 day, the bond between the wafers was still quite strong.

One possible explanation is that the wafers were bonded together, the BHF can only entered from the interface between the two wafers. Assuming that the BHF can enter from the entire stack interface, theoretically the BHF will have to etch 50 mm thick of silicon dioxide. If this is truly the case, the estimated etch time will be 7000 hours at best scenario. The presence of PDMS on top of the silicon dioxide can also hinder the etching process of the silicon dioxide.

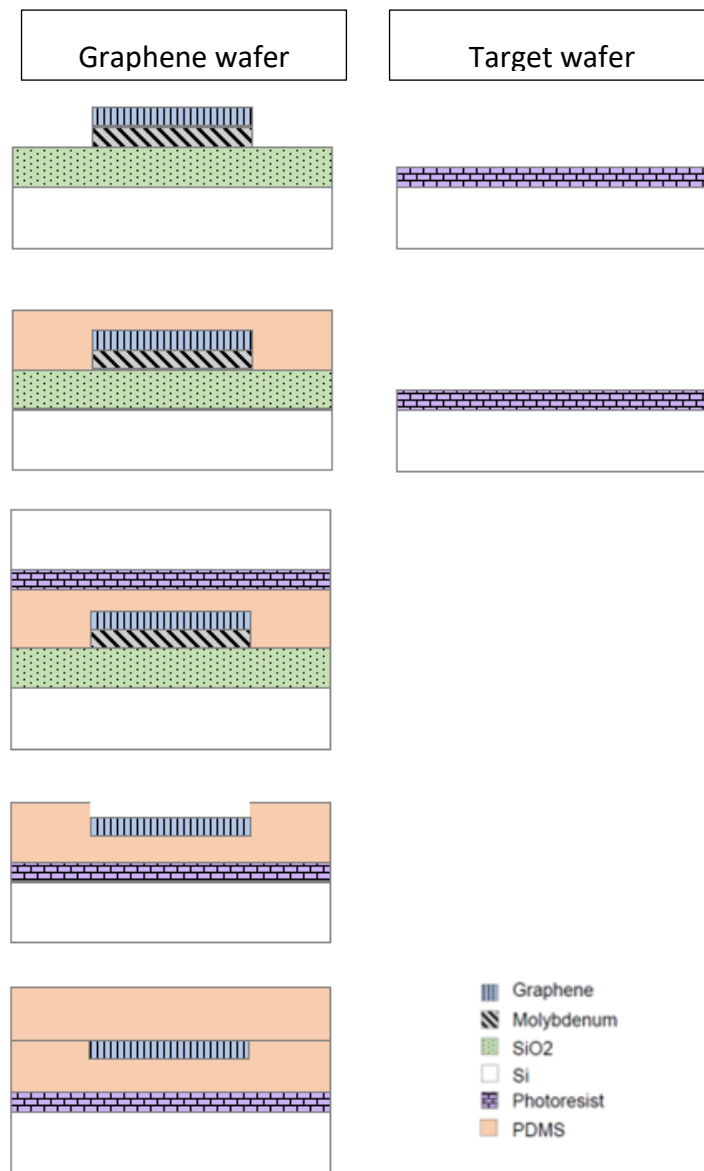


Figure 27 Simplified flowchart for graphene transfer process with molybdenum etching.

Aside from impracticality of removing the silicon dioxide layer, prolonged exposure can lead to absorption of HF into the PDMS. HF is considered as a harmful substance which can be dangerous if it is not removed or handled properly.

Another alternative for delaminating the graphene was sought. During the past process the potential use of the metal catalyst to delaminate the graphene was overlooked. Instead of letting the graphene layer to rest on the silicon dioxide, the graphene layer adhered to the previously applied PDMS layer. Unlike silicon dioxide, the etch rate of molybdenum in hydrogen peroxide (H<sub>2</sub>O<sub>2</sub>) is much faster.

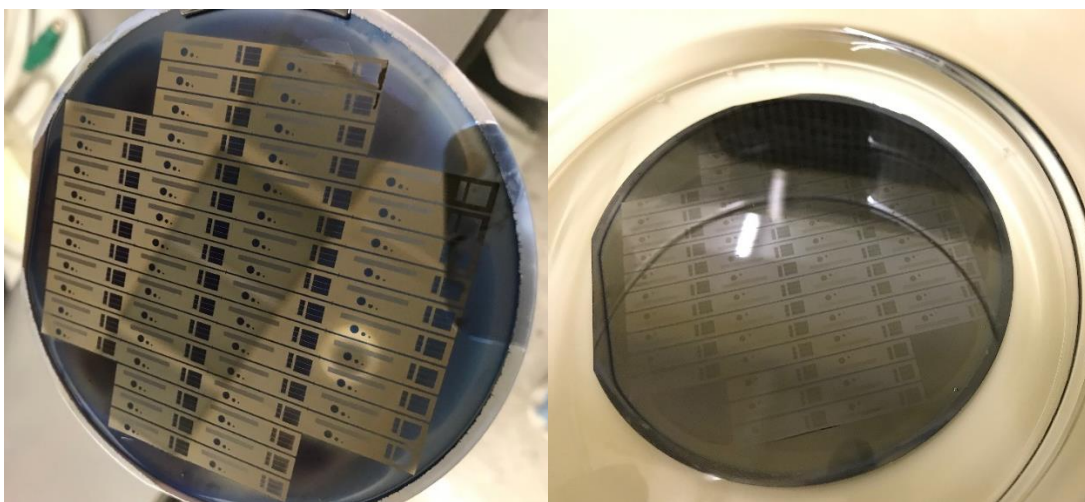
Two concerns arose before doing the test with bonded wafers. The first one is the effect of hydrogen peroxide to the PDMS. Polymer can react in two different ways when exposed to a certain chemical solution. Like most material, there can be a chemical reaction that dissolve the PDMS. The dissolution can happen due to part of the polymer reacts with the chemical solution thus causing de-polymerization of polymer. Another possible reaction that is diffusion of solution into the PDMS. Chemical fumes can diffuse into the PDMS causing it to



deform and increase in weight. Although PDMS is mostly liquid impermeable, Organic solvent such as chloroform and ether can also diffuse into the PDMS and cause swelling.

Mata et al. (2005) conducted a study on the effect of various chemical solution immersion to the PDMS [59]. The study suggested that 10 minutes immersion to hydrogen peroxide can cause a 2% of increase in weight. The swelling of PDMS indicated by the increase of weight is a reversible process to a certain extent. The absorbed gas is released from the PDMS over time. The use of the oven in vacuum environment can accelerate the release rate of the gas. Unlike HF that damages the PDMS over time, swelling caused by hydrogen peroxide is a more acceptable side effect that can still be solved. Nevertheless, significant swelling was reported to cause alteration to PDMS shape accuracy, while the extent of damage that be caused to PDMS layer that has not been patterned is still unknown.

A preliminary test was performed to see the possibility of etching the molybdenum layer which was coated by PDMS. For this test, a wafer with graphene on molybdenum was used. This wafer was coated with 50  $\mu\text{m}$  of PDMS, fully cured. The thickness of the molybdenum layer was 50 nm. Typically, during the transfer-free graphene process, the molybdenum layer was completely etched within 1 minute. A longer etching time was expected during the test due to limited access of etchant to the molybdenum.



*Figure 28 (Left) Graphene on silicon dioxide. (Right) Graphene on silicon dioxide, coated with PDMS. Molybdenum was removed after PDMS coating.*

The etching process for molybdenum coated by PDMS took 20 minutes. The resulting wafer was visually different than previous results of the transfer-free process. The graphene color was not dark blue but rather gray. It is likely that the difference in color was due to the graphene layer adhering to the PDMS as opposed to the silicon dioxide as in previous attempts. The PDMS layer was not visibly damaged after 20 minutes of immersion in hydrogen peroxide.

With the result from the preliminary test, further tests were performed based on the flow chart in Figure 27. The graphene wafer was coated with PDMS. The partial curing scheme was performed. The wafer was cured in the oven for 30 minutes at 60°C and then bonded with another wafer with plasma-treated photoresist. The curing process was continued during wafer bonding for 1 hour. The process is always continued on the following day to ensure the PDMS layer is fully cured. A PDMS with an imperfect curing process can be more susceptible to chemical reaction during the immersion into a chemical solution. The bonded wafer was later immersed into a solution of hydrogen peroxide in a beaker glass. The bond between the two wafers was tested every 5 minutes.

by using a wafer tweezer. The interface of the two wafers was not loosen even after 1 hour. The bonded wafer was then forcefully separated by using the tweezer. After 1 hour of etching, a similar result from the preliminary test was obtained with the PDMS remained intact and the molybdenum was completely removed, however the PDMS and graphene was not transferred to the target wafer. The target wafer was in the same shape as before the wafer bonding process.

After two attempts with similar result, a study on bonding strength of PDMS to different substrates could possibly explain the unsuccessful results. From Table 4, the bond between PDMS and silicon dioxide is much stronger than the bond with the photoresist, both positive and negative photoresist. The use of photoresist to bond with PDMS then needs to be reconsidered. The naturally high bonding strength of PDMS to silicon dioxide is comparable to the bonding strength of PDMS to PDMS presented in Figure 25.

The high bonding strength of PDMS to silicon dioxide can cause inconsistency in the bonding process result which is unaffordable with very limited number of samples. Most of the processes that are being done so far is only capable of processing one wafer at a time, limiting the sample generation rate. The graphene deposition tool and the wafer bonder being one of those processes. The total work invested for one sample from the start until the delamination of the bonded wafer was approximately 6 hours.

*Table 4 Average bond strength of PDMS to various substrate[60]*

Substrate	Average bond strength (MPa)	Standard Deviation (MPa)
Silicon with native oxide	0.33957	0.06744
Silicon without native oxide	0.18616	0.01090
Silicon dioxide	0.24132	0.02252
Negative resist (SU8)	0.10515	0.05099
Positive resist (AZ P4620)	0.08274	0.08402
Aluminum with native oxide	0.26890	0.03681
Glass	0.22753	0.02714

## 6.7. Blank transfer of graphene layer

Another alternative for transferring the graphene layer was then pursued. A conformal contact between PDMS and silicon dioxide is avoided. The conformal contact is most probably to form when liquid PDMS is in contact with the silicon dioxide. Continuing from idea in previous process, the available molybdenum layer on the wafer is used as sacrificial layer to release the graphene and PDMS from the original wafer. Instead of patterning the molybdenum before graphene deposition. Deposition of graphene is performed on the molybdenum on the whole wafer. Therefore, transferring a blank sheet of graphene onto the target wafer.

Transferring a blank sheet of graphene has several advantages. By doing all of the photolithography process on the target wafer, the original wafer does not need alignment markers. The use of wafer bonder can be

avoided in the future, if another option for bonding the wafers is available. Since all of the patterning steps is performed on the target wafer, alignment during bonding process is no longer necessary.

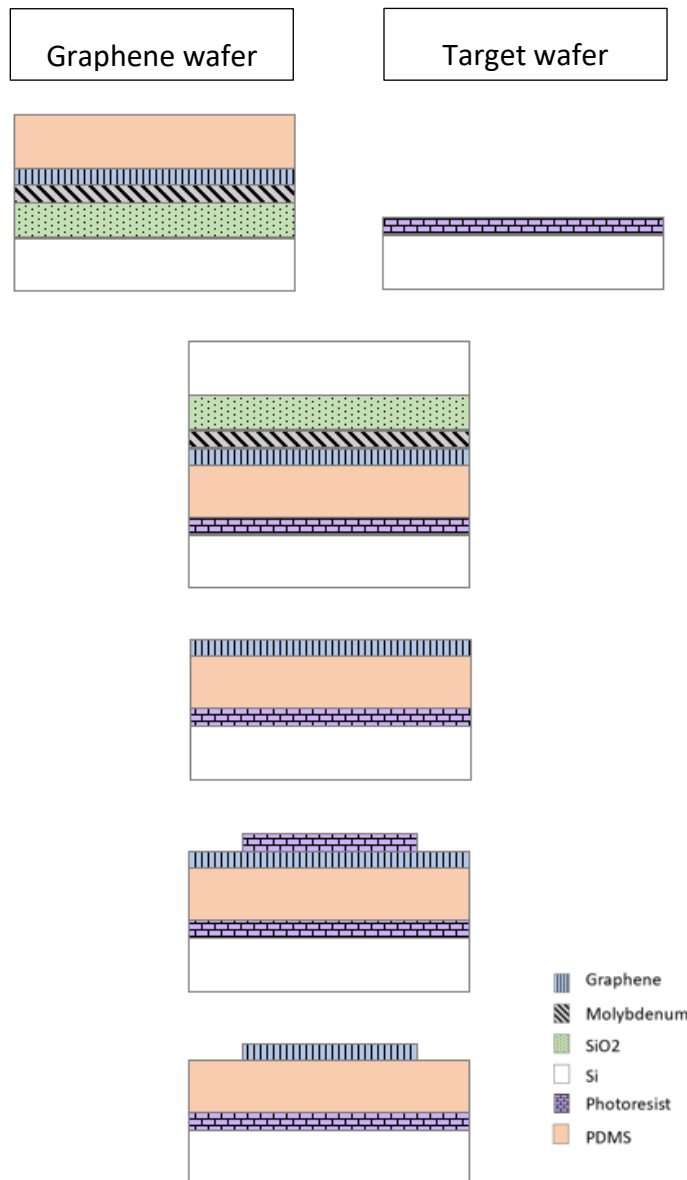
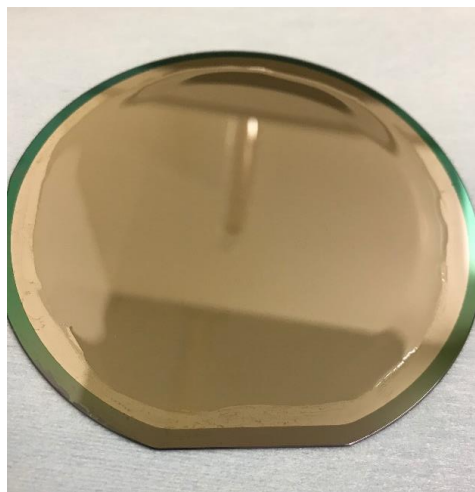


Figure 29 Simplified flow chart of transferring blank graphene layer

At this point of the project, photoresist was still used on the target wafer for releasing the device at the end of the process. Although the bond strength between the PDMS and photoresist is still lacking, there was no other alternative for sacrificial layer to release the device. At this point, proceeding with the transfer process was a higher priority to progress on the project.

Even though photoresist was still used in this process, a different photoresist was used. In the previous attempts, the positive photoresist SPR-3012 was used. For the next attempt, a more viscous AZ9260 positive photoresist was used. This type of photoresist is typically used for producing a thicker layer of photoresist. This type of photoresist has been reported to be used in combination with PDMS for micromachining purposes [61][62]. Hopefully, this photoresist can provide a better adhesion to the PDMS.

Starting from a silicon wafer, thermal oxide was deposited on top with a thickness of 600 nm in the furnace. The molybdenum with the thickness of 50 nm was sputtered on the silicon dioxide. The wafer was then undergone graphene deposition. A 50  $\mu\text{m}$  thick PDMS layer was spin-coated on the wafer. Learning from the past trials, the molybdenum coated by PDMS was etched slower than exposed molybdenum. To ensure that there is an access for the etchant to reach the molybdenum and also to reduce the etching time, the PDMS layer was removed from the edge of the wafer by using acetone. The PDMS was cured in 60°C for 30 minutes to partially cure the PDMS. The wafer was then bonded to photoresist on a silicon wafer with alignment markers, the chamber is set to 60°C to continue the curing process. Several tests were performed with different combination of bonding force and etching time. The bonding force was tested in the range of 50 N to 500N. The etching time was tested from 2 hours up to 1 day.



*Figure 30 The graphene wafer after PDMS coating. The PDMS was removed at the edge to expose the molybdenum.*

The new process flow was not easy to be performed. There are still a lot of unknowns when dealing with wet etching of a bonded wafer. The bonding parameters and the optimal etching setup was still not established. Compared to the previous process flow, these conditions were more crucial with larger area of molybdenum that needs to be etched.

During the first trial, the wafers were bonded with 500 N force and was etched for approximately 3 hours. The graphene was able to be transferred to the target wafer, but the PDMS and graphene layer was sliding down to the bottom of the wafer. One possible reason for this occurrence was the setup of the etching in combination with the weak bond between the PDMS and photoresist. The stack was inserted into a plastic carrier during the etching and rinsing process. To avoid the PDMS to reattach to the original wafer, the delamination of the target wafer needs to be performed in a liquid environment. The plastic carrier was not meant for fitting two wafers in one slot (Figure 31). With a little room to move, removal of the target wafer from the carrier can damage the PDMS.

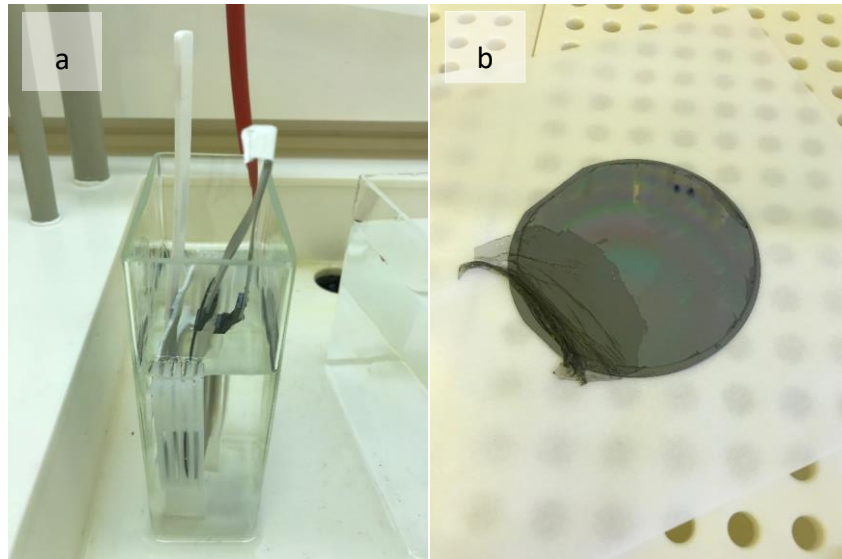


Figure 31 The first graphene/PDMS transfer with blank graphene. (a) The target wafer is being removed from the solution. (b) Target wafer with the graphene/PDMS.

For later tests, the wafer stack was etched inside a flat beaker glass filled with hydrogen peroxide. The concern of putting the wafer in horizontal position during etching is that the weight of the top wafer is constantly pushing the bottom wafer and closing the interface between them. The closed interface and the hydrophobic nature of the PDMS, may prevent the etchant from entering the interface and reach the molybdenum.

As feared, etching the wafer stack in horizontal position limited the flow of etchant into the interface. The weight of the top wafer was pushing the interface and closing the gap created by etched molybdenum. After 2 hours of etching in  $H_2O_2$ , most of the molybdenum still remained on the wafer (Figure 32a). While with the same process parameters, 15 minutes of etching in  $H_2O_2$  can also etched more molybdenum (Figure 32b). The only difference in the two cases was the etching process on the later wafer stack was performed immediately after the bonding process while the other was let to rest for one day after the bonding process. This case complicates the transfer process, since two samples with the same process parameter was not able to produce the same result.

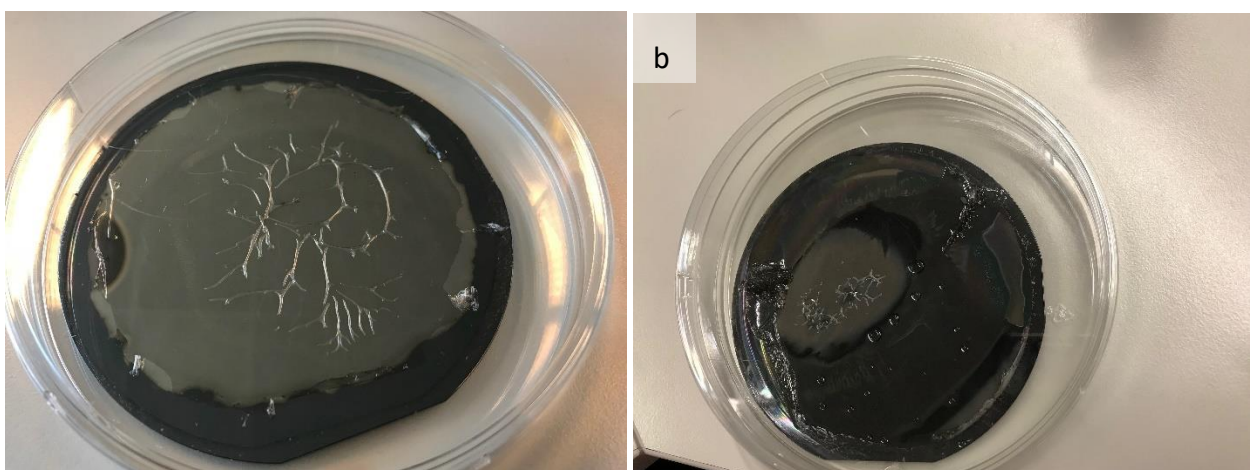
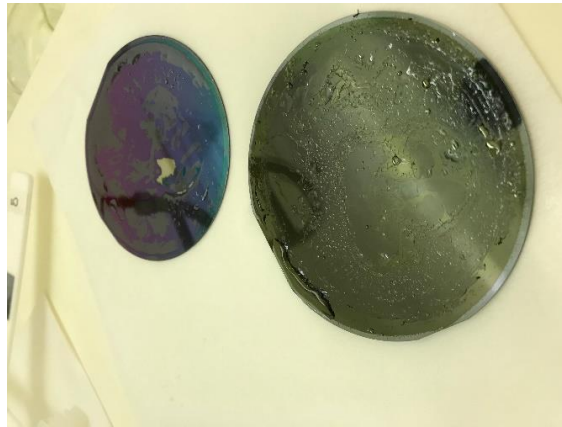


Figure 32 The failed results of molybdenum etching in beaker glass. (a) etched one day after the bonding process. (b) etched immediately after the bonding process

Another problem was observed on the wafer, after the separation process wrinkles appeared on the PDMS. These wrinkles were only seen on area with molybdenum on it. The wrinkles could appear due to the force

separation process of the wafer or the force applied during the bonding process. As there is no way to ascertain the reason from this result alone, a lower bonding force was used to see if the wrinkles can be reduced. The use of lower bonding force can also allow the PDMS in a more relaxed condition. The PDMS can be imagined behaving similar to rubber. The PDMS is put in a compressive condition during the bonding process. When the molybdenum is removed the compressed PDMS can expand and filling the gap left by the molybdenum.

The bonding force was reduced gradually on every test from 600 N to 100 N. At 100 N, successful result of PDMS transfer was able to be obtained. The wafer stack was etched until the wafer could be separated with minimum resistance, the etching time was approximately 4 hours. A small island of molybdenum was still remaining on the wafer. The graphene was not transferred on the area with molybdenum. The graphene has a stronger bond to the molybdenum as it was grown on the molybdenum as the metal catalyst. On the transferred PDMS, some bubbles were forming between the PDMS and photoresist. These bubbles were formed when there is a void below the PDMS layer exposed to hydrogen peroxide. The exact mechanism of the formation was unknown to the writer.



*Figure 33 The graphene and PDMS transferred to the target wafer*

A longer etch time was tested to completely remove the molybdenum. Inconsistencies in the result were also a major problem during this test. After eight hours of etching, an island of molybdenum still remained on the wafer. The size of the island was not linear to the etching time. Due to the lack of repeatability of the process, different alternatives that can improve the etching process of molybdenum were investigated. It is suspected that the molybdenum does not have a clear entry point thus etchant has a difficulty to access the molybdenum. So far, the PDMS was removed at the edges of the wafer after the spin coating by using acetone. This was done to prove access to the molybdenum for the etchant. But even with utmost care, this is a manual process and a thin layer of PDMS could still remained. The remaining thin layer of PDMS at the edge can hinder the etching process of the molybdenum underneath and slow down the etching process.

The other improvement that can be made is the use of different molybdenum etchants. So far hydrogen peroxide was used and as a molybdenum etchant it was working adequately. With the long etch time on the latest test, a faster etch rate is desirable to reduce the damage occurred to the PDMS.

## 6.8. Improving the etch rate: entry points, photoresist ring and wafer cleaving

The lack of entry point was probably the cause of the slow etch rate of the molybdenum. A thin layer of PDMS may still remained on the edge of the wafer even after the attempt of removing it by using acetone. The edge

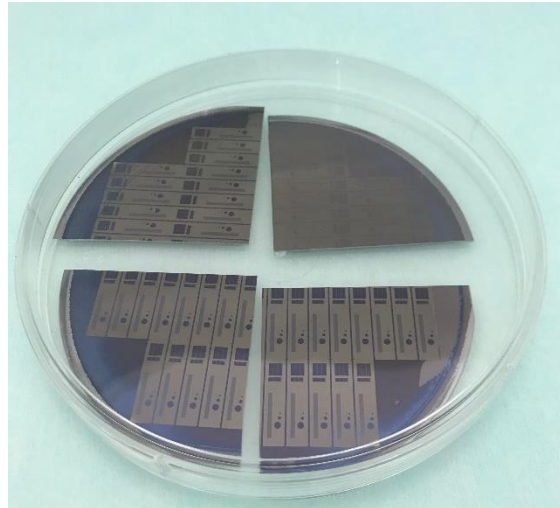
of the molybdenum is crucial to be protected from the PDMS. It is the first area that is in contact with the etchant. After an area of molybdenum is removed, the void it leaves behind will become a pathway for etchant to reach the center part of the wafer.

While creating a through hole for etchant at the back of the wafer directly to the molybdenum layer with deep reactive ion etching (DRIE) would be possible, there are a lot of considerations and adjustments that need to be made on the existing process. The size and number of the through holes would need to be figured out. Then the mask for the holes would need to be designed and ordered. The effect of these holes to the graphene deposition was also unknown. With the limited amount of time, this option was not pursued; but it can be performed as future work.

There were two different techniques to deal with the entry point issue. The first one is to use photoresist ring that will protect the edge of the molybdenum during PDMS spin coating. This photoresist ring later can be removed before the bonding process to create a clean molybdenum surface. The second technique is to cleave the edge of the wafer just before the bonding process. From the cleaving process, the molybdenum will be exposed from the side which can be easily accessed even after the wafer bonding process.

### 6.8.1. Wafer cleaving

The wafer cleaving was performed by creating a scratch at the edge of the wafer. The scratch damaged the silicon crystal structure. A fulcrum is then placed underneath the wafer, right below the scratch. A small force is then applied with a tweezer from the top of the wafer to create a lever with the fulcrum at the center. The crack will propagate along the crystal plane and split the wafer in a precise way along a crystal plane.



*Figure 34 Example on a good cleaving result*

The cleaving process is performed after the coating and curing of PDMS. On the wafer, there are 600 nm of silicon dioxide, 50 nm of molybdenum, a graphene layer and 50  $\mu\text{m}$  of PDMS. After the graphene deposition, thermal stress accumulates on the wafer. The accumulated stress made it harder to cleave the wafer along the (110) plane as the stress induces lattice defects in the wafer causing the cut to deviate from the (110) plane (Figure 35). The cleaving process needs to be performed with caution, as it can shatter the whole wafer.

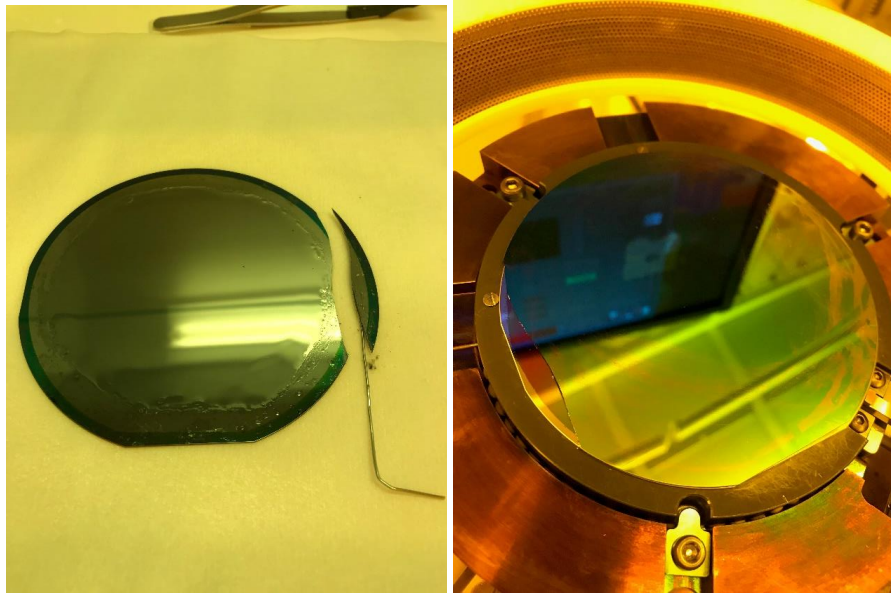


Figure 35 (Left) Cleaved test wafer. (right) Cleaved wafer bonded with the target wafer with photoresist.

After the etching for 1 hour in hydrogen peroxide, delamination of the bonded wafer was noticeable. After delamination was performed, a small island of molybdenum was remaining on the opposite of the cleaved side. The island of molybdenum pulled the PDMS to the original wafer thus transfer of the PDMS was not able to be performed.

From this result, the cleavage was not able to help to transport the etchant to the other end of the wafer. Since it was working on one side, increasing the number of entry points by cleaving the wafer on four different sides would increase the effectiveness of etchant delivery from multiple sides.

A test was performed with wafer that was cleaved on four sides. The wafer stack was etched in hydrogen peroxide for about 1 hour (Figure 36a), similar to the previous attempt with a single cleavage. A big island of molybdenum remained on the wafer which inconsistent with the result of the single cleavage test. Another test with four cleavages was performed and similar result was obtained.

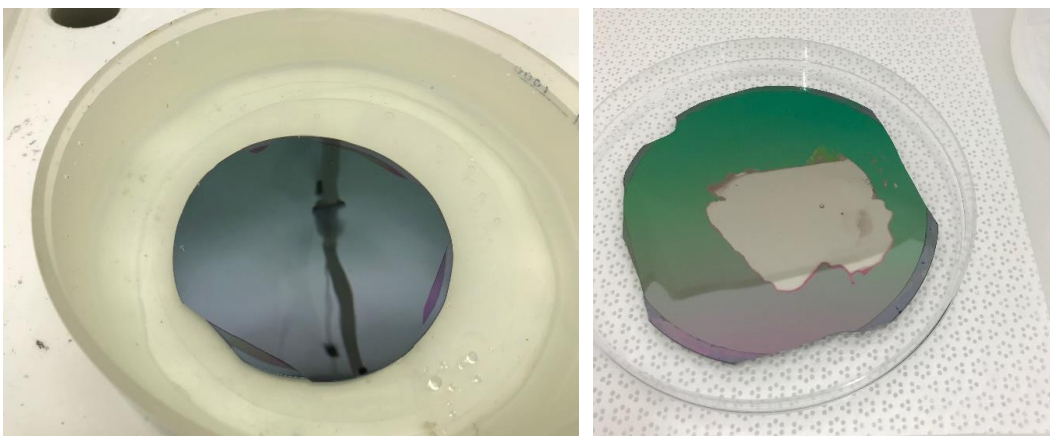
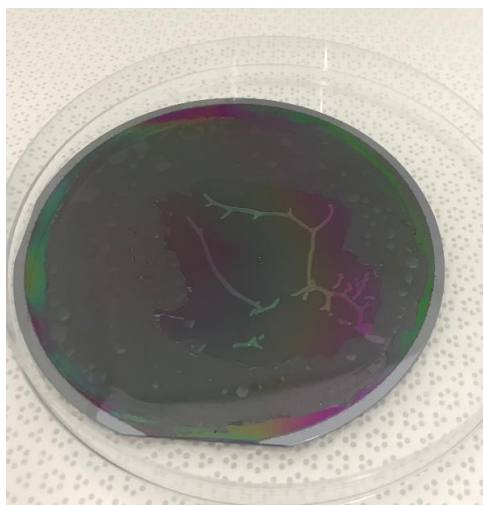


Figure 36 Test with four cleavages. (a) Bonded wafer stack with four cleavages etched in  $H_2O_2$ . (b) The original wafer after the separation process.

The contribution of the cleavage to the molybdenum etching during the first test was questioned. The effect of wafer cleaving was not reproducible in the following tests. Apart from the disappointing result, stress in the wafer made the cleaving process to be skill dependent and risky. Some dust from the cleaving process could



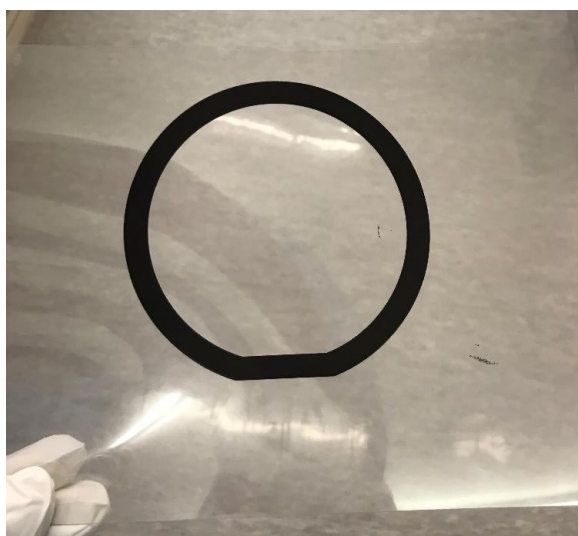
also be seen on the top of the PDMS. Removal of the dust was not possible due to the adherent nature of the PDMS. Weighing on the risk against the inconclusive result, this process was not attempted any further.



*Figure 37 The target wafer for the four cleavages test. The graphene layer was transferred to the target wafer except for the area where molybdenum remained.*

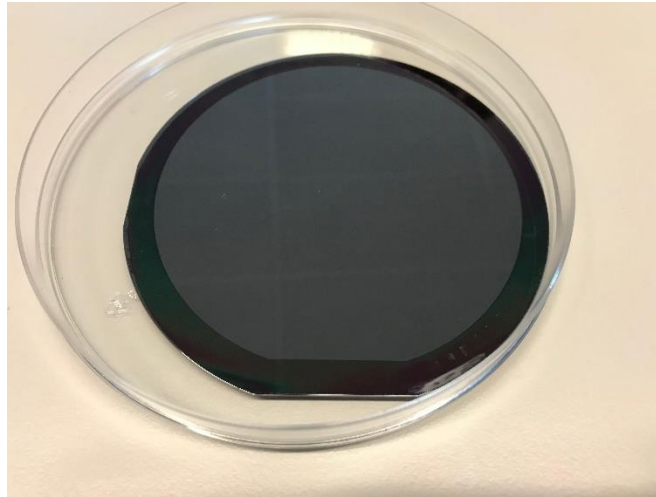
### 6.8.2. Photoresist ring

The other technique for improving the delivery of the etchant was the use of photoresist ring to protect the edge of the molybdenum. The photoresist was patterned by using a makeshift mask made of printed overhead sheet.



*Figure 38 The makeshift mask made of overhead sheet*

The SPR-3012 was used as the photoresist with the thickness of  $2.1\ \mu\text{m}$ . The photoresist was coated on top of the graphene and molybdenum layer. During the exposure, the makeshift mask was placed on the wafer. The alignment was done manually by fixing the pattern on the mask to the edge of the wafer. After exposure, the exposed photoresist was removed with the developer MF-322. The wafer was then exposed again without using the mask so that it can be removed by using the developer. Since the target wafer had unexposed photoresist on it, the use of developer can remove the photoresist ring selectively without damaging the photoresist on the target wafer.



*Figure 39 The graphene wafer with photoresist ring.*

After the second exposure, the graphene wafer was coated with the PDMS. The PDMS on top of the photoresist was removed with isopropanol. The wafer was then bonded with the target wafer. During the separation process, before the wafer stack is exposed to the hydrogen peroxide, it is exposed to the developer. With the photoresist ring removed, clean molybdenum surface can be accessed by the hydrogen peroxide. While the PDMS layer was transferred to the target wafer, PDMS was not able to adhere to the target wafer completely, part of the PDMS was folded in and could not be folded back.

A thin layer of PDMS was also spotted at the edge of the target wafer. This thin layer originated from the top of the photoresist ring which was cleaned with isopropanol. The use of isopropanol was not effective to remove the PDMS. Underneath the PDMS adhering to the target wafer, brown color was seen. It looked like the photoresist on the target wafer was etched during the separation process.



*Figure 40 The PDMS on the target wafer transferred using photoresist ring technique.*

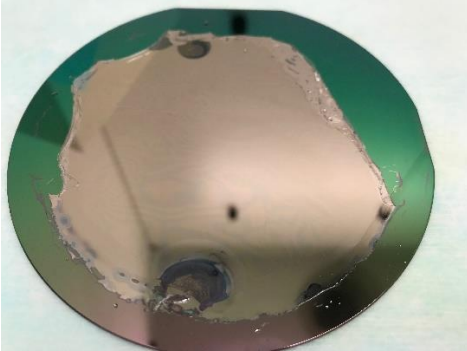
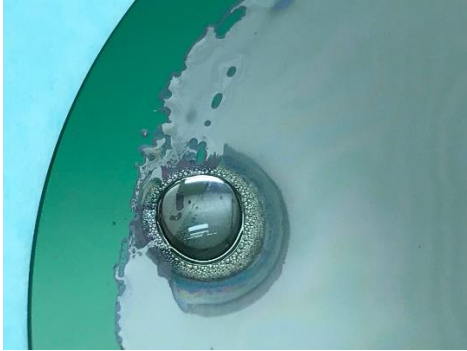
The use of photoresist ring was able to transfer the PDMS to the target wafer. The photoresist ring also prevented the interface between the two wafers to be sealed during the bonding process. When the ring was removed, a gap was formed that let the etchant to enter into the interface. But it came with its own set of troubles. The damaged occurred on the target wafer could reduce the probability of the formation of good bonding between the PDMS and the photoresist.

## 6.9. Improving the etch rate: different etchant for Molybdenum

The use of hydrogen peroxide for etching the molybdenum was adopted from the transfer-free graphene process. With the addition of the PDMS and a larger area of molybdenum to etch, other options for etchant needed to be explored. From the handbook for metal etchant, there are other chemical solution that can be used as etchant for molybdenum[63]. It is important to avoid the use of high temperature during the etching process to avoid damaging the PDMS. The most promising one for etching molybdenum in room temperature would be the use of ammonium hydroxide ( $\text{NH}_4\text{OH}$ ) and  $\text{H}_2\text{O}_2$  mixture (RCA-1) which was also recommended by the lab's chemist. But,  $\text{NH}_4\text{OH}$  will remove the photoresist from the wafer. The other possible etchant is an etching solution that is PES-77-19-04 which mainly consist of phosphoric acid ( $\text{H}_3\text{PO}_4$ ). The PES etching solution is intended for etching aluminium, but it is reported to also work for etching molybdenum. The use of hydrogen fluoride which was avoided in the past was also mentioned for etching molybdenum. Other recommendation that was received from the lab's chemist was ferric chloride ( $\text{FeCl}_3$ ) which can be used in room temperature and but more effective in higher temperature ( $50^\circ\text{C}$ ). The other known etchant was nitric acid ( $\text{HNO}_3$ ) which was typically use for wafer cleaning process.

The test was performed by putting a wafer with molybdenum and PDMS into an etchant in a glass beaker. An etching with peroxide was also performed as a reference. Some tests were performed on old wafers due to the limited supply of wafer with molybdenum. These old wafers came from failed blank transfer process, with molybdenum layer still remained on the wafer. All tests were performed on wafer with 50 nm of molybdenum covered by PDMS.

Table 5 Result of molybdenum etching with various etchant

Etchant	Result
H <sub>2</sub> O <sub>2</sub> (31%)	
FeCl <sub>3</sub> (40%)	
HNO <sub>3</sub> (69.5%)	
PES 77-19-04	

<p>Diluted PES 77-19-04 with DI water 1:1</p>	
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The hydrogen peroxide was tested with a wafer without graphene. The test was performed to see the performance of hydrogen peroxide in etching the molybdenum. The molybdenum was etched away completely after about 5 minutes. The etching of a full wafer molybdenum layer without graphene was never attempted before during this project. The PDMS layer was delaminated rapidly from the wafer within a few minutes after exposed to the hydrogen peroxide. Discoloration can be seen at the edge of the molybdenum where the etching process has begun. With the molybdenum removed, the PDMS lose its bond to the wafer. The PDMS is less dense than water or hydrogen peroxide which makes it float on the solution. The PDMS was then pulled from the edge by its tendency to float. As more area got delaminated from the wafer, more etchant can access the molybdenum from the top. With bigger force pulling the PDMS up than down to the wafer, the PDMS was delaminated before the molybdenum got etched completely.

This phenomenon was not happening with patterned molybdenum during the preliminary test. In patterned molybdenum, the PDMS was also coated on the silicon dioxide. The bond between silicon dioxide and PDMS kept the PDMS from delaminated from the wafer.

From the test, hydrogen peroxide worked well for the intention to transfer the PDMS. But when the wafer was bonded, the PDMS cannot float because it is being held by the target wafer. On the bright side, hydrogen peroxide can etch the molybdenum layer covered by PDMS.

The ferric chloride and PES showed similar results. After 20 minutes of etching both etchants failed to etch the molybdenum layer underneath the PDMS. The area outside of the PDMS got removed within the first 2 minutes, but between the 2 to 20 minutes, there was no change visually on the molybdenum layer. The  $\text{FeCl}_3$  was tested both in room temperature and elevated temperature with identical result. The inability of both etchants to etch underneath the PDMS layer might have something to do with their higher viscosity compared to hydrogen peroxide.

Dilution of PES was attempted by mixing it with DI water with 1:1 ratio. The dilution was done to reduce the viscosity of the PES. It turned out that dilution made the PES lost its effectiveness. Diluted PES was unable to etch the molybdenum including area that was not covered by PDMS.

The  $\text{HNO}_3$  showed a better start, the exposed molybdenum was removed within seconds. But as soon as it reached area covered by the PDMS, the etching stops. A test was performed with a drop of  $\text{HNO}_3$  applied on a cut made on the PDMS. The  $\text{HNO}_3$  reacted rapidly with the molybdenum, bubbles were forming as a by-product of the reaction. These bubbles stopped the etchant from progressing to other area. Looking at the chemical reaction of molybdenum and nitric acid, nitric oxide gas is produced from the reaction. After 20 minutes of exposure, the PDMS around the cut was swollen. From the study of PDMS chemical resistance, weight increase cause by nitric acid is twice higher than hydrogen peroxide [59].



From all the test with different etchants, hydrogen peroxide still showed as the most viable option as etchant for the molybdenum. With most etchants were unable to etch the molybdenum underneath a PDMS layer. The use of  $\text{HNO}_3$  had shown some promise, but the gaseous product of the reaction and the damage that it does to the PDMS made the hydrogen peroxide to be favored.

## 6.10. Nickel lift-off process

In the attempt to find another sacrificial layer to replace the photoresist, the use of nickel layer was investigated. A special property of nickel and silicon dioxide interface is utilized. This interface is susceptible to delamination when exposed to water. An entire layer of nickel on a wafer can be peeled off when it is submerged in the water. The nickel is often used as metal catalyst for graphene deposition. It can withstand the high temperature in graphene deposition. In the proposed process (Figure 41), nickel is used as sacrificial layer to delaminate the graphene and PDMS from the wafer. The metallization and patterning can be performed on the same wafer as the graphene deposition. A dicing foil is used to flip the structure upside down to perform the PDMS encapsulation on the back of the structure.

The process starts with deposition of 300 nm of thermal silicon dioxide in the furnace. The nickel layer with a thickness of 200 nm is then deposited using E-beam evaporation. The nickel layer is sealed by using 500 nm of silicon dioxide deposited using plasma-enhanced chemical vapor deposition (PECVD). This sealing is done to prevent moisture to get into the nickel and silicon dioxide interface. From this point, the transfer free graphene process is performed. The molybdenum layer is patterned before the graphene deposition. The titanium or titanium nitride is deposited as the metal contact for the graphene. The PDMS layer was then patterned using reactive ion etching. The edge of the wafer is damaged by using a blade to open the sealing made by the PECVD silicon dioxide. The dicing foil is attached, and nickel layer is peeled in the water with the help of the dicing foil. From the damage made by the blade, the water will reach the nickel and silicon oxide interface and delaminate the nickel from the silicon wafer. Remaining layers such as nickel, silicon dioxide and molybdenum are removed by using their respective etchants until graphene layer is the only layer remaining. The PDMS is spin-coated to finish the encapsulation of the graphene. The device is then removed from the dicing foil.

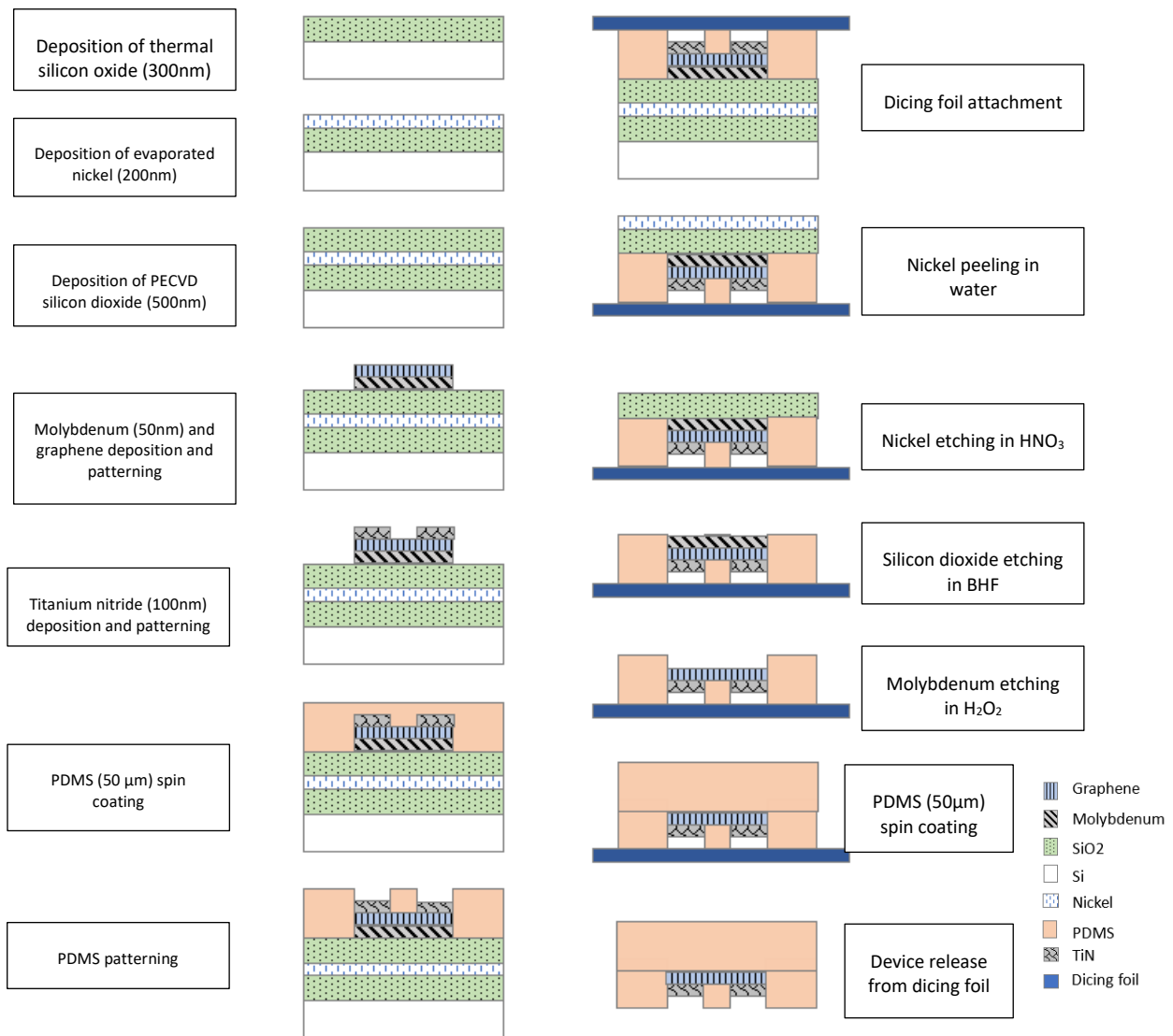


Figure 41 Simplified flow chart for the Nickel lift-off process.

Before investing all of the effort into the whole process. The peeling mechanism of the nickel needs to be tested. While nickel can survive the high heat of the graphene deposition process, in this process the nickel will be fully sealed in silicon dioxide. The accumulation of thermal stress can cause the nickel to break itself or the surrounding layer.

A test was performed with a wafer that was process up to the graphene deposition. The molybdenum was not patterned and a layer of PDMS was spin coated on top of the graphene (Figure 42). From this point, the nickel layer will be peeled by first damaging the silicon dioxide and then exposing it to water. A piece of Kapton tape was attached to one send of the wafer to help with the peeling process.



Figure 42 The test wafer for the nickel lift-off process. Incisions were made around the PDMS to break the silicon dioxide sealing.



Figure 43 (left) Close-up on the incision after the wafer is submerged in water. (right) The test wafer after the peeling attempt.

When the wafer was submerged in the water, the incision becomes clearer and wider (Figure 43). Some part of the nickel was peeled off. When peeling of the layer was attempted by pulling the Kapton tape, only the PDMS layer got peeled off from the wafer. The PDMS was not strong enough to pull the layer underneath. Another try was attempted without the PDMS layer. The Kapton tape was directly attached to the molybdenum layer. Some area was able to be peeled from the wafer but mostly it happened on the area directly in contact with the tape.

Upon closer inspection with the microscope, the molybdenum layer was damaged by the nickel layer. Nickel layer broke the silicon dioxide layer on top and it cracked the molybdenum layer.



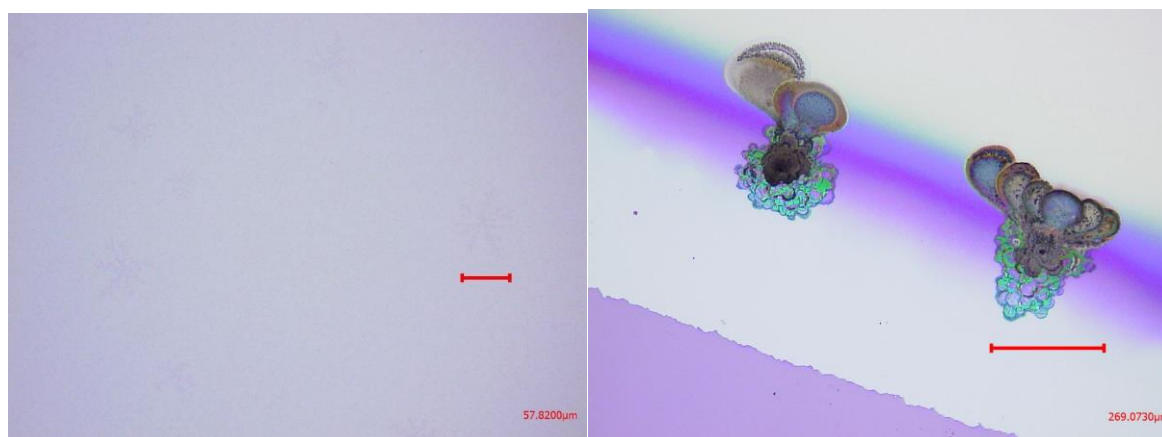


Figure 44 (left) Cracks on the molybdenum layer. (right) Nickel Diffusing out of the silicon dioxide.

These defects were observed when the graphene was deposited at 915°C. With lower temperature (850°C), defects were still spotted but these were fewer. These micro scale defects were probably the cause of the failure of the peeling process. The nickel layer expanded and diffused to its neighboring layer during the graphene deposition. With the failure of the peeling process, this process was no longer continued.

### 6.11. Etch and pick process

Another transfer process similar to the blank wafer transfer was devised. The blank transfer so far has yielded the best result with the issue of damage to PDMS occurred during long exposure to hydrogen peroxide and bad adhesion to the target wafer.

The final transfer process investigated was the etch and pick process. The idea of the process was found when exploring the effect of different etchants for molybdenum. A wafer with graphene and molybdenum coated with PDMS was etched by using PES. As previously reported, the etching process stopped at the area covered by PDMS. When this wafer was later etched in hydrogen peroxide, delamination of PDMS was not happened within the first 5 minutes. Instead, molybdenum layer was etched slowly until after approximately 20 minutes the PDMS was delaminated from the wafer. By using this phenomenon, the molybdenum can be etched partially after the PDMS layer was applied without delaminating the PDMS layer. This will reduce the amount of molybdenum that needs to be etched during the delamination process.

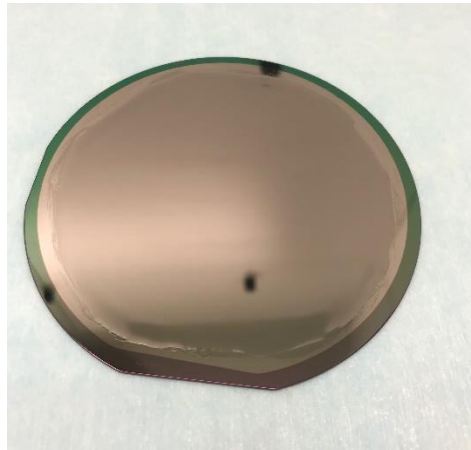
Two wafers were prepared similar to the blank wafer transfer process. The first wafer used for graphene deposition and the other wafer used for the patterning process. The graphene wafer contained a molybdenum and graphene layer coated with a fully cured PDMS (Figure 45). The graphene wafer will be etched in PES first for 2 minutes to remove the exposed molybdenum. After rinsing, the wafer was dried using the spin dryer. This process is important because it will cause the PDMS to create sealing around the molybdenum (Figure 46). This sealing can be seen on the wafer when the etching process in hydrogen peroxide is performed. The molybdenum at the edge of the PDMS was thicker than the center.

The sealing occurred when the PDMS became in contact with silicon dioxide. During the spin-drying process, the PDMS can be forced to move due to centrifugal force and became in contact with the surrounding silicon dioxide. The sealing slows down the etching process of the molybdenum by limiting the etchant access to the molybdenum. The hydrogen peroxide still can access the molybdenum from some area and etch the

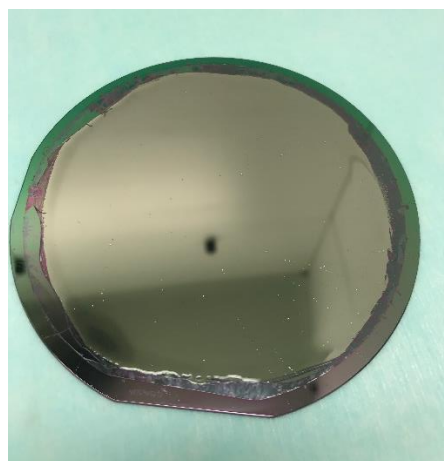
molybdenum from the middle. As shown in [60], the bond strength between PDMS and silicon dioxide is quite strong. The PDMS was held back from floating by its bond to the silicon dioxide.

The sealing effect is limited by the thickness of the molybdenum layer. The use of 200 nm and 300 nm of molybdenum for this process was attempted. But the sealing effect did not happen. This could be caused by the movement of PDMS during the spin-drying process could not cover the 200 nm distance to the silicon dioxide to create the sealing.

As the wafer was being exposed to hydrogen peroxide, the effect of the sealing became more apparent. When the molybdenum at the middle was already turned a little reddish signifying a change in thickness, the molybdenum at the edge of the PDMS was still metallic in color (Figure 47). This metallic ring will become smaller during the etching process. The ring will be gone typically between 15 - 18 minutes of etching. When the ring is removed, molybdenum etching will become faster and delamination of the PDMS will soon follow. So, the first etching of the molybdenum can only be performed at most for 15 minutes.



*Figure 45 Starting material for the etch and pick process. The graphene wafer coated with 50 μm of PDMS.*



*Figure 46 The wafer after 2 minutes of etching in PES*

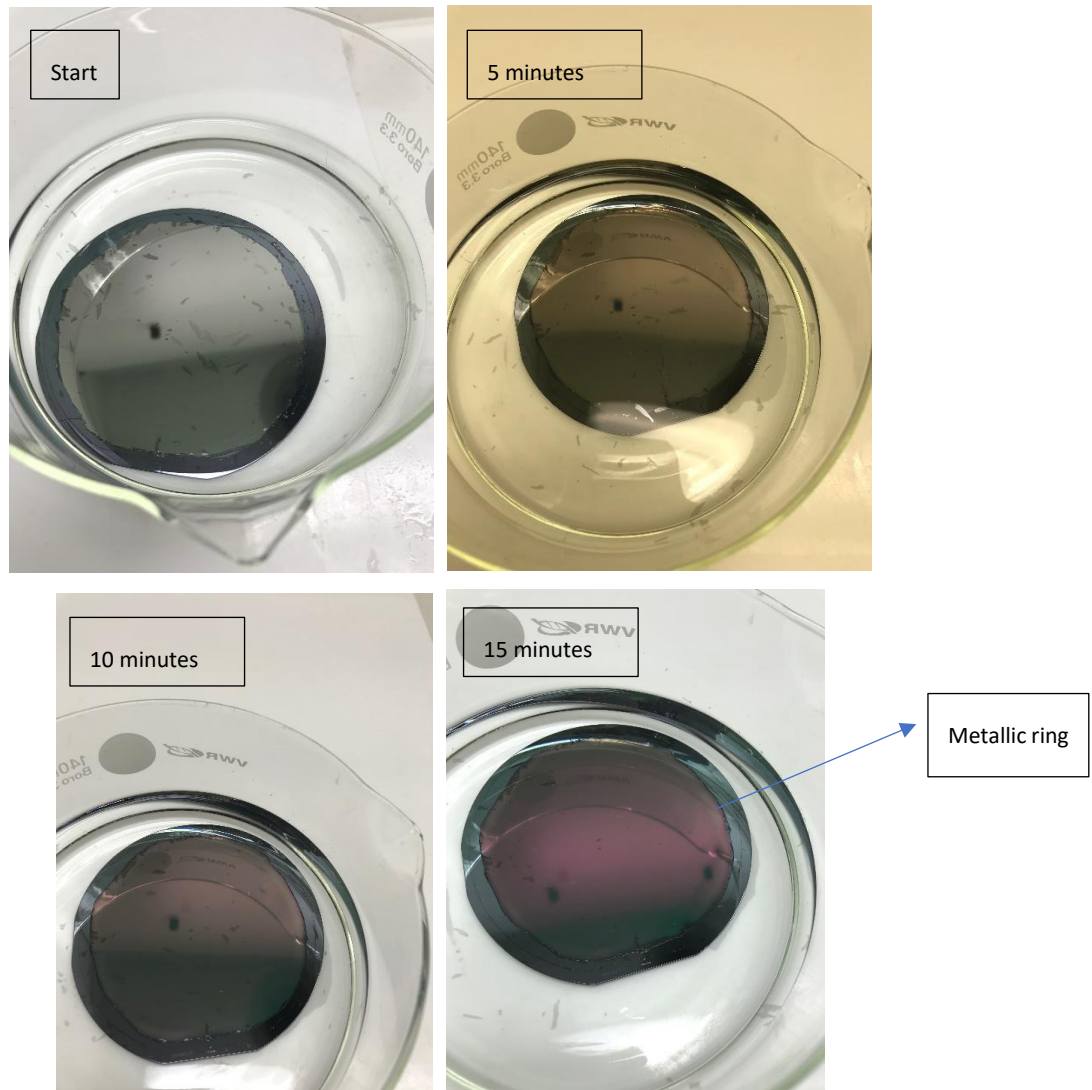


Figure 47 The changes occurred on the wafer within 15 minutes in  $H_2O_2$ . A metallic ring at the edge of the PDMS was seen.

As long as the molybdenum layer turned to a more reddish color, bonding process can be performed. As the target wafer, a wafer with alignment markers was coated with  $50\mu m$  of PDMS. This PDMS acts as the replacement of photoresist for the release mechanism of the device. After the dicing process, the device can be removed from the target wafer. While the PDMS that was spin coated on the silicon wafer will remain on the wafer. This PDMS also has a role to catch the PDMS on the original wafer. The PDMS to PDMS interface can result in a stronger bond compared to the PDMS – photoresist bond. Following the data in Figure 25, partial curing scheme was performed on the wafer on the target substrate. For this PDMS, curing was performed at  $60^\circ C$  for 30 minutes. Immediately after the curing process, the graphene wafer and the target wafer were bonded manually by hand. The use of the wafer bonder was avoided since the force delivered in low settings was not accurate. With the PDMS-PDMS interface, a large force is not necessary to promote bonding, large force will only increase the chance of wrinkles to form on the PDMS.

The wafer stack was allowed to rest overnight to let the partially cured PDMS to be fully cured. The separation process was performed in a vertical bath (Figure 48) filled with hydrogen peroxide. The wafer stack needs to be etched vertically to avoid the weight of the top wafer to push the PDMS and seal the molybdenum layer.

As learned during testing the hydrogen peroxide, the delamination of PDMS from the original wafer can help the etchant to access the molybdenum and increase the etch rate.



*Figure 48 The glassware and wafer carrier used in the separation process.*



*Figure 49 Target wafer after delamination process of the etch and pick process.*

The wafer stack is exposed to the hydrogen peroxide on average for 1.5 hour. The wafer stack need to be rotated every 20 minutes to help the flow of etchant on the wafer interface. After separation process, it can be seen that the graphene and the PDMS layer was transferred to the target wafer with minimum damage compared to the past attempts (Figure 49).

Some darker spots can be seen on the wafer because of graphene flakes redeposition. These flakes were trapped on the PDMS interface and cannot be removed after the bonding process. By removing the flakes floating on the solution everytime, this issue can be avoided.

## 6.12. Summary

The transfer process of graphene has shown that it is not a simple process. The transfer process based on the blank transfer showed a promising outcome compared to transferring a patterned layer of graphene. The strong adhesion between PDMS and silicon dioxide made it difficult to remove PDMS layer that was coated on top of a silicon dioxide.

There were several shortcomings of the blank transfer process. The long etching time during the separation process caused damage to occur on the PDMS layer. The adhesion of the PDMS to target wafer was also a concern, with a lot of tests ended up failing due to the delamination of the PDMS from the target wafer.

Improvements on the etch rate were explored. The attempt to secure entry points for the etchant to the molybdenum layer through wafer cleaving and photoresist ring provided improvement on the etch rate but both wafer cleaving and photoresist ring caused their own set of problems. Different etchants such as  $\text{FeCl}_3$ ,  $\text{HNO}_3$ , and PES were explored, but each failed to etch the molybdenum layer underneath the PDMS.

The use of nickel as lift-off layer with high thermal budget was ended with failure. Although it is heat resistant, the accumulated thermal stress on the nickel layer damaged the other neighboring layer. Because of the defects from the thermal stress, delamination of the nickel layer from the wafer was no longer possible.

After all of those attempts, a new process was made. The idea of process was to etch the molybdenum twice to lessen the amount of molybdenum to etch during the separation process. The molybdenum was etched partially after the PDMS coating. After it was being bonded to a target wafer with a partially cured PDMS layer on top, the separation process was done in the hydrogen peroxide.

The etch can be done faster than the separation process in the normal blank transfer process. Separation process in the etch and pick process can be done in 1.5 hour to 2 hours. The simplified version of the process flowchart can be seen in Figure 50.

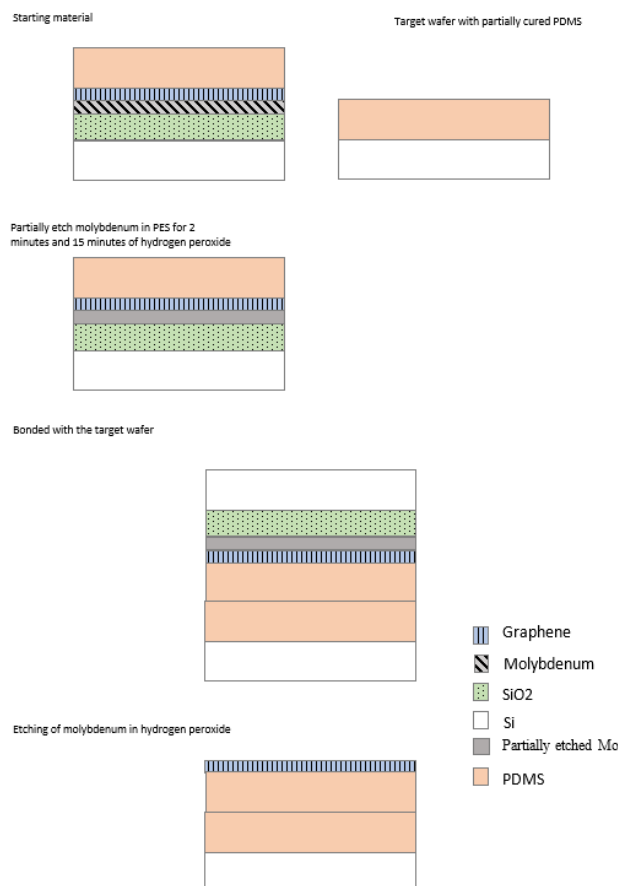


Figure 50 Simplified flowchart for etch and pick process.

## 7. Graphene Patterning

### 7.1. Reactive ion etching of graphene

Following the transfer process, the transferred graphene layer needs to be patterned. The graphene layer is patterned by using oxygen plasma. Rao et al. (2011) have reported the etching of monolayer graphene on silicon dioxide by using reactive ion etching (RIE) with 70 W power for 15 s [64]. A similar setup was tested by using the multilayer graphene used in this project.

A test was performed on a transferred graphene layer on PDMS. The SPR-3012 photoresist with the thickness of 2.1  $\mu\text{m}$  was used as the masking layer (Figure 51). The multilayer graphene had more than 5 layers of graphene. Thus, it was expected that the etching time will take longer than what was reported. The pattern for the photoresist was not produced by the mask that had been designed for this project. At that time, the mask was still unavailable and thus another mask was used to see if the graphene patterning was feasible.

*Table 6 The etching parameter for graphene.*

Power	60 W
Oxygen flow	20 sccm
Helium flow	55.6 sccm
pressure	0.05 mbar

The sample was etched for 2 minutes with the recipe in Table 6. Visual inspection was performed using a microscope (Figure 52). But from visual inspection alone, the transparent layer of graphene was difficult to identify. While normally, the presence of a graphene layer can be identified with the use of Raman spectroscopy which was placed outside of the cleanroom, further processes cannot be performed with sample brought outside of the clean room. Cracks were forming at the area around the photoresist. The cracks were thought to be the graphene layer. The etching was continued for another 2 minutes and after seeing that nothing was changed under the microscope, an additional 2 minutes of etching was performed.

The photoresist layer was then removed to see if there is any difference between the area exposed to plasma and covered by photoresist. After exposed to acetone, the photoresist layer was not able to be removed. The exposure of plasma cured the photoresist. The photoresist was suspected to receive excess heat from plasma exposure. The PDMS is also not good at conducting heat thus trapping the heat in the photoresist. Even after being soaked for 3 days in acetone, the photoresist was not able to be removed. The NMP solution at 50°C was used instead of acetone. The photoresist layer was removed, but the graphene layer was heavily damaged. In most part, the graphene layer was removed. The photoresist was not dissolved in the solution but rather peeled off from the wafer. The peeled photoresist seemed to bring the graphene layer as it was delaminated from the wafer.

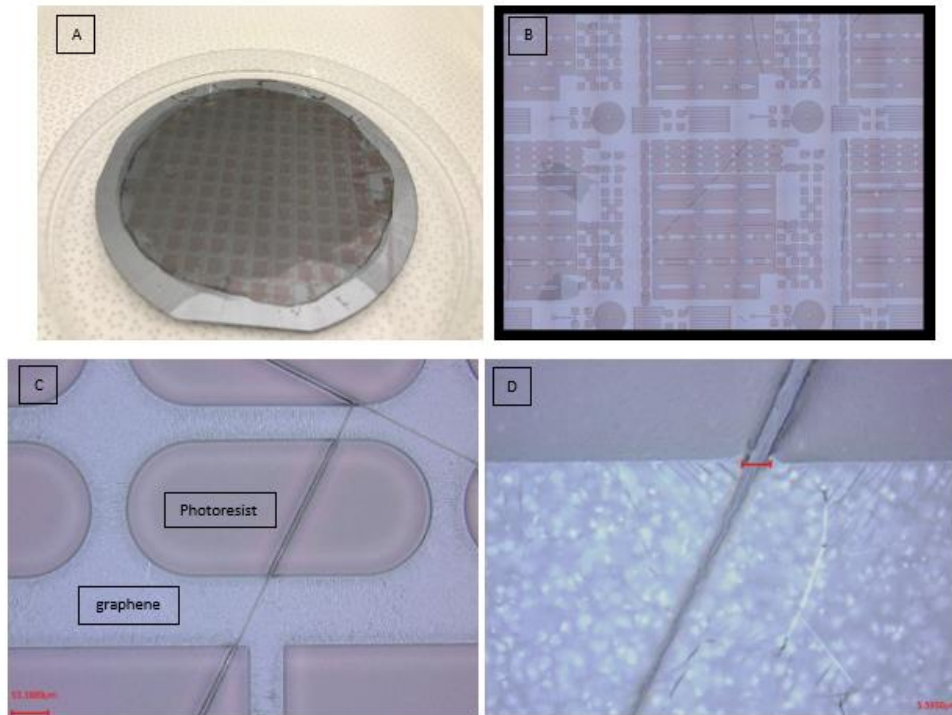


Figure 51 (a) The test wafer before the etching process. (b) overview of the pattern. (c) View of the pattern with 10x magnification. (d) A close-up look of the pattern with 150x magnification.

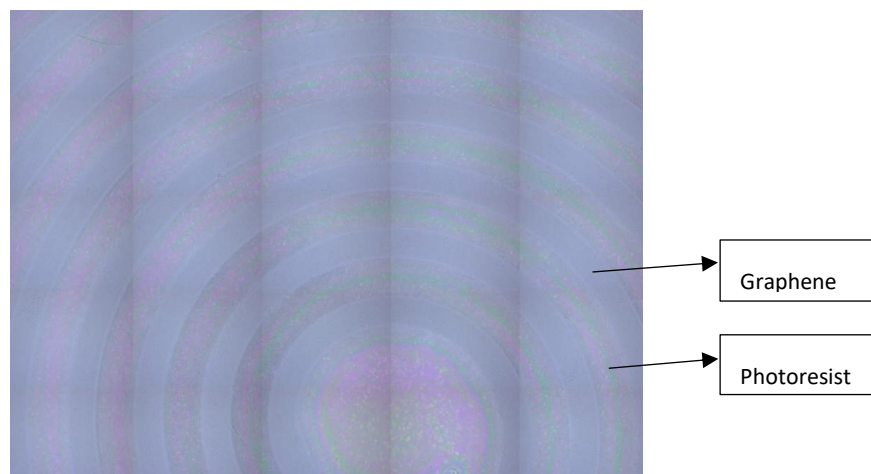


Figure 52 The test wafer after plasma exposure of 6 minutes

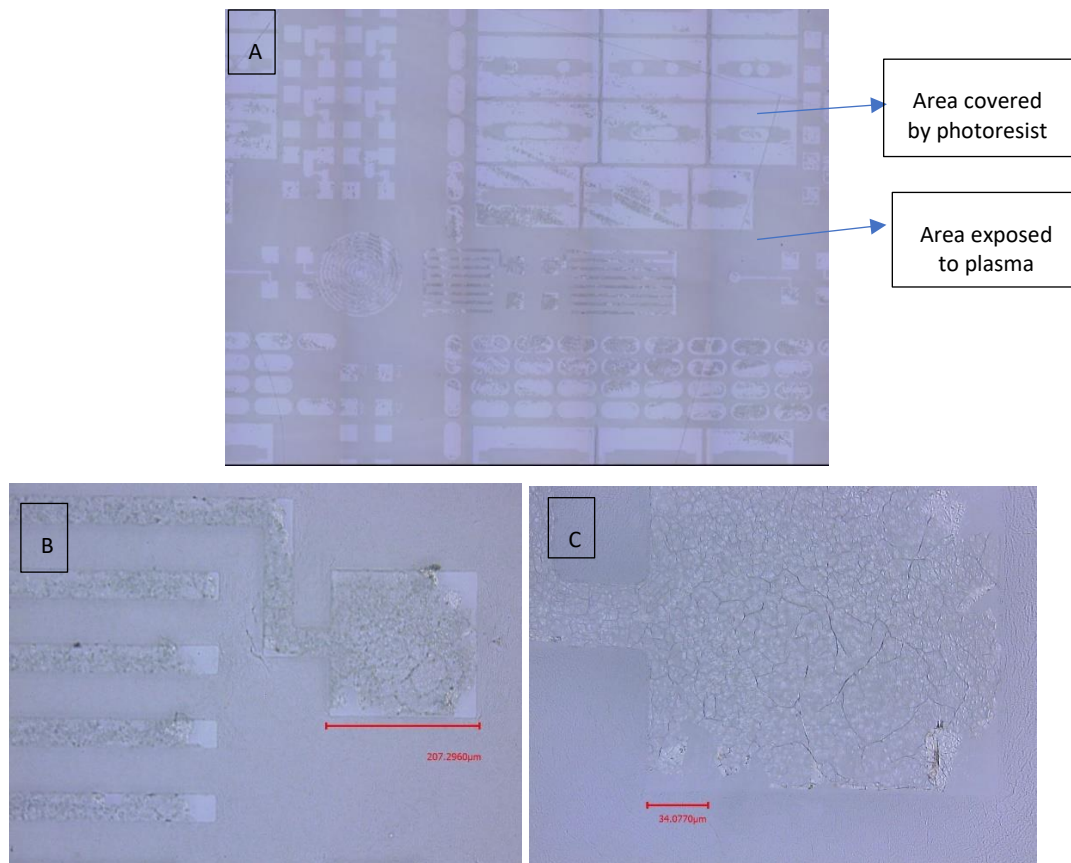


Figure 53 The test wafer after photoresist stripping. (a) overview of the pattern. (b) Remaining graphene layer. (c) A closer look of the remaining graphene layer with 50x magnification.

After the photoresist was removed from the wafer, Raman spectroscopy was performed on the wafer. The presence of graphene can be confirmed when three peaks are spotted on three different Raman shifts. Graphene presence is indicated by the ratio of these peaks rather than the intensity, as the intensity of the reading is dependent on the type and condition of the laser and the reflectance of the sample. The first is the G-peak which occurs around  $1584\text{ cm}^{-1}$ , this band relates to the  $sp^2$  hybridization of carbon atoms in graphene. This peak will become more prominent in multilayer graphene which has more carbon atoms compared to monolayer graphene. The second is the D-peak at  $1350\text{ cm}^{-1}$ . This peak relates to any kind of defect occurring on the  $sp^2$  hybridization. The final peak is the 2D-peak at  $2700\text{ cm}^{-1}$ [65]. This peak is more prominent in monolayer graphene. The number of layers in graphene can be identified by comparing the intensity of the G-peak and the 2D-peak. Figure 54 shows the relationship between the number of layers with the G-peak and 2D-peak ratio.

The Raman spectroscopy was performed on three samples. One sample was the graphene layer on silicon dioxide. The graphene layer from this sample was obtained through the same process recipe as the one on the PDMS layer. The second sample was the transferred graphene on PDMS before any plasma exposure. The final sample was the wafer with patterned graphene on PDMS. From these samples, the condition of the graphene after each process can be compared.



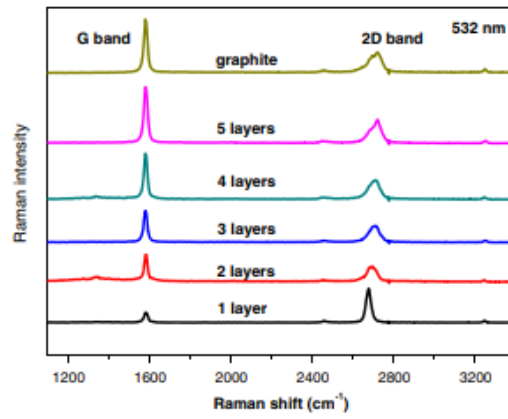


Figure 54 The Raman spectroscopy result for different number of graphene layers[66].

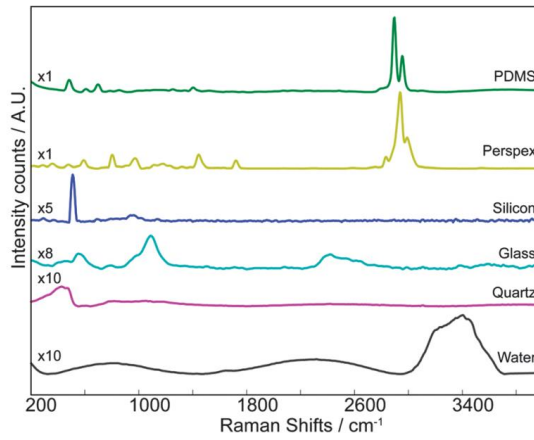


Figure 55 Raman spectra of PDMS and silicon[67].

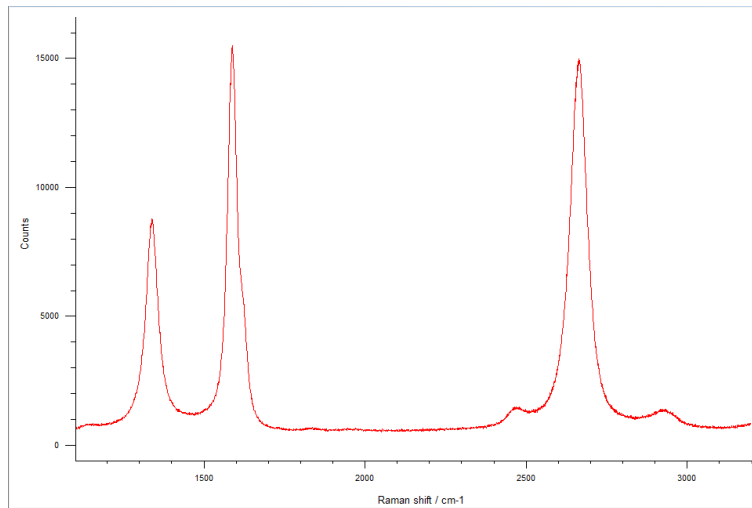


Figure 56 The Raman spectroscopy result on multilayer graphene on silicon dioxide.

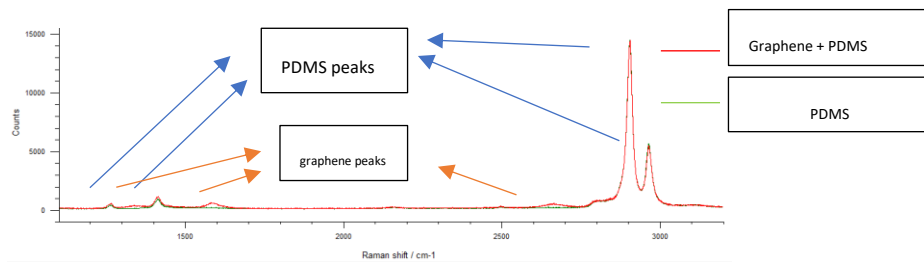


Figure 57 The Raman spectroscopy of graphene on PDMS before plasma exposure.

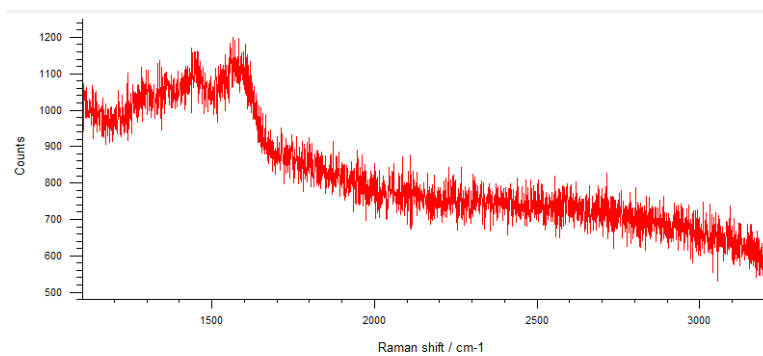


Figure 58 The Raman spectroscopy of graphene patterned with RIE on PDMS.

The graphene layer on the silicon dioxide (Figure 56) showed a prominent G-peak and 2D-peak, suggesting a multilayer graphene. The exact number of layers past 5 layers of graphene cannot be determined by Raman spectroscopy. A strong D-peak also suggests that the graphene layer contained a considerable amount of defect[65].

In Raman spectroscopy, every layer on the sample will contribute to the measurement. The contribution of the materials in a sample possess a superposition property. As long as other materials don't possess a peak in the position as the graphene peaks, the identification of the graphene layer can still be performed.

The result of Raman spectroscopy on transferred graphene on PDMS showed two strong peaks between 2900  $\text{cm}^{-1}$  and 3000  $\text{cm}^{-1}$ . Comparing it to the PDMS Raman spectra, these peaks were contributed from the PDMS along with the peak on the 1500  $\text{cm}^{-1}$  and 1300  $\text{cm}^{-1}$  Raman shift. The graphene peaks were still sighted in the measurement result. Although considerably smaller than the PDMS peaks; the D-peak, G-peak, and 2D peak were all discernible. Influence from the PDMS spectra may be occurring on the 2D-peak and D-peak as they are closely located to the PDMS peaks. The intensity of the G-peak was almost equal to the 2D-peak which was also the case on graphene spectra on the silicon dioxide.

The Raman spectroscopy was performed on the etched graphene layer on PDMS Figure 58. The measurement was performed on the area exposed to the plasma. Compared to the other measurements, the signal read during the measurement was significantly lower. A weak G-peak was detected on the sample This was showing that after being exposed to 60 W plasma for 6 minutes,  $\text{sp}^2$  hybridization carbon bonds still exist on the wafer. The plasma was not only affected the graphene but also the PDMS. The PDMS prominent peaks were not detected in the measurement result. The two peaks below the 1500  $\text{cm}^{-1}$  could be the PDMS peaks but it is inconclusive with considering the weak intensity of the spectra.

## 7.2. Graphene etching with the barrel plasma chamber

### 7.2.1. Test using graphene on silicon dioxide

Unfortunately, the used RIE machine was down at a later stage of the process and had not been repaired until the writing of this thesis. As a replacement, the barrel plasma chamber was used to etch the graphene. Compared to RIE, this plasma chamber does not have electrical biasing between the power source and the wafer that direct the ions in the chamber to the wafer, resulting in isotropic etching. With less directionality of the ions, the etching process of the graphene layer may take longer time and higher plasma power.

The use of a barrel chamber to etch graphene was documented by Jia et Al. (2017), oxygen plasma with 150W power was used to etch a multilayer graphene on silicon dioxide[68]. The thickness of a multilayer graphene was reduced from 8.4 nm to 0.6 nm after 180s of etching. Although 0.6 nm of graphene was still detected after 3 minutes of plasma exposure, a significant reduction of the graphene current density was reported after plasma exposure (Figure 59).

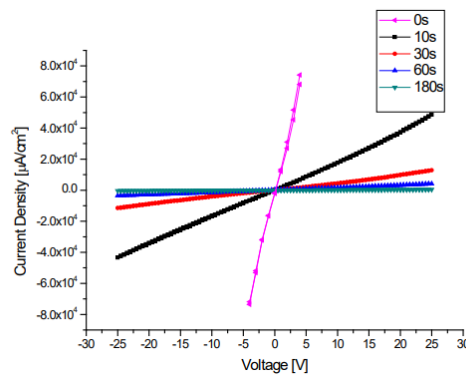


Figure 59 The graphene I-V characteristic of different cumulative plasma exposure [68].

To see if the same result can be replicated in our clean room, a test was performed with a graphene layer on silicon dioxide. The wafer from the transfer-free graphene process was used. Only two power settings were available in the plasma chamber, 100 W and 500 W. A single wafer was cleaved into 4 pieces, two quarters were used to test the etching process with 100 W and 500 W power. One quarter was used as a reference and the last quarter was used as a spare to proof a recipe from the test quarters.

Table 7 The test arrangement and result for graphene etching with a plasma chamber.

Quarter	Treatment	Resistance	Cumulative etch time
A	100 W	~500Ω	7 mins
B	500 W	>60 MΩ	50 mins
C	Reference	~400 Ω	0 min
D	Proof sample (500W)	>60 MΩ	1 min

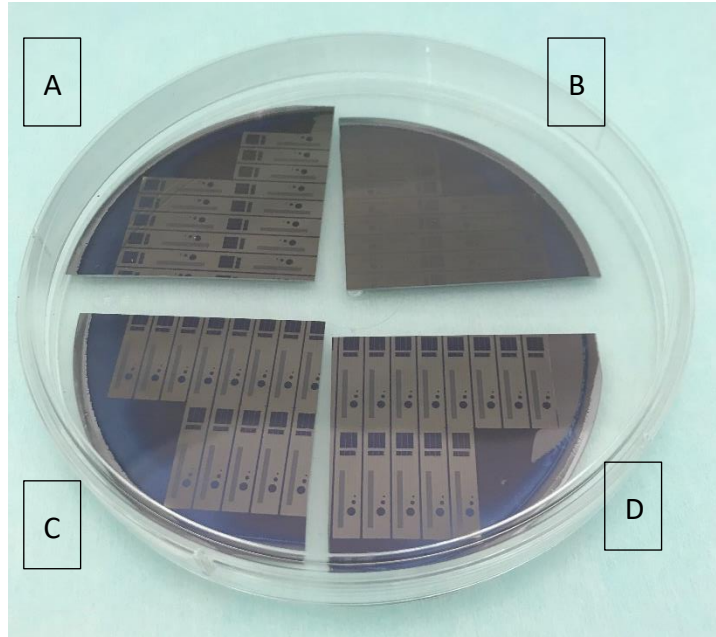


Figure 60 The cleaved graphene wafer for testing the plasma exposure recipe. Quarter A and B are exposed to the plasma. Quarter C and D are untreated.

The first test was performed on wafer A with 100 W power setting. The test was performed until there is a visual change on the graphene layer. The use of 100 W was closer to the 150 W power compared to 600 W. With lower power, longer etching time than 3 minutes was expected. After 7 minutes of plasma exposure, the colour of the graphene layer remained unchanged.

For the 500 W power setting, there was only one recipe with 10 minutes of etching time available. This recipe was tested with quarter B. After 10 minutes, the color of the graphene layer was fading. Although the pattern of the graphene was still able to be seen. The etching process was continued to see if the graphene can be completely removed until the pattern becomes indistinguishable. The recipe was repeated 5 times and no further change to the graphene was seen.

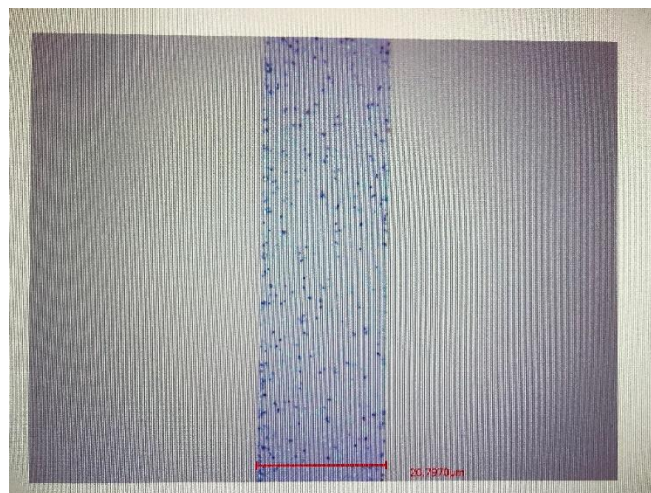


Figure 61 Quarter B after 50 minutes of 500 W plasma exposure.

A simple electrical measurement was performed with a multimeter. Contact with the graphene layer was established by using a silver paste to prevent puncturing the graphene layer with the probe. The paste was applied at two points on each quarter with approximately the same distance. Since there can be a variation to

the distance of the points, a comparison can only be made to the order of magnitude of the resistance. The reference wafer showed a resistance of about 400  $\Omega$  and the sample exposed to the 100 W showed resistance in the same order of magnitude. The sample treated with 600 W plasma overloaded the resistance measurement of the multimeter which has a maximum range of 60M $\Omega$ .

When the graphene etching was performed with RIE, the issue with the burned photoresist was encountered. The burned photoresist was not possible to be removed by using acetone, the removal process was also removing the graphene layer underneath it. To avoid this issue when processing with the plasma chamber, the time limit of plasma exposure for the photoresist was tested.

The SPR-3012 photoresist with 2.1  $\mu\text{m}$  thickness was used for the test. Because the 600 W plasma was proven to be able to etch the graphene layer. The setup for the test was simple, the sample was exposed to the plasma for a certain amount of time and then the photoresist was exposed to acetone. The exposure time was increased until the photoresist was no longer able to be removed by acetone. The test started with exposure of photoresist for 30 seconds. The photoresist was still able to be removed with acetone until 1 minute and 10 seconds of exposure.

From the information about the photoresist maximum exposure time, quarter D of the graphene wafer was used to see if after 1 minute in 600 W plasma, the graphene layer is able to be etched. After 1 minute of exposure, a similar fade in color was seen on the graphene layer. The electrical resistance of the graphene layer was measured to be above 60 M $\Omega$ .

### 7.2.2. Test using graphene on PDMS

With the result of the previous test, a graphene layer on PDMS was coated with 2.1  $\mu\text{m}$  of photoresist. After 1 minute of plasma exposure, the photoresist was removed successfully with acetone. The electrical resistance of the exposed layer was measured and compared with the resistance of the covered area. As previously done, contact to the graphene was made with the help of silver paste. An electrical resistance in the order of k $\Omega$  was still measured on the exposed area. On the covered area, electrical resistance in the order hundreds of ohms was measured similar to the previous test. It shows that the etching process also depended on another parameter apart from plasma power. Most likely it is caused by the temperature of the substrate. A certain temperature is needed to activate the chemical reaction during plasma exposure. The PDMS has a heat capacity of 118 J/K.mol[69] while silicon dioxide has 44.21 J/K.mol[70] at the same temperature. The heat capacity shows that more energy is required to increase the temperature of the PDMS compared to the silicon dioxide. Longer exposure to plasma is required to achieve a similar result with the test on silicon dioxide.

Increasing the exposure time will increase the risk of burning the photoresist. A metal hard mask was used instead of photoresist. Metals can withstand long exposure of oxygen plasma with minimum damage. The only drawback is the extra fabrication step to create the mask.

The aluminum with 1% silicon was used as the material for the mask. The thickness of the aluminum was 200 nm and it was sputtered on the graphene layer with low power (1 kW) to avoid damaging the PDMS. The patterning process for the mask had to be performed by wet etching since the graphene layer was directly underneath. The wafer was soaked in PES 77-19-04 aluminum etchant for approximately 5 minutes.

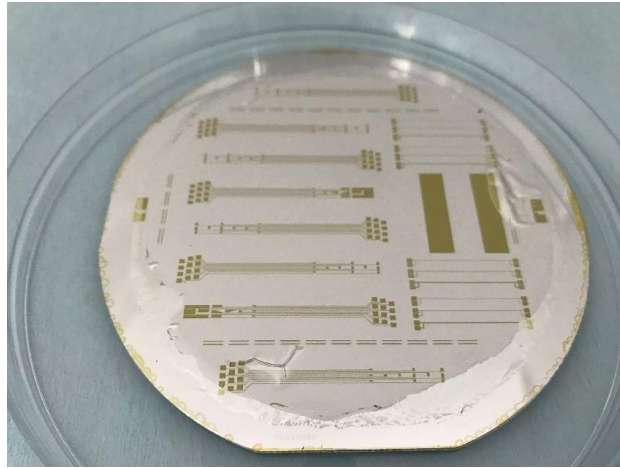


Figure 62 Graphene on PDMS coated with aluminum. The photoresist was patterned on top of the aluminum.

After soaked in PES, some parts of the aluminum mask were delaminated. The delamination occurred mostly on interconnects and small features. Due to the isotropic nature of wet etching, undercuts might cause the delamination of the small structures. It is also known that the adhesion of metals to graphene is typically weak. Better optimization on the etching time is therefore required to keep the masking layer intact.

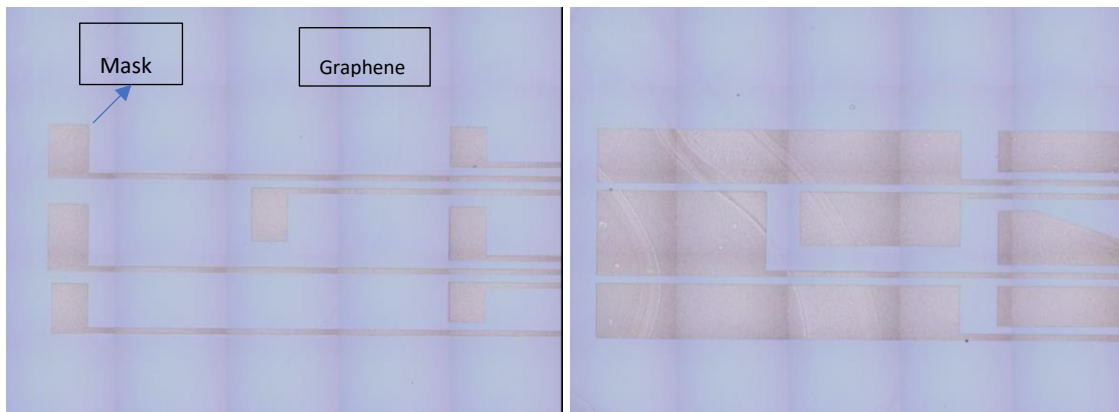


Figure 63 The electrode array hard mask.

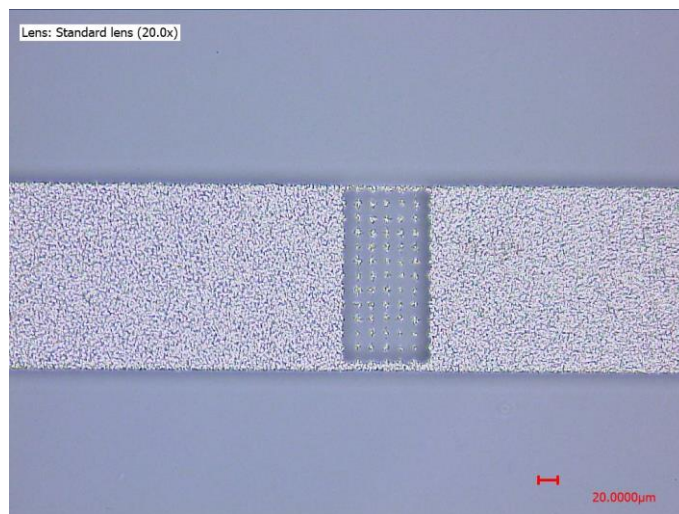


Figure 64 The TLM structure. The holey structure managed to be fabricated on the mask.

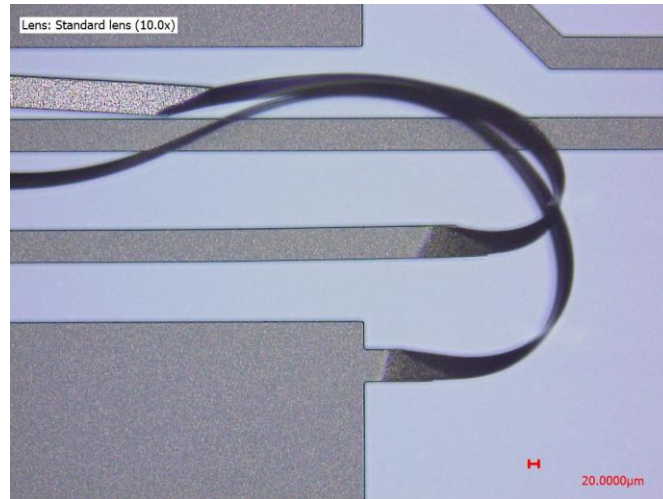


Figure 65 Delamination of interconnects.

After 4 minutes of cumulative exposure to oxygen plasma, the resistance of the exposed graphene layer was overloading the multimeter reading. The electrical measurement was performed on the exposed structure for the optical transmittance test. Visual changes to the graphene were observed through the microscope. The same area was examined each time to see how the graphene changes after each plasma exposure.

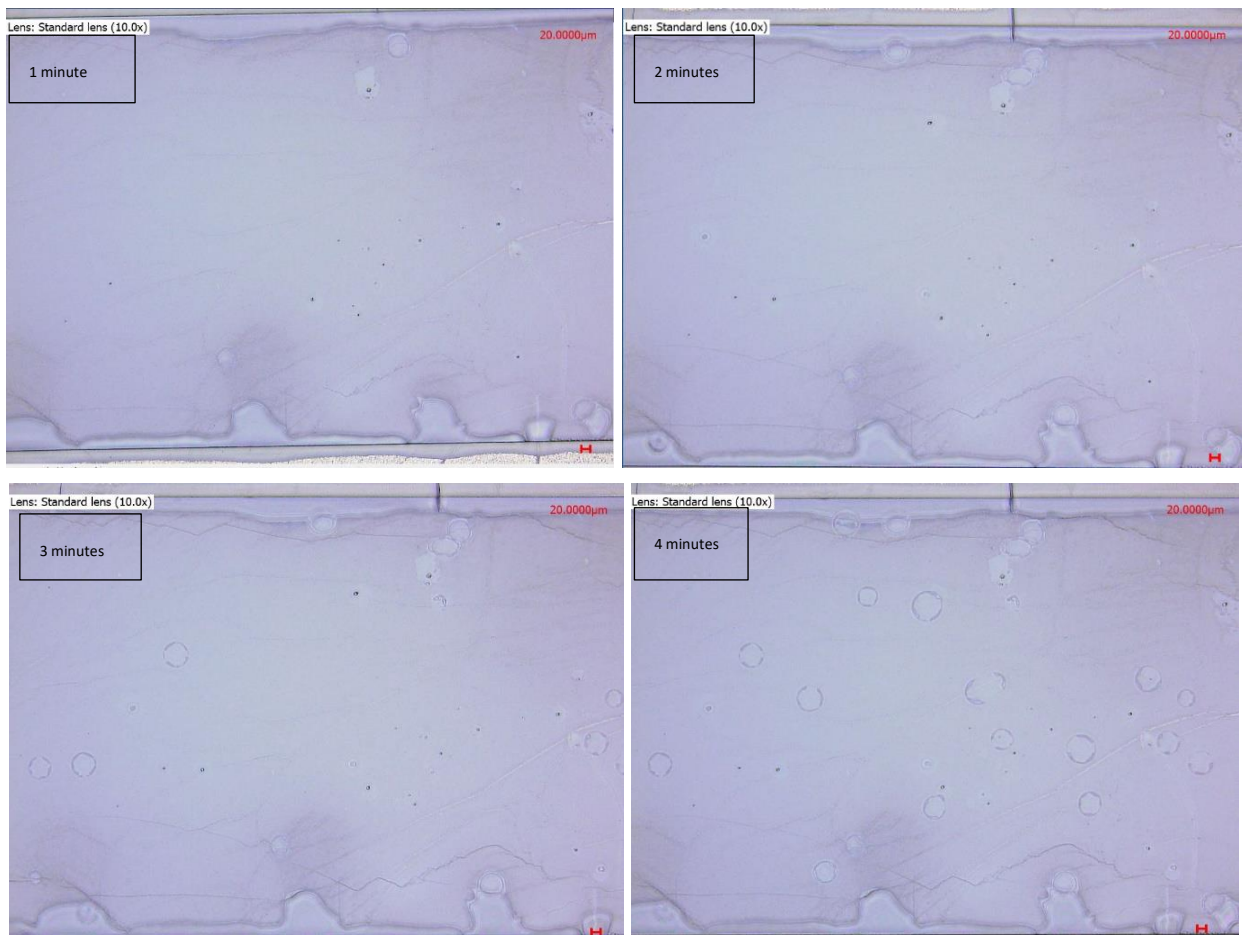


Figure 66 Changes to the exposed graphene layer over time.

The process was continued with removing the mask in PES solution for 10 minutes. Under the microscope, the area that was exposed and covered can be recognized. The resistance of the area covered by the mask was measured, sadly high electrical resistance in the order of  $k\Omega$  was also measured.



Figure 67 The remaining graphene layer after the metal mask was removed.

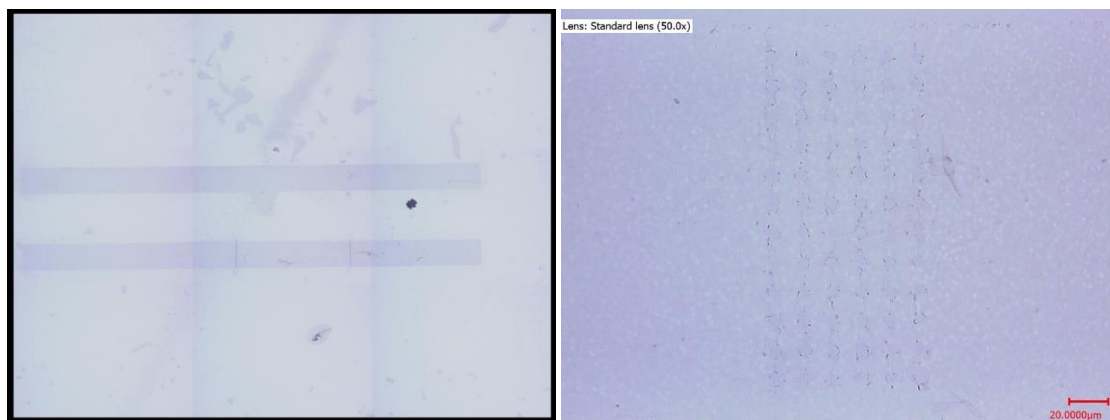


Figure 68 The TLM structure after the metal mask was removed. (left) The overview of the TLM structure. (right) the close-up on the holey structure.

### 7.3. Different approach on graphene etching with plasma chamber

Based on previous test on graphene etching, the reaction occurred between the graphene and oxygen plasma is temperature dependent. In the previous test, after each exposure to plasma for 1 minute, the sample was taken out of the plasma chamber to be inspected under the microscope to see if the graphene layer is already etched. During the inspection, temperature of the chamber was going down, thus it was probable that the sample never reach the necessary temperature for optimum reaction.

Another test was performed using the same recipe with 600W of oxygen plasma for 1 minute, but the sample was exposed twice before performing inspection on the sample. By doing this, the temperature of the chamber after the first exposure was kept for the second exposure. The maximum temperature of the chamber during the second exposure was increased by  $8^{\circ}\text{C}$ , from  $39^{\circ}\text{C}$  from the first exposure to  $47^{\circ}\text{C}$  during the second exposure.



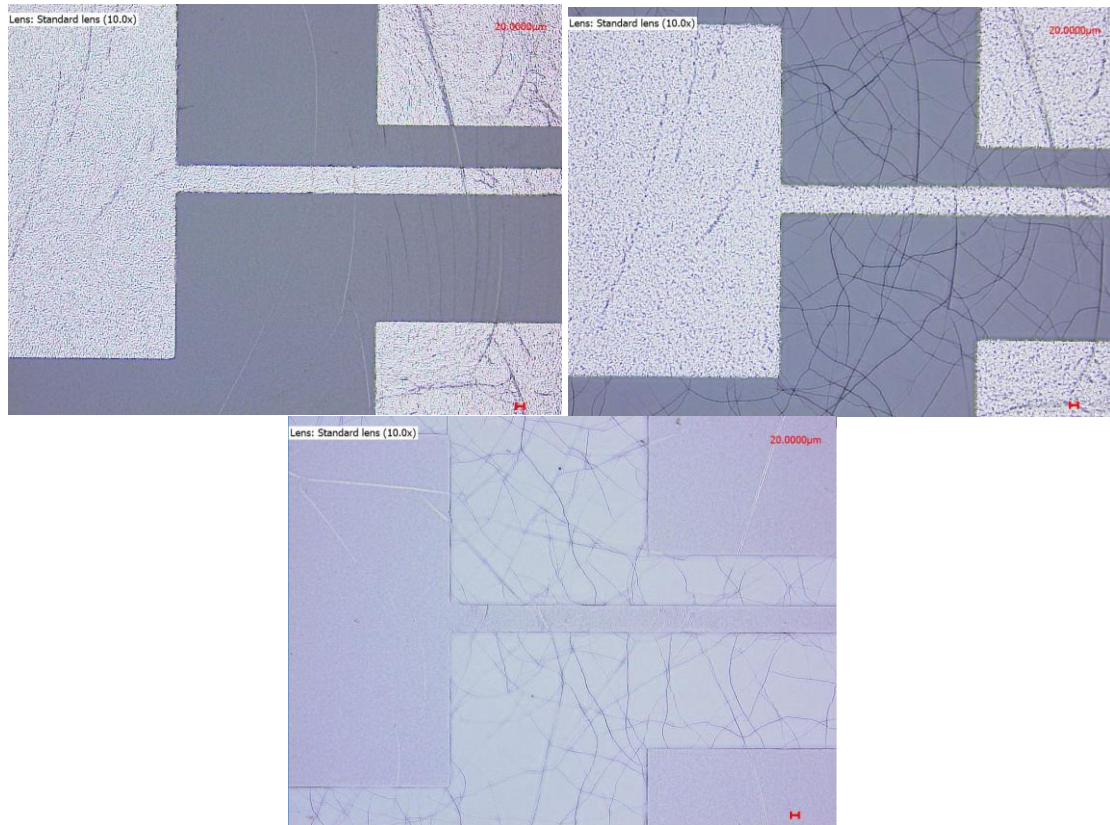


Figure 69 The result of graphene etching for 2 consecutive minutes on the electrode array contact pads. (a) Before the plasma exposure. (b) After 2 minutes of plasma exposure. (c) After the aluminum hard mask was removed.

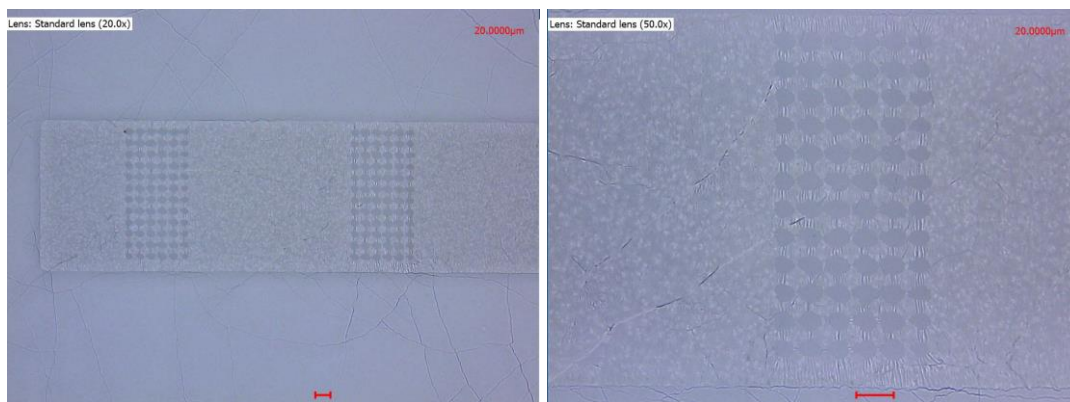


Figure 70 The patterned graphene layer for holey TLM structure.

Using this way of doing the plasma exposure, the contrast between the exposed and covered area can be seen. A comparable result can be seen on the holey structure fabricated. A sharper structure was able to be produced compared to the graphene patterned with 4 minutes of non-consecutive exposure. Holes with a diameter of  $10\ \mu\text{m}$  were produced in the holey graphene structure. Defects from the aluminum mask was transferred to the resulting graphene pattern.

The electrical resistance measurement showed that exposed area had resistance more than  $60\ \text{M}\Omega$ . On the other hand, the covered area retained electrical resistance around  $500\ \Omega$ . This indicate that there is a certain limit of exposure to plasma that the aluminum hard mask can handle before damage starts to occur on the graphene layer. The oxidation of the aluminum mask was seen after the sample was exposed to plasma more than 3 minutes. Even after 2 minutes of plasma exposure, oxidation to the aluminum can be seen during the removal of the mask after the exposure process. The aluminum

mask that was etched in 5 minutes during the patterning took more than 10 minutes to be removed after the exposure.

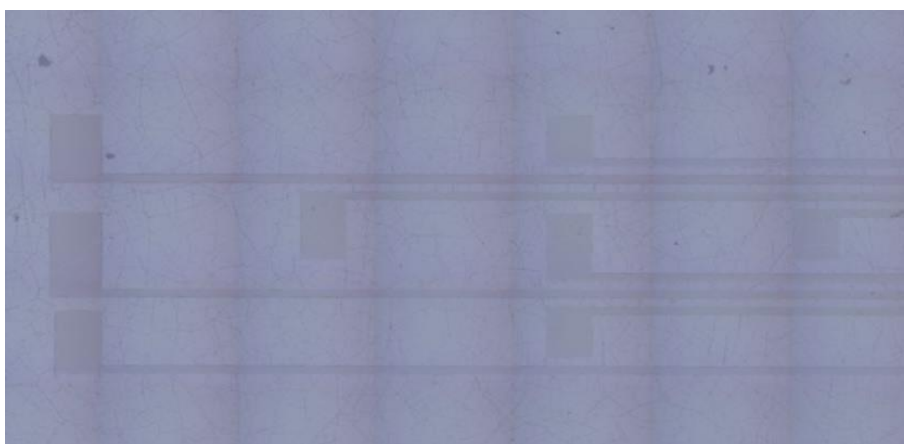


Figure 71 Overview on the graphene electrode array with no metal compensation scheme.



Figure 72 The patterned graphene layer.

Although the exposed graphene layer was seen to be completely removed after the patterning process, a closer look on area with defect from the transferring process showed the comparison between graphene exposed to oxygen plasma and the PDMS substrate. After the transferring process, some area of the graphene might not be transferred or delaminated because of bubble formation or unremoved molybdenum. A closer look to this area showed us that from the etching process, there is a residual layer from the graphene etching process.

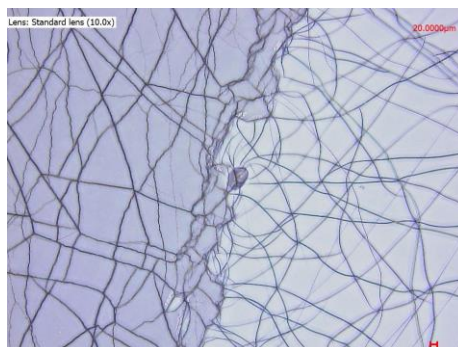


Figure 73 A closer look on the defect area after the etching process. The left side is the exposed graphene layer and to the right is area with no graphene before the exposure.

## 7.4. Summary on graphene etching

To summarize, the etching process using plasma chamber is more difficult than the use reactive ion etching but it is still plausible. The use of the aluminum hard mask is recommended to avoid burnt photoresist due to plasma exposure. However, there is also a limit of exposure that can be performed with the aluminum mask. The etching process of graphene relies on temperature dependent reaction. The use of 2 minutes consecutive exposure with 600 W oxygen plasma has shown a satisfying result in both structural quality and electrical performance. Holes with a diameter of 10  $\mu\text{m}$  was made in the TLM structure. The patterned graphene managed to retain its electrical resistance after patterning process.

Defect on the mask is transferred to the graphene layer. The use of aluminum did not provide a good adhesion to the graphene layer. The uneven surface of PDMS caused cracks on some area of the aluminum. The use of other metal with higher adhesion to graphene still need to be explored.

Similar to the graphene etching on silicon dioxide, graphene on PDMS was not able to be completely removed. A residual non-conductive layer (presumably made of carbon) remained on the PDMS. A distinguishable pattern was probably seen on the wafer due to exposed area became thinner than unexposed area.

A significant damage to the PDMS can be seen after 2 minutes of consecutive exposure. The high power and temperature of the exposure process caused cracks to appear on the PDMS. The formation cracks on PDMS can cause a reliability issue on the electrode array and may increase the scattering effect of light which reduce the total transmittance of the PDMS.

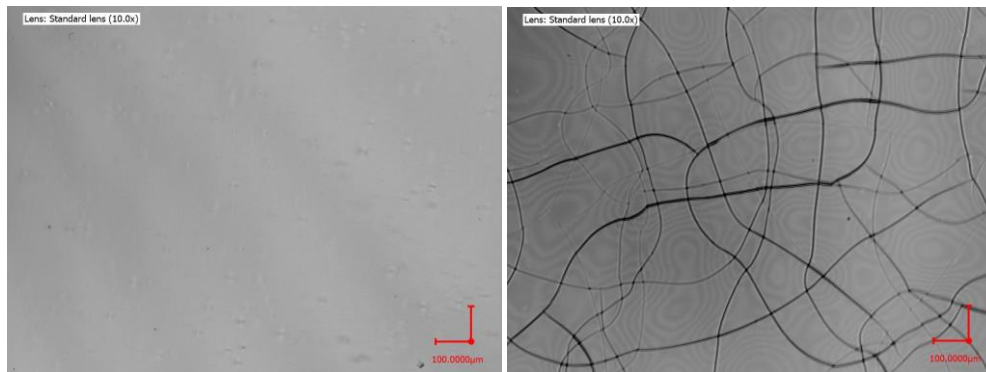


Figure 74 Laser view of PDMS treated with (left) 100W plasma and (right) 600W plasma for 1 minute.

## 8. Deposition of Metal Contacts and Sacrificial metal

After the graphene patterning, metal contacts need to be deposited on the graphene layer. These metal contacts are required to interface electrical signals to the graphene layer. Wires need to be attached to the electrode array to carry these signals. When choosing the type of metal to serve as the metal contact, good contact with the graphene layer and the ease of wire bonding on the metal are two major concerns.

Aluminum is a common metal to wire bond on, but it provided a bad contact resistance to the graphene in the previous studies[71]. Titanium is one metal that has low contact resistance with graphene but is difficult to wire bond on. One possible candidate as the contact is to combine aluminum and titanium as a stack. The titanium can provide a good contact resistance with the graphene layer while the aluminum deposited on top can be used as landing material for the wire bonding. Both material was deposited by using sputtering with low power recipes (1kW) to avoid damaging the graphene and the PDMS.

Another metal layer needs to be deposited to act as a sacrificial layer. The sacrificial layer will be used as landing material for PDMS etching and protect the graphene layer underneath. The layer is deposited after the deposition of metal contacts. The sacrificial metal will be removed after the PDMS etching by using a chemical solution. It is important that the sacrificial metal and the contact metal can be etched selectively.

### 8.1. Flowchart of the metal contact and sacrificial metal deposition

A process flow was devised to fabricate the metal contacts and sacrificial metal. Since titanium and aluminum are selective to each other during wet etching process, titanium/aluminum stack is chosen as the contact metal and titanium is selected as the sacrificial metal.

The process is continuing on the graphene patterning process. A titanium layer with 100 nm thickness is deposited on the wafer followed by 200 nm aluminum deposition. A layer of photoresist is spin-coated and patterned to create the metal contacts. The aluminum layer is then patterned by using PES. The patterning of the aluminum layer with RIE was attempted but the same combination of gas to etch the aluminum is also used in the titanium etching recipe. The titanium layer underneath was also etched when patterning the aluminum layer. After the patterning of the aluminum layer in PES (Figure 76), the photoresist is stripped away by using acetone and isopropanol.

Another layer of titanium is sputtered on top as the sacrificial metal. To pattern the sacrificial metal, a layer of photoresist is applied. The titanium layer is etched with 0.55% HF for 100 seconds. The process is finished with photoresist stripping.

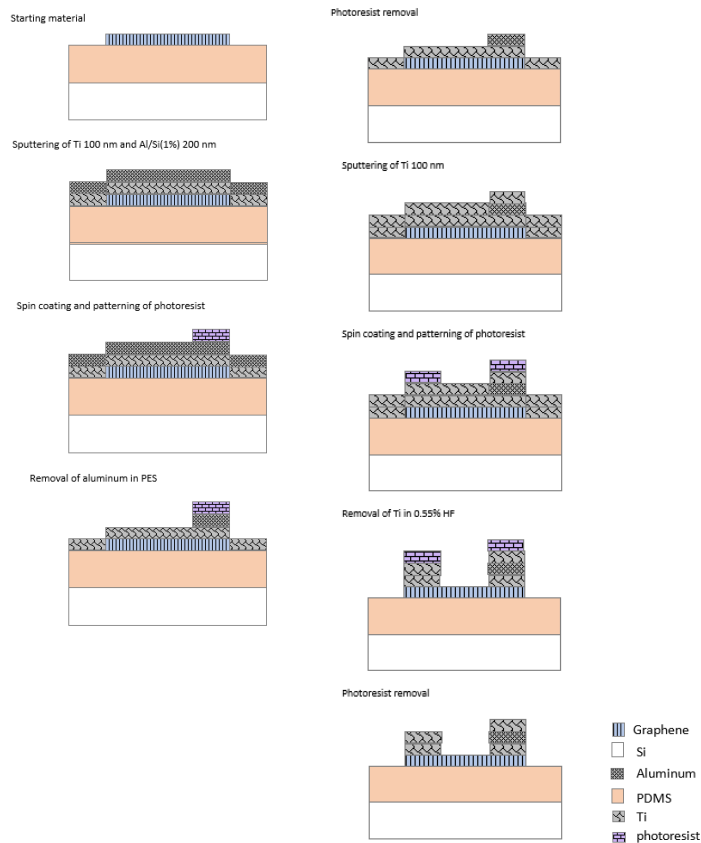


Figure 75 Simplified flowchart of the metal contact and sacrificial layer deposition.

By using profilometer, the thickness of the fabricated metal stack can be measured compared to the substrate. A wafer with silicon dioxide was used to test the recipe. According to the deposition recipe, the thickness of the titanium layer is 100 nm and the aluminum is 200 nm. From the profilometer, the thickness of a metal stack with Ti/Al/Ti composition was measured to be 256 nm and the contact metal stack with Ti/Al was measured to be 180 nm thick (Figure 78). Subtracting both values yielded the thickness of the sacrificial metal which was 76 nm. The aluminum layer on top was stripped away, the thickness of the titanium contact layer was known to be 78 nm. From this information, it can be concluded that the thickness of the aluminum layer was 102 nm. Although all of the metal layers were thinner than expected, the desired structure for the metal stack was able to be fabricated (Figure 77).



Figure 76 Aluminum on titanium layer

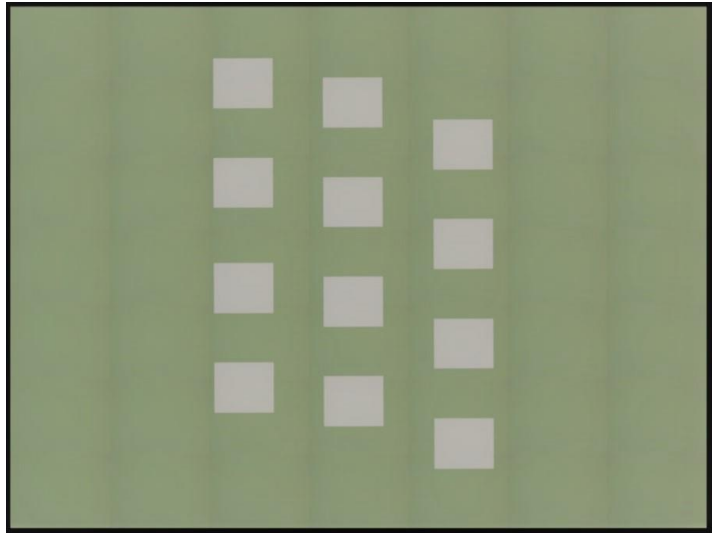


Figure 77 Ti/Al/Ti on silicon dioxide

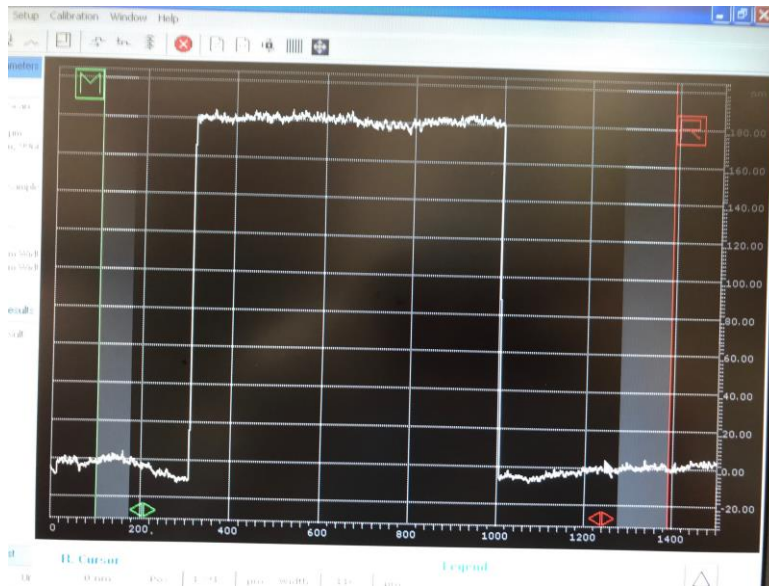


Figure 78 The profilometer measurement of the Ti/Al stack.

# 9. PDMS Etching for Contact Opening

## 9.1. PDMS and aluminum hard mask deposition

After the metal contacts and sacrificial metal were deposited, a layer of PDMS is applied on the wafer. The PDMS was spin-coated with the thickness of 50  $\mu\text{m}$ . The curing process was done at 90°C for 1 hour. The access to the graphene layer and metal contact is made by etching the PDMS with reactive ion etching. With approximately 50  $\mu\text{m}$  holes need to be made through the PDMS, this process requires long exposure to plasma which photoresist will not be able to survive. The metal hard mask once again was used to perform this process. A 400 nm thick aluminum with 1 % silicon was used as the masking material.

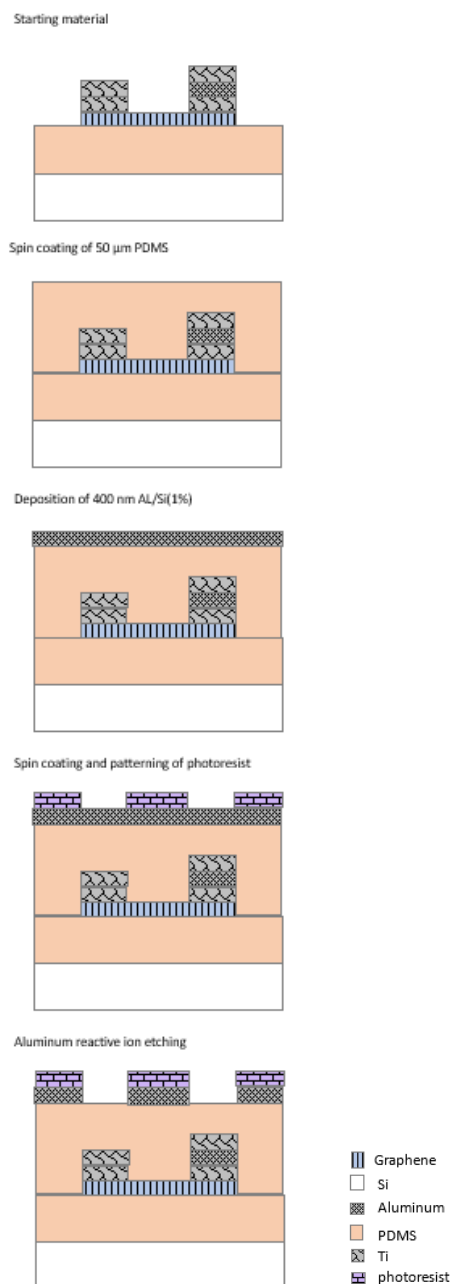


Figure 79 Simplified flowchart of hard mask patterning.

The mask was patterned using SPR-3012 photoresist. The wafer was exposed to hexamethyldisilazane (HMDS) vapor for 10 minutes before the coating process to increase the adhesion of photoresist to the aluminum. After the photoresist had been patterned, the aluminum mask was etched by using reactive ion etching with HBr and Chlorine gas. The photoresist didn't need to be stripped after the aluminum etching. During the PDMS etching, exposure to plasma will remove the photoresist in the process.

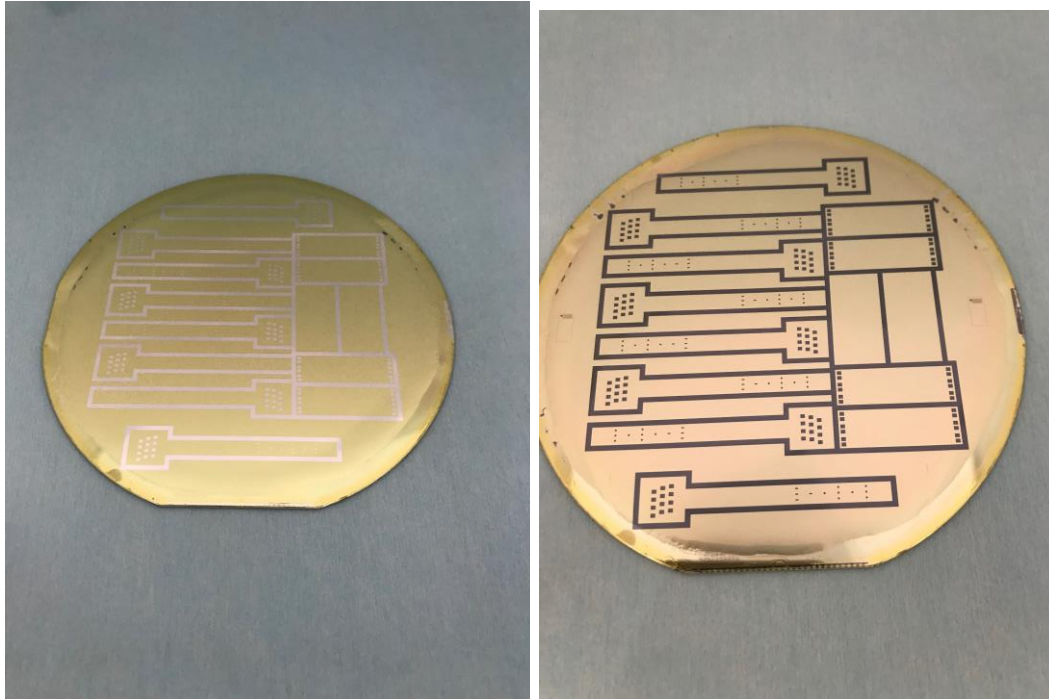


Figure 80 (left) The aluminum layer coated with photoresist before the mask patterning. (right) The hard mask for PDMS patterning

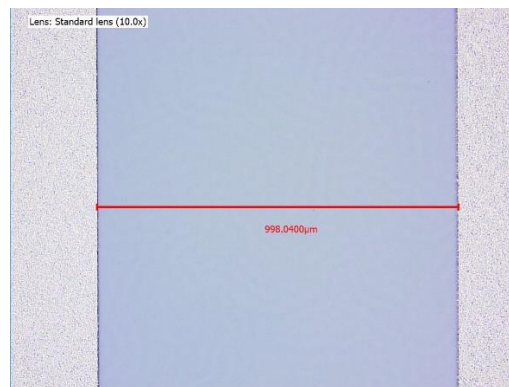


Figure 81 The aluminum hard mask under the microscope.

## 9.2. PDMS etching

The PDMS layer was then etched using reactive ion etching. The combination of SF<sub>6</sub>, CF<sub>4</sub> and O<sub>2</sub> gas was used in the chamber. The PDMS layer was etched until the layer underneath (landing material) is reach. The etch rate of the PDMS layer, varies depending on the condition of the machine. A test was performed to measure the etch rate of the PDMS (Figure 82). The test wafer was a silicon wafer coated by 50 µm of PDMS. The thickness of the aluminum hard mask was 400 nm. A record of the latest etching progress can be seen in Table 8. Measurement of the depth was done using the



profilometer. The depth of the hole was measured from the top of the mask to the bottom of the hole. Under the microscope, silicon layer was already seen (Figure 83).

The record on Table 8 was obtained when testing the etch rate of the PDMS. The etch rate calculation was done assuming that the thickness of the aluminum mask remain constant. The wafer contained PDMS layer on silicon substrate. Since the thickness of the PDMS was around 50  $\mu\text{m}$ , between minute 70 to 86 of the etching process, silicon was etched instead of PDMS. The etch rate measured from start to 35 minutes can be slightly off due to photoresist layer was still on the mask. The most accurate information regarding the etch rate of PDMS can be seen between minute 35 to 75.

Table 8 The latest PDMS etching log

Cumulative time	Depth of opening	Remark
Start	3.945 $\mu\text{m}$	The photoresist was still on top of the mask, with a thickness of 1.9 $\mu\text{m}$
35 minutes	25.61 $\mu\text{m}$	Etch rate: 0.619 $\mu\text{m}/\text{min}$
70 minutes	49.86 $\mu\text{m}$	Etch rate: 0.6928 $\mu\text{m}/\text{min}$
86 minutes	71.587 $\mu\text{m}$	Etch rate: 1.35 $\mu\text{m}/\text{min}$



Figure 82 The test wafer after the PDMS etching process

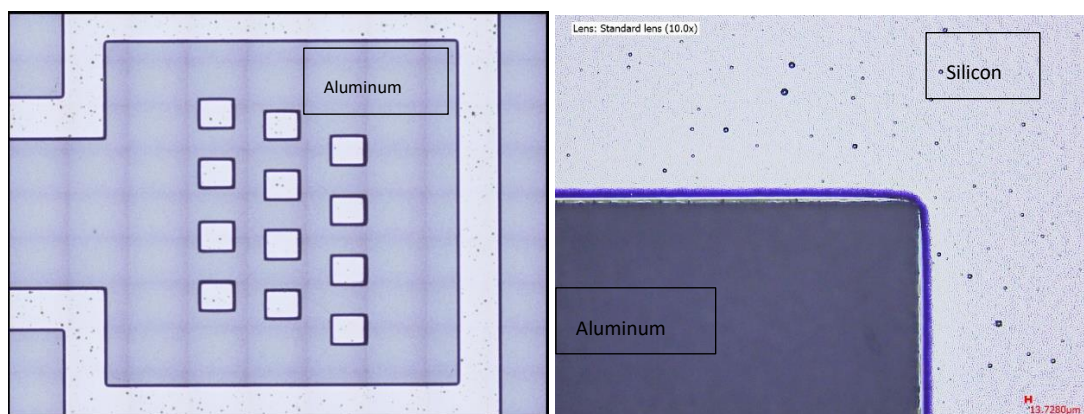
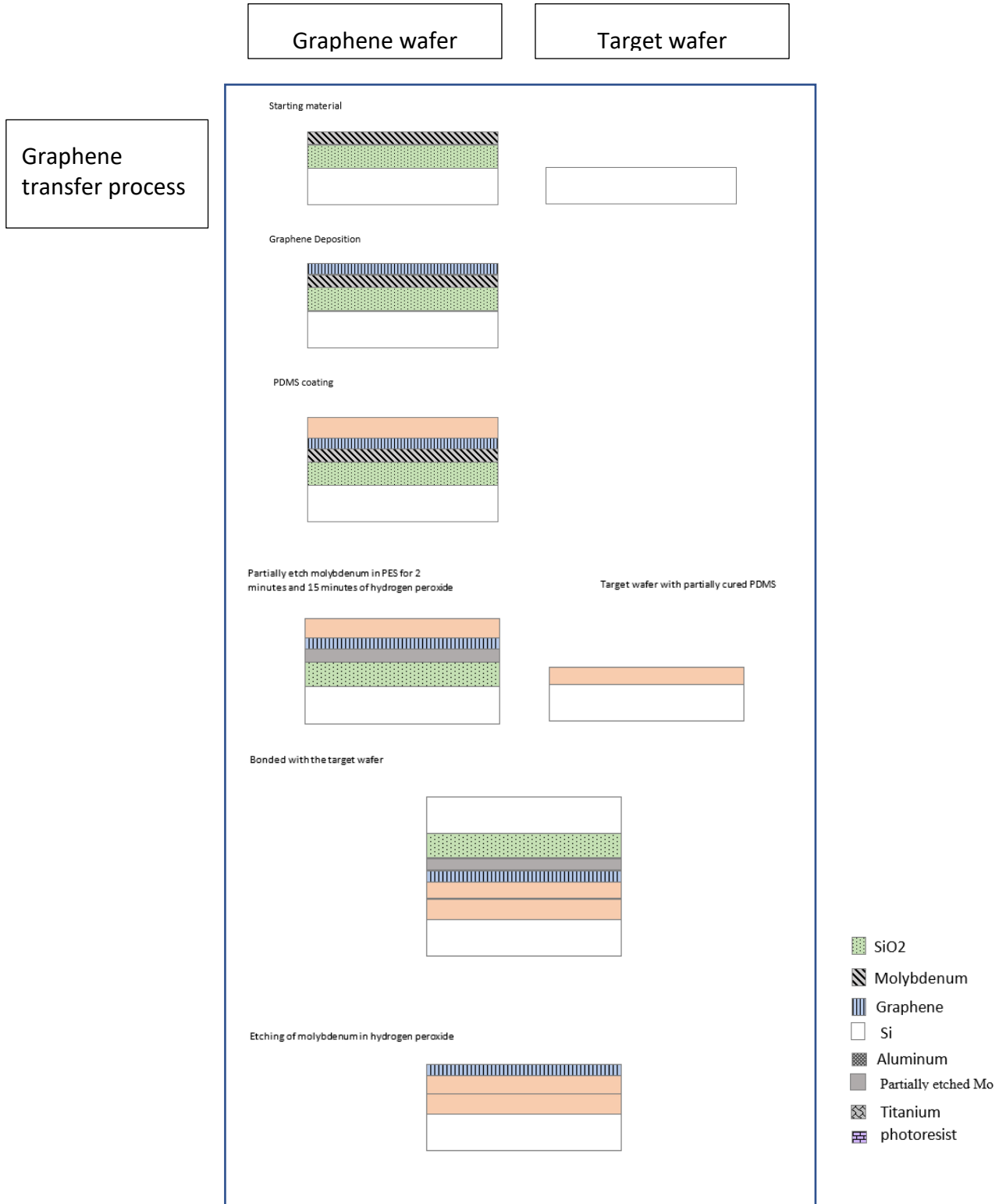


Figure 83 The result of PDMS etching under the microscope

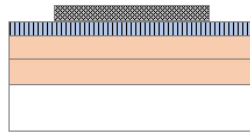
# 10. Final flowchart of the Entire process

The following is final flowchart of the fabrication for the graphene electrode array. These are cartoon images; thus, proportion of the layers is not on the right scale.

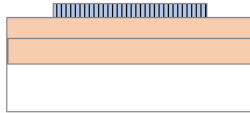


Graphene  
patterning

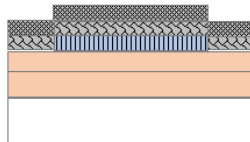
Aluminum hard mask deposition 200 nm



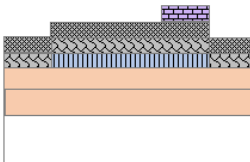
Graphene etching in oxygen plasma



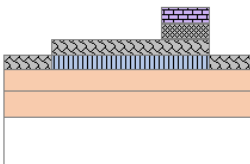
Sputtering of Ti 100 nm and Al/Si(1%) 200 nm



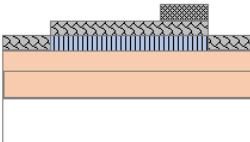
Spin coating and patterning of photoresist



Removal of aluminum in PES



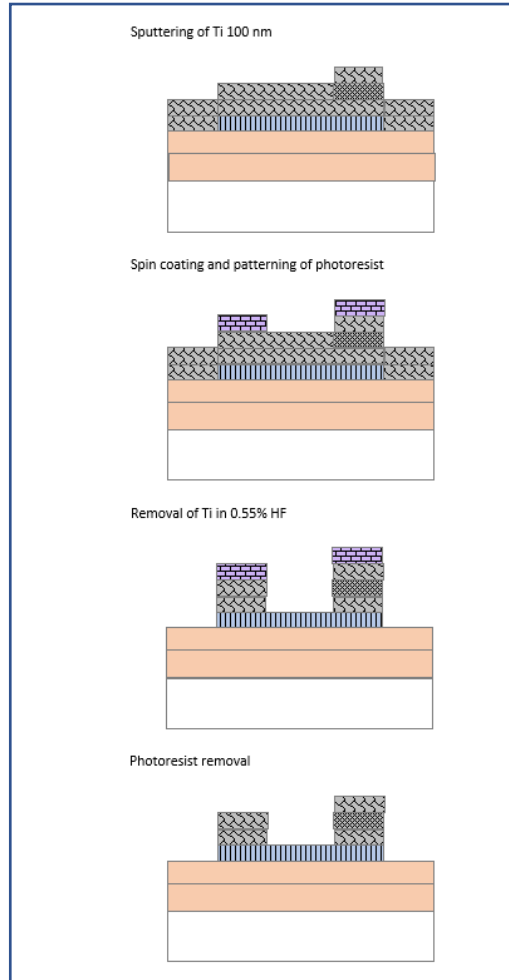
Photoresist removal



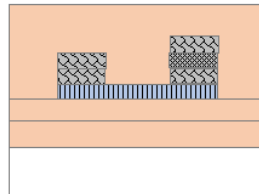
Contact metal  
patterning

-  SiO2
-  Molybdenum
-  Graphene
-  Si
-  Aluminum
-  Partially etched Mo
-  Titanium
-  photoresist

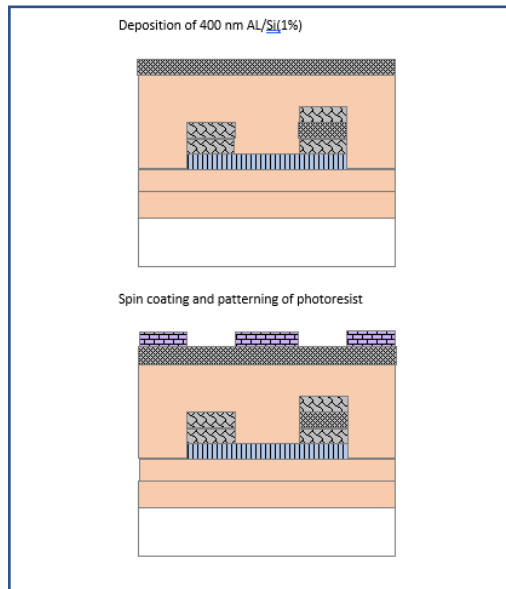
Sacrificial metal patterning



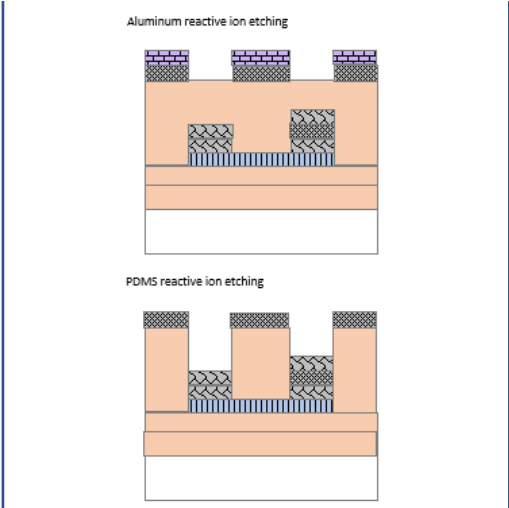
Spin coating of 50 μm PDMS



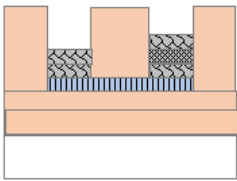
PDMS patterning



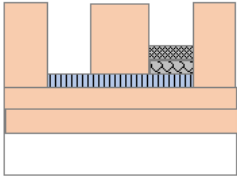
- SiO<sub>2</sub>
- Molybdenum
- Graphene
- Si
- Aluminum
- Partially etched Mo
- Titanium
- photoresist



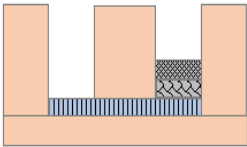
Aluminum wet etching in PES











Titanium wet etching in 0.55% HF



Dicing and device release



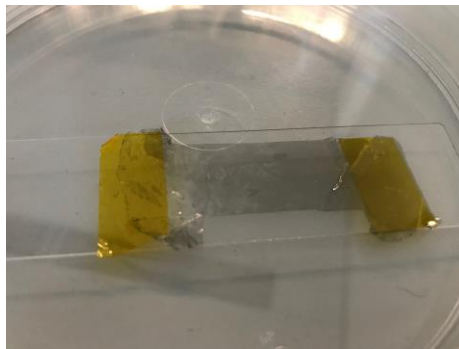
-  SiO<sub>2</sub>
-  Molybdenum
-  Graphene
-  Si
-  Aluminum
-  Partially etched Mo
-  Titanium
-  photoresist

## 11. Measurements

Measurement on the device was not able to be performed due to unforeseen reasons. Although each step in the fabrication process has been tested, the final run of the fabrication process was not able to be performed due to the unavailability of the clean room and the metal deposition machine in the last phase of the thesis project.

### 11.1. Optical transmittance measurement.

The optical transparency was one important parameter for the graphene electrode array. A piece of graphene on PDMS was placed on glass (Figure 84). The Lambda ARTA was used to measure the optical transmittance of the sample. Two types of optical transmittance were measured. The internal transmittance which measures the percentage of flux passing through the sample with only taking into account the loss due to absorption of energy by the sample. The total transmittance which taking into account the energy loss due to various scattering.



*Figure 84 Test sample for optical transmittance measurement.*

From the measurement results, energy loss because of the PDMS was minimum compared to the loss caused by the graphene layer. The 50  $\mu\text{m}$  PDMS layer had more than 99% internal transmittance and 97% of total transmittance. While the test sample had about 72% to 77% internal transmittance (Figure 85). By eliminating the contribution of the PDMS layer, the internal energy loss from the graphene layer was at worst 26%. With the absorption rate of a single layer of graphene is about 2.3%[33], the number of layers in our multilayer graphene was about 11 layers. A similar result was measured on the total transmittance measurement (Figure 86). The similar transmittance value indicates that most of the energy loss in graphene was caused by absorption rather than scattering.

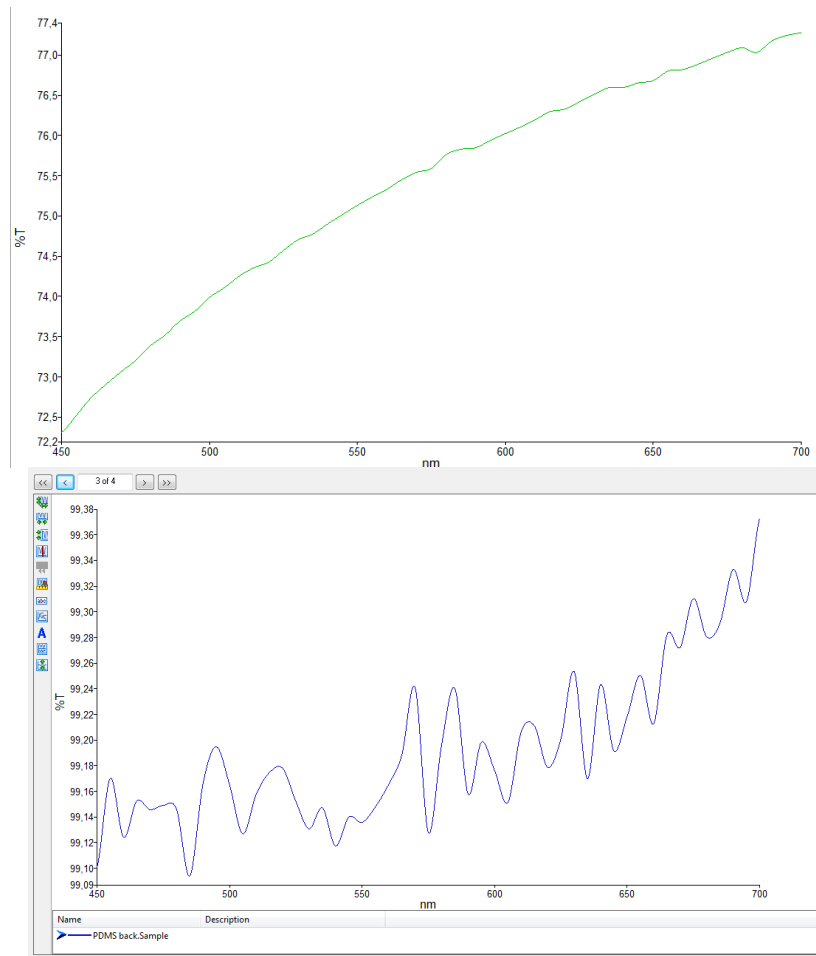


Figure 85 The internal transmittance measurement. (top) Measurement of the test sample with graphene and PDMS. (bottom) the internal transmittance of PDMS.

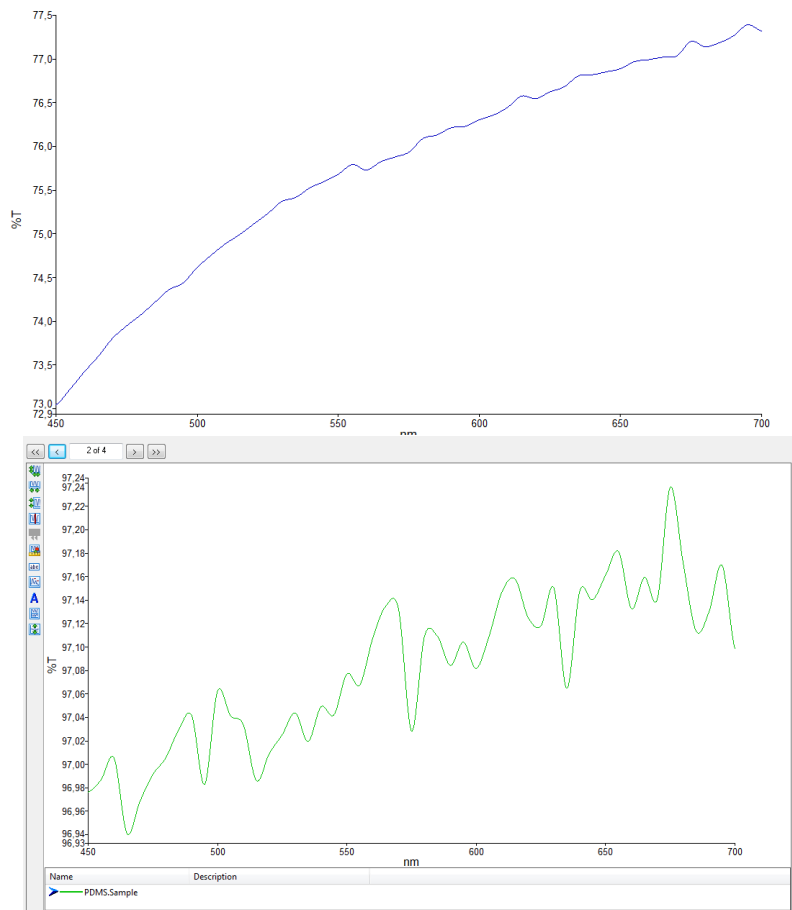


Figure 86 The total transmittance measurement. (top) measurement of the test sample with graphene and PDMS. (bottom) the total transmittance of PDMS.



## 12. Conclusion

This thesis explained the design, implementation, and fabrication process of a graphene electrode array as a foundation for future work. A simple goal of having a graphene layer encapsulated by PDMS turned out to be challenging of every step. Mask design for electrode array was presented along with test structures to characterize electrical and optical properties of the fabrication process. The transfer process of graphene layer to a PDMS substrate was explored from the use of different methods, different ways to increase the etch rate of molybdenum were explored. The use of wafer cleaving and photoresist ring to create entry points for etchant showed a promising result but those options had some drawbacks. The wafer cleaving process was hard to performed on wafer with high thermal stress and it also produced some dust during the cleaving process. The use of photoresist ring to create entry points for etchant was quite effective. The use of makeshift mask to create this structure is one of the advantages of this process. But it still suffers with bad adhesion of graphene and PDMS to the photoresist at the target wafer. The use of photoresist ring may be worth to be investigated alongside partially cured PDMS at the target wafer. Out of some known etchants for molybdenum, hydrogen peroxide was the only etchant that was able to etch molybdenum layer underneath a PDMS layer.

Novel approach on graphene transfer process was presented as the final transfer process. In the proposed method, graphene layer was able to be transferred to a PDMS substrate by performing a 2-step etching process. The molybdenum was thinned before the bonding process. The thinning process was performed by using hydrogen peroxide etchant after the PDMS coating. To avoid the PDMS to delaminate from the wafer and float to the liquid's surface, etching process with PES was performed to remove the molybdenum layer surrounding the PDMS. The spin-dryer was used to dry the wafer after etching process with PES. The use of spin-dryer is important to form a sealing bond at the edge of the PDMS to silicon dioxide. The sealing process limits the flow etchant so that it can only reach the molybdenum from limited entry points. The effect of the PDMS sealing was seen during the molybdenum thinning process. The molybdenum got etched from the middle instead of the edge. After precisely 15 minutes of exposure to hydrogen peroxide, the molybdenum layer should have been thinned and the PDMS layer will still adhere to the wafer. Visually, a wafer is ready to go on to the next process when the molybdenum layer become slightly red. The process is continued to the bonding process to the target wafer. The target wafer contained partially cured PDMS which have a good adhesion to other PDMS.

After the wafers were bonded, the second phase of the molybdenum etching was performed. This etching process must be done while the wafer stack is in vertical position to avoid the top wafer closing the interface between the wafer due to gravity. The etching process for the second step can vary from 30 minute until 4 four hours. A prolonged exposure to the hydrogen peroxide can cause damage to the PDMS layer with bubble formations were seen after hours of etching process. The graphene and PDMS layer should be transferred to the target wafer.

The graphene etching was performed on both the reactive ion etcher and also barrel plasma chamber. The etching process of graphene is now known to be temperature activated. Exposing the same wafer 2 times consecutively will provide a different result than exposing it two times with time interval.

A satisfying pattern with the capability of patterning a 10  $\mu\text{m}$  wide diameter while still maintaining the graphene electrical resistance. Although pattern can be distinguished between area exposed to plasma and not, the exposed graphene left behind a residual layer of non-conductive material on the

wafer. The Raman spectroscopy measurement was performed on the exposed graphene layer. The results of the measurements were compared between before and after the plasma exposure.

While the final run on the thesis stopped until the graphene etching, the process of patterning the metal layer for both the sacrificial and contact metal have been tested. For contact metal, a combination of titanium and aluminum layer was chosen. The titanium layer provided a good contact resistance to graphene and the aluminum was there for the wiring bonding process. As for the sacrificial metal, a titanium layer was chosen. The titanium is chosen due to its selectivity to aluminum etchant and aluminum etchant is resistant towards titanium etchant. The reactive ion etching process was not able to pattern the desired pattern since the two chosen metal, titanium and aluminum shared the exact same recipe for RIE. The metal patterning process was done using wet etching. The PES solution was used to etch the aluminum layer and the 0.55% HF was used to etch the titanium layer.

The metal deposition process on graphene and PDMS has been done previously during graphene etching process as hard mask. Although graphene bonding to metal was not good and prone to delamination caused by undercuts, the test performed on silicon dioxide should be able to be adapted for deposition and patterning on graphene and PDMS.

The last step of the fabrication process is to create openings on the PDMS layer. This process has been done multiple times. Because it is performed on a thick 50  $\mu\text{m}$  PDMS substrate, the contribution of the layer on the surface of the wafer will cause minimum impact to the PDMS patterning process.

With the unavailability of clean room facility and equipment at the last phase of the final run of the fabrication process, the measurement using designed test structures was not able to be performed. The optical transmittance measurement was able to be performed. From the transmittance measurement, the graphene and PDMS layer had a similar total transmittance and internal transmittance of about 77% transmittance across the visible light spectrum. The similar value between internal and total transmittance, means that most of the light energy through the graphene/PDMS layer was absorbed by the graphene instead of scattered. From the calculation of the measured graphene optical transmittance was about 74% which means graphene absorbed 26% of light. If each layer of graphene absorbs about 2.3%. Our multilayered graphene has approximately 11 layers of graphene.

## 13. Future Recommendations

The result of the current project was seen as a first step into graphene electrode array. Further optimization on each process is still necessary. Therefore, the following section presents the recommendation for future work.

- The use of etchant lines can be incorporated to the back of the graphene wafer. The etchant lines are holes that can delivery etchant directly to the molybdenum layer, it may help to speed up the etching process of molybdenum. Reducing the etching time of molybdenum will significantly reduce the chance of defect formation in the PDMS layer.
- The options for increasing the adhesion of PDMS to PDMS bonding still need to be explored. The imperfect adhesion between PDMS caused formation of defects during the transfer process. In addition to the partial curing scheme, the use of uncured PDMS as adhesive may be a promising option to create conformal contact between 2 layers of PDMS.
- The graphene etching process is still imperfect. The use of lower plasma power is necessary to avoid damaging the PDMS layer. The use of other metal with better adhesion to graphene can also improve the resulting pattern. A thicker metal can also be a good candidate to reduce crack formation on the mask.
- Exploring the use of biocompatible PDMS. During the early stage of the project, biocompatible PDMS (Nusil MED-1000 and MED-6015) was purchased with the hope of replacing the PDMS that was currently used (sylgard 184). Aside from biocompatibility, MED-6015 was designed to be optically transparent thus could improve the optical transmittance of the device. During this project, the use of MED-6015 was tested once. But because of the difference in mechanical and chemical properties, not every process using sylgard 184 can be translated perfectly into the use of MED-6015.
- Optimizing the PDMS reactive ion etching recipe. The current recipe provides a slow etch for PDMS. It can take approximately 2 hours for etching the 50  $\mu\text{m}$  PDMS. With the etcher only available on limited amount of time every week for etching polymers, a faster etch rate can provide more opportunity for processing.
- Having a proper setup for graphene transfer to PDMS. So far, the molybdenum etching in hydrogen peroxide is performed with equipment supplied by the clean room. This setup is far from optimal for etching bonded wafer. In bonded wafer case, the weight of the other wafer can hinder the movement of etchant especially with soft material like PDMS is place between the bonded wafer. This effect was prominent when molybdenum etching was done horizontally. Having a setup that can suspend both wafer when submerged can help to produce a more consistent result by eliminating uncontrolled factor like wafer weight or placement.
- Exploring other option for graphene metal catalyst. During this project, only molybdenum catalyst was used. The use of other catalyst can maybe provide other option for transferring the graphene layer.

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## 15. Appendix





# Transfer-free graphene process on molybdenum catalyst for flexible electrodes

## Flow chart

**Version**  
**20 November 2018**

ME2214

Process engineer: Gandhi

Start: 2018

Contamination: Yes – CU, Ni, Pt

Mentor : Sten

**Labs:** CR100, CR10000, SAL

EKL(Else Kooi Laboratory)	
DELFT UNIVERSITY OF TECHNOLOGY	
Address :	Feldmannweg 17, 2628 CT Delft, The Netherlands
P.O. Box	5053, 2600 GB Delft, The Netherlands
Phone :	+31 - (0)15 - 2783868
Fax :	+31 - (0)15 - 2622163
Website :	<a href="http://ekl.tudelft.nl/EKL/Home.php">http://ekl.tudelft.nl/EKL/Home.php</a>

Detailed information about possible contamination:

Place/Clean Rooms used in process:

- Write the sequence of used labs from start to finish.
- Which (Non-standard) materials or process steps
- What kind of process or machine was used?
- The other materials that wafers contain that are also processed on this machine

Lab/Clean room	(Non-standard) material/ process steps	Process/Machine/	Other materials used in machine
CR100	non	non	non
CR10000	Yes, graphene	BlackMagic	Cu, Pt, Ni
SAL		Mo wet etching	

If other labs are used:

Write the steps number: Possible contamination issues/materials.

None

If there are non-standard processing steps in a standard process: Write down the steps number, the material and machine that is used.

Step number	Material	Machine/Tool

# STARTING MATERIAL

Use 10 **single side polished process wafers**, with the following specifications:

Type:	p-type
Orientation:	1-0-0, 0 deg off orientation
Resistivity:	2-5 $\Omega\text{cm}$
Thickness:	$525 \pm 15 \mu\text{m}$
Diameter:	$100.0 \pm 0.2 \text{ mm}$

Wafers taken out of an already opened box must be cleaned before processing, according to the standard procedure.  
Wafers taken out of an unopened wafer box do not have to be cleaned before processing.

## 1. Wafer 1

### 1. CLEANING PROCEDURE: HNO<sub>3</sub> 100% and 65%

Cleaning 10 minutes in fuming nitric acid (Merck: HNO<sub>3</sub> 100%) at ambient temperature.  
Use wet bench "HNO<sub>3</sub> (100%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinsers with the standard program until the resistivity is 5 MΩ.

Cleaning 10 minutes in concentrated nitric acid (Merck: HNO<sub>3</sub> 65%) at 110 °C.  
Use wet bench "HNO<sub>3</sub> (65%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinsers with the standard program until the resistivity is 5 MΩ.

Drying Use the Semitool "rinsers/dryer" with the standard program, and the white carrier with a red dot.

## 2. OXIDATION

Furnace no: C1 or D1

Target thickness: 600 nm

Program name: WETOXID 54 min at 1100 °C (check!)

PROCESS	TEMPERATURE (in oC)	GASSES & FLOWS (in liter/min)	TIME (in minutes)	REMARKS
boat in	800	nitrogen: 3.0 oxygen: 0.3	5	
stabilize	800	nitrogen: 3.0 oxygen: 0.3	10	
heat up	+10 oC/min	nitrogen: 3.0 oxygen: 0.3	30	
stabilize	1100	nitrogen: 3.0 oxygen: 0.3	10	
oxidation	1100	nitrogen: 2.25 oxygen: 3.85	68	
cool down	-5 oC/min	nitrogen: 3.0	100	wait for operator
boat out	600	nitrogen: 3.0	5	

NOTE: The total process time can be slightly reduced in the "cool down" step: the "boat out" step can be started after ± 60 minutes, when the actual temperature of the furnace will be about 800 oC.

### 3. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:  
Program: Th. SiO<sub>2</sub> on Si, >50nm auto5pts

Oxide thickness: 600 nm

### 4. Catalyst deposition @ Class 100

Use the TRIKON SIGMA sputter coater for the deposition of the catalyst metal Mo layer on the process wafers.  
Follow the operating instructions from the manual when using this machine.

Mo: 50 nm, recipe Mo\_50nm\_50C\_slow

Visual inspection: the metal layer must look shiny.

### 5. Graphene growth @ Class 10000

Use the AIXTRON BlackMagic Pro to grow CNTs using LPCVD at 915°C. Use recipe: Mo\_NEW\_915C\_20min

Use graphene reactor interior (Cu contaminated)!

**USE WHITE BLISTER WITH Cu WRITTEN ON IT**

#### 6. PDMS MIXING @ POLYMER LAB

Mix Sylgard 184 elastomer and solvating agent with 10:1 ratio with 6 gram of elastomer per wafer. Mix and degas the solution in Thinky are-250 mixer

#### 7. COATING AND BAKING

Use Brewer Science Manual Spinner to spin coat the PDMS solution on wafer 1.

Program name: x\_PDMS\_50um

Step	Speed (rpm)	Acceleration (rpm/s)	Time (s)
1	500	300	10
2	1250	300	30

Bake the wafer in the Memmert oven for 60 minutes at 90°C. Leave the wafer in room temperature overnight to continue the curing process.

**USE DEDICATED BOX FOR POLYMER**

#### 8. Mo etching with PES 77-19-04 @ SAL

**Use contaminated glass ware.** Etch the Mo layer around the PDMS using PES 77-19-04. Etching takes 2 min. Rinse in DI water. Use single wafer dryer to dry the wafer.

Use the **Cu** holder when drying the wafer in the single wafer dryer.

#### 9. Mo etching with H<sub>2</sub>O<sub>2</sub> @ SAL

**Use contaminated glass ware.** Etch most of the Mo layer underneath the PDMS using H<sub>2</sub>O<sub>2</sub> (31%). This step is done to reduce the amount of Molybdenum while still keeping the Molybdenum layer as release mechanism in later step. **Etching takes exactly 15 min.** Rinse in DI water. **Do not use wafer dryer to dry the wafer. Dry the wafer by evaporation overnight.**

## 10. Wafer 2

#### 11. COATING AND BAKING

Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95degC for 90 seconds. Always check the temperature of the hotplate and the relative humidity ( $48 \pm 2\%$ ) in the room first.

Use coating **Co – Zero Layer** (resist thickness: 1.400  $\mu$ m).

#### 12. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

Follow the operating instructions from the manual when using this machine.

Use **COMURK mask**, the correct litho job:

Die-size 10x10 mm

Job: litho/Zefwam

And the correct exposure energy (120 mJ/cm<sup>2</sup>).

#### 13. DEVELOPMENT

Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment.

The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 degC for 90 seconds. Always check the temperature of the hotplates first.

Use development **program Dev - SP**

#### 14. INSPECTION: LINEWIDTH

Visually inspect the wafers through a microscope and check the line width. No resist residues are allowed.

#### 15. MARK WAFERS

Use the glass scribe to write the run ID and wafer number in the wafer flat.

#### 16. PLASMA ETCHING OF ALIGNMENT MARKS

Use the Trikon Omega 201 plasma etcher.  
Follow the operating instructions from the manual when using this machine.  
The process conditions of the etch program may not be changed!

Use sequence **URK\_NPD** and set the platen temperature to **20 °C** to etch 1200 Å deep ASM URK's into the silicon.

#### 17. CLEANING PROCEDURE: TEPLA + HNO<sub>3</sub> 100% and 65%

Plasma strip Use the Tepla plasma system to remove the photoresist in an oxygen plasma.  
Follow the instructions specified for the Tepla stripper and use the quartz carrier.  
Use program 1

Cleaning 10 minutes in fuming nitric acid (Merck: HNO<sub>3</sub> 100%) at ambient temperature.  
Use wet bench "HNO<sub>3</sub> (100%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning 10 minutes in concentrated nitric acid (Merck: HNO<sub>3</sub> 65%) at 110 °C.  
Use wet bench "HNO<sub>3</sub> (65%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the Semitool "rinsers/dryer" with the standard program, and the white carrier with a red dot.

#### 18. COATING AND BAKING

Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95°C for 90 seconds. Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co – 3012-2.1um** (resist thickness: 2.1 μm).

#### 19. PDMS MIXING @ POLYMER LAB

Mix Sylgard 184 elastomer and solving agent with 10:1 ratio with 6 gram of elastomer per wafer. Mix and degas the solution in Thinky are-250 mixer

#### 20. COATING AND BAKING @ POLYMER LAB

Use Brewer Science Manual Spinner to spin coat the PDMS solution on wafer 2.

Program name: x\_PDMS\_50um

Step	Speed (rpm)	Acceleration (rpm/s)	Time (s)
1	500	300	10
2	1250	300	30

Bake the wafer in the Memmert oven for 30 minutes at 60°C.

#### 21. Wafer Bonding

This process should be done within 1 hour after the wafer is taken out from the oven.

Use AML wafer bonder to bond wafer 1 and wafer 2. Place wafer 1 at the bottom plate and wafer 2 at the top plate. Set the upper and lower platen to 20°C. Use a controlled force setting with 100 N set point. Do the bonding process for 60 minutes.

## **22. Wafer stack (wafer 1+ wafer 2)**

### **23. MOLYBDENUM ETCHING @ SAL**

Use contaminated glass ware. Always use a tall glassware with vertical carrier for single wafer. Etch the Mo layer completely away underneath the graphene to transfer the graphene and PDMS to wafer 2 using H<sub>2</sub>O<sub>2</sub> (31%). The etching usually takes 30 min to 1 hour. The wafer stack needs to be rotated every 20 minutes to ensure etchant reach all of the molybdenum. Rinse in DI water.

**Do not use the wafer dryer. Dry the wafer by evaporation overnight.**

## **24. Wafer 2**

### **25. COATING AND BAKING**

Use the brewer manual spinner to coat the wafer with Shipley SPR3012 positive photoresist. Soft bake at 95 degC for 5 min in memmert oven.

Resist thickness: 2.100 µm

Use contaminated wafer chuck for spin coating.

### **26. ALIGNMENT AND EXPOSURE**

Use the EVG 420 Contact aligner to expose the photoresist. Use mask for device ME2214, layer GRAPHENE. Calculate the exposure time by consulting the contact aligner exposure energy data log.

### **27. DEVELOPMENT**

Develop the photoresist using MF322 developer. Development time 90 sec.

### **28. PLASMA ETCHING OF GRAPHENE @ POLYMER LAB**

Use TEPLA in SAL lab to etch the graphene layer using plasma. Graphene is etched in oxygen plasma for 4 min with 600W power.

Use **recipe 2**

### **29. PHOTORESIST STRIPPING @ POLYMER LAB**

Photoresist is removed using acetone. Do a visual check to see if the photoresist is still remained.

### **30. METAL CONTACT DEPOSITION**

Use the TRIKON SIGMA sputter coater for the deposition of the metal contact. Metal contact consists of titanium buried under aluminium. Perform the LUR test before the deposition according to the manual. Follow the operating instructions from the manual when using this machine.

Ti: 100 nm, Al : 200nm, recipe Ti100nm\_al200nm\_25C

Visual inspection: the metal layer must look shiny.

### **31. COATING AND BAKING**

Use the brewer manual spinner to coat the wafer with Shipley SPR3012 positive photoresist. Soft bake at 95 degC for 5 min in memmert oven.

Resist thickness: 2.100 µm

Use contaminated wafer chuck for spin coating.

### **32. ALIGNMENT AND EXPOSURE**

Use the EVG 420 Contact aligner to expose the photoresist. Use mask for device ME2214, layer CONTMET. Calculate the exposure time by consulting the contact aligner exposure energy data log.

### **33. DEVELOPMENT**

Develop the photoresist using MF322 developer. Development time 90 sec.

### **34. ALUMINUM ETCHING @ SAL**

Use PES 77-19-04 to etch the aluminum layer.  
Etch time approximately 4-5 minutes

### **35. PHOTORESIST STRIPPING**

Photoresist stripping using acetone for 2 minutes and IPA for 2 minutes. Rinse in DI water afterwards. Check for residual photoresist.

### **36. SACRIFICIAL TITANIUM DEPOSITION**

Use the TRIKON SIGMA sputter coater for the deposition of the titanium sacrificial layer on the process wafers. Perform the LUR test before the deposition according to the manual. Follow the operating instructions from the manual when using this machine.

Ti: 100 nm, recipe Ti\_100nm\_25C

Visual inspection: the metal layer must look shiny.

### **37. COATING AND BAKING**

Use the brewer manual spinner to coat the wafer with Shipley SPR3012 positive photoresist. Soft bake at 95 degC for 5 min in memmert oven.

Resist thickness: 2.100 µm

Use contaminated wafer chuck for spin coating.

### **38. ALIGNMENT AND EXPOSURE**

Use the EVG 420 Contact aligner to expose the photoresist. Use mask for device ME2214, layer SACRMET. Calculate the exposure time by consulting the contact aligner exposure energy data log.

### **39. DEVELOPMENT**

Develop the photoresist using MF322 developer. Development time 60 sec.

### **40. WET ETCHING OF TITANIUM**

Use 0.55% HF to pattern the titanium layer. PDMS substrate will be visible. Etch time approximately 30 seconds.

### **41. PHOTORESIST STRIPPING @ POLYMER LAB**

Photoresist is removed using acetone. Do a visual check to see if the photoresist is still remained.

### **42. PDMS MIXING @ POLYMER LAB**

Mix Sylgard 184 elastomer and solving agent with 10:1 ratio with 6 gram of elastomer per wafer. Mix and degas the solution in Thinky are-250 mixer

### **43. COATING AND BAKING OF PDMS @ POLYMER LAB**

Use Brewer Science Manual Spinner to spin coat the PDMS solution on wafer 1.

Program name: x\_PDMS\_50um



Step	Speed (rpm)	Acceleration (rpm/s)	Time (s)
1	500	300	10
2	1250	300	30

Bake the wafer in the Memmert oven for 60 minutes at 90°C.

#### 44. ALUMINIUM HARD MASK DEPOSITION

Use the TRIKON SIGMA sputter coater for the deposition of the aluminium hardmask for PDMS etching. Perform the LUR test before the deposition according to the manual. Follow the operating instructions from the manual when using this machine.

Al: 400 nm, recipe Al\_400nm\_stack\_25C or AlSi\_200nm\_25C (2 times)

Visual inspection: the metal layer must look shiny.

#### 45. COATING AND BAKING

Use the brewer manual spinner to coat the wafer with Shipley SPR3012 positive photoresist. Soft bake at 95 degC for 5 min in memmert oven.

Resist thickness: 2.100 µm

Use contaminated wafer chuck for spin coating.

#### 46. ALIGNMENT AND EXPOSURE

Use the EVG 420 Contact aligner to expose the photoresist. Use mask for device ME2214, layer PDMS-CO. Calculate the exposure time by consulting the contact aligner exposure energy data log.

#### 47. PLASMA ETCHING OF ALUMINIUM

Use the Trikon Omega 201 plasma etcher. Hard mask for PDMS etching is patterned. Follow the operating instructions from the manual when using this machine. The process conditions of the etch program may not be changed!

Use sequence **Al04\_350** and set the platen temperature to **25 °C**.

#### 48. PLASMA ETCHING OF PDMS

Use the Trikon Omega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. The process conditions of the etch program may not be changed!

Use sequence **PDMS\_4** and set the platen temperature to **25 °C**. etch until reaching the sacrificial metal layer. Typical etch time 50-60 mins. Etch rate is about 1 µm/minute

#### 49. WET ETCHING OF ALUMINIUM

Use PES 77-19-04 to remove the remaining hard mask.

#### 50. WET ETCHING OF TITANIUM

Use 0.55% HF to remove the titanium sacrificial layer. Etch time approximately 30 seconds.

#### 51. DICING @ MEMS lab

Use blades to dice the device. Cut the PDMS layer along the dicing line. Use scotch tape to delaminate the device from the wafer.