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DOI
10.1109/NANO61778.2024.10628789

Publication date
2024

Document Version
Final published version

Published in
2024 IEEE 24th International Conference on Nanotechnology, NANO 2024

2024 IEEE 24th International Conference on Nanotechnology (NANO)
July 8-11, 2024. Gijón, Spain

Spin Wave Majority Gates Cascading by Gilbert Damping Embracement (Can the Devil be turned into an Angel?)

Pantazis Anagnostou[1], Arne Van Zegbroeck[2], Said Hamdioui[3], Christop Adelmann[4], Florin Ciubotaru[5], and Sorin Cotofana[6]

***Abstract*— Recent theoretical and experimental spintronics developments clearly indicate that Spin Waves (SW) interference based Majority gates (MAJ3) open an alternative road towards ultra low-power circuit implementations potentially capable to outperform CMOS counterparts. However, hurdles still exist, e.g., gate cascading, as due to the very nature of SW interference MAJ3 gates are not input output coherent, i.e., produce output waves with different amplitudes corresponding to 'weak' and 'strong' majority, which precludes their direct cascading within the SW domain. State of the art designs address this issue by means of hybrid SW-CMOS systems that make use on domain converters, which are energy expensive and diminish if not nullify the ultra-low power promise of the SW-based computing paradigm. In this paper we propose a gate cascading technique that rely on the natural SW amplitude decay while propagating through a magnetic conduit. We demonstrate the concept by constructing the building block MAJ3(MAJ3(In_1, In_2, In_3), In_4, In_5) and verifying its correct behaviour by means of micromagnetic simulations. We evaluate the proposed design in terms of energy consumption, delay, and area, and our calculations indicate that, when compared with its domain conversion counterpart, our proposal consumes 49.5% less energy, at the expense of 48% area and 76.5% delay overhead, respectively.**

I. Introduction

Various research fields and industries have witnessed significant changes and developments during recent years. One such field that have experienced huge extension is spintronics [4], [7], [3], which is considered one of the main challenger to eventually replace current Complementary Metal-Oxide-Semiconductor (CMOS) technology [15], [12]. One rather promising ultra-low power spintronics avenue makes use of Spin Waves (SWs) as data carriers and performs computation by means of SWs interference [11].

While, potentially speaking, information can be encoded in various SW parameters, e.g., wavelength, frequency, amplitude, the most natural way is to rely on the SW phase for this purpose, i.e., information is encoded in the (relative) SW phase and a relative phase of 0 represents a logic 0, while a relative phase of π a logic 1. Given that, an odd number of SWs coexisting in the same wave-guide constructively interact if in phase and destructively if out of phase, such an encoding provides natural support for majority voting. By following this line of thinking, researchers have suggested the utilization of the 3-input Majority Gate (MAJ3) [9], [6], [5], [19], [13] as the primary building block for the implementation of complex SW-based logic circuits. While MAJ3 and Inverter, which is implemented by just changing the MAJ3 output reading position [19], form a universal gate set, many hurdles exist, e.g., fan-out achievement, gate cascading, on the road towards SW domain only non-toy circuit implementations. To address such issues one needs to rely on hybrid SW-CMOS systems that make use on domain converters, which are energy expensive and diminish if not nullify the ultra-low power promise of the SW-based computing paradigm.

One of the main SW domain-only computation roadblock is the fact that MAJ3 gates are not input-output compatible, which precludes their direct cascading. This is due to the fact that MAJ3 SW interference can create output waves with different amplitudes ('weak' and 'strong' majority), despite having the same phase difference, thus the same logic value, as graphically depicted in Fig. 1.

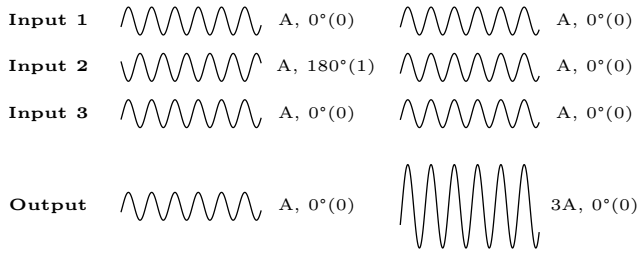

Fig. 1. 'Weak' vs 'Strong' MAJ3 gate output.

The cascading problem is not apparent when examining the output of a single MAJ3 gate, since only the phase difference with a reference signal is considered to determine

This project has received funding from the European Union's Horizon research and innovation program under grant agreement No 101070417 "Computation Systems Based On Hybrid Spin-Wave–CMOS Integrated Architectures" - SPIDER.

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2024 IEEE 24th International Conference on Nanotechnology (NANO) | 979-8-3503-8624-0/24/$31.00 ©2024 IEEE | DOI: 10.1109/NANO61778.2024.10628789

the gate output value, i.e., 0 or 1. However, when a 'strong' majority is passed on to a next MAJ3 gate, it can overpower the other two inputs, regardless of their values, leading to an incorrect result. For instance, if the output of the 1^{st} MAJ3 gate is a 'strong' majority with a logic value of 0, and the other two inputs of the 2^{nd} gate are 1, the 'strong' majority signal dominates the SW interference within the 2^{nd} MAJ3 gate resulting into a wrong output logic value of 0, as depicted in Fig. 2.

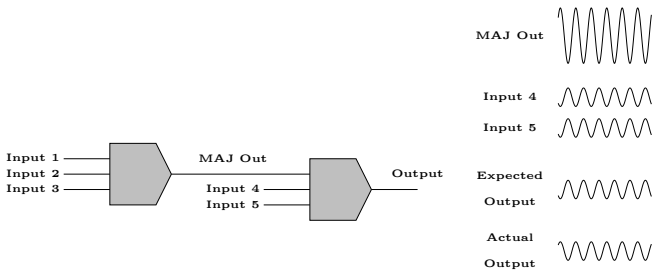


Fig. 2. SW MAJ3 gates direct cascading.

This problem can be dealt with by double SW-charge-SW domain conversion, which is rather power expensive. Moreover, given that the SW computing energy efficiency comes from the fact that after SW generation no (negligible) power is consumed by SW propagation through the waveguides, one should maximize the amount of computation before performing any domain conversion. As domain conversion based gate cascading limits the SW computing island to one MAJ3 gate only, it precludes the full utilization of the SW computing paradigm potential. Alternatively, cascading can be performed by means of directional coupling, which normalizes the MAJ3 SW amplitude in the case of a 'strong' majority [22], [21], [14], but such an approach induces significant MAJ3 gate area and delay overheads since a second waveguide and longer propagation paths are required.

In this paper we propose to perform 'strong' majority normalization by taking advantage of the otherwise detrimental natural SW strength attenuation induced by Gilbert damping [18]. The main idea behind our proposal is to make use of SW attenuation profile in a certain material to determine the transducer (antenna) positions such that when the 1^{st} MAJ3 gate output reaches 2^{nd} MAJ3 gate it is weak enough not to dominate its output but still strong enough to participate into the 2^{nd} MAJ3 gate interference process.

The paper is organized as follows: In Section II we introduce the novel SW gate cascading methodology and in Section III we present a concept design based on the proposed technique and verify its correct behavior by means of micromagnetic simulations. In Section IV, we provide implementation results and a comparison between our implementation and current state-of-the-art. We conclude the paper with a few closing thoughts and future work directions.

II. Direct MAJ3 Cascading Methodology

Instead of actively normalizing MAJ3 SW output by external means, e.g., domain conversion, lateral coupling, we propose to allow for a MAJ3 gate output longer SW propagation path such as its amplitude attenuates due to the natural decay induced by means of Gilbert damping [18] before reaching the next MAJ3 gate. Note that Gilbert damping depends on α a waveguide material parameter that characterizes the energy dissipation rate of the magnetic material and hence controls the propagation, and decay, of the propagating SW. Thus, by letting the SW amplitude to naturally decrease and carefully placing the input antennas (transducers) of the next MAJ3 gate, we can reach a waveguide configuration that allows for MAJ3 gate direct cascading within the SW domain.

Based on this, we propose a design consisting of two MAJ3 gates implemented over the same waveguide where the 1^{st} MAJ3 gate output is placed relatively far from the other two inputs of the 2^{nd} MAJ3 gate to ensure that its strength attenuates enough before it interferes with them. To obtain correct results the distance between the 1^{st} MAJ3 gate output and the other two input ports of 2^{nd} MAJ3 gate must be computed such that the condition presented in Fig. 3 are fulfilled.

To achieve proper functionality of the 2^{nd} MAJ3 gate, the 1^{st} MAJ3 gate output should have a lower than $2 \times A$ amplitude, where A is the unit SW amplitude value, to guarantee that it cannot dominate the other two 2^{nd} MAJ3 inputs, but also greater than $0.1 \times A$ such that it can still contribute to the result, especially when the other 2^{nd} MAJ3 gate two inputs are $0/1$ and $1/0$, thus they cancel each other.

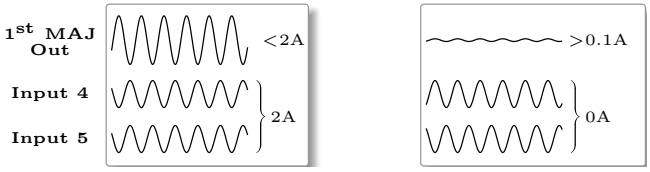


Fig. 3. Conditions to be fulfilled for the proposed technique to work

By meeting these conditions, a device can be built that connects two, or possibly more, MAJ3 gates together within a single waveguide. In the sequel, we focus on the design and verification of two MAJ3 gates directly connected within the SW domain which evaluates MAJ3(MAJ3(In_1, In_2, In_3), In_4, In_5), an essential component for building MAJ3 gate based complex circuits.

III. Verification

To demonstrate our proposal we construct an example design of MAJ3(MAJ3(In_1, In_2, In_3), In_4, In_5) and validate its correct behavior by means of mumax[3] based micro-magnetic simulations [20]. We select CoFeB as waveguide material due to its relatively large damping thus faster in terms of distance SW amplitude decay and a waveguide length L = $12\,\mu m$, width W = $50\,nm$, and thickness T = $1\,nm$. Since SWs can have different configurations depending on their orientation [11], [2], we apply a strong PMA anisotropy for the material since it results in a Forward Volume Spin Waves (FVSWs) configuration, which is ideal for CoFeB.

Last but not least, we apply an external field of B_{ext} = 60 mT with the same orientation as the anisotropy, to slightly alter the dispersion relation. Finally, we set the SW excitation frequency to f = 5.2 GHz. The set of these parameters, which are presented in Table I, leads to the excitation of spin waves with a wavelength of λ = 150.5 nm. Note that small wavelength SWs excitation [10] provides easier control and examination of the results and device scaling to smaller dimensions reducing, which reduces the circuit power consumption and delay.

TABLE I
SIMULATION PARAMETERS.

Parameter	Value
M_s	1.2 MA m^{-1}
A_{ex}	18 pJ m^{-1}
k_{anis}	0.9 MJ m^{-3}
B_{ext}	60 mT
f_{exc}	5.2 GHz

To determine the distance between the gate ports, we first simulate an one antenna only design to determine the attenuation profile for SW excited within this specific structure as depicted in Fig. 4.

Based on this behavior, we determine the placement of the input and output ports at specific waveguide locations such that the conditions mentioned in Fig. 3 are satisfied. For the 1st MAJ3 gate, the position of the output port should be far away from In_4 and In_5, but also close to the inputs In_1 - In_3. As for the output of the 2nd MAJ3 gate, the output port should be placed somewhere in between the 1st and 2nd gate where the output of the 1st MAJ3 gate has attenuated enough and cannot overpower the other two inputs of the 2nd gate. For these reasons, the inputs of the 1st MAJ3 gate are placed at $3 \times \lambda$ distance between them, and its output at $8 \times \lambda$ from In_1 antenna. As for the inputs In_4 and In_5 of the 2nd MAJ3 gate, the first one is placed at $40 \times \lambda$ while the latter one at $43 \times \lambda$ from In_1. The input and output ports positions along with the influence, compared to unit amplitude A, each input has on those output positions, is presented in Table II while a complete schematic of the design is depicted in Fig. 5.

TABLE II
INPUT AND OUTPUT PORTS LOCATIONS.

Antenna	Location	SW Amplitude on 1st MAJ3 Out	SW Amplitude on 2nd MAJ3 Out
In_1	$x = -4\,\mu m$	$0.75 \times A$	$0.3052 \times A$
In_2	$x + 3 \times \lambda$	$0.8246 \times A$	$0.33 \times A$
In_3	$x + 6 \times \lambda$	$0.92 \times A$	$0.38 \times A$
In_4	$x + 40 \times \lambda$	$0.3052 \times A$	$0.75 \times A$
In_5	$x + 43 \times \lambda$	$0.2592 \times A$	$0.6765 \times A$
1^{st} $MAJ3$ Out	$8 \times \lambda$	-	-
2^{nd} $MAJ3$ Out	$32 \times \lambda$	-	-

To verify the correct operation of the proposed design, we evaluated all 32 possible combinations of inputs, many of which would normally fail without the use of a domain converter. A reference signal of logic value 0, indicated with the color red, is utilized to measure the phase difference between the signals and thus interpret their logic values. As it can be observed in Fig. 6, the proposed design properly functions. For example, in $\boldsymbol{Case\ \#3}$, the three ports of the 1st MAJ3 gate all have a logic **0** as their input and the output they produce is also **0** as indicated by the color red which matches that of the reference signal. The 'strong' majority then propagates and interferes with the two input ports of the 2nd gate. Based on their values $(\mathbf{0}, \mathbf{1}, \mathbf{1})$ logic **1** should be the expected output which is indeed verified, as indicated by the color blue. The same holds true for all the other input value combinations.

IV. RESULTS & IMPLICATIONS

Since we demonstrated proper operation of the proposed structure a close examination of its figure of merit is of interest to assess its advantages and possible disadvantages. To this end we compare the delay and energy consumption of our proposal with the ones of the structure computing MAJ3(MAJ3(In_1, In_2, In_3), In_4, In_5) by means of **2** MAJ3 gates cascaded by means of domain conversion.

Table III summarize the energy consumption and delay of the proposed design and the domain conversion based counterpart. The hybrid SW-CMOS device consists of **6** inputs (SW excitation ports), **3** for each MAJ3 gate, and **2** output (SW reading ports). In contrast, the proposed design consists of **5** input ports and **2**, or **1** if the 1st MAJ3 out is not required, reading ports. Thus our proposal requires

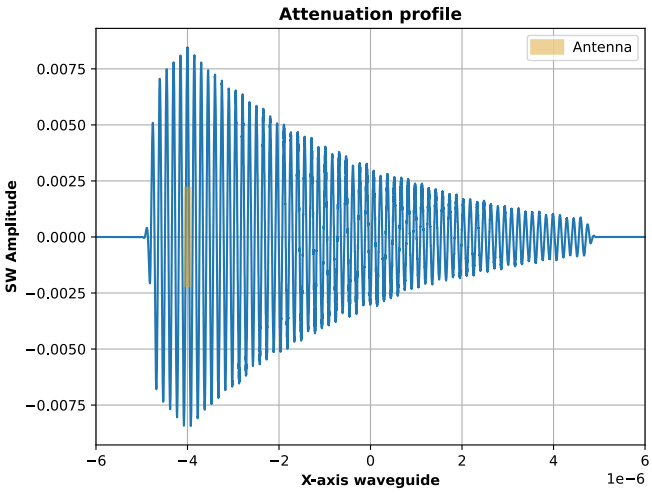


Fig. 4. SW amplitude attenuation profile.

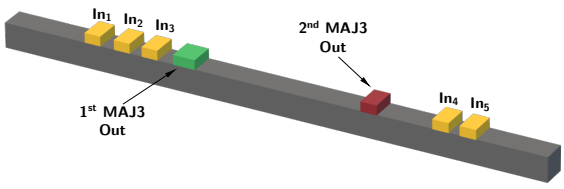
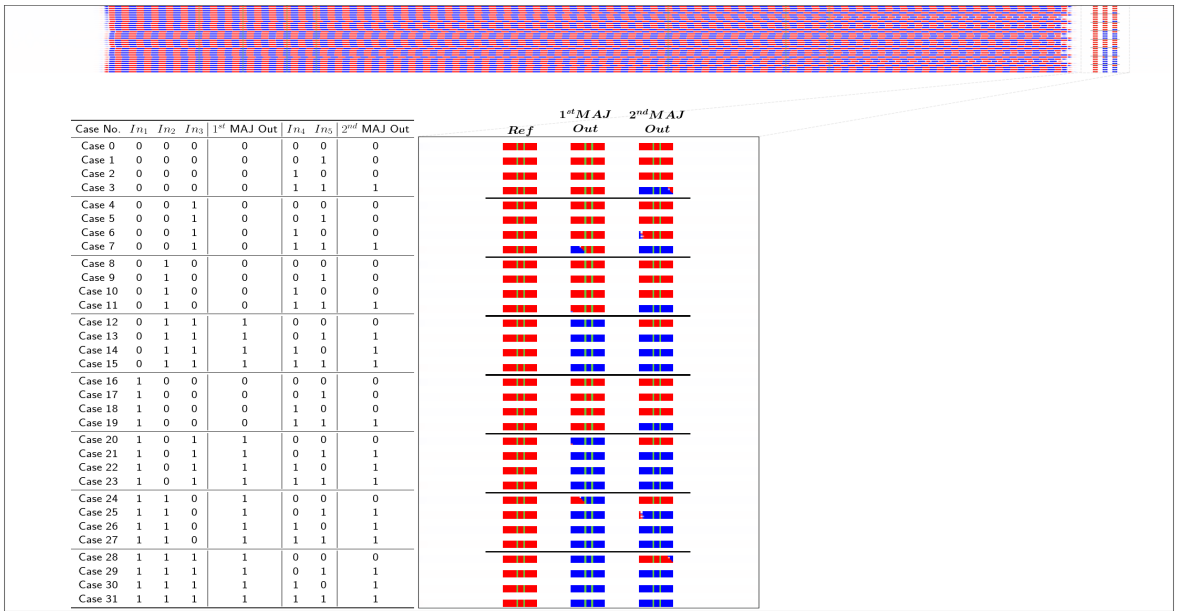


Fig. 5. MAJ3(MAJ3(In_1, In_2, In_3), In_4, In_5) implementation.



Case No.	In_1	In_2	In_3	1^{st} MAJ Out	In_4	In_5	2^{nd} MAJ Out
Case 0	0	0	0	0	0	0	0
Case 1	0	0	0	0	0	1	0
Case 2	0	0	0	0	1	0	0
Case 3	0	0	0	0	1	1	1
Case 4	0	0	1	0	0	0	0
Case 5	0	0	1	0	0	1	0
Case 6	0	0	1	0	1	0	0
Case 7	0	0	1	0	1	1	1
Case 8	0	1	0	0	0	0	0
Case 9	0	1	0	0	0	1	0
Case 10	0	1	0	0	1	0	0
Case 11	0	1	0	0	1	1	1
Case 12	0	1	1	1	0	0	0
Case 13	0	1	1	1	0	1	1
Case 14	0	1	1	1	1	0	1
Case 15	0	1	1	1	1	1	1
Case 16	1	0	0	0	0	0	0
Case 17	1	0	0	0	0	1	0
Case 18	1	0	0	0	1	0	0
Case 19	1	0	0	0	1	1	1
Case 20	1	0	1	1	0	0	0
Case 21	1	0	1	1	0	1	1
Case 22	1	0	1	1	1	0	1
Case 23	1	0	1	1	1	1	1
Case 24	1	1	0	1	0	0	0
Case 25	1	1	0	1	0	1	1
Case 26	1	1	0	1	1	0	1
Case 27	1	1	0	1	1	1	1
Case 28	1	1	1	1	0	0	0
Case 29	1	1	1	1	0	1	1
Case 30	1	1	1	1	1	0	1
Case 31	1	1	1	1	1	1	1

Fig. 6. MAJ3(MAJ3(In_1, In_2, In_3), In_4, In_5) micromagnetic simulation results.

one less excitation port and in case the 1st MAJ3 gate output is not externally needed (for fanout purposes) one less reading port. While the actual excitation and reading ports energy consumption figures very much depend on the utilized CMOS technology, which is out of the scope of our investigation, we can still compare the two designs by making use of previously reported estimates. The energy consumption of a single magnetoelectric (ME) cell, excitation port, was calculated to be $14.4\,\mathrm{aJ}$ [24], [25], [17], while the energy for reading a SW signal was calculated to be $2.7\,\mathrm{fJ}$. Based on these estimates our proposal reduces the energy consumption by $2.714\,\mathrm{fJ}$ when the output of the 1st MAJ3 is not explicitly required for fan-out purposes and $14.4\,\mathrm{aJ}$ otherwise.

Looking at the delay of the two approaches, the hybrid system can complete the calculations after 2 MAJ3 gate delay and one domain conversion delay. On the other hand, the proposed design delay includes the time needed to excite the input SWs plus the time needed for the propagation of all the signals to the output port and the output signal reading. To compare the two designs we have to compute their SW propagation to output delays. To calculate those, we performed micromagnetic simulations on the proposed design and a single MAJ3 gate and determined that the time needed for proper operation is $13.5\,\mathrm{ns}$ and $3.5\,\mathrm{ns}$, respectively.

In total, the hybrid SW-CMOS system needs **2** times the propagation and excitation delay of a single MAJ3 gate plus and **2** output readings. As for the proposed design, the propagation and excitation delay of the structure should also be considered while only one reading is necessary. By making use of the numbers reported in [24], [25], [17] the SW excitation delay in $0.42\,\mathrm{ns}$ and the SW reading is $0.03\,\mathrm{ns}$ we compute an overall delay of $7.9\,\mathrm{ns}$ for the hybrid SW-CMOS system and $13.95\,\mathrm{ns}$ for the proposed design.

Assuming that each transducer occupies an area of F^2 we calculate the total area of the two approaches for F=$50\,\mathrm{nm}$ as it was used in the simulations. For the conversion-based approach, a total of 8 ports are required, along with the area the two MAJ3 waveguides occupy. The waveguides are assumed to have the same geometry and characteristics as the attenuation based counterpart, but each with a reduced length of $4\,\mu\mathrm{m}$. Although the proposed gate reduces the total number of ports to 6, the approach adds a 48% area overhead, compared to the hybrid system, since it requires a longer waveguide ($12\,\mu\mathrm{m}$) for the placement of the antennas and the SW propagation.

We note that we only did the comparison at the device level where the advantages of the proposed design are already demonstrated. However, the use of the proposed device on more complex circuits [1], [8], [23], [16] can offer even better results, reducing the power consumption of the circuits by a significant percentage. The comparison on a circuit level is however out of the scope of this paper.

TABLE III
ENERGY CONSUMPTION, DELAY, AND AREA COMPARISON.

	Ports (Excitation + Reading)	Energy Consumption (fJ)	Delay (ns)	Area (μm^2)
2MAJ3 Gates + Converter	6× ME + 2× Read	5.4864	7.9	0.8362
Controlled SW Amplitude Attenuation Gate	5× ME + 1× Read	2.772	13.95	1.2391

V. CONCLUSIONS

In this paper we introduced an approach to circumvent the main roadblock on the way from Spin Wave Majority gates to circuits, which is related to the fact that due to the very nature of SW interference MAJ3 gates are not input output coherent, i.e., produce output waves with different amplitudes corresponding to 'weak' and 'strong' majority, which precludes their direct cascading within the SW domain. We proposed a

gate cascading technique that take advantage on the natural SW amplitude decay while propagating through a magnetic conduit. We demonstrated the concept by constructing the building block MAJ3(MAJ3(In_1, In_2, In_3), In_4, In_5) and verified its correct behaviour by means of micromagnetic simulations. We evaluated the proposed design in terms of energy consumption, delay, and area, and our calculations indicate that, when compared with its domain conversion counterpart, our proposal consumes 49.5% less energy, at the expense of 48% area and 76.5% delay overhead, respectively.

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