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Hard superconducting gap in germanium

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The co-integration of spin, superconducting, and topological systems is emerging as an exciting pathway for scalable and high-fidelity quantum information technology. High-mobility planar germanium is a front-runner semiconductor for building quantum processors with spin-qubits, but progress with hybrid superconductor-semiconductor devices is hindered by the difficulty in obtaining a superconducting hard gap, that is, a gap free of subgap states. Here, we address this challenge by developing a low-disorder, oxide-free interface between high-mobility planar germanium and a germanosilicide parent superconductor. This superconducting contact is formed by the thermally-activated solid phase reaction between a metal, platinum, and the Ge/SiGe semiconductor heterostructure. Electrical characterization reveals near-unity transparency in Josephson junctions and, importantly, a hard induced superconducting gap in quantum point contacts. Furthermore, we demonstrate phase control of a Josephson junction and study transport in a gated two-dimensional superconductor-semiconductor array towards scalable architectures. These results expand the quantum technology toolbox in germanium and provide new avenues for exploring monolithic superconductor-semiconductor quantum circuits towards scalable quantum information processing.

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The intimate coupling between superconductors and semiconductors in hybrid devices is at the heart of exciting pursuits, including topological qubits with Majorana zero modes^{1,2}, superconducting (Andreev) spin qubits³, and gate-tunable superconducting qubits⁴. Combining hybrid devices with high-fidelity semiconductor spin qubits in a single material platform may resolve key challenges for scalable quantum information processing. In particular, quantum information transfer between spin and topological qubits^{5–8} may enable a universal gate set for topological quantum computation and, conversely, superconductors may be used to coherently couple spin qubits at a distance via crossed Andreev reflection^{5,9} or topologically protected links¹⁰.

The use of epitaxial superconducting Al to induce a hard superconducting gap in III-V semiconductors^{11,12} stimulated great progress with hybrid devices, leading to experimental reports of topological superconductivity in planar Josephson junctions¹³ and in electrostatically defined quasi-1D wires¹⁴, the demonstration of Andreev spin qubits³, and the realization of a minimal Kitaev chain in coupled quantum dots¹⁵. However, spin qubits in III-V semiconductors suffer from the hyperfine interactions with the nuclear spin bath¹⁶ that severely deteriorate their quantum coherence¹⁷ and challenges their integration with hybrid devices.

On the other hand, spin qubits with quantum dots in Ge^{18–21} can achieve long quantum coherence due to the suppressed hyperfine interaction²² and the possibility of isotopic purification into a nuclear spin-free material²³. Thanks to the light effective mass²⁴ and high mobility exceeding one million cm^2/Vs ²⁵, holes in planar Ge/SiGe heterostructures have advanced semiconductors spin qubits to the universal operation on a 2×2 qubit array²⁶, and the shared control of a 16 semiconductor quantum dot crossbar array²⁷. Moreover, the ability of holes to make contacts with low Schottky barrier heights to metals²⁸, including superconductors, makes Ge a promising candidate for hybrid devices. Initial work used superconducting Al to contact Ge either via thermal diffusion^{29–31} or by deposition on the sidewalls of etched mesas^{32,33}. However, the key demonstration of a superconducting gap in Ge free of subgap quasiparticle states is lacking, challenged by the difficulty of contacting uniformly a buried quantum well (QW) with a superconductor, whilst maintaining the low disorder at the superconductor-semiconductor interface and in the semiconductor channel.

Here we address these challenges and demonstrate a hard superconducting gap in Ge. We contact the quantum well with a superconducting germanosilicide (PtSiGe), similar to the silicidation process used by the microelectronics industry for low resistance contacts³⁴. The superconductor is formed uniformly within the heterostructure and reaches the buried quantum well via a controlled thermally-activated solid phase reaction between the metal (Pt) and the semiconductor stack (Ge/SiGe). This process is simple, robust, and does not require specialised vacuum conditions or etching because the superconductor-semiconductor interface is buried into the pure semiconducting heterostructure and consequently remains pristine. This represents a conceptually different approach compared to the subtractive nanofabrication processes commonly used for hybrid devices, since our additive process does not deteriorate the active area of the semiconductor. As a result, we demonstrate a suite of reproducible Ge hybrid devices with low disorder and excellent superconducting properties.

Results

Material properties. Our approach to superconductor-semiconductor hybrid devices in Ge is illustrated in Fig. 1a. We

use an undoped and compressively-strained Ge quantum well, grown by chemical vapor deposition on a Si(001) wafer³⁵ and separated from the surface by a SiGe barrier (Methods). This heterostructure supports a two-dimensional hole gas (2DHG) with high mobility ($\sim 6 \times 10^5 \text{ cm}^2/\text{Vs}$), long transport scattering time τ (~ 30 ps), and long mean free path ($\sim 7 \mu\text{m}$) (Supplementary Fig. 1) and hosts high-performance spin-qubits²⁰. Crucial for the reliable search of topological superconductivity³⁶ and for scaling to large spin-qubit architectures³⁷, the disorder in our buried Ge quantum wells is characterised by an energy level broadening $\hbar/2\tau$ of ~ 0.01 meV, which is more than one order of magnitude smaller than in the other material systems exhibiting a hard superconducting gap (Supplementary Table 1).

As shown by the schematics in Fig. 1a, we obtain PtSiGe contacts to the quantum well by room-temperature evaporation of a Pt supply layer, metal lift-off, and rapid thermal process at 400°C (Methods). This low-temperature process preserves the structural integrity of the quantum well grown at 500°C , whilst activating the solid phase reaction driving Pt into the heterostructure and Ge and Si into the Pt (Supplementary Fig. 3). As a result, low-resistivity germanosilicide phases are formed^{38,39} and under these process conditions the obtained PtSiGe films are superconducting with a $T_c \approx 0.5$ K and an in-plane critical field of $B_{c\parallel} \approx 400$ mT (Supplementary Fig. 2). Finally, we use patterned electrostatic gates, insulated by dielectric films in between, to accumulate charge carriers in the quantum well and to shape the electrostatic confinement potential of the hybrid superconductor-semiconductor devices (Methods). This approach to hybrid devices is different compared to the conventional process with 1D nanowires, where an epitaxial superconductor proximitizes the semiconductor region underneath. Because we do not perform any etch during the nanofabrication of hybrid devices, the low-disorder landscape that determines the 2DHG high mobility is likely to be preserved when further dimensional confinement is achieved by means of electrostatic gates. By contrast, for processes where etching of the superconductor is required, the fabrication of hybrid devices yields to mobility degradation⁴⁰.

The morphological, structural, and chemical properties of the hybrid devices are inferred by aberration corrected high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) and electron energy-loss spectroscopy (EELS). Figure 1b shows a HAADF-STEM image of a cross-section of a superconductor-normal-superconductor quantum point contact (SNS-QPC) taken off-center to visualise the two gate layers (Fig. 2a shows a top view of the device). We observe a uniform quantum well of high-crystalline quality, with sharp interfaces to the adjacent SiGe and absence of extended defects. As a result of the annealing, Pt diffuses predominantly vertically through the SiGe spacer reaching the quantum well. The sharp lateral interfaces between the two PtSiGe contacts and the QW in between set the length of the channel populated by holes via the top-gates. The PtSiGe film presents poly-crystalline domains with a crystal size up to 50×50 nm and orthorhombic phase (PBNM, space group number 62)⁴¹. This is inferred from the power spectra or fast Fourier transforms (FFTs) taken from the two PtSiGe domains interfacing with the QW from the left contact, shown in Fig. 1c along with a schematic view of the unit cell of such phase. More detailed studies by atomic-resolution plane HAADF-STEM are required to assess the junction uniformity in the direction parallel to the junction and whether this would impact Majorana experiments. The analysis of EELS elemental concentration profiles across the Ge QW \rightarrow PtSiGe heterointerface (Supplementary Fig. 4) reveals that the threefold PtSiGe stoichiometry is Ge-rich, with relative composition in the range between $\text{Pt}_{0.1}\text{Si}_{0.2}\text{Ge}_{0.7}$ and $\text{Pt}_{0.1}\text{Si}_{0.05}\text{Ge}_{0.85}$ depending locally on

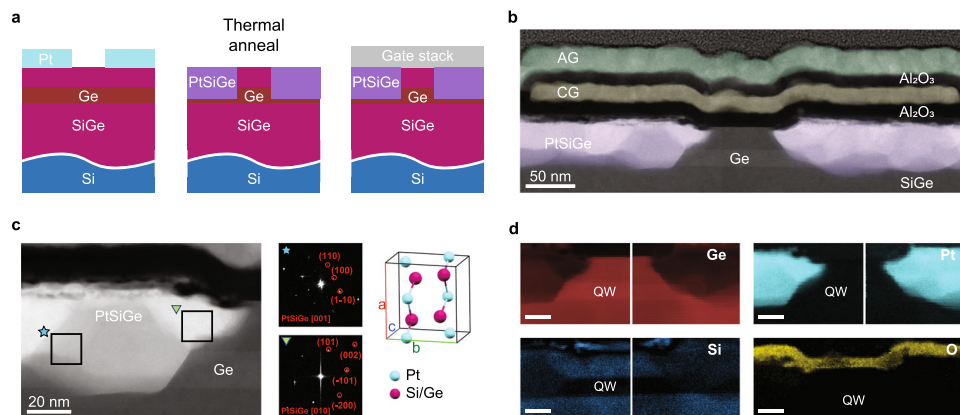


Fig. 1 Material properties of superconductor-semiconductor Ge devices. **a** Schematics of the fabrication process for a superconductor-normal-superconductor quantum point contact (SNS-QPC). First, platinum is deposited on the heterostructure, then thermal annealing at 400 °C drives Pt in the heterostructure to form PtSiGe, finally two gate layers are deposited, insulated by Al₂O₃. **b** False-color high angle annular dark field scanning transmission electron microscopy (HAADF STEM) image of a cross-section of a SNS-QPC. The PtSiGe contacts are violet, the Ti/Pd constriction gate (CG) operated in depletion mode is yellow, the Ti/Pd accumulation gate (AG), used to populate the quantum well, is green. A scanning electron microscopy top view image of this device is shown in Fig. 2. **c** Atomic resolution HAADF STEM image of the Ge/PtSiGe interface along with the indexed fast Fourier transforms (FFTs) of the two regions (black squares) within the PtSiGe contacts and a schematic of the PtSiGe orthorhombic unit cell. The corresponding ternary lattice parameters $T = a_T, b_T, c_T$ that define the dimensions of the unit cell can be calculated, in a first approximation, by Vegard's law: $T_{\text{PtSi}_{1-x}\text{Ge}_x} = x B_{\text{PtGe}} + (1-x) B_{\text{PtSi}}$ where $B = a_B, b_B, c_B$ are the lattice parameters of the binary compounds PtSi and PtGe, and x is the relative content of Ge with respect to Si. **d** Electron energy-loss spectroscopy (EELS) composition maps showing the Pt, Ge, Si and O signals for the central area of the TEM lamella of panel (b), the scale-bar indicates 50 nm. The PtGeSi stoichiometry is extracted by quantitative EELS analysis and reported in Supplementary Fig. 4.

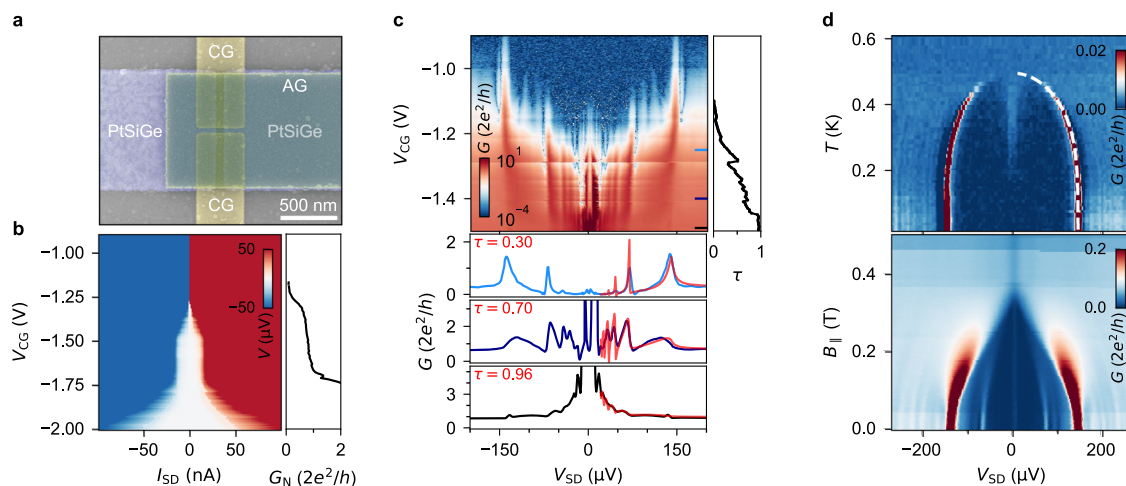


Fig. 2 Highly-transparent Josephson junctions. **a** False-color scanning electron microscope image of the SNS device. The PtSiGe contacts are violet, the constriction gates (CG) are yellow and the accumulation gate (AG) is green. The channel length between the two superconducting leads is 70 nm and the channel width between the constriction gates is 40 nm. The two constriction gates are separate by design but always shorted together during measurements. **b** Color map of the voltage drop across the junction V vs source-drain current I_{SD} and constriction-gate voltage V_{CG} at zero magnetic field along with normal-state conductance G_{N} trace vs V_{CG} . G_{N} is calculated as the conductance average where the voltage drop across the device is in the range [500, 650] mV or $[-650, 500]$ mV, that is much higher than the estimated superconducting gap. **c** Color map of G in units of $2e^2/h$ vs the source-drain voltage V_{SD} and V_{CG} . Bottom panel shows line-cuts of conductance at $V_{\text{CG}} = [-1.25, -1.4, -1.49]$ V, red lines are the fit with the coherent scattering model from which transparency τ is extracted. Right inset shows the evolution of the transparency, as extracted from the fitting of conductance curves to the coherent scattering model (Methods), with the constriction gate V_{CG} . **d** Color map of G vs T and V_{SD} (top panel), and vs B_{\parallel} and V_{SD} (bottom panel), where B_{\parallel} is the in-plane magnetic field in the direction of transport and T the temperature. The color scale in panel (d) has been saturated to better infer the low conductance limit. The source-drain bias is applied between the PtSiGe contacts, and the voltage drop across the junction is measured with a standard 4-terminal setup. The accumulation voltage for measurements in (b, c and d) was set to -4.5 V, where the 2DHG is expected to reach saturation density (see Supplementary Fig. 1) of $\approx 6 \times 10^{11} \text{ cm}^{-2}$ ³⁵. Measurement presented in (b, c) and in panel (d (bottom)), are performed at 15 mK, corresponding to an electron temperature of -25 mK.

the analysed grain. The EELS compositional maps in Fig. 1d show the elemental distribution of Ge, Si, Pt, Al, and O, at the key regions of the device. We observe Pt well confined to the two contacts areas, which also appear Ge-rich. Crucially, O is detected only in the Al₂O₃ dielectric layer below the gates, pointing to a

high-purity quantum well and a pristine superconductor-semiconductor interface.

Highly transparent Josephson junction. We perform low-frequency four-terminal current and voltage bias measurements

(Methods) on the SNS-QPC device shown in Fig. 2a to infer the properties of the superconductor-semiconductor interface. Accumulation (AG, in green) and constriction (CG, in yellow) gates control transport within the 70 nm long channel between the two PtSiGe leads. We apply a large negative voltage to the accumulation gate to populate the quantum well with holes, and we then control the effective width of the channel by applying a more positive voltage to the constriction gates, thus depleting the underlying quantum well.

The current bias measurements (Fig. 2b) reveal a tunable supercurrent with a plateau when the constriction gate voltage V_{CG} is in the range $\approx [-1.75, -1.50]$ V. This is the same range where we observe the first conductance plateau in the normal-state conductance G_N (Fig. 2b, right inset), indicating that the switching current (I_{sw}) plateau observed in the color plot stems from the supercurrent discretization due to the discrete number of modes in the QPC^{30,42}. Supercurrent discretization up to the third conductance plateau is shown in Supplementary Fig. 5 (data are for a different SNS-QPC device with identical design to the one presented here). The discretization of the supercurrent at zero magnetic field, indicates that the quality of the 2DHG is preserved also upon the formation of the superconducting contacts. We use the switching current as a lower bound for the critical current and we estimate an $I_{sw}R_N$ product of 51 μ V, showing an improvement as compared to previous results obtained with pure Al contacts in Ge QWs^{30,32,33}, despite the Al T_c is higher than the PtSiGe T_c . The measured $I_{sw}R_N$ product is ~ 0.5 times the theoretical I_cR_N product calculated for a ballistic short junction using the Ambegaokar-Baratoff formula $\pi\Delta^*/2e = 110 \mu$ V with I_c being the critical current, Δ^* the induced superconducting gap and e the electron charge⁴³. This discrepancy has been observed in previous works^{30,44} and is consistent with a premature switching due to thermal activation⁴⁵.

By operating the device in voltage-bias configuration and stepping the constriction gates, we observe in the conductance color plot the typical signature of multiple Andreev reflections (MARs) (Fig. 2c). When the applied voltage bias corresponds to an integer fraction of $2\Delta^*$, with Δ^* being the induced superconducting gap, we observe differential conductance dI/dV peaks (dips) in the tunneling (open) regime^{46,47}. We measure MARs up to the 5th order, suggesting that the coherence length ξ_N in the Ge QW is a few times larger than the junction length L , and setting a lower bound to the phase coherence length in the QW $l_\psi > 5L = 350$ nm. These observations are consistent with the findings of ref. ³³ where a similar Ge/SiGe heterostructure is used. Fitting the differential conductance with the coherent scattering model described in ref. ⁴⁸ (and used in refs. ^{44,47,49}) reveals single channel transport with gate tunable transparency up to 96%. Such a high transparency confirms the high quality interface between the PtSiGe and the Ge QW. From the MARs fit we estimate an induced superconducting gap $\Delta^* = 70.6 \pm 0.9 \mu$ eV, which is about half compared to the $\Delta^* = 129 \mu$ eV¹⁴ and 150μ eV⁵⁰ for recent InAs-Al devices reporting topological superconductivity.

Further, we characterise the evolution of the induced superconducting gap with temperature and magnetic field. After setting the device in tunneling regime, where sharp coherence peaks are expected at $e|V_{SD}| = 2\Delta^*$ (Fig. 2d), we observe the induced superconducting gap closing with increasing temperature and magnetic field. By fitting the temperature dependence of the coherence peaks with the empirical formula from ref. ⁵¹ we obtain a critical temperature of 0.5 K. The peak close to zero bias emerging at $T > 0.2$ K can be explained in terms of thermally-activated quasiparticle current⁴⁹. The in-plane magnetic field in the transport direction quenches the superconductivity at $B_{c\parallel} = 0.37$ T. The same critical field is found for the in-plane direction perpendicular to the transport direction while for the out of plane

direction $B_{c\perp} = 0.1$ T (Supplementary Fig. 6). This in-plane vs out-of-plane anisotropy is expected given the thin-film nature of the PtSiGe superconductor⁴⁵.

Hard induced superconducting gap. To gain insights into the quality of the Ge/PtSiGe junction we characterise transport through the normal-superconductor quantum point contact (NS-QPC) device shown in Fig. 3a. Importantly, the methodology based on spectroscopy of NS devices alleviates the ambiguity of measuring the amount of quasiparticle states inside the gap with SNS junctions³¹. On the left side of the QPC there is a PtSiGe superconducting lead and on the right side a normal lead consisting of a 2DHG accumulated in the Ge QW. With the accumulation gate (AG) set at large negative voltages to populate the QW we apply a more positive voltage to the constriction gates (CG), creating a tunable barrier between the superconducting and the normal region. In Fig. 3b we progressively decrease the barrier height (decreasing V_{CG}) going from the tunneling regime, where conductance is strongly suppressed, to a more open regime where conductance approaches the single conductance quantum G_0 . Line-cuts of the conductance color map are presented in the bottom panel of Fig. 3c. In the tunneling regime, we observe a hard induced superconducting gap, characterised by a two orders of magnitude suppression of the in-gap conductance to the normal-state conductance, and the arising of coherence peaks at $e|V_{SD}| \approx \Delta^* = 70 \mu$ eV. Figure 3b also shows that the induced superconducting gap varies with the constriction gate voltage. This observation brings confidence that we are measuring the induced superconducting gap rather than the parent gap⁵². A possible explanation is that, upon increasing the density in the semiconductor nearby the junction, the coupling to the parent superconductor might vary, as also observed in other hybrid nanostructures⁵³.

The evolution of the gap as a function of in-plane magnetic field (B_{\parallel}) shown in Fig. 3c confirms that the gap remains hard for finite magnetic fields up to 0.25 T, ultimately vanishing at $B_{\parallel} \approx 0.37$ T. The magnetic field evolution of the gap in all three directions matches the behaviour observed in the SNS-QPC (Supplementary Fig. 7).

Finally, Fig. 3d reports the conductance traces in tunneling regime for all the six measured devices (an overview of the geometries of these devices and the respective measurements are available in the Supplementary Fig. 8, the conductance maps for all these devices are shown in Supplementary Fig. 9). For all devices we observe suppression of conductance equal or larger than two orders of magnitude. At a quantitative level, the conductance traces of Fig. 3d are well fitted by the BTK theory⁵⁴ (Supplementary Fig. 9) consistent with a hard induced superconducting gap free of subgap states^{11,44}. This finding is the signature of a robust process that yields a reproducible high-quality superconductor-semiconductor interface, overcoming a long-standing challenge for hybrid superconductor-semiconductor quantum devices in Ge.

Superconducting quantum interference devices. We use the superconducting quantum interference device (SQUID) in Fig. 4a to demonstrate phase control across a Josephson junction, an important ingredient for achieving topological states at low magnetic field^{50,55–57}. The device is composed of two Josephson field-effect transistors (JoFETs) with a width of 2 μ m and 1 μ m for JoFET₁ and JoFET₂ respectively, and equal length of 70 nm. The critical current of the junctions I_{c1} and I_{c2} can be tuned independently by applying the accumulation gate voltages V_{AG1} and V_{AG2} to the corresponding gates. We investigate the oscillations of the SQUID switching current as a function of the

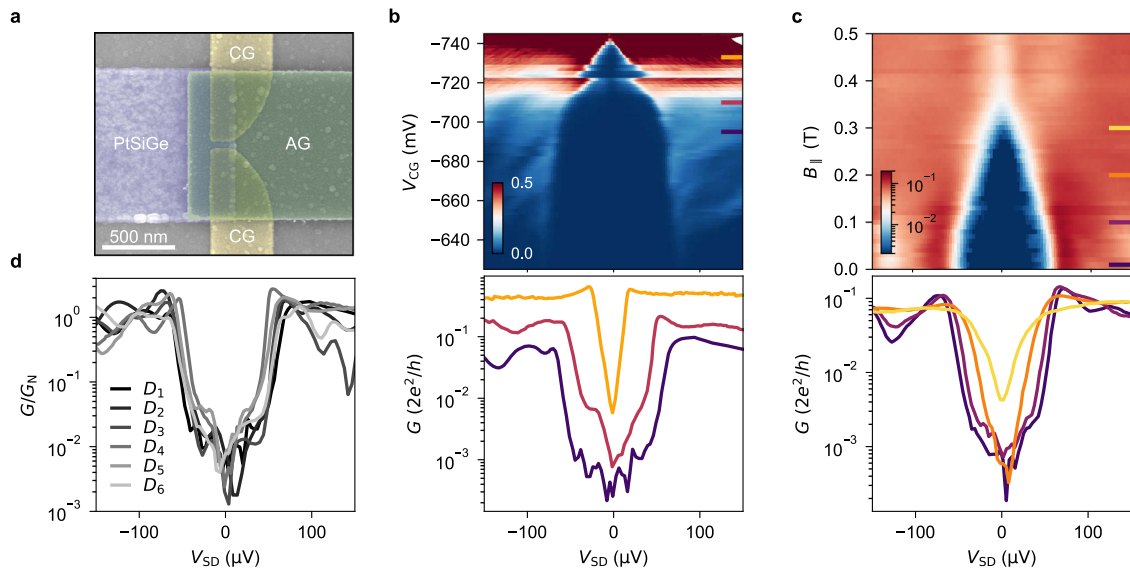


Fig. 3 Hard induced superconducting gap. **a** False-color SEM image of the normal-superconductor quantum point contact device (NS-QPC). The PtSiGe contact is violet, the constriction gate (CG) are yellow and the accumulation gate (AG) is green. The two constriction gates are separate by design but always shorted together during measurements. **b** Color map of conductance G vs the source-drain voltage V_{SD} and constriction gate V_{CG} , along with line cuts in log-scale of G at the constriction gate voltages $V_{CG} = [-733, -710, -695]$ mV marked by the colored segment in the color-plot. **c** Color map of G in units of $2e^2/h$ vs the in-plane magnetic field $B_{||}$ perpendicular to the transport direction and constriction gate V_{CG} , along with line cuts in log-scale of G at the field strength $B_{||} = [0.01, 0.1, 0.2, 0.3]$ T marked by the colored segment in the color-plot. **d** Conductance traces normalised to the above-gap conductance (G/G_N) vs V_{SD} in tunneling regime for 6 different NS-QPC devices D_1 – D_6 processed in the same fabrication run, device D_1 is the one reported in Fig. 3 a–c, in the remaining devices the constriction gates separation varies (specifications of these devices are provided in Supplementary Fig. 8).

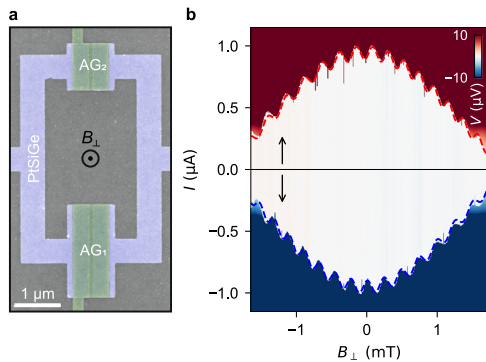


Fig. 4 Phase control of a Josephson junction in a SQUID. **a** False-color SEM image of the two JoFET SQUID device. The JoFETs have a channel length of 70 nm and a channel width of 1 μm and 2 μm respectively and can be independently controlled by gates AG_1 and AG_2 . The geometric loop area of the SQUID is of 10 μm^2 , calculated assuming a rectangle with sides positioned in the center of the PtSiGe loop cross-section. **b** Color-plot of voltage drop (V) across the SQUID vs current (I) and out-of-plane magnetic field (B_{\perp}). Arrows represent the direction of the current (I) sweep. With the gate voltages set at $V_{AG_1} = -3.5$ V and $V_{AG_2} = -1.65$ V the superconducting phase drops mainly over the second junction. Upon sweeping the out-of-plane magnetic field B_{\perp} we observe oscillations of the switching current. Red and blue dashed lines are the fit of the evolution of the critical current with magnetic field. The magnetic field is applied in the out of plane direction as depicted in panel (a).

out-of-plane-magnetic field penetrating the SQUID loop. Namely, we set V_{AG_1} and V_{AG_2} , such that both arms support supercurrent and $I_{c1} \gg I_{c2}$. This condition provides that the first junction is used as a reference junction and that the phase drop on it is flux independent, while the phase drop over the second junction is therefore modulated by the external flux through the loop. This allows the measurement of the current-phase-relation

(CPR) of the second junction. This is demonstrated in Fig. 4b where the shown SQUID oscillations are well fitted by the relation: $I_{c,\text{SQUID}} = I_{c1}(B_{\perp}A_1) + I_{c2}(B_{\perp}A_2) \sin(2\pi B_{\perp}A_{\text{SQUID}} - LI_{c1}(B_{\perp}A_1)/\Phi_0)$ where $I_{c1,2}(BA_{1,2})$ are the Fraunhofer dependencies of the critical current obtained from fitting the Fraunhofer pattern of each junction (Supplementary Fig. 10), $A_{1,2}$ are the junction areas, B_{\perp} is the out-of-plane magnetic field and Φ_0 the flux quantum. From the fit of the data in Fig. 4b (red dashed-line) we extract the effective SQUID loop area $A_{\text{SQUID}} = 8.9 \mu\text{m}^2$ (comparable to the 10 μm^2 SQUID geometric area) and the self-inductance $L = 1.65$ pH. In order to confirm for the self-inductance effects, we also fit SQUID oscillations for the opposite direction of the current bias (blue dashed-line) and we get similar values for the effective loop area and self-inductance.

Scalable junctions. As a first step towards monolithic superconductor-semiconductor quantum circuits in two dimensions, we fabricate and study transport in a macroscopic hybrid device comprising a large array of 510 PtSiGe islands (Fig. 5a) and a global top gate. Each pair of neighbouring islands forms a Josephson junction whose transparency can be tuned by the global accumulation gate. The top panel of Fig. 5b shows a current bias measurement of the junctions array resistance. As the accumulation gate becomes more negative, all the junctions are proximitized and a supercurrent flows through the device. Remarkably, as the source-drain current approaches the junctions critical current the whole array simultaneously switches from superconducting to resistive regime, as shown from the sharp resistance step (Fig. 5b top).

With this device we also study the evolution of the switching current in a small perpendicular magnetic field. In the bottom panel of Fig. 5b we observe Fraunhofer-like interference, along with the fingerprint of flux commensurability effects associated with the periodicity of the array. At integer numbers of flux quantum per unit area of the periodic array $f = B_{\perp}/B_0$, where

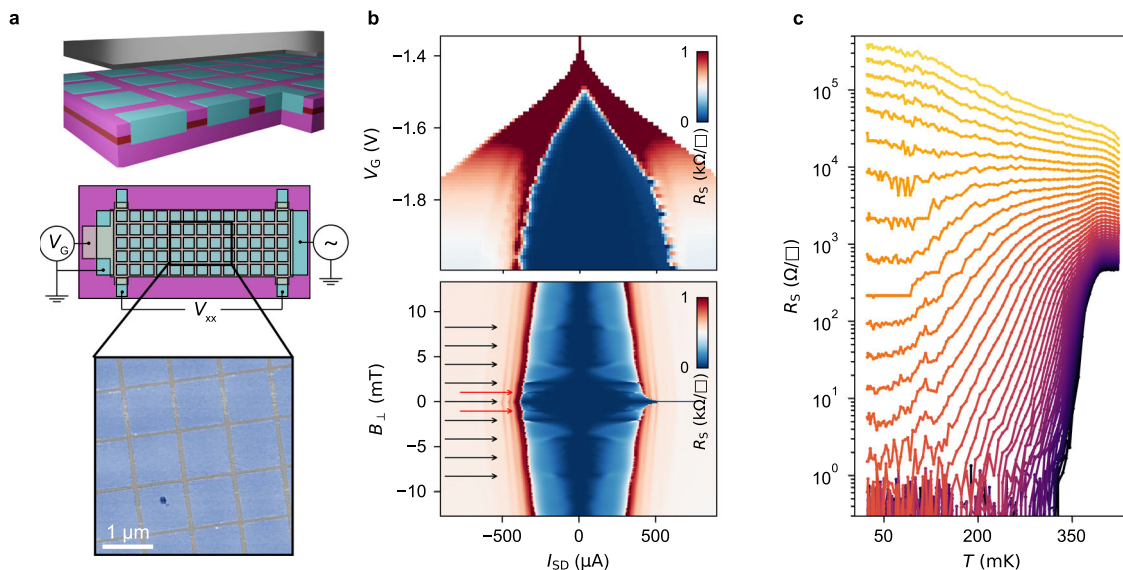


Fig. 5 A gated 2D superconductor-semiconductor array. **a** 3D and top schematics of an array of 51×10 PtSiGe islands. The inset shows an atomic force microscopy image of the PtSiGe islands of the array. The PtSiGe islands are 930×930 nm wide and the separation between neighbouring islands is of 70 nm. **b** Top panel shows a color map of sheet resistance (R_s) vs accumulation gate voltage V_G and source-drain current I_{SD} . Bottom panels show a color map of sheet resistance vs out of plane magnetic field B and source-drain current I_{SD} . The measurement is taken at gate voltage $V_G = -1.99$ V, where we expect carriers in the quantum well to approach a saturation density value of about $6 \times 10^{11} \text{ cm}^{-2}$ and have a mean free path ($\sim 7 \mu\text{m}$) much longer than the separation between neighbouring islands. Black arrows denote the magnetic field corresponding to one flux quantum Φ_0 per unit cell of the array. Red arrows correspond to one-half flux per unit cell. **c** Sheet resistance as a function of temperature for gate voltages ranging from -2 V to -1.55 V. Yellow curves correspond to small negative gates, and purple curves to large negative gates.

$B_0 = \Phi_0/A$ with A the junction area and Φ_0 the flux quanta, we observe switching current peaks at $\pm 1f$, $2f$, $3f$, $4f$ and $5f$, denoted by a black arrow in the plot. We also notice this effect at fractional values of f , most notably at $f/2$ (red arrow). Flux commensurability effects, due to the pinning and interference of vortices in Josephson junctions arrays, have been previously reported^{58,59}.

The observation of simultaneous switching of super-current and of the Fraunhofer pattern with flux commensurability effects, suggests that all islands effective areas are similar and that the supercurrent through the various junctions is comparable, meaning that all junctions respond synchronously to the applied gate voltage. This is further supported by the observation of sharp switching of super-current and the Fraunhofer pattern of a 1D array of superconducting islands presented in Supplementary Fig. 11.

Finally we present in Fig. 5c the sheet resistance as a function of temperature for different gate voltages. As the gate voltage becomes more negative, the coupling between neighbouring superconducting islands increases and the system transitions from an insulating to a superconducting regime. At low gate voltage the resistance increases with decreasing temperature (yellow curves) indicating the insulating state, while at high gates the resistance drops to zero (purple curves) owing to the global superconducting state. At intermediate gate voltages ($-1.95\text{V} \leq V_G \leq -1.93\text{V}$, orange curves) there is a transition where the resistance shows a weak temperature dependence. It will be interesting to study this regime in detail, in light of the recent claims of an anomalous metallic state between the superconducting and the insulating phases⁵⁹.

Discussion

In conclusion, we have developed superconducting germanosilicides for contacting Ge quantum wells, which has resulted in excellent superconducting properties imparted to the high-mobility 2DHG. We induced a hard superconducting gap in Ge, a large advancement compared to previous work on Ge

hybrid superconductor-semiconductor devices^{30–33}. We were able to observe a hard gap with 100% yield across all the six measured devices, pointing to a robust and reproducible fabrication process. Next to this central result, we further demonstrate phase control across a Josephson junction and take advantage of the planar geometry to scale these devices in 2D arrays.

While we focused on the poly-crystalline superconducting PtSiGe compound, we anticipate two strategies to further increase the size of the induced superconducting gap, which sets a relevant energy scale for hybrid devices. Firstly, following the approach in ref. ³³ a superconducting layer with a larger gap, such as Al or Nb, may be deposited on top of the superconducting PtSiGe. Secondly, other ternary superconducting germanosilicides with a higher critical temperature may be explored, starting from the deposition and thermal anneal of other platinoid metals such as Rh and Ir⁶⁰.

Based on our findings, we foresee the following use cases for superconductor-semiconductor hybrids in high mobility planar Ge. Although a hard gap is necessary but not sufficient on its own for achieving a topologically protected system, this work positions planar Ge as a promising platform to explore Majorana bound states in phased-biased Josephson junctions^{13,61,62}. Calculations with experimentally realistic material parameters⁵⁷ show that accessing the topological phase is feasible by careful design of Ge planar Josephson junction geometries that relaxes magnetic field and spin-orbit constraints. More advanced future experiments should build on our current results to fully assess the readiness of Ge for Majorana bound states experiments, such as increasing the induced superconducting gap and measuring it by non local spectroscopy in multi-terminal devices and demonstrate the two-electron charging effect in hybrid Ge/PtSiGe islands, a prerequisite for their use in topological quantum computation.

Crucially, the realization of a hard superconducting gap positions planar Ge as a unique material platform to pursue the coherent coupling of high fidelity spin qubits using crossed

Andreev reflection to enable two-qubit gates over micrometer distances^{5,9}. Remote coupling of spin qubits in Ge may also be achieved by coupling spin qubits via superconducting quantum dots^{5,6}, potentially offering a topological protection¹⁰. Coupling on an even longer distance may be obtained via superconducting resonators⁶³. In such a scenario, a capacitive interaction may suffice, but connecting the resonator to a superconducting ohmic, such as PtSiGe, could result in a larger lever arm and therefore boost the coupling, while a direct tunnel coupling would give further directions to explore. The ability to couple qubits over different length scales is highly relevant and a critical component in network-based quantum computing³⁷.

Furthermore, the demonstration of a hard gap in Ge motivates the investigation of alternative spin qubits systems, such as Andreev spin qubits (ASQ)^{64,65}, that may be coupled with gatemons⁶⁶ or superconductors⁶⁷. Similar to semiconductor spin qubits, the use of isotopically purified Ge²³ may overcome the strong decoherence from the nuclear environment currently limiting progress with ASQs in III-V materials^{3,66}.

All together, these findings represent a major step in the Ge quantum information route, aiming to co-integrate spin, superconducting, and topological systems for scalable and high-fidelity quantum information processing on a silicon wafer.

Methods

Ge/SiGe heterostructure growth. The Ge/SiGe heterostructure of this study is grown on a 100-mm n-type Si(001) substrate using an Epsilon 2000 (ASMI) reduced pressure chemical vapor deposition reactor. The layer sequence comprises a Si_{0.2}Ge_{0.8} virtual substrate obtained by reverse grading, a 16 nm thick Ge quantum well, a 22 nm-thick Si_{0.2}Ge_{0.8} barrier, and a thin sacrificial Si cap³⁵. Detailed electrical characterisation of heterostructure field effect transistors from these heterostructures are presented in ref. ³⁵.

Device fabrication. The fabrication of the devices presented in this paper entails the following steps. Wet etching of the sacrificial Si-cap in buffer oxide etch for 10 s. Deposition of the Pt contacts via e-gun evaporation of 15 nm of Pt at pressure of 3×10^{-6} mbar at the rate of 0.5 Å/s. Rapid thermal anneal of Pt contacts at 400 °C for 15 min in a halogen lamps heated chamber in argon atmosphere. Atomic layer deposition of 10 nm of Al₂O₃ at 300 °C. Deposition of the first gate layer via e-gun evaporation of 3 nm of Ti and 17 nm of Pd. For the devices with a second gate layer the last two steps are repeated, 27 nm of Pd are deposited for the second gate layer to guarantee film continuity where overlapping with first gate layer.

Transport measurements. Electrical transport measurements of the SNS-QPC, NS-QPC, and SQUID devices are carried out in a dry dilution refrigerators at a base temperature of 15 mK, corresponding to an electron temperature of ≈ 25 mK measured with a metallic N-S tunnel junction thermometer. This refrigerator is equipped with a 3-axis vector magnet. Measurements of the junctions array are carried out in a wet dilution refrigerator with base temperature of 50 mK and z-axis magnet.

Measurements are performed using a standard 4-terminals low-frequency lock-in technique at the frequency of 17 Hz. Voltage bias measurements are performed with an excitation voltage $V_{AC} < 4 \mu\text{V}$. By measuring in a four-terminal setup, additional data processing to subtract series resistances of various circuit components is avoided. For the measurements in Fig. 2b–d and Fig. 5b the (maximum) gate voltage is tuned to be just below the threshold for hysteresis, caused by trapped charges in the surface states at the semiconductor/dielectric. In these electrostatic conditions the valence band edge at the semiconductor/dielectric interface and the Fermi level align and the density in the buried channel is expected to approach a saturation density of about $6 \times 10^{11} \text{ cm}^{-2}$ ³⁵.

Simulations and fitting of MARs. The experimentally measured conductance $G_{exp}(V)$ of an SNS junction is assumed to be superposition of N single-mode contributions⁴⁷:

$$G_{theory}(V) = \sum_{i=1}^M N_i G^{(\tau_i, \Delta)}(V) \quad (1)$$

where $G^{(\tau_i, \Delta)}$ is the simulated conductance for the N_i modes with transparency τ_i . We allow for M different transparencies, but all N_i modes have the same superconducting gap Δ . The simulations of conductance were implemented in Python using a modified version of the code presented in ref. ⁶⁸.

The theoretically computed conductance $G_{theory}(V)$ is fitted to $G_{exp}(V)$ using a nonlinear least-squares procedure: $\chi = \int [G_{exp}(V) - G_{theory}(V)]^2 dV$ is minimised

for the fitting parameters Δ , N_i , τ_i with $i \in 1, \dots, M$. The fitting is performed for increasing M, provided that all N_i and τ_i are nonzero. We note that we assume a coherent 1D system. When the MAR contribution is significant, this assumption leads to an overestimation of the sharpness and amplitude of the peaks. Nonetheless, overall we find a good agreement between the data and the model.

Data availability

All data included in this work are openly available at 4TU research data repository <https://doi.org/10.4121/19940174>. All other relevant data are available from the corresponding author upon reasonable request.

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Author contributions

A.S. grew the Ge/SiGe heterostructures. A.T. fabricated the devices. C.N.B., M.B. S.M., J.A. performed transmission electron microscopy characterisation. A.T. with C.B. measured Josephson junction devices, SNS-QPCs, and 2D arrays in wet dilution refrigerators, analysed the data and performed numerical simulation of the MARs processes. V. L. and A.T. measured SNS-QPC, NS-QPC devices and SQUIDs in dry dilution refrigerators and analyzed the data with the supervision of J.W. and input from F.B. and M.V. A.T. wrote the manuscript with input from all authors. G.S. conceived and supervised the project.

Competing interests

The authors declare no competing interests.

Additional information

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