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DOI
10.1109/IWASI.2019.8791334

Publication date
2019

Document Version
Accepted author manuscript

Published in
Proceedings - 2019 8th International Workshop on Advances in Sensors and Interfaces, IWASI 2019

SPINE (SPIN Emulator) - A Quantum-Electronics Interface Simulator

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***Abstract*—A quantum computer comprises a quantum processor and the associated control electronics used to manipulate the qubits at the core of a quantum processor. CMOS circuits placed close to the quantum bits and operating at cryogenic temperatures offer the best solution for the control of millions of qubits. The performance requirements of the electronics are very stringent and its design requires the simultaneous optimization of both the circuits and the quantum system. This paper presents the SPINE (SPIN Emulator) toolset for the co-design and co-optimization of electronic/quantum systems. It comprises a SPICE simulator enhanced with a Verilog-A model based on a Hamiltonian solver emulating the quantum behavior of single-electron spin qubits. A co-design methodology is proposed to derive on the one hand the specifications of the electrical signals to be applied to and captured from the qubits, and to ensure on the other hand, the compliance of the electronics in generating the required signals. This methodology results in an optimized qubit performance while considering practical trade-offs in the control circuits, such as power consumption, complexity and cost as proven by a practical design example.**

***Index Terms*—Quantum computing, spin qubit, Hamiltonian simulation, co-simulation, co-design methodology, classical electronic interface**

I. Introduction

Quantum computing can potentially address problems that cannot be solved on classical computers within a reasonable time [1]. Equivalent to the bits in a classical processor, the fundamental units for quantum computation are the quantum bits (qubits) that must be cooled to deep cryogenic temperatures, so as to exhibit quantum behavior. The generic architecture of large-scale quantum computation is shown in Fig. 1 [2]. The actual quantum processor containing the qubits executing the *quantum circuits*, at the bottom of the stack, is connected to the quantum-to-classical interface consisting of *electronic circuits* for the generation and read-out of signals to and from the qubits. The remaining upper layers, from the microarchitecture up to the algorithm layer, ensure proper algorithm execution by controlling the electronic hardware, similar to a classical computer architecture.

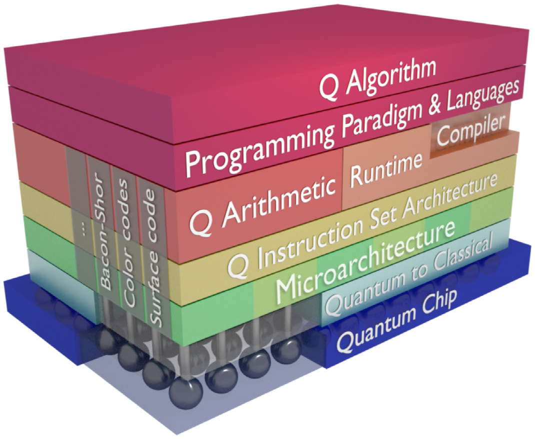


Fig. 1. The layered architecture of a quantum computer (taken from [2]).

State-of-the-art quantum processors contain less than 100 qubits [3]. However, quantum algorithms for new molecule discovery or gene editing would require thousands or even millions of qubits [4]. At such a large scale, it is inconceivable to have the control electronics at any other place than next to the qubits because of cost, size, and wiring complexity.

The electronic interface implemented by CMOS Integrated Circuits (ICs) has to be designed tailor-made for quantum processors. For scaling up to millions of qubits, it is essential that the control electronics is placed physically close to the quantum processor and operate at cryogenic temperatures not higher than 4 K. The power budget of cryogenic electronics is therefore very tightly restricted due to the limited cooling power available in cryogenic refrigerators [5], [6]. CMOS ICs are the only viable alternative that can satisfy the scalability, integration and cost requirements for implementing the control electronics. Thus, a methodology and related tools for the co-design of electronic and quantum systems are of paramount importance [7], [8]. The focus of our work is to develop a toolset and a flow for the co-design and optimization of the electronic interface consisting of transistor-level CMOS circuits interacting with the physical qubits of the quantum circuits.

A plethora of over 100 simulation tools are available in the public domain, such as quantiki [9] and Qiskit [10] for the upper layers in Fig. 1, from the quantum algorithm layer to the quantum instruction set architecture layer [11], and even down to the micro-architecture [2]. A recent publication [12] is the first one to consider the co-simulation of the quantum processor with the “classical control system”. The latter is however only represented at the architectural block-diagram level similar to Simulink [13]. In order to achieve the very restrictive design specification of the electronic interface it is however necessary to co-simulate and co-optimize the transistor-level schematics together with the quantum system.

For the quantum control interface, SPICE circuit simulators, such as Spectre, HSPICE or Eldo, are well-accepted industry standards, and equivalently, for the simulation of quantum systems, Hamiltonian solvers, such as QuTiP [14], are available. However, the actual interface between classical electronics and the quantum processor has mostly remained unexplored and, to the best of the authors’ knowledge, no tool is available that supports both the simulation of classical CMOS electronics and quantum systems.

In this paper, a co-design methodology is proposed, along with a toolset called SPINE (SPIN Emulator) for the co-simulation of the transistor-level ICs and a quantum processor based on single-electron spin qubits. Using this tool, circuit designs can be optimized for qubit performance requirements and an exhaustive verification of the entire quantum computer can be performed.

The paper is organized as follows: Section II introduces the proposed co-design methodology; Section III describes the components of the toolset, simulation of a quantum system and the implementation of SPINE; a design example is presented in Section IV; possible future developments and conclusions are presented in Section V.

II. Co-Design Methodology

The proposed methodology for the co-design of mixed electronic-quantum systems is summarized in Fig. 2. SPINE encompasses a Hamiltonian solver and a SPICE simulator; the toolset used for each step of the design process is specified on the right in Fig. 2. The detailed description of the toolsets is contained in Section III. The design starts by first selecting a qubit technology, such as spin or superconducting, and a high-level control architecture. This is followed by obtaining the specifications for the control and readout signals needed from qubit simulations in order to achieve the desired performance of the quantum processor, see Section IV. Based on the signal specifications, trade-offs can be made between qubit performance and that of the control electronics, such as power and area. An initial block-level architecture can now be defined and an error budget for the different circuit blocks can be assigned. For the chosen control architecture and blocks, further co-optimization of the electronics and the qubits can be performed, such as optimizing the number of qubits that can be frequency multiplexed over a single electronic channel. Finally, the transistor-level circuits and the quantum processor can be fully designed and a circuit-level co-simulation of the entire system can be performed for verification of the final design.

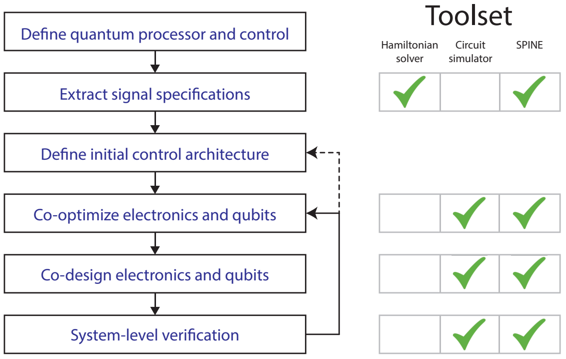

Define quantum processor and control
Extract signal specifications
Define initial control architecture
Co-optimize electronics and qubits
Co-design electronics and qubits
System-level verification
Toolset
Hamiltonian solver
Circuit simulator
SPINE

Fig. 2. Outline of the proposed classical electronic/quantum system co-design methodology along with the tools used in every step.

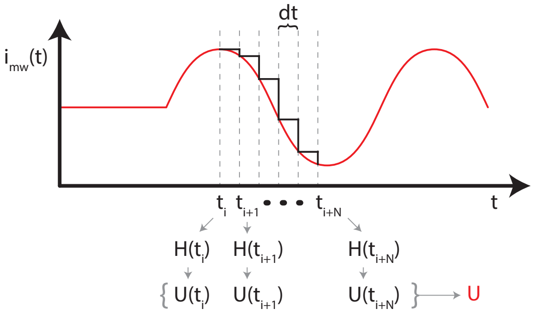


Fig. 3. All signals are considered piecewise constant in a numerical simulation of the quantum physical system.

III. Toolset Implementation

A. Simulation of Quantum Physics

Before diving into the implementation of SPINE, the simulation of quantum systems is reviewed. For a single qubit, the quantum state $|\psi\rangle$ is described as the linear combination of the states $|0\rangle$ and $|1\rangle$, the quantum-mechanical equivalent of the classical states ‘0’ and ‘1’:

$$|\psi\rangle = \alpha_0 \cdot |0\rangle + \alpha_1 \cdot |1\rangle = \begin{bmatrix} \alpha_0 \\ \alpha_1 \end{bmatrix}, \quad (1)$$

where α_0 and α_1 are complex numbers, restricted to $|\alpha_0|^2 + |\alpha_1|^2 = 1$. The quantum state is evolved by multiplication with a unitary matrix U representing the quantum operation:

$$|\psi_{i+1}\rangle = U \cdot |\psi_i\rangle \quad (2)$$

In case of quantum algorithm simulators, U represents one ideal quantum gate, i.e., a simple operation on the qubit, as required for the execution of the quantum algorithm. To find the link between the desired quantum operation (described by U) and the physical behavior of the actual quantum processor, the evolution of the quantum state is found by solving the Schrödinger equation given a Hamiltonian H describing the physical system:

$$i\hbar \cdot \frac{\partial |\psi\rangle}{\partial t} = H \cdot |\psi\rangle, \quad (3)$$

where $\hbar$ is the reduced Planck's constant. In general, the Hamiltonian is time-dependent and is influenced by the classical signals applied to the quantum processor. For instance, for an isolated single-electron spin qubit, under the excitation of a microwave current $i_{mw}(t)$:

$$H = \frac{\hbar}{2} \cdot \begin{bmatrix} -\omega_0 & \alpha \cdot i_{mw}(t) \\ \alpha \cdot i_{mw}(t) & \omega_0 \end{bmatrix}, \tag{4}$$

where α is a constant coefficient that can be determined experimentally, and ω_0 is the precession frequency, i.e., the rotation speed, of the electron spin. Finding the exact solution of the Schrödinger equation for an arbitrary current $i_{mw}(t)$ is not trivial and numerical simulations are used instead. For every simulation time step, the Hamiltonian parameters are considered to be piecewise constant (Fig. 3), and a solution to the Schrödinger equation can be found:

$$U(t_i) = e^{-i/\hbar \cdot H(t_i) \cdot dt}, \tag{5}$$

where $U(t_i)$ is the quantum operation for the Hamiltonian $H(t_i)$ valid at time step t_i for a duration dt. For the time step dt, an oversampling of the signal by a factor of 10 has been found to give accurate results for this system.

The overall quantum operation is then found by combining the results from all N time steps:

$$U = \prod_{n=N}^{0} U(t_n) \tag{6}$$

The process *fidelity*, a measure for how accurate the intended operation U_{ideal} is performed, can be calculated as:

$$F = \frac{1}{n^2} \cdot \left| \mathrm{Tr} \left[U_{ideal}^{\dagger} U \right] \right|^2, \tag{7}$$

where $n = 2^Q$ and Q is the number of qubits simulated.

For a physical system, the states $|0\rangle$ and $|1\rangle$ represent energy levels of the system, e.g., in case of a single-electron spin qubit, the energy level of a spin-down electron ($|\downarrow\rangle$ = $|1\rangle$) or a spin-up electron ($|\uparrow\rangle$ = $|0\rangle$). More energy levels could be required to describe all physical effects. For instance, the interaction between 2 spin qubits is mediated by a higher energy level, i.e. the singlet state [15]. The quantum state is updated to reflect the extra energy levels:

$$\begin{aligned} |\psi\rangle = \alpha_{\uparrow\uparrow} \cdot |\uparrow\uparrow\rangle + \alpha_{\uparrow\downarrow} \cdot |\uparrow\downarrow\rangle + \alpha_{\downarrow\uparrow} \cdot |\downarrow\uparrow\rangle + \alpha_{\downarrow\downarrow} \cdot |\downarrow\downarrow\rangle \\ + \alpha_{20} \cdot |S_{20}\rangle + \alpha_{02} \cdot |S_{02}\rangle \end{aligned} \tag{8}$$

where $|S_{20}\rangle$ and $|S_{02}\rangle$ represent the two possible singlet states and α_i the probability amplitudes. In this case, for the quantum algorithm, the basis used in the quantum computation is $|00\rangle$ = $|\uparrow\uparrow\rangle$, $|01\rangle$ = $|\uparrow\downarrow\rangle$, $|10\rangle$ = $|\downarrow\uparrow\rangle$, $|11\rangle$ = $|\downarrow\downarrow\rangle$. Instead of 4-dimensional vectors and matrices, as would be minimally required for 2 qubits, a simulation of the full 6-dimensional quantum state vectors and a 6×6 Hamiltonian is required [see (8)].

Thus, it is clear that to simulate a system with more energy levels, or more qubits, the size of the vectors and matrices rapidly grows. Together with the many time steps required for an accurate simulation [see (6)], this highlights the challenge of accurately simulating quantum physics.

B. Hamiltonian Simulations

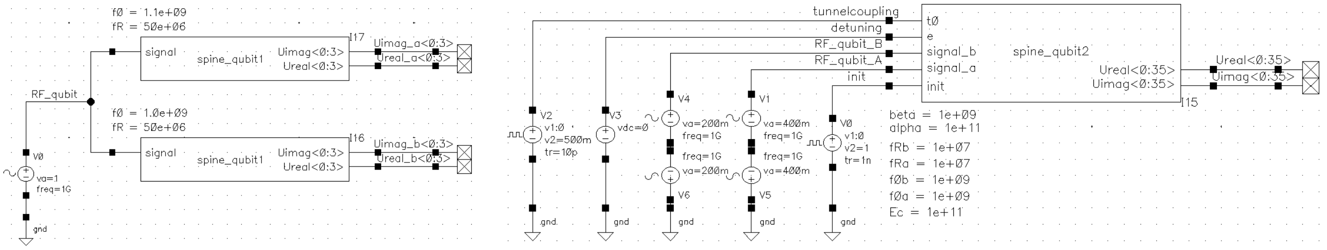
The proposed co-design methodology requires quantum simulations at different steps that do not necessarily entail the co-simulation with the electronic circuit. For such simulations, a generic Hamiltonian simulator based on (2), (5) and (6) can be used, which is also integrated with SPINE as described in Section III-C. In our work Hamiltonian simulations are implemented both in MATLAB and C++. The optimized C++ implementation with and without multi-threading uses the Intel© Math Kernel Library (MKL). The two Hamiltonian simulators were benchmarked on an **N**-qubit system with singlet states included (**N** electrons in **N** quantum dots) with a finite tunnel coupling between each pair of quantum dots. The computation time scales with the size of the Hamiltonian under simulation and increases rapidly with the number of qubits, while at the same time every qubit operation requires thousands of simulation steps. On our workstation, containing an Intel® Core™ i7-4700HQ with 8.0 GB DDR3 RAM, the largest Hamiltonian we were able to simulate was the Hamiltonian of a 7 qubit system. The C++ implementation proved more efficient than MATLAB both in terms of speed, 2-35 times faster depending on the number of qubits, and memory usage, 1 GB vs. 2.5 GB for MATLAB for 7 qubits.

C. SPINE

SPINE was developed for the co-simulation of electronics and quantum physics to observe the interaction of the two. Electrical SPICE circuit simulators perform a quasi-static time-domain solution providing an excellent fit for the inclusion of time-discrete Hamiltonian simulation. Using Cadence Virtuoso as a framework, the quantum physical system is included as a module in the electrical simulation; during co-simulation SPICE provides the control signals for the quantum system as inputs and retrieves the quantum states as outputs, see Fig. 4.

The quantum physical module is implemented in Verilog-A and is treated as a special block of the overall electrical system; like every other component of the system it is reevaluated at each time point and its state is recomputed according to (5) and (6). Different Verilog-A modules are introduced for each type of Hamiltonian as required for a different number of qubits or energy levels. At this time only modules emulating either one single-electron spin qubit (Fig. 4a) or a system of two coupled single-electron spin qubits (Fig. 4b) have been implemented in SPINE, but others can be easily added in the future.

The electrical signals are applied to the input ports of the Verilog-A blocks representing the quantum processor, see Fig. 4; the RF control signal is applied at `signal`, the quantum dots detuning signal is applied at `e`, `t0` is connected to the control signal for tunnel coupling, and `init` is an input signal to reset the operation to the identity matrix. The Verilog-A block `spine_qubit1/2` provides the solution of



(a)

(b)

Fig. 4. The quantum physical system is included as a verilog-A module in the electrical circuit simulator. (a) Two modules, each emulating one single-electron spin qubit, have been instantiated; the two qubits are uncoupled and cannot be entangled. (b) A system of two coupled single-electron spin qubits.

the Schrödinger's equation (Eq. 3) at time t_i resulting in $U(t_i)$, Eq. 5, and ultimately calculates the performed operation, Eq. 6. The resulting complex operation **U**, which can be used to calculate the operation fidelity [(7)], is available at the output with separated real (`Ureal<>`) and imaginary (`Uimag<>`) parts with the matrix flattened to an array. In Fig. 4 are also shown the quantum module parameters, which take their values when this block is instantiated during the simulation: *Ec* is the charging energy of the quantum dot, *f0* the spin precession frequency, *fR* the rotation frequency at a 1-V RF-signal, *beta* the tunnel coupling at 1 V and *alpha* the detuning energy at 1 V.

The electrical-quantum system can be simulated very accurately due to the variable time-step control mechanism of SPICE, which allows it to be set by both the activity in the electrical circuit and the quantum time constants.

IV. SPINE Design Applications

A. Control Signal Fidelity and Power Minimization

As mentioned before, a major concern in scaling quantum computers is the power consumption required by the control electronics. A reduction of the power consumption can be obtained at the cost of quality of the signal being generated for qubit control, or more errors during qubit read-out. The latter is less desirable as it leads to a considerably more complex error-correcting circuitry leading to increased power. In order to address the quality of controlling waveforms, quantum simulations considering signal non-idealities are required to assess the minimum signal quality that can ensure a tolerable error rate in the quantum processor.

As an example, we consider the control signal required to perform a single-qubit operation for single-electron spin qubits [Hamiltonian in (4)]. A microwave control signal $i_{mw}(t)$ as shown in Fig. 5 must be generated, which can display several signal non-idealities (as shown in Table I) that reduce the qubit operation fidelity. Once the effect of each of these errors on the qubit fidelity is known, a larger error budget can be allocated in the electrical circuit to the characteristics requiring the most power and more stringent constraints can be put on the others, thereby optimizing the total power consumption while ensuring the required overall qubit fidelity.

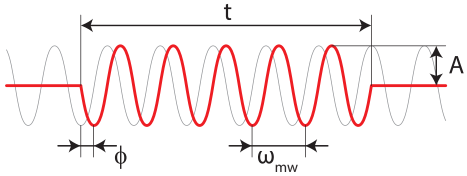


Fig. 5. Shown in red is the typical control signal required for performing a single-qubit operation; the microwave signal has a rectangular envelope of duration t. The grey line indicates the phase of the electron spin.

TABLE I
Error sources for a microwave pulse for a single-qubit operation (assuming a rectangular envelope), and the maximum inaccuracy or amount of noise tolerable for achieving a 99.9 % fidelity on performing a π-rotation in 50 ns considering only one of these error sources is present.

Contributor	Symbol	Error source	Max. tolerable
Microwave Frequency	ω_{mw}	Inaccuracy	0.3 MHz
		Noise	
Microwave Phase	ϕ	Inaccuracy	1.8 deg
		Noise	
Microwave Amplitude	A	Inaccuracy	2 %
		Noise	
Microwave Duration	t	Inaccuracy	1 ns
		Noise	

We consider as an example the effect of inaccuracies on the microwave amplitude. First, simulations of the quantum system were performed for control signals with different levels of amplitude errors on an otherwise ideal signal, as shown in Fig. 7. From this plot, the required signal specifications can be derived when the tolerable qubit admissible error is known. For specific cases, these requirements can also be derived analytically [16], [17]. As an example, Table I also reports the maximum inaccuracy or amount of noise tolerable for achieving a 99.9 % fidelity on performing a π-rotation in 50 ns considering only one of these error sources is present.

Based on the signal specifications found using these initial simulations and a proper budgeting of the various errors, control circuits can be designed meeting the desired requirements and can be validated using a co-simulation of the electronics and quantum system.

It can be seen that if a fidelity $>$ 99.9 % is desired, the amplitude should be accurate to within 2 %. A simple

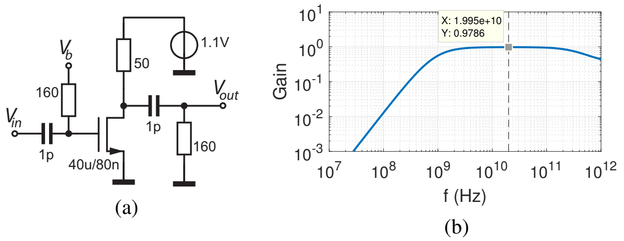


Fig. 6. (a) An example output driver circuit. (b) The simulated gain versus frequency.

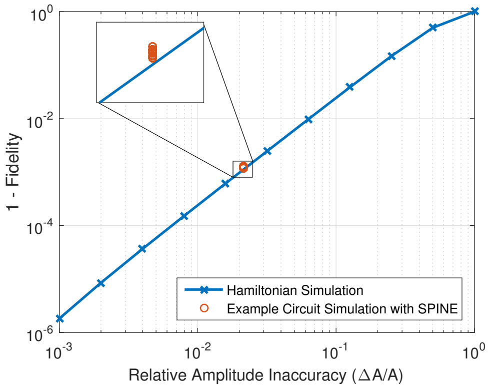


Fig. 7. The simulated fidelity for one of the sources of inaccuracy in the microwave amplitude. The red circles indicate the different runs of the transient simulation of the driver circuit with noise.

driver for applying the RF-signal to the quantum processor, as depicted in Fig.6a, has been designed in a standard CMOS technology targeting this accuracy. From the simulation result in Fig. 6b, it is clear that the gain has the required accuracy at the qubit frequency of 20 GHz. A co-simulation of this driver circuit and the quantum processor with SPINE directly shows that this driver will give the required fidelity of 99.9 % (Fig. 7).

Additionally, the effect of various non-idealities in the electrical circuit, such as process variation, mismatch and electrical noise, can be simulated directly with the quantum processor. As an example, multiple transient simulations with different realizations of electrical noise were performed, giving rise to the various circles shown in Fig. 7. As the noise does not degrade the fidelity significantly, and the circuit has sufficient bandwidth (Fig. 6b), the bias current in the transistor can be safely reduced to minimize the circuit's power consumption while delivering the required control signal fidelity.

B. System Level Verification

To show the power of the proposed toolset for the verification of the quantum computer, a full system containing a controller targeting multiple qubits is simulated. Again, a fidelity of 99.9% is targeted while performing a π-rotation in 50 ns (Table I). Fig. 8 shows the system under consideration, containing a high-level description of the quantum computer's controller, Verilog-A models of the digital-to-analog converters (DACs) and an analog mixer circuit at transistor-level integrated together with SPINE. In this design, the mixer is expected to be the main factor limiting the fidelity, and as such will be simulated in great detail using its full analog schematic.

The performance was verified by simulating a small quantum algorithm executed by the controller and consisting of 4 gates: a π-rotation around the X-axis in 50 ns followed by three additional $\pi/2$-rotations in 25 ns around the X- and Y-axis, see Fig. 9. It can be seen that in response to the controller, the DACs generate the required in-phase and quadrature-phase signals for the mixer, and the analog mixer circuit performs the required upconversion. In response to the generated RF-signal V_{out}, the qubit performs the expected rotations as evident from the simulated spin-up probability, finally achieving a 99.98% chance of success meeting the required system performance.

V. Conclusion

The implementation of a scalable quantum computer with tens to hundreds of thousands of qubits will be achievable only if the control electronics is placed closely to the quantum processors core at cryogenic temperatures. The electronics and its interface for quantum processors need to be designed in conjunction with the physical qubits. Co-design of the classical electronics and the quantum processor is essential to obtain a full system that meets the required performance under practical constraints, such as cost, size, power and reliability.

SPINE, a design tool and methodology have been introduced in this paper and its usefulness to practical electronics/quantum interface simulation, verification and validation have been exemplified. The integration within the Cadence Virtuoso environment via Verilog-A enables the synchronous simulation of the electronic circuitry with the physical quantum components. The proposed methodology was applied to the design of cryogenic CMOS ICs constituting the key elements of the control signal generation and receiver chain [18]. The toolset is essential in the current design of a complete set of ICs for the control and readout of spin qubits.

Future developments of SPINE are envisaged to extend to superconducting qubits and simulations of larger sets of qubits, which are very time-consuming, by taking better advantage of parallel architectures and faster algorithms.

Acknowledgment

The authors would like to thank Intel Corp. for funding.

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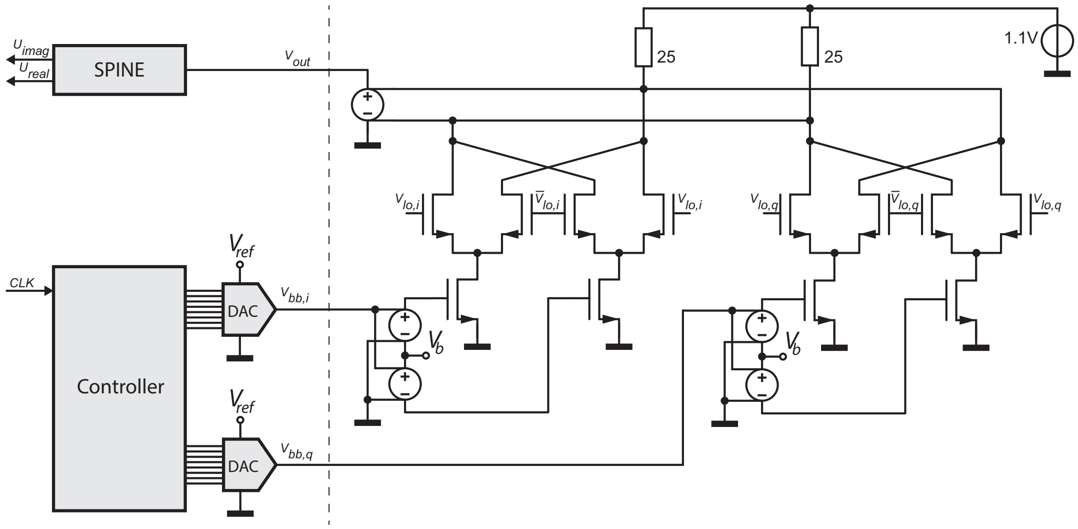

Fig. 8. Schematic of a full system, containing a high-level description of the controller, Verilog models for the DACs, an analog mixer circuit and finally SPINE.

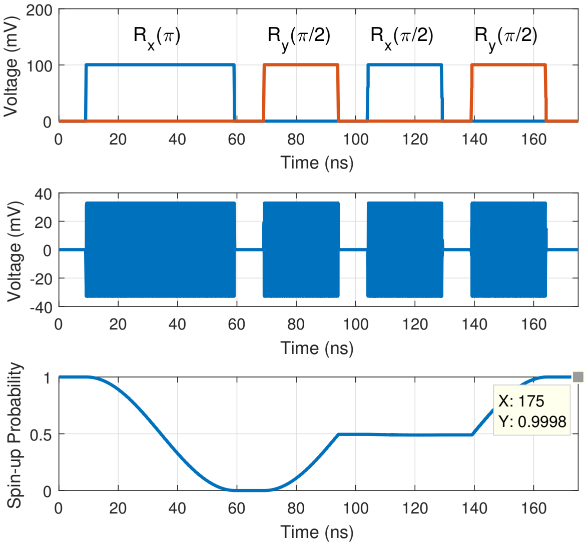

Fig. 9. Result of the full system simulation, from top to bottom: the voltage at the output of the DACs, the I- and Q-signals, driving the mixer, along with a description of the quantum gate; the voltage at the output of the mixer, driving the qubit; and finally the qubit spin-up probability assuming the qubit was initialized to spin-up.

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