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A 121.4-dB DR Capacitively Coupled Chopper Class-D Audio Amplifier

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***Abstract*— This article presents a class-D amplifier (CDA) with high dynamic range (DR). To eliminate the typically dominant noise contribution of a resistive feedback network, the input and feedback signals are chopped and applied to a capacitive feedback network. However, this leads to high-voltage (HV) transients at the input of the loop filter, which, due to timing and impedance mismatch in the chopped feedback network, could degrade linearity and even overstress low-voltage (LV) core devices. Robust processing of the HV chopped feedback signal is guaranteed with chopper timing skew correction, chopper impedance matching, and deadbanding. The prototype, implemented in a 180-nm bipolar-CMOS-DMOS (BCD) process, achieves 121.4 dB of DR, 5.9 dB higher than state-of-the-art closed-loop CDAs, and 8-μV_{RMS} output-referred noise (A-weighted). It also achieves a peak total harmonic distortion (THD) + N of −109.8 dB and a peak efficiency of 93%/88% while driving 15 W/26 W into an 8-/4-Ω load.**

***Index Terms*— Audio power amplifier, capacitively coupled chopper amplifier, class-D amplifier (CDA), dynamic range (DR), noise.**

I. Introduction

CLASS-D amplifiers' (CDAs) ability to achieve high power efficiency has led to their wide adoption in audio applications. In high-end applications, audio digital-to-analog converters (DACs) with a dynamic range (DR) of above 130 dB are commercially available [1], [2], [3], [4], matching that of the human ear. However, the DR of typical monolithic class-D audio amplifiers is much lower, only around 110 dB for analog-input designs [5], [6], [7], [8], [9], [10] and up to about 115 dB for digital-input designs [11], [12], [13], [14].

In [15], a CDA with 120 dB of DR is reported. It employs an open-loop architecture, in which a digital input is first delta-sigma-modulated and then directly used to control the duty cycle of an output stage. As such, its noise performance is limited by supply noise and clock jitter, as shown in Fig. 1(a). To achieve the reported 120-dB DR, an integrated clock jitter of less than 2 ps (rms) is required [15], which increases the system's cost. The open-loop architecture also leads to significant distortion at high power levels and to poor power supply rejection. In [16], the supply voltage is adaptively reduced at low power levels to reduce jitter sensitivity, while feedback is employed at high power levels to reduce distortion and improve supply rejection. However, the additional dc–dc converter required for supply scaling reduces power efficiency, whereas the amplitude-dependent use of resistive feedback causes significant noise floor modulation.

Most CDAs employ a closed-loop architecture to suppress output stage distortion and improve their immunity to supply noise and clock jitter. In this case, their noise floor is typically limited by the thermal noise generated by the resistors that set the CDA's closed-loop gain (or by the resistive or current DAC in a digital-input architecture) and by the amplifier in the first stage of the loop filter, as shown in Fig. 1(b). The contribution of the latter is usually low since a well-designed active-*RC* integrator typically satisfies $g_m R_{IN} \gg 1$, where R_{IN} is the integrator's input resistance and g_m is the amplifier's transconductance [17]. Furthermore, in addition to the resistor's thermal noise, the amplifier's $1/f$ noise is also often significant. However, reducing resistor noise is more difficult, as this comes at the expense of reducing the CDA's input impedance and increasing the power consumed in its feedback network, especially for high-voltage (HV) CDAs.

For low-noise closed-loop amplification, the capacitively coupled chopper amplifier is a good choice [18], [19], [20]. Its capacitive feedback network does not contribute any noise, nor does it consume static power. This enables high energy efficiency, making it popular in biomedical and instrumentation applications. The amplifier's $1/f$ noise is mitigated by chopping, making its thermal noise the dominant contributor [see Fig. 1(c)].

This work presents a capacitively coupled chopper CDA that achieves 121.4-dB DR [21]. Unlike conventional chopper amplifiers, which process small input and output signals [18], [19] or are used in discrete-time switched-capacitor circuits [20], the proposed audio amplifier must process large continuous-time signals at both its low-voltage (LV) input (±1.8 V) and HV output (±14.4 V). Since the loop filter of the CDA operates in the LV domain, the HV transients coupled into the loop filter via a capacitive feedback network will degrade loop filter linearity and may even damage thin-oxide core devices. To prevent this, a feedback-after-*LC* architecture is used to remove HV edges in the CDA output, while the timing and impedance of the switches in the chopped feedback

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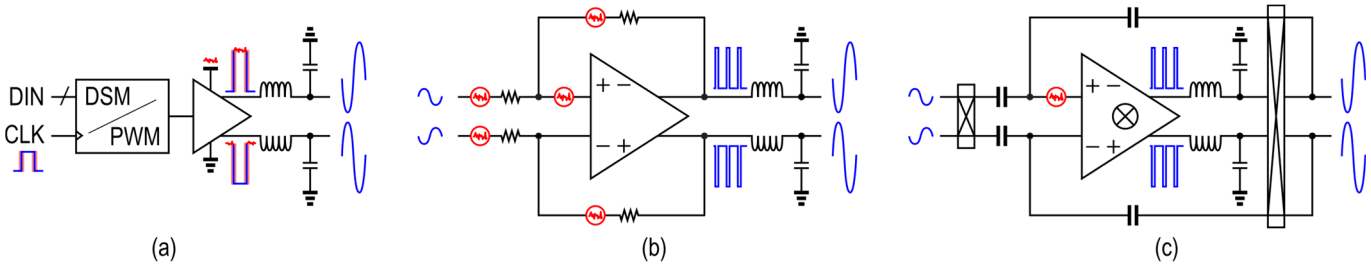


Fig. 1. Major noise sources in different CDA architectures: (a) open-loop, (b) closed-loop with resistive feedback, and (c) proposed closed-loop with capacitive feedback.

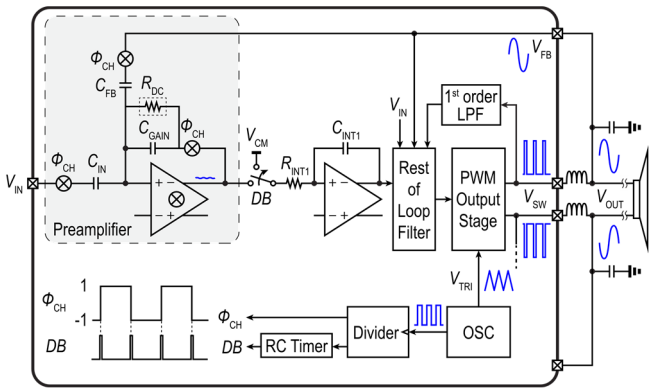


Fig. 2. Architecture of the proposed capacitively coupled CDA.

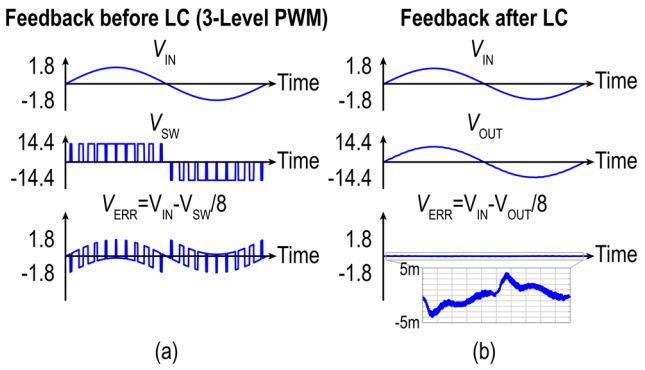


Fig. 3. Error signal waveform for (a) feedback-before-*LC* and (b) feedback-after-*LC* CDAs. The closed-loop gain is 8 with a ±1.8-V differential input swing.

network have been carefully optimized. Residual chopping glitches are blocked by a deadband, so high CDA linearity is maintained.

The rest of this article is organized as follows. Section II introduces the capacitively coupled chopper CDA architecture. Section III describes the circuit implementation and mitigation techniques to overcome HV transients. Section IV presents the measurement results, and Section V concludes this article.

II. Capacitively Coupled Chopper CDA Architecture

A. Overview

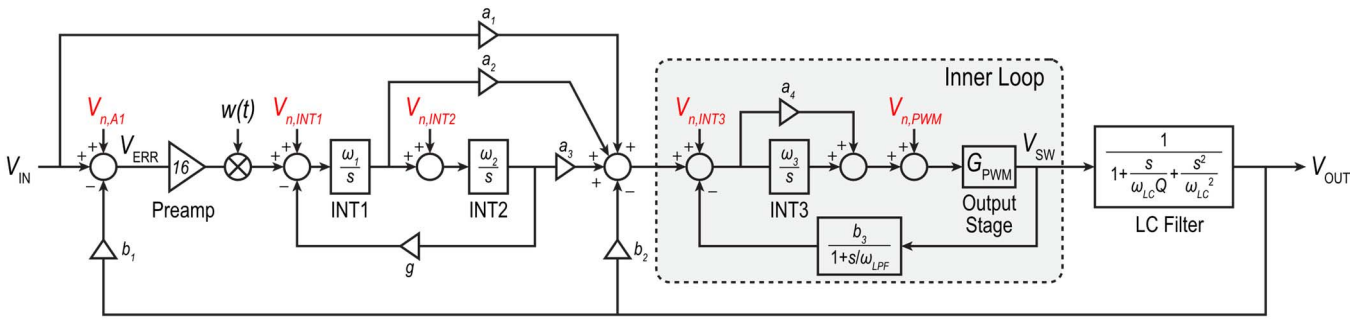
To achieve low noise, this work employs a capacitively coupled preamplifier in the loop filter [22]. Fig. 2 shows an overview of the proposed capacitively coupled chopper CDA. The ratio between the input capacitor C_{IN} and the global feedback capacitor C_{FB} sets an overall closed-loop gain of 8. The preamplifier itself has a gain of 16×, which suppresses the noise contribution of the noisy active-*RC* integrators that comprise the succeeding stages of the loop. The output stage employs three-level fixed-frequency pulsewidth modulation (PWM) with a switching frequency $f_{SW} = 4.2$ MHz and a 14.4-V supply [23].

Incorporating the *LC* into the feedback loop [7], [12], [24] is necessary for the proposed capacitive feedback scheme.[1] Since the output stage generates [6], [8], [9], [10], [11] high-frequency switching signals at V_{SW}, taking feedback from these nodes would result in a residual error signal ($V_{IN} - V_{OUT}/8$) that would saturate A_1, as shown in Fig. 3(a). In contrast, due to the *LC* filter's suppression of the high-frequency components, the error signal is now in the order of millivolts [see Fig. 3(b)]. To mitigate $1/f$ noise, the input stage of A_1 is chopped. Beneficially, chopping also allows the use of a much smaller resistance to set the dc bias at A_1's virtual ground (R_{dc} in Fig. 2), which is more robust to leakage, especially under process and temperature variations. This is because the value of R_{dc} would have to be much larger to push the preamplifier's high-pass corner below 20 Hz, instead of below f_{CH} in the case of chopping. Furthermore, chopping relaxes the matching constraint on C_{FB} and C_{IN} pairs, thereby improving the common-mode rejection of the preamp and, therefore, power supply rejection ratio (PSRR) of the CDA [26].

However, chopping inevitably also introduces nonlinear glitches due to the large-signal nonlinearity of chopper switches and the amplifier, limiting the total harmonic distortion (THD) of conventional capacitively coupled amplifiers (e.g., to −76 dB in [19]). In signal acquisition applications, the subsequent ADC's sampling time can be carefully chosen to avoid the chopping glitches [18], [20]. This is not possible in an audio amplifier. Therefore, a deadband switch is introduced at the output of A_1 to prevent these glitches and the corresponding settling transients of the preamplifier from introducing distortion.

Chopping is performed at $f_{CH} = 200$ kHz, an odd subharmonic of f_{SW}, to avoid the chopping-induced intermodulation distortion (IMD) [27] due to PWM sidebands around f_{SW} [26].

[1]The *LC* filter is required anyway for applications with high output power (>10 W) or when the speaker cable is longer than a few tens of centimeters, to suppress the electromagnetic interference (EMI) generated by the CDA's output stage [25].



a_1	a_2	a_3	a_4	b_1	b_2	b_3	g	G_{PWM}	ω_1	ω_2	ω_3	ω_{LC}	ω_{LPF}
1.1875	0.0156	0.0625	21.333	0.1250	0.1250	0.0234	0.0294	28	2.38 Mrad/s	1.49 krad/s	10.5 Mrad/s	503 krad/s	490 krad/s

Fig. 4. Simplified block diagram of the proposed CDA.

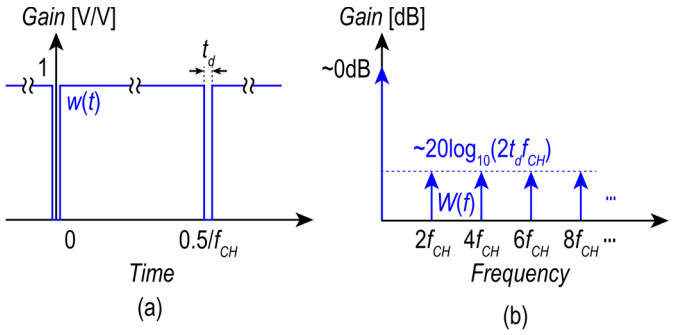


Fig. 5. (a) Time-domain waveform the periodic deadband window $w(t)$ and (b) first few terms of its frequency-domain representation $W(f)$.

A lower chopping frequency would require a lower $1/f$ corner for A_1, increasing its input capacitance, and thus its area and power, whereas a higher chopping frequency increases IMD due to PWM sidebands around even multiples of f_{SW} and the deadband's noise folding gain. These considerations will be analyzed in Section II-B.

Fig. 4 shows the block diagram corresponding to the proposed CDA. The deadband is modeled as a multiplication by a periodic window $w(t)$. The LC filter's 180° phase shift is addressed with a lead compensator, implemented using an inner loop that feeds back the switching node V_{SW} through a first-order low-pass filter [7]. The outer loop consists of the preamplifier and a resonator, and the latter built with two integrators and local feedback to place their two poles optimally in the audio band for maximal loop gain.

B. Noise

The main sources of thermal noise in the proposed CDA are also shown in Fig. 4. Due to the 16× gain from the preamplifier, audio band noise from later loop filter stages is suppressed by 24 dB, and therefore, the CDA's in-band noise floor is mainly determined by the preamplifier. However, the noise of the later stages is not sufficiently suppressed at high frequencies, and periodic windowing introduced by the deadband partially folds the wideband thermal noise at the preamplifier's output to the audio band. These will be analyzed in the following.

As shown in Fig. 5(a), the deadband window can be expressed as

$$w(t;t_d,T)\overset{\text{def}}{=}\begin{cases}0, & |t|<\dfrac{t_d}{2}\\ 1, & \dfrac{t_d}{2}\le|t|<\dfrac{T-t_d}{2}\\ w(t-kT), & \text{otherwise}\end{cases}\tag{1}$$

where t_d is the deadband's duration, T is its period (equal to $0.5/f_{\text{CH}}$), and k is a nonzero integer. The Fourier transform of $w(t)$ is given by

$$W(f)=\left[\underbrace{\left(1-\frac{t_d}{T}\right)}_{a_0}+\sum_{\substack{n=-\infty\\ n\neq 0}}^{\infty}\underbrace{-\frac{t_d}{T}\text{sinc}\left(\frac{n\pi t_d}{T}\right)}_{a_n}\right]\delta\left(f-\frac{n}{T}\right)\tag{2}$$

whose first few terms are sketched in Fig. 5(b).

According to (2), the deadband marginally attenuates in-band noise by a factor of a_0 but folds frequency components around even multiples of the chopping frequency with a scaling factor of a_n, the magnitude of which is largely determined by the duty cycle of the deadband (t_d/T).

The wideband thermal noise at the preamplifier output includes noise generated by A_1 and the noise present in the feedback signal. Since A_1 is a wideband gain stage, its output noise at different time instants can be assumed uncorrelated. Therefore, the deadband attenuates its noise by a factor of $(1-t_d/T)$, which can be verified by summing over all noise folding terms

$$\begin{aligned}V_{n,A_1,\text{fold}}^2&=\sum_{n=-\infty}^{\infty}|a_n|^2V_{n,A_1}^2=\frac{1}{T}\int_{-T/2}^{T/2}w^2(t)V_{n,A_1}^2\,\text{d}t\\&=\left(1-\frac{t_d}{T}\right)V_{n,A_1}^2.\end{aligned}\tag{3}$$

As long as $t_d \ll T$, the noise folding changes the noise contribution of A_1 by a negligible amount.

On the other hand, the wideband noise present in the feedback signal includes noise contributed by the later stages of the loop filter and the output stage, shaped by their respective

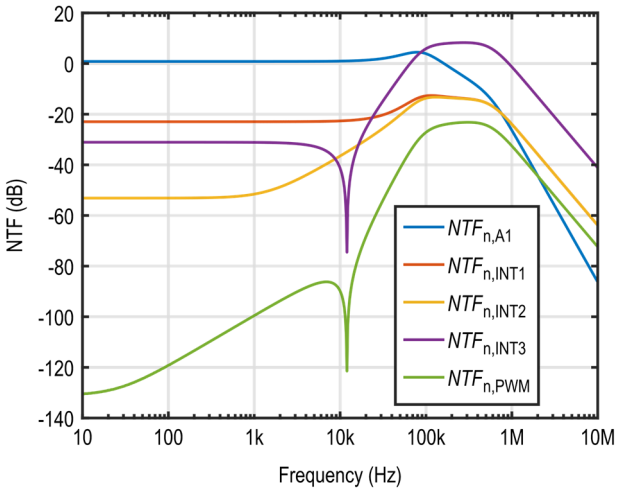


Fig. 6. NTFs (normalized to closed-loop gain) of each noise source highlighted in Fig. 4.

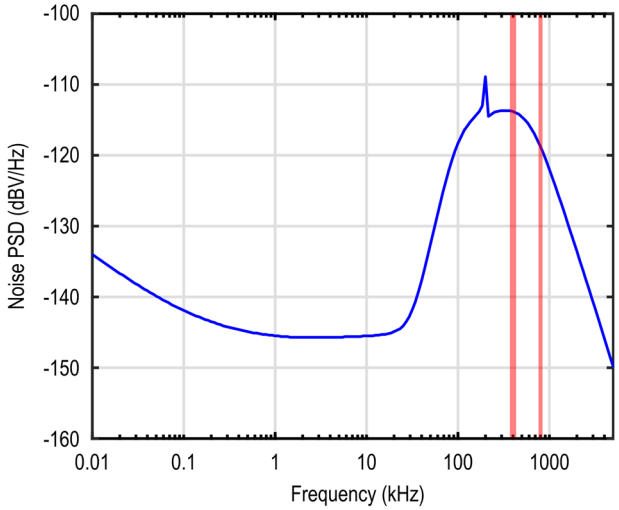


Fig. 7. Simulated noise PSD of the CDA output, with the first two bands subjected to noise folding highlighted.

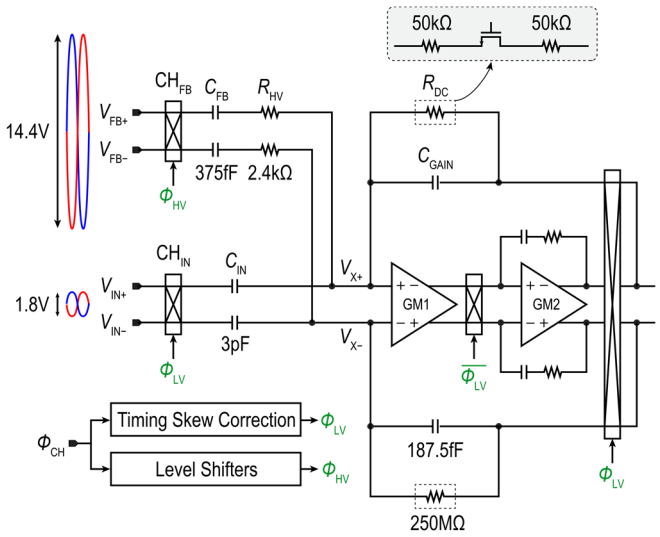


Fig. 8. Schematic of the capacitively coupled chopper preamplifier.

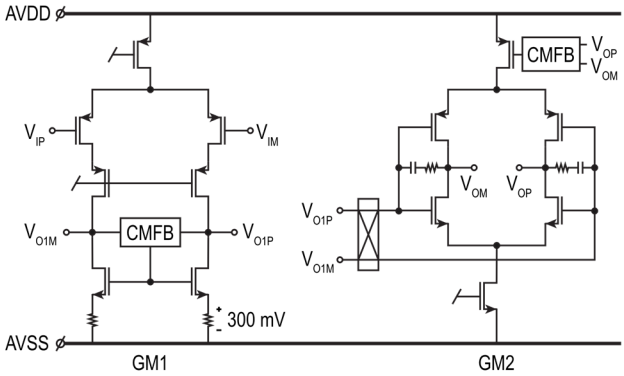


Fig. 9. Circuit implementation of amplifier A_1.

noise transfer functions (NTFs), which are shown in Fig. 6. Except for that from A_1, these sources of noise are suppressed in the audio band by the gain of the preceding stages and eventually roll off beyond the unity-gain frequency of the outer loop. However, between 100 kHz and 1 MHz, they appear at the output with much less attenuation.

Fig. 7 plots the simulated noise spectral density (NSD) at the output, showing the aforementioned out-of-band noise bump. [The residual $1/f$ noise is mostly contributed by the feedback chopper, which is implemented with laterally diffused MOSFET (LDMOS) transistors (Section III-A).] The most significant sources of folded noise are around $2f_{\mathrm{CH}}$ and $4f_{\mathrm{CH}}$, i.e., 400 and 800 kHz, respectively. For these two cases

$$|a_n| \approx \frac{t_d}{T}, \quad n = 1, 2. \tag{4}$$

Reducing the out-of-band noise would require increasing the integrator area as in conventional resistive CDAs. To avoid a significant noise penalty, the deadband's duty cycle is chosen to be 1% ($t_d/T = 0.01$), thus attenuating the folded noise by 40 dB, corresponding to a deadband duration of 25 ns. The preamplifier is designed to settle sufficiently within this duration. For a higher f_{CH}, the reduced NSD of alias bands is compromised by the increase in $|a_n|$.

In addition, the deadband may also fold back the out-of-band quantization noise of the (typically $\Delta\Sigma$) audio DAC that drives the CDA. If the DAC has a white out-of-band noise spectrum, sampling 10% of the frequency range per octave (400 kHz $\pm$ 20 kHz, 800 kHz $\pm$ 20 kHz, and so on) will result in the folding down of approximately -10 dB of the out-of-band noise. For a total out-of-band noise in the order of -40 dBFS [28], [29] and given the aforementioned 40-dB attenuation of folded noise by the deadband, the additional filtering required to keep the folded input noise below -130 dBFS is about

$$-40 \text{ dBFS} - 40 \text{ dB} - 10 \text{ dB} - (-130 \text{ dBFS}) = 40 \text{ dB}.$$

This can be achieved by a second-order low-pass filter. Alternatively, quantization noise folding may be avoided by co-designing a DAC to operate at a sampling frequency

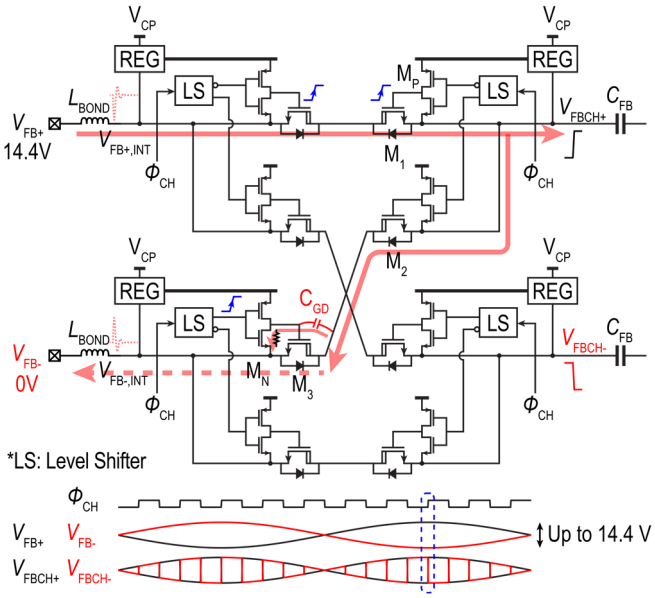


Fig. 10. HV chopper (CH_{FB}) and its switching transient during a chopping transition.

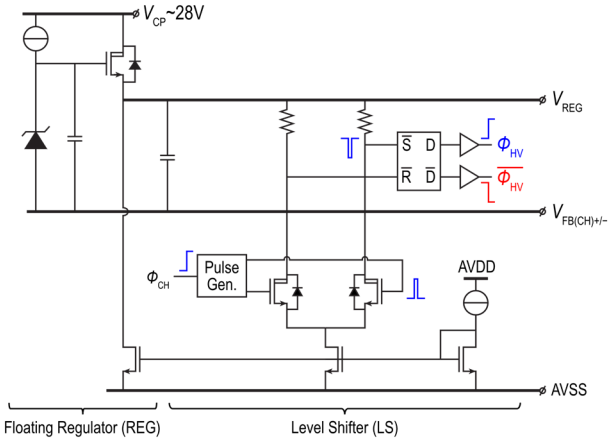


Fig. 11. Schematic of the floating regulator and level shifter [26]. A replica of this circuit is used for timing skew correction.

of $2\,f_{CH}$, which places the alias bands at the nulls of the DAC's output spectrum [22].

III. Circuit Implementation

A. Capacitively Coupled Chopper Preamplifier

Fig. 8 shows a schematic of the capacitively coupled chopper preamplifier.[2] The input capacitance is chosen to be 3 pF to minimize the attenuation by the parasitic capacitance (∼1 pF) at the summing node V_X such that the noise performance is not compromised by the reduced feedback factor due to the parasitics. The Monte Carlo simulation indicates a 1-σ mismatch of 0.12% for C_{FB}. Without chopping, this would limit the typical PSRR to 58 dB.

[2]There was a typo in the callout for R_{dc} in Fig. 2 of the conference paper [21], which had the resistor in the middle of two nMOS switches. This is corrected in Fig. 8 of this article.

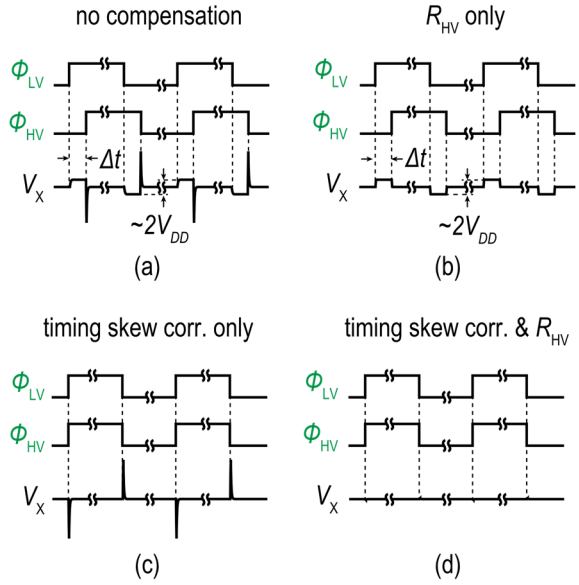


Fig. 12. Chopper clock and virtual ground waveform with (a) no timing skew and impedance compensation, (b) impedance compensation only, (c) timing skew correction only, and (d) both timing skew correction and impedance compensation.

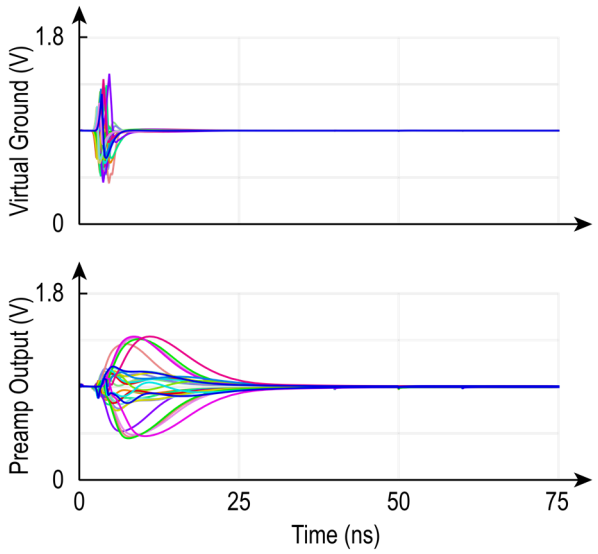


Fig. 13. Transient waveform at the virtual ground and output of the preamplifier during a chopping transition.

The dc bias at V_X is set by a duty-cycled resistor R_{dc} implementing an equivalent resistance of 250 MΩ [22], [30], which ensures a flat gain response around $f_{CH} \pm 20$ kHz. In a CDA, temperature fluctuations can be significant and signal-dependent due to the thermal dissipation of the output stage. Therefore, a duty-cycled resistor is chosen over a pseudoresistor for its robustness under temperature variations. The periodic switching of this resistor also introduces some noise folding and IMD, but they are insignificant since the duty cycle (∼0.04%) is much smaller than the deadband's one.

The preamplifier is built around a two-stage Miller-compensated opamp, as shown in Fig. 9. The input stage

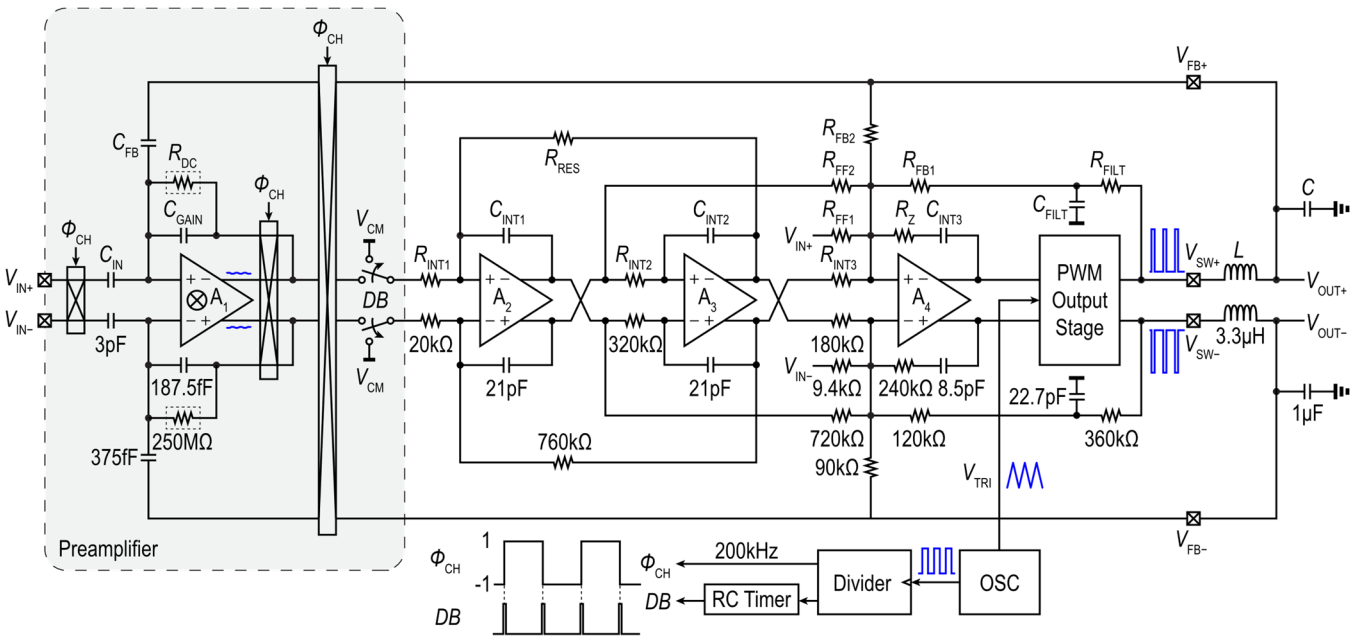


Fig. 14. Top-level schematic of the proposed capacitively coupled CDA.

employs a pMOS input pair that achieves a $1/f$ noise corner of about 50 kHz with an input capacitance of around 1 pF, to keep its $1/f$ noise contribution below 10%. Its nMOS load is heavily degenerated to reduce its noise contribution.

The input chopper (CH_{IN}) is implemented with conventional bootstrapped switches for high linearity. The feedback chopper (CH_{FB}) is also bootstrapped and employs back-to-back LDMOS switches to handle the output up to 14.4 V [26], as shown in Fig. 10. Level shifters (see Fig. 11) are required to control the switches in the HV chopper, which adds delay and offsets the switching instants of the two choppers. In this capacitively coupled CDA, the timing skew can cause the voltage across the virtual ground to temporarily exceed the supply range by up to two times (ignoring parasitic loading at V_X), as shown in Fig. 12(a) and (b). A replica-based timing skew correction circuit is employed to reduce the timing skew from more than 3 ns to be within 200 ps [26].

The ON-resistance mismatch of the two choppers can also cause large transients at V_X, which is exacerbated by the need to upsize CH_{FB} to mitigate the large $1/f$ noise of LDMOS transistors [see Fig. 12(a) and (c)]. The gate length is fixed for n-channel LDMOS transistors in this process, so their width must be increased. According to simulations, an ON-resistance of about 10 Ω for each set of back-to-back switches is required to keep their total $1/f$ noise contribution below 10%. This problem is addressed by adding a series resistance R_{HV} (=2.4 kΩ) to match the resistance ratio of the input and feedback paths to the ratio of their capacitive impedance (1:8), assuming low source impedance (≪300 Ω) at the CDA input. If a source with higher output impedance is used, two external resistors in series with C_{FB} can be employed. Some residual mismatch is acceptable as long as the swing of the residual glitches at V_X, shown in Fig. 12(d), does not lead to oxide damage, and the resulting transient at the output of A_1 settles before the deadband ends. The deadband, nominally 25 ns long, is generated by an *RC* timer, while the same type of component is used in A_1's constant-g_m biasing circuit to ensure settling within the deadband across process, voltage, and temperature (PVT).

In addition, unlike [26], where the HV feedback signal is directly accessible within the chip, the output of this work is fed back from the off-chip *LC* filter. In simulations, cross conduction through CH_{FB}, even only lasting several hundred picoseconds, can create ringing up to several volts across the parasitic inductance from the bondwire, printed circuit board (PCB) trace, and the *LC* filter, adding to the glitches at V_X. The HV chopper transients during a chopping transition are shown in Fig. 10. Cross conduction happens when coupling through C_{GD} pulls up the gate of a transistor that is supposed to be OFF, e.g., transistor M_3 in Fig. 10. This can happen when M_1 is turned on too quickly by its gate pull-up transistor M_P, causing the displacement current through C_{GD} of M_3 to exceed $V_{TH,M_3}/R_{ON,M_N}$, where R_{ON,M_N} is the ON-resistance of the gate pull-down transistor M_N. Hence, the ratio of the pull-up and pull-down strength of the switch drivers for CH_{FB} is resized to 1/7 in this work such that the switches can be kept OFF during such switching events [31].

Fig. 13 shows the simulated waveform at V_X and the output of A_1 under process and temperature variations during a chopping event. The swing at V_X is well within the supply range, while the glitch at the output mostly settles within 25 ns, which is limited by the bandwidth of the preamplifier.

B. Class-D Amplifier

As shown in Fig. 14, the rest of the loop filter stages employ an active-*RC* topology for high linearity. The 2.1-MHz triangle wave required for PWM is generated by a differential

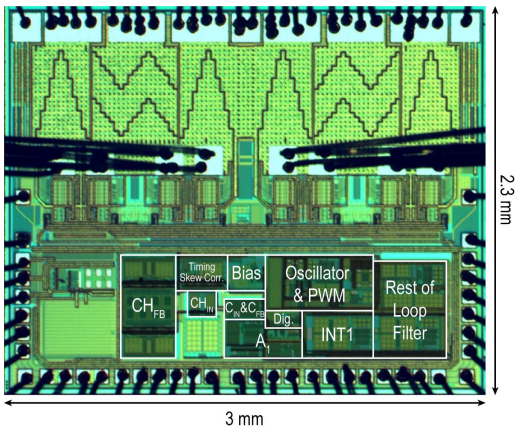


Fig. 15. Die photograph.

oscillator. The output stage employs a three-level topology with constant output common mode for low idle power. Amplifiers A_2–A_4 in the loop filter, the differential oscillator, and the output stage are reused from [23].

The triangle wave's peaks and zero crossings are extracted to create a 4.2-MHz digital clock, which is then divided by 21 to generate a 200-kHz clock with a 50% duty cycle for chopping.

IV. Measurement Results

A prototype of the proposed capacitively coupled CDA is implemented in a 180-nm bipolar-CMOS-DMOS (BCD) process. Fig. 15 shows a photograph of the die, which occupies 7 mm^2. The output stage employs a 14.4-V supply (PVDD), while the rest, including the loop filter, oscillator, and timing, operates from a 1.8-V supply (AVDD). The quiescent current drawn from AVDD is 7 mA, in which the preamplifier draws 1 mA. The HV chopper draws about 1 mA from PVDD. An Audio Precision APx555 Analyzer generates the input and captures the output of the CDA.

Fig. 16(a) shows the measured output spectrum when the CDA delivers 1 W into an 8-Ω load, corresponding to −10 dBFS. In this case, the measured THD + N is −109.6 dB. Fig. 16(b) shows the result for a 4-Ω load at the same output swing, where the THD + N is −109.8 dB.

Fig. 17 shows the output spectrum with a −80-dBFS input, where the measured SNR is 41.4 dB, indicating that the prototype achieves a DR of 121.4 dB. The measured A-weighted integrated output noise is 8 μV_{RMS}.

Fig. 18(a) shows the measured THD + N across output power levels with both 8-Ω load and 4-Ω load. In both cases, the peak THD + N is about −110 dB. The maximum output power (defined at 10% THD) is 15 and 26 W for 8- and 4-Ω loads, respectively. The noise floor, which dominates over distortion at small signal amplitudes, is about 10 dB lower than that contributed by a pair of 20-kΩ resistors, which is common for conventional resistive-feedback CDAs [5], [10]. The THD stays below −100 dB until the point of clipping. Fig. 18(b) plots the measured THD + N across input frequency, which is between −108.8 and −113.5 dB. Fig. 19 shows the spectrum measured from a two-tone test. At an output power

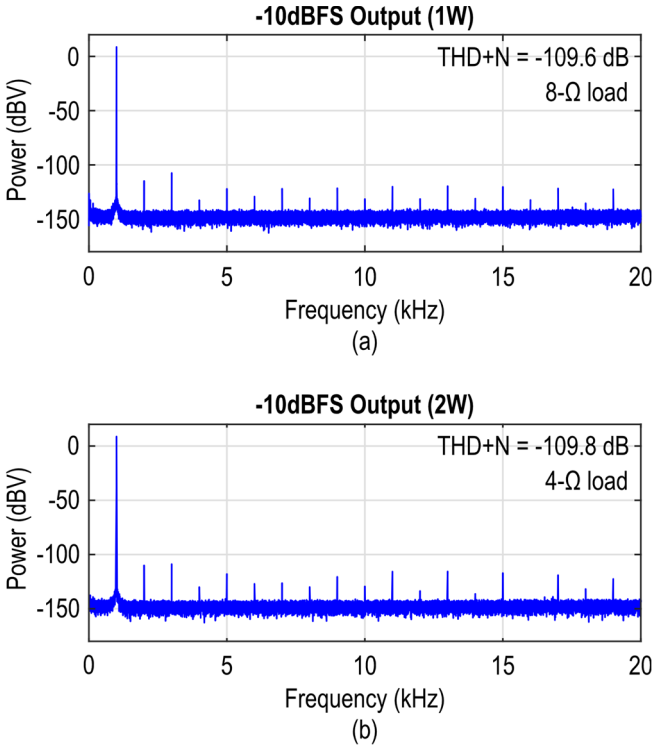


Fig. 16. Measured output spectra at −10 dBFS for (a) 8-Ω load and (b) 4-Ω load.

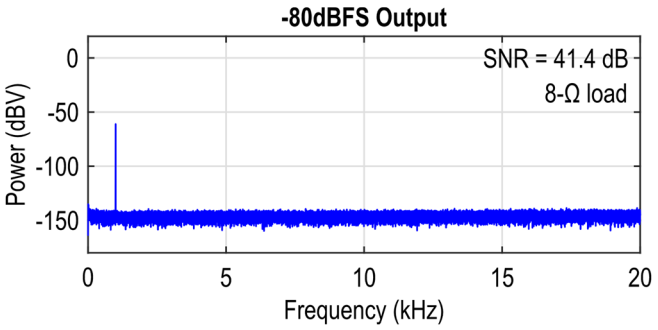


Fig. 17. Measured output spectrum at −80 dBFS.

of 0.5 W, the third-order intermodulation distortion (IM3) is about −110 dB. Fig. 20 shows the measured THD + N and DR for six samples. The peak THD + N varies by less than 1 dB for an 8-Ω load and less than 2 dB for a 4-Ω load. The DR is within 0.5 dB for all samples.

To evaluate the noise folding effect of the deadband, the deadband duration is made programmable. Fig. 21 shows the measured THD + N and DR while varying the deadband duration. When the deadband duration is intentionally reduced, linearity degrades as a portion of the nonlinear chopping glitches propagates down the loop filter. On the other hand, when the deadband is lengthened, the DR degrades due to increased noise folding, as mentioned in Section II-B.

Fig. 22 shows the measured power efficiency. The peak efficiency is 93% and 88% for 8- and 4-Ω loads, respectively.

Fig. 23 plots the PSRR measured from six samples. The worst case PSRR is 89 dB at low frequencies. The degraded

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	TPA3255 [5]	Sun ISSCC'22 [16]	Zhang JSSC'22 [7]	Karmakar JSSC'20 [10]	Cope ISSCC'18 [11]	Schinkel JSSC'17 [12]	Wang JSSC'10 [15]
Process	**180 nm BCD**	-	0.5 µm CMOS	180 nm BCD	180 nm BCD	180 nm BCD	130 nm BCD	65 nm CMOS
Architecture	**Analog-In**	Analog-In	Digital-In	Analog-In	Analog-In	Digital-In	Digital-In	Digital-In
Feedback Network	**Capacitive**	Resistive	Resistive(1)	Resistive	Resistive	Resistive	Resistive	N.A.
Supply (V)	**14.4**	51	0.625~5	14.4	14.4	8~20	14/25	3
R_{LOAD} (Ω)	**8/4**	4	8	8/4	4	8	4	8
$P_{OUT,MAX}$ (W)	**15/26**	315	1.5	12/21	28	20	80	0.4
Efficiency	**93%/88%**	~90%(2)	81	91%/87%	91%	90%	>90%	88
$I_{Q,PVDD}$ / Channel (mA)	**9**	24	2.4	8	17	21	-	2.4
$I_{Q,AVDD}$ / Channel (mA)	**7**	30	-	-	-	-	-	-
THD+N (dB)	**-109.6/-109.8**	-84	-95.4	-107.1/-105.6	-102.2	-97.7	-88.6	-94(2)
DR	**121.4**	113	121	110(3)	109	115.5	115	120
A-wt. Output Noise (μV_{RMS})	**8**	85	3.15	-	31	20	19/34	1.7
PSRR (dB) (Frequency/Hz)	**89~71 (20~20k)**	>65 dB -	100 (217)	-	70~62 (20~20k)	80~50 (20~20k)	90~60** (20~20k)	82 (1k)

(1) Feedback only enabled at high output power
(2) Estimated from graph
(3) SNR number used

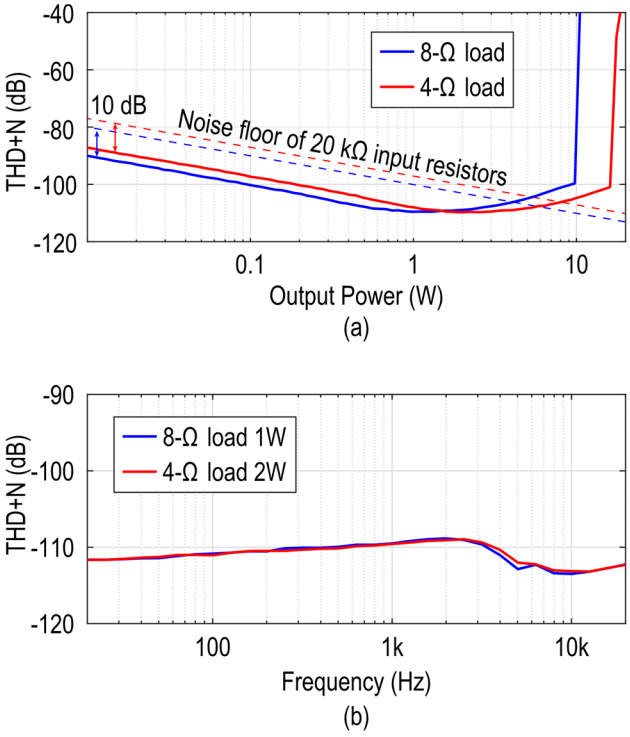


Fig. 18. Measured THD+N across (a) output power and (b) input frequency.

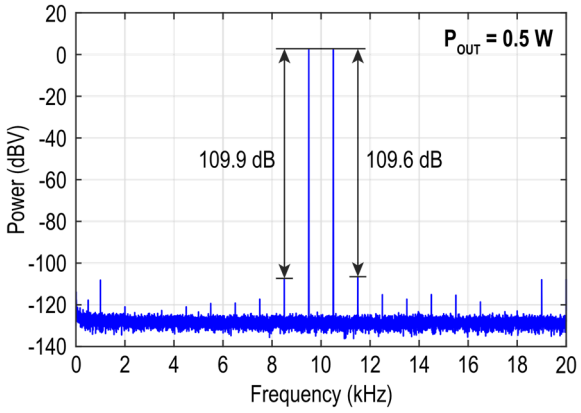


Fig. 19. Measured spectrum from a two-tone test.

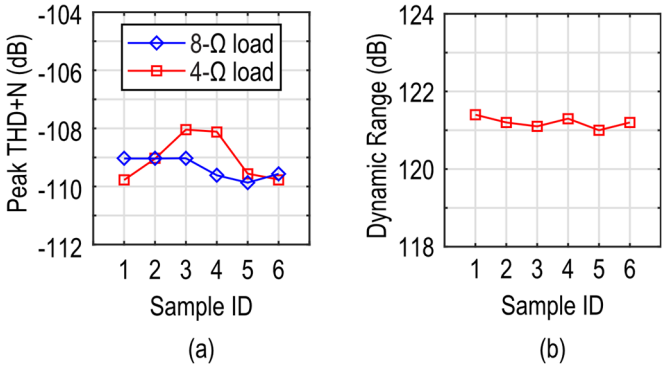


Fig. 20. (a) THD + N and (b) DR for six samples.

PSRR compared to [26] was traced to the mismatch of the near-minimum-width resistor pair R_{FB2} (see Fig. 14). Supply noise thus leaks into the differential signal present at the input of the third integrator, which, in this design, is only suppressed by about 30 dB, as shown in Fig. 6.

Table I summarizes the prototype's performance and compares it with state-of-the-art CDAs, including both analog- and digital-input ones. Due to the capacitively coupled architecture, this work achieves 5.9-dB higher DR, 2.4× lower A-weighted integrated output noise, and 2.5-dB better peak

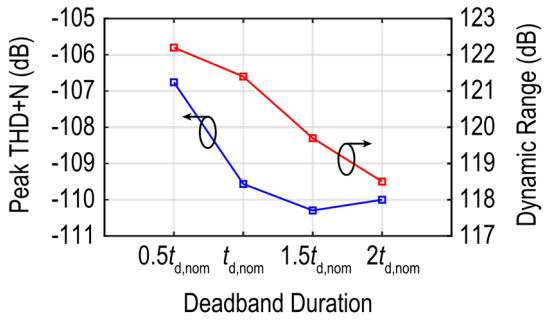


Fig. 21. Peak THD + N (left axis) and DR (right axis) for different deadband settings.

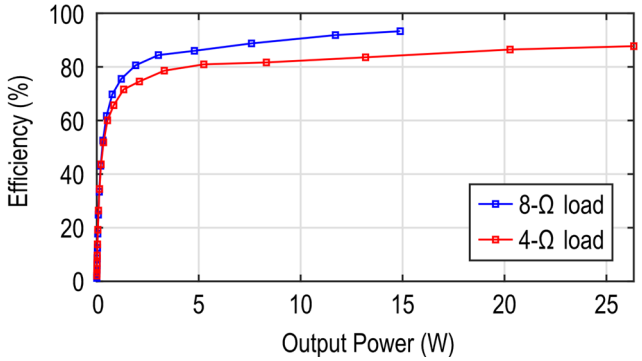


Fig. 22. Measured power efficiency across output power.

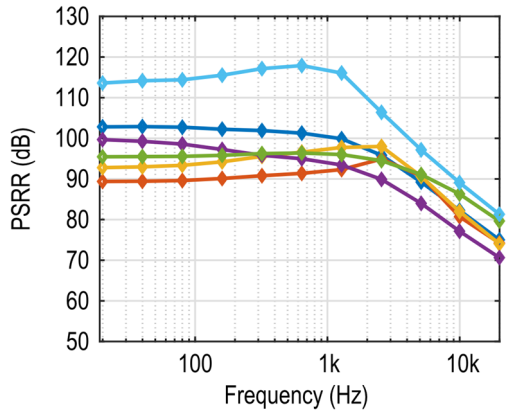


Fig. 23. Measured PSRR across the audio band of six samples.

THD + N. Meanwhile, it achieves competitive efficiency, idle power, and PSRR among HV (>10 V) CDAs.

V. Conclusion

In conclusion, a capacitively coupled chopper Class-D audio amplifier is presented, which enables significant improvement in the DR. To protect thin-oxide devices, HV chopping transients are addressed through timing and impedance matching. Deadbanding is applied to suppress the residual glitches and maintain high linearity. Due to the low-noise capacitively coupled chopper preamplifier in the loop filter, the 180-nm prototype achieves 8 μV_{RMS} of A-weighted integrated noise and 121.4-dB DR.

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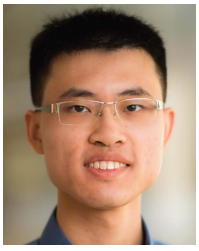

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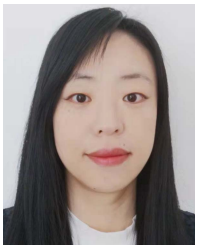

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