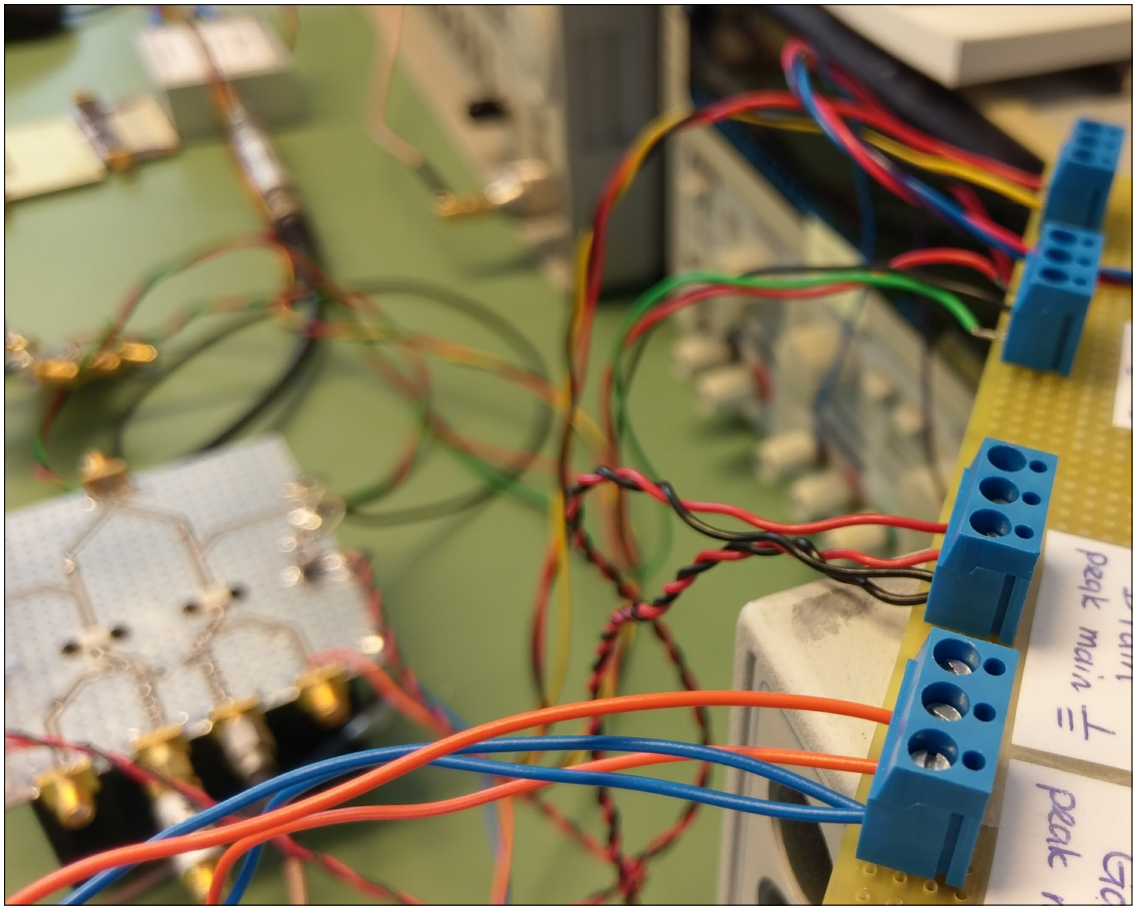
RF Power Amplifier Test System

for Interpolating-supply Power Amplifiers

July 21, 2017

Jun Feng and Alexander Louwerse



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RF Power Amplifier Test System

for Interpolating-supply Power Amplifiers

by

Jun Feng and Alexander Louwerse

to obtain the degree of Bachelor of Science

Supervised by dr. Morteza Alavi and ing. Marco Pelk
Proposed by prof.dr. Leo de Vreede
Department of Microelectronics

Defended before prof.dr. Leo de Vreede (chair), dr. Morteza Alavi
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Bachelor Graduation Thesis
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DELFT UNIVERSITY OF TECHNOLOGY

FACULTY OF ELECTRICAL ENGINEERING, MATHEMATICS
AND COMPUTER SCIENCE

ELECTRICAL ENGINEERING PROGRAMME

Summary

The objective of the bachelor graduation project detailed in this thesis is the development of a system suited for testing radio frequency (RF) power amplifiers (PAs). This PA test system is in particular set up for testing two-transistor interpolating-supply amplifiers.

Interpolating-supply PAs are efficiency-enhanced by employing multiple transistors supplied by different, fixed drain supply voltages, leading to different efficiency characteristics, which are then combined by switching between the transistors, resulting in an enchanced overal efficiciency. Turning on the right amplifying transistor takes place digitally by pre-adjusting the different data inputs or control of gate biases.

The PA test system is required to provide support for measurement and signal generation for 40 dBm output power of a 20 dB gain PA. Moreover, it is required to provide remote control access to the measurement equipment and automation of the tests, implemented in MATLAB.

The to-be-measured PA performance metrics were constrained to static tests for drain efficiency, power-added efficiency, AM/AM distortion, total harmonic distortion (THD) and intermodulation distortion (IMD).

In order to meet the requirements while making use of the available resources, it was recognized that the following subsystems were necessary:

- Baseband signal generation using a DAC;
- RF signal generation using a to-be-calibrated IQ modulator;
- Pre-amplifier, by own design; and
- Spectrum analyzer, controlled remotely.

The baseband signal generation subsystem was characterized with respect to noise and gain performance, which resulted in the making of noise-reducing LC low-pass filters. The provided IQ modulators were successfully calibrated for device non-idealities in an automated MATLAB GUI, allowing for clean RF signal generation. Three pre-amplifiers with over 27.5 dB power gain were realized for sufficient PA input power. A set of MATLAB functions and scripts for the spectrum analyzer and top-level control was written, enabling semi-automatic PA testing.

At the time of writing this thesis, the PA test system was put in use to characterize and evaluate two interpolating supply PAs. For automation, another GUI was implemented for the PA test system. The system proved to be able to determine PA input, output and DC power to measure the gain, linearity and efficiency in multiple static tests and for different PA bias conditions. Also THD and IMD for single-transistor were measured using the PA test system. The results were to a realistic extent similar to the simulated PA characteristics, aside from some anomalies which could possibly be explained by PA design implementation mistakes or test system nonidealities.

Preface and Acknowledgements

In the span of two months, we delved into the world of testing power amplifiers and we present the process and results in this document. With four other ambitious group members also interested in micro-electronics, we developed a proof-of-concept of a novel energy efficiency-enhancement technique for radio frequency (RF) power amplifiers. The subject is very relevant with the foreseen rapid increase of wireless data transfer and global warming.

As the persons responsible for the power amplifier test system, we consider this experience to have been very valuable and satisfactory as it allowed us to work in freedom with the real tools (software *and* hardware) used in RF engineering at the Department of Microelectronics of TU Delft.

We would like express our sincere thanks to our supervisors Morteza Alavi and Marco Pelk, who were great in bringing over knowledge when needed and always had time to help us out.

Secondly, we are grateful to Leo de Vreede for proposing this project and granting us a lot of freedom at the microelectronics department.

We are very thankful to Atef Akhnoukh for his kind help when the secretary or supervisors were not available.

Further, Ioan Lager receives our gratitude for being an excellent organizer of the bachelor graduation process, providing clear and relevant information for guidance.

Also, we thank Bilal Bouazzata, Laurens Buijs, Martijn Hoogelander and Niels van der Kolk for being fantastic friends and project group members. Their skillfulness and autonomous attitude allowed us to focus on the development of our work.

We finally thank our families for supporting us during the past three years of our bachelor Electrical Engineering studies, granting us the opportunity and time to pursue this path. Without them, we could not have been able to complete this graduation project.

Jun Feng and Alexander Louwerse
Delft, July 2017

Contents

1 Introduction

As demand for faster rates of information exchange rises and more devices utilize (complex) wireless communication modulation schemes, as lately seen with the development of 5G network operating in the 28, 39 GHz radio frequency (RF) band and push towards the Internet of Things, the need arises for power amplifiers (PAs) which are highly efficient, to reduce costs and extend battery life, yet also highly linear, to enable complex communication schemes and remain within the designated frequency bands [1].

A potential answer to these needs is an *interpolating-supply PA*, which utilizes multiple, separate transistors. Each transistor has their own fixed supply voltage, which leads to the transistors having a different efficiency from one another. By switching between the transistors depending on the intended envelope output power, a greater overall efficiency can be obtained. However, switching between the transistors has adverse effects on the linearity of the PA, especially when so called "hard-switching" is employed, in which the switching is performed near-instantaneously. The discontinuities associated with the switching causes distortions, amongst which the introduction of harmonics or intermodulation of input tones. Thus employing a smoother transition should decrease the adverse effects on linearity.

1.1 Project Objective

To study the achievable performance when employing an interpolating-supply PA topology, an Electrical Engineering Bachelor Graduation Project was set up. In this project a group of six students were assigned to work on two different interpolating PA designs for 20 dB gain and 40 dBm power output, create working prototypes and construct a testing setup with which to measure the developed PAs.

The six students are divided in teams of two, each of which will be responsible for one part of the overall project. One team worked on a topology that switches between the used transistors by changing the biases applied to the different transistors, detailed in [2]. The second team worked on a topology that switches by diverting the input signal from one transistor to the other, detailed in [3]. The final team developed the RF PA test system addressed in this thesis.

This thesis presents our design process, design considerations and achieved results, concerning the PA test system development for measurement of PA parameters and quantities of interest and generation of the appropriate signals, as to characterize the by the other teams developed PAs.

1.2 PA Test Systems State-of-the-art

While PA test systems are crucial in a PA design cycle, not often are these test systems precisely detailed in design literature with at most one section devoted to test methodology. Nevertheless, a compilation of literature on PA testing and evaluation gives a valuable impression of the PA test system state-of-the-art regarding performance metrics and methodology.

Efficiency and linearity are common PA performance metric used to asses PA designs [4–6]. For data transmission error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) of the (demodulated) PA output are also of interest [7, 8]. In more rare cases, time domain measurements are employed in order to observe the envelope outputted by the PA of interest [9]. The performance metrics allow for comparison of PA realizations based on different classes or topologies [10] and can be used to define more relevant figures-of-merit when combined such as a linearity figure-of-merit based on multiple single-tone measurement to approximate intermodulation (IMD) linearity [11].

Internal measurements of a PA when operational are very interesting while hard to achieve without disturbing the device. [12] and [13] give examples on implementing the possibility of such in-situ measurements in the matching network of the to-be-designed PA. For further time-domain measurements of the waveform, a more involved system using a six-port reflectometer is presented in [14].

PA linearity can also be assessed in analyzing phase (AM/PM) distortion [15], for which often a vector network analyzer (VNA) is used. However, VNAs can be very costly or not readily available. For this reason, novel methods for AM/PM distortion have been developed. For instance, [16] proposes a digital signal processing (DSP) in conjunction with comparison circuitry as an alternative method. Moreover, in [17] a more simple method employing conventional two-tone generators, a spectrum analyzer and data post-processing is presented.

With two-tone inputs, another way to assess PA linearity is to look at IMD products. These products can be especially troubling when the PA frequency operating channel is narrow [18]. As the IMD measurements takes frequently place in the form of basic 3rd-order intercepts points (TOI) determination [18–21], we did not see novel IMD-related PA test setup features.

Finally, in the scope of this project, it is certainly possible that digital pre-distortion (DPD) will be ultimately desired to further enhance interpolating-supply PAs. [22] explains in great detail the impact of measurement imperfections on DPD-enhanced PAs such as analog-to-digital converter (ADC) limitations.

1.3 Thesis Outline

The outline of this thesis is as follows. In Chapter 2 we discuss on the different requirements for the testing system. After which, in Chapter 3, an overview of the entire testing system is provided, including small components and the measurement programme.

In the later chapters the system is discussed in more detail, starting with Chapter 4, which explains the purpose of the different components used to generate the desired base band signals, their limitations and applied solutions to those limitations. Chapter 5 then discusses the purpose of the IQ modulator, its imperfections and how to compensate for them. In Chapter 6 the design and implementation of the pre-amplifier are discussed. After which in Chapter 7 the procedures surrounding the spectrum analyzer are discussed. In Chapter 8 the measurement programme is discussed in more detail.

Then at last the results of the measurements of the PAs are discussed and compared to simulated results in Chapter 9, from which in Chapter 10 conclusions are drawn and finally our recommendations for future work are given.

In the Appendix a list of used hardware can be found.

2 | Programme of Requirements

As detailed in the thesis introduction, Chapter 1, we were assigned to develop a test system for radio frequency (RF) power amplifier (PA) performance evaluation. We developed the test system in particular for a novel PA architecture specified as *interpolating-supply PA*, which involves two or more fixed DC supplies, two or more amplifying transistors and specifically controlled generation of input and/or bias signals to the PA.

The test system is most suited for the professional market, for example for RF engineers who seek to quickly evaluate their realized PA design. In order to assess our test system, we set up a Programme of Requirements (PoR). The PoR consists of functional and non-functional key performance indicators including conditions applying to its development, production and implementation amongst others.

We will use the PoR put forward in the following sections for assessment of the design and results throughout the thesis.

2.1 Functional Requirements

Functional requirements define the purpose of the PA test system and the tasks it is expected to perform. We made a distinction between primary and secondary functional requirements, that is, vital tasks and tasks which can be done if time allows it while not essential. This distinction takes the limited development time and foreseen hands-on time with manufactured PAs into consideration.

Primary Functional Requirements

2.1.1 Power Amplifier Family Compatibility

The PA test system must be at least compatible with testing interpolating-supply PAs utilizing two transistors, providing a sufficient number of applicable bias connections and calibrated input signal paths.

2.1.2 Linearity Measurements

The PA test system must be able to measure the PA degree of linearity. To do this at least three types of static measurements are to be performed:

- *Amplitude modulation (AM/AM);* In order to determine the PA gain variation with respect to its input power.
- *Phase modulation (AM/PM)*; In order to determine the PA phase shift with respect to its input power.
- *Harmonic distortion (THD);* In order to determine how prevalent the higher order components introduced by the PAs are for sigle-tone input signals.
- *Intermodulation (IMD)*; In order to determine how prevalent the higher order components introduced by the PAs are for two-tone input signals.

2.1.3 Efficiency Measurements

The PA system must measure the power efficiency of the PA, in order to see the effect of the design of the PAs on the efficiency and thus be able to compare it with other designs.

2.1.4 Measurement Data Management

The PA test system must show the user the real-time measured data concerning the chosen measurement. The measured data and any post-processed data must be exportable for further usage.

2.1.5 Level of Remote Controllability

The PA test system measurements must be remote controllable from a single computer with sufficient communication connections to the measurement hardware. The user must still be able to manually control, connect and/or disconnect the hardware as desired.

Secondary Functional Requirements

2.1.6 QAM Measurement

A good representation of future use of the designed PAs is the amplification of a signal modulated by Quadrature Amplitude Modulation, as this modulation scheme uses distinct voltage levels to transfer the data. The PAs can than be adjusted to those distinct levels, which should increase the overall efficiency when a QAM-signal is used. For this reason the system should be able to generate and measure simple QAM-signals. However, as this is of lesser importance it should be performed if time allows for it.

2.1.7 Automation of Measurements

By automating the measurements, not only can time be saved, but it can also make it easier for other people to work with and understand the working of the system. For automation it is also possible to implement "single-button measurements", which could be combined with a Graphical User Interface that would allow these measurements to be easily performed and the resulting data displayed for the user.

2.2 System Requirements

System requirements are specific technical requirements on the functioning and performance as well as production and discarding of the PA test system.

2.2.1 Power Limitations

Due to the desired maximum output power of 40 dBm, or 10 watt, for the PAs in this project, the system must be able to measure a signal with a maximal power of 40 dBm. Due to the 20 dB gain requirement of the designed PAs, the maximal power delivered to the PAs by the test system must be 20 dBm.

2.2.2 Measurement Frequency

The interpolating-supply PAs in this project are designed for 100 MHz signal range. Thus, the PA test must at least provide support at this frequency.

2.2.3 Measurement Quantities

In order for the system to measure the linearity and efficiency of the PAs, the following things need to be measured:

- *Delivered power*; Using this data, one can determine the amplitude modulation and intermodulation caused by the PAs. The measuring range for this parameter is 0 to 40 dBm. If the performed measurements in this range are done in steps of 1 dBm, the system needs to have a precision of half the step size, thus 0.5 dBm.
- *Input power*; To determine the efficiency, one needs to know how much power is supplied to the PA. The measuring range for the RF-input is -25 to 15 dBm with a step size of 1 dBm, as it needs to align with the desired output. To be able to properly compare input and output power for the efficiency calculation, the precision needs to be the same, thus 0.5 dBm.
- *DC power*; For efficiency measurements, the PA test system must be able to measure the DC power dissipated by the PA.

3 | Test System Decomposition

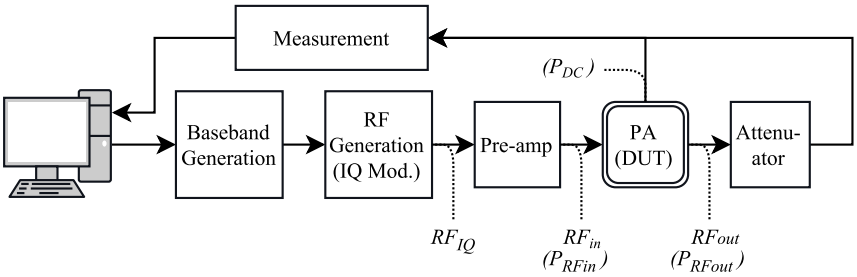


Figure 3.1: Abstracted overview of the entire PA test system and the signal name conventions.

From the assigned power amplifier (PA) test system and our Programme of Requirements (Chapter 2), we set up a conceptual system design by means of a block diagram. As the project progressed, we continuously adjusted this system design as some hardware or methods were recommended for usage by our supervisors due to design problems, straightforward availability or time constraints. For clarity, a highly simplified overview of the entire PA test system is shown in Fig. 3.1.

This chapter decomposes the final test system, explains the purpose behind every part, but leaves things such as the calibration process or the design process to later chapters. We also describe the measurement programme, which we established after exchanges and agreement with the PA design teams. This chapter grants insight into the general functioning of the setup and allows easier discussion in later chapters.

3.1 Software and Hardware Overview

The PA test system is composed of main test hardware, a set of MATLAB files on a PC and additional hardware such a power supplies. Fig. 3.2 shows a decomposition of the PA test system into the underlying categories. The categories are shortly described in the following subsections.

3.1.1 MATLAB

Graphical user interface (GUI) and encapsulation The MATLAB-implemented GUI is the top-level control of the PA test system. We carry out and monitor the measurements from the GUI. Also, power amplifier specification, hardware connection setup and IQ modulator calibration (see below) are done from the GUI.

Input signal processing The nature of interpolating-supply power amplifiers is that the gate bias or input signals are controlled such that (a combination of) the most efficient transistor(s) is (are) amplifying. To realize this, multiple MATLAB scripts for different PA architectures generate the specified inputs, taking into account the type of measurement and driving hardware.

Measurement data processing For evaluation of different PA performance metrics and real-time monitoring the raw measurement data is first processed in MATLAB. The applied processing methods depend on the specific measurement—the measurement programme is put forward in Section 3.2.

Hardware interfaces The PC interfaces with the signal generation card and spectrum analyzer through a VISA TCP/IP connection and GPIB connection, respectively. The Standard Commands for Programmable Instruments (SCPI) type commands are used for back and forth communication and are managed in MATLAB.

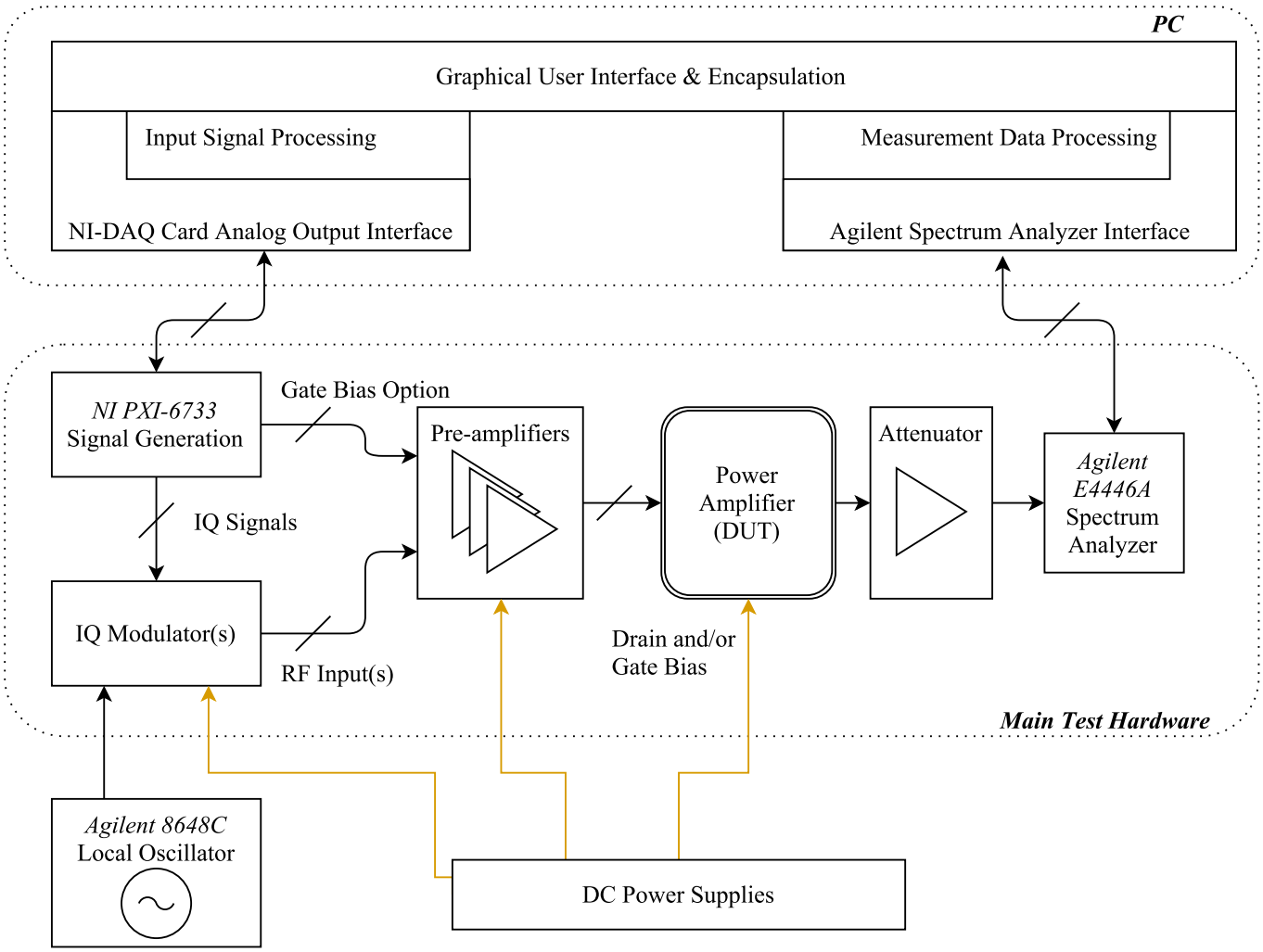


Figure 3.2: A schematical decomposition of the power amplifier test system.

3.1.2 Main Test Hardware

Signal generator The supervisors proposed a National Instruments PXI-6733 signal generation card for baseband signals, in essence a digital-to-analog converter. The DAC features eight 740 MSa/s analog output channels and is accompanied by a buffer board for attenuation and modulator driving capability. We generate the in-phase and quadrature signals for the IQ modulator as well as optional gate bias signals for certain interpolating-supply topologies.

IQ modulator In order to provide radio frequency (RF) signals to the PA under test, we use IQ modulators. IQ modulator modules were provided by the supervisors and are based on Texas Instruments (TI) TRF370417 50-MHz to 6-GHz Quadrature Modulator. The challenge in using IQ modulators is the required calibration, which is necessary due to inherent imperfections such as DC offsets. The IQ modulator calibration is detailed in Section 5.2.

Pre-amplifier For sufficient input signal power level at the PA input, pre-amplifiers are employed since the IQ modulator and signal generation card have a limited power output.

Attenuator The spectrum analyzer is not able to directly measure the high-power PA output signal, as this would damage the measurement device. For this reason we place an attenuator at the PA output.

Table 3.1: An overview of the measurement programme.

Measurement	Method
Efficiency	
Drain efficiency η_D	Static power measurements, $\eta_D = P_{RFout}/P_{DC}$
Power-added efficiency η_{PAE}	Static power measurements, $\eta_{PAE} = (P_{RFout} - P_{RFin})/P_{DC}$
Linearity	
AM/AM distortion	Sweep P_{RFin} for a single-tone input while measuring P_{RFout}/P_{RFin}
THD	Spectrum analysis for single-tone input
IMD	Spectrum analysis for two-tone input

Spectrum analyzer For PA output signal power and phase measurement we are provided with an Agilent E4446A spectrum analyzer. It is remotely controlled through MATLAB.

Power amplifier The design under test (DUT) in this test system is a PA. In the scope of our project, we test two interpolating-supply topologies: one with controlled gain and other with controlled gate bias.

3.1.3 Additional Hardware

Local oscillator The IQ modulator requires a local oscillator (LO) for upconversion of the baseband signals to RF. We are provided with a Agilent 8648C signal generator for this purpose and can use a LO at varying frequencies.

Power supply The IQ modulators, pre-amplifiers and PAs all require a power supply to operate. We use different power supplies available from the microelectronics department.

3.2 Measurement Programme Overview and Background

The measurement programme encompasses the measurements carried out using the PA test system in the scope of this project for interpolating-supply PA evaluation. Table 3.1 shows an overview of the measurement programme.

In view of the limited project duration, the measurement programme consists only of static measurements: the baseband signal does not change during each measurement sample. We do not perform dynamic tests, that is, digitally modulated RF signals such as 16-QAM and the corresponding channel leakage or error vector performance.

Furthermore, we initially opted to measure AM/PM distortion too, however we could not get this functionality working in time on the spectrum analyzer.

The following paragraphs explain the performance metrics and describe each measurement in brief. Chapter 8 covers the measurement methods in more detail.

Efficiency measurements We measure two similar performance metrics for the PA efficiency: the drain efficiency η_D and power-added efficiency (PAE) η_{PAE}. The efficiencies are defined as

$$\eta_D = \frac{P_{RFout}}{P_{DC}}, \tag{3.1a}$$

$$\eta_{PAE} = \frac{P_{RFout} - P_{RFin}}{P_{DC}}. \tag{3.1b}$$

As shown in Fig. 3.1 the P_i variables denote the power measured at certain points in the PA test system, that is, P_{RFout} is the power of the PA RF output signal RF_{out}, P_{RFin} is the power of the PA RF input signal RF_{in} and P_{DC} is supply power dissipated at the drain of the PA. η_{PAE} takes into account the input RF power, but does not differ much from η_D when the PA has high gain.

AM/AM distortion PA linearity is most easily deduced from its gain, which ideally is constant over the specified PA input power range. We measure the PA gain G_{PA} as

$$G_{PA} = \frac{P_{RFout}}{P_{RFin}} \tag{3.2}$$

We refer to deviations from the ideal, constant gain as AM/AM distortion (as a function of P_{RFin}).

Total harmonic distortion (THD) With a single-tone input a PA under test can possibly still output a signal with components at higher frequencies than the input tone, that is, higher-order harmonics. This is distortion of frequency as opposed to distortion of amplitude gain for AM/AM distortion. In particular, we are interested in THD as

$$THD = \frac{P_2 + P_3 + P_4 + \ldots + P_N}{P_1}, \tag{3.3}$$

where P_i is the power of the $i$the-order harmonic of the input tone. In the scope of this project PA design teams expressed that the THD could help in detecting oscillation behaviour at higher-order harmonic frequencies.

Intermodulation distortion (IMD) The final performance metric in the measurement programme is IMD. IMD arises in general from multi-tone inputs at different frequencies.

With a two-tone harmonic input $RF_{in}(t)$ at f_{BB1} and f_{BB2}, the output of a nonlinear amplifier output $RF_{out}(t)$ can be approximated as

$$RF_{out}(t) = \sum_{i=1}^{N} G_i \cdot [RF_{in}(t)]^i, \tag{3.4}$$

with N an arbitrary integer depending on the extent of nonlinearity. For $i = 3$ (3rd-order IMD) the two-tone input will result in harmonics at $2f_{BB1} + f_{BB2}$, $f_{BB1} + 2f_{BB2}$, $2f_{BB1} - f_{BB2}$ and $|f_{BB1} - 2f_{BB2}|$. With small tone spacing it is certainly possible that the output signal will be distorted as for example $2f_{BB1} - f_{BB2} \approx f_{BB1}$, but also with wide tone spacing due to 2nd- or higher-order intermodulation products. It can be even more worrying to have 3rd-order components interfere with adjacent channel signals.

For the above reasons, we measure the IMD up to 3rd-order. Moreover, from static measurements the 3rd-order intercept point (TOI or IP3) can be estimated by means of power level extrapolation: the 3rd-order distortion components are expected to grow 3 dB per dB two-tone input power. Beyond IP3 the 3rd-order components hold a larger share of the total output power than the components at f_{BB1} and f_{BB2}.

4 | Baseband Signal Generation

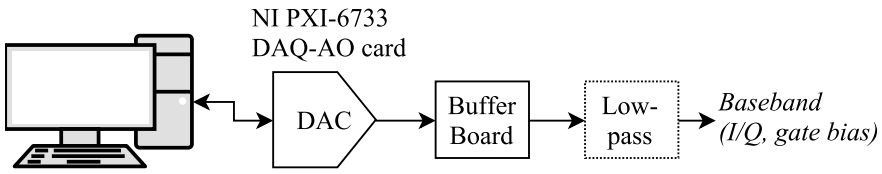


Figure 4.1: Simple overview of the baseband signal generation subsystem.

Controlled input signals are essential for radio frequency (RF) power amplifier (PA) evaluation. For this purpose we generate baseband signals in the test system. Baseband signals contain information at frequencies much lower than the RF carrier frequency f_c: in the scope of this interpolating-supply PA project $f_c = 100$ MHz. The baseband signals can be upconverted to the RF domain around f_c using subsequent mixers present in IQ modulators. Chapter 5 covers the IQ modulators.

For signal generation two hardware options were made available during the project:

- The "low-speed" National Instruments PXI-6733 DAQ Analog Output Series device with up to 740 kSa/s output sample rate;
- The "high-speed" National Instruments PXIe-5450 differential I/Q generator with up to 400 MSa/s output sample rate.

Within their respective output voltage ranges, both signal generators have a 16-bit output resolution. The PXIe-5450 high-speed signal generator has the capability of generating RF signals instantly without the need of upconversion, removing the need of mixers. The high-speed signal generator further has the advantage of a greater signal information bandwidth around $f_c = 100$ MHz compared to the low-speed device; assuming perfect signal reconstruction, the high-speed signal generator can have a theoretical information bandwidth up to 100 MHz, whereas the low-speed solution has a maximum bandwidth of 370 kHz.

Because the high-speed signal generator was in use during the first two weeks of the project and our project time was limited, we decided to start with the low-speed National Instruments (NI) PXI-6733 DAQ Analog Output Series device (DAQ-AO card)—in the remainder of this chapter simply referred to as digital-to-analog converter, *DAC*. The bandwidth of the DAC is sufficient for carrying out the measurement programme (Section 3.2) and a transition to a high-speed signal generator is simple, as it only requires the signal to be digitally upconverted. The DAC makes the use of upconverting mixers necessary, which offered additional instructive experience.

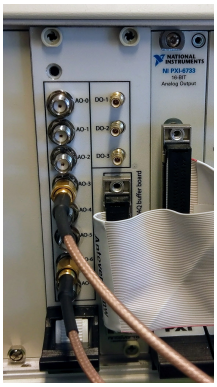
This chapter first covers the specifications and limitations of the chosen DAC for signal generation. Subsequently, we discuss the gain and noise due to the buffer board which accompanies the DAC. The designed and realized LC filter in order to reduce the noise are presented next. Finally, we show the final results regarding baseband signal generation.

4.1 DAC Signal Generation

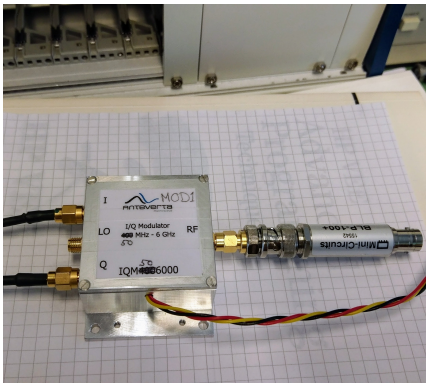
4.1.1 Specifications and Limitations

The DAC features 16-bit signal generation as indicated above, but other remaining specifications of the card are relevant too. Table 4.1 shows all relevant specifications regarding the DAC [23].

The output sample rate limits the baseband bandwidth to 740/2 = 370 kHz. This assumes the presence of an ideal low pass reconstruction filter being able to filter out the attenuated digital baseband copies spaced 740 kHz apart in the frequency domain. As a perfect reconstruction filter is not implemented in the hardware, we only generate baseband signals up to 200 kHz to preserve the waveform shape.



(a) Buffer board and DAC



(b) IQ modulator

Figure 4.2: Main components of the PA test system signal generation subsytems. (a) NI PXI-6733 DAQ-AO card (right) and buffer board (left) for baseband. (b) IQ modulator for upconversion to RF.

Table 4.1: Relevant DAC specifications.

Quantity	**Specified Value**
Voltage range	$\pm$10 V
Resolution	16 bit ($\equiv$ 65536 steps)
Output sample rate	740 kSa/s
Number of analog output ports	8
Output impedance	0.1 Ω
Current drive (max.)	$\pm$5 mA
Offset error (max. after calibration)	$\pm$168 μV
Noise	80 µV (rms), DC to 1 MHz

The DAC has a maximum current drive of 5 mA and low output impedance of 0.1 Ω. These specifications result in a minimum load input impedance of $\approx$ 2 kΩ, when the full $\pm$10 V voltage range is used. As 50 Ω is the most common load input impedance, an accessory buffer board was provided with the DAC immediately connected to the DAC output through the 68-Pin AO I/O connector as shown in Fig. 4.2a.

4.1.2 Initialization and Control

A C-based driver for the DAC was provided by the supervisors. The driver can be controlled from within MATLAB and we wrote a small initialization script building upon the provided driver files. This script, `initNIDAQ(fs,wfm_size)`, can be used to specify the waveform size (number of samples) and output sample rate. The initialization ends with updating all waveforms (analog outputs, datamarker and triggers) to default zeros using the provided function `update_waveforms`. The DAC repeats the waveforms at the specified output sampling rate given to `update_waveforms` as input arguments, requiring a waveform for each of the eight available analog output ports.

4.2 Buffer Board

The buffer board allows for using the DAC for low impedance loads while also providing convenient SMA connectors for the analog outputs. The buffer board reads that it is manufactured at Anteverta-mw, however no official data sheet exists—it was custom-built. We do know that the output impedance of the buffer board is 50 Ω from a sine wave measurement with an oscilloscope switching between high impedance and 50 Ω modes, showing a reduction of the measured wave amplitude by half.

The buffer board also allows for usage of the full DAC voltage range of $\pm$10 V. The cascaded IQ modulator covered in the next chapter starts to enter gain compression above 7.3 dBm input power for signals around 100 MHz [24], such that the IQ modulator should be driven with rms voltage levels lower

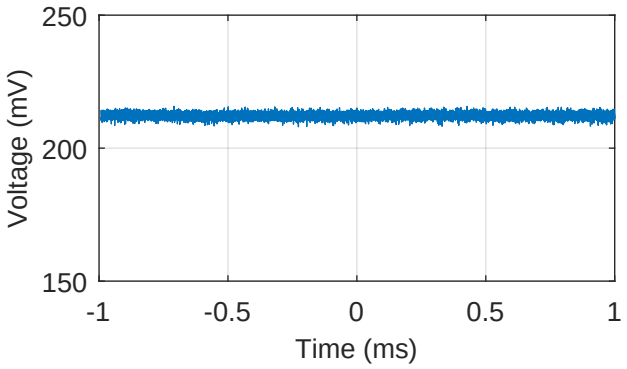


Figure 4.3: Waveform captured by the oscilloscope at the buffer board output with the DAC at maximum positive output voltage. The measured peak-to-peak noise amounted to roughly 10 mV.

than ≈ 0.52 V (50 Ω). To this end, the "buffer" board attenuates the DAC's output signals to maintain the DAC specified resolution of 16-bit, assuming no noise is added.

Neither gain (attenuation) nor noise level of buffer board were fully specified beforehand. The following two subsections expand on the characterization and noise reduction methods applied to the buffer board and (to some extent) the DAC. The characterizations are essential as a good test system must have well determined input test signals to the design under test. All oscilloscope measurements in this chapter were carried out in 50 Ω input impedance mode with a 50 Ω BNC coax cable.

4.2.1 Gain Characterization

Measurements at various output DC voltage levels of the DAC showed that the buffer board has an attenuation factor which is not a well-rounded number (integer). For example, the measurement shown in Fig. 4.3 revealed that the buffer board outputs a ≈ 212 mV mean voltage over a 50 Ω load when the DAC is at the 10 V specified maximum positive voltage. This results in an attenuation factor of 47.2 or an equivalent gain of 0.0212.

However, the linearity of the buffer board is not guaranteed. We therefore carried out a DC sweep with the DAC and measured the mean voltage automatically with the oscilloscope (50 Ω mode). The automatic control of the oscilloscope is more elaborated on in Section 5.2.2. The sweep utilized the full DAC output voltage range of ± 10 V. With an input step size of ≈ 45 mV, more than 400 sample points were collected.

The measurement result of the sweep showed that the buffer board is very linear over the full DAC output range but also revealed a small offset error. The high linearity allowed for an attempt of gain and offset estimation by means of a polynomial fit.

As shown by Fig. 4.4, a 6th-order fit resulted in fit errors less than 0.8 mV. A gain estimation of 0.02095 was found, equivalent to an attenuation factor of 47.72. Furthermore, the buffer board offset is estimated to be 1.719 mV. The attenuation factor is in the neighborhood of 50, such that the buffer board output voltage range is limited to little over $\pm 10/50 = \pm 200$ mV.

4.2.2 Noise Characterization and Reduction

Noise characterization Measured waveforms on the buffer board output using the oscilloscope without averaging enabled (such as Fig. 4.3) clearly show the presence of noise. From the waveforms captured for the gain characterization as explained above, a peak-to-peak noise in the order of 10 mV was measured. This peak-to-peak noise level is much more than expected as the DAC rms noise level is specified to be 80 µV while the buffer board attenuates nearly by a factor of 50.

Further measurements of single tones as seen in Fig. 4.5a generated with the DAC showed that the peak-to-peak noise level remains to be around 10 mV. Frequency domain analysis exhibits significant spectral copies at integer multiples of the output sample rate of the DAC. In Fig. 4.5b, the copies are visible at 2×740 kHz and 3×740 kHz, indicating that the reconstruction filter in either DAC or buffer board are

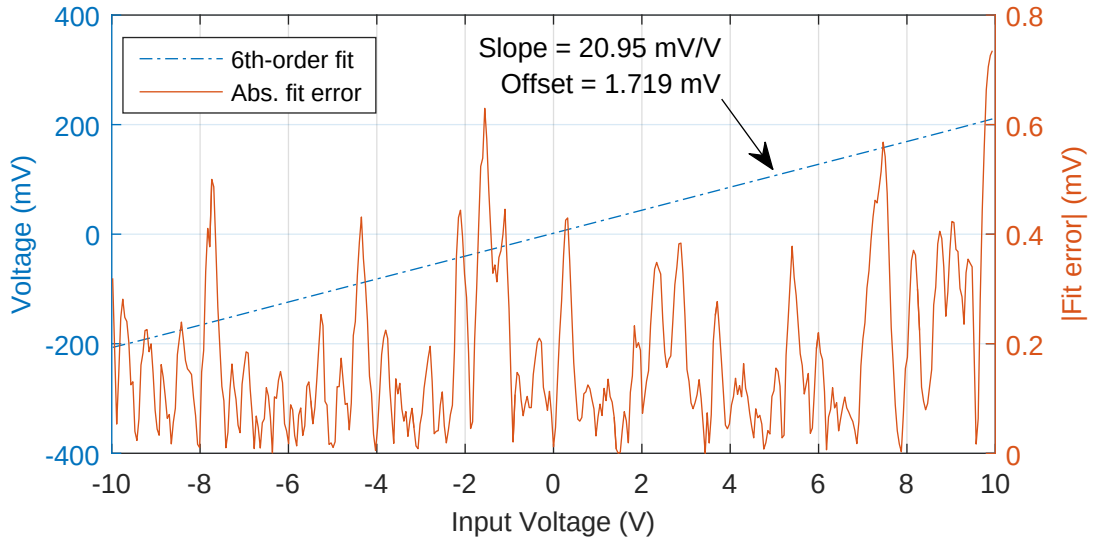
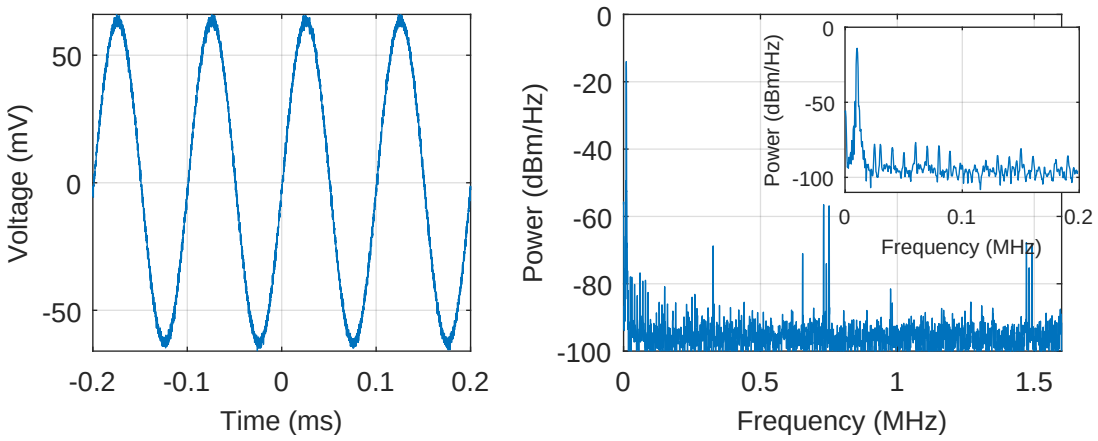


Figure 4.4: Buffer board gain and voltage offset estimated from the fitted mean voltage measurement data with the fit error for justification of the 6th-order polynomial fit.



(a) Waveform (b) Power spectrum

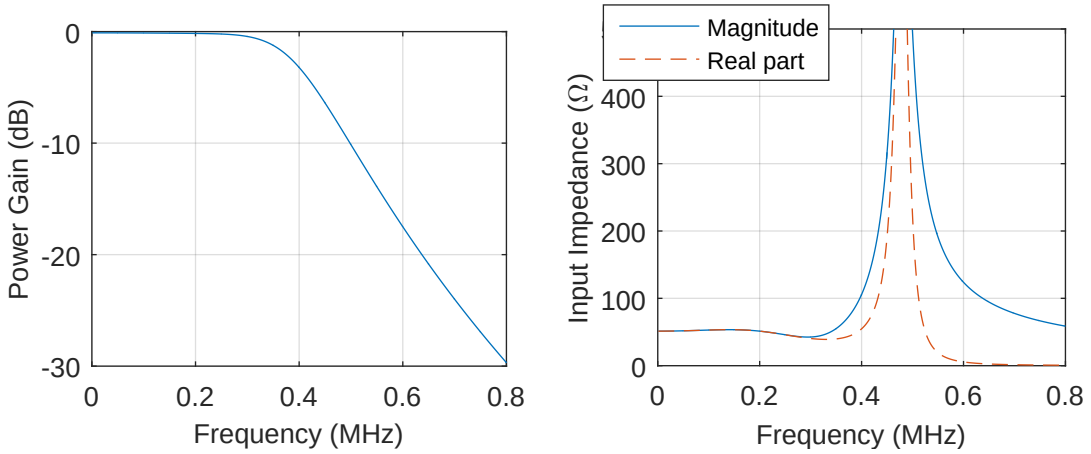
Figure 4.5: 10 kHz sine wave measured at the output of the buffer board at a 740 kSa/s output sample rate. (a) Part of the waveform measured. (b) Power spectrum with a zoomed in view.

insufficient. Furthermore, additional noise is seen more strongly around DC, not copied at multiples of the output sample rate. As confirmed by our supervisor, this phenomenon is due to $1/f$ noise arising in the buffer board.

LC filter design In order to reduce noise as shown in Fig. 4.5 we decided to design a low-pass filter to at least attenuate the spectral copies at the multiples of the output sample rate while also filtering away any higher frequency noise. A high-pass filter is not suitable as a varying bias interpolating-supply PA requires a controlled DC gate bias voltage. Thus, the $1/f$ noise cannot be easily removed.

We set the following requirements for the LC low-pass filter:

- sufficient attenuation to suppress a spectral copy at 740 kHz;
- flat transfer and little (none) attenuation up until 200 kHz; and
- input and output impedance of 50 Ω up untill 200 kHz.



(a) Gain (b) Impedance

Figure 4.6: 5-pole LC low-pass filter simulations from ADS including parasitic effects. (a) Gain simulation. (b) Input impedance, which is equal to the output impedance.

From the impedance requirement we chose a symmetric π-type LC filter topology; this requires less inductors compared to a T-type topology. For a flat transfer up to 200 kHz, we chose a maximally flat Butterworth filter and used an online design tool [25] to compute ideal values for different filter orders with f_{-3dB} at 350 kHz and ran simulations in Advanced Design System (ADS).

Measurements such as seen in Fig. 4.5b indicated that at 740 kHz 30 dB power attenuation is required to suppress the spectral copy. For this reason, we decided to build a 5-pole low-pass filter with $5 \times 6 = 30$ dB/octave rolloff and consisting of two inductors and three capacitors. Picking the components allowed for simulations including non-ideal (parasitic) effects, with inductor DC resistance being most critical to have little attenuation.

The final simulations are shown in Fig. 4.6. The power attenuation at 200 kHz is less than 0.5 dB while at 740 kHz over 25 dB power attenuation is expected. Moreover, input and output impedance do not exceed 54 Ω up until 200 kHz.

4.3 Results and Discussion

Four LC-filters were built, shown in Fig. 4.7, of which two were made using a more lossly dielectric, namely X7R instead of NP0, due to time-constraints. The gain of the filters were measured by connecting the signal generator to a filter, sweeping the frequency and measuring the resulting signal with the spectrum analyzer.

The resulting gain characteristics can be found in Fig. 4.8, which shows that the two version have a similar frequency response, with the main difference being the about 0.2 dB additional attenuation.

DC and harmonic measurements confirmed that the noise was reduced. Fig. 4.9 shows a comparison with the earlier 10 kHz sine wave with the first spectral copy being attenuated by 25 dB. The peak-to-peak noise voltage was reduced from 10 mV to 2.4 mV, regardless of signal type.

The 25 dB attenuation at 740 kHz is less than the first specified 30 dB. At the time of evaluating the realized filter performance, no more time was left to further improve the filter and order additional components. A higher-order filter could further reduce the noise due to spectral copies.

The low frequency $1/f$ noise, however cannot be reduced by means of a low-pass filter, which is also confirmed by Fig. 4.9b. A high-pass filter cascaded with the low-pass filter could alleviate this, but some PAs require a controlled DC voltage—a high-pass filter would remove this capability.

Within the provided time, it was not feasible to evaluate the combination of all (eight) analog output ports and one of the realized low-pass filters. The total gain from the DAC to the filter output is therefore varying depending on the specific output ports and filters used. The generated RF signal to the PAs under test must be precisely measured beforehand.

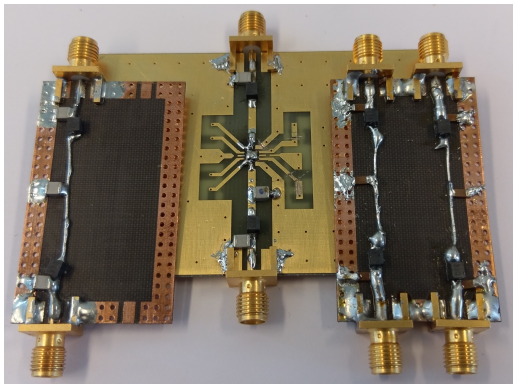


Figure 4.7: Four realized prototype LC filters, each compromising two inductors in the direct path and three capacitors to ground in π-topology.

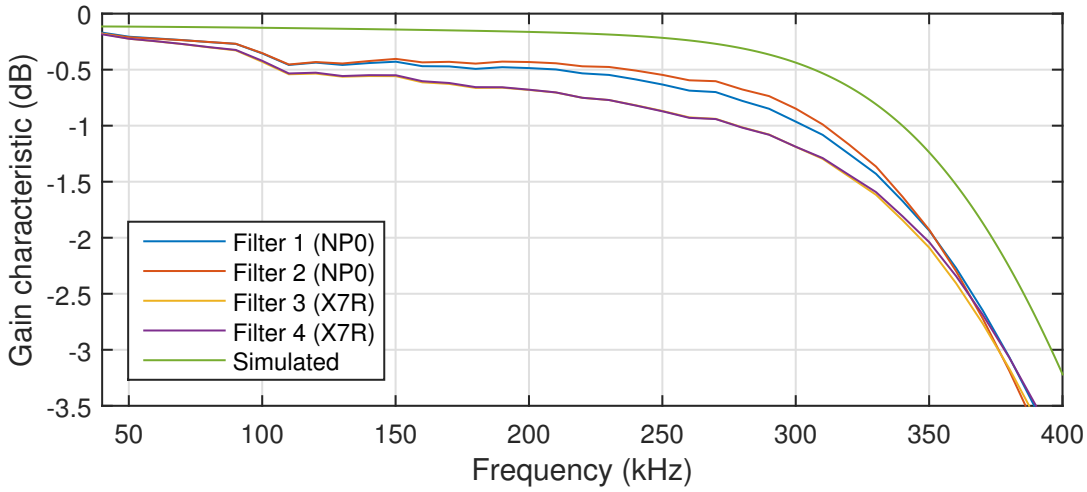
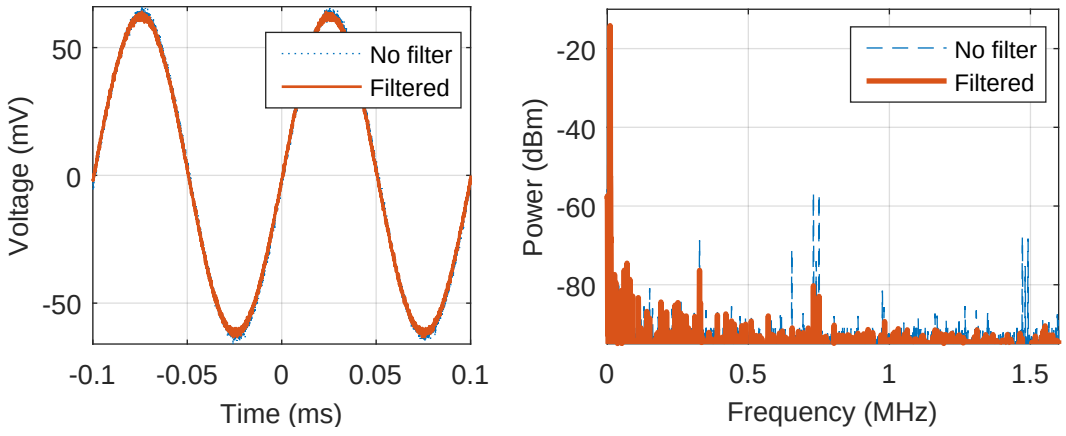


Figure 4.8: Gain characteristic of the four produced LC-filters, with the filters labeled in order of production, and of the simulated filter



(a) Waveform

(b) Power spectrum

Figure 4.9: 10 kHz sine wave measured at the output of the realized LC filter at a 740 kSa/s output sample rate compared to the no-filter case. (a) Part of the waveform measured. (b) Power spectrum.

5 | RF Signal Generation

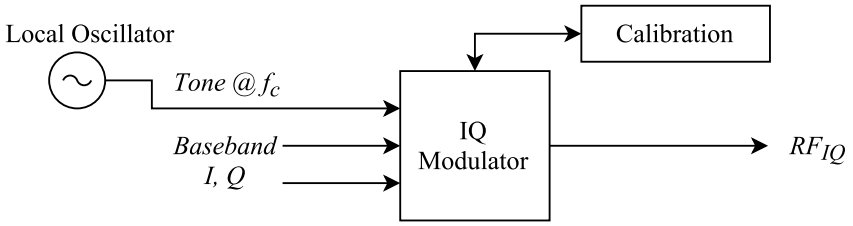


Figure 5.1: Simple overview of the RF signal generation subsystem.

The test setup evaluates radio frequency (RF) power amplifiers (PAs) and consequently generates RF signals for the PA input(s). To this end, we incorporated IQ modulators in the PA test system. Fig. 5.1 shows a simple overview of the RF signal generation subsystem.

This chapter briefly presents background on IQ modulators and the hardware implementation in our PA system. Consequently, the effectuated automatic calibration required to minimize IQ modulator non-idealities is covered. Finally, the calibration results are compared to the IQ modulator data sheet specifications, [24].

5.1 IQ Modulator

IQ modulators (ideally) are devices which sum two output signals of their two internal mixers, as shown in Fig. 5.2. The mixers multiply two signals in time domain: a baseband signal and an RF signal (carrier). The carrier is phase shifted internally by 90°such that an in-phase (0°) and quadrature (90°) mixer can be distinguished.

In this chapter, we designate the in-phase and quadrature baseband inputs by $I_{BB}(t)$ and $Q_{BB}(t)$, respectively; the IQ modulator output signal is designated by $RF_{IQ}(t)$. We also assume that the local oscillator (LO) produces the carrier $\cos(2\pi f_c t) = \cos(\omega_c t)$. Thus, mathematically the ideal IQ modulator generates

$$RF_{IQ}(t) = I_{BB}(t)\cos(\omega_c t) - Q_{BB}(t)\sin(\omega_c t). \tag{5.1}$$

For this project, we were provided with IQ modulator modules from Anteverta-mw. The module utilizes at its core a Texas Instruments TRF370417 *50-MHz to 6-GHz Quadrature Modulator*. The module features a 50 Ω input and output impedance and is specified to have a voltage gain of roughly -8 dB at our 100 MHz carrier frequency f_c [24]. At the output of the IQ modulator (module) a 50 Ω coaxial low-pass filter with $f_{-3dB} \approx 108$ MHz is connected to remove harmonics arising from amplifiers inside modulator [26]. We view this low-pass filter as part of the IQ modulator in the RF signal generation subsystem.

5.2 IQ Calibration

In practice, IQ modulators are required to be calibrated beforehand in order to be able to generate a RF signal with the desired precision. This subsection covers the automatic calibration methods by means of a remote-controlled oscilloscope for the provided IQ modulators.

5.2.1 Modulator Non-idealities

By evaluating the IQ modulator output signal for different $I_{BB}(t)$ and $Q_{BB}(t)$ non-idealities concerning DC offsets, gain imbalance and phase mismatch were discovered.

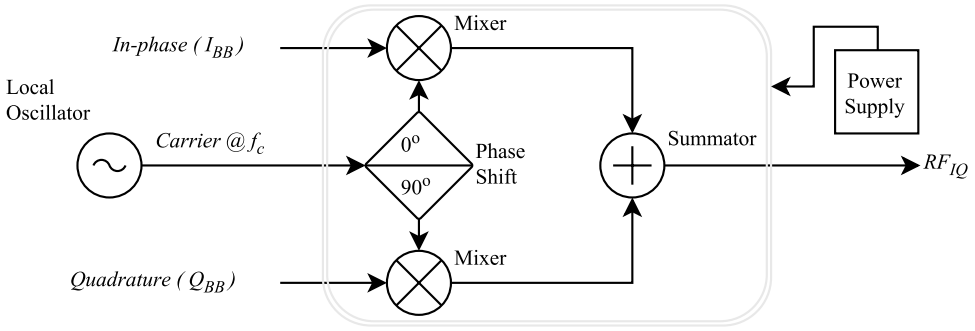


Figure 5.2: Operation of an ideal IQ modulator.

DC offset When generating a 0 V DC voltage with the DAC for $I_{BB}(t)$ and $Q_{BB}(t)$, $RF_{IQ}(t)$ was measured to be a harmonic at f_c. This phenomenon is known as LO leakage and can arise from non-ideal isolation between mixer ports or internal DC offsets [27]. In any case, we can model the LO leakage as due to a DC offset $O_{I/Q}$ in $I_{BB}(t)$ and $Q_{BB}(t)$, that is,

$$RF_{IQ}(t) = [I_{BB}(t) + O_I]\cos(\omega_c t) - [Q_{BB}(t) + O_Q]\sin(\omega_c t). \tag{5.2}$$

The sum of a cosine and sine with equal frequency can always be rewritten into a single harmonic with equal frequency. The LO leakage can be counteracted by calibration for a fixed compensating DC value in both $I_{BB}(t)$ and $Q_{BB}(t)$.

Gain imbalance In Fig. 5.2 the paths from the baseband inputs to the summation are assumed to have unity gain. When these paths are not symmetrical, a gain imbalance exists and thus $RF_{IQ}(t)$ cannot be well determined beforehand. When attempting to generate lower single side band (LSSB) modulation, that is $I_{BB}(t) = \cos(\omega_{BB}t)$ and $Q_{BB}(t) = \sin(\omega_{BB}t)$, we expect a single tone applying the product-to-sum identity:

$$\begin{aligned} RF_{IQ,USSB}(t) &= \cos(\omega_{BB}t)\cos(\omega_c t) - \sin(\omega_{BB}t)\sin(\omega_c t) \\ &= \cos[(\omega_{BB} + \omega_c)t]. \end{aligned} \tag{5.3}$$

With the uncalibrated IQ modulator, also a substantial tone at $f_{BB} - f_c$ arose. A possible cause is gain imbalance, which we can model as

$$\begin{aligned} RF_{IQ}(t) &= G_I\cos(\omega_{BB}t)\cos(\omega_c t) - G_Q\cos(\omega_{BB}t)\sin(\omega_c t) \\ &= \frac{G_I + G_Q}{2}\cos[(\omega_{BB} + \omega_c)t] + \frac{G_I - G_Q}{2}\cos[(\omega_{BB} - \omega_c)t], \end{aligned} \tag{5.4}$$

where path gains G_I and G_Q are not necessarily equal. Thus, assuming that $G_{I/Q}$ are time-independent, we can counteract gain imbalance by digitally calibrating G_I of $I_{BB}(t)$ to equal G_Q.

Phase mismatch We observed that phase mismatch is another cause for undesired side band creation. The oscilloscope showed that the DAC-generated USSB IQ harmonics were not perfectly 90°out of phase, but also perfect IQ modulator LO quadrature shift is not guaranteed. For example, a (small) LO quadrature error ϕ_{LO} results in

$$\begin{aligned} RF_{IQ}(t) =& \cos(\omega_{BB}t)\cos(\omega_c t) - \cos(\omega BBt)\sin(\omega_c t + \phi_{LO}) \\ =& \underbrace{\tfrac{1}{2}[1 + \cos(\phi_{LO}) - \sin(\phi_{LO})]}_{\approx 1}\cos[(\omega_{BB} + \omega_c)t] + \\ & \underbrace{\tfrac{1}{2}[1 - \cos(\phi_{LO}) - \sin(\phi_{LO})]}_{\approx 0}\cos[(\omega_{BB} - \omega_c)t], \end{aligned} \tag{5.5}$$

where both product-to-sum and sum-to-product identities were applied. As ϕ_{LO} grows, the undesired component at $f_{BB} - f_c$ will become more prominent. An undesired component arises in the same way when a baseband quadrature ϕ_{BB} exists. Therefore, we counteract all static phase mismatch from the LO and baseband signals solely by calibration of the digital phase shift of $I_{BB}(t)$ with respect to $Q_{BB}(t)$.

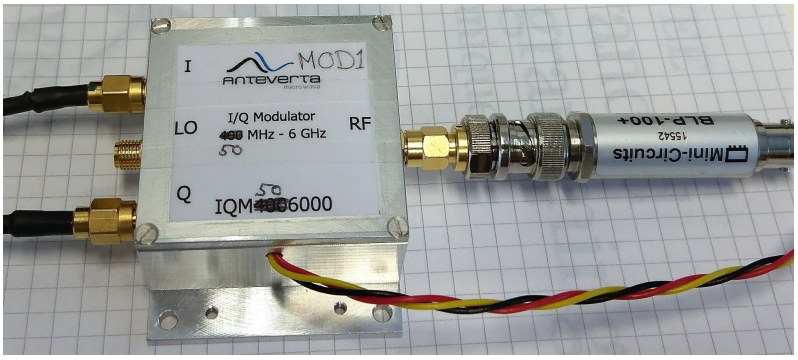


Figure 5.3: IQ modulator and 108 MHz low-pass filter used in this project.

5.2.2 Remote-control Oscilloscope

The IQ calibration utilizes a Rohde and Schwarz RTO1044 oscilloscope connected directly to the IQ modulator at the low-pass filter output (see Section 5.1 and Fig. 5.3). The IQ modulator is driven using the DAC and buffer board combination.

For convenience and calibration automation, we wrote a set of 14 MATLAB functions in order to remote control the oscilloscope. The set of functions have purposes in the following categories:

- *Basic:* waveform displaying and capturing;
- *Measurement:* settings and data transfer of time domain measurement, FFT analysis and cursors; and
- *Miscellaneous:* (communication) initializations and data handling.

Communication between the PC running MATLAB and oscilloscope is established using Standard Commands for Programmable Instruments (SCPI) commands over a TCP/IP interface with the Virtual Instrument Standard Architecture (VISA) standard.

5.2.3 LO Leakage Calibration

We developed a single-script automated calibration procedure measuring LO leakage due to DC offsets as detailed in Section 5.2.1.

The calibration applies DC signals on the I and Q ports as follows:

1. Set DC ranges and step sizes, initialize instrument communication and settings $\Rightarrow I_{DCo} = Q_{DCo} = 0$.
2. Sweep I_{DCo} and measure LO leakage V_{LO} rms $\Rightarrow$ set I_{DCo} to corresponding lowest V_{LO} measured.
3. Sweep Q_{DCo} and measure LO leakage V_{LO} rms $\Rightarrow$ set Q_{DCo} to corresponding lowest V_{LO} measured.
4. Adjust step size, repeat steps 2 and 3 around the new I_{DCo}, Q_{DCo} settings.

The number of iterations and adjustment of step sizes allows for a trade-off between calibration time and accuracy.

5.2.4 Single Sideband Calibration

Two other calibration procedures were developed based on SSB modulation, enabling IQ calibration for gain imbalance and phase mismatch. Both procedures measure the desired and undesired sidebands using oscilloscope cursor peak detection in FFT mode. Peak detection is more precise than setting the cursor at the expected frequencies. The peak detection will not be disturbed by the LO leakage, as SSB calibration will be ran after LO leakage calibration and the LO suppression is expected to be > 20 dB better than the sideband suppression from the IQ modulator specifications [24].

Table 5.1: Final IQ calibration results achieved (lower is better).

	LO Leakage (dBm)	**Sideband Suppression (dBc)**
Uncalibrated – Observed @100 MHz	-30	-15
Calibrated – Datasheet @80 MHz	-60	-35
Calibrated – Our Work @100 MHz	-75	-60

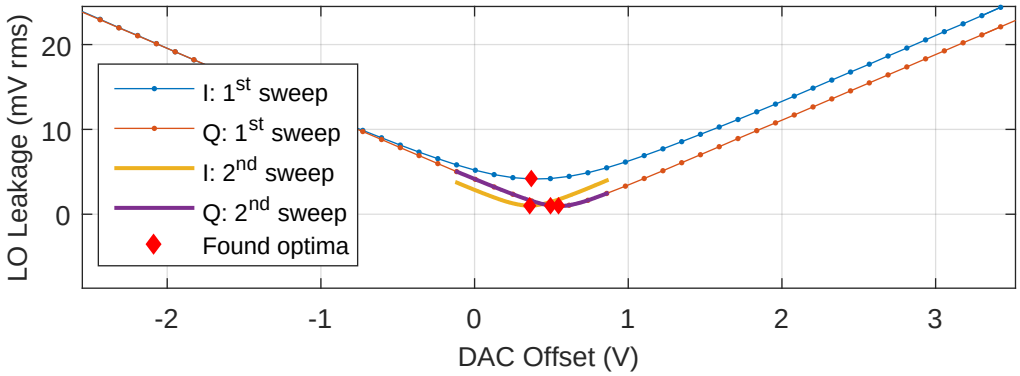


Figure 5.4: Calibration results for DC offset. This calibration performed four sweeps in total: I followed by Q and both repeated once, as described in Section 5.2.3.

The procedure for phase mismatch calibration is as follows:

1. Set f_{BB} and phase ϕ_o range and step size, initialize instrument communication and settings $\Rightarrow \phi_o = 0°$.
2. Apply sinewaves on I and Q ports shifted by $90° + \phi_o$ (and offsetted by I_{DCo}, Q_{DCo}, respectively).
3. Sweep ϕ_o, measure the second largest peak in FFT mode $\Rightarrow$ set ϕ_o to corresponding largest sideband suppression measured.
4. Adjust step size, repeat step 3 around the new ϕ_o setting.

A similar procedure applies for the gain imbalance calibration where instead of a phase shift, a gain factor G_o applied to the sinewave on the I port is swept.

5.3 Results and Discussion

We were able to calibrate the provided IQ modulators for usage with and without the noise-reducing buffer board LC low-pass filters. In addition to the scripts for calibration with the oscilloscope, we also realized a graphical user interface (GUI) as shown in Fig. 5.5 for further automation. Calibration results for one the provided IQ modulators are shown in Fig. 5.4 and Fig. 5.6 for the non-ideality of interest: LO leakage and undesired sidebands, respectively.

As summarized in Table 5.1, LO leakage was reduced to -75 dBm, which is 15 dB lower than the specified -60 dBm in the data sheet at similar circumstances [24]. After four sweeps, no further reduction of the LO leakage could be measured.

The SSB calibration also showed significant improvements of the sideband suppression from gain and phase variation, such that a -60 dBc undesired sideband could be reached. This suppression is a 25 dB improvement over the datasheet sideband specifications. Both gain and phase calibration showed improved suppression, but gain imbalance seemd to be more dominant than phase mismatch. For this reason a phase calibration had to be carried out before the gain calibration.

All results considered, the IQ calibration was very accurate and well automated with the GUI allowing for precise RF signal generation.

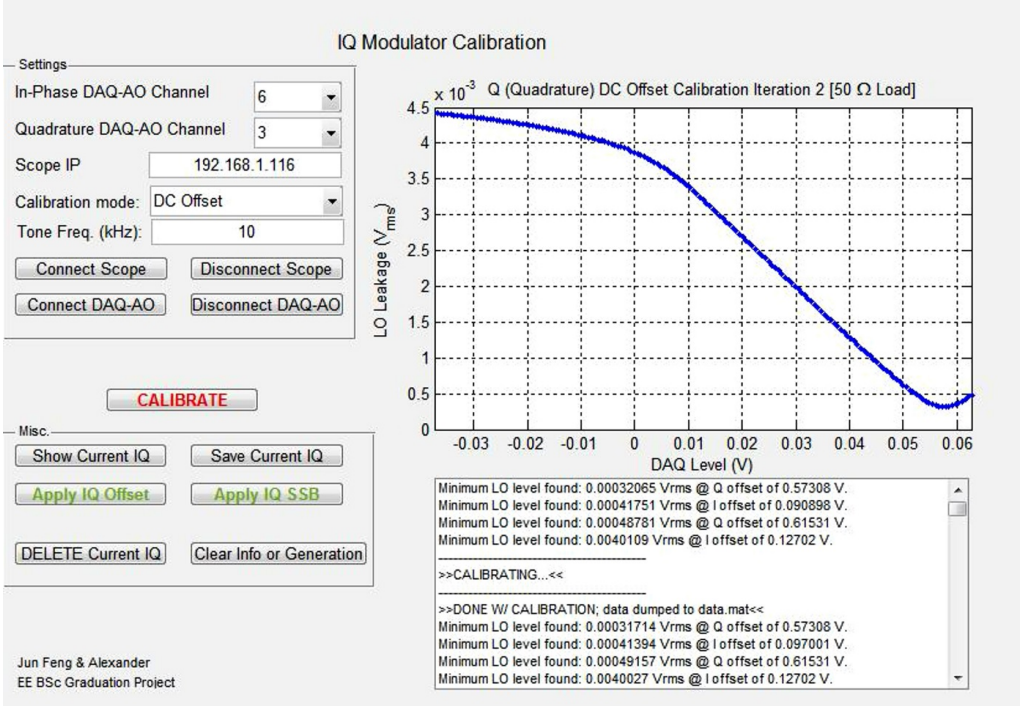
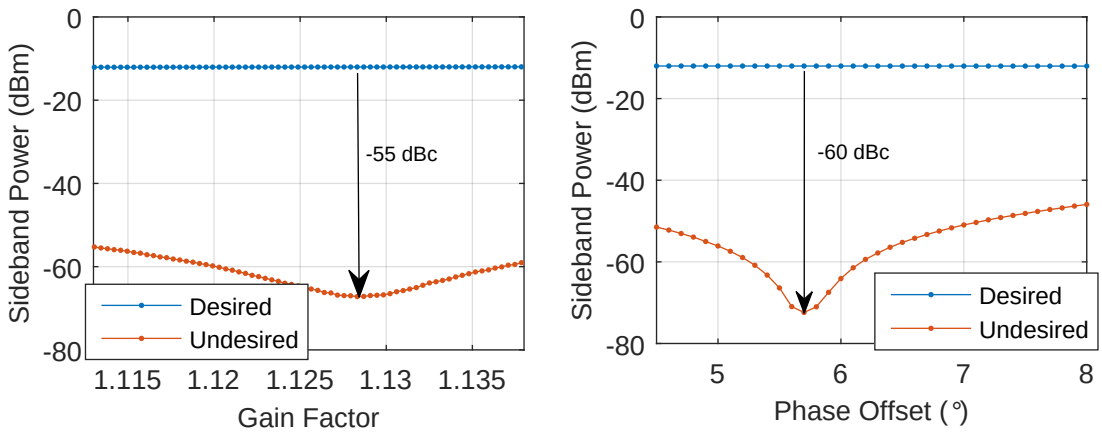


Figure 5.5: Screenshot of the GUI used for IQ calibration.



(a) Gain calibration

(b) Phase calibration

Figure 5.6: Calibration results for USSB with a 10 kHz baseband harmonic. (a) Calibration for gain imbalance. (b) Calibration for phase mismatch.

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6 | Pre-amplifier

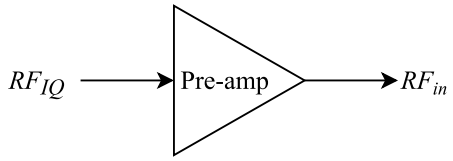


Figure 6.1: Simple system overview of the pre-amplifier subsytem.

6.1 Requirements

The main requirement of the pre-amplifier design is that it amplifies the signal sent by the IQ modulator (RF_{IQ}) to the desired power level. This level depends on the gain of the power amplifiers (PAs) designed by the other teams, which changed over the course of this project between 20 and 28 dB. The power level thus varied between 12 and 20 dBm. Based on the -8 dBm first approximation of the maximal power of RF_{IQ}, this leads to the pre-amplifier needing a gain between the 20 and 28 dB.

The pre-amplifier also needs to be able to follow signals with a large swing properly. Assuming a output power of 20 dBm, the greatest peak voltage V_p that needs to be delivered is:

$$V_p = \sqrt{2} \cdot V_{rms} = \sqrt{2} \cdot \sqrt{10^{(20-30)/10} \cdot 50} \approx 3.16 \text{ V}. \tag{6.1}$$

Since the highest frequency of interest in RF_{IQ} is (near) 100 MHz, the minimal slew rate SR of the pre-amplifier is:

$$SR = 2\pi f \cdot V_p \approx 2 \cdot \pi \cdot 100^6 \cdot 3.16 \approx 1987 \text{ V/µs}. \tag{6.2}$$

When performing a two-tone measurement the distortion of the signal caused by the pre-amplifier, due to mismatched gain and intermodulation, makes evaluating the distortion caused by the PAs more difficult. These criteria are however not that vital, as one could employ pre-distortion techniques to limit the distortion to lower levels if it obscures the evaluation too much.

For stability one has to make sure that any oscillations die out quick enough. With a maximal signal frequency of 100 MHz, the minimal time between rising and falling edges for rectangular waves is 5 ns. Any oscillation must thus fall to 5 % within 5 ns.

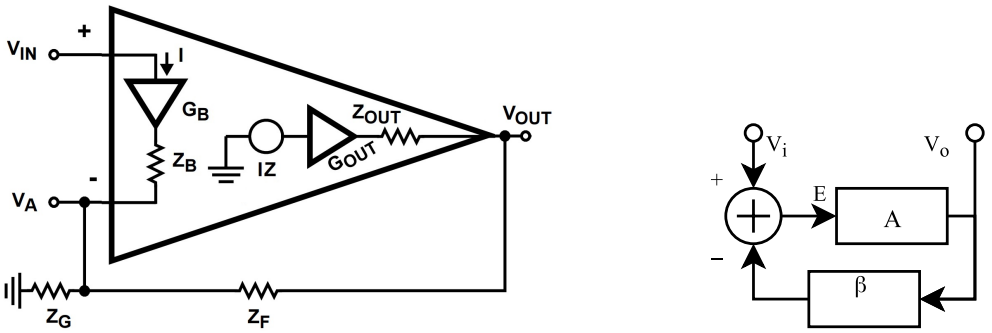
Summarizing, the pre-amplifier needs to meet the following requirements:

- Gain between 20 and 28 dB;
- Slew rate $\geq$ 1987 V/µs;
- Intermodulation distortion $\leq$ -30 dBc;
- Gain flatness of 0.5 dB in $\pm$ 10 kHz around 100 MHz; and
- Settling time = 5 ns.

6.2 Simulations

The pre-amplifiers were designed by use of the software Advanced Design System (ADS), with which the following simulations were performed:

- *AC analysis*; In order to study the gain of the pre-amplifier over frequency.
- *Harmonic Balance analysis*; In order to study the distortion caused by harmonics and intermodulation introduced by the pre-amplifier.



(a) CFA model taken from [29]

(b) Block diagram

Figure 6.2: Simple models for noninverting amplifiers with negative feedback. (a) Simplified current feedback amplifier. (b) Negative feedback block diagram.

- *Transient analysis*; In order to study the stability of the pre-amplifier.

The basic schematic used in the design process can be contains the appropriate source at the pre-amplifiers input, a 50 Ω load, as the PAs will have a 50 Ω input impedance, and a 5 pF capacitance, as the devices used in the PAs have a typical input capacitance of 4.5 pF.

For the harmonic balance a source is used which generates two tones, 95 and 105 MHz, of equal power. The chosen frequencies allow the user to distinguish between intermodulation and harmonics of the tones. For the transient analysis a rectangular pulse is send to the pre-amplifier, which due to the short rise and fall time (1 ns) provides the pre-amplifier with a wide range of frequencies. With this one can determine the stability of the pre-amplifier, as one or more of those frequencies could cause oscillations in the pre-amplifier which would be seen during simulation.

All sources have a 50 Ω output impedance and deliver a -8 dBm signal, as this is the output impedance of the IQ-modulator and the estimated maximal power that could be delivered with it.

6.3 Design

During the design of the pre-amplifier different alternatives for different matters were considered and certain choices were made from them. In this section those choices are discussed.

6.3.1 Device

First of all, a suitable device needed to be selected. For this we have opted for an operational amplifier (op-amp), as it is simpler to design an amplifier with than with a transistor, which allows us to spend more time on other matters. Furthermore the op-amp is of the current feedback amplifier (CFA) variety, which has a better bandwidth than voltage feedback amplifier (VFA), due to their direct gain not only being dependant on the transimpedance of the op-amp, but also on the feedback network.

The choice was made to use the THS3091 CFA, as this device was already in the supervisor's possession and meets our requirements [28].

6.3.2 Topology Analysis

Before the network around the device can be determined, a model for the device should be established, which can be found in Fig. 6.2a.

From the model we deduced the output voltage will not be inverted, if the current I flows out of the inverting input. The feedback network thus needs to be connected to the inverting input and the input signal delivered at the noninverting input. This input sees a very high impedance (1,3 MΩ for the chosen device [28]), due to the input buffer. To still match the input with the IQ-modulators, a 50 Ω resistance to

ground needs to be placed at the noninverting input, as the output impedance of the IQ-modulators are also 50 Ω.

After analyzing the schematic for a noninverting CFA and leaving out the effect of Z_{OUT} as this value approaches zero, namely 0.06 Ω, the following equation is deduced for the loop gain of the CFA:

$$\frac{V_O}{V_{IN}} = \frac{\frac{Z(1+Z_F/Z_G)}{Z_F(1+Z_B/(Z_F\|Z_G)}}{1+\frac{Z}{Z_F(1+Z_B/(Z_F\|Z_G))}}. \tag{6.3}$$

When we simplify the system to a block diagram, as shown in Fig. 6.2b, we can write the output as

$$V_O = V_{IN}A - V_O A\beta, \tag{6.4}$$

which can be rewritten into the loop gain as

$$\frac{V_O}{V_{IN}} = \frac{A}{1+A\beta} = \frac{\frac{Z(1+Z_F/Z_G)}{Z_F(1+Z_B/(Z_F\|Z_G)}}{1+\frac{Z}{Z_F(1+Z_B/(Z_F\|Z_G))}}. \tag{6.5}$$

Continuing from this we see that the direct gain A can be expressed as

$$A = \frac{Z(1+Z_F/Z_G)}{Z_F(1+Z_B/(Z_F \parallel Z_G)}, \tag{6.6}$$

while the feedback ratio β can be expressed as

$$\beta = \frac{Z_G}{Z_G+Z_F} = \frac{1}{1+Z_F/Z_G}. \tag{6.7}$$

The total loop gain can also be approximated by $1/\beta$, and equivalently $1+Z_F/Z_G$ only when A is very large. This is the case if the transimpedance Z is large.

Thus, if one needs a power gain of X, the necessary resistance ratio can be calculated as follows:

$$\frac{Z_F}{Z_G} = G_V - 1 = \sqrt{G_P} - 1 = \sqrt{10^{X/10}} - 1. \tag{6.8}$$

When determining the absolute values of the Z_F and Z_G the recommended values were used when the desired voltage gain aligned with the reported gains in the data sheet. If the desired gain was not found in the data sheet, the value of Z_F of the closest reported gain was used. Z_G was then obtained by dividing Z_F by the desired ratio.

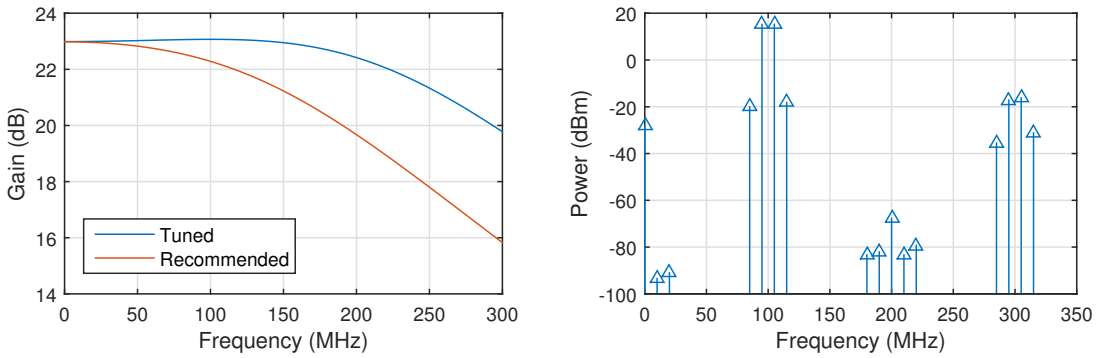
This resulted in gain over frequency characteristics, which at lower frequency obtain the desired gain, but started to decayed at frequencies below the 100 MHz, as can be seen in Fig. 6.3a. This is due to the fact that the direct gain of the CFA is dependent on the transimpedance, which decays over frequency. As such the CFA cannot deliver the right amount of energy to obtain the desired gain at higher frequencies. The direct gain is however also dependent on Z_F. By lowering the value of Z_F, the direct gain increases and thus the bandwidth. Note however that Z_G needs to change with the same factor as Z_F, in order to maintain the same loop gain. To find the value at which the gain was flattest, the tuning capability of ADS was used.

The last design that was fully simulated was for 23 dB gain of which the gain characteristic can be found in Fig. 6.3a. From this figure one can see that the maximal gain difference within a 110 MHz bandwidth is 0.08 dB. From the transient simulation a settling time of about 3 ns was determined. The maximal level of distortion caused by either harmonic or intermodulation is also within the desired bounds, as the largest distortion tone is -31.4 dBc, as shown in Fig. 6.3b.

6.4 Results and Discussion

6.4.1 Implementation

In order to have an amplifier to test the setup with and see whether a repurposed PCB can be used for the pre-amplifier, our daily supervisor has provided one CFA that should have a 25 dB gain. When measuring



(a) Gain (b) Two-tone

Figure 6.3: Simulation results for a 23 dB CFA. (a) Gain with both the recommended and tuned resistor values. (b) Two-tone signal and its harmonic and intermodulation products.

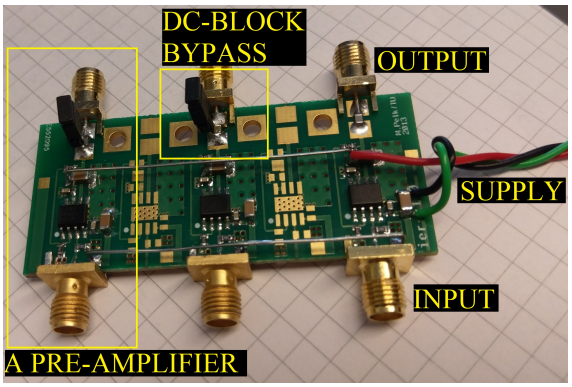


Figure 6.4: Pre-amplifier board including the DC-block bypass pins for 2 of the amplifiers.

the gain of this CFA it was noted that the gain at 100 MHz was in fact 27.5 dB. This, however, was beneficial to us, as the gain of the designed PAs again saw a change to around 20 dB, which thus necessitated a pre-amplifier with a 28 dB gain. Unfortunately, this meant that our own designed CFA has not been produced and instead two more of the provided 27.5 dB gain CFA were made.

All three CFAs were equipped with a DC-blocking capacitance at the output, as the spectrum analyzer cannot withstand a DC-signal. For controlling gate biases, however, this is not desired, as the pre-amplifier is necessary to amplify the bias send by the DAC, which is a low frequency signal. To allow for convenient switching between a DC and non-DC-blocked output, pin headers have been solder at both ends of the capacitor, with which we can bypass the capacitor if need be. In Fig. 6.4 the resulting pre-amplifier board, including these bypass pins, is shown.

6.4.2 Measurement

To evaluate the operation of the pre-amplifier, a frequency sweep was performed, the result of which can be found in Fig. 6.5, by using the signal generator as the source and the spectrum analyzer to measure the output. Chapter 7 covers our work on the spectrum analyzer. As can be seen at lower frequencies the gain approaches 25 dB, as would be expected. At higher frequencies the gain does not behave as expected, as the gain increases by 6 dB before decaying from 115 MHz onwards. Within a 500 kHz span of 100 MHz the greatest gain mismatch is 0.3 dB, which makes it tolerable for our purposes.

The difference between the simulated and actual gain curves could be explained, in part, by not including parasitic elements in the feedback network during simulation, such as a capacitance connecting the inverting input with the ground. Such a capacitance would decrease the impedance Z_G when frequency increases, which results in a higher loop gain, until it is limited by the transimpedance.

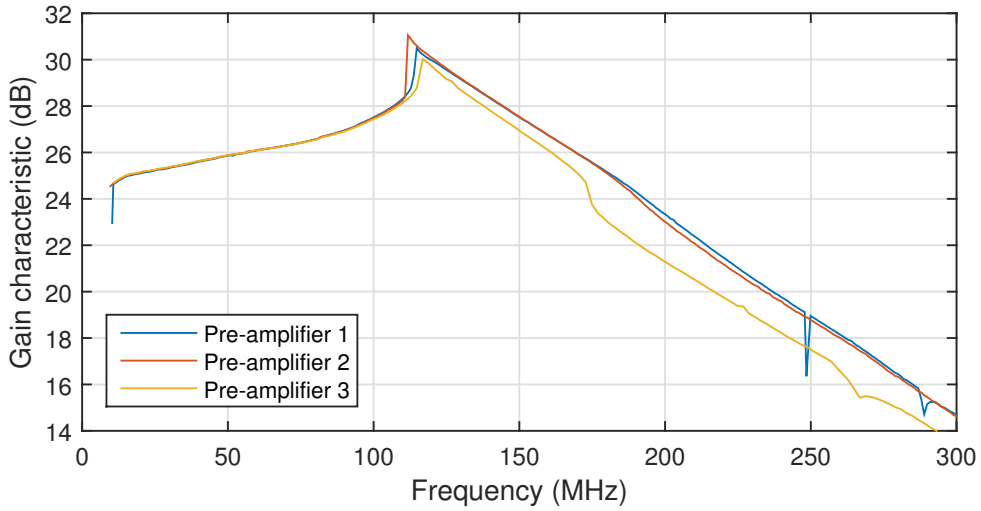


Figure 6.5: Gain over frequency of the pre-amplifiers with a -8 dBm input.

Another explanation for this difference in gain is the mismatch between the output impedance of the pre-amplifier and the input impedance of the measurement setup, including the used cables, which changes over frequency, due to the capacitive and inductive nature of coax cables.

7 | Spectrum Analyzer

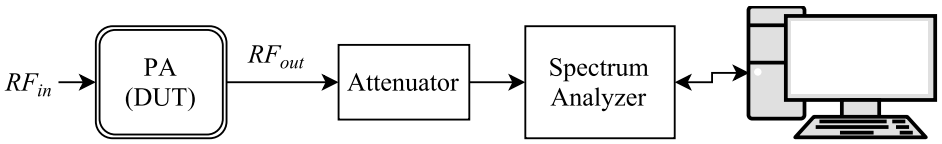


Figure 7.1: Simplified overview of the spectrum analyzer subsytem.

Fig. 7.1 shows a a simplified overview of the spectrum analyzer subsystem, which in essential in PA testing. This chapter briefly addresses our work on the spectrum analyzer, with the most time invested in writing a complete set of control functions.

7.1 Input Conditions

For our purposes the relevant specifications of the power spectrum analyzer (PSA) are the 30 dBm input power limit and the fact that it cannot withstand a DC-signal at its input. Since we need to be able to measure signals with at most 40 dBm power, an attenuator of at least 10 dB needs to be employed. It would also be wise to make use of a DC-decoupler, as to provide absolute certainty that the PSA is not feed a DC-signal.

For these purposes our supervisors provided us with a DC-decoupler with attentuators installed, henceforth addressed as the coupler. Fig. 7.2 depicts the PSA and the coupler connected to each other as part of the PA test system.

The attenuation of the coupler and the cables carrying the signal from the power amplifiers (PAs) were characterized, by connecting the signal generator directly to the spectrum analyzer and measuring the power of the received signal. The connecting circuit consisted of different combinations of the cables (both alone and with others) and the coupler. From this analysis yielded that the coupler and the two connecting cables together have an attenuation of 42.9 dB, for which each cable contributed with 0.1 dB.

7.2 Measurements and Control

To be able to perform measurements automatically and transfer data to a PC, the PC needs to be able to communicate with the PSA. For this 11 functions were made which perform different tasks, but all rely on Standard Commands for Programmable Instruments (SCPI) commands, to control the PSA or request data, which are send over a GPIB-connection.

The functions can be divided in the following categories:

- *Settings:* initialization and alter settings for visualization, traces and markers.
- *Data acquisition:* collecting of data, through traces and markers.
- *One-button measurement:* special measurement routines built-in to the PSA.

We were unfortunately not able to utilize the IQ demodulation mode of the PSA. The cause for this problem is most probably that we did not properly setup the reference signals. Another option would be to use the oscilloscope to this end, but our time was limited. Thus, we do not carry out phase (AM/PM) distorion measurements.

One-button measurements are, as mentioned before, built-in routines that allow the user quickly and easily perform certain measurements. Two such measurements are of use for our measurement programme:

- *Harmonic distortion:* measures the power of a single tone in the given span and that of up to the tenth harmonic of that single tone. The measurement can then return the power and frequencies of each of

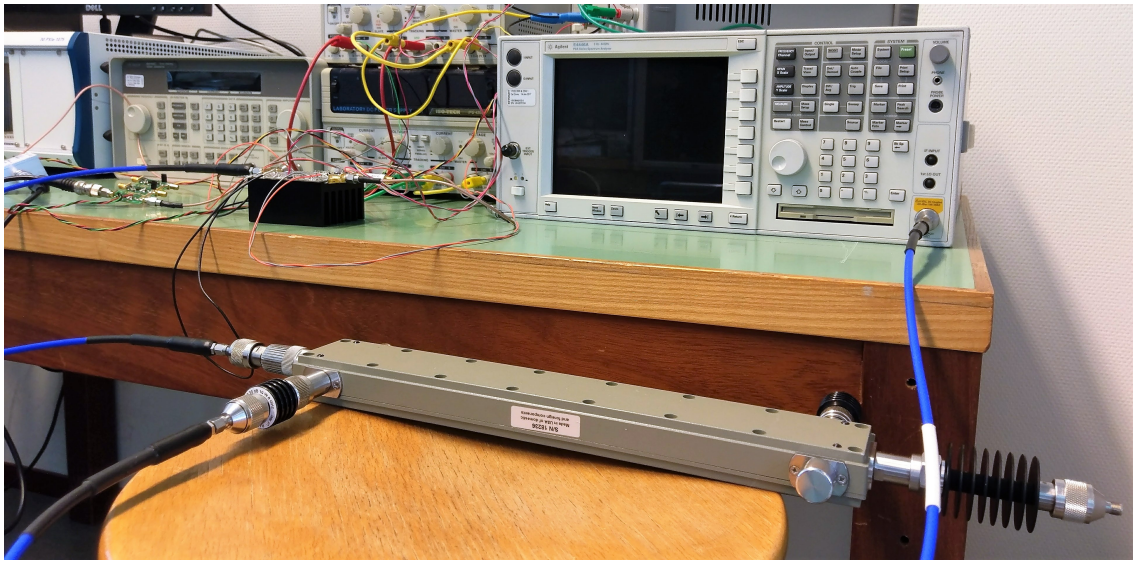


Figure 7.2: Spectrum analyzer and the coupler connected to each other to prevent high power inputs to the spectrum analyzer.

those harmonics or the the total harmonic distortion (THD) in either percentage of the fundamental or dB relative to the fundamental.

- *Intermodulation:* measures the power of two tones of similar strength and that of the third order modulations of those two tones. The measurement can then return the third order intercept point (TOI) calculated from either the upper or lower product or return the worst of either. It can also return the power and frequency of the upper and lower base tones and of the upper and lower intermodulations.

8 Measurement Programme Methodology

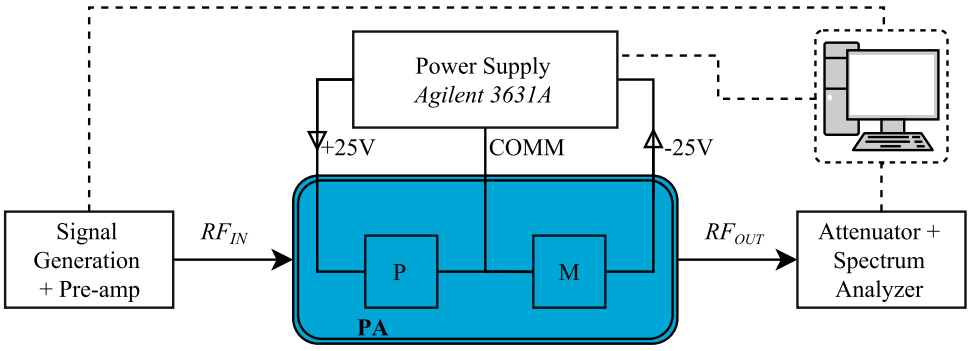


Figure 8.1: Simplified overview of DC power measurement and the PA test system when in measuring and monitoring phase. P and M stand for the peak and main transistors in the interpolating-supply PA family.

Section 3.2 provided a brief overview of the performance metrics in the measurement programme, which are drain efficiency η_D, power-added efficiency η_{PAE}, AM/AM distortion, total harmonic distortion (THD) and intermodulation distortion (IMD). This chapter describes how we approached the measurements of these performance metrics.

8.1 Execution Procedure

The measurement programme was carried out by use of MATLAB graphical user interface (GUI), a picture of which can be found in Fig. 8.2.

The user, using this GUI, will follow the following procedure when executing the measurement:

1. Specify RF_{in} signal type, power range and step size.
2. Initialize measurement equipment.
3. Notify the user to connect the PA for testing. Generate, measure and save the according drive profile, while showing monitoring data on-screen.
4. Load driving profile, execute the measurement, while showing monitoring data on-screen.
5. Process and save all data.

Drive profile generation As detailed in the chapters on signal generation, it was not possible to generate precisely determined RF_{in} signals due to noise and the infeasiblity of calibrating for all possible combinations of analog output channels and IQ modulators.

However the overall gain from the DAC to the output of the pre-amplifier is roughly 7 dB in all cases and allowed us to generate a "drive profile" for each specified range and step size of RF_{in} for PA testing.

The drive profile is generated by *directly* connecting the PA output to the attenuator. The script automatically tries to generate the desired starting RF_{in} power level by iteration. When successful it uses the given step size to generate and measure the subsequent RF_{in}. Finally, the DAC input waveforms and corresponding RF_{in} power levels are stored.

Measuring and monitoring The real PA test takes place during step 4 of the above procedure. The drive profile is loaded and the script step-by-step generates each waveform (and corresponding RF_{in}) contained in the profile. For each step RF_{out} and P_{DC} are measured and plotted on-screen in real-time on the smaller

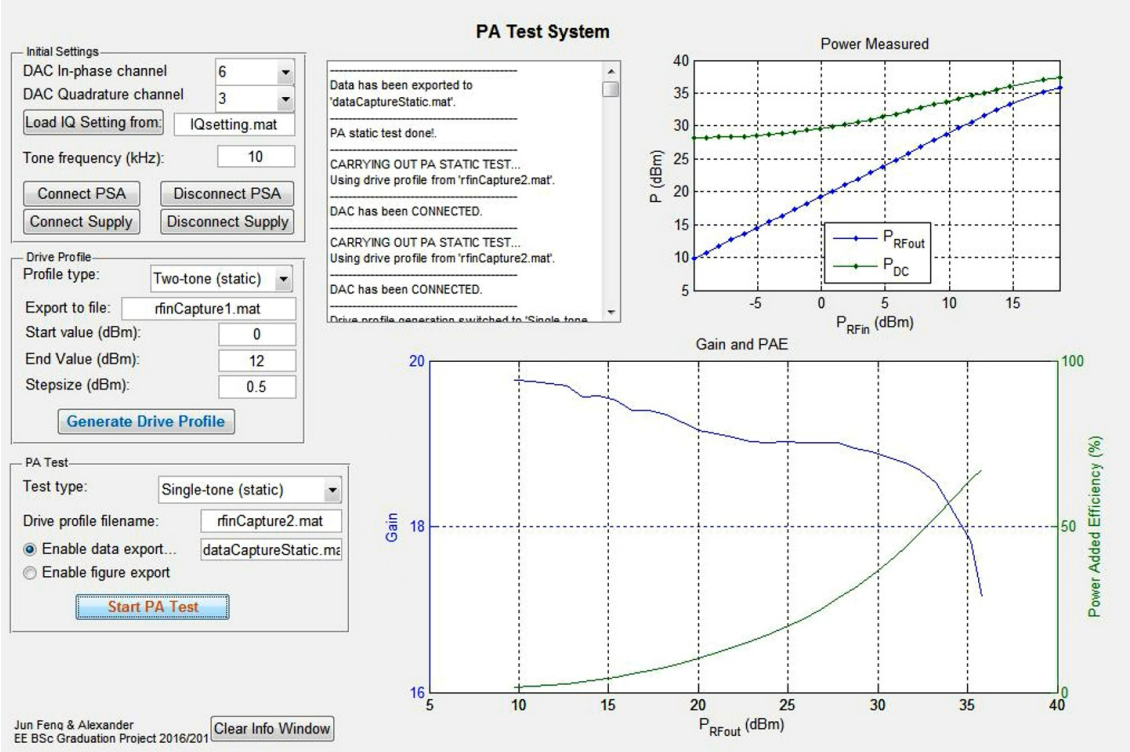


Figure 8.2: PA test system GUI after having performed a gain and efficiency measurement using a single tone.

graph. Depending on the measurement made, either the gain and power added efficiency, the total harmonic distortion and the power of the second harmonic or the third order intercept point are shown in the major graph of the GUI.

Data processing The final phase of the script processes the measurement data to obtain gain and efficiency plots and saves these plots and the data for the PA designers.

8.2 Power Measurement

There are three power levels that need to be measured, in order to determine η_D, η_{PAE} and AM/AM distortion (gain), that is, P_{RFin}, P_{RFout} and P_{DC} are required put forward in Section 3.2. In this section these different power levels and the method with which they are measured will be discussed.

8.2.1 PA RF Input Power

Before anything sensible can be said about the PA, one needs to know what power P_{RFin} is given to the input of the PA. As this parameter cannot be measured easily during a measurement without interfering with the operation of the PA, this will need to be measured before it is supplied to the PA. To this end the signal coming from the pre-amplifier is first measured, by using the power spectrum analyzer (PSA). The power of the supplied tone (or tones) is then measured resulting in a so-called “drive profile”.

8.2.2 PA RF Output Power

Once P_{RFin} is known, we can compare it with the output power P_{RFout} in order to analyze gain as defined in Section 3.2. P_{RFout} is measured the same way as the input power, but now the output of the PA is connected to the spectrum analyzer, and the output of the pre-amplifier to the input of the PA.

8.2.3 PA Drain DC Power

To investigate the efficiency of the PA, one needs to know how much power is entering the PA, which is obtained by measuring the voltages and current supplied to the drain(s) of the PA.

The Agilent power supply used in our testing system can measure those quantities and can also communicate with the PC via a GPIB-connection. The PC can control the output and request the measured data by using once again Standard Commands for Programmable Instruments (SCPI) commands. Fig. 8.1 shows the drain power supply connections in our PA system for interpolating-supply PAs.

8.3 Distortion

The PA linearity influence the signals in multiple ways and in order to understand what these effects are on an arbitrary signal, we want to measure these distortions.

8.3.1 Total harmonic distortion (THD)

THD, defined in Section 3.2, is the creation of tones at multiples of the original tone. This will be measured by using the *harmonic distortion* measurement functionlity of the spectrum analyzer, as discussed in Section 7.2.

8.3.2 Intermodulation distortion (IMD)

The last form of distortion covered by this measurement programme is the introduction of 3rd-order intermodulation tones due to the two tones in the original signal applied to a nonlinear PA (Section 3.2). The strength at which these tones are introduced by the PA, is described by the third order intercept point (TOI or IMD3), which is measured by use of the *intermod* measurement functionality of the spectrum, as discussed in Section 7.2.

8.4 Final PA Test Setup

Fig. 8.3 depicts the final PA test system hardware in real life. The subsystems labeled subsystems are as follows:

1. PC running MATLAB scripts (GUI)
2. Baseband DAC + LC filter
3. IQ modulator
4. Pre-amplifier
5. PA under test
6. Attenuator (coupler)
7. Spectrum analyzer
8. Controlled power supply
9. Oscilloscope

The next chapter discusses on the results achieved with the PA test system.

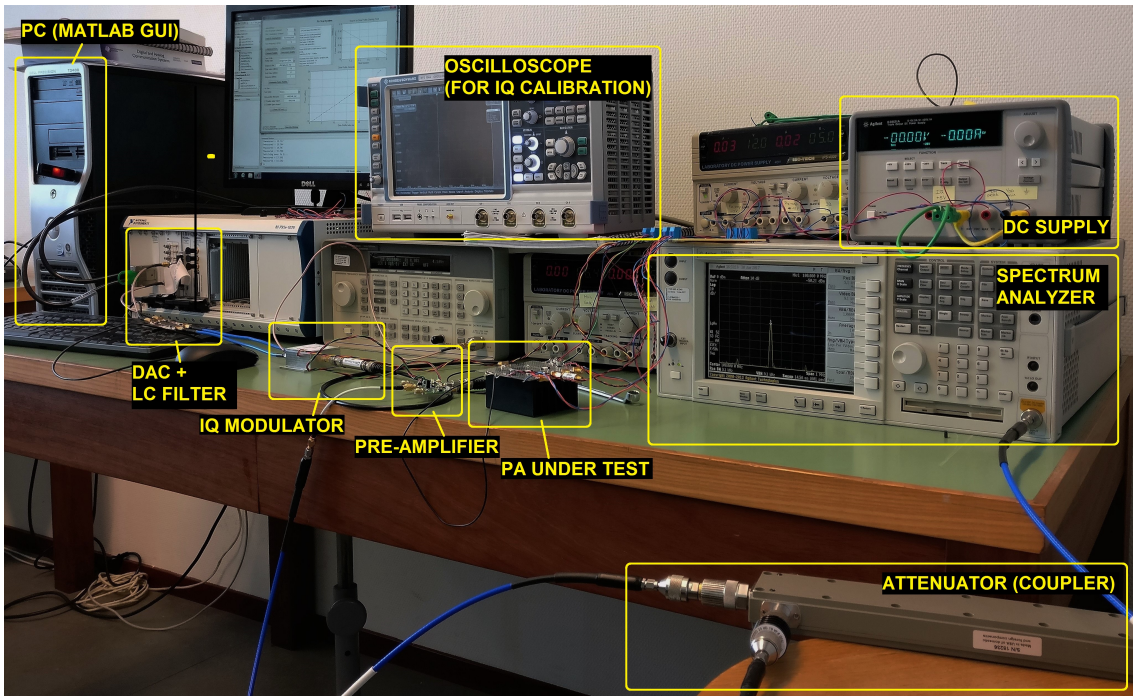


Figure 8.3: Final PA test system hardware with each subsystem designated.

9 PA Test Results and Discussion

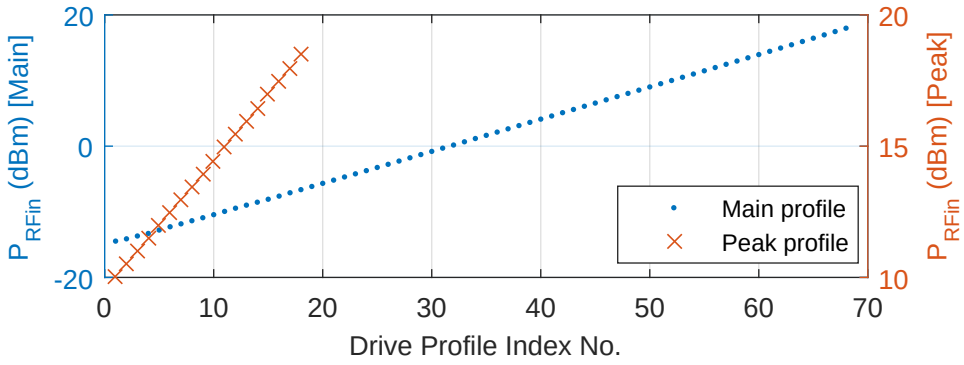
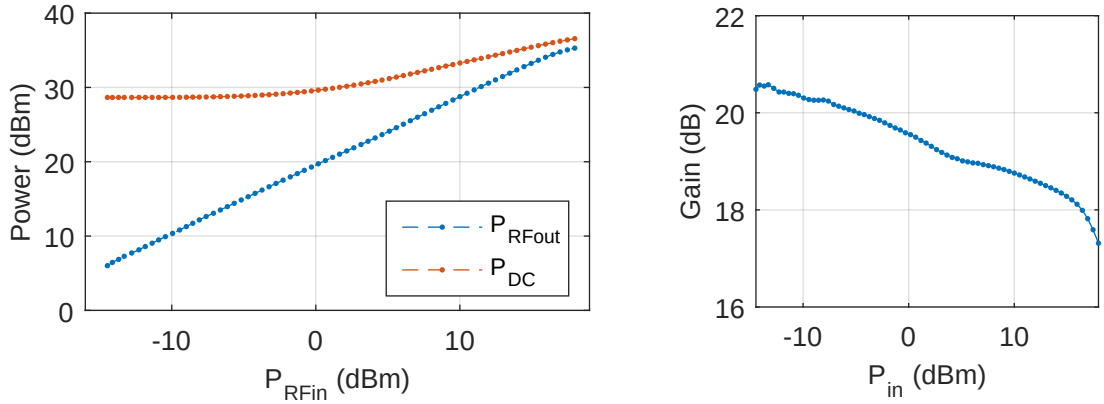


Figure 9.1: Two drive profiles generated for a PA operating in nominal (main) or peak power modes.



(a) Power

(b) Gain

Figure 9.2: PA [2] test results using the main drive profile in Fig. 9.1. (a) Monitored RF_{out} and DC power. (b) Corresponding computed gain.

The PA test system and the measurement programme as overviewed in Chapter 3 and Chapter 8 were employed to evaluate two interpolating-supply power amplifiers (PAs) [2, 3] designed and assembled as part of the overall project. A total of 21 static tests were performed. This chapter presents several measurement results achieved with the PA test system and discusses upon these results.

9.1 Basic Generation and Measurement

Fig. 9.1 depicts two of the drive profiles generated during PA testing after range and step size specification of P_{RFin} by the PA designers. The script finds the first desired drive profile value within a 0.025 dB accuracy margin. The subsequent drive profile samples taken were unfortunately not as accurate, differing by ≈ 0.5 dB, due to signal-dependent gain in the input path. We could resolve this by having the script reiterate for each drive profile sample: this trade-offs time for accuracy.

Fig. 9.2 shows the monitored RF_{out} and DC power during one of the PA test as well as the corresponding gain characteristic derived. Fig. 9.3 shows the resulting efficiency measurement from the drive profile and power data: $\eta_{PAE} < \eta_D$ as expected. In most cases, the PA designers agreed that the results were realistic. The next section compares the gain and efficiency results in more detail.

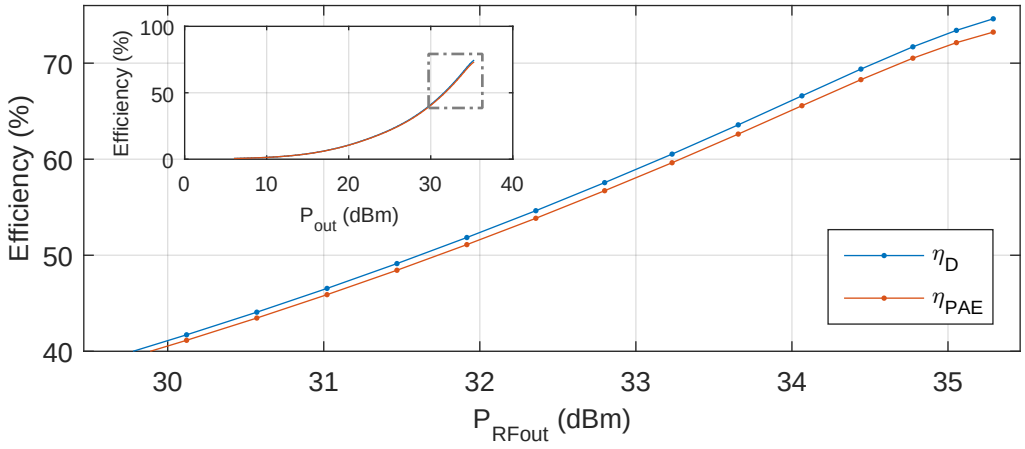


Figure 9.3: Results for efficiency following from the test in Fig. 9.2. The mini-figure shows the corresponding full efficiency characteristic.

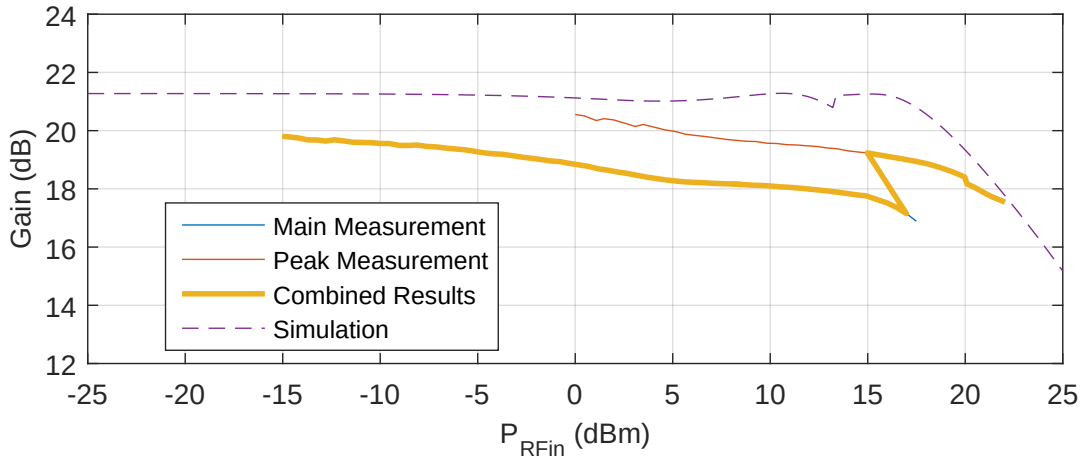


Figure 9.4: Comparison of gain measurement and simulation for a varying bias interpolating supply PA biased at 28 V peak transistor drain voltage.

9.2 Comparison with PA Simulation

We compared simulation results from the PA designers with the measurement results they obtained with the use of our PA test system. In this section we compare the gain and drain efficiency results for the varying bias interpolating supply power amplifier biased at 28 V for the peak transistor.

The gain comparison shown in Fig. 9.4 reveals a deviation up to 3 dB. The deviation does not seem to be a systematic offset, however a lowered gain in the measurement suggests that our pre-measured input power (the drive profile) might be higher than actually fed to the PA when under test caused by mismatch between the pre-amplifier and PA under test. The PA designers suspect that temperature variations and non-ideal losses are possible causes too. In any case, the input power can be measured more precisely in real-time using another coupler at the PA input.

The drain efficiency comparison shown in Fig. 9.5 reveals that the main transistor measurement closely matches the simulations. This also holds for the power added efficiency. For the peak transistor however, we see a roughly 10% difference at 40 dBm output. There is a small chance that this deviation is due to the PA test system, since the main transistor is measured in the same way. We still need to further discuss this phenomenon with the PA designers.

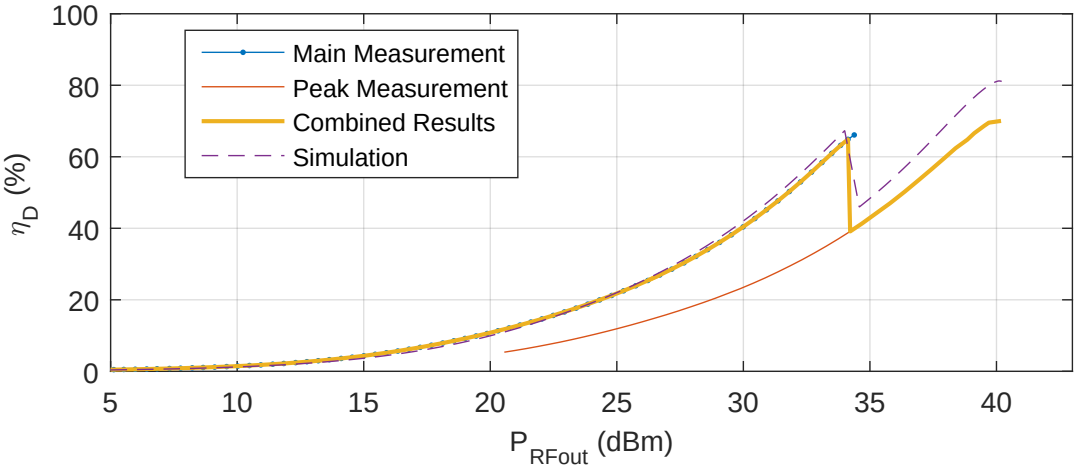
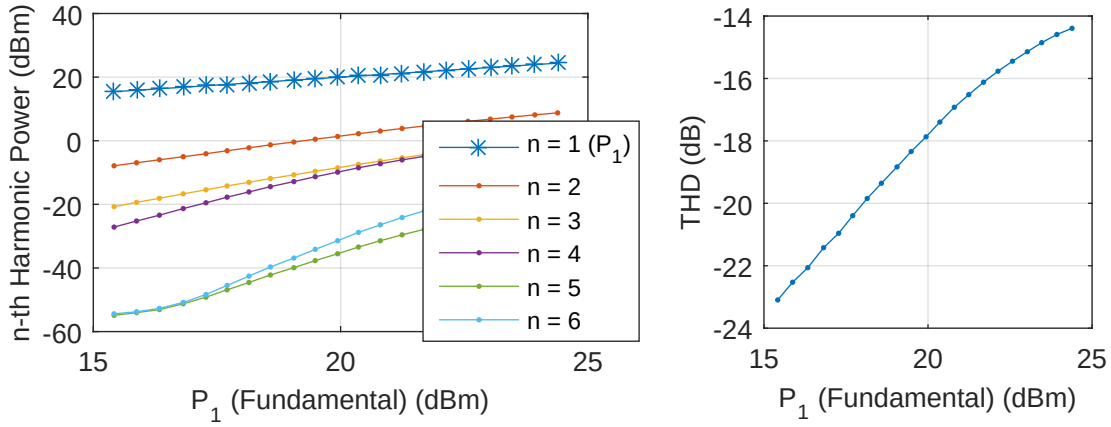


Figure 9.5: Comparison of drain efficiency measurement and simulation for a varying bias interpolating supply PA biased at 28 V peak transistor drain voltage.



(a) Harmonics

(b) THD

Figure 9.6: THD results, P_1 is the fundamental (100 MHz) output power. (a) Power of harmonics. (b) THD.

Comparisons with results at different biasing values for this PA show similar deviations. In the limited time, we did not yet evaluate result comparisons for the other interpolating supply PA.

9.3 THD

The THD measurement proved to be slow as we measure up to the 10th harmonic. Results for the main transistor for the varying bias PA are shown in Fig. 9.6. The output power range was kept small and the spectrum analyzer did not switch from attenuator. We could not compare results with simulations as THD was not of great interest for the design teams, but the distortion increases for increasing input powers as expected.

9.4 IMD

In the limited time, we only performed single-transistor IMD measurements, with a dynamic range of -18 to 14.3 dBm input power. Thus, we did not dynamically switch between the transistors of the PA under test.

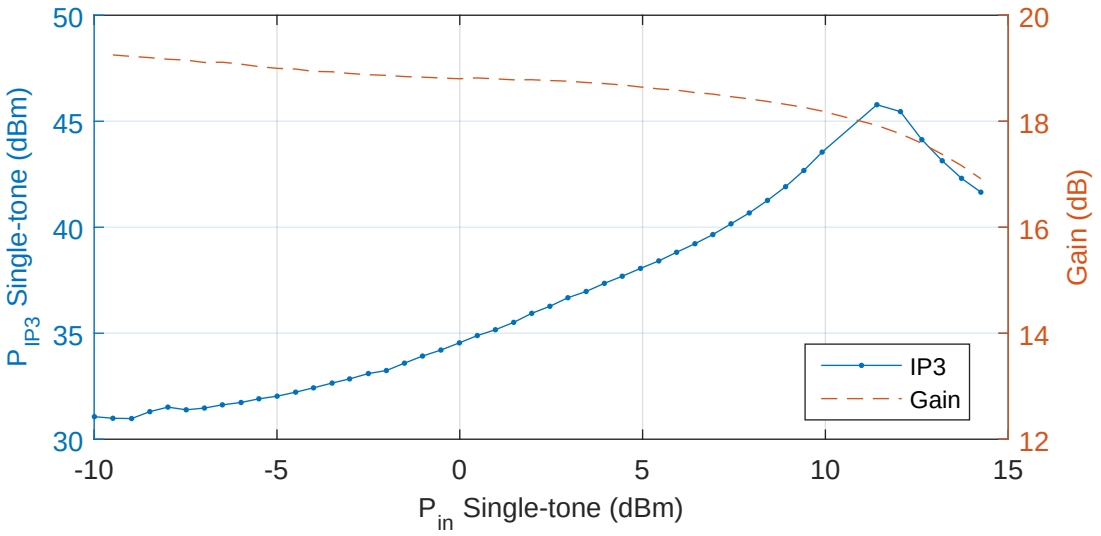


Figure 9.7: IMD measurement for the main transistor of the varying bias interpolating supply PA biased at 28 V peak transistor drain voltage.

Additionally, we could not obtain comparable simulation results for the IMD measurements carried out. We consequently used the gain measured during the IMD measurement for verification.

The IMD measurement shown in Fig. 9.7 shows an increasing P_{IP3} for the main transistor of the varying bias PA. This is as expected since more power is lost in higher-order products and the 3dB per dB assumption for the 3rd-order product does not hold for large signal behaviour. When compression starts we see that P_{IP3} drops: the 1dB/dB growth for the fundamental tone no longer continues. We could not create a larger input power for two-tones unfortunately, to observe an extended IMD characteristic. Still, the obtained IMD vs. gain characteristic was as expected, such that the measurement system performed IMD measurements convincingly.

10 | Conclusion and Future Work

10.1 Conclusion

A radio frequency power amplifier (RF PA) test system compatible with the interpolating-supply PA family has been developed. The automatized RF PA test system was put into use, resulting in performance measurement and characterization of two-transistor interpolating-supply PAs detailed in [2, 3] with respect to static linearity and efficiency.

The intended PA device performance specifications (20 dB gain at 40 dBm-output and 100 MHz), availability of hardware and the assembled PA test system requirements lead to a semi-automated PA test system with top-level control through MATLAB. The deemed necessary subsystems are baseband and RF signal generation, the pre-amplifier stage and implementation of the measurement programme, which includes remote control of signal generation and measurement hardware.

A designed low-pass LC filter in the baseband signal generation subsystem was constructed to reduce peak-to-peak noise from the DAC buffer board from 10 mV to 2.4 mV. Additionally, an automated procedure utilizing an remote-controlled oscilloscope successfully performed IQ modulator calibrations at 100 MHz, reducing LO leakage and undesired sidebands exceeding data sheet specifications. The IQ calibration was finalized in the form of a graphical user interface (GUI) for automation.

Single-stage, 27.5 dB-gain pre-amplifiers were designed and constructed to ensure that a sufficient P_{RFin} of 21.5 dBm could be achieved for PA testing at 100 MHz.

The desired PA P_{RFin}, P_{RFout} and P_{DC} power levels could be measured using a remote controlled 44 GHz spectrum analyzer and DC power supply, by using Standard Commands for Programmable Instruments (SCPI) over a GPIB-connection initiated in MATLAB. RF_{in} was attenuated by 42.9 dB using a coupler to not overload the spectrum analyzer.

The measurements of the PA test system could be run automatically from a top-level MATLAB script once the system had been set-up, with the exception of a need for human interaction in order to change the setup from either measuring RF_{in} or RF_{out}, as these two signals cannot be measured simultaneously without interfering with the operation of the PAs. For this reason drive profile generation is included in the top-level script. The PA test systems also presents the data in real-time for monitoring purposes.

The PA test system is also accessed through a GUI and proved to be able to automatically determine PA gain (distortion), drain efficiency and power-added efficiency in a total of 21 static tests over differing P_{RFin} ranges. The measurement results were deemed realistic by comparisons to simulations. The PA test system is also capable of measuring total harmonic distortion (THD) and intermodulation distortion (IMD) for single-transistor stages.

The phase distortion was not implemented as we were not able to resolve problems with synchronizing (triggering) the spectrum analyzer. Therefore, all primary requirements are fully met except for the phase distortion characterization which was not realized. In addition to this, both IQ calibration and PA test system were successfully automatized by means of GUIs.

10.2 Future Work

A next-generation version of the PA test system addressed in this thesis can have improvements at both functionality and subsystem levels when compared to the current version.

Functionality A first would be to complete the requirements not met, namely implementing the capability of measuring the phase distortion, which could be done by looking into the IQ-demodulation employed by the spectrum analyzer used in this project or by using a different piece of equipment, which would be able to directly measure the phase shift of the signal such as a vector network analyzer. This would require another set of MATLAB scripts for remote control.

Another requirement that could be resolved is the capability to generate and measure dynamic performance for a quadrature amplitude modulation (QAM) signal. QAM-type modulation is in particular interesting for interpolating-supply PAs as this modulation scheme utilizes a discrete number of envelope amplitudes. For this a driving procedure would need to be implemented and a measurement procedure set-up, which would, amongst other things, measure the constellation points and the error vector magnitude.

Signal generation Currently one has to invest time in calibrating the IQ modulation to prevent, amongst other things leakage of the local oscillator. This can be omitted by performing the IQ modulation in the digital domain, as there it can be performed almost without errors, as you are limited by the constraints of the data type and the resolution of the DAC. This would require an signal generator which can directly produce samples at at least twice the desired carrier frequency, such as the earlier mentioned PXIe-5450 from National Instruments, which has a sample rate of 400 MSa/s.

If one keeps the current DAC, the performance related to it can still be improved. Due to the large noise introduced by the buffer, 10 mV rms, which is also amplified by the pre-amplifier, the testing system cannot produce a desired 10 mV exact bias signal. To lower the noise, the buffer could best be replaced with a device with lower noise.

Another solution to produce the desired bias signals, is to remove the attenuation, for at least some of the analog outputs, as this would increase the voltage range from around -200 to 200 mV, to -10 to 10 V, which would eliminate the need for the pre-amplifier for generating the bias signals, which leads to a noise level much closer to the desired 10 mV. However, a solution then has to be implemented for the limited driving capability of the current DAC.

Pre-amplifier and pre-distortion One could also aim at improving the pre-amplifiers by reducing the distortion introduced by it, increase the gain of it and, if one wants to measure at higher frequencies, increase the bandwidth of it. Distortion could be decreased either by accepting the non-linearity of the pre-amplifier and employing digital pre-distortion techniques to correct for it, design of a new topology, or selecting a different device, which would reduce the non-linearity of the pre-amplifier itself, after which pre-distortion techniques could still be employed to further reduce the effect of per-amplifier non-linearity.

To allow the system to measure power amplifiers (PAs) with lower gains or generate greater power levels with them, the gain of the pre-amplifier would need to increase to accommodate for that. This could also be done by designing a different topology or selecting a different device. Note, however, that if higher power levels need to be measured, one must also take into account the power rating of the coupler, as the coupler in the current setup is rated for a 20 W maximal input power.

Finally, as the gain of the current design falls below the designed gain from around 170 MHz onwards, the pre-amplifier is a bottleneck for high-bandwidth testing. To flatten the gain the best solution would be selecting a different device, as the THS3091 device currently in use is already approaching its gain-bandwidth limit.

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Appendices

A List of Hardware

- Agilent 82357B (USB/GPIB interface)
- Agilent 8648C (signal generator)
- Agilent E3631A (remote controlled power supply)
- Agilent E4446A (spectrum analyzer)
- Custom Anteverta-mw bufferboard
- HP 778D-011 (dual directional coupler)
- Iso-Tech IPS-4303 (power supply) *Twice*
- Mini-Circuits BW-N20W20+ (attenuator)
- Mini-circuits BLP-100+
- NI PXI-6733
- NI PXIe-1075 (18-Slot 3U PXI Express Chassis with AC)
- NI PXIe-8381 (MXI-Express Gen II x8)
- Radiall R415720000 (attenuator) *Twice*
- TI THS-3091 (op-amp) *Thrice*
- TI TRF370417 (IQ modulator) *Twice*
- Windows PC with Matlab 2013b