Hybrid Space Vector Modulation Scheme for the Multiport Hybrid Converter

Stecca, Marco; Abdelhakim, Ahmed; Soeiro, Thiago Batista; Canales, Francisco; Bauer, Pavol; Palensky, Peter

DOI
10.1109/TPEL.2022.3201264

Publication date
2023

Document Version
Final published version

Published in
IEEE Transactions on Power Electronics

Letters

Hybrid Space Vector Modulation Scheme for the Multiport Hybrid Converter

Marco Stecca, *Member, IEEE*, Ahmed Abdelhakim, *Senior Member, IEEE*, Thiago Batista Soeiro, *Senior Member, IEEE*, Francisco Canales, Pavol Bauer, *Senior Member, IEEE*, and Peter Palensky, *Senior Member, IEEE*

***Abstract*—This work proposes a hybrid space vector modulation (HSVM) scheme for multiport hybrid converters (MHCs). Moreover, the impact of shifting the auxiliary currents from the main ones is proposed and investigated in order to enhance the converter efficiency. The proposed operational schemes have been implemented in a three-phase 5 kW MHC prototype. It is shown that the proposed HSVM scheme can improve the MHC efficiency by 0.3% at full load with respect to space vector modulation. At partial loads, the improvement is even more significant, reaching +0.7% at 30% of the rated power. A further 0.15% increase in efficiency at full power can be achieved by a 180° phase shifting of the auxiliary currents with respect to the main terminal currents, reaching a peak efficiency of 98.5%.**

***Index Terms*—Hybrid space vector modulation (HSVM), multiport hybrid converter (MHC), voltage source converter (VSC).**

I. Introduction

MULTIPLE ac grids or loads can be interfaced to a common dc grid or generation system by several dedicated voltage source converters (VSCs) [1]. Interestingly, as discussed in [2], a single multiport converter can be used to replace those several VSCs of the multiterminal grid. This configuration is particularly advantageous when the system is designed to supply the majority of the dc power to an individual ac terminal, while the remaining ac terminals are mostly comprised of auxiliary loads. This condition is commonly found, for example, in electric traction applications, e.g., electric ships and trains, and high-power medium voltage dc (MVDC)-based distribution systems featuring energy hubs, and micro and nanogrids [2].

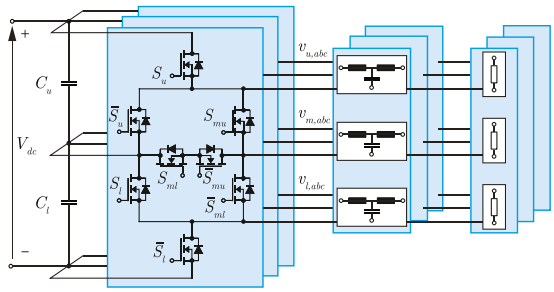

Fig. 1. Circuit schematic of a three-phase multiport hybrid converter (MHC) supplying three separate loads.

Examples of a single converter multiport implementation are found in [1] and [3]. These works use a nine-switch converter, which can feed two independent ac loads, and it is derived by adding a single switch in series with each half-bridge leg of a three-phase, two-level VSC. However, previous literature has shown that three-level topologies are a better solution than two-level VSC in terms of efficiency, power density, and operating costs in high-power and high-voltage implementations [4], [5]. In this context, the multiport hybrid converter (MHC), which is a three-port converter based on the three-level active neutral point clamped (ANPC), has been proposed in [2]. The MHC circuit topology is shown in Fig. 1. As can be noticed, this MHC is built by adding two switches per phase-leg to the ANPC structure. In this way, the MHC allows the utilization of lower voltage class semiconductors and, therefore, better switch loss performance becomes possible. The MHC operation has been presented in [2] and [6], where the outputs are modulated with space vector modulation (SVM).

This letter proposes two modulation schemes that aim at enhancing the efficiency of the MHC proposed in [2]. First, a hybrid space vector modulation (HSVM) scheme specially designed for the MHC is presented. This HSVM method fulfills the MHC operating requirements, which dictates that the output modulation waveforms for each individual ac terminals do not intercept the ones of the other ac terminals. Second, a scheme foreseeing the phase shifting of the auxiliary ac terminals' currents with respect to the currents at the ac terminal processing the main system power is presented. This scheme allows the

Manuscript received 9 June 2022; revised 28 July 2022; accepted 8 August 2022. Date of publication 24 August 2022; date of current version 10 October 2022. *(Corresponding author: Marco Stecca.)*

Marco Stecca, Pavol Bauer, and Peter Palensky are with the Electrical Sustainable Energy Department, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: m.stecca@tudelft.nl; p.bauer@tudelft.nl; p.palensky@tudelft.nl).

Ahmed Abdelhakim is with the Department of Energy Conversion, ABB Research Sweden, 72178 Västerås, Sweden (e-mail: ahmed.abdelhakim@se.abb.com).

Thiago Batista Soeiro is with the Power Electronic & EMC Group, University of Twente, 7522 NB Enschede, The Netherlands (e-mail: t.batistasoeiro@utwente.nl).

Francisco Canales is with the Power Electronics Department, ABB Research Switzerland, 5405 Baden, Switzerland (e-mail: francisco.canales@ch.abb.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3201264.

Digital Object Identifier 10.1109/TPEL.2022.3201264

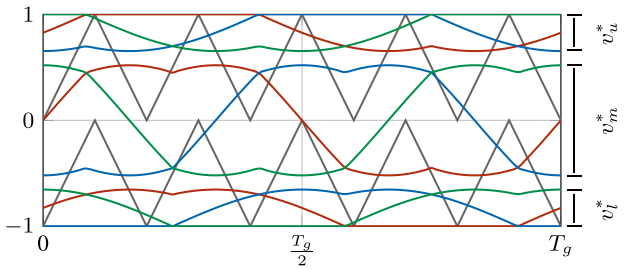

Fig. 2. Proposed HSVM modulation scheme for a three-phase MHC during one fundamental period T_g. v_u^*, v_m^*, and v_l^* are the modulation waveforms for the upper, main, and lower output, respectively, and the two sawtooth waveforms are the carrier signals.

TABLE I
MHC STATES AND REQUIRED ON SWITCHES TO ACHIEVE THEM CONSIDERING PHASE-a. NOTE THAT THE STATES OF THE REMAINING SWITCHES ARE NOT CONSIDERED IN THIS TABLE

Output	State	Required ON switch(es)
v_u	V_{dc}	S_u
	$V_{dc}/2$	$\overline{S}_u$
v_m	V_{dc}	$S_u + S_{mu}$
	$V_{dc}/2$	$S_{ml} + \overline{S}_{mu}$
	0	$\overline{S}_l + \overline{S}_{ml}$
v_l	$V_{dc}/2$	S_l
	0	$\overline{S}_l$

reduction of the MHC power losses further by reducing the rms currents across some of the MHC's semiconductors. The proposed HSVM schemes have been tested in a three-phase 5 kW MHC laboratory prototype under various load conditions.

The rest of this article is organized as follows. Section II reviews the MHC operation and introduces the proposed hybrid modulation schemes. Section III describes the experimental verification of the proposed modulations. Finally, Section IV concludes this letter.

II. MHC Operation and Proposed Hybrid Modulation

The MHC main load can be modulated using any continuous modulation scheme suited for the conventional ANPC converter. In addition, two extra sets of reference signals have to be utilized for the modulation of the upper and lower auxiliary loads, as shown in Fig. 2. The MHC is operated with S_x as complementary of $\overline{S}_x$, where $x = u, l, mu, ml$, as indicated in Fig. 1. The possible states of the three MHC outputs and the switches which are required to be ON to achieve these switches are listed in Table I. Note that the states of the remaining switches are not considered in this table. To ensure the MHC proper operation, v_u^* and v_l^*, which are the modulation waveforms of the upper and lower auxiliary outputs, cannot intersect with v_m^*, which is the modulation waveform of the main output. This condition guarantees that S_u or S_l are ON whenever needed by the main load. If this condition is not respected, the auxiliary outputs' voltage and current would get distorted, and therefore, the MHC does not operate properly [2]. This can be particularly challenging in motor drives applications where the main load can operate with different frequencies than the auxiliary switches, posing a limit to the maximum modulation index each load can operate.

The MHC feeds a main load and two auxiliary loads. During the operation, the auxiliary loads can consume different powers, which results in unbalance between the dc-link capacitors. This unbalance can be corrected by introducing a bias factor δ to the main output modulation waveform v_m^* [2]. Note that to avoid any disturbance in the MHC operation, which might occur if the reference signals intersect with each other, the following constraint has to be guaranteed:

$$(M_m + M_l + M_u + 2\delta_{\max}) \leq 1 \tag{1}$$

where M_m, M_l, and M_u, are, respectively, the modulation indices of the main load, upper auxiliary load, and lower auxiliary load, and $\delta_{\max}$ is the maximum bias factor at the worst-case unbalance scenario between the auxiliary loads. The modulation indices are calculated by

$$M_i = \frac{2 \cdot v_i}{V_{\text{dc}}} \tag{2}$$

where v_i is the peak ac phase voltage and i indicates the three MHC outputs.

In terms of modulation strategy, SVM is generally preferred among the continuous modulation methods of VSCs, due to its higher dc-link voltage utilization and simplicity of implementation [7]. The MHC operating with SVM has been discussed in [2]; therefore, this article focuses on the proposed HSVM method for modulating the MHC.

A. Hybrid Space Vector Modulation

Discontinuous pulsewidth modulation (DPWM) schemes for the modulation of three-phase VSCs have been proposed to reduce their semiconductors' switching losses [8]. These mainly consist of cyclically clamping one of the three phase-legs either to the positive or to the negative dc rails, while controlling the generated ac terminal voltage by switching the other two remaining phase-legs. In this way, the semiconductors of the clamped leg do not switch during the entire period, but only during a fraction of it, reducing the overall switching losses. DPWM methods have already been proposed for various VSC topologies, but not for the MHC.

As previously mentioned, the MHC operation does not allow the intersection of the modulation waveforms of the various outputs, which poses a limitation for the implementation of typical DPWM methods in the MHC. In fact, the main T-type module cannot be operated with DPWM in a motor drive application; otherwise, during the clamping time, v_m^* would intersect with v_u^* and v_l^*. However, the two auxiliary outputs need to be clamped at different dc rails, since they need to be positioned at the top and the bottom of the main modulation waveforms. More specifically, as illustrated in Fig. 2, v_u^* can clamp at +1, while v_l^*, at -1. Consequently, the upper output can be operated with maximum DPWM (DPWM MAX), the main output with SVM, and the lower output with minimum DPWM (DPWM MIN). In this way, the upper and lower output only clamp in one state, +1 and -1, respectively, avoiding crossing with v_m^*. This set of modulation schemes constitutes a HSVM method that is suitable for the MHC. The HSVM method allows the proper operation of the MHC and, at the same time, reduces the MHC

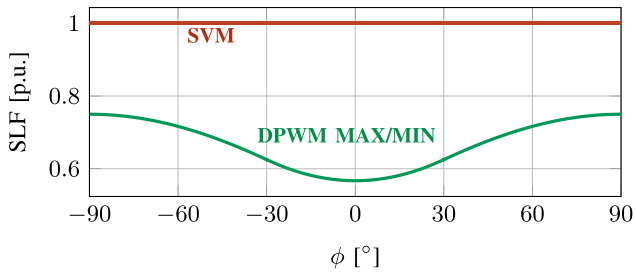

Fig. 3. SLF of SVM, DPWMMAX, and DPWMMIN. Note that discontinuous modulation methods can be used only in the auxiliary outputs.

switching losses. An example of the reference signals for the MHC operating with HSVM is shown in Fig. 2.

The HSVM method does not impact the main output, since this is still operated with SVM; however, the auxiliary ports will see a reduction of the switching losses since they are DPWM modulated. Considering the auxiliary outputs, which are two-level modulated, the average switching power loss per device over a fundamental period can be defined as

$$P_{\text{sw}} = \frac{V_{dc}}{2\pi V_b} f_{\text{sw}} E_{\text{on,off,rr}} \int_0^{2\pi} \left| i\left(\omega_e t\right) \right| \mathrm{d}\omega t \tag{3}$$

where V_b represents the datasheet reference voltage, f_{sw} the switching frequency, $E_{\text{on,off,rr}}$ is a combined switching loss value per commutation for a specified dc voltage and output current, and $i(\omega_e t)$ equals zero in the intervals where no switching occurs and equal to the phase current otherwise. Equation (3) can be normalized to its value for SVM ($2V_{\text{dc}} f_{\text{sw}} \hat{I} E_{\text{on,off,rr}} / \pi V_b$), with $\hat{I}$ the peak line current, resulting in the switching loss function (SLF), which for the DPWMMAX and DPWMMIN methods is derived as follows [8], [9]:

$$\text{SLF} = \begin{cases} \frac{1}{2} - \frac{1}{4}\sin\varphi & -\frac{\pi}{2} \le \varphi \le -\frac{\pi}{6} \\ 1 - \frac{\sqrt{3}}{4}\cos\varphi & -\frac{\pi}{6} \le \varphi \le \frac{\pi}{6} \\ \frac{1}{2} + \frac{1}{4}\sin\varphi & \frac{\pi}{6} \le \varphi \le \frac{\pi}{2} \end{cases} \tag{4}$$

where φ is the phase shift between the output voltage and current. The SLF is shown in Fig. 3 in the full φ range, where it can be seen that the DPWM MAX and DPWM MIN allow a reduction of up to 40% of the switching losses compared with conventional SVM at full power factor.

It has to be noted that the two-level modules' switches (S_u, $\overline{S}_u$, S_l, and $\overline{S}_l$) suffer switching losses only according to the auxiliary currents. This occurs because the two carriers of Fig. 2 guarantee that the switching action of S_u and $\overline{S}_u$ only occurs when the S_{mu} is OFF, and therefore, the switching happens when the upper two-level module is only feeding the upper load and not the main load. The same reasoning can be extended to the lower two-level module and its switches.

The switching losses distribution among the switches of phase-a derived through the circuit simulator is shown in Fig. 4. In the simulation, V_{dc} is set to 800 V, the line frequencies $f_{g,u}$, $f_{g,m}$, and $f_{g,l}$ are 50 Hz, and the switching frequency f_{sw} is 18 kHz. The voltages of the auxiliary outputs are set to 80 V, the main output terminal to 380 V, and the MHC is operating at full power factor. Fig. 4 displays the switching losses of the

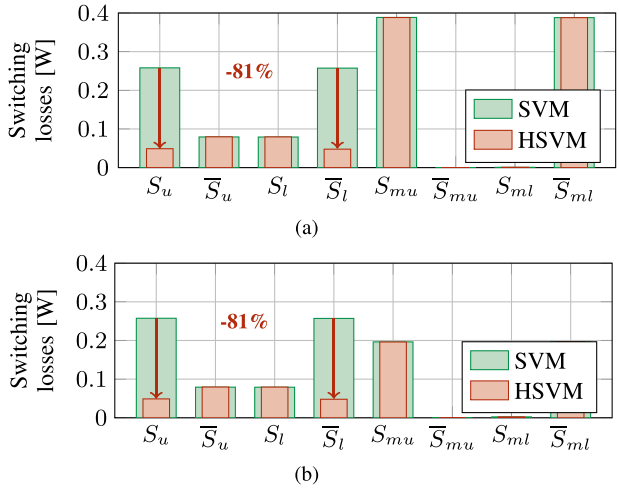

Fig. 4. Switching losses distribution among the individual switches of phase-a when the MHC operates with SVM and HSVM while supplying (a) 2 × 300 W auxiliary loads and a 4.4 kW main load, and (b) 2 × 300W auxiliary loads and a 2.2 kW main load.

individual switches when the MHC operates under SVM and HSVM. Two operating points are considered, Fig. 4(a) is relative to when the MHC supplies 2 × 300 W auxiliary loads and a 4.4 kW main load, and Fig. 4(b) when the MHC supplies 2 × 300 W auxiliary loads and a 2.2 kW main load. It can be seen that the switching losses of S_u and $\overline{S}_l$ are reduced by 81%, leading to an overall reduction of 60% in the two-level operated switches. Note also that the change in loading in the main output, from Fig. 4(a) and (b), only impacts the switching losses in the T-type module switches (S_{mu}, $\overline{S}_{mu}$, S_{ml}, and $\overline{S}_{ml}$). This shows that the two-level module switches suffer switching losses only according to the auxiliary load currents, as previously explained.

Another important metric for the benchmarking of modulation methods is the harmonic distortion at the output. The harmonic distortion functions (HDF) of SVM, DPWM MAX, and DPWM MIN, which are indicators of the waveform quality and harmonic losses, are shown in Fig. 5 as a function of the modulation index M_i, following the derivations presented in [8], [9]. Fig. 5 shows that the DPWM MAX and DPWM MIN show the worse performance for $M_i = 0.5$; however, at low and high modulation indices, the performances are only slightly worse than SVM. The auxiliary outputs are typically operated at low modulation indices since they are used to supply low power loads; therefore, the degradation in harmonic performance is limited when applying the DPWM MAX and DPWM MIN methods.

To conclude, Figs. 3 and 5 show the advantage of the DPWM methods in terms of lower switching losses, but also the drawback of higher harmonic distortion, with respect to the continuous SVM method.

B. 180° Shifting of the Auxiliary Current Outputs

Considering the MHC operation, it can be noted that the upper switch is used to modulate both the upper and the main output voltage. Therefore S_u conducts the currents flowing to both of them, as shown in Fig. 6. However, these currents are decoupled

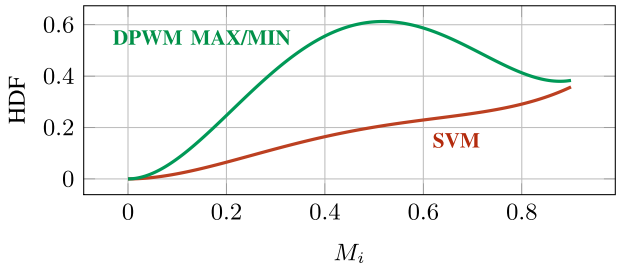

Fig. 5. HDF of SVM, DPWMMAX, and DPWMMIN under the same switching frequency. Note that discontinuous modulation methods can be used only in the auxiliary outputs.

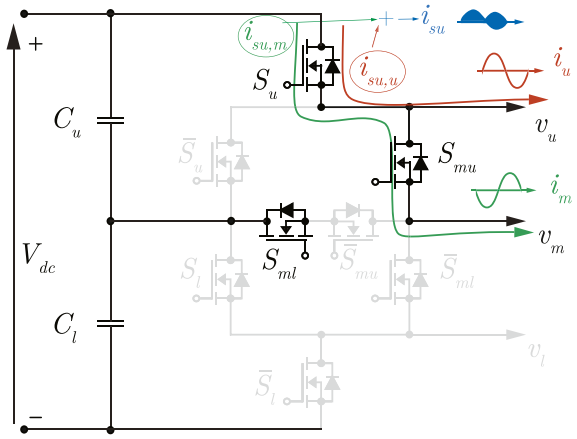

Fig. 6. MHC switching state considering phase-a when the upper auxiliary and the main load are supplied through S_u. The ON switches are highlighted with black color. If the upper auxiliary current i_u and the main load current i_m are phase shifted of 180° between them the rms current in S_u is minimized.

from each other since they are a function of the individual load conditions and of their respective terminals' output voltages, which in turn only depend on the modulation waveforms and V_{dc}. Therefore, i_{su}, which is the current flowing through S_u, is related to both the upper, i_u, and main, i_m, output currents and can be defined as follows:

$$i_{su} = i_{su,u} + i_{su,m} \tag{5}$$

where $i_{su,u}$ is the fraction of the upper output current flowing through the S_u, and $i_{su,m}$ is the fraction of the main output current flowing through the S_u.

Under the condition that the three MHC outputs are not synchronized, a phase shift between the phase of the main output voltage v_m and the phase of the two auxiliary outputs v_u and v_l can be introduced. Such phase shift, depending on the outputs' load conditions, for some applications, will result in a phase shift also between the output currents. Therefore, if the phase shift of the modulation indices is controlled to lead to a 180° phase shift between $i_{su,u}$ and $i_{su,m}$, the rms current in S_u will be lower, further reducing the MHC losses. This concept can be applied both between the main and upper output and between the main and lower output, impacting the power losses in S_u and $\overline{S_l}$, respectively. Furthermore, such phase shift can be applied with any modulation technique, both continuous and discontinuous ones.

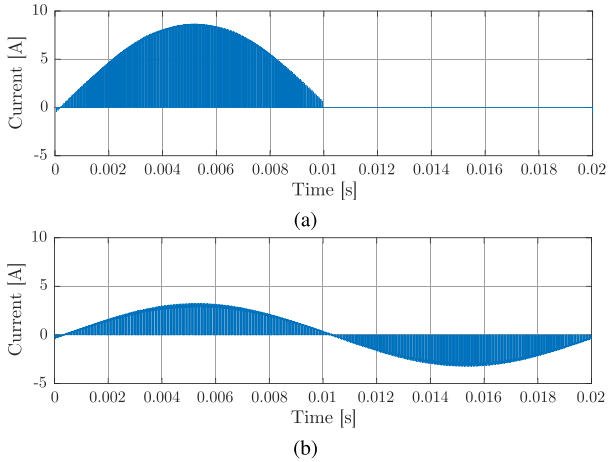

Fig. 7. Steady-state waveforms of (a) $i_{su,m}$ and (b) $i_{su,u}$ derived through circuit simulation.

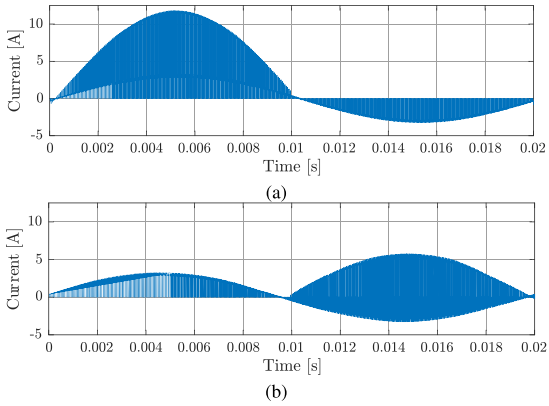

Fig. 8. Steady-state waveforms of i_{su} when (a) the upper and main output currents are in phase, and (b) when the two are 180° shifted.

A circuit simulation software is used to show the proposed concept. A simulation model of an MHC has been built to show the waveform of the current through S_u and to calculate its rms value under various phase shifts between the main and upper output terminals. The simulation parameters are kept equal to the ones described in Section II-A. The steady-state waveforms of $i_{su,m}$ and $i_{su,u}$ derived through the circuit simulator are shown in Fig. 7(a) and (b), respectively. If these two currents are in phase, the two half-waves with the highest average current values will lay in the same half-cycle, as possible to see in Fig. 8(a). On the other hand, if i_u and i_m are phase shifted of 180° between each other, the positive component of $i_{su,u}$ will sum up with the negative component of $i_{su,m}$, therefore resulting in a lower i_{su} rms, as shown in Fig. 8(b). In Fig. 9, the rms current in S_u is calculated for a fixed auxiliary load power and by varying the main load power when the phase currents of the upper and main outputs are in phase or shifted of 180°. When a 180° shift is applied, the rms current in S_u can be strongly reduced, up to 40%.

Furthermore, through the circuit simulator, the conduction losses distribution among the switches of phase-a are calculated. Fig. 10 displays them when the MHC operates under HSVM and

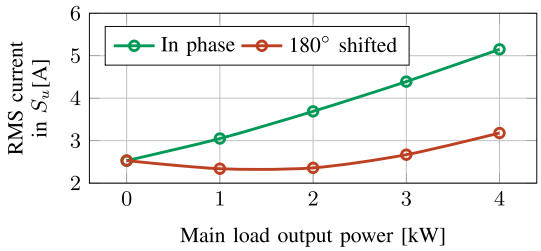

Fig. 9. RMS current in S_u for a fixed auxiliary load output power and varying the main load output power when the phase currents of the upper and main outputs are in phase or shifted of 180°.

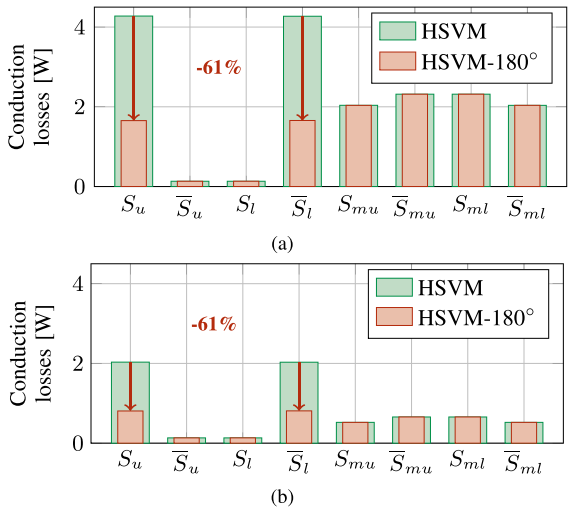

Fig. 10. Conduction losses distribution among the switches of phase-a when the MHC operates under HSVM and the main output current is 0 and 180° shifted from the auxiliary ones while supplying (a) 2 × 300 W auxiliary loads and 4.4 kW main load, and (b) 2 × 300 W auxiliary loads and 2.2 kW main load.

when shifting by 0° and by 180° the auxiliary output currents. Two operating points are considered, Fig. 10(a) is relative to when the MHC supplies 2 × 300 W auxiliary loads and a 4.4 kW main load, and Fig. 10(b) when the MHC supplies 2 × 300 W auxiliary loads and a 2.2 kW main load. It can be noted that the shifting of the auxiliary currents with respect to the main output current leads to a 61% reduction in conduction losses in S_u and $\overline{S}_l$, which are also the two switches more heavily loaded. Note that the other switches are not impacted by such phase shift, confirming the fact that this method does not impact the operation of the MHC.

III. Experimental Validation

The proposed HSVM modulation strategy and the 180° shift-based HSVM are implemented in a 5 kW three-phase MHC prototype, which is shown in Fig. 11. The MHC power switches can be selected with a voltage class of $V_{\text{dc}}/2$, as for the ANPC converter, with exception of S_{mu} and $\overline{S}_{ml}$, which in some switching states they need to block the full V_{dc} voltage and, therefore, need to be selected with a voltage class of V_{dc}. Regarding the current rating, the half-bridge modules' switches (S_u, $\overline{S}_u$, S_l, $\overline{S}_l$) need to withstand the main and respective auxiliary load, therefore they need to be sized for the sum of these two powers. The T-Type module switches (S_{mu}, $\overline{S}_{mu}$, S_{ml}, $\overline{S}_{ml}$), instead, only feed the main load, therefore they need to be sized for the main load power. Following these constraints, the MHC prototype is assembled with the 900 V 120 m Ω C3M0120090 J SiC MOSFET from Cree as switch, and it is operated following the same parameters used for the circuit simulations of Section II-B supplying resistive loads. These are interfaced with the MHC output terminals utilizing *LCL* filters, assembled with 340 μ H inductances and 5 μF capacitances. The load resistances are fixed to have the auxiliary outputs delivering each 0.3 kW, and the main output terminal 4.4 kW, for a total MHC power of 5 kW.

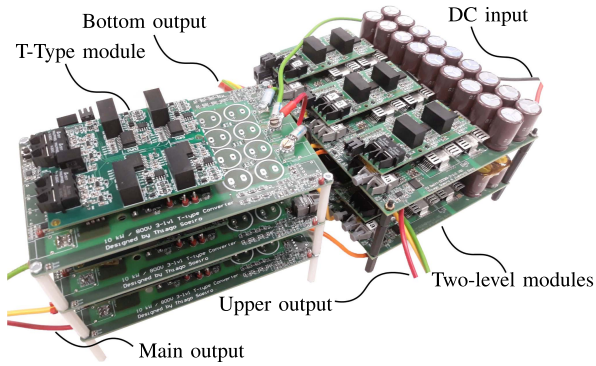

Fig. 11. Three-phase 5 kW MHC prototype, highlighted the dc input and ac outputs, and the two-level and T-type modules used for the MHC assembly.

The phase-a waveforms of the MHC operating with HSVM are shown in Fig. 12(a). The voltage waveforms are shown before and after the *LCL* filters, with subscripts i and f, respectively, while only the load current is shown. Currents and voltages are shown for the three outputs, with subscripts u, m, or l. The upper and lower outputs clamp at their current's positive and negative peaks, respectively. The same quantities are also presented in Fig. 12(b) when the MHC operates with HSVM and a phase shift of 180° between the main output current and the two auxiliary currents. The individual MHC outputs are not impacted by the 180° shifting, and the overall MHC operation is equivalent to the one of Fig. 12(a). The HSVM modulation and the 180° shift-based HSVM are implemented to reduce the MHC power losses. The effectiveness of these methods is evaluated through the Yokogawa WT500 power analyzer, while the MHC auxiliary loads provide fixed power of 0.3kW each, and the main output varies in power from 0.8 to 4.4 kW. The MHC efficiency is measured under various SVM and HSVM, and when shifting the auxiliary currents of 180°. The efficiency curves are shown in Fig. 13. Note that the efficiency measurements include also the losses in the three *LCL* filters and in the dc-link capacitors. The HSVM method increases the efficiency with respect to SVM, in the order of 0.3% at full load, and up to 0.7% at 30% full power. A further efficiency increase is provided by the 180° shifting, especially for total power higher than 2 kW. The current shifting can provide a 0.15% efficiency improvement, which is remarkable at this high efficiency values, $\approx 98.5\%$.

Another important performance metric to be considered for benchmarking modulation schemes is the total harmonic distortion (THD), which defines the filtering requirements. As for the efficiency curves, the load current THD is evaluated for SVM

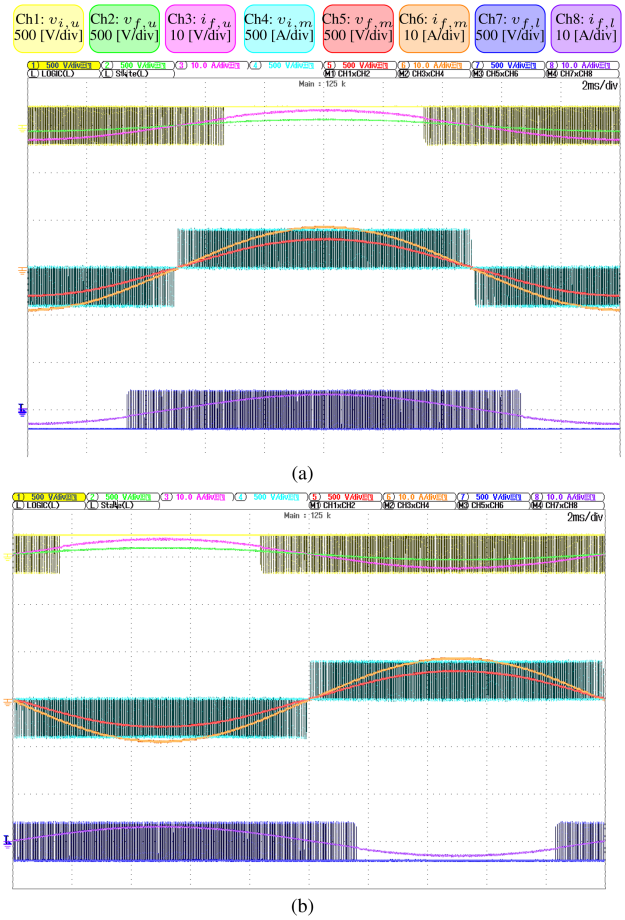

Fig. 12. MHC waveforms of phase-a when operating with (a) HSVM and (b) HSVM, and the main current is shifted from the auxiliary currents of 180°.

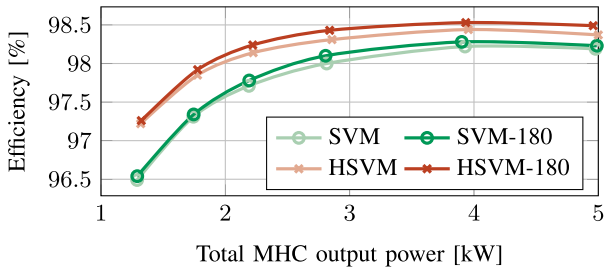

Fig. 13. MHC measured efficiency varying the main load output power, when the auxiliary outputs deliver 0.3 kW each, for different modulation strategies.

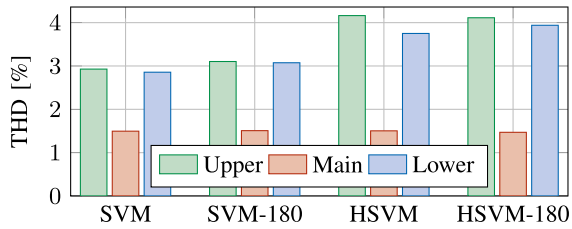

Fig. 14. Measured THD of the three MHC outputs at full main power for different PWM modulation strategies.

and HSVM and with the 180° shift. Fig. 14 shows the current THD of the MHC outputs under the previously mentioned conditions. The THD is measured after the *LCL* filters at the loads' currents. As expected and discussed in Section II-A, the SVM method leads to lower harmonic distortion. Instead, the HSVM method presents higher distortion in the auxiliary outputs than the SVM method. The main output sees no changes in THD since even when the MHC is modulated through HSVM, the main output is still SVM modulated, as explained in Section II-A. In addition, it is noted that the auxiliary currents shift of 180° creates a marginal difference in the harmonic distortion. Furthermore, the difference in THD between the main and auxiliary output is due to the different loading conditions and modulation index.

IV. Conclusion

This letter proposed an HSVM scheme for MHCs, which consists of the upper and lower outputs modulated with maximum and minimum DPWM, respectively, and the main output with SVM. Also, a scheme shifting the auxiliary currents with respect to the main currents has been described to reduce the MHC power losses further.

The proposed concepts have been implemented in a three-phase 5 kW MHC prototype. Their effectiveness in improving the MHC efficiency has been shown by measuring the MHC efficiency under various load conditions. It is shown that the HSVM method can improve the MHC efficiency of 0.3% at full load, and at partial loads, the improvement is even more considerable, +0.7% at 30% the full power. An additional 0.15% increase in efficiency can be achieved by shifting the auxiliary currents of 180° from the main currents. Such efficiency increase is significant since the system already operates at high efficiency, ≈98.5%, and it comes with a relatively uncomplicated modification in the control loop.

References

[1] C. Liu, B. Wu, N. R. Zargari, D. Xu, and J. R. Wang, "A novel three-phase three-leg AC/AC converter using nine IGBTs," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1151–1160, May 2009.

[2] A. Abdelhakim and F. Canales, "Hybrid neutral-point-clamped inverter with multiple output voltages," Swedish Patent SE2051459A1, 2020.

[3] S. M. D. Dehnavi, M. Mohamadian, A. Yazdian, and F. Ashrafzadeh, "Space vectors modulation for nine-switch converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1488–1496, Jun. 2010.

[4] M. Stecca, T. B. Soeiro, L. R. Elizondo, P. Bauer, and P. Palensky, "Comparison of two and three-level DC-AC converters for a 100 kW battery energy storage system," in *Proc. 29th IEEE Int. Symp. Ind. Electron.*, 2020, pp. 677–682.

[5] D. Zhang, J. He, and D. Pan, "A megawatt-scale medium-voltage high-efficiency high power density 'SiC+si' hybrid three-level propulsion systems," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 5971–5980, Nov./Dec. 2019.

[6] A. Abdelhakim, T. B. Soeiro, M. Stecca, and F. Canales, "Multiport hybrid converter (MHC) for electrified transportation systems," *IEEE Trans. Ind. Electron.*, 2022.

[7] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003. [Online]. Available:https://www.wiley.com/en-us/Pulse+Width+Modulation+for+Power+Converters%3A+Principles+and+Practice-p-9780471208143

[8] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, Sep./Oct. 1998.

[9] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan. 1999.