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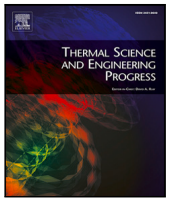

Thermal characterization methodology for thin bond-line interfaces with high conductive materials

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ABSTRACT

Silver sintering offers a promising landscape for Pb-free die attachment in electronics packaging. However, the sintered interface properties are highly process-dependent and deviate from bulk silver properties. Conventional measurement methods do not adequately capture the die-attach application geometry. Hence, this study introduces a novel methodology for characterizing thin bond-line interfaces with high-conductive materials. The transient heat flux impedance $\Delta Z_{th}(t, \Delta x)$ was measured between two thermally sensitive devices interconnected using pressureless Ag-sintering material. A correction factor was derived, based on thermal half-space principles, to account for non-uniform heat spreading over the die-attach interface. Experimental findings estimate an effective conductivity of ~115W/mk for the pressureless Ag-sintered interface. The measurement results were validated by measuring a SAC305 soldered interface, which exhibited ~55 W/mK, and a non-conductive epoxy interface of ~2.5 W/mK. Voids on the die-attach layer, resulting from material processing, were identified to influence the interface thermal behavior. An uncertainty analysis was further discussed, emphasizing equipment tolerances, measurement sensitivity, and geometrical and thermal anisotropies. The article concludes with a comparative summary of the proposed methodology against conventional methods, highlighting differences in working principle, thickness range, measurement parameters, and their advantages and limitations.

1. Introduction

Understanding and optimizing the die-attach material properties is crucial for high-temperature, high-power electronic devices [1–4]. The effectiveness of these materials has a significant impact on thermal performance and thermo-mechanical reliability, particularly in applications where efficient energy conversion and thermal management are pivotal [5–7]. Power devices undergo electrical overstress, mechanical vibrations, environmental humidity, and temperature fluctuations. Consequently, the die-attach layer that provides the necessary mechanical, electrical, and thermal bonding of the die to the package substrate endures thermo-mechanical stresses, affecting the device's electrical and thermal performance [8,9].

High-conductive materials such as silver sintering are emerging as a promising solution for lead-free die-attachments in power device packaging due to their low processing temperature and high melting point after processing [10–13]. Despite their benefits, the thermal properties of silver sintering materials are often extracted based on bulk materials that do not represent thin interconnect layers. On the other hand, characterizing and extracting the thermal conductivity of a thin interface material (< 50 μm) presents a formidable challenge [14–17]. Streb et al. [18] explain the discrepancies in thermal conductivity extracted with conventional measurement methods such as laser flash, transient plane source measurements, and the ASTM D5470 standard DynTIM tester. Besides, these methods require specific samples that do not adequately represent the application form factor. The widely adopted JESD51-14 transient dual interface test method [19], despite an industry standard to determine Junction-to-Case thermal resistance, requires necessary resolution for extracting die-attach interface thermal resistance, particularly for materials with superior thermal conductivity [20].

Simone et al. [21] proposed a one-dimensional time–temperature transient model to determine the heat transfer coefficient between two flat metallic surfaces. In this study, we have demonstrated a similar methodology, particularly for characterizing die-attach interface thermal properties within the application-specific form factor. Motivated by the evolving landscape of die-attach materials [22–26] and the

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need to understand the effective interface thermal properties, this study demonstrates the following:

(1) A methodology to estimate the effective interface thermal conductivity for complex and highly conductive die-attach materials, such as Ag-sintering, with appropriate form factor for semiconductor packaging applications.
(2) A correction factor to account for the influence of non-uniform heat spreading based on thermal half-space principles.
(3) A comparative summary to highlight the differences between the proposed methodology and other conventional measurement methods.

In the following section, the material selection and sample preparation are discussed first. Subsequently, the measurement methodology is detailed and the measurement results are presented with a comparative summary of the proposed methodology against other industry standard measurement methods.

2. Materials and methods

2.1. Material selection

To demonstrate the experimental methodology, two thermally sensitive active devices were selected: (i) Thermal Test Chip (TTC) and (ii) Schottky Diodes.

(a) Thermal Test Chips

Thermal Test Chips (TTCs) are specialized devices designed with integrated heating and temperature sensing elements to characterize and optimize interconnect materials and package thermal performance. The fabrication of TTCs follows a relatively straightforward and similar process to that of semiconductor devices. The TTCs can be developed on various semiconductor substrates, such as silicon (Si) or silicon carbide (SiC), by first depositing an oxide or nitride passivation layer using (plasma-enhanced) chemical vapor deposition techniques. Subsequently, the active heating and temperature sensing elements are lithographically defined. A second passivation layer is then applied over the active areas with vertical vias. An aluminum bond pad is deposited over the vias, facilitating wire bonding or flip chip bonding application. Further details on the development of TTCs are provided in [27,28].

The test chip utilized in this study is a commercially available Silicon-based TTC with dimensions of 3.2 mm × 3.2 mm × 400 μm and a 165 Ω resistance per heating cell (3.2 mm × 0.2 mm). Each heating cell can handle a maximum current of ~400 mA, resulting in a maximum power rating of ~250 W per test chip when properly cooled. Fig. 1(a) presents the calibration of a single heating cell at various ambient temperatures alongside a schematic layout of the TTC used in this study. The calibrated heating cell exhibits a linear temperature dependence with a sensitivity of ~ 0.47 Ω/°C over the temperature range of −55 to 150 °C.

To best demonstrate the methodology, an ideal strategy would have been to connect all heating elements on the test chip in parallel, ensuring a more uniform temperature distribution across the device. However, due to practical constraints, a single heating cell on the test chip was utilized in this study. A concentrated heat flux of ~2.6 W/mm^2 was applied over Resistor-5 or Heater-5, which is positioned centrally (see Fig. 1(a)). This configuration resulted in a non-homogeneous thermal flux across the device. The lateral heat spreading over the silicon surface can potentially influence the estimated thermal conductivity at the die-attach interface. To account for this effect, a geometrical correction factor based on a characteristic width was employed. This correction factor is explained further in detail within the experimental results section. The backside of the test chip substrate was metalized with TiPtAu (100/100/100 nm) to promote adhesion with the die-attach interface.

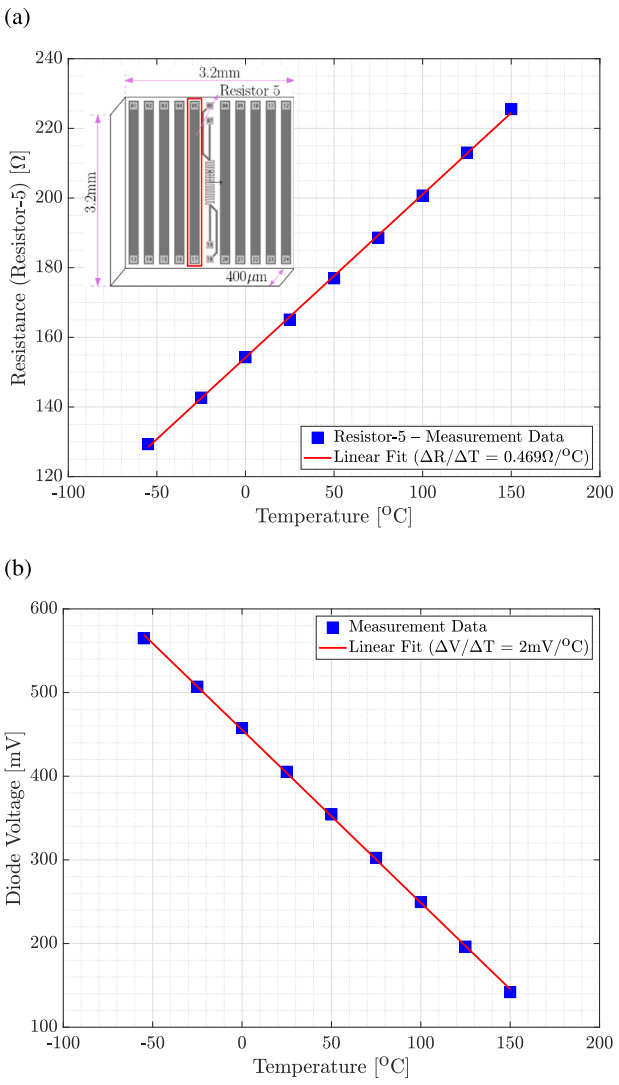


Fig. 1. The resistance sensitivity of Resistor-5 (a) and Schottky diode (b) was evaluated at nine different temperatures, which exhibits a linear temperature dependence.

(b) Schottky Diode

A 200 V 60 A Silicon Schottky Rectifier in bare die form was utilized as the second active device in this study. Silicon Schottky Diodes are semiconductor devices with metal–semiconductor junctions, known as the Schottky barrier. They are used for fast switching and low forward voltage drop applications. However, in this study, we utilized these Schottky diodes for the sole purpose of temperature measurement. These diodes contain solderable top and bottom surfaces with TiNiAg (3 μm) metal composition. Silicon Schottky diodes are temperature-sensitive devices that allow us to calibrate the Forward Voltage (V_f) with temperature (see Fig. 1(b)). A perfectly linear relationship can be exerted with a sensitivity of ~2 mV/°C.

(c) Die-attach materials

The choice of die-attach material is crucial to demonstrate the methodology. Three different materials with a wide range of thermal conductivities were selected for comparative analysis.

(1) **Commercial pressureless Ag-sinter material** with a high thermal conductivity of ~300 W/mK.

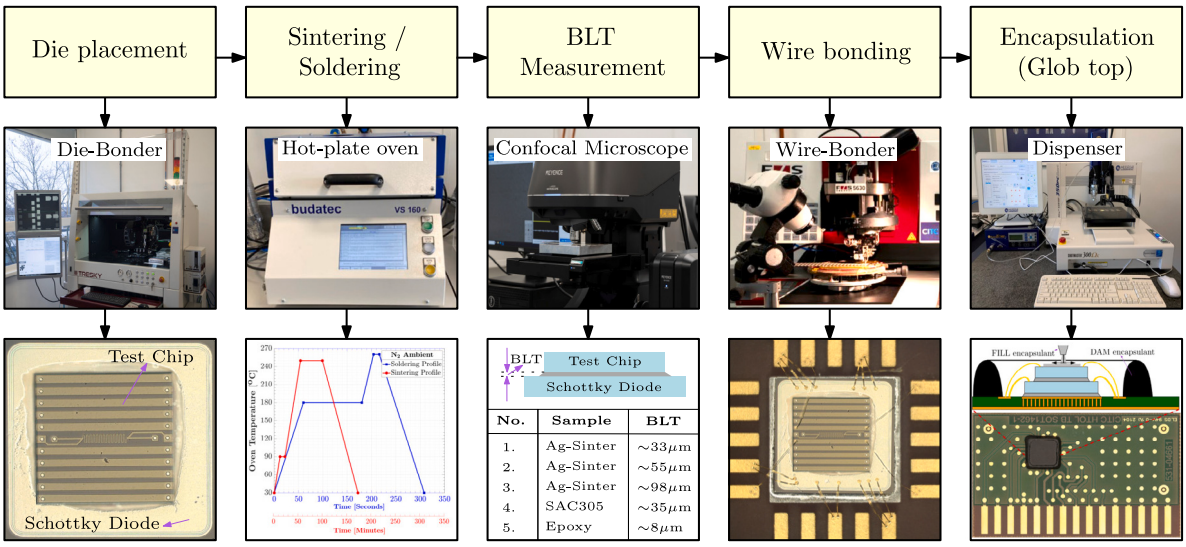


Fig. 2. Illustration of the various package assembly processes involved in sample preparation. The TTC was placed over the diode using a die-bonder and subsequently cured using an industrial hot-plate oven. Upon curing, the interface bond line thickness (BLT) was measured using a confocal laser microscope. The samples were further wire-bonded and encapsulated.

(2) **Commercial SAC305 solder paste** with a thermal conductivity of ~58 W/mK, and
(3) **Non-conductive epoxy material** with a thermal conductivity of <5 W/mK.

The thermal conductivity values mentioned are based on the material datasheet.

2.2. Sample preparation

The sample preparation involves semiconductor back-end packaging processes, which are schematically illustrated in Fig. 2. The first step in the assembly process involves gluing the test chip onto the diode due to matching thermal expansion coefficients. The gluing process is different for each die-attach material.

- **Ag-Sintering:** Kapton films of varying thicknesses were used as stencils to apply the wet paste onto the TiNiAg metalized top surface of the Schottky diodes. The thermal test chips were then mounted using a die-bonder and sintered under nitrogen in a commercial hot-plate oven. The Ag paste was initially dried at 90 °C for ten minutes and subsequently sintered at 250 °C for forty-five minutes (see Fig. 2).
- **SAC305 Soldering:** Similar to the Ag-sintering process, SAC305 solder paste was stencil printed, and the devices were assembled using a die-bonder and soldered in a hot-plate oven. The sample was first ramped up to 180 °C at a ramp rate of 150 K/min and held constant under Nitrogen for 120 s. Subsequently, the sample was further heated to 260 °C at 200 K/min and held at this reflow temperature under nitrogen for 12 s (see Fig. 2).
- **Non-conductive epoxy:** The non-conductive epoxy material was dispensed on the diode surface, the test chip was placed, and the assembly was cured in a hotplate at 150 °C for an hour. Due to the lower curing temperature, the process order was reversed: the Schottky diode was first soldered to a PCB, and then the test chip was attached using epoxy.

Following the gluing step, the die-attach interface thickness, also known as the Bond Line Thickness (BLT), was measured using a confocal laser microscope. For the Ag-sintered samples, the BLT was varied during assembly by using stencils of different thicknesses. The primary goal of varying the BLT was to quantitatively evaluate its impact on thermal performance. The measured BLTs are shown in Fig. 2.

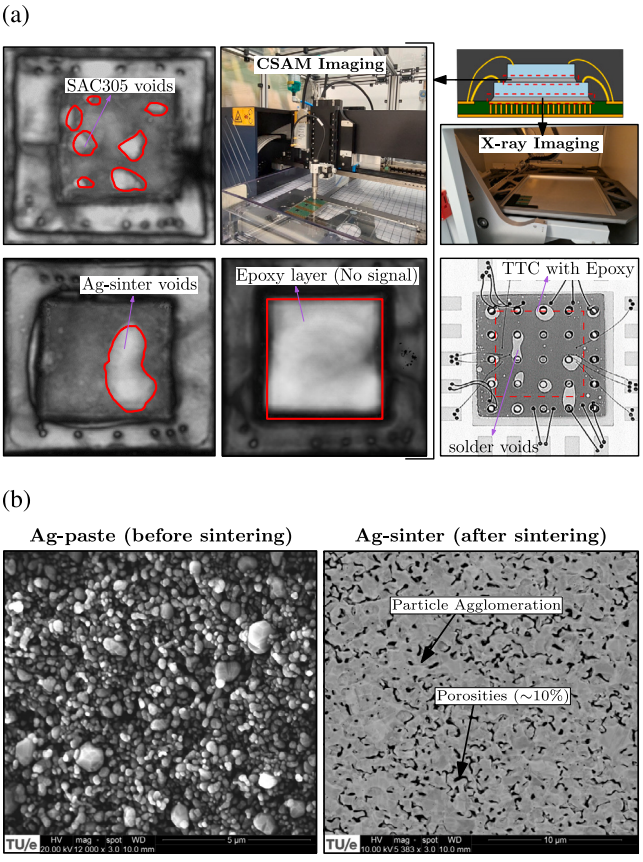


Fig. 3. (a) Inspection of samples using CSAM imaging and X-rays. Voids on the Ag-sintered layer and SAC305 soldered layer were observed. No signal passes through epoxy material due to higher acoustic impedance. X-ray examination indicates voids on the PCB solder layer (below the diode). (b) SEM images of the Ag-paste before sintering (laterally dispensed in a flat plate) and after sintering (vertically cross-sectioned) are shown. Agglomeration of particles with 10% porosities was observed after sintering.

The entire stack, except for the epoxy samples, was subsequently soldered onto a PCB and wire-bonded (see Fig. 2). The samples were

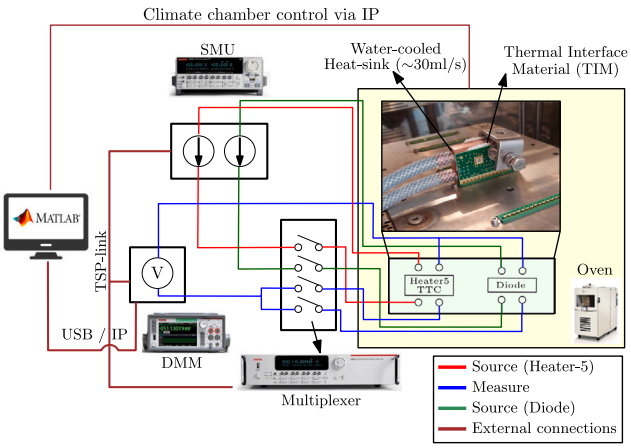


Fig. 4. Schematic illustration of the experimental setup developed for measuring TTC on Diode configuration.

bonded using 99.99% pure gold wire bonds, with different wire diameters for the test chip (25 μm) and the diode (50 μm) due to practical constraints in bonding at different heights.

Finally, the samples were encapsulated using a solvent-free, premixed thermoset epoxy-based "Fill" adhesive, along with a "Dam" encapsulant to protect the wire bonds (see Fig. 2). These epoxy-based encapsulants can withstand temperatures up to 160 °C.

The encapsulated samples were further inspected using Confocal Scanning Acoustic Microscopy (CSAM) imaging. CSAM revealed abnormalities, primarily voids, within the Ag-sinter and SAC305 die-attach materials (see Fig. 3(a)). The presence of voids on the die-attach interface can potentially influence the effective thermal conductivity of the interface which is taken into account and explained in the experimental results section. The epoxy-layered sample exhibited higher acoustic impedance, which hindered the acoustic signal, making it difficult to evaluate the quality of the epoxy bonding. Therefore, no definitive information about the epoxy bonding quality could be obtained. However, epoxy samples facilitated X-ray inspection to detect solder voids beneath the diode (see Fig. 3(a)). While the presence of voids is undesirable, the region of interest within this study is the interface between the test chip and the diode.

It is important to be aware that the effective thermal conductivity of an Ag-sintered interface is significantly influenced by the porosity of the sintered layer. Therefore, the Ag-paste was examined using an electron microscope both before and after sintering (see Fig. 3(b)). Post-sintering, the agglomeration of particles was observed, with the porosity estimated to be approximately ~10%.

3. Experimental procedure

A dedicated setup was developed to demonstrate the thermal characterization methodology, depicted schematically in Fig. 4. The test boards with assembled samples were secured on a test socket inside a climate chamber oven. The backside of the test boards was clamped with a water-cooled heat sink using a thermal interface material. Electrical connections from the test socket were routed through a multiplexer (switch matrix) to connect the device to sourcing (SMU) and measuring (DMM) equipment. The source unit has a compliance of 40 V up to 1 A continuous current, and the measuring equipment has a resolution of ±0.16 mV, which translates to ±0.005 K/W. The SMU, DMM, and Multiplexer are interconnected using a trigger synchronization and communication (TSP) protocol. All equipment, including the oven, is controlled using a user-defined MATLAB program. The electrical connections to the test chip and the diode are made of 4-point Kelvin contacts to minimize measurement inaccuracies.

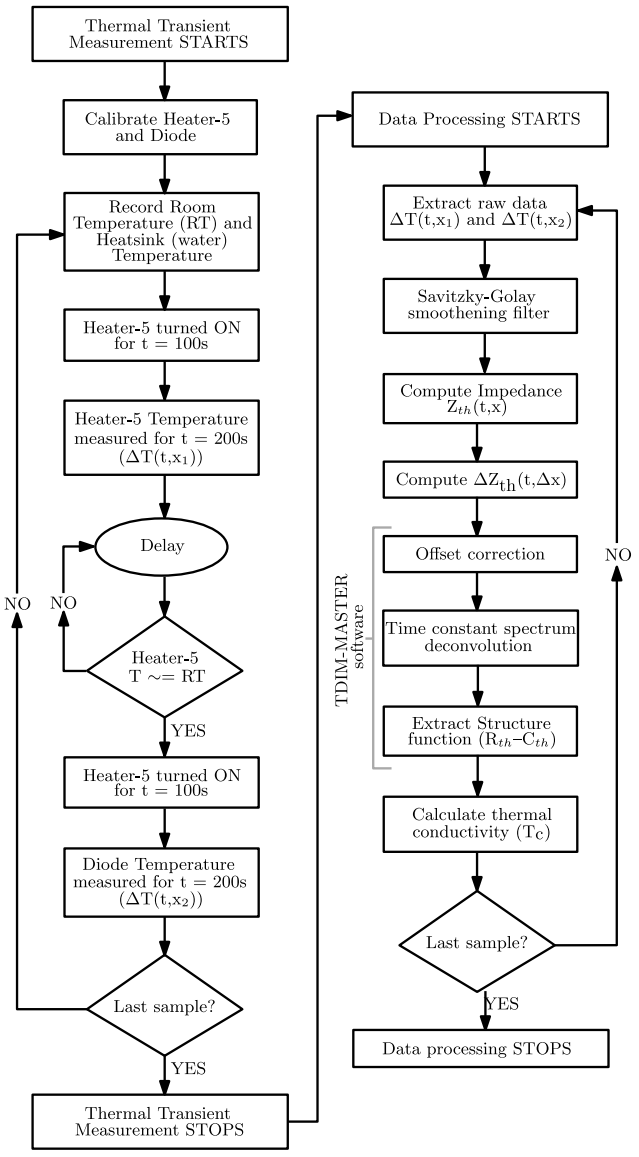


Fig. 5. Flow chart demonstrating the experimental methodology and data processing. All measurements were performed at room temperature (~25 °C). The heat sink temperature was the same as room temperature. The data processing was partly performed using JEDEC TDIM-Master software.

The thermal characterization methodology proposed in this study is an adaptation of the industry standard JESD51-14 transient dual interface test method [19]. The JESD51-14 determines Junction-to-Case thermal resistance $Z_{th(j\text{-}c}(t)$ of a package by comparing measurements with and without Thermal Interface Material (TIM). The JESD51-14 suggests mounting the devices on a water-cooled heat sink for 1-dimensional heat flow from the device to the heat sink. In this study, the samples were mounted using TIM on a water-cooled heat sink, which has a flow rate of 30 ml/s. The water-cooled heat sink ensures the heat generated from the test chip is driven towards the diode. The fundamental difference between both methods is that the JESD51-14 measures only the device junction temperature, whereas the proposed method measures the temperature difference between the device junction and substrate under the transient mode, thereby the effective interface thermal resistance can be extracted.

The workflow of the measurement method and the data processing steps are charted in Fig. 5. The measurements begin with the calibration of Heater-5 and the diode. After recording the ambient

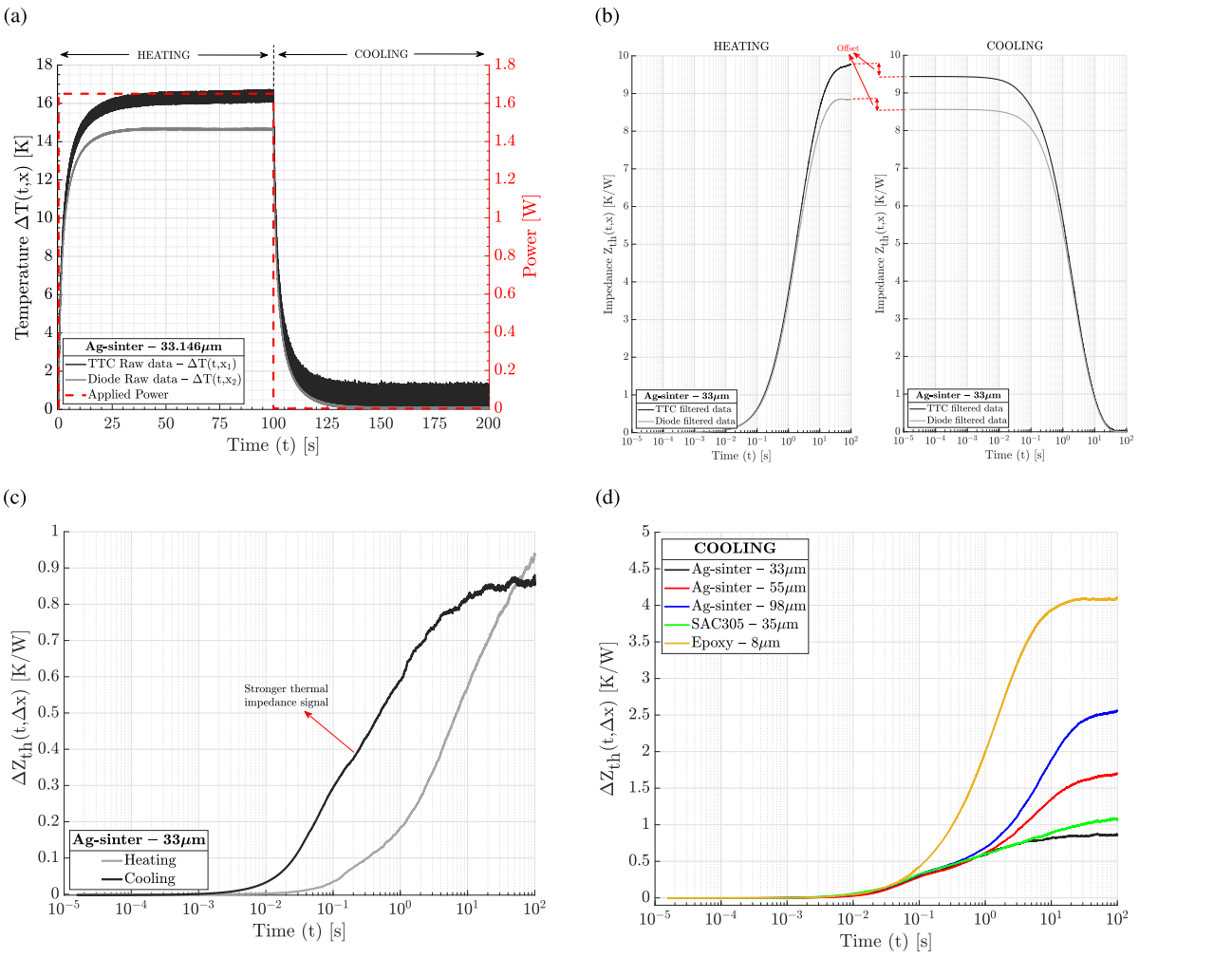


Fig. 6. (a) Raw measurement data of the test chip and the diode is shown along with the applied power input. The test chip has a lower signal-to-noise ratio compared to the diode. (b) Smoothened impedance data is shown on a logarithmic scale, highlighting the offset between heating up and cooling down. (c) The heat flux impedance obtained from the cooling down curve indicates a stronger heat dissipation signal. (d) The heat flux impedance data of all five samples; Ag-sinter ~ 33 μm, ~ 55 μm, and ~ 98 μm; SAC305 solder paste and non-conductive epoxy glue are shown.

conditions, the change in temperature $\Delta T(t,x)$ of both the test chip and the diode was sequentially measured by applying a maximum heat flux of ~2.6 W/mm^2 for one hundred seconds and further cooled down over another one hundred seconds. Fig. 6(a) illustrates the measured $\Delta T(t,x)$ of the test chip and the diode for the Ag-sintered sample with a bond line thickness of approximately 33 μm, along with the applied input power. The measurement data of the test chip shows a lower signal-to-noise ratio, indicating higher fluctuation compared to the diode measurement. The fluctuation in temperature measurements of the test chip was approximately ±0.5 K.

Normalizing the measured temperature $\Delta T(t,x)$ with the applied input power yields transient thermal impedance $Z_{th}(t,x)$ for both the test chip and the diode based on the heating up and cooling down measurements (see Fig. 6(b)). The data shown are processed after fitting a Savitzky–Golay smoothening filter to mitigate measurement noise. The impedance data provides comprehensive insights into the thermal characteristics spanning from transient to steady-state conditions.

An offset in impedance between heating up and cooling down is observed, indicating heat loss during switching currents. This offset is corrected at a later stage. By subtracting the diode impedance $Z_{th}(t, x_2)$ from the test chip impedance $Z_{th}(t, x_1)$, we obtain the heat flux impedance $\Delta Z_{th}(t, \Delta x)$ between the test chip and the diode (see Fig. 6(c)). The heat flux impedance shows more pronounced thermal dissipation signals during the cooling down phase compared to heating up, which is in agreement with the guidelines stated in JESD51-14 [19].

Consequently, the heat flux impedance $\Delta Z_{th}(t, \Delta x)$ was determined for all samples during the cooling down phase, and the results are shown in Fig. 6(d). The heat flux impedance $\Delta Z_{th}(t, \Delta x)$ for the Ag-sintered interfaces increases with increasing bond line thicknesses. Likewise, the thermally non-conductive epoxy material exhibits the highest heat flux impedance compared to Ag-sintered samples and SAC305. The obtained heat flux impedance represents the combined resistance of the test chip silicon and the die-attach interface. Therefore, further processing is required to extract the effective interface thermal resistance and subsequently translate it into effective interface thermal conductivity.

An essential step in extracting the contribution of interface thermal resistance from the heat flux impedance is to determine the time-constant spectrum. The offset in the cooling down curve (Fig. 6(b)) was corrected first by extrapolating the $\Delta Z_{th}(t, \Delta x)$ to t = 0 as shown in Fig. 7. Subsequently, the time-constant spectrum was established and discretized into finer steps to construct the thermally equivalent Foster network, which was further transformed into a Cauer network. The resistance-capacitance network in the Cauer domain (structure-function) represents the actual thermal properties of the materials within the system. For a detailed explanation of the steps involved in structure-function computation, please refer to [29–31]. In this study, we utilized the TDIM-Master software provided by JEDEC for offset correction, time-constant spectrum deconvolution, and structure-function

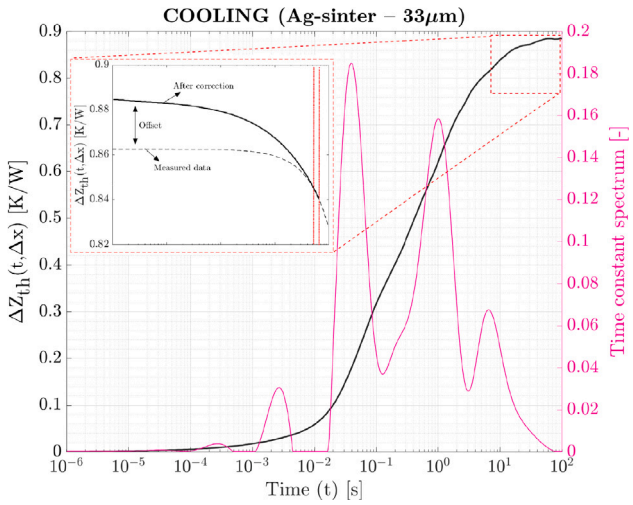


Fig. 7. The offset on heat flux impedance data $\Delta Z_{th}(t, \Delta x)$ was corrected and the time-constant spectrum was determined.

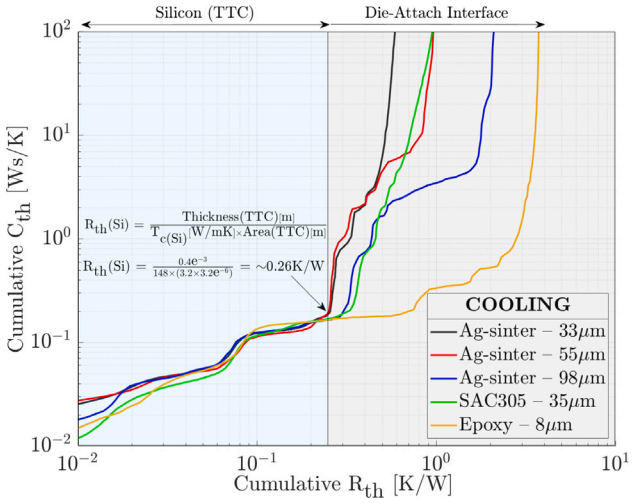


Fig. 8. Cumulative structure function of Ag-sinter ~ 33 μm, ~ 55 μm, ~ 98 μm, SAC305 & Epoxy glue is shown. The Silicon test chip has a resistance of ~0.26 K/W, and the remainder provides the effective thermal resistance of the die-attach interface.

computation. The results are discussed in the following section, including a correction factor for non-uniform heat spreading and an uncertainty analysis.

4. Experimental results and discussion

4.1. Thermal characterization results

Upon generating the RC Cauer network from the time constant spectrum, the TDIM Master generates the cumulative structure-function. This graphical representation illustrates the thermal resistance-capacitance network of the system, encompassing the bulk silicon of the test chip and the die-attach interface (see Fig. 8). The cumulative structure function is plotted on a logarithmic scale to highlight the influence of silicon resistance. The theoretical thermal resistance of the test chip silicon was calculated to be ~0.26 K/W, corresponding to the transition point identified in the structure-function. This enables determining the effective interface thermal resistance of the die-attach as emphasized in Fig. 8.

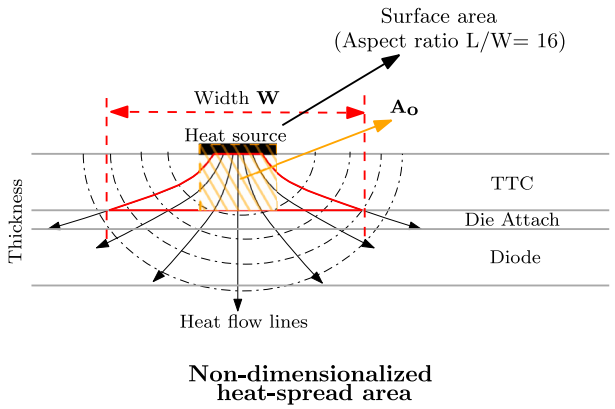


Fig. 9. Schematic representation of heat spreading on half-space. A characteristic width was determined from the out-of-plane heating area, and a correction factor was established to estimate the heat spread area on the die-attach.

Knowing the effective interface thermal resistance, the effective thermal conductivity of the die-attach interface can be calculated as follows:

$$T_c[W/mK] = \frac{1}{R_{th}[K/W]} \frac{L[m]}{A[m^2]} \quad (1)$$

In Eq. (1), 'L' represents the bond line thickness, and 'A' denotes the active heat spreading area on the die-attach interface. However, the actual interaction area (electrical, thermal, and mass transfer) between two contacting bodies varies depending on the contacting surfaces [32]. Two fundamental phenomena can influence heat transfer area; thermal contact resistance due to interface imperfections and thermal spreading resistance. The extracted effective interface thermal resistance from Fig. 8 is a summation of resistances from the metallization layers, die-attach material, and other contact resistances. For more details on the influence of thermal contact resistance in heat transfer, please refer to [33,34].

Thermal spreading resistance is a widely researched topic in thermal engineering, which needs to be taken into account in scenarios where a concentrated heat source interacts with a broader conducting surface, resulting in spreading resistance. Hence, considering the Heater-5 area as the active heat spreading area on the die-attach interface may provide insufficient representation for computing the effective interface thermal conductivity. Decades of research on both steady-state and transient thermal spreading phenomena over smooth and rough surfaces are extensively documented in [32]. The square root of the heat source area $\sqrt{A_o}$ is commonly used to non-dimensionalize spreading resistance for different shapes on a half-space. [35] has validated $\sqrt{A_o}$ as the most appropriate parameter to compute non-dimensional spreading resistance. In this study, we employed the characteristic parameter $\sqrt{A_o}$ to derive a correction factor that adequately represents the active heat spreading area on the die-attach (Fig. 9).

Two assumptions were made to compute the active area on the die-attach surface for non-uniform heating surfaces:

- The geometry of Heater-5 has an aspect ratio (L/W) of 16. Hence, the heat spreading along the length of the heater surface was assumed to be uniform.

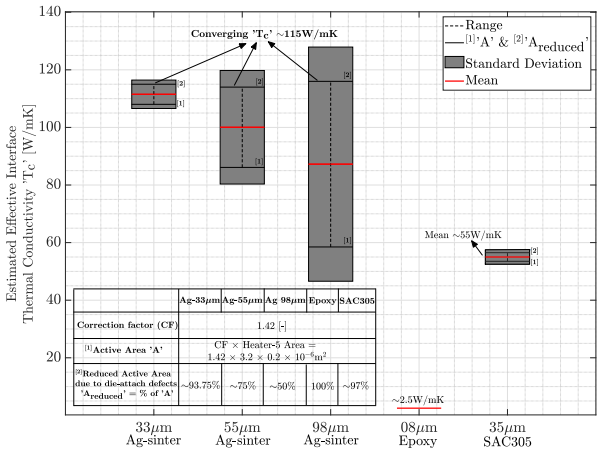


Fig. 10. Standard deviation of effective interface thermal conductivity 'T_c' estimated based on active area 'A' and reduced active area '$A_{reduced}$' due to interface defects.

- The second assumption is that the primary heat transfer area to the die-attach is equivalent to the area of Heater-5; thus, considering an isothermal out-of-plane heating area A_o.

Accordingly, a characteristic width ($\sqrt{A_o}$) was determined, and a correction factor was derived (see Fig. 9). It is important to note that this correction factor is derived under the assumption of concentrated heating over an infinitely large plane. Further validation of the correction factor's applicability is essential. Based on the effective interface thermal resistance extracted from Fig. 8 and the active area 'A' estimated from Fig. 9, the effective interface thermal conductivity 'T_c' can be determined using Eq. (1). However, the presence of voids on the die-attach interface (see Fig. 3(a)) leads to underestimation of 'T_c'. Therefore, based on voids identified from CSAM imaging, a reduced active area '$A_{reduced}$' was determined, establishing the 'T_c' of Ag-sintered interface. A standard deviation was further shown based on Active Area 'A' and Reduced Active Area '$A_{reduced}$'. The results are depicted in Fig. 10, leading to the following conclusions:

- Ideally, thermal conductivity should be independent of the interface thickness. However, due to processing defects observed on the die-attach layer (see Fig. 2), the effective interface thermal conductivity varies among samples with different thicknesses.
- A standard deviation of the effective thermal conductivity for Ag-sintering and SAC305 was determined based on the active area 'A' and the reduced active area '$A_{reduced}$'. Ag-sinter samples with bond line thicknesses of 55 μm and 98 μm exhibit the largest deviation due to the presence of voids. However, based on '$A_{reduced}$', a converged T_c of ~115 W/mK was estimated for Ag-sintered interfaces.
- In comparison, the SAC305 interface exhibits ~55 W/mK, while epoxy glued interface indicates ~2.5 W/mK, which are expected as mentioned in their datasheet.

The estimated effective thermal conductivity for Ag-sintered interface (~115 W/mK) compared to the Ag-sintered material conductivity stated in the datasheet (~300 W/mK) highlights the limited understanding of interface properties as opposed to bulk materials. Therefore, based on the literature, a comparison of the Ag-sinter properties as a function of porosity is presented in Table 1. The thermal conductivity determined based on the proposed method is in a similar range as observed from literature. However, there are two primary distinctions:

- The samples analyzed in this study have the appropriate form factor for die-attach interfaces, as compared to sintered coupons or dog-bone structures.

Table 1
A comparison of Ag-sinter thermal conductivity from literature.

No.	Material Type	Porosity (%)	Thermal Conductivity (W/mK)	Ref.
1.	Heraeus C1075S pressure-assisted Ag-sintering	~38%	~75 W/mK	[36]
2.	DuPont LF131 pressure-assisted Ag-sintering	~19%	~175 W/mK	[36]
3.	Heraeus LTS016 pressure-assisted Ag-sintering	~7%	~350 W/mK	[36]
4.	Heraues LTS043 pressure-assisted Ag-sintering	~4%	~375 W/mK	[36]
5.	Nanosilver 250 °C &; 10MPa	~0%–15%	~200–158 W/mK	[37]
6.	Heraeus Ag-paste 200 °C & 5MPa	~22%	~150 W/mK	[38]
7.	**Pressureless Ag 250 °C (This study)**	**~10%**	**~115 W/mK (Eff. Interface conductivity)**	[–]

Table 2
Standard Uncertainty Analysis.

Source of Uncertainty		Standard Uncertainty				
		Ag ~33μm	Ag ~55μm	Ag ~98μm	SAC305 ~35μm	Epoxy ~8μm
BLT Measure-ments	Equipment tolerance	±0.1μm				
	Die Tilt (~5% BLT)	±2μm	±3μm	±5μm	±2μm	±0.5μm
Measurement Sensitivity		±0.16mV = ±3.9mΩ = ±0.008K = ±0.005K/W				
TTC Noise-to-Signal ratio		±0.5K = ±0.3K/W				
Offset correction		~0.04K/W	~0.03 K/W	~0.06 K/W	~0.07 K/W	~0.04 K/W
Silicon thermal conductivity		140–156 W/mK = ±8W/mK = ±0.015K/W				

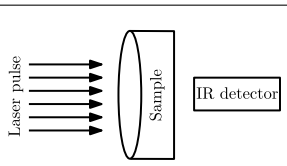
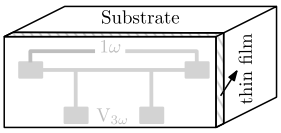
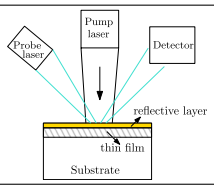
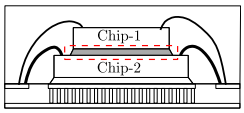
- The estimated thermal conductivity is an effective interface property that includes metallizations, the die-attach material, and other contact interactions.

4.2. Discussion

The methodology proposed in this study has demonstrated its capability to measure the effective interface thermal resistance across varying bond line thicknesses and materials with diverse thermal properties. Based on the measured interface thermal resistance, this study has also demonstrated a means to estimate the effective interface thermal conductivity for surfaces with non-uniform heat-spreading and interfaces with processing defects. Nevertheless, it is essential to acknowledge that several other factors might introduce uncertainty to the measurement results (see Table 2).

- Measuring the bond line thickness of the die-attach interface is critical for estimating the effective interface thermal conductivity (Eq. (1)). The confocal laser microscope has a tolerance of ±0.1 μm. Additionally, the samples typically exhibit die-tilt during the curing process, amounting to ~5% of BLT.
- The measuring equipment (DMM) has a sensitivity of ±0.16 mV, translating to an uncertainty of ±0.005 K/W. Furthermore, the low signal-to-noise ratio observed in Fig. 6(a) results in fluctuations of ±0.5 K, which corresponds to ±0.3 K/W in $Z_{th}(t, x_1)$.

Table 3
A comparative summary of the proposed methodology against other thin-film thermal conductivity measurement methods.

	Laser flash method	3ω method	Time-Domain Thermoreflectance (TDTR)	Heat flux Impedance (This paper)
Working principle				
Thin film thickness	~0.1mm to a few mm.	~0.01 to 0.1mm	Depends on the penetration depth of the probe laser (Typ. ~0.01 to a few mm.)	~0.008 (demonstrated in this paper) to a few mm.
Measurement parameter	Temperature	Temperature-dependent Electrical resistance	Temperature	Temperature Sensitive Electrical Parameters
Advantages	1. Fast and non-destructive. 2. High accuracy and precision	1. Non-destructive and contactless. 2. Suitable for very thin samples.	1. High sensitivity and high spatial resolution. 2. Non-destructive and contactless	1. Right form factor. 2. Wide range of thicknesses and materials. 3. Non-destructive and contactless.
Limitations	1. Specific samples and specialized equipments are needed. 2. Not suitable for optically transparent materials.	1. Complexity. 2. Dependence on substrate properties. 3. Limited thickness range.	1. Complexity. 2. Specific samples and specialized equipments. 3. Limited material compatibility.	1. Accuracy needs to be validated. 2. Require specific samples and dependent on the sample quality.

- The offset observed in Fig. 6(b), results in an uncertainty of ~0.03 to 0.07 K/W in $\Delta Z_{th}(t, \Delta x)$.
- Extracting the interface thermal resistance by subtracting the influence of silicon, introduces an uncertainty due to variations in silicon's thermal conductivity at room temperature (typically between 140 W/mK to 156 W/mK), leading to an uncertainty of ±0.015 K/W. Besides, the thermal properties of silicon have a strong temperature dependency.

Managing these uncertainty parameters poses challenges, especially in addressing geometrical and thermal anisotropies. Besides, the correction factor introduced for non-uniform heat spreading requires further validation. Moreover, the presence of intermetallic compounds at the die-attach interface introduces additional challenges in ensuring reliable interconnect formation. Despite several practical challenges addressed, the methodology provides compelling reasons for its adoption as a tool to determine die-attach interface thermal conductivity in semiconductor packaging.

Table 3 summarizes the proposed heat flux impedance methodology alongside three other conventional thin-film thermal conductivity measurement methods, namely laser flash, 3ω, and Thermoreflectance thermography. The comparative summary presented highlights the differences in their working principle, thin-film thickness range, measurement parameters, and their advantages and limitations.

5. Conclusion

While several drop-in replacements for lead (Pb) solders are emerging, it is important to understand the effective thermal conductivity of the die-attach interface and their influence on the package thermal performance. This study has addressed this critical need by introducing a methodology for characterizing the effective interface conductivity for complex and high conductive die-attach materials, overcoming misrepresentations of bulk material properties for thin film interfaces.

- The methodology demonstrated its efficiency by estimating the thermal conductivity across a wide range of die-attach materials (pressureless Ag-sintering material, SAC305 solder paste, and non-conductive epoxy) with varying bond line thicknesses (~8–98 μm).
- A correction factor for non-uniform heat spreading based on the thermal half space principles was introduced to estimate the effective heating area on the die-attach interface.
- The influence of die-attach materials processing defects was identified as a significant challenge. Hence, standard deviations in thermal conductivity measurements were determined.
- Besides, parameters such as geometrical and thermal anisotropies, equipment sensitivity, and other external influences, introduce uncertainty to the measurement results. This has been briefly discussed along with a comparative summary of the proposed method against other conventional measurement methods.

In conclusion, this study advances our understanding of die-attach interface thermal conductivity recognizing that bulk material properties do not adequately represent interface behavior. This is particularly important for complex materials such as Ag-sintering, whose effective interface conductivity is heavily dependent on its processing conditions.

For future research and practical applications, the methodology can be simplified by connecting two diodes using the desired die-attach material, achieving a PNP or NPN configuration with a die-attach interface. This approach can mitigate the effects of non-uniform heat spreading. An NPN interface configuration, in particular, might further minimize the influence of silicon resistance on the interface measurements, as device heating occurs at the P-junction, which is closer to the die-attach interface. Continued refinement of measurement techniques and deeper exploration into interface thermal behavior will lead to sustainable semiconductor packaging technologies.

CRediT authorship contribution statement

Henry A. Martin: Writing – review & editing, Writing – original draft, Resources, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Sébastien Libon:** Conceptualization. **Edsger C.P. Smits:** Writing – review & editing, Supervision, Project administration. **René H. Poelma:** Writing – review & editing, Supervision. **Willem D. van Driel:** Supervision. **GuoQi Zhang:** Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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