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Wide Voltage Range DC/DC Converters

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WIDE VOLTAGE RANGE DC/DC CONVERTERS

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WIDE VOLTAGE RANGE DC/DC CONVERTERS

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus prof. dr. ir. T. H. J. J. van der Hagen
chair of the Board for Doctorates
to be defended publicly on
Thursday 12th, September 2024 at 10:00 o'clock

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To my mom and dad

CONTENTS

SUMMARY

In the last decade, the market for Electric Vehicles (EV) has expanded at an unprecedented rate. Concurrently, there has been a surge in the demand for public Direct Current (DC) EV charging stations. To accommodate a diverse array of EVs, these charging stations are required to support a broad operational voltage and power spectrum. However, this necessity introduces a trade-off between the operational range and the efficiency and utilization of the installed power within the charging infrastructure. The core of the issue lies in the fact that the charging stations, designed to cater to a wide range of operational conditions, often do not operate at their peak efficiency outside their designated optimal performance region.

To address this challenge, this thesis investigates the advantageous DC/DC power electronics solutions that can maintain high efficiency across a wider operational range while optimizing the utilization of installed power. The research topics include the suitable DC/DC converters for the back-end power modules of the charging system, the multi-objective design process of the power modules, and the advanced operation of the power modules.

SUITABLE DC/DC POWER MODULES

The back-end DC/DC power modules are required to operate with extremely wide battery voltage ranges due to the introduction of EV models with high battery pack voltage. However, conventional power electronic converters yield poor efficiency performance when they are operated in such a wide voltage range.

In this thesis, novel power electronic solutions for the back-end power modules within EV charging systems are introduced. These solutions are characterized by their reconfigurable topologies and the application of advanced modulation techniques. Through experimental validation, it is demonstrated that these innovative solutions significantly broaden the operational voltage spectrum while maintaining high efficiency across the entire range of operations. Consequently, these proposed power electronics building blocks represent a significant advancement for DC-type EV charging infrastructure, offering an efficient solution to meet the dynamic demands of electric vehicle charging.

MULTI-OBJECTIVE DESIGN OF POWER MODULES

The multi-objective design and benchmark of power electronic converters in terms of cost, power density, and efficiency performance is challenging, primarily due to the poor availability of the components' data. Component cost models depending on physical component properties are typically applied in the literature, but they are not so straightforward to implement. Moreover, a large database acquired from manufacturers is needed for a better fitting, which is not easily accessible.

This thesis proposes a multi-objective power electronic converter design and benchmark process in terms of the normalized cost, power density of the magnetic components and heatsinks, and the average efficiency performance. This process utilizes well-accessible data provided by the components' re-distributors to establish the correlations between the cost and loss performance of the components. Using this multi-objective design process, three re-configurable structure PSFB converters are analyzed and benchmarked for the wide voltage range public EV charging application. The research results prove the feasibility of the proposed multi-objective design and benchmark process, and identify the t-PSFB and r-PSFB converters to be the outstanding solutions in the wide voltage range public EV charging application.

ADVANCED OPERATION OF POWER MODULES

The charging strategies, which define how the electric energy is transferred from the charger to the EV battery, significantly impact the system's performance metrics. On the one hand, the charging strategy, especially the injected current, determines how fast the battery is being charged, affecting the cells' efficiency and aging. On the other hand, it determines how and in what range the power electronics converter of the EV charger will operate, thus affecting the efficiency and utilization rate of the circuit components.

This thesis conducts a simulation case study to investigate how different charging strategies affect the performance of a modular EV charger. It is found that, firstly, the alternative charging strategies together with the modular structure of the charger can narrow the operation range of the power modules compared to the conventional CC-CV charging strategy. Combined with a tailored power module design, higher charging cycle efficiency can be achieved using alternative charging strategies. Secondly, alternative charging strategies can improve the utilization rates of installed power if combined with a flexible parallel modular multiple outputs structure.

SAMENVATTING

In het afgelopen decennium is de markt voor elektrische voertuigen (EV) in ongekend tempo gegroeid. Tegelijkertijd is er een toename in de vraag naar openbare gelijkstroom (DC) EV-laadstations. Om een breed scala aan EV's te kunnen huisvesten, moeten deze laadstations een breed operationeel spannings- en vermogensspectrum ondersteunen. Deze noodzaak brengt echter een afweging met zich mee tussen het operationele bereik en de efficiëntie en het gebruik van het geïnstalleerde vermogen binnen de laadinfrastructuur. De kern van het probleem ligt in het feit dat de laadstations, die zijn ontworpen om te voldoen aan een breed scala aan operationele omstandigheden, vaak niet op hun maximale efficiëntie werken buiten hun aangewezen optimale prestatiegebied.

Om deze uitdaging aan te pakken, onderzoekt dit proefschrift de voordelige DC/DC-vermogenselektronica-oplossingen die een hoge efficiëntie kunnen behouden over een breder operationeel bereik en tegelijkertijd het gebruik van het geïnstalleerde vermogen kunnen optimaliseren. De onderzoeksonderwerpen omvatten de geschikte DC/DC-converters voor de back-end-vermogensmodules van het laadsysteem, het multiobjectieve ontwerpproces van de vermogensmodules en de geavanceerde werking van de vermogensmodules.

GESCHIKTE DC/DC-VERMOGENSMODULES

De back-end DC/DC-vermogensmodules moeten werken met extreem brede batterijspanningsbereiken vanwege de introductie van EV-modellen met een hoge batterijspanning. Conventionele vermogenselektronische converters leveren echter slechte efficiëntieprestaties wanneer ze worden gebruikt in zo'n breed spanningsbereik.

In dit proefschrift worden nieuwe vermogenselektronische oplossingen voor de back-end-vermogensmodules binnen EV-laadsystemen geïntroduceerd. Deze oplossingen worden gekenmerkt door hun herconfigureerbare topologieën en de toepassing van geavanceerde modulatietechnieken. Door experimentele validatie wordt aangetoond dat deze innovatieve oplossingen het operationele spanningsspectrum aanzienlijk verbreden, terwijl een hoge efficiëntie over het gehele bereik van de werking wordt gehandhaafd. Bijgevolg vertegenwoordigen deze voorgestelde vermogenselektronicabouwstenen een aanzienlijke vooruitgang voor DC-type EV-laadinfrastructuur en bieden ze een efficiënte oplossing om te voldoen aan de dynamische eisen van het opladen van elektrische voertuigen.

MULTI-OBJECTIEF ONTWERP VAN VERMOGENSMODULES

Het multi-objectieve ontwerp en de benchmark van vermogenselektronische omvormers in termen van kosten, vermogensdichtheid en efficiëntieprestaties is een uitdaging, voornamelijk vanwege de slechte beschikbaarheid van de componentgegevens. Componentkostenmodellen die afhankelijk zijn van fysieke componenteigenschappen worden

doorgaans toegepast in de literatuur, maar ze zijn niet zo eenvoudig te implementeren. Bovendien is een grote database van fabrikanten nodig voor een betere aanpassing, die niet gemakkelijk toegankelijk is.

Dit proefschrift stelt een multi-objectief ontwerp en benchmarkproces voor vermogenselektronische omvormers voor in termen van de genormaliseerde kosten, vermogensdichtheid van de magnetische componenten en koellichamen en de gemiddelde efficiëntieprestaties. Dit proces maakt gebruik van goed toegankelijke gegevens die door de herdistributeurs van de componenten worden verstrekt om de correlaties tussen de kosten en verliesprestaties van de componenten vast te stellen. Met behulp van dit multiobjectieve ontwerpproces worden drie herconfigureerbare structuur PSFB omvormers geanalyseerd en gebenchmarkt voor de brede spanningsbereik openbare EV laadtoepassing. De onderzoeksresultaten bewijzen de haalbaarheid van het voorgestelde multi-objectieve ontwerp en benchmarkproces en identificeren de t-PSFB- en r-PSFB-converters als de uitstekende oplossingen in de brede spanningsbereik openbare EV-laadtoepassing.

GEAVANCEERDE WERKING VAN VERMOGENSMODULES

De laadstrategieën, die definiëren hoe de elektrische energie van de lader naar de EV-batterij wordt overgebracht, hebben een aanzienlijke impact op de prestatiemetingen van het systeem. Enerzijds bepaalt de laadstrategie, met name de geïnjecteerde stroom, hoe snel de batterij wordt opgeladen, wat de efficiëntie en veroudering van de cellen beïnvloedt. Anderzijds bepaalt het hoe en in welk bereik de omvormer van de EV-lader zal werken, wat de efficiëntie en benuttingsgraad van de circuitcomponenten beïnvloedt.

Dit proefschrift voert een simulatiecasestudy uit om te onderzoeken hoe verschillende laadstrategieën de prestaties van een modulaire EV-lader beïnvloeden. Ten eerste is gebleken dat de alternatieve laadstrategieën samen met de modulaire structuur van de lader het werkingsbereik van de vermogensmodules kunnen verkleinen in vergelijking met de conventionele CC-CV-laadstrategie. Gecombineerd met een op maat gemaakt powermoduleontwerp kan een hogere laadcycusefficiëntie worden bereikt met behulp van alternatieve laadstrategieën. Ten tweede kunnen alternatieve laadstrategieën de benuttingspercentages van geïnstalleerd vermogen verbeteren als ze worden gecombineerd met een flexibele parallelle modulaire structuur met meerdere uitgangen.

1

INTRODUCTION

1.1. BACKGROUND

The climate change is extremely likely to be caused by the increased anthropogenic greenhouse gas (GHG) emission driven by economic and population growth [1]. To adapt and mitigate the risks of climate change, intergovernmental actions have been taken and several treaties have been made, such as the Kyoto Protocol and Paris Agreement, with the focus on reducing the risks and impacts of climate change by controlling emissions of the main anthropogenic GHGs [2] [3].

Governments around the world have developed tailored climate strategies and targets within the framework of international agreements. European Union as a leader in tackling climate change, has made the 2020, 2030, and 2050 climate strategies and targets [4]. The key targets of these strategies are summarized in the table 1.1 below. The Netherlands has committed itself to various international agreements and has developed a climate agreement aiming to emit 49% less CO_2 by 2030 compared to 1990, and by 2050, GHG emissions must have fallen by 95% [5].

1.1.1. EV ADOPTION

Transportation being one of the largest sources of GHG emission needs to be addressed with priority. The anthropogenic GHG emissions mainly come from electricity and heat production, industry, transport, buildings, agriculture, forestry and other land use (AFOLU), and other energy. Figure1.1 shows the total anthropogenic GHG emissions from economic sectors in 2010 [1], where the circle shows the shares of direct GHG emissions (in % of total anthropogenic GHG emissions) from five economic sectors in 2010. The pull-out shows how shares of indirect CO_2 emissions (in % of total anthropogenic GHG emissions) from electricity and heat production are attributed to sectors of final energy use. It can been seen that the GHG emissions from the transport sector account for around 14% globally. In the Netherlands, the transport sector is responsible for a quarter of all Dutch energy-related CO_2 emissions and 20% of the total Dutch GHG emissions. Target has been set by the EU government to reduce CO_2 emissions of the transport sector

1

EU Climate Targets	
by 2020	20% cut in greenhouse gas emissions (from 1990 levels) 20% of EU energy from renewables 20% improvement in energy efficiency
by 2030	At least 40% cuts in greenhouse gas emissions (from 1990 levels) At least 32% share for renewable energy At least 32.5% improvement in energy efficiency
by 2050	climate neutrality – an economy with net-zero GHG emissions

Table 1.1: Key targets of climate strategies of EU

by 60% in comparison with 1990 [6]. The Netherlands made agreements on sustainable growth of the transport sector that, CO_2 emissions caused by the transport sector must be reduced by 17% to at most 25 megatonnes (in comparison with 1990) in 2030, and to at most 12 megatonnes by 2050. Especially, one long-term perspective set out in the Agreement on Energy for Sustainable Growth is that all new passenger cars must be capable of driving without producing any CO_2 emissions by 2035, and this will be applied to all passenger cars by 2050. [7].

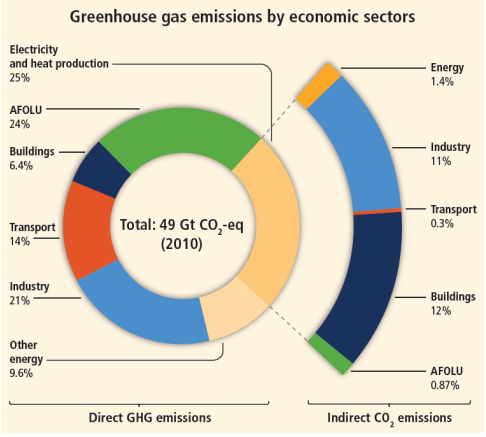

Figure 1.1: Total anthropogenic GHG emissions from economic sectors in 2010. [1]

Road transport accounts for the predominant part of the total emissions of the trans-

port sector. The statistics from [8] show the CO_2 emissions on Dutch territory by mobile sources in million kg. It can be concluded that around 73% of the total CO_2 emissions come from road traffic. In a more specific measure, more than 50% of CO_2 emissions are caused by passenger transport by road, and above 25% are produced by freight transport. Inland shipping, fisheries, and maritime shipping in Dutch territorial waters are responsible for nearly 20% of the CO2 emissions caused by the Dutch transport sector [7].

The electrification of transportation is a significant contribution to reduce CO_2 emissions, and to which Electric Vehicle (EV) is the key. Figure 1.2 shows the comparative life-cycle GHG emissions of a global average mid-size car by powertrain [9]. It can be seen that the life-cycle emissions of BEVs and PHEVs is less than ICE vehicles. Together with the efforts to decarbonize electricity generation, which effectively reduce the emission of well-to-tank fuel cycle, the mitigation of emissions from the transport sector could be maximized.

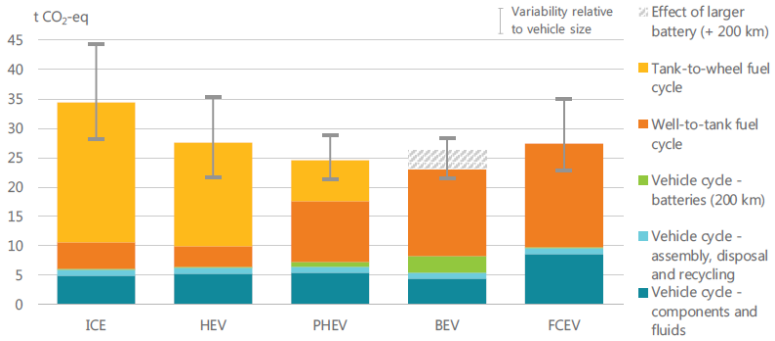

Figure 1.2: Comparative life-cycle GHG emissions of a global average mid-size car by powertrain, 2018 [9]

Among the different energy storage systems for EV, Lithium-Ion battery is the preferred choice due to its high specific energy, high specific power, long cycling times, wide range of operation temperature, low memory effect, low maintenance requirement, fast response time, small self-discharge rate and potential lower cost [10]. Figure 1.3 shows the mapping of different energy storage systems in terms of specific energy and specific power. It can been seen that Lithium Ion battery is able to provide relatively high power density and energy density at the same time, which are crucial to EV application. Moreover, the price of Lithium Ion battery is showing a trend of dropping [11]. Hydrogen fuel cells, on the other hand, is still limited by its cost, durability, and low energy density of the on-board hydrogen storage [12]. Moreover, The hydrogen refueling infrastructure is far from mature. There are only 381 refueling stations worldwide by the end of 2018 [9]. In this thesis, the term EV refers to Lithium-Ion battery EV.

1.1.2. DC-TYPE EV CHARGER

With the policy incentives and the development of new technologies, the EV market is growing rapidly, and so is the need for DC-type EV chargers which are cost-efficient, fast, accessible, and with high efficiency.

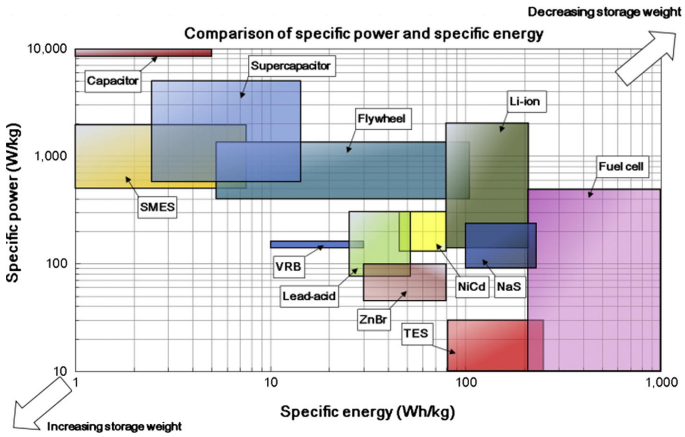

Figure 1.3: Comparison of specific power and specific energy [10]

The typical diagram of an isolated DC-type EV charger is shown in Figure 1.4. It converts the electric energy from the grid and supplies the vehicle battery with a DC charging current or voltage per the vehicle's request.

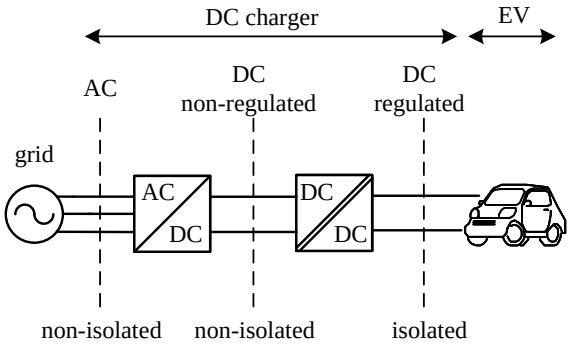

Figure 1.4: The typical diagram of an isolated DC-type EV charger [13]

In order to be able to provide public charging service to various EVs, the charger needs to have wide output voltage and power range. Table 1.2 shows the battery and charging specification of three different EV models as examples. It could be seen that the battery voltage of EVs would not only changes in a large range during charging process, but also varies among different models. Moreover, the maximum allowed charging power differs drastically with different models.

Having these wide voltage and power ranges may lead to lowered efficiency and poor utilization of the installed power of the charging system. Since the chargers would only have optimal performance in certain operation region, lowered efficiency could happen when the operation condition is out of the design region, such as operating at very low

Car Model	Nissan Leaf (40kW)	Tesla model 3 (long range)	Porche taycan (turbo)
end-of-discharge votlage (V)	240	240	495
end-of-charge voltage (V)	403	403	830
maximum charging power (kW)	50	250	270

Table 1.2: Battery and charging specifications for different EV models

voltage and/or low power. On the other hand, poor utilization of the installed power could happen when operating the charger at low power, leaving the rest of the installed power capability idle. An example is using a charger with 300kW power rating which could been used to charging a Porche Taycan, to charge a Nissan Leaf. Since the maximum charging power is limited by the EV, the exceeding 250kW installed power is left idle. Last but not least, the time that an EV is connected to a charger is much longer than the actual charging time. A study on the public charge infrastructure in the city of Amsterdam [14] finds out that only 12 to 18% of the average connection time is actually used for charging.

1.2. RESEARCH OBJECTIVE

To address the challenges of the EV charging application, a cost-efficient, fast, and flexible DC-type Electric Vehicle (EV) charger which features multiple output charging spots through the implementation of multiplexing techniques is proposed as a possible solution.

In order to successfully develop such a charging system, both the physical layer and the virtual layer need to be designed. The physical layer is the whole hardware of the power-delivering system constructed by the power modules. It includes not only the individual power modules but also the system structure. The virtual layer determines how the hardware operates. It consists of several elements: the modulation method to control the power module, the charging strategy which determines how the power is regulated during the charging process, and the multiplexing method to control the power flow from the output ports of the charger.

The research objective of this thesis focuses on the physical layer, and it is as follows:

To research the design and operation of the advantageous isolated back-end (DC/DC) power electronic converters which can be used as Power Electronic Building Blocks (PEBBs) for a flexible Electric Vehicle (EV) DC-type charger that features wide voltage range operation.

1.3. RESEARCH QUESTIONS AND METHODOLOGIES

To achieve the research objective, three main research questions need to be answered. The first and foremost research question is:

1. *What are the suitable DC-DC converters for the back-end power modules?*

To answer this first question, the following methodology is used:

- Define the design specifications for the isolated DC-DC converters.

- Conduct literature reviews on possible isolated DC-DC converter design solutions and identify the advantageous converter topologies and modulation methods.
- Propose 2-3 candidates, conduct further analytical modeling, simulation, and design
- Verify the designs by prototyping and experimental tests.

Once the suitable DC/DC converters are identified, the question becomes: how to better design them? Thus, the second research question and the methodology used are as follows:

2. *How to conduct a multi-objective design for an optimal power module design?*

- Define the most critical design objectives for the power modules.
- Propose a multi-objective design procedure that yields the optimal converter designs based on the design objectives.
- Form the multi-objective design space using analytical modeling and simulation.
- Choose an optimal point of design, and verify the design method with the experimental prototype.

Last but not least, when the power modules can be selected and designed, the third research question is:

3. *How to operate the power modules in the charging system to achieve higher efficiency and utilization?*

The methodology to tackle this research question is as follows:

- Conduct literature reviews on possible lithium-ion battery charging strategies.
- Investigate the influence of charging strategy on power converters among the evaluation criteria.
- Simulate and compare the performance of the power modules with different charging strategies. The evaluation criteria is the efficiency of the power converter over the whole charging cycle, and the utilization rate of the installed power.
- Study the multiplexing method, and investigate how to achieve flexible power distribution by multiplexing method.
- Verify the feasibility of multiplexing by a scaled-down prototype consisting of at least 2 power modules.

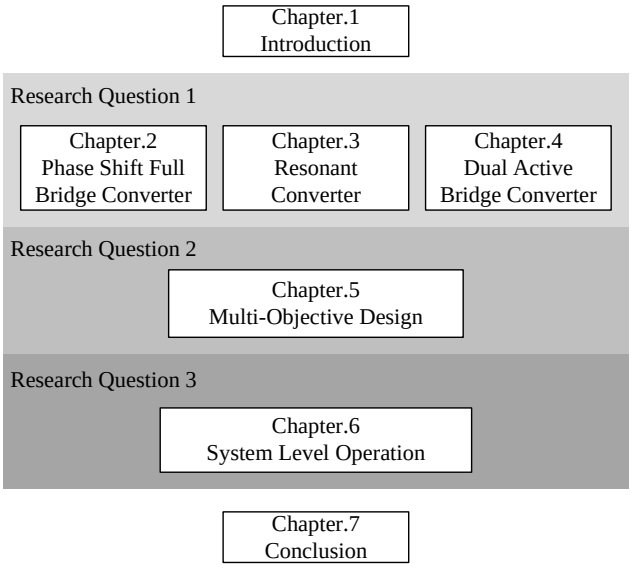

Figure 1.5: The outline of this thesis

1.4. OUTLINE OF THE THESIS

This thesis tries to answer the research questions and present the research outcomes. Figure 1.5 shows the outline of this thesis.

Chapters 2, 3, and 4 address research question 1 by presenting the design and evaluation of advantageous DC/DC converters that can be used for the wide voltage range EV charging application. More specifically, chapter 2 introduces the reconfigurable phase shift full bridge converter design, chapter 3 the reconfigurable resonant converter design, and Chapter 4 the dual active bridge converter design with a novel modulation method. The research question 2 is addressed in Chapter 5, where a multi-objective power electronic converter design process is proposed to optimize the efficiency performance, power density, and cost. Chapter 6 tackles research question 3 by investigating the impacts of the lithium-ion battery charging strategies and conducting a survey on the charging system structure. Finally, the conclusion is summarized in Chapter 7, and some future works are discussed.

1.5. THE DESIGN REQUIREMENTS

The design restrictions of the isolated back-end DC/DC converter of the EV chargers are obtained by studying the EV charger standards, including the CHADEMO and IEC 61851 standards of electric vehicle conductive charging system, Part 23: DC electric vehicle charging station [13].

1. Isolation requirements: the secondary circuit(output side) of the DC supply shall be designed as an IT (isolated terra) system, and protection measures in accordance with 411 of IEC 60364-4-41:2005 shall be applied. In addition, if the DCEV

charging station has multiple DC outputs designed for simultaneous operation, each output circuit shall be isolated from each other by basic insulation or reinforced insulation.

2. The minimum input voltage $V_{in(min)} = 540V$. This is the result of the 600V output of a conventional three-phase rectifier considering the 10% mains dip.

3. The maximum input voltage $V_{in(max)} = 900V$. By limiting the maximum input voltage, the 1200V semiconductor device could be better utilized. otherwise higher voltage rating devices should be considered.

4. The minimum output voltage $V_{out(min)} = 150V$. This is the minimum output voltage stated in the chademo standard. In the IEC61851 standard, the minimum output voltage is 50V, but from a fast charging point of view, with a 50V output voltage, the charging power is fairly low. Moreover, considering the trend of the increasing battery capacity, and higher demand of fast charging, the higher 150V is chosen as the minimum output voltage.

5. The maximum output voltage $V_{out(max)} = 1000V$. This is the maximum output voltage stated in IEC61851.

6. The maximum current ripple during CC phase (peak2peak) $I_{out,ripple(max)} = 9A$, as in IEC61851.

7. The maximum voltage ripple during CV phase (peak2peak) $V_{out,ripple(max)} = 10V$, as in IEC61851.

8. The minimum switching frequency $f_{sw(min)} = 15kHz$, to avoid the audible frequency band.

9. The maximum switching frequency $f_{sw(max)} = 150kHz$, to have easier EMC requirements.

10. The EV charger should be able to operate under ambient temperatures from -5 to 40 degrees celsius.

11. The maximum output current allowed is 125A for a 50kW charger, and 25A for a 10kW charger. This is because of the limitation of charging cable (non-liquid cooling)

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2

RECONFIGURABLE PHASE SHIFT FULL BRIDGE CONVERTER

This chapter analyzes, designs, and tests a re-configurable phase-shift full-bridge (r-PSFB) isolated DC/DC converter well suited for a wide voltage operating range. By controlling the auxiliary switches, a series or parallel connection can be realized on the secondary side of the converter. As a result, the r-PSFB converter can operate in an extremely wide voltage range without compromising the system efficiency. In this chapter, the characteristics of the r-PSFB converter and its design considerations are discussed in detail. An 11kW r-PSFB converter prototype with 640-840V input voltage and 250-1000V output voltage ranges is developed and tested to validate the analysis and efficiency of the designed converter. A comparative study against a conventional PSFB converter is conducted for benchmark purposes to prove the advantages of the studied r-PSFB converter.[1]

[1] This Chapter is based on:
D. Lyu, T. B. Soeiro and P. Bauer, "Design and Implementation of a Reconfigurable Phase Shift Full-Bridge Converter for Wide Voltage Range EV Charging Application," in IEEE Transactions on Transportation Electrification, vol. 9, no. 1, pp. 1200-1214, March 2023, doi: 10.1109/TTE.2022.3176826.

2.1. INTRODUCTION

The Electric Vehicle (EV) market has been expanding with an unprecedented speed in the last decade. The EV cars stock market nearly doubled from 2018 to 2020, as shown in [1]. Along with this trend, rises the demand for public EV charging stations. While the most common EV battery voltage architecture is 400V, adopted by many manufacturers, namely, Tesla, Nissan, etc., new high-end EV models with 800V battery voltage architectures are introduced to the market. Examples are Porsche Taycan [2], Hyundai IONIQ 5 [3], Rapide E from Aston Martin [4], and Lucid Air from Lucid Motors [5]. Therefore, the challenge for the EV chargers is clear: to provide charging services to different cars, which will demand the power electronic circuits to operate with extremely wide battery voltage ranges.

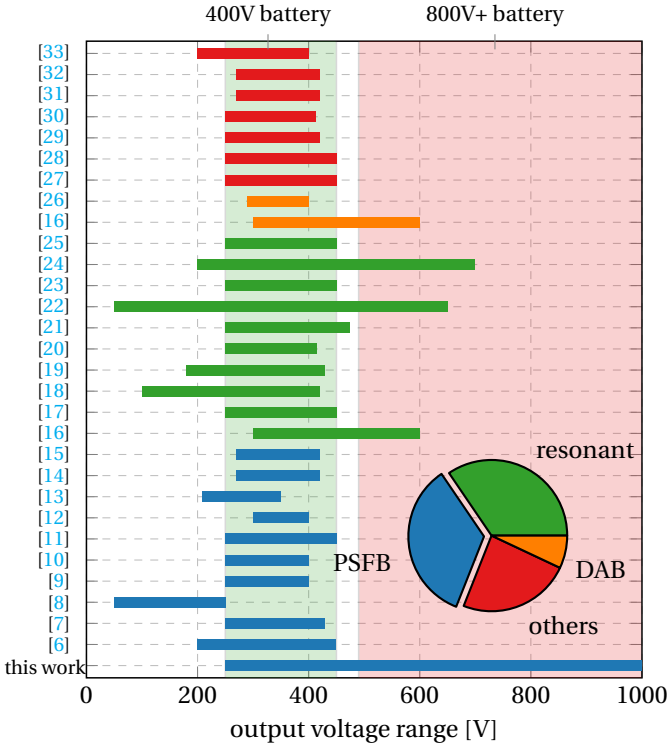


Figure 2.1: Output voltage ranges of the DC/DC converter prototypes reported in the literature from 2011 to 2021. (only the studies with prototype design and testing are included.)

However, according to the knowledge of the authors, there is no study in the literature that has provided experimentally verified isolated DC/DC converters for battery charging that is able to charge both the 400V and 800V EVs [6–33]. Figure 2.1 shows the output voltage ranges of the available literature of DC/DC converters researched for the EV charging application from the year of 2011 up to 2021. It is shown that, while most of the designs are focused on the 400V EV charging, none can charge both the 400V and

800V EVs.

The problem lies in the poor efficiency performance when these converters are made to operate in such a wide voltage range. As can be seen from Figure 2.1, the most popular isolated DC/DC converter topologies used in EV charging are the phase-shift full-bridge (PSFB) converter and the series resonant circuits.

PSFB converters are widely used in EV charging application [6–15]. For the PSFB type converter, the highest efficiency is obtained at the smallest phase shift, or in other words, the highest operating output voltage. And the efficiency will drop as the phase shift increases or the output voltage decreases. The work developed [7] proposes a hybrid-switching PSFB converter that provides a wide ZVS range for the leading leg and ZCS for the lagging leg. Interestingly, the freewheeling circulating losses can also be avoided, and the undesirable voltage overshoots can be clamped well. However, additional passive components (two diodes, a capacitor, and an inductor) are needed, and the complexity of the converter increases. The work in [8] proposes a secondary-side PSFB converter that extends the soft-switching operation and eliminates the circulating current, but it comes with the cost of two additional switches and more complex control. In [13] a ZVS full-bridge DC/DC converter is proposed, which incorporates a diode clamping circuitry on the primary side for the voltage ringing clamping, and uses an asymmetrical PWM modulation together with an additional auxiliary inductor to reduce circulating losses.

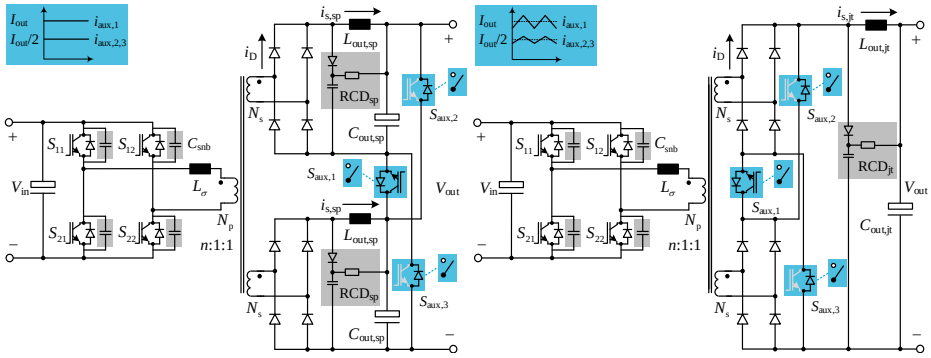
Due to its simple structure and ability of soft-switching, resonant converters are also widely used for EV charging [16–25]. The resonant converter is typically controlled by frequency modulation. The highest efficiency is typically achieved when the switching frequency is close to the resonant frequency in the inductive region of the resonant tank, i.e., when the converter voltage gain is mostly given by the transformer turns ratio, and the H-bridge inverter operates with Zero-Voltage-Switching (ZVS) turn-on. The efficiency of the resonant converter will drop when the voltage regulation is necessary, particularly at low voltage values where the circuit has to operate deeply in the inductive equivalent impedance of the resonant tank. In order to improve the ZVS performance and efficiency of the resonant converter in the wide output voltage range EV charging application, the work in [18] proposes to connect the LLC converter to a SEPIC converter. The SEPIC converter can follow the EV battery voltage and provide a wide DC link voltage range so that the LLC converter can always operate in proximity of the resonant frequency. The work in [19] proposes to reduce the switching frequency range of the LLC converter by adding delay-time control on the secondary side rectifier switches, which unavoidably increases the cost and complexity of the converter. The authors of [22] suggest the addition of a BUCK converter to the LLC converter so that the LLC converter operates with a fixed switching frequency, and the BUCK converter is responsible for the voltage regulation. However, the BUCK converter still suffers from an efficiency drop when operated at a low duty cycle. In [24] a three-level CLLC resonant converter is presented whereby combining the working modes of the three-level full-bridges, the voltage regulation range is extended while the controllable switching frequency is kept within a reasonable range. The work in [25] introduces an asymmetric parameters methodology for designing the CLLC converter for EV charging application so that the switching frequency range can be reduced for the bi-direction EV charging application.

Unfortunately, none of these researches have investigated the charging of 800V EVs,

and no experimental results have shown high-efficiency performance in the operation range of 400V and 800V EV charging, which is crucial for the current and future EV charging application. Moreover, when the charging voltage up to 1000V has to be considered, the usage of rectifier diodes with 1700V voltage rating becomes necessary if the aforementioned topologies are used, which are more commercially limited and less compatible compared to the 650V and 1200V ones, which have a broad application range in several other markets.

In order to extend the output voltage conversion range of a PSFB converter without compromising the system efficiency performance in the whole operational range, Sun et al. (2011) [34] proposed the idea of a re-configurable structure PSFB converter, which can be re-configurable by connecting its two isolated outputs in series for high voltage operation and in parallel for high current operation. This idea is further extended in [35–38], where a wide input voltage range of 100-400V and output voltage range of 15-96V is realized with more re-configurable steps on the secondary side, and one more switching leg on the primary side to enable the series and parallel re-configuration in the primary side. Since this idea of re-configurable structure also enables the utilization of lower current and voltage rating devices on the secondary sides and does not bring extra complexity to the control stage, it seems well suited for the wide output voltage EV charging application. The paper from Sun et al., [34] focuses on the design of a constant peak power protection control scheme for the circuit, a nonlinear smooth transition control method for the two configurations and the stability analysis of the re-configurable structure. The works presented in [35–38] describe more in detail the circuit operation principle, and design considerations including the separate transformer design for better thermal management, ZVS performance and loss calculation for the re-configurable PSFB converter. However, the steady-state analytical model for calculating the current stresses of the circuit's components, which requires adjustments to that of the conventional PSFB converter, is not elaborated. The voltage ringing issue on the secondary side, which is inherent for the PSFB type converter, is not addressed in these works. Whereas in the EV charging application, where the output voltage is up to 1000V, the voltage ringing needs to be well-clamped to ensure the safe operation of the rectifier diodes. Moreover, the aforementioned works have not considered different output filter structures, which require different numbers and voltage/current ratings of the filter components. This trade-off has to be examined in the EV charging application. Last but not least, no actual benchmark comparison between the re-configurable PSFB converter and the conventional PSFB converter has been carried out for the wide voltage range necessary for the EV charging application.

This chapter designs and implements a re-configurable phase-shift full-bridge (r-PSFB) converter based on the idea of the wide output range and constant peak power (RS-WOCP) converter from Sun et al. [34] for the wide output voltage EV charging application. Compared to a traditional PSFB converter, the operational phase shift angle of the converter during the charging of the low voltage battery is reduced, resulting in high efficiency in a larger operational output voltage range. In the series connection mode, the output voltage of the converter is twice that of a single secondary side, allowing the converter to charge up to 1000V without the necessity of employing higher voltage rating devices (e.g., 1700V Shottky diodes). While in the parallel connection mode, the con-



(a) separate output filter and RCD snubber (selected topology)

(b) joint output filter and RCD snubber

Figure 2.2: r-PSFB converter with separate or joint output filter and RCD snubber, with $i_{aux,1,2,3}$ illustrated. Note that $S_{aux,1,2,3}$ can be either mechanical switches or semiconductor transistors. The separate output filter structure is chosen in this work for further analysis and design.

verter can charge the 400V EVs more efficiently due to the reduced current stresses on the components. Another important point to highlight is that most of the conventional EVs designed for the lower cost mass-market will employ the conventional 400V battery. Therefore, an EV charger may be mostly used for this voltage class. Based on this, it is wise to implement circuits where high power efficiency is found within the 400V battery charging profile, even if the output voltage range covers the 800V battery charging. Unfortunately, the conventional PSFB and most resonant converters used for EV charging would feature a BUCK-type regulation, and naturally, the peak efficiency range would be found at the highest voltage range, i.e., the 800V EV battery class. This technical feature highlights the suitability of the r-PSFB converter for the application of EV charging.

The contribution of this chapter is as follows:

1. Extended analysis and comparison of the two possible output filter and snubber circuitry structures of the r-PSFB converter.

2. The detailed steady-state model of the r-PSFB converter is presented and verified, while the modification to the conventional PSFB converter is explained thoroughly.

3. The complete design guideline of the r-PSFB converter is elaborated, including the essential snubber circuitry design.

4. The benchmark design of an 11kW r-PSFB converter and conventional PSFB converter for the wide output voltage range (250-1000V) EV charging application is presented, which was not yet elaborated in the literature. This is particularly important because it identifies the r-PSFB converter as an outstanding solution for the future EV market.

5. The experimental results show excellent charging cycle efficiency for both 400V and 800V EV battery charging, and a peak efficiency of 98.3% using SiC switches,

which is among the highest reported in the available literature analyzing the PSFB converter in the EV charging application with proven prototype experimental results.

2.2. THE OPERATIONAL PRINCIPLE AND ANALYTICAL MODELING

There are two possible structures that can be implemented for the r-PSFB converter, namely the separate output filter structure, and the joint output filter structure. Figure 2.2 shows the circuit schematics of these two possible r-PSFB converters. Three-winding transformer is used, which has one primary and two secondary windings, with the turns ratio $n:1:1$. The primary side is fed by the DC input voltage V_{in} and a full-bridge inverter. An equivalent leakage inductance L_σ is present in the primary side, which is utilized for the ZVS turn-on of the transistors. Each of the secondary sides is connected to a diode bridge rectifier. For the separate output filter structure as shown in Figure 2.2a, each diode-bridge rectifier is connected to an output filter, L_{out} and C_{out}, and a RCD snubber circuitry. Three auxiliary switches, $S_{\text{aux},1,2,3}$, connect the two secondary sides and enable two different configurations according to their switching states. For the joint output filter structure as shown in Figure 2.2b, the two diode-bridge rectifiers are firstly connected to $S_{\text{aux},1,2,3}$, and they share a common output filter and RCD snubber. The RCD snubber circuitry is used for mitigating the voltage spikes on the secondary side diodes [39]. The lossless turn-off snubber C_{snb} for the H-bridge is also shown in the primary side of the transformer. The auxiliary switches can be implemented by either mechanical switches or semiconductor transistors, as shown in Figure 2.2.

2.2.1. RE-CONFIGURATION BY THE AUXILIARY SWITCHES

In an EV charging session, before the actual energy transfer happens, there is a communication period. During this period, the EV will inform the charger about the required charging voltage and current value [40]. By comparing the voltage value to a preset boundary voltage value V_{re}, the r-PSFB converter can be configured into a parallel connection configuration if the required charging voltage value is lower or as a series connection if the value is higher, by setting the states of the auxiliary switches $S_{\text{aux},1,2,3}$. It is important to mention that the r-PSFB converter does not need to change the configuration during operation in the EV charging application. This is because the voltage range of the 400V EVs does not overlap with the 800V EVs [41]. Therefore, the boundary voltage value V_{re} can be set to be higher than the maximum charging voltage of the 400V EV batteries and lower than the minimum charging voltage of the 800V ones, such as 500V. As a result, the converter operates only in series connection when charging 400V EVs and operates only in parallel connection when charging 800V EVs. With this mechanism, the use of mechanical switches as the auxiliary switches for the re-configuration, such as relays, is possible, which has less cost and lower equivalent conduction resistance. The detailed explanation is as follows.

SERIES CONNECTION

When $S_{aux,1}$ is kept on while $S_{aux,2,3}$ are maintained off, the negative rail of the upper rectifier is connected with the positive rail of the lower rectifier, making the two secondary side circuits connected in series. This configuration, in principle, enables the converter to supply high output voltage with the utilization of diodes and capacitors with halved voltage rating compared to those of the conventional approach.

PARALLEL CONNECTION

When $S_{aux,1}$ is kept off while $S_{aux,2,3}$ are maintained on, the positive and negative rails of the two rectifiers are connected in parallel. The parallel connection configuration enables the converter to operate in the low output voltage range with lower current stresses on the components.

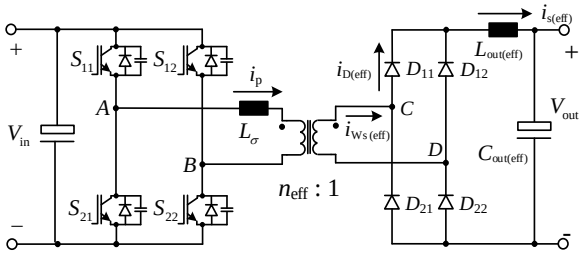


Figure 2.3: The equivalent circuit of Figure 2.2a without the RCD snubber circuits

2.2.2. COMPARISON BETWEEN THE TWO STRUCTURES OF THE R-PSFB CONVERTER

While the primary side H-bridge, transformer, and secondary side rectifier diode bridges are identical, the two different structures shown in Figure 2.2 have differences regarding the output LC filter, the RCD clamping snubber circuitry, and the auxiliary switches.

From the perspective of the component counts, the separate output filter structure has double component counts for the RCD snubber circuitry and LC filter.

However, the separate output filter structure enables the usage of low voltage rating diodes and capacitors for D_{RCD}, C_{RCD} and C_{out}, whose voltage rating is half compared to that of the joint output filter structure. This is particularly interesting in the EV charging application where the voltage is up to 1000V, as it enables the usage of 1200V or even lower voltage rating diodes for the RCD circuitry, which is much more commercially available and compatible compared to the 1700V diodes that have to be used in the joint output filter structure. From the perspective of cost, components with lower voltage ratings usually have lower costs. Thus the usage of halved voltage rating components counters the double components count.

Additionally, the separate output filter structure has slightly lower current and voltage stress on $S_{aux,1,2,3}$. Placing before L_{out}, $S_{aux,1,2,3}$ in the joint structure need to block the rectifier diode bridge voltage, and the current passing through has the current ripple that is determined by L_{out}. In comparison, in the separate structure, $S_{aux,1,2,3}$ need to block the output voltage, and the current through $S_{aux,1,2,3}$ in the separate structure

equals the average of that of the joint structure, but without the current ripple. As a result, the separate structure enables the usage of slightly lower current/voltage rating switches for $S_{aux,1,2,3}$, or has less conduction loss compared to the joint structure when the same switches are used. The comparison of the current and voltage stresses between the separate and joint structure is summarized in Table 2.1. V_{cp} represents the clamping voltage determined by the RCD clamping snubber circuitry, which will be further explained in Section V.

Table 2.1: The comparison of the current and voltage stresses between Figure 2.2a and Figure 2.2b

	separate structure	joint structure
V_{stress} of D_{RCD}	V_{cp}	$2V_{cp}$
V_{stress} of C_{RCD}	V_{cp}	$2V_{cp}$
V_{stress} of C_{out}	$V_{out}/2$	V_{out}
V_{stress} of $S_{aux,1}$	V_{out}	$2V_{cp}$
V_{stress} of $S_{aux,2,3}$	$V_{out}/2$	V_{cp}
I_{stress} of $S_{aux,1}$	I_{out}	$i_{s,jt}$
I_{stress} of $S_{aux,2,3}$	$I_{out}/2$	$i_{s,jt}/2$

Moreover, the separate output filter structure has a better performance clamping the diode voltage on the two secondary sides because the two separate output capacitors help share the output current evenly on the two secondary sides. On the other hand, in the joint filter structure, the diode voltage on the two secondary sides is prone to uneven sharing due to the mismatch of the diode resistance between the two sides. As a result, the joint output filter structure has a higher risk of over-voltage on the diodes.

Last but not least, the separate output filter structure facilitates thermal distribution, as the losses are divided into two parts instead of concentrating on one spot.

In conclusion, in the EV charging application, the halved voltage stress, less current stress, better voltage clamping, and thermal distribution of the separate structure shown in Figure 2.2a prevails over the higher component counts compared to the joint structure shown in Figure 2.2b. The joint structure can be a better candidate in the low power/voltage application, where the usage of the common 650/1200V diodes is possible, and the inductor does not have a severe thermal issue. The r-PSFB converter with the separate output filter and RCD snubber will be further analyzed and designed in this work.

2.2.3. OPERATING PRINCIPLE

Being either the series or parallel connection configuration, the r-PSFB converter shown in Figure 2.2a can be seen as equivalent to a conventional PSFB with a turns ratio of n_{eff} : 1, an output inductor $L_{out(eff)}$, and an output capacitor $C_{out(eff)}$, whose values change for the two configurations. Figure 2.3 shows the schematics of the equivalent conventional PSFB converter of the r-PSFB converter, and Table 2.2 lists the equivalent circuit

parameters for the series and parallel configurations.

Table 2.2: The circuit parameters in the equivalent PSFB shown in Figure 2.3

	series connection	**parallel connection**
$S_{\text{aux,1,2,3}}$	1,0,0	0,1,1
n_{eff}	$n/2$	n
$L_{\text{out(eff)}}$	$2L_{\text{out,sp}}$	$L_{\text{out,sp}}/2$
$C_{\text{out(eff)}}$	$C_{\text{out,sp}}/2$	$2C_{\text{out,sp}}$
$i_{\text{Ws(eff)}}$	i_{Ws}	$2i_{\text{Ws}}$
$i_{\text{D(eff)}}$	i_{D}	$2i_{\text{D}}$
$i_{\text{s(eff)}}$	$i_{\text{s,sp}}$	$2i_{\text{s,sp}}$

Like the conventional PSFB converter, the r-PSFB converter is typically controlled with fixed switching frequency by phase-shift modulation where the two half-bridge legs are operated with 50% duty cycle. The phase-shift refers to the asynchronization between the operation of the two half-bridge legs. When the phase shift is null, the diagonal pair of transistors (S_{11} & S_{22}, or S_{12} & S_{21}) turn on and off synchronously, making the primary side voltage v_{AB} alternate between $+V_{\text{in}}$ and $-V_{\text{in}}$, which is equivalent to a bipolar modulation of the H-bridge inverter. When the phase shift is non-null, the synchronization is broken, and the parallel pair of transistors (S_{11} & S_{12}, S_{21} & S_{22}) are able to be kept turned on at the same time, creating a third circuit state that is $v_{\text{AB}} = 0V$, leading to a controllable unipolor modulation action. Due to the impressed i_{p} caused by L_σ and inverter bridge capacitance the switching transition in each half-bridge leg creates a lowered di_{p}/dt and dv_{AB}/dt on the primary side, making the ZVS turn-on possible and lowering the turn-off losses of the transistors. Figure 2.4 shows the typical switching signals and current waveform of the PSFB converter in continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

The operation can be divided into 5 phases: the active phase where the diagonal transistors conduct ($T_1 - T_2$); the reactive phase where the parallel transistors conduct ($T_2^{'} - T_3$); the commutation phase where the secondary side current commutes among the rectifier diodes ($T_3^{'} - T_4$); and two transition phases during the dead-time of each bridge ($T_2 - T_2^{'}$ and $T_3 - T_3^{'}$). A complete description of the operation of a PSFB converter can be found in [42]. The r-PSFB converter can be modeled in the same way as an equivalent PSFB converter with the relation shown in Table 2.2.

2.2.4. STEADY STATE ANALYTICAL MODELING OF THE R-PSFB CONVERTER

The steady state analytical model of the r-PSFB in CCM and DCM is introduced and verified by simulation in this section. For the simplicity of the circuit analysis, the following assumption is made:

- $T_2 = T_2^{'}$, $I_{\text{p2}} = I_{\text{p2}}^{'}$, $I_{\text{s2}} = I_{\text{s2}}^{'}$

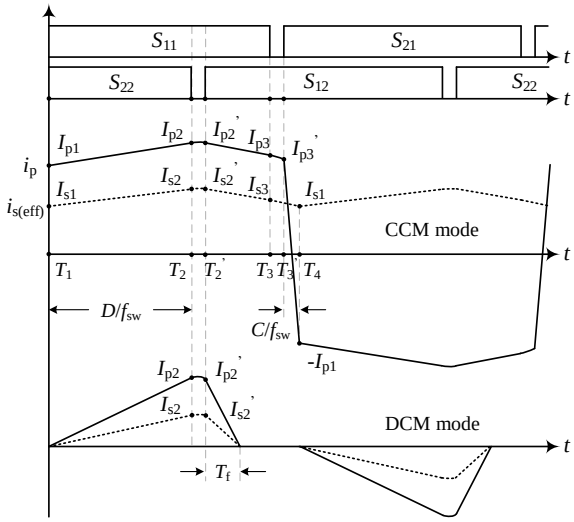


Figure 2.4: The typical switching signals and current waveform of the PSFB converter in CCM and DCM

- $T_3 = T_3^{'}$, $I_{p3} = I_{p3}^{'}$

This is because the transition phases are very short (tens or several hundred nanoseconds) compared to the other three phases. The influence of them on the overall current waveform is therefore negligible.

Firstly, the initial inductor current I_{s1} can be calculated according to Equation (2.1):

$$I_{s1} = I_{out} - \frac{V_{out}(V_{in(ref)} - V_{out})}{4 f_{sw} L_{total(ref)} V_{in(ref)}} \tag{2.1}$$

Where $V_{in(ref)}$ and $L_{total(ref)}$ are the reflected input voltage and the total inductance value seen from the secondary side, respectively, and they are calculated by:

$$V_{in(ref)} = V_{in} / n_{eff} \tag{2.2}$$

$$L_{total(ref)} = L_{\sigma(ref)} + L_{out(eff)} = L_{\sigma} / n_{eff}^2 + L_{out(eff)} \tag{2.3}$$

If $I_{s1} \geq 0$, the converter operates in CCM, otherwise, it works in DCM. In CCM, the duty cycle D is calculated as in **??**, and the commutation cycle C is calculated according to **??**. In DCM, the current starts from zero, thus, $I_{s1} = 0$. The duty cycle D in DCM is calculated differently, as Equation (2.8).

With I_{s1}, D and C calculated, $I_{s2,3}$ and $I_{p1,2,3}$ can be determined based on the voltage-second balance on the inductor. I_{s2} can be calculated by Equation (2.4) for both CCM and DCM operation.

$$I_{s2} = I_{s1} + \frac{D(V_{in(ref)} - V_{out})}{2 f_{sw} L_{total(ref)}} \tag{2.4}$$

Table 2.3: The closed-form steady state analytical model of the current stresses on the transistors of the r-PSFB converter. Herein, it is assumed that the body diodes of the MOSFETs do not conduct and thus the MOSFET channels process the whole impressed current.

		IGBT	MOSFET
CCM	$I_{\mathrm{S(lead),rms}}$	$\sqrt{((I_{\mathrm{s1}}^2+I_{\mathrm{s1}}I_{\mathrm{s2}}+I_{\mathrm{s2}}^2)D+2I_{\mathrm{s1}}^2T_{\mathrm{02n}}f_{\mathrm{sw}})/(6n_{\mathrm{eff}}^2)}$	$\sqrt{(-(I_{\mathrm{s2}}+I_{\mathrm{s3}})(I_{\mathrm{s2}}+I_{\mathrm{s1}}-I_{\mathrm{s3}})C+I_{\mathrm{s1}}^2+I_{\mathrm{s2}}I_{\mathrm{s1}}+I_{\mathrm{s2}}^2)/(6n_{\mathrm{eff}}^2)}$
	$I_{\mathrm{S(lead),avg}}$	$((I_{\mathrm{s1}}+I_{\mathrm{s2}})D+2I_{\mathrm{s1}}T_{\mathrm{02n}}f_{\mathrm{sw}})/(4n_{\mathrm{eff}})$	$((2C+2D-1)I_{\mathrm{s1}}+(C+2D-1)I_{\mathrm{s2}}-CI_{\mathrm{s3}})/(4n_{\mathrm{eff}})$
	$I_{\mathrm{AD(lead),rms}}$	$\sqrt{((1-D-C)(I_{\mathrm{s1}}^2+I_{\mathrm{s2}}^2+I_{\mathrm{s1}}I_{\mathrm{s2}})+2f_{\mathrm{sw}}I_{\mathrm{s3}}^2T_{\mathrm{p20}})/(6n_{\mathrm{eff}}^2)}$	0
	$I_{\mathrm{AD(lead),avg}}$	$((1-D-C)(I_{\mathrm{s1}}+I_{\mathrm{s2}})+2f_{\mathrm{sw}}I_{\mathrm{s3}}T_{\mathrm{p20}})/(4n_{\mathrm{eff}})$	0
	$I_{\mathrm{S(lagg),rms}}$	$\sqrt{((2f_{\mathrm{sw}}T_{\mathrm{02n}}-1C+1)I_{\mathrm{s1}}^2-I_{\mathrm{s1}}(C-1)I_{\mathrm{s2}}-I_{\mathrm{s2}}^2(C-1))/(6n_{\mathrm{eff}}^2)}$	$\sqrt{(-(I_{\mathrm{s2}}+I_{\mathrm{s3}})(I_{\mathrm{s2}}+I_{\mathrm{s1}}-I_{\mathrm{s3}})C+I_{\mathrm{s1}}^2+I_{\mathrm{s2}}I_{\mathrm{s1}}+I_{\mathrm{s2}}^2)/(6n_{\mathrm{eff}}^2)}$
	$I_{\mathrm{S(lagg),avg}}$	$((2f_{\mathrm{sw}}T_{\mathrm{02n}}-C+1)I_{\mathrm{s1}}-I_{\mathrm{s2}}(C-1))/(4n_{\mathrm{eff}})$	$(-CI_{\mathrm{s2}}-CI_{\mathrm{s3}}+I_{\mathrm{s1}}+I_{\mathrm{s2}})/(4n_{\mathrm{eff}})$
	$I_{\mathrm{AD(lagg),rms}}$	$\sqrt{f_{\mathrm{sw}}I_{\mathrm{s3}}^2T_{\mathrm{p20}}/(3n_{\mathrm{eff}}^2)}$	0
	$I_{\mathrm{AD(lagg),avg}}$	$f_{\mathrm{sw}}I_{\mathrm{s3}}T_{\mathrm{p20}}/(2n_{\mathrm{eff}})$	0
DCM	$I_{\mathrm{S(lead),rms}}$	$\sqrt{I_{\mathrm{s2}}^2D/(6n_{\mathrm{eff}}^2)}$	$\sqrt{I_{\mathrm{s2}}^2(2f_{\mathrm{sw}}T_{\mathrm{f}}+D)/(6n_{\mathrm{eff}}^2)}$
	$I_{\mathrm{S(lead),avg}}$	$I_{\mathrm{s2}}D/(4n_{\mathrm{eff}})$	$I_{\mathrm{s2}}(-2f_{\mathrm{sw}}T_{\mathrm{f}}+D)/(4n_{\mathrm{eff}})$
	$I_{\mathrm{AD(lead),rms}}$	$\sqrt{f_{\mathrm{sw}}I_{\mathrm{s2}}^2T_{\mathrm{f}}/(3n_{\mathrm{eff}}^2)}$	0
	$I_{\mathrm{AD(lead),avg}}$	$f_{\mathrm{sw}}I_{\mathrm{s2}}T_{\mathrm{f}}/(2n_{\mathrm{eff}})$	0
	$I_{\mathrm{S(lagg),rms}}$	$\sqrt{I_{\mathrm{s2}}^2(2f_{\mathrm{sw}}T_{\mathrm{f}}+D)/(6n_{\mathrm{eff}}^2)}$	$\sqrt{I_{\mathrm{s2}}^2(2f_{\mathrm{sw}}T_{\mathrm{f}}+D)/(6n_{\mathrm{eff}}^2)}$
	$I_{\mathrm{S(lagg),avg}}$	$I_{\mathrm{s2}}(2f_{\mathrm{sw}}T_{\mathrm{f}}+D)/(4n_{\mathrm{eff}})$	$I_{\mathrm{s2}}(2f_{\mathrm{sw}}T_{\mathrm{f}}+D)/(4n_{\mathrm{eff}})$
	$I_{\mathrm{AD(lagg),rms}}$	0	0
	$I_{\mathrm{AD(lagg),avg}}$	0	0

$$D^{\mathrm{DCM}}=2\sqrt{\frac{I_{\mathrm{out}}V_{\mathrm{out}}f_{\mathrm{sw}}L_{\mathrm{total(ref)}}}{V_{\mathrm{in(ref)}}(V_{\mathrm{out}}-V_{\mathrm{in(ref)}})}} \tag{2.8}$$

$$T_{\mathrm{p20,02n}}=I_{\mathrm{p3,p1}}\cdot L_{\sigma}/V_{\mathrm{in}} \tag{2.9}$$

$$T_{\mathrm{f}}=I_{\mathrm{s2}}\cdot L_{\mathrm{total(ref)}}/V_{\mathrm{out}} \tag{2.10}$$

The effective rms and average current stress on the secondary side diodes $I_{\mathrm{D,rms/avg(eff)}}$ can be calculated by Equations (2.11) to (2.13). Depending on the configuration, the actual diode current stress can be calculated from the effective value based on Table 2.2.

$$I_{\mathrm{D,rms(eff)}}^{\mathrm{CCM}} = \sqrt{(1-C)(I_{\mathrm{s2}}^2 + I_{\mathrm{s1}} I_{\mathrm{s2}}) + C I_{\mathrm{s3}}^2 + I_{\mathrm{s1}}^2/6} \tag{2.11}$$

$$I_{\mathrm{D,rms(eff)}}^{\mathrm{DCM}} = \sqrt{I_{\mathrm{s2}}^2 (2 f_{\mathrm{sw}} T_{\mathrm{f}} + D^{\mathrm{DCM}})/6} \tag{2.12}$$

$$I_{\mathrm{D,avg(eff)}} = I_{\mathrm{out}}/2 \tag{2.13}$$

The rms current stress on the primary winding of the transformer, $I_{\mathrm{Wp,rms}}$, can be calculated based on Equations (2.14) and (2.15) in CCM and DCM operation respectively.

$$I_{\mathrm{Wp,rms}}^{\mathrm{CCM}} = \sqrt{\frac{-(I_{s2}+I_{s3})(I_{s2}+I_{s1}-I_{s3})C + I_{s1}^2 + I_{s2} I_{s1} + I_{s2}^2}{3 n_{\mathrm{eff}}^2}} \tag{2.14}$$

$$I_{\mathrm{Wp,rms}}^{\mathrm{DCM}} = \sqrt{\frac{I_{\mathrm{s2}}^2 (2 f_{\mathrm{sw}} T_{\mathrm{f}} + D^{\mathrm{DCM}})}{3 n_{\mathrm{eff}}^2}} \tag{2.15}$$

The effective rms current stress on the secondary winding of the transformer, $I_{\mathrm{Ws,rms(eff)}}$, can be calculated using the turns ratio n_{eff} by Equation (2.16). Depends on the configuration, the actual secondary winding current can be calculated from the effective value based on the conversion shown in Table 2.2.

$$I_{\mathrm{Ws,rms(eff)}} = I_{\mathrm{Wp,rms}} \cdot n_{\mathrm{eff}} \tag{2.16}$$

In order to show the accuracy of the analytical model, LTspice simulation of a r-PSFB converter using IGBTs is conducted, and the simulation results of the current stresses on the semiconductors are compared to the analytical modeling results, as shown in Figure 2.5. The compared current stresses include the leading and lagging leg transistor rms and average current $I_{\mathrm{S(lead/lag),rms/avg}}$, the leading and lagging leg anti-parallel diode rms and average current $I_{\mathrm{AD(lead/lag),rms/avg}}$, and the secondary side rectifier diode rms and average current $I_{\mathrm{D,rms/avg}}$. It can be seen that the analytical model corresponds well with the simulation model.

2.3. DESIGN REQUIREMENTS OF THE POWER MODULE

The design requirements for the r-PSFB converter shown in Figure 2.2 are summarized in Table 2.4.

V_{out} is set to be 250-1000V, in which the converter operates in parallel connection mode within 250-500V, and in series connection mode within 500-1000V.

V_{in} is in the range of 640-840V, so that a battery energy storage device, such as a SAMSUNG ESS [43], can be connected to the DC bus between the typically employed grid-connected AC/DC rectifier and this DC/DC converter, allowing power buffering during charging, and consequently reducing the grid burden. Therefore, V_{in} is not a controllable parameter, which is different than some designs where the V_{in} could be controlled according to the output voltage [18, 23].

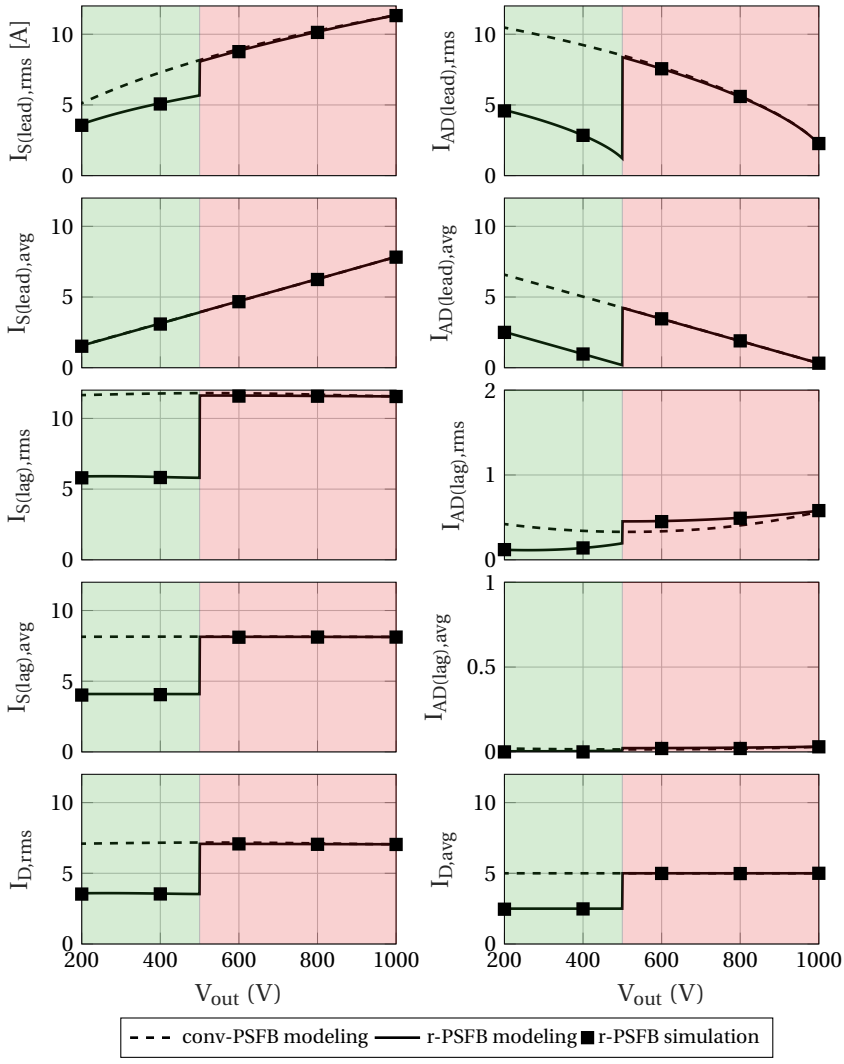


Figure 2.5: The analytical modeling and LTspice simulation results of the conventional PSFB and the r-PSFB converter (V_{in}=640V, I_{out}=10A, L_{σ}=10μH, using IGBT as transistors)

Table 2.4: Design requirements of the r-PSFB power module

requirements	values
input voltage V_{in} range	640-840V
output voltage V_{out} range	250-1000V
switching frequency f_{sw}	15kHz
power rating P	11kW
MAX output current $I_{out(max)}$	30A
MAX output current peak-to-peak ripple $I_{out,ripple(max)}$	9A
MAX output voltage peak-to-peak ripple $V_{out,ripple(max)}$	10V
MAX ambient temperature $T_{a(max)}$	40°C

The grid phase voltage in Europe is typically 230V±10%, which gives a maximum peak line-to-line voltage of 620V. Considering some non-ideal voltage drop on the circuitry and components, the minimum output voltage of the three-phase AC/DC converter is 640V.

The maximum input voltage is 840V, which is limited by the input battery, and this enables the usage of the 1200V voltage rating devices with a 30% safety margin taken into consideration.

The maximum output power is set to be 11kW to enable the utilization in household applications in the European market. The household three-phase wiring typically has a phase voltage rating of 230V and a current rating of 16A. Therefore, the maximum power that can be drawn without modification of the electric wiring is limited to 11kW.

$I_{out,ripple(max)}$ and $V_{out,ripple(max)}$ are set according to the current version of the charging standards IEC 61851-23:2014 [40].

2.4. DESIGN OF THE 11KW R-PSFB CONVERTER

2.4.1. BOUNDARY VOLTAGE VALUE OF RECONFIGURATION V_{RE} AND THE AUXILIARY SWITCHES

As it has been explained in Section II.B, the boundary voltage value of reconfiguration V_{re} is the voltage value below which the r-PSFB will be configured into a parallel connection configuration and above which it will be configured as a series connection configuration.

Since the voltage range of the 400V battery architecture is between 200V to 500V, and that of the 800V+ architecture is within the range from 500V to 1000V, V_{re} is set to be 500V, so that the converter can charge the 400V EVs in parallel connection configuration, and charge the 800V ones in series connection configuration.

2.4.2. TRANSFORMER TURNS RATIO n

The turns ratio can be determined based on the input and output voltage range and V_{re}. In order to be able to provide a maximum 500V output voltage in the parallel connection

configuration based on V_{re}, the transformer turns ratio considering 5% non-ideal voltage and duty cycle loss on the components, can be calculated as:

$$n = \frac{V_{in(min)}}{V_{re}} \cdot 95\% = 1.216 \tag{2.17}$$

This turns ratio can also ensure a maximum 1000V output voltage for the series connection configuration.

2.4.3. OUTPUT INDUCTANCE VALUE L_{OUT}

Based on the maximum current ripple requirement, the minimum output inductance value $L_{out(min)}$ could be set. The output current ripple in CCM, in which the current of the inductor is always above zero, can be calculated by:

$$I_{out,ripple} = \frac{V_{in,ref}(1-D)D}{L_{out}} \cdot \frac{1}{2f_{sw}} \tag{2.18}$$

$I_{out,ripple(max)}$ happens when $D = 0.5$, $V_{in} = V_{in(max)}$. Based on which $L_{out(min)}$ could be calculated as:

$$L_{out(min)} = 2 \cdot \frac{1}{2f_{sw}} \cdot \frac{V_{in(ref,max)}}{4I_{out,ripple(max)}} = 1.3\text{mH} \tag{2.19}$$

Note that in the parallel connection mode, the effective inductance value is half of L_{out} as shown in Table 2.2, thus in order to ensure the maximum current ripple requirement in the parallel connection configuration, the factor 2 in Equation (2.19) has to be considered.

2.4.4. OUTPUT CAPACITOR C_{OUT}

In the series connection mode of the r-PSFB converter, each of the output capacitor can have a voltage ripple of $0.5V_{out,ripple(max)}$, but at the same time, the maximum output current ripple can be reached in the series connection mode is only $0.5I_{out,ripple(max)}$ when the L_{out} value is designed according to Equation (2.19). As a result, the minimum capacitance value for the single output capacitor of the r-PSFB converter in the series connection mode operating in CCM can be calculated as:

$$C_{out(min)} = \frac{I_{out,ripple(max)}}{16f_{sw}V_{out,ripple(max)}} = 3.75\mu\text{F} \tag{2.20}$$

When it's in the parallel connection mode, each output capacitor needs to withstand $V_{out,ripple(max)}$, while the current ripple of each output inductor is $0.5I_{out,ripple(max)}$. As a result, in the parallel connection mode the minimum required output capacitance is halved compared to that of the series connection mode. Overall, the minimum output capacitance value of the r-PSFB converter equals $C_{out(min)}$ calculated in Equation (5.5).

In the actual experiment, C4AQLBW6130A3NK from KEMET is used for the prototype, which has a capacitance value of 130μF and voltage rating of 500V. The capacitance value is over-rated, but it facilitates the test of the prototype as it provides stable output voltage.

Table 2.5: Worst-case current and voltage stresses of the components for the 11kW conv-PSFB and the r-PSFB with the same design requirements as in Table 2.4, assuming $L_\sigma = 10\mu$H

		conv-PSFB	**r-PSFB**
worst-case current (A)	$I_{\text{IGBT(lead),rms(max)}}$	20.8	17.7
	$I_{\text{IGBT(lead),avg(max)}}$	8.8	8.7
	$I_{\text{ADIGBT(lead),rms(max)}}$	31.6	18.0
	$I_{\text{ADIGBT(lead),avg(max)}}$	20.3	9.0
	$I_{\text{IGBT(lag),rms(max)}}$	34.3	25.2
	$I_{\text{IGBT(lag),avg(max)}}$	23.9	17.6
	$I_{\text{ADIGBT(lag),rms(max)}}$	2.8	1.7
	$I_{\text{ADIGBT(lag),avg(max)}}$	0.3	0.1
	$I_{\text{D,rms(max)}}$	21.0	15.4
	$I_{\text{D,avg(max)}}$	15.0	11.0
worst-case voltage (V)	$V_{\text{IGBT(max)}}$	840	840
	$V_{\text{D(max)}}$	1382	690
desired V & I ratings (30% margin)	IGBT channel	1200V, 49A	1200V, 36A
	IGBT anti-parallel diode	1200V, 45A	1200V, 26A
	rectifier diode	1974V, 30A	986V, 22A
semiconductor choices	IGBT version	IKQ50N120CT2	IKW40N120CS6
	SiC MOSFET version	C3M0032120D	IMW120R030M1H
	rectifier diode	C5D25170H	IDW30G120C5B

2.4.5. SEMICONDUCTOR CHOICES

With the calculation of the transformer turns ratio n and the output inductance L_{out}, the worst-case current and voltage stresses on the components can be analyzed based on the analytical modeling if the leakage inductance value L_σ is defined, and based on which the current and voltage rating of the semiconductor components can be chosen.

Table 2.5 summarizes the worst-case current and voltage stresses for the semiconductor components assuming $L_\sigma = 10\mu$H, which is close to the value obtained in the designed transformer used in the prototype discussed in Section V. The current stresses are obtained from the analytical modeling, and the voltage stresses are based on the maximum input voltage and turns ratio n.

It can be seen that for the same design requirements, the r-PSFB converter experiences less current stresses on the primary side IGBTs (25.2A) than the conventional PSFB converter (34.3A), which means that lower current rating transistors can be utilized in the r-PSFB converter, resulting in lower costs as indicated in Figure 2.6. The primary reason is due to the parallel connection configuration. As can be seen from Figure 2.5, all the current stresses except $I_{\text{IGBT(lead),avg}}$, have almost halved current stresses when the circuit is in parallel connection configuration. Note that the maximum power requirement also limits the series connection operation for high output current cases. This is again beneficial for the current stresses as the converter always benefits from the current stresses reduction brought by the parallel connection configuration when the

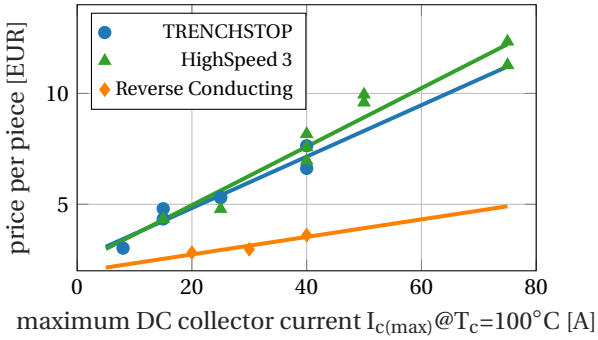


Figure 2.6: The cost v.s. current rating of different Infineon IGBT series. The cost is obtained from Digi-Key per piece on 02/26/2021.

output current is high. The same difference is seen in the current stresses of the secondary side rectifier diodes.

Moreover, the voltage stresses on the secondary-side rectifier diodes of the r-PSFB are halved compared to that of the conventional PSFB thanks to the series connection configuration, while the primary side voltage stresses on the transistors are the same. This allows the usage of cheaper and lower voltage rating diodes for the r-PSFB converter.

Considering a 30% safety margin for the current and voltage rating of the IGBT and diode, the ideal current/voltage ratings and the chosen semiconductor components are calculated and listed in Table 2.5. Note that, a SiC MOSFET is also selected in order to compare the performance against the IGBT version.

2.4.6. MAGNETIC COMPONENTS DESIGN

The procedure of the design of the magnetic components is shown in Figure 2.7. In order to avoid overly large number of solutions, the Litz wire gauge is set to be AWG 41, and the core material for the transformer is Ferrite N87, for the inductor is Metglas Amorphous Cut Core. Five design variables are considered for finding the optimal design. The core shape for the transformer is the EE cores, and for the inductor are the UU cores. The number of stacked cores is selected to be within 1 to 5 for transformer design, and 1 to 2 for inductor design. The current density allowed in the wires is set from 4.5×10^6 to $13.5 \times 10^6 A/m^2$. The maximum allowed flux density is set to 80% of the B_{sat} of the core material. The worst-case scenarios for the designs of the magnetic components happen when the winding currents are the maximum, which results in the most losses. For the conventional PSFB converter, the worst-case scenario is when $V_{\text{in}} = 840V$, $I_{\text{out}} = 30A$, $V_{\text{out}} = 366V$, and for the r-PSFB converter, the worst-case scenario is when $V_{\text{in}} = 840V$, $I_{\text{out}} = 22A$, $V_{\text{out}} = 500V$. The loss calculation is conducted using the method from [44]. Combining the total losses P_{mag} (W) and surface area A_{mag} (m^2) of the magnetic components, the temperature rise ΔT is estimated based on Equation (5.9) [45].

$$\Delta T = \left(\frac{P_{\text{mag}}}{10 \cdot A_{\text{mag}}}\right)^{0.833} \tag{2.21}$$

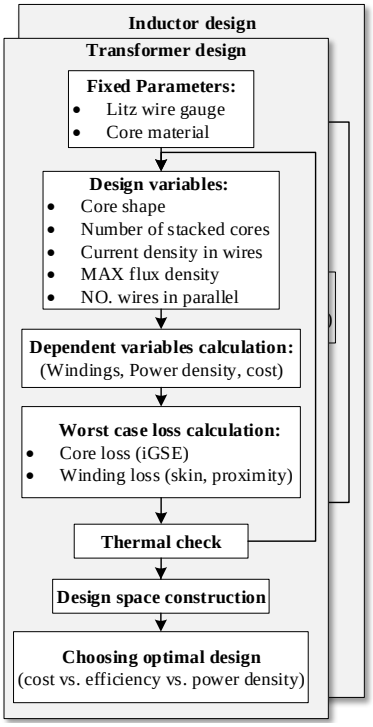


Figure 2.7: Design procedure for the magnetic components

The specifications of the chosen designs are listed in Table 2.6 and Table 2.7 respectively. The winding arrangement indicates the way how the primary and secondary windings are positioned. P-S-S indicates that the primary winding is wounded firstly, and then the two secondary windings on top of it.

There are two interesting observations from Tables 2.6 and 2.7. Firstly, even though the r-PSFB converter requires the transformer to have two secondary windings and two inductors, compared to the single secondary winding transformer and a single inductor for the conventional PSFB converter, it does not result in increments of total magnetic components losses and core material. This is because the winding current stresses on the magnetic components are more relaxed in the r-PSFB converter compared to its conventional counterpart. Secondly, it can be seen from Table 2.7 that the temperature rise of the two inductors of the r-PSFB converter is around 27°C lower than that of the conventional PSFB converter. This demonstrates that by having two separate inductors, the thermal management of the r-PSFB converter is simpler than the conventional PSFB converter, as the heat is distributed in two spots.

2.4.7. AUXILIARY SWITCHES

The auxiliary switches $S_{aux,1,2,3}$ can be implemented by using either semiconductor transistors or mechanical switches. Since the configuration of the r-PSFB converter is deter-

Table 2.6: The transformer designs for the conv-PSFB and r-PSFB converters

design specs	PSFB	r-PSFB
switching frequency f_{sw}	15-kHz	15-kHz
core material	Ferrite N87	Ferrite N87
core shape	EE 70/33/32	EE 70/33/32
No. cores stacked	5	5
Litz wire gauge	AWG 41	AWG 41
Litz wire strands (primary)	600	600
Litz wire strands (secondary)	600	600
No. parallel wires (primary)	2	2
No. parallel wires (secondary)	1	1
No. primary turns N_{prim}	8	12
No. secondary turns N_{sec}	13	10
winding arrangement	P-S	P-S-S
MAX flux density B_{max}	0.186-T	0.248-T
worst-case loss	66.3-W	61.5-W
temperature rise ΔT	54.6°C	50.2°C
power density	7.2-kW/L	7.1-kW/L

mined prior to the charging process, the auxiliary switches do not need to change during the operation of the converter. Therefore, the mechanical switch T9GV1L14-5 is chosen for $S_{aux,1,2,3}$ for the r-PSFB converter prototype, which is a power relay with 30A current rating. Compared with semiconductor transistors and diodes, the mechanical switches bring less conduction losses.

2.4.8. RCD SNUBBER CIRCUITRY

Figure 2.8 shows the schematic of the RCD clamping circuitry, with the reflected leakage inductor $L_{\sigma(ref)}$, transformer stray capacitor C_{tf} and rectifier diode junction capacitor C_{rec} highlighted. Due to the resonance between $L_{\sigma(ref)}$ and the combination of C_{tf} and C_{rec}, a voltage ringing will happen on the secondary side diodes, with a peak voltage value that can reach twice the value of the secondary winding voltage [39], which can be critical for the safe operation of the rectifier diodes. With the design requirements of this power module stated in Section III, the voltage ringing on the rectifier diodes of the r-PSFB converter, $V_{ringing}$, can be calculated as:

$$V_{ringing} = 2 \cdot \frac{V_{in,max}}{n} = 2 \cdot \frac{840}{1.2} = 1400V \tag{2.22}$$

which will cause over-voltage failure on the 1200V diodes. Therefore, the RCD clamped snubber circuitry is designed to clamp the voltage ringing to a reasonable value, V_{cp}, so

Table 2.7: The inductor designs for the conv-PSFB and r-PSFB converters

design specs	PSFB	r-PSFB
No.inductors	1	2
inductance L_{out}	1.3-mH	1.3-mH
switching frequency f_{sw}	15-kHz	15-kHz
core material	Metglas	Metglas
core shape	AMCC0080	AMCC0080
No. cores stacked	2	1
Litz wire gauge	AWG 41	AWG 41
Litz wire strands	600	600
No. parallel wires	2	2
No. turns N	34	48
MAX flux density B_{max}	1.248-T	1.248-T
air gap	1.6-mm	1.7-mm
worst-case loss (single)	70.2-W	28.3-W
temperature rise ΔT (single)	80.0°C	52.9°C
power density (total)	10.1-kW/L	7.9-kW/L

that a safe operation for the 1200V rectifier diodes is ensured.

Firstly, the capacitor of the RCD circuitry, C_{RCD}, is chosen to be 200nF, so that it can be regarded as a voltage clamping device with enough energy storage capacity. Secondly, the clamped voltage value V_{cp} of the r-PSFB converter is set to be 1000V, considering that 1200V diodes can be used. The resistance value of the resistor of the RCD circuitry, R_{RCD}, can be calculated according to Equation 2.23:

$$R_{RCD} = \frac{(V_{cp} - V_{o(max)}) \cdot (V_{cp} - V_{d(max)})}{f_{sw} \cdot C_{sec} \cdot V_{cp} \cdot (2V_{d(max)} - V_{cp})} \tag{2.23}$$

in which $V_{o(max)}$ and $V_{d(max)}$ are the maximum output and input voltage of the RCD circuitry, respectively. C_{sec} is the combination of C_{tf} and C_{rec}, which can be estimated by measuring the resonant frequency of the voltage ringing, with L_σ known. In this r-PSFB converter, C_{sec} is measured to be around 400pF, $V_{d,max} = 840/1.2 = 700V$, $V_{out,max} = 1000/2 = 500V$. Thus, based on Equation (2.23), 62kΩ resistors are chosen for the RCD snubber. Assuming the same C_{sec}, 5.2kΩ resistors are chosen for the conventional PSFB converter to clamp the diode voltage at around 1480V, while diodes with 1700V voltage ratings are used. The loss dissipated on R_{RCD} can be calculated by:

$$P_{RCD} = \frac{(V_{cp} - V_{out,max})^2}{R_{RCD}} \tag{2.24}$$

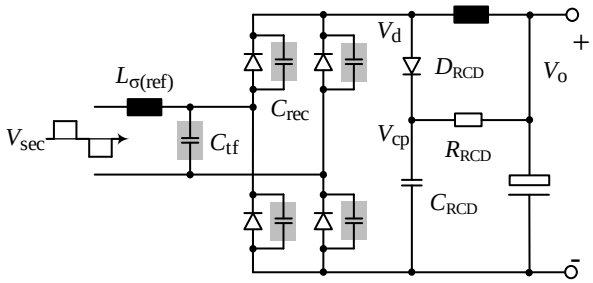


Figure 2.8: Schematic of the RCD clamping circuitry

2.5. EXPERIMENTAL RESULTS OF THE R-PSFB PROTOTYPE

Based on the designs in Section IV, an 11-kW, 640-840V input voltage, 250-1000V output voltage r-PSFB DC/DC converter prototype is built, and set-point open-loop tests are done to verify the efficiency performance of the system. Figure 2.9 shows the constructed prototype. The power density of the converter is 2.3kW/L. Table 2.8 lists the equipment used in the test.

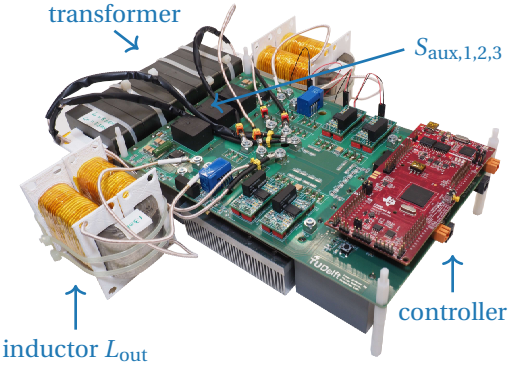


Figure 2.9: The 11kW r-PSFB converter prototype

Table 2.8: The equipment used in the experiment

	equipment model
microcontroller	TI TMS320F283790
input power supply	Delta Elektronika SM1500-CP-15
output electronic load	Delta Elektronika SM1500-CP-15
power analyzer	Yokogawa WT500
oscilloscope	Yokogawa DLM3000

Figures 2.10 and 2.11 shows the operational waveform of the r-PSFB converter in parallel and series connection modes under various V_{out} and I_{out} conditions.

From Figure 2.10, it can be seen that, in the parallel connection mode, the output current is shared between the two rectifiers, enabling the use of diodes with lower current rating compared to the conventional PSFB converter. When operating with 5A output current, as shown in Figure 2.10(a)(c)(e), the difference of current of the two secondary sides is unnoticeable. When operating with 30A output current, as shown in Figure 2.10(b)(d)(f), the current difference becomes observable. This uneven sharing of current is due to the difference of impedance of the two secondary sides, which can come from the transformer secondary winding, diode resistance and inductor impedance, and relay contact resistance. To have an even current sharing, screening on those components is needed to ensure identical impedance. However, even without screening, less than 2A of current difference is observed when this r-PSFB prototype is operating with $I_{out(max)}$, which is around 6.7% compared to $I_{out(max)}$. This demonstrates the feasibility of the parallel connection operation of the r-PSFB converter.

From Figure 2.11, it can be seen that, in the series connection mode, the output voltage is shared evenly between the two rectifiers, with less than 50V difference, enabling the use of diodes and capacitors with lower voltage rating compared to the conventional PSFB converter.

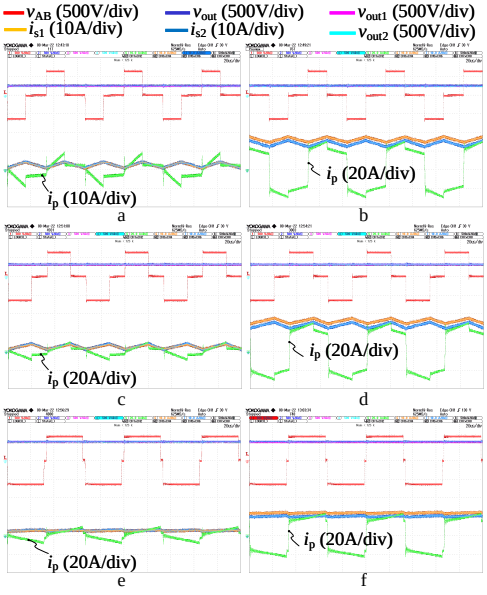


Figure 2.10: The operational waveform of the r-PSFB converter in parallel connection mode, with V_{in}=640V. $v_{out1/2}$ and $i_{s1/2}$ are the output voltage and current of the two secondary side rectifiers, measured after the RCD circuitry and on the output inductors, repectively. (a) V_{out}=250V, I_{out}=5A. (b) V_{out}=250V, I_{out}=30A. (c) V_{out}=320V, I_{out}=5A. (d) V_{out}=320V, I_{out}=30A. (e) V_{out}=500V, I_{out}=5A. (f) V_{out}=500V, I_{out}=22A.

Figure 2.12 demonstrates the voltage clamping effect of the RCD snubber circuitry with different V_{in} and connection modes. It can be seen that, with the maximum input

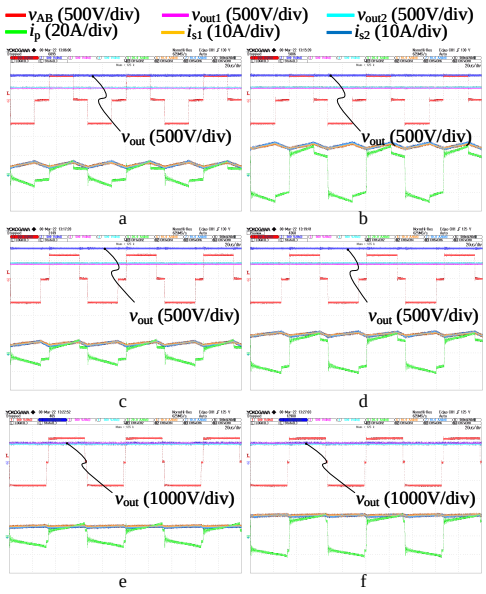


Figure 2.11: The operational waveform of the r-PSFB converter in series connection mode, with V_{in}=640V. (a) V_{out}=660V, I_{out}=5A. (b) V_{out}=660V, I_{out}=15A. (c) V_{out}=830V, I_{out}=5A. (d) V_{out}=830V, I_{out}=10A. (e) V_{out}=1000V, I_{out}=5A. (f) V_{out}=1000V, I_{out}=11A.

voltage of 840V, the diode voltages are clamped exactly at 1000V in both parallel and series connection modes. Therefore, the safe operation of the 1200V diodes is ensured.

Figure 2.13 shows the tested efficiency of the r-PSFB converter together with the estimated efficiency of the r-PSFB and the conventional PSFB converter. The estimated efficiency is obtained using the steady-state analytical model in Section III, and the loss calculation formulas introduced in [44, 46].

It can be seen from Figure 2.13 that the tested efficiency of the r-PSFB converter corresponds very well to the estimation. For the IGBT version, the peak efficiency, η_{peak}, of 97.6% is obtained in series connection mode when $V_{in} = 640V$, $V_{out} = 1000V$ and $I_{out} = 10A$, and an efficiency of 97.4% is tested in parallel connection mode when $V_{in} = 640V$, $V_{out} = 490V$ and $I_{out} = 20A$. For the SiC MOSFET version, η_{peak} of 98.3% is obtained in series connection mode when $V_{in} = 640V$, $V_{out} = 1000V$ and $I_{out} = 10A$, and 98.2% is tested in parallel connection mode when $V_{in} = 640V$, $V_{out} = 490V$ and $I_{out} = 20A$.

The benefits brought by the reconfiguration are clearly seen from Figure 2.13. First of all, the r-PSFB prototype has an efficiency jump when the configuration changes, keeping the efficiency high in a wider voltage range compared to the conventional PSFB. This occurs because the equivalent duty cycle increase leads to lower current stress on the semiconductors as shown in Figure 2.5. From $V_{out} = 1000V$, the efficiency of both r-PSFB and conventional PSFB converter start to drop as V_{out} decreases. This is due to the increasing phase shift that is required to step-down V_{out}. However, thanks to the reconfiguration from voltage to current doubler, the phase shift of the r-PSFB converter reset at $V_{out} = 500V$. Less current stresses are found on the primary side semiconductors during

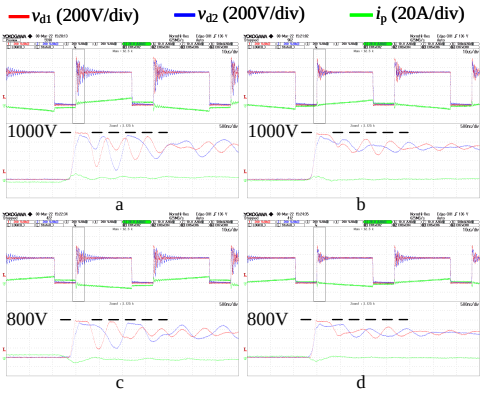
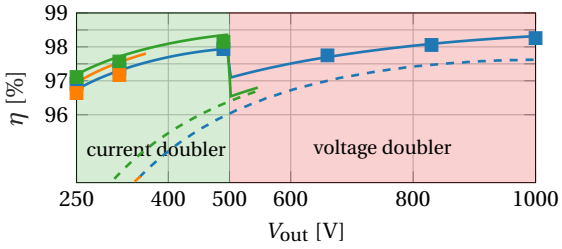
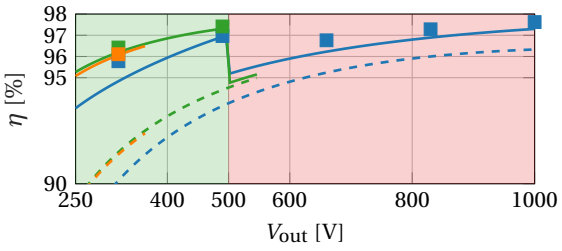
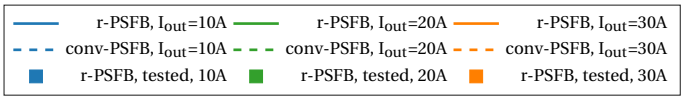


Figure 2.12: The voltage clamping of the RCD snubber circuitry. $v_{d1,2}$ is the diode voltage of the two secondary sides. (a) V_{in}=840V, series connection. (b) V_{in}=840V, parallel connection. (c) V_{in}=640V, series connection. (d) V_{in}=640V, parallel connection.



(a) SiC version





(b) IGBT version

Figure 2.13: The estimated and measured efficiency of the conventional PSFB and the r-PSFB converter (V_{in}=640V, f_{sw}=15kHz, L_σ=8.6μH, C_{snb}=470pF, f_{sw}=15kHz, R_g = 11Ω for IGBT version and 5Ω for SiC MOSFET version, T_j = 125°C)

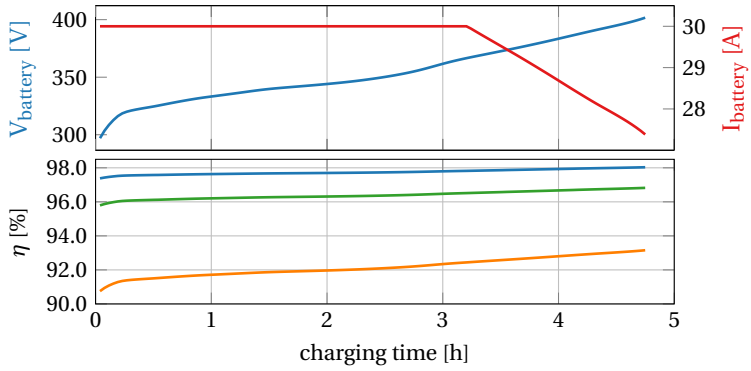
the current doubler operation (V_{out}=250-500V), which improves the efficiency performance when V_{out} is low.

For a better comparison between the conventional PSFB and the r-PSFB, the charg-

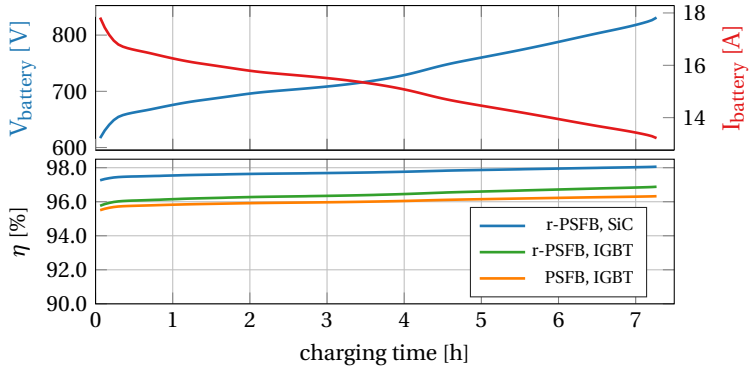
ing cycle efficiency η_{cycle} proposed in [46] of the two converters are estimated, which can be calculated by Equation (6.7). $\eta(t)$ is the instantaneous efficiency of the converter during charging, and T_c is the total charging time.

$$\eta_{\text{cycle}} = \int_0^{T_c} \frac{\eta(t) \cdot dt}{T_c} \tag{2.25}$$

Two EV batteries representing a 400V EV and an 800V EV are considered. One with 400V nominal voltage and 50.35kWh capacity, and the other with 800V nominal voltage and 79.2kWh capacity. The constant current constant voltage (CCCV) charging profiles of the 11kW PSFB and r-PSFB converters charging these two EV batteries are simulated using an impedance-based model of a lithium nickel oxide (LNCO) Boston Power SWING 5300 [47]. The charging profiles are shown in Figure 2.14. Then the charging cycle efficiency of charging the 400V battery, denoted as $\eta_{400\text{V},50.35\text{kWh},\text{CCCV}}$, the 800V battery, denoted as $\eta_{800\text{V},79.2\text{kWh},\text{CCCV}}$, is calculated based on the estimated efficiency. Table 2.9 shows the charging cycle efficiency.



(a) 400V, 50.36kWh



(b) 800V, 79.2KWh

Figure 2.14: Charging process of a 400V, 50.35KWh and an 800V, 79.2kWh battery using an 11kW converter, and the efficiency estimation

Table 2.9: The estimated charging cycle efficiency of the conventional PSFB and r-PSFB

η_{cycle}	conv-PSFB (IGBT)	r-PSFB (IGBT)	r-PSFB (SiC)
$\eta_{400V,50.36kWh,CCCV}$	92.2	96.4	97.8
$\eta_{800V,79.2kWh,CCCV}$	96.0	96.4	97.8

It can be seen that the r-PSFB converter provides the same η_{cycle} for both 400V and 800V+ EVs, while the conventional PSFB converter has a significantly poorer η_{cycle} for the charging of 400V EVs compared to the 800V EVs. This is mainly due to the large phase shift when V_{out} is low. On the other hand, as demonstrated, the r-PSFB converter is able to reset the phase shift by changing the series connection mode into the parallel connection mode when charging the 400V EVs, resulting in less current stress on the semiconductors, which have been observed from Figure 2.5. Therefore, the conduction, switching, and magnetic losses are also reduced. Moreover, the loss from the RCD snubber of the conventional PSFB converter is also higher because of the high voltage difference applied.

Moreover, comparing the IGBT and the SiC versions, even though the η_{peak} of the SiC version is around 0.7% (98.3% – 97.6%) higher than the IGBT version, the η_{cycle} is 1.4% (97.8% – 96.4%) higher. This indicates that η_{cycle} is the best metric for stating the performance of the converter. During the charging process, the converter operates outside of the η_{peak} point most of the time. As a result, the efficiency performance at the other operational points matters considerably. It can be seen from Figure 2.13 that the SiC version has higher efficiency than the IGBT version at the operational area other than the η_{peak} point, which contributes to the difference of η_{cycle}.

Additionally, the specifications of this r-PSFB prototype are benchmarked against the PSFB type prototypes reported in the IEEE literature in the last decades for EV charging application, shown in Table 2.10. It can be seen that, this 11-kW prototype covers an unprecedented wide output voltage range from 250V to 1000V that is able to charge both the 400V and 800V EVs. Considering the maximum output current and power rating of the prototypes, this work utilizes the most cost-effective semiconductor transistors. The η_{peak} of this prototype using cost-effective IGBTs is much higher than the IGBT prototype from [8], but lower than some Si MOSFET prototypes. And the SiC version of this prototype reaches the same highest η_{peak} of 98.3% reported in [11, 15]. This work also provides the charging cycle efficiency η_{cycle}, which is considered as a better evaluation criterion for the EV charging application.

2.6. CONCLUSION

A re-configurable PSFB converter with an extremely wide voltage range is analyzed, designed and tested. The converter extends the operational voltage range while keeping high efficiency in the whole operating range, thanks to the ability of reconfiguration. The operation and design of the converter are explained in detail. Finally, the comprehensive test results of the 11-kW prototype with 640-840V input voltage and 250-1000V

Table 2.10: Benchmark of the r-PSFB converter designed in this work with the PSFB type DC/DC converters used for EV charging application found in the literature. $I_{\text{transistor}}$ is the current rating of the transistors @ $T_c = 100°C$ used in the literature, PD is the volumetric power density.

reference	$V_{\text{out,min}}$ [V]	$V_{\text{out,max}}$ [V]	$I_{\text{out,max}}$ [A]	P [kW]	$\text{type}_{\text{transistor}}$	$I_{\text{transistor}}$ [A]	η_{peak} [%]	f_{sw} [kHz]	PD [kW/L]
[6]	200	450	11	3.3	Si MOSFET	29	96	200	/
[7]	250	420	/	3.6	hybrid	48	98.1	42	/
[8]	50	200	/	1	IGBT	60	94	50	/
[9, 10]	250	400	20	6	SiC MOSFET	30	96.5	200	12
[11]	250	450	4	2	Si MOSFET	46	98.3	50	/
[12]	300	400	/	1	/	/	95	/	/
[13]	209	350	3.75	1.2	Si MOSFET	35	95	100	/
[14]	270	420	7.85	3.3	Si MOSFET	31.6	97.9	100	/
[15]	270	420	7.85	3.3	Si MOSFET	31.6	98.3	50	/
this work	250	1000	30	11	IGBT	40	97.6	15	2.3
this work	250	1000	30	11	SiC MOSFET	45	98.3	15	2.3

output voltage are presented, including the calculation of charging cycle efficiency. The results show excellent correspondence between the estimation and test, which, therefore, demonstrates the feasibility of this converter in EV charging applications.

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3

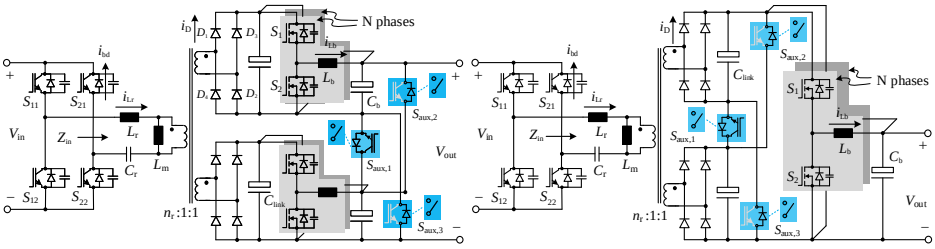
Reconfigurable Resonant Converter

This chapter introduces a novel two-stage DC/DC resonant topology designed to support electric vehicle (EV) charging across a broad output voltage spectrum ranging from 150 to 1000V, aiming for high efficiency throughout the full load spectrum. The introduced system comprises a dual-secondary-side LLC resonant converter, coupled with two interleaved buck converters operating in triangular current mode, and is enhanced by three auxiliary switches to enable reconfiguration. The work evaluates two distinct configurations of the proposed system, providing a comparative analysis. A thorough analytical model of the system is established to facilitate efficiency assessments across various configurations and aid in the development of a prototype converter. An 11kW prototype has been constructed and subjected to empirical testing, demonstrating a peak efficiency of 97.66% and maintaining efficiency levels above 95% across the entire voltage range under full load conditions. This two-stage converter sets a new benchmark in the literature for output voltage range capabilities of resonant power converters, ensuring efficient charging for current and forthcoming EV models across any charging cycle.[1]

[1] This chapter is based on:
B. O. Aarninkhof, D. Lyu, T. B. Soeiro and P. Bauer, "A Reconfigurable Two-stage 11kW DC-DC Resonant Converter for EV Charging with a 150-1000V Output Voltage Range," in IEEE Transactions on Transportation Electrification, doi: 10.1109/TTE.2023.3279211.

3.1. INTRODUCTION

The electrification of the world's transportation fleet has gained momentum in recent years. For example the widespread use of Electric Vehicles (EVs) today. This shift to EVs is all in light of a global effort to reduce Global Greenhouse Gas (GHG) emissions [1]. Consequently, the demand for public EV chargers to accommodate all these vehicles will increase correspondingly. According to the Sustainable Development Scenario (SDS) [2], 6% of the electricity consumption in the European Union in 2030 will come from EV charging, compared to 0.2% in 2019.



(a) Configuration I: S_{aux} after the interleaved BUCK stage (b) Configuration II: S_{aux} before the interleaved BUCK stage (selected)

Figure 3.1: The schematics of the proposed reconfigurable two-stage Resonant Power Converter (RPC) in two different arrangements. Note that $S_{aux,1/2/3}$ can be either mechanical switches or semiconductor transistors.

Most EVs currently produced use a battery pack with a nominal voltage of 400 V. However, in recent years, some models have been announced that use a higher voltage battery architecture [3]. This higher battery voltage which is typically close to 800 V can be one of the solutions enabling a faster charging time of EVs [25].

The introduction of these higher voltage battery architectures imposes a challenge on the EV chargers: the (common) 400 V battery architecture as well as the new high voltage battery architectures need to be accommodated. As a result, the typical DC/DC converters used in the EV chargers must operate in an extremely wide output voltage.

However, there are few studies in literature that have provided experimentally verified isolated DC/DC converter designs that are able to charge both the 400V and 800V EVs, though Lyu et al. (2022) proposed a reconfigurable Phase Shifted Full Bridge (PSFB) to achieve this wide output voltage range [15]. For Resonant Power Converters (RPC), no such large output voltage range has been achieved [6–11, 13, 14, 27–64]. Based on the studies about the resonant converters in the EV charging application in the past decade (2010-2021), Figure 3.2 shows the reported output voltage ranges of the RPCs. Most of the studies report an output voltage range between 250-450 V, corresponding with the typical battery voltage of a 400 V battery architecture. Seven studies reported an output voltage range of ΔV_o >320 V [5–11].

The challenge lies in the poor efficiency performance when these converters are made to operate in such a wide voltage range. The RPC is typically controlled by frequency modulation, and it is well-known for its high efficiency performance when it is operated at the resonant frequency point. However, operating the RPCs with frequency modulation in a wide output voltage range will result in a wide switching frequency

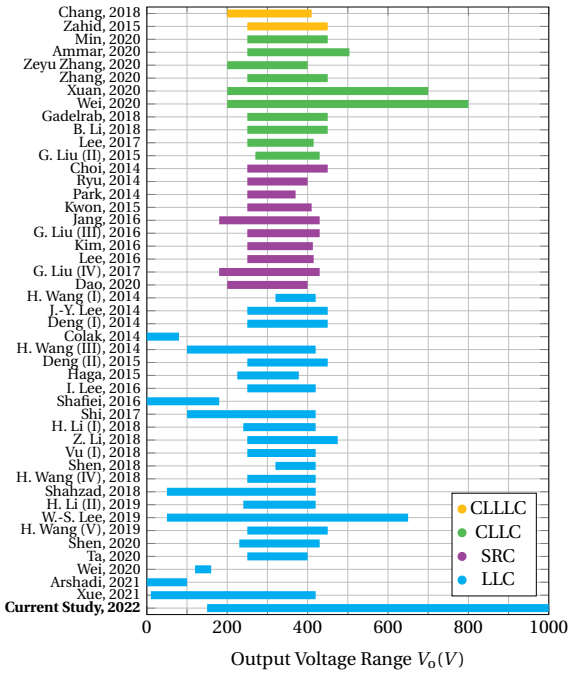


Figure 3.2: Overview of the output voltage range of all studies found regarding Resonant Power Converters and EV charging from 2014-2022 [6–11, 13, 14, 27–64].

range, which brings the issues of more complicated magnetic component design, a decrease in efficiency and reduced EMI performance [12]. As a result, the conventional RPC, such as an LLC converter, is not able to provide high efficiency in a wide voltage range application.

To extend the output voltage conversion range of the RPCs without compromising the system efficiency performance in the whole operational range, mainly five methods can be found in the literature. The first method uses a variable input DC link voltage while operating the RPC in the resonant frequency point [5, 6]. The output voltage regulation of the RPC using this method is entirely performed by the variable input voltage. The direct benefit of this method is that the RPC is operated at the maximum efficiency point with a simple fixed frequency modulation. However, this method requires a controlled front-end converter which provides the adjustable input DC link voltage for the RPC. As a result, the design and implementation complexity shift from the RPC converter to the front-end converter.

The second method is based on having two RPC converters operating in an interleaving way. Both switch at the resonant switching frequency, and they are phase-shifted to control the output voltage [9]. This method operates the RPCs with constant switching frequency, which is easy to implement and provides ZVS and high efficiency for the individual RPCs. However, due to the increase of circulating current-induced conduction loss, the interleaved RPC has a significant efficiency drop when the output voltage is low.

The third method uses a three-level bidirectional RPC together with Pulse Frequency Modulation (PFM), often abbreviated as; frequency modulation [8]. This RPC features two pairs of three-level full bridges, a resonant inductor and a capacitor. By combining the four operational modes of each of the three-level full bridges, this three-level bidirectional RPC adapts to a wide output voltage range with a small range of switching frequency change. However, the trade-off is the cost of the converter and control complexity, as it requires in total 16 transistors.

The fourth method is to use a flexible voltage gain control scheme for the full-bridge resonant converter, for example, proposed by Wei et al. (2020) [7]. A flexible voltage gain control could be a combination of reconfiguration between full-bridge and half-bridge of the switching bridge [66], a variable DC-link voltage provided by the grid-connected circuit and/or series compensation capacitance [67], Phase Shift Modulation (PSM) which results in a controllable duty cycle of the H-bridge inverter, and dual control where both frequency modulation and PSM are implemented together [26]. These approaches extend the voltage range by the increased control complexity without modification on the converter topology.

The fifth method uses a two-stage structure, where the RPC is the first stage, followed by a buck converter as the second stage [11]. This two-stage solution allowed for a decoupling of the functions of the proposed converter: the resonant stage provides galvanic isolation and a constant voltage step-up through the turns ratio of the transformer. Only the buck converter controls the output voltage since the LLC is operated only at the resonant frequency. Consequently, this approach achieves a wide voltage regulation range with a simple control scheme due to the control decoupling of the two stages. However, the drawback is higher cost, and the efficiency performance depends on this additional stage.

Table 3.1: Comparison of all wide output voltage range solutions involving an RPC.

	Variable input voltage SEPIC PFC + LLC [5]	Variable input voltage SEPIC PFC + LLC [6]	Two interleaved LLC converters [9]	Three level CLLC Converter [8]	Combination of Control Strategies CLLC converter [7]	Two-Stage: LLC + buck converter [11]
Modulation	Constant f_{sw}, Variable V_{in}	Constant f_{sw}, Variable V_{in}	PSM	PFM + Variable operational modes	PFM + Variable V_{in} + reconfig. HB or FB	LLC: Constant f_{sw} buck: Duty cycle
Output Voltage range	100-420 V	100-420 V	10-420 V	200-700 V	200-800 V	50-650 V
Switching frequency range	-	200 kHz	100 kHz	31-70 kHz	140-250 kHz	120 kHz & 50 kHz
Number of switches	5	5	4	16	8	5
Number of Diodes	9*	9*	4	4	0	9
Number of Transformers	1	1	2	1	1	2
Peak efficiency	97.4%	88.4%	98.10%	96.8%	98.5%	97.32%
Maximum Power	3.3 kW	3.3 kW	1 kW	3.5 kW	22 kW	20 kW
Control Complexity	Moderate	Moderate	Moderate	Complex	Complex	Simple
Power Density	-	-	-	-	8 kW/L	-

A comparison of all studies regarding wide output voltage range RPCs is given in Table 3.1. It can be seen that, in the case of designing an RPC for wide voltage regulation when bidirectional operation is not a necessity, the two-stage approach is the conventional way to be implemented. The RPC stage can operate at a constant frequency near the series resonant frequency, allowing for optimal design of the magnetic components and minimal losses. Besides this, ZVS of the primary switches is guaranteed for the entire operating range. However, the efficiency performance of the two-stage solution still has room for improvement. When a simple continuous conduction mode (CCM) buck converter is used for the voltage regulation stage, the efficiency is limited by mainly two factors, namely the turn-on switching loss and the low duty cycle when the output voltage is low. As a result, the two-stage RPC converter will suffer from considerable efficiency drop during; moments of heavy load where the turn-on switching loss is high, and moments when the output voltage, and thus the equivalent duty cycle, is low.

Commercial solutions for wide output voltage EV charging are available, such as the ABB Terra 53/54 50kW, ENERCON E-charger 600 [69], ABB Terra 184 CC HVC and Porsche Charge Box [70]. The proposed topology has not been used in the commercially available EV chargers of which the topology is known [69] [70]. On top of that, none of these EV chargers use an isolated topology which would be likely to achieve high efficiencies over the entire output voltage and power range, which makes the proposed two-stage converter unique.

This chapter proposes a new two-stage reconfigurable LLC resonant converter cascaded with interleaved Triangular Current Mode (TCM) buck converter to address the shortcomings. Figure 3.1 shows the two possible configurations of the proposed converter. This converter is capable of a wide output voltage range operation (150-1000 V) that enables the charging of both the 400V and 800V EVs. The LLC full-bridge converter stage is operated at the resonant frequency to benefit from the high efficiency and easy design. By having the interleaved TCM buck converter for the second stage, the turn-on switching loss can be eliminated and the efficiency can be improved due to ZVS [18]. The interleaving also reduces the current stresses (and thereby conduction losses) for the individual TCM buck converter [19], and it allows the large output current ripple of a single TCM buck converter to be partially attenuated, reducing the required DC-link

output capacitance. Moreover, the reconfigurable structure allows the secondary sides to be connected in parallel or in series, depending on the output voltage conditions [15]. With this structure, the interleaved buck converter can be operated with high duty cycle even when the output voltage is low, which results in higher efficiency performance.

The contribution of this chapter is as follows:

1. A two-stage LLC converter cascaded with interleaved TCM buck converter with a reconfigurable structure is proposed in this chapter, allowing for a wide output voltage range while maintaining a high efficiency over the entire load range.

2. The complete design guidelines including the steady-stage analytical model of the converter is presented. The two possible arrangements and the choice of transistor technologies of the proposed converter are comprehensively evaluated.

3. The proposed converter is experimentally verified, and the performance benchmark of the proposed converter and the conventional frequency modulated LLC converter for the wide output voltage range (150-1000V) EV charging application is presented. This design benchmark is particularly important because it identifies the proposed converter as an outstanding solution for the future EV market without compromising efficiency.

3.2. OPERATING PRINCIPLE OF THE TWO-STAGE CONVERTER

The key enablers of the wide output voltage range two-stage converter proposed in this study is the Voltage-Doubler/Current-Doubler (VD/CD) reconfigurable structure. This structure allows to either connect the two TCM buck outputs in series (to achieve between 500-1000 V) to charge the 600 V or 800 V batteries, or in parallel (to achieve 150-500 V) to charge the 400 V or lower voltage batteries. And this flexibility in connection is beneficial because the efficiency of the buck converter decreases with decreasing duty cycle D, and the range of the duty cycle during the charging process can be reduced by half by using the VD/CD reconfigurable structure. Consequently, this structure allows the maximum efficiency to be achieved twice in the whole output voltage range. This is especially advantageous since both the 400 V as well as the 800 V battery architectures can be charged with similar high efficiency.

The operating principle of the reconfigurable structure is as follows: during the communication period in an EV charging session, the EV will inform the charger about the required charging voltage and current value [65]. By comparing the voltage value to a preset boundary voltage value V_{re}, the proposed two-stage LLC converter can be configured into a parallel connection configuration if the required charging voltage value is lower than 500 V or as a series connection if the value is higher than 500 V, by setting the states of the auxiliary switches $S_{\text{aux},1,2,3}$. This connection configuration is done before the start of the charging session, and thus the commutation occurs at zero current.

If there are EVs with voltage range across 500V, the sudden change of capacitor voltage due to the dynamic reconfiguration can be avoided by implementing a simple shutdown, reconfiguration, and restart mechanism in the controller of the charger. During the energy transferring process, the communication between the vehicle and the charger is still on, and the vehicle continues to send a setting value of charging current or voltage

to the DC EV charging station throughout the charging process [65]. Once the charging voltage reaches 500V, which is the reconfiguration value of the converter, the charger executes a shutdown process. Once the shutdown process is finished, the charging current is zero, and the contactors of the DC power lines are open, the converter can be configurated from the parallel connection into the series connection. Then the energy transferring process is resumed. Another approach is that the conventional frequency modulation can be implemented in the LLC converter stage. By adjusting the switching frequency the converter can cover the exceeding battery voltage range.

The two settings of the auxiliary switches are described below:

SERIES CONNECTION

When $S_{aux,1}$ is kept on while $S_{aux,2,3}$ are maintained off, the negative rail of the upper converter transformer's secondary-side rectifier is connected with the positive rail of the lower side converter rectifier, making the two secondary side circuits connected in series. This configuration enables the converter to supply high output voltage with the utilization of diodes and capacitors with halved voltage rating compared to those of the conventional approach.

PARALLEL CONNECTION

When $S_{aux,1}$ is kept off while $S_{aux,2,3}$ are maintained on, both the transformer's secondary side rectifiers of the converters are connected in parallel. This configuration enables the converter to operate in the low output voltage range <500 V.

Two locations exist where the VD/CD structure can be implemented: After the Interleaved TCM buck converter (Configuration I), or after the LLC converter (Configuration II). See Figures 3.1a and 3.1b, respectively, for a schematic of both Configurations.

The VD/CD structure can be either implemented with solid-state switches or mechanical relays. A benchmarking between both circuits shown in Figures 3.1a and 3.1b will be presented in Section 3.6. First, the analytical models of the LLC converter and TCM buck converter are presented in Section 3.3 and Section 3.4, respectively.

3.3. STEADY STATE ANALYTICAL MODELLING OF THE LLC CONVERTER

The LLC converter operates at a fixed switching frequency slightly above the series resonant frequency $f_{sr} = 1/\sqrt{(L_r C_r)}$. A simplified analysis technique to represent the LLC converter operating close to f_{sr} is the Fundamental Harmonic Approximation (FHA) [20]. This approximation enables classic AC analysis to be used by reducing the entire secondary side of the LLC converter to an equivalent AC resistance R_{AC}.

All equations regarding the LLC converter are listed in Table 3.2. R_L is the load resistance after the rectifier. The input impedance Z_{in} can be seen as the impedance seen from the primary side full bridge towards the secondary side. For an explanation of M_v, Z_o and Q_L the reader is referred to [20]. The rest of the parameters given in Table 3.2 can be found in Figure 3.1.

Figure 3.3 shows the typical operational waveforms of the LLC converter in resonant frequency.

Table 3.2: All analytical equations regarding the LLC converter.

Description	Parameter	Equation	
Equivalent AC Resistance	R_{AC}	$\frac{8n^2 R_L}{\pi^2}$	(3.1)
Equivalent load resistance	R_{L}	$\frac{(2 \cdot V_{\text{link}})^2}{P_{\text{o}}}$	(3.2)
Voltage gain	M_{v}	$\frac{1}{\sqrt{\left(1+l-l\cdot\left(\frac{\omega_0}{\omega}\right)^2\right)^2+Q_L^2\cdot\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)^2}}$	(3.3)
Inductance Ratio	l	$\frac{L_{\text{r}}}{L_{\text{m}}}$	(3.4)
Characteristic Impedance	Z_{o}	$\sqrt{\frac{L_r}{C_r}}$	(3.5)
Quality Factor	Q_{L}	$\frac{Z_0}{R_{\text{AC}}}$	(3.6)
Amplitude of Input Impedance	$\lvert Z_{\text{in}}\rvert$	$\sqrt{\frac{64L_m^2R_L^2n^4}{64R_L^2n^4L_rC_r+L_m\pi^2}}$	(3.7)
Angle of Input Impedance	$\angle Z_{\text{in}}$	$\arctan\left(\frac{8\sqrt{L_rC_r}n^2}{L_m\pi^2}\frac{V_o^2}{P_o}\right)$	(3.8)
Series Inductor RMS current	$I_{\text{Lr,RMS}}$	$\frac{4}{\pi}\frac{1}{\sqrt{2}}\frac{V_{\text{in}}}{\lvert Z_{\text{in}}\rvert}$	(3.9)
Magnetizing RMS current	$I_{\text{Lm,RMS}}$	$\frac{4V_{\text{in}}}{\pi\sqrt{2}}\frac{M_{\text{v}}}{\omega L_m}$	(3.10)
Maximum resonant Capacitor voltage	$V_{\text{Cr,max}}$	$\frac{1}{\omega C_r}\sqrt{2}I_{\text{Lr,RMS}}$	(3.11)
Switch turn-on current	$I_{\text{Sx,on}}$	$-\sqrt{2}I_{\text{Lr,RMS}}\sin(\angle Z_{\text{in}})$	(3.12)
Switch turn-off current	$I_{\text{Sx,off}}$	$\sqrt{2}I_{\text{Lr,RMS}}\sin(\angle Z_{\text{in}})$	(3.13)
RMS switch current	$I_{\text{Sx,RMS}}$	$\frac{\sqrt{2}I_{\text{Lr,RMS}}}{2\sqrt{\pi}}\sqrt{\cos(\angle Z_{\text{in}})\sin(\angle Z_{\text{in}})+(\pi-\angle Z_{\text{in}})}$	(3.14)
Average switch current	$I_{\text{Sx,avg}}$	$\sqrt{2}I_{\text{Lr,RMS}}\frac{\cos(\angle Z_{\text{in}})+1}{2\pi}$	(3.15)
RMS switch bodydiode current	$I_{\text{bd,RMS}}$	$\frac{\sqrt{2}I_{\text{Lr,RMS}}}{2\sqrt{\pi}}\sqrt{-\cos(\angle Z_{\text{in}})\sin(\angle Z_{\text{in}})+\angle Z_{\text{in}}}$	(3.16)
Average switch bodydiode current	$I_{\text{bd,avg}}$	$\sqrt{2}I_{\text{Lr,RMS}}\frac{\cos(\angle Z_{\text{in}})-1}{2\pi}$	(3.17)
Average 'rectifier Diode' current	$I_{\text{D,avg}}$	$\frac{1}{2}\frac{P_{\text{o}}}{V_{\text{link}}}$	(3.18)
RMS 'rectifier Diode' current	$I_{\text{D,RMS}}$	$\frac{\pi}{2}I_{\text{D,avg}}$	(3.19)
RMS DC-link capacitor current	$I_{\text{Clink,RMS}}$	$\frac{1}{2}\frac{P_{\text{o}}}{V_{\text{o}}}\sqrt{\frac{\pi^2}{8}-1}$	(3.20)

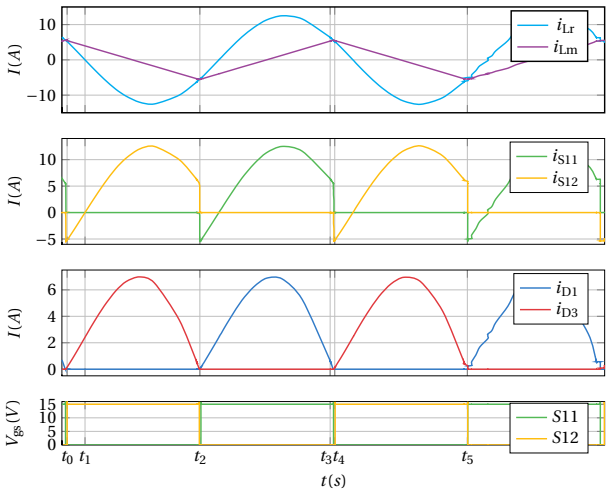


Figure 3.3: Operational waveforms of the LLC converter, which is the first stage in the proposed two-stage converter. The series resonant current i_{Lr} and magnetizing current i_{Lm} are given in the top graph, i_{S1} and i_{S2} are the drain-to-source currents of S11 and S12, respectively, and currents through diode $D1$ and $D3$ are given in the third graph. The final graph shows the gate-to-source voltage V_{gs} of S11 and S12. See Figures 3.1a and 3.1b for reference.

3.3.1. SOFT SWITCHING

The LLC converter can achieve ZVS turn-on of the primary side switches. Due to the operation of the converter just above f_{sr}, where the input impedance of the Resonant Tank Network (RTN) is inductive, ZVS is achieved in all primary side switches for the entire load range of the LLC converter.

The maximum magnetizing inductance L_m that allows the output capacitances to be completely charged/discharged within a given deadtime is given by (3.21) [21].

$$L_{m,max} = \frac{t_{dead}}{16 \cdot C_{equi} f_{sw}} \tag{3.21}$$

Where C_{equi} is the equivalent representation of all output capacitances C_{oss}. Which is calculated based on the method proposed by Kasper et al. (2016) [22].

$$C_{equi} = 4 \cdot C_{oss} \tag{3.22}$$

3.4. STEADY STATE ANALYTICAL MODELLING OF THE INTERLEAVED TCM BUCK CONVERTER

The TCM buck is a synchronous buck converter, as shown in Figure 3.5. All equations of the analytical model of the TCM buck converter used in this chapter are given in Table 3.3.

Figure 3.4 shows the typical operational waveforms of a TCM buck converter. In the top graph of Figure 3.4 it can be observed that the current through the inductor I_{Lb} can

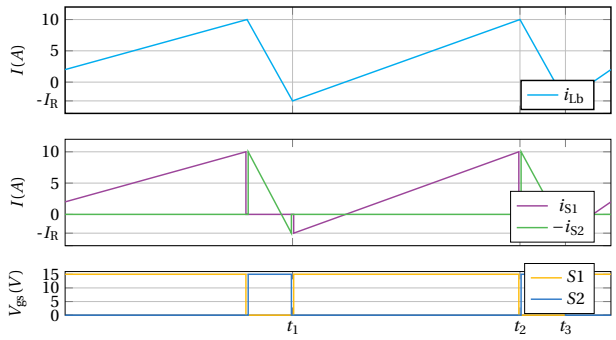


Figure 3.4: Operational waveforms of a TCM buck converter, building block of the second stage in the proposed two-stage converter. i_{Lb} is the current through the inductor of the buck converter, i_{S1} and i_{S2} are the currents through the top and bottom switch of the half bridge, respectively. See Figure 3.5.

reverse its direction (become negative). The current continues to turn negative until $I_{Lb} = -I_R$ is reached. At this point, S2 turns off, and the converter enters a period in which a resonant transition occurs (see Section 3.4.1). After this, I_{Lb} will flow through the body diode of S1 (see Figure 3.5), allowing for ZVS turn-on at t_1. The TCM buck converter also achieves ZVS turn-on of S2, in the same way as the regular buck converter.

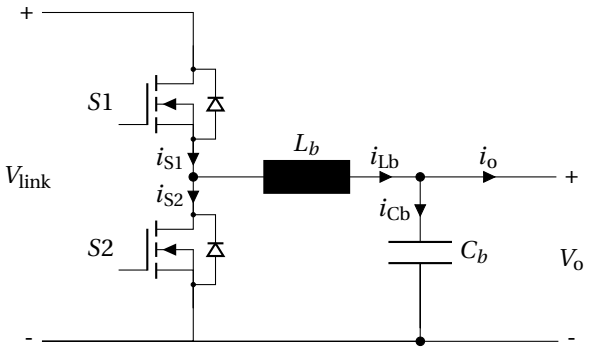


Figure 3.5: Schematic of a single TCM buck converter.

3.4.1. DEADTIME ANALYSIS

The process of charging and discharging the output capacitances C_{oss} occurs by means of resonance in the synchronous buck converter. The equivalent circuit during deadtime is shown in Figure 3.6.

ZVS turn-on of S1 does not occur in a certain range of I_R, and whether it is achieved can be determined numerically solving the equations for a series resonant circuit, given in **??**. By solving these equations it can be seen in Figure 3.7 that C_{eq} is not always fully charged/discharged for every combination of t_{dead} and I_R.

Table 3.3: All equations where the analytical model of the TCM buck converter is based on.

Description	**Definition**	
Dutycycle	$\mathrm{D} = \mathrm{V_o} / V_{\mathrm{in}}$	(3.23)
Switching frequency	$\mathrm{f_{sw}} = \frac{1}{L_\mathrm{b}} \cdot D \cdot \frac{V_{\mathrm{in}} - V_{\mathrm{out}}}{2(I_\mathrm{o} + I_\mathrm{R})}$	(3.24)
Average Inductor Current	$\mathrm{I_{Lb,avg}} = I_\mathrm{o}$	(3.25)
Peak-to-Peak Inductor Current	$\mathrm{I_{Lb,pk-pk}} = 2(I_\mathrm{o} + \lvert I_\mathrm{R} \rvert)$	(3.26)
Maximum Inductor Current	$\mathrm{I_{Lb,max}} = 2(I_\mathrm{o} + \frac{1}{2}\lvert I_\mathrm{R} \rvert)$	(3.27)
RMS Inductor Current	$\mathrm{I_{Lb,rms}} = \sqrt{\frac{1}{3} I^2_{\mathrm{Lb,pk-pk}} - I_\mathrm{R} I_{\mathrm{Lb,pk-pk}} + I^2_\mathrm{R}}$	(3.28)
	$\mathrm{k_1} = \lvert I_\mathrm{R} \rvert / I_{\mathrm{Lb,pk-pk}}$	(3.29)
Average high-side switch current	$\mathrm{I_{S1,avg}} = D I_\mathrm{o}$	(3.30)
RMS high-side switch current	$\mathrm{I_{S1,RMS}} = \sqrt{\left(I_\mathrm{R}\sqrt{D\frac{k_1}{3}}\right)^2 + \left(I_{\mathrm{Lb,max}}\sqrt{D\frac{1-k_1}{3}}\right)^2}$	(3.31)
Average low-side switch current	$\mathrm{I_{S2,avg}} = (1-D) I_\mathrm{o}$	(3.32)
RMS low-side switch current	$\mathrm{I_{S2,RMS}} = \sqrt{\left(I_\mathrm{R}\sqrt{(1-D)\frac{k_1}{3}}\right)^2 + \left(I_{\mathrm{Lb,max}}\sqrt{(1-D)\frac{1-k_1}{3}}\right)^2}$	(3.33)
Turn-off current high-side switch	$\mathrm{I_{S1,off}} = I_{\mathrm{Lb,max}}$	(3.34)
Turn-off current low-side switch	$\mathrm{I_{S2,off}} = I_\mathrm{R}$	(3.35)
Interleaved output current ripple	$\Delta I_\mathrm{o} = \frac{V_{\mathrm{in}} D}{f_{\mathrm{sw}}} \left(1 - \frac{\lfloor N_{\mathrm{phase}} D \rfloor}{N_{\mathrm{phase}} D}\right) \left(1 + \lfloor N_{\mathrm{phase}} D \rfloor - N_{\mathrm{phase}} D\right)$	(3.36)
Output capacitor RMS current	$\mathrm{I_{Cb,rms}} = \sqrt{\frac{\Delta I_\mathrm{o}^2}{12}}$	(3.37)

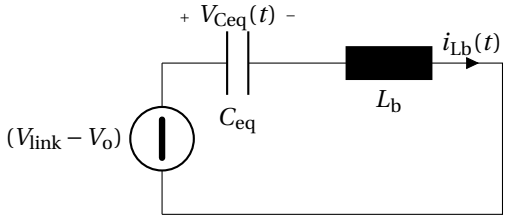


Figure 3.6: Equivalent circuit of the TCM buck converter during deadtime. This is a series resonant circuit.

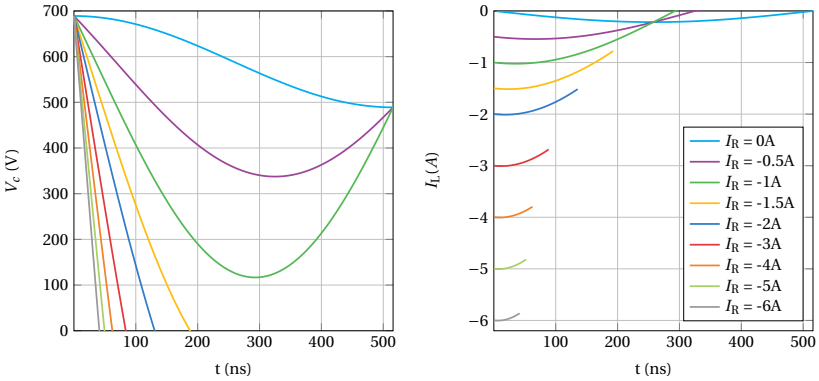


Figure 3.7: Voltage across the equivalent capacitance C_{eq} of Figure 3.6 and the current through the inductor L_b at that same time in the resonant interval during t_{dead}. ZVS is only achieved when $V_c = 0$ V. This figure shows that not all values of I_R will lead to ZVS. V_{in}=689 V, V_o=100 V, C =355 pF, L =75.8 µH.

3.5. CONVERTER DESIGN

3.5.1. DESIGN REQUIREMENTS

The design requirements are listed in Table 3.4, where the targets for $\Delta I_{o,max}$, $\Delta V_{o,max}$ and $T_{ambient}$ are taken from DC charging station standard IEC-61851-23:2014 [23].

3.5.2. SEMICONDUCTOR SELECTION

LLC CONVERTER

Applying the analytical equations from Table 3.2, the maximum average current stress of the switch for the LLC converter can be approximated to be $\hat{I}_{sw,avg} = 8.59A$. And assuming that each switch conducts exactly half of the positive sine wave, the maximum rms current stress on the switches can be calculated to be $\hat{I}_{sw,rms} = 13.5A$.

A range of different 1200 V commercial MOSFET and IGBT devices that suit these requirements are compared. The switches that would result in the lowest losses for the LLC converter are selected:

- LLC IGBT version: IKW40N120CS6 from Infineon.
- LLC MOSFET version: IMW120R060M1 from Infineon.

Table 3.4: Design requirements for the wide output voltage range resonant converter.

Parameter	Symbol	Value
Input voltage range	V_{in}	640-840 V
Output voltage range	V_{out}	150-1000 V
Switching frequency LLC	$f_{sw,LLC}$	15 kHz
Maximum output power	$P_{o,max}$	11 kW
Maximum output current	$I_{o,max}$	30 A
Maximum output current ripple during CC*	$\Delta I_{o,max}$	9 A
Maximum output voltage ripple during CV*	$\Delta V_{o,max}$	10 V
Operating temperature range	$T_{ambient}$	−5-40 °C

INTERLEAVED TCM BUCK CONVERTER

The maximum output current is $I_{o,max} = 30$ A. Since $N_{phase} \geq 2$, the average output current of a single buck converter is, therefore, maximum 15 A. Taking the conservative values of $I_R = -5$A and $D = 1$, the maximum current stress of the interleaved TCM buck converter switch can be calculated using (3.26), (3.29) and (3.31) to be $I_{S1,rms} = 18.93A$.

The requirements for the switches in the Interleaved TCM buck converter in Configuration One are equal to the requirements for the switches of the LLC converter. Therefore the same two switches are selected: as IGBT the IKW40N120CS6 and as MOSFET the IMW120R060M1.

3.5.3. RESONANT CAPACITORS

The resonant capacitors in the LLC converter are subject to the total transformer current. The maximum voltage amplitude across the capacitor is calculated using (3.11). The maximum $I_{Lr,rms}$ follows from the design script and is equal to 20 Arms. The capacitor bank is arranged with N_p parallel capacitors to lower the RMS current on an individual capacitor. The selected resonant capacitor is the B32671L6473K000: (47 nF). These capacitors have a DC voltage rating of 630 V, with no derating required at f_{sw}=15 kHz. The required voltage rating, using (3.11), is only ≈200 V (peak). The number of parallel capacitors to achieve the required C_r is 33.

3.5.4. TRANSFORMER DESIGN

The operating frequency of the LLC converter is relatively low ($f_{sw,LLC}$= 15 kHz), as stated in Table 3.4. This low frequency and high power naturally results in the requirement of large area-product cores. The minimal number of turns of the primary side winding can be calculated by (3.38).

$$N_{min} = \frac{V_{in}}{4 \cdot A_c \cdot B_{op} \cdot f_{sw}} \tag{3.38}$$

An airgap might be required to lower the magnetizing inductance value L_m, required

to satisfy ZVS requirements of the LLC converter. The relationship between the airgap length and the magnetizing inductance can be approximated by (3.39).

$$L \approx \frac{N^2}{R_g} \approx \frac{N^2}{2 \cdot l_{air}/\mu_0 A_c} \tag{3.39}$$

The winding losses are calculated in MATLAB based on the procedure described by Mühlethaler et al. (2012) [24], and the core losses are calculated using the improved Generalized Steinmetz Equation (iGSE) [24] [68]. The details are not further elaborated upon in this work.

3.5.5. INDUCTOR DESIGN

The work in [15] is used for designing the four inductors of the Interleaved TCM buck converter and the external resonant inductor $L_{r,ext}$ of the LLC converter. The minimum number of turns can be calculated using (3.40), and the required airgap length l_g to achieve the required inductance can be calculated by (3.41).

$$N_{min} = \frac{L I_{max}}{B_{max} A_c} \tag{3.40}$$

$$l_g = \frac{L I_{max}^2 \mu_0}{B_{max}^2 A_c} \tag{3.41}$$

The winding losses and core loss are, again, calculated in MATLAB based on the procedure described in [24] [68].

3.5.6. DESIGN SUMMARY

The selection choices of all other components of the proposed converter are summarized in Tables 3.5 and 3.6. The output capacitors of the Interleaved TCM buck converter are selected to meet the requirements from IEC-61851-23:2014 [23] (see Table 3.4).

3.6. RESULTS OF THE ANALYTICAL COMPARISON

In order to compare the efficiency performance of the two possible configurations presented in Figure 3.1, the charging-cycle efficiency [15] is used, which represents the average efficiency of the converter over the whole charging process.

As explained in Section 3.2, two possible configurations of the two-stage converter were compared together with the use of either SiC MOSFETs or IGBTs. The results for the first stage, the LLC converter, are given in Section 3.6.1, while the results of the Interleaved TCM buck converter configuration comparison are given in Section 3.6.2.

3.6.1. LLC CONVERTER

For the LLC converter in this chapter only a comparison was made between a SiC MOSFET based or IGBT based LLC converter. The performance of the converter was measured based on the charging cycle efficiencies, as explained in [15]. Table 3.7 indicates that the efficiency of both the SiC MOSFET based and IGBT based LLC converter have approximately the same charging cycle efficiencies, given f_{sw} = 15 kHz. Therefore, the IKW40N120CS6 IGBT version of the LLC converter is selected due to its lower cost.

Table 3.5: All components in the final design of the LLC converter.

Component	Description/Part Number
LLC IGBT's	IKW40N120CS6
Resonant capacitors	B32671L6473K000 (47 nF)
Transformer core shape	EE70/33/32
Number of parallel cores n_{cores}	5
Transformer Airgap	0.3 mm
N_{pri}	20
N_{sec}	30 (2 · 15)
Magnetizing Inductance L_{m}	4.8 mH
External Resonant Inductor Core Shape	EE70/33/32
Number of parallel cores n_{cores}	1
Inductor airgap	1.3 mm
N	14
Resonant Inductance L_{r}	64.43 uH
Rectifier Diodes	IDW30G120C5B
LLC output capacitors	C4AQIBW5600A3NJ (2 · 2·60 uF)

Table 3.6: All components in the final design of the Interleaved TCM buck converter.

Component	Description/Part Number
SiC MOFSET's	IMW120R060M1 (2 · 2 · 2)
Parallel phases per module N_{phase}	2
Inductor core shape	EE70/33/32
Number of parallel cores n_{cores}	1
Inductor airgap	1.6 mm
N	12
buck Inductance L_{b}	75.6 uH
LLC output capacitors	C4AQILW5150A36J (2 · 2·15 uF
Power Relays	TE-T9G (3x)

Table 3.7: Efficiency and Losses of the 11 kW LLC converter using either a MOSFET (IMW120R060M1) or an IGBT (IKW40N120CS6) as transistor (V_{in} =840 V).

Switch Type	**Charge Cycle Efficiencies ($\eta(-)$)**				
	11 kW 400 V	55 kW 400 V	11 kW 800 V	55 kW 800 V	**Average**
IMW120R060M1	0.9799	0.9787	0.9798	0.9795	**0.9795**
IKW40N120CS6	0.9796	0.9763	0.9795	0.9786	**0.9784**

3.6.2. INTERLEAVED TCM BUCK CONVERTER

The comparison of different design solutions for the Interleaved TCM buck converter is more elaborate because a given design solution consists of 5 different variables:

- Configuration 1 or 2
- Minimum switching frequency (see (3.24))
- IGBT or SiC MOSFET based
- Number of interleaved phases per module N_{phase}

Running the analytical comparison of several possible design solutions and comparing the average efficiency of all four charging cycles proposed in [15] gives us the solution space given in Figure 3.8. Note that no competitive IGBT could be found for use in Configuration 2 (which requires higher $V_{DS,max}$ than Configuration 1) due to the unsatisfactory switching losses performance from the devices available on the market.

It can be seen that the MOSFET-based solutions are more efficient when compared to IGBT-based solutions. And, specifically, Configuration 1 using MOSFETs generates the most efficient converters for each respective $f_{sw,min}$. The selected solution for the TCM buck converter in this chapter is shown in Table 3.8.

Table 3.8: Selected final design of the TCM buck converter in this chapter.

Design Parameter	**Value**
Configuration	1
$f_{sw,min}$	15 kHz
Switch technology	MOSFET
Switches	IMW120R060M1
N_{phase}	2

The reason that IGBT-based converters achieve a lower average efficiency in the TCM buck converter is because of the high switching frequencies operation required for partial loads (see (3.24)).

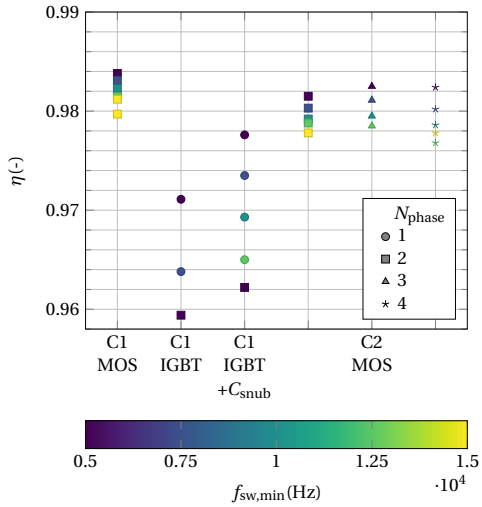


Figure 3.8: Average charging cycle efficiency of the Interleaved TCM buck converter solution space. C1 = Configuration 1, and C2 = Configuration 2.

The calculated efficiency of the selected design solution of the Interleaved TCM buck converter over the entire operating range of the system is shown next to the measured efficiency in Figure 3.9.

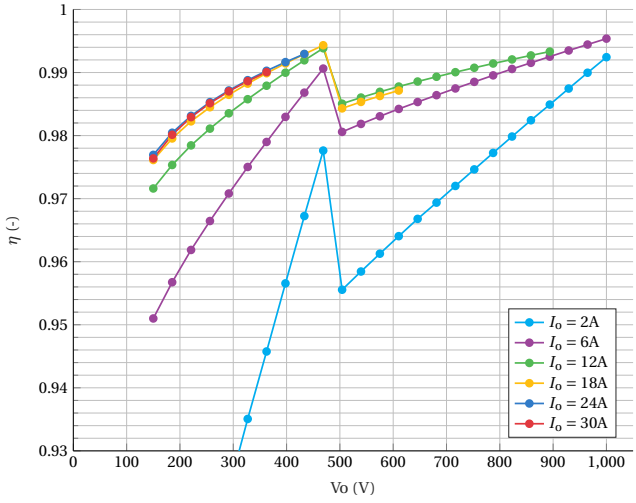


Figure 3.9: Analytical efficiency of the TCM buck converter for different I_o over the entire V_o range (with V_{in} = 525 V)

3.7. COMPARISON TO CONVENTIONAL FREQUENCY-MODULATED LLC

In order to emphasize the benefit of the proposed two-stage wide output voltage range EV charger solution, a comparison is made with the conventional frequency-modulated LLC converter. To do this, the buck stage is removed from the two-stage converter shown in Figure 3.1b, however, the re-configurable secondary sides of the LLC are kept to improve efficiency and reduce switching frequency operational range. The proposed LLC design from Table 3.5 is then employed using solely pulse frequency modulation to control the output voltage (rLLC PFM). The analytical efficiency comparison over the entire operational range is shown in Figure 3.10.

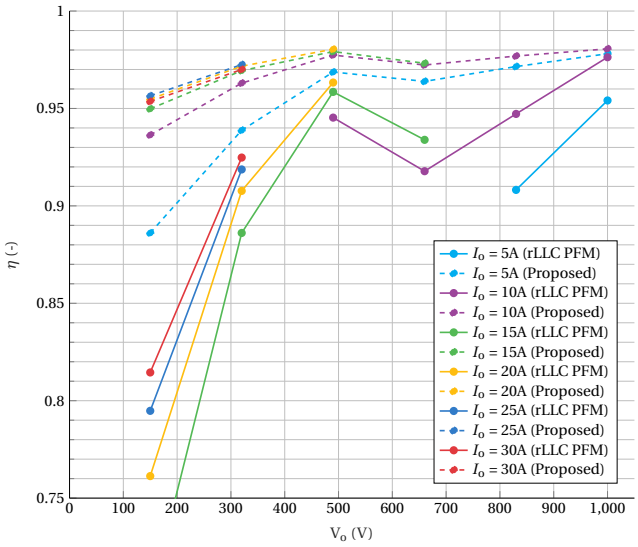


Figure 3.10: Analytical efficiency comparison between the proposed solution and the conventional frequency modulated LLC converter (rLLC PFM). The output voltage is on the x-axis, and the colors indicate different I_o.

Judging from Figure 3.10, the benefit of the proposed wide output voltage EV charger appears evidently: the proposed solution is highly efficient over the entire operational range, which is not the case for the rLLC PFM. The switching frequency operational range of the rLLC PFM is 4.8-87.3kHz. Operational points which showed large deviations between the analytical model and LTSpice simulations are not displayed for the rLLC PFM. These were operational points for which the FHA model was not valid. The rLLC PFM deviates from the series resonant frequency operational point, which creates reactive currents in the RTN that cause additional losses. On top of that, the IGBT's need to switch at multiples of the base 15 kHz for some operational points, causing additional switching losses.

This almost flat high-efficiency curve of the proposed solution is enabled due to the unique combination of the LLC converter, Interleaved TCM Buck converter and re-configurable stage, resulting in the highest reported output voltage range for a resonant converter

based EV charger while maintaining this almost flat high-efficiency curve.

3.8. EXPERIMENTAL RESULTS

The selected design solutions for the LLC converter and Interleaved TCM buck converter are verified experimentally. Figures 3.11 and 3.12 present the hardware demonstrators of the LLC converter and Interleaved TCM buck converter, respectively.

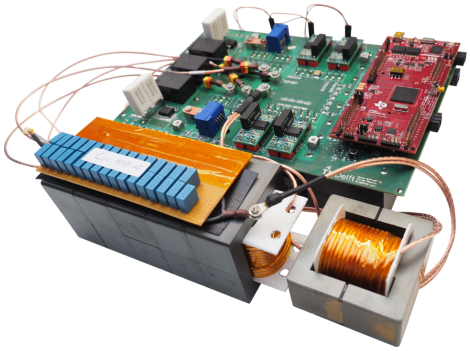


Figure 3.11: Designed LLC converter hardware demonstrator.

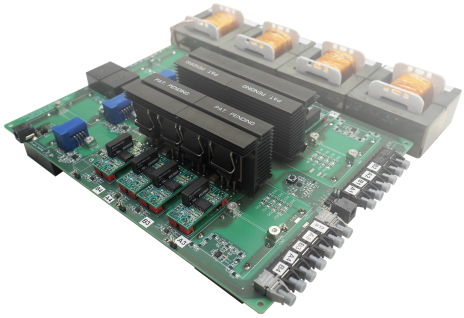


Figure 3.12: Designed interleaved TCM buck converter hardware demonstrator.

3.8.1. LLC CONVERTER

The experimentally measured efficiency of the LLC converter over the load range from 400 W to 11 kW with an input voltage of 640 V is shown in Figure 3.13. The peak efficiency of the LLC converter is 98.231% at P_o = 6.37 kW; see Figure 3.14.

The measured operational waveforms at different output powers of the LLC converter are shown in Figure 3.15.

3.8.2. INTERLEAVED TCM BUCK CONVERTER

The efficiency of the selected interleaved TCM buck converter solution presented in Table 3.8 is measured. The results are given in Figure 3.16, where they are compared with

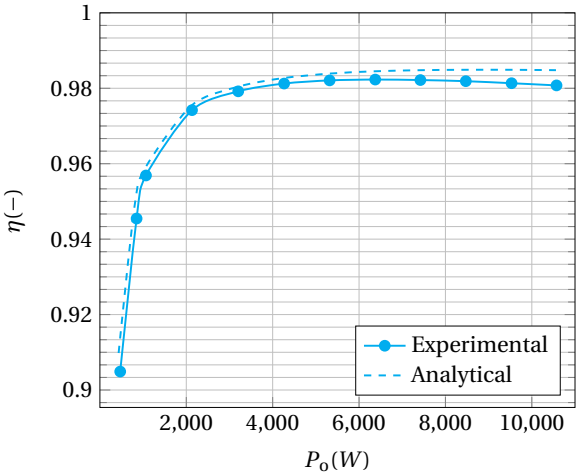


Figure 3.13: LLC converter efficiency over the entire output power range P_o as calculated analytically and measured experimentally.

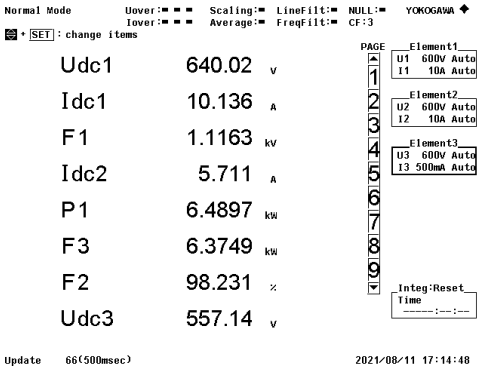


Figure 3.14: Screenshot taken on the Yokogawa WT500 Power Analyzer at the operation point with the highest measured efficiency P_o=6.37 kW

the calculated efficiency. The peak efficiency is measured at V_o=1000 V and I_o=5 A at 99.577%.

The waveforms of the Interleaved TCM buck converter at different operating points are given in Figures 3.18 and 3.19. The converter is placed in Current-Doubler mode in Figure 3.18, and in Voltage-Doubler mode in Figure 3.19Note that, the data shown for the voltage-doubler mode is measured only in one of the interleaved TCM buck converters.

3.8.3. TWO-STAGE CONVERTER EFFICIENCY

The power efficiencies of the two individual stages were given in the previous sections, Sections 3.8.1 and 3.8.2. Combining the power efficiencies given in these sections gives the total efficiency of the proposed two-stage converter in Figure 3.20, achieving a peak

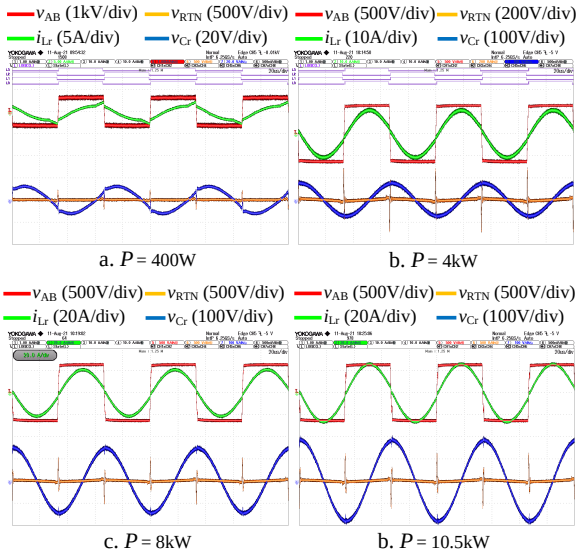


Figure 3.15: The operational waveforms of the LLC converter at different output powers P_o, with V_{in}=640V. i_{Lr} is the current through the resonant inductor, v_{Cr} is the voltage across the resonant capacitor, v_{AB} and v_{RTN} are the terminal voltage from the H-bridge and the voltage across the resonant tank network (the voltage across the series connection of L_r and C_r), respectively.

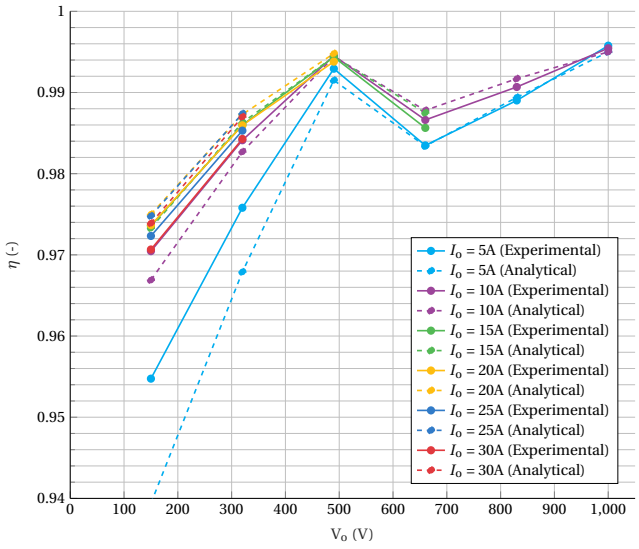


Figure 3.16: Comparison of $\eta_{analytical}$ and $\eta_{measured}$ for the Interleaved TCM Buck converter over the entire operating range. The output voltage is on the x-axis, and the colors indicate different I_o

efficiency of 97.66%.

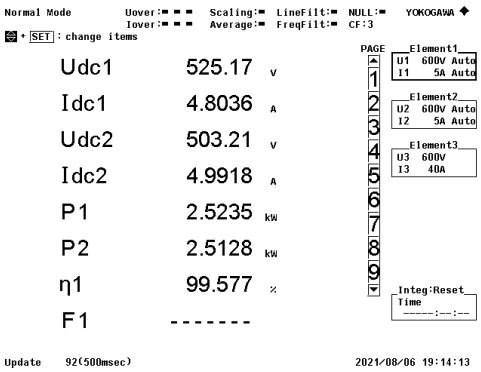


Figure 3.17: A screenshot taken on the Yokogawa WT500 Power Analyzer at the operation point with the highest measured efficiency V_o=1000 V, I_o=5 A.

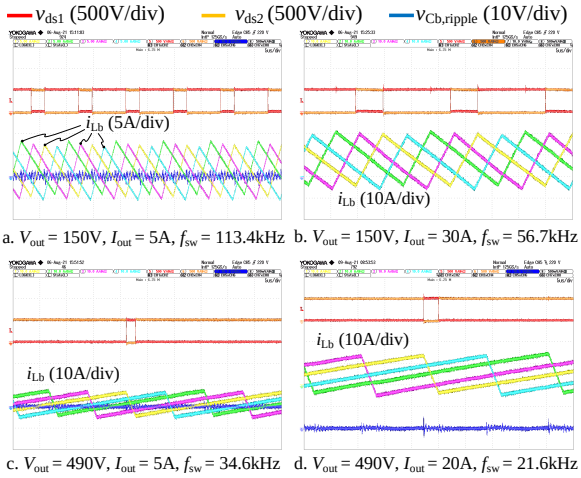
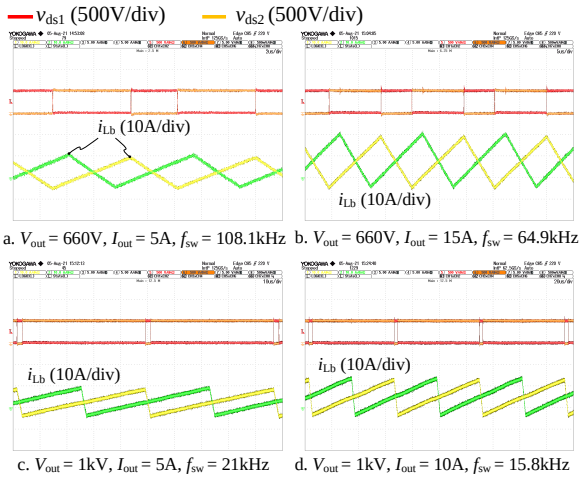


Figure 3.18: The operational waveform of the Interleaved TCM buck converter in current-doubler mode in different output voltage and current, with V_{in}=525V. v_{ds1} is the drain-source voltage on the high-side MOSFET, v_{ds2} is the drain-source voltage on the low-side MOSFET, $v_{Cb,ripple}$ is the voltage ripple on the output capacitor C_b.

3.9. CONCLUSION

The aim of this chapter was to propose an 11 kW DC-DC converter that is suited for EV charging with a wide output voltage range with very high efficiency over the entire operational range based on a resonant power converter topology. The implemented solution consisted of a two-stage power converter. This is based on an LLC resonant converter followed by an Interleaved TCM buck converter. The achieved output voltage range of 150-1000 V in the current study was not previously reported in literature regarding resonant power converters for EV charging. And therefore, the proposed converter is capable of charging different EV battery types while doing so very efficiently. A prototype of the



a. V_{out} = 660V, I_{out} = 5A, f_{sw} = 108.1kHz b. V_{out} = 660V, I_{out} = 15A, f_{sw} = 64.9kHz

c. V_{out} = 1kV, I_{out} = 5A, f_{sw} = 21kHz d. V_{out} = 1kV, I_{out} = 10A, f_{sw} = 15.8kHz

Figure 3.19: The operational waveform of the Interleaved TCM buck converters in voltage-doubler mode in different output voltage and current, with V_{in}=525V. v_{ds1} is the drain-source voltage on the high-side MOSFET, v_{ds2} is the drain-source voltage on the low-side MOSFET.

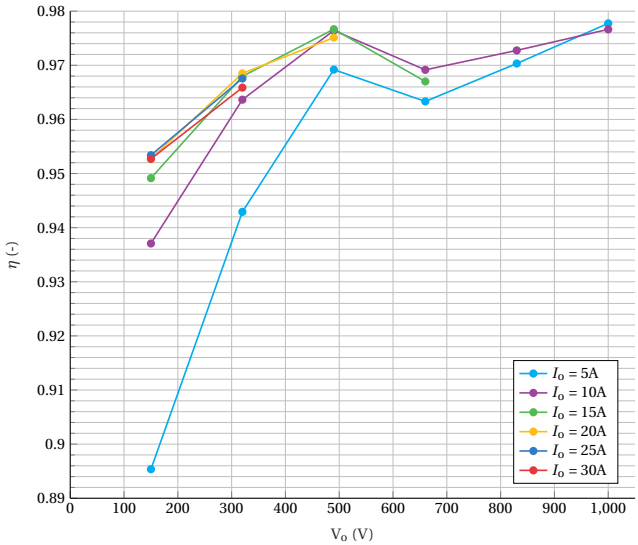


Figure 3.20: Measured efficiency of the two-stage LLC + interleaved TCM buck converter over the entire operating range. The efficiencies of the Interleaved TCM buck converter in Figure 3.16 are multiplied by the (interpolated) efficiency of the LLC converter determined from Figure 3.13 to obtain the efficiency of the two-stage converter.

proposed converter was designed and used to evaluate the efficiency: >95% efficiency was achieved over the entire output voltage range at maximum power, with a peak efficiency of 97.66%. The obtained efficiency for the 11 kW-400 V Charging cycle is 96.85%

and 95.67% for the 11 kW-800 V Charging cycle.

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4

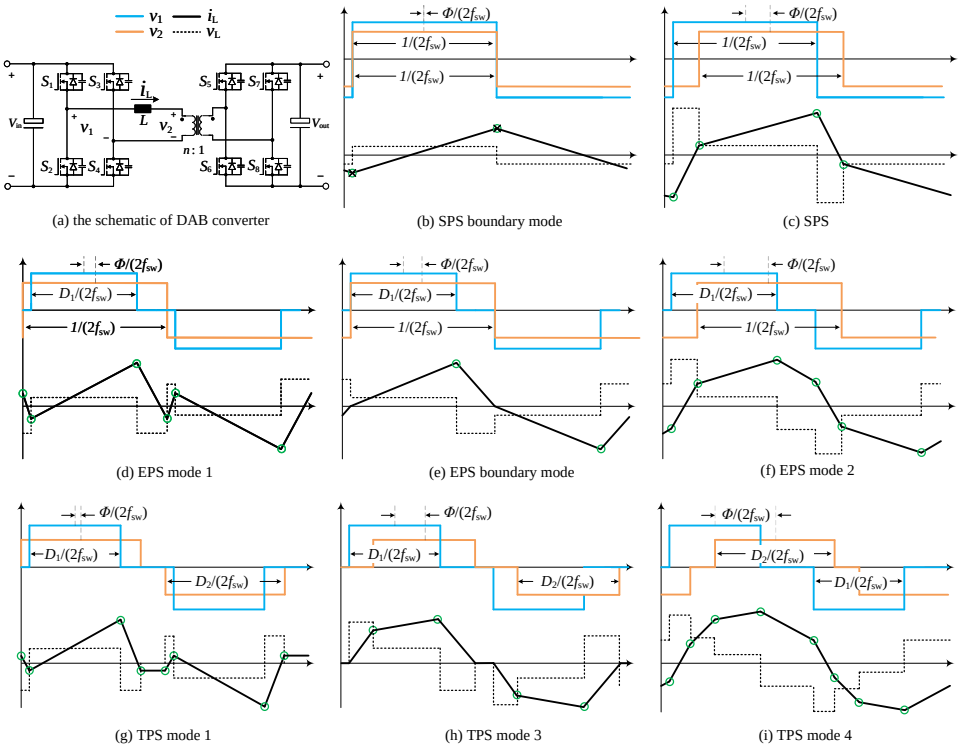
WIDE VOLTAGE RANGE DESIGN OF DUAL ACTIVE BRIDGE CONVERTER

This chapter proposes two modulation schemes for Dual Active Bridge (DAB) converters, aiming to maximize Zero Voltage Switching (ZVS) operation in a wide operational range. The first one is a ZVS-optimized constant frequency modulation scheme constructed based on the boundary conditions of ZVS operation. This modulation scheme provides the maximum number of ZVS events across a wide operational range with ease of implementation. Additionally, a variable frequency modulation scheme is proposed to enable continuous full ZVS operation for the DAB converter at full power, eliminating the loss of ZVS brought by the transitioning of modulation regions. This feature expands the full ZVS range, leading to improved Electromagnetic Interference (EMI) performance and overall power efficiency. These advancements make the combination of the proposed modulation schemes well-suited for applications such as off-board Electric Vehicle (EV) charging. Experimental validation is conducted on an 11-kW DAB converter prototype with an output voltage range from 250V to 950V, demonstrating the efficacy of the proposed modulation schemes in achieving ZVS and enhancing converter efficiency.[1]

[1] This chapter is based on:
D. Lyu, C. Straathof, T. B. Soeiro, Z. Qin and P. Bauer, "ZVS-Optimized Constant and Variable Switching Frequency Modulation Schemes for Dual Active Bridge Converters," in IEEE Open Journal of Power Electronics, vol. 4, pp. 801-816, 2023, doi: 10.1109/OJPEL.2023.3319970.

4.1. INTRODUCTION

The dual-active-bridge (DAB) converter is firstly proposed in [1, 2] as a soft switching DC/DC converter suitable for high power applications, and studies have been conducting ever since to improve its performance [3–39]. The DAB converter consists of two H-bridges, with a transformer that has a relatively large leakage inductance L, as shown in Figure 4.1(a). Each half-bridge in the circuit operates up to a 50% duty cycle. There are four control parameters that can be manipulated to control the DAB converter. Namely, the phase shift Φ between the two H-bridges, the effective duty cycle of the left and right H-bridge $D_{1,2}$, and the switching frequency f_{sw}. These parameters are depicted in the typical operational waveform shown in Figure 4.1(b)-(i).



(a) the schematic of DAB converter (b) SPS boundary mode (c) SPS

(d) EPS mode 1 (e) EPS boundary mode (f) EPS mode 2

(g) TPS mode 1 (h) TPS mode 3 (i) TPS mode 4

Figure 4.1: The schematics of the DAB converter and the typical operational waveform of SPS (c), EPS (d,f), TPS (g,h,i) modulation in the advantageous modes, and two boundary modes denoted as SPS transition mode (b) and EPS transition mode (e)

Due to its advantages of small number of components, zero voltage switching (ZVS) ability, buck-boost operation, and bidirectional power flow, The DAB converter is obtaining attention progressively in the electric vehicle (EV) charging application [21, 23, 27, 28, 35].

Most EVs launched last decade have a nominal battery voltage of around 400V. Currently, high-end EV manufacturers are increasingly adopting 800V battery architectures

due to their benefits: reduced vehicle weight and faster battery charging times using public DC-fast charging infrastructures. This is especially advantageous as public charger cable current ratings are limited by thermal management. Therefore, today the public DC-type EV charging infrastructures should be able to supply power efficiently to both 400V and 800V EV battery classes.

One of the main challenges for the DAB converter in the public EV charging application is maintaining the high-efficiency performance and zero voltage switching (ZVS) ability in an extended power and voltage regulation range. The conventional single phase shift (SPS) modulation method is the simplest modulation method, which regulates the voltage and power level by controlling Φ [1–3]. At unity voltage gain scenarios, the SPS modulation can provide ZVS over most of the operating range. Figure 4.1(c) shows the typical operational waveform of the SPS modulation method where all transistors operate in ZVS turn-on.

However, at non-unity voltage gain scenarios, the ZVS range is limited at light loads, and current stress is high compared to more advanced modulation methods [3–9, 11–15, 19, 20, 22–26, 28, 29, 31–35]. Figure 4.1(b) shows the waveform of an extreme mode of the SPS modulation, herein denoted as the SPS transition mode, where the operating power and Φ are close to zero. It can be seen that 4 out of 8 transistors lose ZVS. In order to enlarge the ZVS range and reduce the current stress of the SPS modulation especially in the light to medium load and non-unity voltage gain scenarios, the control parameters $D_{1,2}$ are introduced into the modulation methods. As a result, the extended phase shift (EPS) modulation, the dual phase shift (DPS) modulation and the triple phase shift (TPS) modulation are investigated.

The DPS modulation of DAB converter is introduced In [7] to eliminate reactive power in light load operations. The DPS adjusts D_1 and D_2 ($D_1 = D_2$) between 0% and 100% while controlling Φ. It offers wider power transmission and more power transfer than SPS with the same Φ and current stress as per [20]. [33] identifies four DPS modulation modes and proposes an optimized scheme using magnetizing current. However, [30] suggests that DPS is generally inferior to EPS due to higher current stress.

The EPS mode 2 modulation, as proposed in [5], extends the soft switching range of the DAB converter by adjusting Φ and D_1/D_2 based on the largest DC voltage. Although it enhances the ZVS range, it encounters hard-switching issues under light loads. Subsequent works have optimized and extended its soft switching capabilities, with EPS mode 1 enabling ZVS even in light load scenarios where EPS mode 2 fails [6, 12]. The asymmetric EPS modulation introduces a DC offset, necessitating a blocking capacitor [29]. Finally, the studies in [31, 32] employ magnetizing current to further extend the ZVS range, but this approach leads to sub-optimal transformer design and elevated current stresses.

Among TPS, EPS, and DPS, TPS is the most versatile modulation method, permitting independent control of all three parameters: Φ and $D_{1/2}$. EPS and DPS are derivatives of TPS, designed to minimize complexity. Out of the twelve identified TPS modes, due to symmetry, only five warrant examination [11, 13, 19, 24, 26]. These are labeled as TPS mode 1 to 5 [19, 26]. TPS modes 2 and 5 have been demonstrated to be disadvantageous [11, 13] due to their lack of ZVS ability and elevated current stresses. As a result, numerous modulation schemes in literature utilize TPS mode 1, 3, and 4 [11, 13, 19, 24, 26]. Figure 4.1(g)-(i) depict the typical waveforms of TPS mode 1, 3, and 4, respectively. It is

evident that EPS mode 1 is a specific case of TPS mode 1, while EPS mode 2 is a specific case of TPS mode 4.

Several researchers have proposed distinctive modulation schemes that amalgamate modulation methods to optimize efficiency performance for DAB converters relative to SPS modulation. The authors of [4, 9] recommend a blend of triangular (a boundary case between TPS mode 1 and 3) and trapezoidal (a specialized case of TPS mode 3) current modulation for optimal system efficiency. However, only four and two out of eight transistors can achieve ZVS in trapezoidal and triangular modes, respectively, with the remaining transistors only achieving Zero Current Switching (ZCS). In [11], to extend the soft-switching range to the zero-load condition and to reduce rms and peak currents, the recommendation is to operate in TPS mode 1 at low power due to its full ZVS ability and concurrently minimized rms current, and in EPS mode 2 (a special case of TPS mode 4) at high power. At maximum power, EPS mode 2 naturally transitions into SPS. However, the analysis of the critical ZVS condition is not accurate, as it overlooks the output capacitance of the transistors. This omission can result in sub-optimal ZVS performance during practical implementation. To mitigate the conduction and copper losses, [13] employs TCM (TPS mode 3) for low power, OTM (TPS mode 4) for medium power, and CPM (SPS) for high power, even though some switches do not achieve ZVS in TPS mode 3. Additionally, the formulation of the modulation scheme is intricate for practical implementation. The studies in [19,24,26] optimize current stress using varying combinations of EPS and TPS modes. [28] employs SPS for heavy loads and transitions to EPS2, EPS1, and TPS1 as the load decreases. However, implementing the transition between the nine modulation modes using a state machine is not straightforward, and the ZVS loss during the transition is not thoroughly explored. [35] introduces a modulation scheme for DAB converters that maximizes the ZVS range and achieves quasi-optimal inductor rms current, amalgamating TPS1, EPS1, EPS2, and SPS. In [36], universal analytical expressions for TPS modulation are derived, and an RMS current-minimized scheme, grounded in GOC equations, is introduced. However, it prioritizes RMS current reduction, potentially compromising optimal ZVS performance. Asymmetric duty modulation, explored in [37, 38], provides additional flexibility through duty cycle adjustments, resulting in reduced RMS current and an expanded soft-switching range. However, its complexity, compared to symmetrical duty modulations, poses challenges to implementation. The ZVS analysis in [38], based on the stored energy equation, omits energy considerations from the non-switching bridge, leading to inaccuracies acknowledged by the authors. Although [38] demonstrates full ZVS operation, it is confined to BUCK mode operation with a voltage regulation range from 0.5 to 1.

Component modifications and variable switching frequency modulation have also been explored in the literature to enhance the DAB converter's performance. [10] employs variable AC link reactance with a dual leakage transformer to mitigate peak transformer currents during light load SPS operation. [22] introduces a modulation scheme utilizing a voltage offset across the DC blocking capacitor, allowing for a broader soft-switching range with simple implementation. Expanding the ZVS range by decreasing magnetizing inductance is also possible [32, 33, 40]. However, these methods require hardware changes, such as specific transformer designs and additional capacitors, possibly reducing power density and increasing current stress. An alternative is to manipulate

the switching frequency without hardware alterations. [17] proposes finding the optimal design trade-off among switching loss, conduction loss, and drive loss by manipulating the switching frequency. However, the possibility of maximizing the ZVS range is not explored. The work in [18, 20] proposes including variable switching frequency in SPS and EPS modulation to extend the soft-switching range. However, the ZVS analysis is based on inductive and capacitive energy equations, which are inaccurate due to the omission of energy provided by the non-switching bridge.

In conclusion, compared to the operation with only SPS method, an appropriate modulation scheme, comprising SPS, DPS, EPS, and TPS methods significantly enlarges the ZVS range and reduces current stress in the DAB converter. However, it is still challenging to achieve a full ZVS operation in a wide voltage regulation range application such as EV charging due to the inevitable ZVS lost during the transition between these modulation methods. Most of the proposed modulation schemes in the literature focus on the optimization of current stresses, leading to sub-optimal ZVS performance. And the modulation scheme are practically hard to implement. Moreover, there is no study covering the wide voltage range operation of the DAB converter from 250V to 1000V, which is necessary for the off-board EV charging application.

In the context of EV charging applications, converters or power modules are expected to operate at full power for the majority of charging scenarios, particularly in common situations such as home charging and workplace charging [41]. In these scenarios, low to medium power chargers with a capacity of up to 50 kW are commonly used, and they operate at their full power until the batteries of the EVs reach a high state of charge (SOC). This behavior is evident in charging profiles from various sources such as [42–44], where 50 kW chargers continue to operate at full power until the EV's SOC exceeds 80%. In fast to ultra-fast charging scenarios, the individual power modules within the charger also operate at full power most of the time, particularly when implementing the multi-step constant current (MSCC) charging strategy [45]. Under this strategy, power modules run at full power until the required charging power decreases, at which point they are sequentially turned off. Charging profiles from sources like [46–49] exemplify these charging scenarios. Consequently, operating with a reduced number of ZVS events at full power operating points is undesirable due to its adverse effects on both Electromagnetic Interference (EMI) performance and power efficiency. It is crucial to achieving continuous ZVS operation for minimizing the switch-bridge cross-talk caused by the hard switching and achieving high efficiency performance throughout the charging process.

This chapter proposes to combine the TPS mode 1, EPS mode 1, EPS mode 2 together to form a ZVS-advantageous constant switching frequency modulation scheme. These three modes are chosen because their operational ranges are naturally connected, meaning there will not be any abrupt change of phase shifts during the changing of modes. With this modulation scheme, the DAB converter is able to operate with full ZVS for all eight switches in most of the operational points. However, two or four out of eight switches can lose ZVS during the transition region where the DAB changes between the EPS mode 1 and 2. To address this issue, for the dominating full power charging scenarios, the variable switching frequency is introduced into the modulation scheme to ensure full ZVS performance. Since in the EV charging application, the converter will operate in full power condition most of the time, this modulation scheme will ensure

reliable operation of the EV charger without introducing modification on the converter components or topology.

The main contributions of this chapter are as follows:

- The proposal of a ZVS-optimized constant frequency modulation scheme and its construction method based on straightforward ZVS analysis. The proposed scheme aims to maximize ZVS events in the DAB converter while ensuring easy practical implementation.
- The proposal of a variable switching frequency modulation scheme and its construction method to address the lost of ZVS issue during mode transition in the constant frequency modulation scheme. This variable switching frequency modualtion scheme ensures full ZVS operation of the DAB converter in a wide voltage range during the full power charging process to improve the EMI performance.
- The experimental testing of the proposed modulation schemes on an 11kW DAB prototype with a wide output voltage range (250-950V). This wide voltage range test of the DAB converter was not yet elaborated on in the literature. This is particularly important because it demonstrates the feasibility of the proposed modulation schemes for the future EV market.

4.2. ANALYTICAL EXPRESSIONS OF THE TPS MODE 1 AND 4

The EPS mode 1 and 2 modulations are special cases of TPS mode 1 and 4 modulations, which can be observed in Figure 4.1. Thus, the analyses of TPS mode 1 and 4 are presented in this chapter as they are more general and cover the cases for EPS mode 1 and 2. In order to be categorized into TPS mode 1 and 4 as shown in Figure 4.1(g) and Figure 4.1(i), the values of the phase shifts need to fall within the operational conditions summarized in Table 4.1.

Table 4.1: The operational range and the power calculation equations of the TPS mode 1 and 4

TPS	operational conditions	power
mode 1	$\lvert D_1 - D_2\rvert \geq 2\lvert\Phi\rvert$	$\frac{D_1\Phi V_{\text{in}} n V_{\text{out}}}{2Lf_{\text{sw}}}$, if $V_{\text{in}} \geq nV_{\text{out}}$
	$\text{sgn}(D_2 - D_1) = \text{sgn}(V_{\text{in}} - nV_{\text{out}})$	$\frac{D_2\Phi V_{\text{in}} n V_{\text{out}}}{2Lf_{\text{sw}}}$, if $V_{\text{in}} < nV_{\text{out}}$
mode 4	$D_1 + D_2 \geq 2\lvert\Phi\rvert$ $D_1 + D_2 \geq 2 - 2\lvert\Phi\rvert$	$\text{sgn}(\Phi)\frac{-(D_1^2+D_2^2+4\lvert\Phi\rvert^2-2D_1-2D_2-4\lvert\Phi\rvert+2)V_{\text{in}} n V_{\text{out}}}{8Lf_{\text{sw}}}$

For the SPS, TPS mode 1, and mode 4, two types of switching actions occur, the switching of a switching leg (a half-bridge), and the switching of a H-bridge. When the switching action of a half-bridge happens, the voltage of that H-bridge will change between zero and $\pm V$. And when the switching action of a H-bridge happens, the voltage of it will change between $+V$ and $-V$. Table 4.2 summarised the analytical expressions for the instantaneous current values of i_{L} at each switching action.

According to the different voltage changes, the general ZVS requirements for the switching actions are summarized in Table 4.3. Z is the characteristic impedance of the

Table 4.2: The steady state analytical expressions of i_L values for $\Phi > 0$

modulation		switching	i_L values
SPS		$v_1 : +V_{in} \rightarrow -V_{in}$	$\frac{V_{in}+(2\Phi-1)nV_{out}}{4Lf_{sw}}$
		$v_2 : -nV_{out} \rightarrow +nV_{out}$	$\frac{nV_{out}+(2\Phi-1)V_{in}}{4Lf_{sw}}$
TPS mode 1	$V_{in} \geq nV_{out}$	$v_2 : 0 \rightarrow +nV_{out}$	$\frac{D_2 nV_{out}-D_1 V_{in}}{4Lf_{sw}}$
		$v_1 : 0 \rightarrow +V_{in}$	$\frac{(2\Phi+D_1)nV_{out}-D_1 V_{in}}{4Lf_{sw}}$
		$v_1 : +V_{in} \rightarrow 0$	$\frac{(2\Phi-D_1)nV_{out}+D_1 V_{in}}{4Lf_{sw}}$
		$v_2 : +nV_{out} \rightarrow 0$	$\frac{D_1 V_{in}-D_2 nV_{out}}{4Lf_{sw}}$
	$V_{in} < nV_{out}$	$v_1 : 0 \rightarrow +V_{in}$	$\frac{D_2 nV_{out}-D_1 V_{in}}{4Lf_{sw}}$
		$v_2 : 0 \rightarrow +nV_{out}$	$\frac{(2\Phi-D_2)V_{in}+D_2 nV_{out}}{4Lf_{sw}}$
		$v_2 : +nV_{out} \rightarrow 0$	$\frac{(2\Phi+D_2)V_{in}-D_2 nV_{out}}{4Lf_{sw}}$
		$v_1 : +V_{in} \rightarrow 0$	$\frac{D_1 V_{in}-D_2 nV_{out}}{4Lf_{sw}}$
TPS mode 4		$v_1 : 0 \rightarrow +V_{in}$	$-\frac{D_1 V_{in}+(2\lvert\Phi\rvert+D_1-2)nV_{out}}{4Lf_{sw}}$
		$v_2 : -nV_{out} \rightarrow 0$	$\frac{(2\lvert\Phi\rvert+D_2-2)V_{in}+D_2 nV_{out}}{4Lf_{sw}}$
		$v_2 : 0 \rightarrow +nV_{out}$	$\frac{(2\lvert\Phi\rvert-D_2)V_{in}+D_2 nV_{out}}{4Lf_{sw}}$
		$v_1 : +V_{in} \rightarrow 0$	$\frac{D_1 V_{in}-(D_1-2\lvert\Phi\rvert)nV_{out}}{4Lf_{sw}}$

LC resonant circuitry during the half-bridge switching actions, and it can be calculated by Equation (4.1).

$$Z = \sqrt{\frac{L}{2C_{oss}}} \tag{4.1}$$

For the deriving of the expressions in Table 4.3, the conventional inductive and capacitive stored energy equation for ZVS analysis are used by numerous papers [18,20,38]. It is usually written as $0.5LI^2 > 0.5nC_{oss}V_{ds}^2$, in which L is the leakage or external inductance value, and n is the number of transistors involved during the switching transition. This equation oversimplifies the energy exchange during the switching transition because it ignores the energy provided by the non-switching bridge, leading to inaccurate ZVS analysis. In this chapter that energy is taken into consideration. As shown from the ZVS conditions listed in TABLE III, the ZVS current requirement expressions include the non-switching bridge voltage as well.

Combining the current values and the ZVS requirements for the switching actions, sets of inequations can be derived to ensure ZVS at each switching action. The boundary conditions for the DAB converter to operate with full ZVS for all eight switches can be derived for different modulation methods based on these sets of equations.

4.2.1. FULL ZVS BOUNDARY CONDITIONS FOR TPS MODE 1

WHEN $V_{IN} > nV_{OUT}$

Combining the current values and the ZVS requirements for the three switching actions, $(v_2 : 0 \rightarrow +nV_{out})$, $(v_1 : 0 \rightarrow +V_{in})$, $(v_1 : +V_{in} \rightarrow 0)$, the following inequation system can be derived for ensuring the full ZVS performance.

$$\frac{D_2 nV_{out} - D_1 V_{in}}{4Lf_{sw}} \geq \frac{nV_{out}}{Z/n} \tag{4.2}$$

$$\frac{(2\Phi + D_1)nV_{out} - D_1 V_{in}}{4Lf_{sw}} \leq -\frac{V_{in}\sqrt{1-2k}}{Z}, k_w = 0 \tag{4.3}$$

$$\frac{(2\Phi - D_1)nV_{out} + D_1 V_{in}}{4Lf_{sw}} \geq \frac{V_{in}\sqrt{2k-1}}{Z}, k_w = 1 \tag{4.4}$$

k is defined as the voltage ratio as in Equation (4.5), and k_w is the worst case value of k.

$$k = \frac{nV_{out}}{V_{in}} \tag{4.5}$$

Substituting k using the worst value k_w in this equation system, the following boundary conditions can be derived:

$$D_1 \geq \frac{2k|\Phi|}{1-k} + \frac{4Lf_{fw}}{Z(1-k)} \tag{4.6}$$

$$D_2 \geq \frac{2|\Phi|}{1-k} + \frac{4Lf_{fw}}{Zk(1-k)} + \frac{4Lf_{fw}}{Z/n} \tag{4.7}$$

Table 4.3: The ZVS requirements on i_L for different switching actions. V_1 and V_2 here are the voltage value of v_1 and v_2 at the switching actions.

switching actions	conditions	i_L requirement
$v_1: 0 \rightarrow +V_{in}$	if $V_2 < V_{in}/2$	$\leq -\frac{V_{in}\sqrt{1-2V_2/V_{in}}}{Z}$
	if $V_2 \geq V_{in}/2$	≤ 0
$v_1: +V_{in} \rightarrow 0$	if $V_2 > V_{in}/2$	$\geq -\frac{V_{in}\sqrt{1-2V_2/V_{in}}}{Z}$
	if $V_2 \leq V_{in}/2$	≥ 0
$v_1: 0 \rightarrow -V_{in}$	if $V_2 > -V_{in}/2$	$\geq \frac{V_{in}\sqrt{1+2V_2/V_{in}}}{Z}$
	if $V_2 \leq -V_{in}/2$	≥ 0
$v_1: -V_{in} \rightarrow 0$	if $V_2 < -V_{in}/2$	$\leq \frac{V_{in}\sqrt{1+2V_2/V_{in}}}{Z}$
	if $V_2 \geq -V_{in}/2$	≤ 0
$v_1: +V_{in} \rightarrow -V_{in}$	if $V_2 > 0$	$\geq \frac{V_{in}\sqrt{8V_2/V_{in}}}{Z}$
	if $V_2 \leq 0$	≥ 0
$v_1: -V_{in} \rightarrow +V_{in}$	if $V_2 < 0$	$\leq \frac{V_{in}\sqrt{8V_2/V_{in}}}{Z}$
	if $V_2 \geq 0$	≤ 0
$v_2: 0 \rightarrow +nV_{out}$	if $V_1 < nV_{out}/2$	$\geq \frac{nV_{out}\sqrt{1-2V_1/(nV_{out})}}{Z/n}$
	if $V_1 \geq nV_{out}/2$	≥ 0
$v_2: +nV_{out} \rightarrow 0$	if $V_1 > nV_{out}/2$	$\leq \frac{nV_{out}\sqrt{1-2V_1/(nV_{out})}}{Z/n}$
	if $V_1 \leq nV_{out}/2$	≤ 0
$v_2: 0 \rightarrow -nV_{out}$	if $V_1 > -nV_{out}/2$	$\leq -\frac{nV_{out}\sqrt{1+2V_1/(nV_{out})}}{Z/n}$
	if $V_1 \leq -nV_{out}/2$	≤ 0
$v_2: -nV_{out} \rightarrow 0$	if $V_1 < -nV_{out}/2$	$\geq -\frac{nV_{out}\sqrt{1+2V_1/(nV_{out})}}{Z/n}$
	if $V_1 \geq -nV_{out}/2$	≥ 0
$v_2: +nV_{out} \rightarrow -nV_{out}$	if $V_1 > 0$	$\leq -\frac{nV_{out}\sqrt{8V_1/(nV_{out})}}{Z/n}$
	if $V_1 \leq 0$	≤ 0
$v_2: -nV_{out} \rightarrow +nV_{out}$	if $V_1 < 0$	$\geq -\frac{nV_{out}\sqrt{8V_1/(nV_{out})}}{Z/n}$
	if $V_1 \geq 0$	≥ 0

Since D_2 is always larger than D_1 when $V_{in} > nV_{out}$, The value of Φ allowed for the equation system to hold true can be calculated by solving the following equation:

$$D_2 = \frac{2|\Phi|}{1-k} + \frac{4Lf_{fw}}{Zk(1-k)} + \frac{4Lf_{fw}}{Z/n} \leq 1 \tag{4.8}$$

Solving this equation, the boundary condition for the value of Φ can be derived as Equation (4.9). And the maximum value of Φ for the converter to operate in the TPS mode 1 modulation, $\Phi_{TPS(max)}$, can also be obtained from Equation (4.9).

$$|\Phi| \leq \frac{1-k}{2} - \frac{2Lf_{sw}}{Zk} - \frac{2Lf_{sw}n(1-k)}{Z} \tag{4.9}$$

4

WHEN $V_{IN} < nV_{OUT}$

Similarly, the following equation system can be derived for ensuring the full ZVS performance of the TPS mode 1 modulation when $V_{in} < nV_{out}$.

$$\frac{D_2 nV_{out} - D_1 V_{in}}{4Lf_{sw}} \leq -\frac{V_{in}}{Z} \tag{4.10}$$

$$\frac{(2\Phi - D_2)V_{in} + D_2 nV_{out}}{4Lf_{sw}} \geq \frac{nV_{out}\sqrt{1-2k^{-1}}}{Z/n}, k_w^{-1} = 0 \tag{4.11}$$

$$\frac{(2\Phi + D_2)V_{in} - D_2 nV_{out}}{4Lf_{sw}} \leq -\frac{nV_{out}\sqrt{2k-1}}{Z/n}, k_w^{-1} = 1 \tag{4.12}$$

Based on this inequation system, the following boundary conditions can be derived:

$$D_2 \geq \frac{2k^{-1}|\Phi|}{1-k^{-1}} + \frac{4Lf_{sw}n}{Z(1-k^{-1})} \tag{4.13}$$

$$D_1 \geq \frac{2|\Phi|}{1-k^{-1}} + \frac{4Lf_{sw}n}{Zk^{-1}(1-k^{-1})} + \frac{4Lf_{sw}}{Z} \tag{4.14}$$

$$|\Phi| \leq \frac{1-k^{-1}}{2} - \frac{2Lf_{sw}n}{Zk^{-1}} - \frac{2Lf_{sw}(1-k^{-1})}{Z} \tag{4.15}$$

4.2.2. FULL ZVS BOUNDARY CONDITIONS FOR EPS MODE 2

WHEN $V_{IN} > nV_{OUT}$

Combining the current values and the ZVS requirements for the three switching actions, $(v_1 : 0 \rightarrow +V_{in})$, $(v_2 : -nV_{out} \rightarrow +nV_{out})$, $(v_1 : +V_{in} \rightarrow 0)$, the following equation system can be derived for ensuring the full ZVS performance.

$$\frac{(2-2|\Phi|-D_1)nV_{out} - D_1 V_{in}}{4Lf_{sw}} \leq -\frac{V_{in}\sqrt{1+2k}}{Z}, k_w = 1 \tag{4.16}$$

$$\frac{(2|\Phi|-1)V_{in} + nV_{out}}{4Lf_{sw}} \geq 0 \tag{4.17}$$

$$\frac{D_1 V_{in} + (2|\Phi|-D_1)nV_{out}}{4Lf_{sw}} \geq \frac{V_{in}\sqrt{2k-1}}{Z}, k_w = 1 \tag{4.18}$$

Based on this equation system, the following boundary conditions can be derived, and the minimum value of D and Φ for the DAB converter to operate in the EPS mode 2 modulation with full ZVS, $D_{\text{EPS2(min)}}$ and $\Phi_{\text{EPS2(min)}}$, can also be calculated.

$$D_1 \geq \frac{(2-2|\Phi|)k + (4\sqrt{3}Lf_{\text{sw}})/Z}{1+k} \tag{4.19}$$

$$D_1 \geq \frac{-2|\Phi|k + (4Lf_{\text{sw}})/Z}{1-k} \tag{4.20}$$

$$|\Phi| \geq 0.5 - 0.5k \tag{4.21}$$

WHEN $V_{\text{IN}} < nV_{\text{OUT}}$

$$\frac{(2|\Phi|-1)nV_{\text{out}} + V_{\text{in}}}{4Lf_{\text{sw}}} \geq \frac{nV_{\text{out}}\sqrt{8k^{-1}}}{Z}, k_{\text{w}} = 1 \tag{4.22}$$

$$\frac{D_2 nV_{\text{out}} + (2|\Phi| + D_2 - 2)V_{\text{in}}}{4Lf_{\text{sw}}} \geq \frac{nV_{\text{out}}\sqrt{2k^{-1}-1}}{Z/n}, k_{\text{w}} = 1 \tag{4.23}$$

$$\frac{D_2 nV_{\text{out}} + (2|\Phi| - D_2)V_{\text{in}}}{4Lf_{\text{sw}}} \geq \frac{nV_{\text{out}}\sqrt{1-2k^{-1}}}{Z/n}, k_{\text{w}} = 0 \tag{4.24}$$

Based on this inequation system, the following boundary conditions can be derived:

$$D_2 \geq \frac{(2-2|\Phi|)k^{-1} + 4nLf_{\text{sw}}/Z}{1+k^{-1}} \tag{4.25}$$

$$D_2 \geq \frac{-2|\Phi|k^{-1} + 4nLf_{\text{sw}}/Z}{1-k^{-1}} \tag{4.26}$$

$$|\Phi| \geq 0.5 - 0.5k^{-1} + \frac{4\sqrt{2}Lf_{\text{sw}}}{Z} \tag{4.27}$$

4.3. THE ZVS-OPTIMIZED CONSTANT FREQUENCY MODULATION SCHEME

There are infinite combinations of Φ and $D_{1/2}$ that can operate the DAB converter at a certain operational power, switching frequency, input and output voltage. A construction method is thus needed to guide the selection of the advantageous values of Φ and $D_{1/2}$ for the modulation scheme based on the optimization objectives. A straightforward construction method is proposed based on the full ZVS boundary conditions derived in the last section to construct a ZVS-optimized constant switching frequency modulation scheme. This modulation scheme features continuity of the phase shift values, meaning no abrupt change of phase shift value will happen during the operation. And full ZVS operation can be achieved in the majority of the operational range.

4.3.1. CONSTRUCTION OF THE MODULATION SCHEME

This modulation scheme consists of three regions. The converter will operate in the EPS mode 2 region at high power and in the TPS mode 1 region at low power. An EPS mode 1 region is in between to connect them. To achieve the optimal ZVS performance in the whole range, a straightforward method of constructing the modulation scheme is proposed, in which the values of phase shifts in each region are determined by linear interpolation between two anchor operational points. Compared to using Lagrange multiplier method to minimize current stress [39], this method does not require complex calculation. Thus, it is a simple and effective way to construct ZVS-optimized modulation schemes.

For the EPS mode 2 region, the first anchor point is where the converter's power is maximized. It can be written as Equation (4.28).

$$\begin{cases} |\Phi| = 0.5 \\ D_1 = 1 \\ D_2 = 1 \end{cases} \tag{4.28}$$

The other anchor point of the EPS mode 2 region is defined by $\Phi_{\text{EPS2(min)}}$ and $D_{\text{EPS(bdr)}}$. $\Phi_{\text{EPS2(min)}}$ is the minimum value according to Equation (4.21) or Equation (4.27) depending on the value of k, and $D_{\text{EPS(bdr)}}$ is the value of D to in the EPS transition mode as shown in Figure 4.1(e). Thus, this anchor point can be written as Equation (4.29).

$$\begin{cases} |\Phi| = \Phi_{\text{EPS2(min)}} \\ D = D_{\text{EPS(bdr)}} = 1 - 2\Phi_{\text{EPS2(min)}} \end{cases} \tag{4.29}$$

Note that, since it is EPS mode, one of $D_{1/2}$ equals to 1 depending on the value of k, and the non-unity D is calculated according to Equation (4.29).

With the two anchor points, the non-unity value of $D_{1/2}$ inside the EPS mode 2 region can be calculated based on the value of Φ by linear interpolation by:

$$D_{1/2} = \frac{0.5 + \Phi_{\text{EPS2(min)}}(2|\Phi| - 2)}{0.5 - \Phi_{\text{EPS2(min)}}}, \Phi_{\text{EPS2(min)}} < |\Phi| \leq 0.5 \tag{4.30}$$

The TPS mode 1 region starts at $\Phi = 0$ and ends at $\Phi_{\text{TPS(max)}}$ defined by Equation (4.9) or Equation (4.15), at which point either D_1 or D_2 will be equal to 1. With these two anchor Φ values defined for the TPS mode 1, the values of D_1 and D_2 inside the TPS mode 1 can be obtained based on the minimum values to ensure full ZVS operation, which can be calculated based on $|\Phi|$ value and Equations (4.6) and (4.7) or Equations (4.13) and (4.14).

The EPS mode 1 region bridges these two regions. The values of $D_{1/2}$ can be calculated using linear extrapolation between the two anchor points of the EPS mode 2 and TPS mode 1 regions. The resulting equations for $D_{1/2}$ are shown in Equation (4.31). $\Phi_{\text{TPS(max)}}$ is the maximum value of $|\Phi|$ to operate in the full ZVS region of TPS mode1, which can be calculated by Equation (4.9) or Equation (4.15). $D_{1/2,\text{TPS(max)}}$ is the maximum value of $D_{1/2}$ to operate in the full ZVS region of TPS mode 1, and it can be calculated by substituting $|\Phi|$ with $\Phi_{\text{TPS(max)}}$ in Equations (4.6) and (4.7) or Equations (4.13)

and (4.14).

$$D_{1/2} = \frac{1-2\Phi_{\text{EPS(min)}} - D_{1/2,\text{TPS(max)}}}{\Phi_{\text{EPS(min)}} - \Phi_{\text{TPS(max)}}} (|\Phi| - \Phi_{\text{TPS(max)}}) + D_{1/2,\text{TPS(max)}} \tag{4.31}$$

Using this construction method, the phase shift values of the constant frequency modulation scheme can be calculated for different k values. Furthermore, by applying the power calculation equation in Table 4.1, the corresponding power level at each operational point can be calculated. Figure 4.2 shows four examples of the constant frequency modulation scheme and the values of phase shift for different values of k. It can be seen that when $k < 1$ and the DAB converter is operating in the BUCK mode, it operates in EPS mode 2 when the power is high and transitions into EPS mode 1 and further into TPS mode 1 when the power level decreases. A special case of the modulation scheme is when k is close to 1, as shown in Figure 4.2(c). In this case, the minimum value of $|\Phi|$ required for the full ZVS operation in EPS mode 2 is close to zero based on Equations (4.21) and (4.27). This indicates that the converter will operate mostly in EPS mode 2, and will not transition into TPS mode 1. When V_{out} further increases and the DAB converter is in the BOOST mode, the maximum power of the converter can be easily reached with a small value of Φ, meaning the converter might operate mostly in the TPS mode 1 region and transition into EPS mode 1 or EPS mode 2 when the power level is approaching its maximum. In the example of Figure 4.2(d) where V_{out} is high, the DAB converter operates in TPS mode 1 in its power range, and at the maximum power, the operation is at the edge between the TPS mode 1 and EPS mode 1 region.

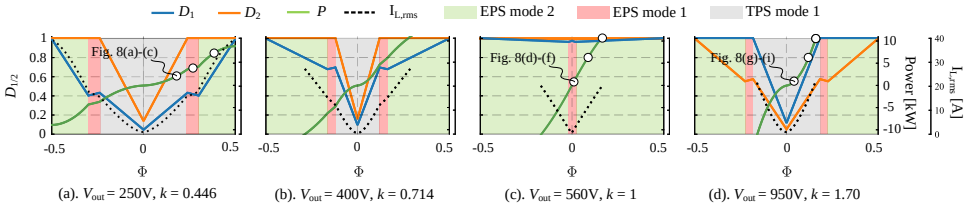


Figure 4.2: The phase shift ($D_{1/2}$ and Φ) and power values for the constant frequency TPS + EPS modulation scheme, under different k values. f_{sw} = 25kHz, and other specifications of the converter can be found in Table 4.4

4.3.2. LOSS OF ZVS DURING TRANSITION

Even though it is possible for all the switches of the DAB converter to have ZVS when it is operated in the TPS mode 1, EPS mode 1, and EPS mode 2, certain switches will lose the ZVS when the operation is at the boundary between two modes. A straightforward way to explain the loss of ZVS is that, in such boundary regions, the switching actions of the H-bridge I are very close to, or even overlapping, that of the H-bridge II (H-bridge I is the left hand side full bridge, and H-bridge II is the right side one). For the EPS boundary mode illustrated in Figure 4.1(c), the switching action of ($v_1 : 0 \rightarrow +V_{\text{in}}$) overlaps that of ($v_2 : -nV_{\text{out}} \rightarrow +nV_{\text{out}}$), and ($v_1 : 0 \rightarrow -V_{\text{in}}$) overlaps that of ($v_2 : +nV_{\text{out}} \rightarrow -nV_{\text{out}}$). It can be

seen from Table 4.3 that the switching action ($v_1 : 0 \rightarrow +V_{\text{in}}$) requires a negative current value for ZVS, while the switching actions ($v_2 : -nV_{\text{out}} \rightarrow +nV_{\text{out}}$) requires a positive current value. Therefore, the ZVS requirement for one of the switching actions can not be fulfilled, and ZVS for certain switches will be lost. Similarly, operating at the edge of the operation region where the switching actions of the two H-bridges are very close will lead to insufficient current values for different ZVS requirements, resulting in partial ZVS or even hard switching. Therefore, this proposed constant frequency modulation scheme introduces improvements to the number of ZVS events compared to other modulation methods, but the loss of ZVS for certain transistors during the transition of modulation regions is inevitable.

Based on the method of construction of the modulation scheme, it is clear that the converter is able to operate with full ZVS in the TPS mode 1 region. This is because all the values of $D_{1/2}$ and Φ in this region fulfill the ZVS requirements shown in Equations (4.6), (4.7) and (4.9) or Equations (4.13) to (4.15).

However, full ZVS will not always be achieved in the EPS mode region. The reason lies in the choice of the anchor points. As explained in Section 4.3.1, the second anchor point for the EPS mode 2 region is at $|\Phi| = \Phi_{\text{EPS(min)}}$, and $D_{1/2} = 1 - 2\Phi_{\text{EPS(min)}}$. In this operational point, even though the ZVS requirement for Φ as shown in Equation (4.21) or Equation (4.27) is fulfilled, the ones for $D_{1/2}$ as written in Equations (4.19) and (4.20) or Equations (4.25) and (4.26) are not guaranteed. This indicates that 2 or 4 transistors on the primary side might lose ZVS when the operation is close to this anchor point of EPS mode 2 region.

This operational point is still chosen as the anchor point of EPS mode 2 region because the resulting modulation scheme offers better overall ZVS performance in the whole operational range. The alternative anchor point is at $|\Phi| = \Phi_{\text{EPS2(min)}}$ with $D_{1/2} = D_{\text{EPS2(min)}}$ fulfilling the ZVS requirements of Equations (4.19) and (4.20) or Equations (4.25) and (4.26). With this anchor point, all the operational points inside the EPS mode 2 region will achieve full ZVS. However, part of the resulting operational region that bridges this anchor point to that of the TPS mode 1 can only achieve ZVS on two out of eight transistors.

To explain this phenomenon, the constant frequency modulation scheme at $V_{\text{out}} = 250V$, k = 0.446 and $f_{\text{sw}} = 25\text{kHz}$ is shown in Figure 4.3 together with the important boundaries of Φ and D. Moreover, the number of switches that can achieve ZVS is also marked in the specific regions. It can be seen that by following the proposed method of scheme construction, the DAB converter will operate with 8/8 ZVS in the whole TPS mode 1 region and most of the EPS mode 2 region, but will operate with 6/8 ZVS in edge of the EPS mode 2 region and the EPS mode 1 region. However, if the alternative anchor point of EPS mode 2 is used, the resulting modulation scheme (indicated by the dashed blue line) will include a specific region inside the EPS mode 2 region where the only 2/8 transistors can achieve ZVS. Note that it is still possible to achieve partial ZVS for the other six switches.

The loss of ZVS happens not only when the power level changes while k is fixed, but also when k changes and the power level is fixed. Figure 4.4 shows the phase shift values at different V_{out} for the constant frequency modulation scheme at the full power operation. When V_{out} is low, the DAB converter needs to operate with high values of Φ and

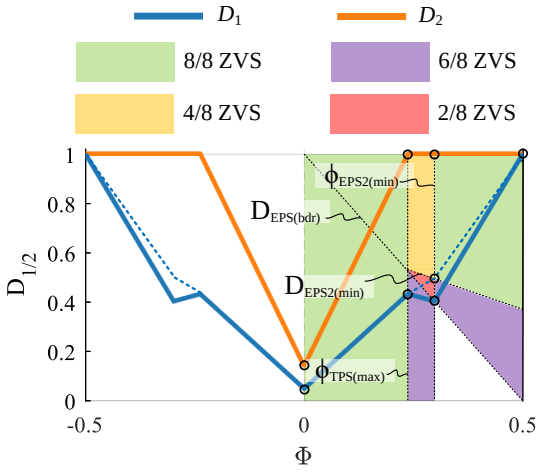


Figure 4.3: The phase shift ($D_{1/2}$ and Φ) values for the constant frequency TPS + EPS modulation scheme when $V_{out} = 250V$, k= 0.446, $f_{sw} = 25$kHz. Specifications of the converter can be found in Table 4.4. The blue dashed line shows the alternative scheme when the anchor point of EPS mode 2 is changed

in the EPS mode 2 region to deliver the maximum rated power. However, as V_{out} further increases, the maximum power operational point will shift from EPS mode 2 region into EPS 1. During the transition from EPS mode 2 to EPS mode 1 ($700V < V_{out} < 870V$), the converter will lose ZVS on two transistors during the full power operation according to the calculation based on the ZVS requirements in Table 4.3. It can be seen that, the loss of ZVS during mode transition can cover a significant operational range as illustrated in Figure 4.4. This will bring detrimental impacts on the EMI and efficiency performance of the DAB converter, especially when it is used in the EV charging application due to the reasons explained in the Introduction.

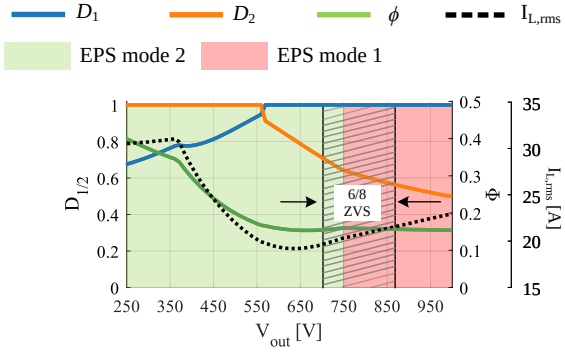


Figure 4.4: The phase shift ($D_{1/2}$ and Φ) values for the constant frequency TPS + EPS modulation scheme at the full power operation, $f_{sw} = 25$kHz. Specifications of the converter can be found in Table 4.4

4.4. THE VARIABLE FREQUENCY MODULATION SCHEME FOR FULL POWER OPERATION

To prevent the DAB from operating at the edge of the operational regions where certain switches will lose ZVS during full power operation, the phase shift Φ can be increased or decreased so that the operation moves more deeply into ZVS-beneficial regions. However, the operational power of the DAB converter will be changed by changing Φ. Table 4.1 shows the conditions of D_1, D_2, Φ and the power calculation of the TPS mode 1 and mode 4. It can be seen that the phase shift Φ is a proportional control parameter for the power of the DAB operation. Therefore, it is not possible to maintain ZVS by only changing Φ. To solve this issue, the switching frequency f_{sw} can be utilized.

4.4.1. WORKING PRINCIPLE

As can be seen from the equations of power calculation in Table 4.1, the power is inversely proportional to f_{sw}. Thus, The switching frequency f_{sw} can be utilized as an additional control parameter to shift the operation of the DAB converter to the ZVS-beneficial modulation modes without changing the power level. f_{sw} can either be increased or decreased to help maintain the ZVS performance. The first one is to increase f_{sw} when the DAB converter is about to enter the boundary mode from EPS mode 2, which decreases the output power, requiring an increase in Φ to achieve the same power. As a result, the operation will remain in the EPS mode 2 region where full ZVS can be achieved. Similarly, f_{sw} can be reduced and Φ needs to be reduced to maintain the same power. The lower value of Φ will help to maintain the operation in the full ZVS part of the TPS mode 1 region.

From the ZVS point of view, whether f_{sw} is increased or decreased is inconsequential as long as ZVS is achieved. However, each approach has their pros and cons. In the case of decreasing f_{sw}, the switching losses on the transistors can be mitigated, but the dB/dt and magnetic flux density stress of the transformer core increases. This means the magnetic components must be designed at the lowest switching frequency and most critical flux density to avoid saturation, resulting in the oversizing of magnetic components. Conversely, increasing f_{sw} will amplify the switching losses, but due to lower dB/dt and flux density stress at higher f_{sw} the magnetic components can be designed similarly to those in the conventional constant frequency modulation. Therefore, aside from the EMC filter circuitry, no hardware change is required when f_{sw} is increased, and this maintains the converter's power density and lowers the design complexity. This chapter focuses on the case of increasing f_{sw}.

4.4.2. CONSTRUCTION OF THE MODULATION SCHEME FOR FULL POWER OPERATION

The variable frequency modulation scheme is modified based on the constant frequency modulation scheme. Since the operation always remains in the EPS mode 2 region in the variable switching frequency modulation scheme, the anchor point of the EPS mode 2 region can be chosen to be the alternative one that fulfills the full ZVS requirements, which is at $|\Phi| = \Phi_{\text{EPS2(min)}}$ with $D_{1/2} = D_{\text{EPS2(min)}}$. In this way, the EPS mode 2 region is utilized more efficiently.

The value of phase shifts and f_{sw} for the variable switching frequency modulation scheme for full power operation is obtained by iteration on the basis of the constant frequency modulation scheme in full power. Firstly, the constant frequency modulation scheme is constructed with the new anchor point and interpolation method. Secondly, the operational region / ZVS performance of the DAB converter operating at its maximum power in this constant frequency modulation scheme is checked. If the operation is not in the ZVS-beneficial EPS mode 2 region and full ZVS can not be achieved, f_{sw} will be increased by an increment. Then Φ will be increased accordingly and $D_{1/2}$ will be re-calculated based on the construction method for the constant frequency modulation scheme explained in Section III-A with the new f_{sw}. This is done until the same power level before changing f_{sw} is reached. Then, the ZVS requirements will be checked again. If full ZVS is not yet achieved, the previous step will be repeated, and f_{sw} and Φ will be further increased until full ZVS operation is reached. This process is looped through different values of k to cover the whole voltage regulation range.

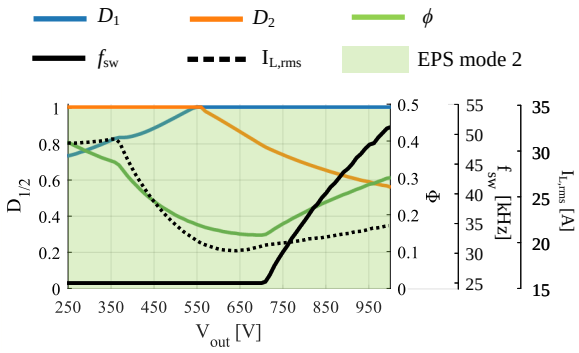


Figure 4.5: The phase shift ($D_{1/2}$ and Φ) and f_{sw} values for the variable frequency modulation scheme at the full power operation. Specifications of the converter can be found in Table 4.4

Figure 4.5 shows the resulting variable frequency modulation scheme for full power operation. It can be seen that starting from $V_{out} \approx 700V$, f_{sw} is increased from 25kHz to around 50kHz, allowing the converter to operate with an increased value of Φ compared to Figure 4.4. As a result, the full power operation remains in the ZVS-beneficial EPS mode 2 region for the whole output voltage range. This indicates that by using the proposed variable frequency modulation scheme, the DAB converter can always have full ZVS during the full-power operation in the whole output voltage range, which is essential for the EV charging application.

Note that it is possible to extend the variable switching frequency modulation to lower power with the same construction method. In this chapter, it is only applied to the full power operation because it is identified as the dominating operational scenario for EV charging.

4.5. EXPERIMENTAL VERIFICATION

An 11kW DAB converter prototype is built to verify the ZVS performance of the proposed modulation schemes. This converter features a wide output voltage range from 250V to 950V, which ensures its effectiveness in charging both 400V and 800V EVs. Figure 4.6 shows the DAB prototype. Table 4.4 summarizes the specification of the DAB prototype.

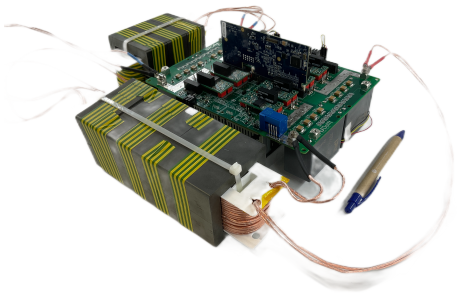


Figure 4.6: The picture of the 11kW DAB converter prototype

A lookup table based power control is implemented in the micro-controller TMS320F28379D for the DAB prototype. Figure 4.7 shows the control method of the prototype. This method is simple and does not require much computational resources. To generate the required lookup table, a matrix containing the power at a given value of Φ, V_{in} and V_{out} is created in Matlab. This is done with a very high resolution for Φ. For each combination of V_{in} and V_{out}, the power vs Φ curve is sampled at fixed power values using the 1D interpolation function. These values of Φ are then stored in a 3D matrix used in the lookup table to determine Φ based on the converter power reference, V_{in} and V_{out}. The values of D_1 and D_2 are paired with Φ based on the construction of the modulation scheme.

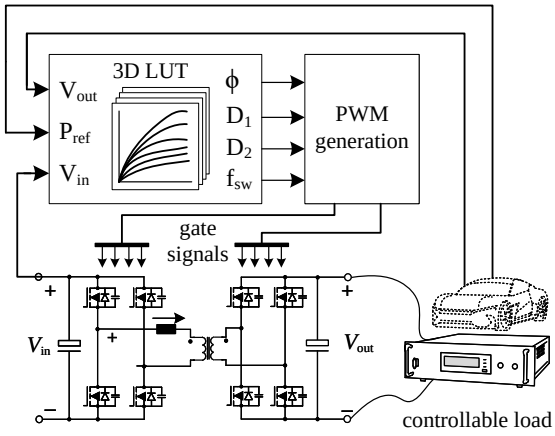


Figure 4.7: The diagram of the lookup table control method

Table 4.4: The specification of the DAB prototype

V_{in} [V]	640
V_{out} [V]	250 - 950
P_{max} [kW]	11
$I_{\text{out(max)}}$ [A]	30
Transistor	G3R20MT12K
Litz wire	AWG41 x 600
Transformer core shape	EE70/33/32
Number of stacked cores n_{cores}	5
Number of parallel wires	2
N_{pri}	16
N_{sec}	14
Leakage inductance L_{k} [μH]	16.2
External inductor core shape	EE70/33/32
Number of stacked cores n_{cores}	3
Number of parallel wires	2
N	9
Inductor airgap [mm]	1.42
Inductance L_{ext} [μH]	87.8

During the charging operation, V_{in} and V_{out} of the DAB converter are measured. Together with the required charging power value P_{ref} sent by the EV, the values of the phase shifts and switching frequency can be extracted from the lookup table. These values are then used to generate the PWM gate signals for the transistors.

4.5.1. RESULTS OF CONSTANT FREQUENCY MODULATION SCHEME

Firstly, the constant frequency modulation scheme is tested on the prototype to set up a benchmark of ZVS and efficiency performance. Figure 4.8 shows the operational waveform of the DAB converter operated with the constant frequency modulation scheme. These nine waveforms are located in at the operational points shown in Figure 4.2.

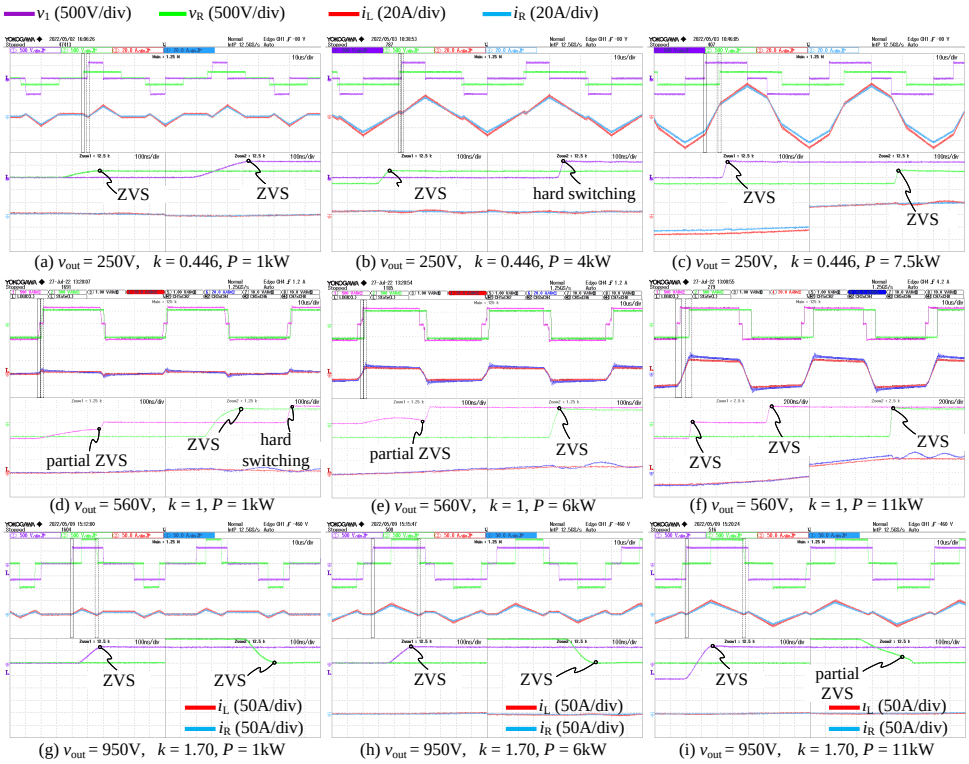


Figure 4.8: The waveform of the DAB converter operating with the proposed constant switching frequency TPS + EPS modulation scheme, with V_{in} = 640V and f_{sw} = 25kHz. v_R and i_R are the voltage and current measured from the secondary winding of the transformer

As can be seen from Figure 4.8(a)-(c), the converter transitions from TPS mode 1 to EPS mode 1 and further into EPS mode 2 when the power increases. In Figure 4.8(a) and (c), where the converter operates deeply in TPS mode 1 and EPS mode 2, all transistors have ZVS as indicated by the zoom-in waveform of the H-bridge voltage and current. And it can be seen in Figure 4.8(b), where the converter operates in EPS mode 1, the $0 \rightarrow +V_{in}$ switching action of the primary side half bridge does not meet the ZVS requirement

of having a zero or negative inductor current value. As a result, two transistors on the primary side lose ZVS as indicated by the sharp voltage change of v_1. In comparison, v_R has a slower and smooth change with this small positive value of inductor current, indicating that ZVS is achieved.

As v_{out} increases and k is close to 1, the converter operates only in EPS modes as seen in Figure 4.8(d)-(f). In the low power scenario as shown in Figure 4.8(d), the converter is operating in the EPS mode 1 and is very close to the EPS transition mode, as the switching action $0 \rightarrow +V_{in}$ occurs closely to the switching action $-V_{out} \rightarrow +V_{out}$. According to the general ZVS equations listed in Table 4.3, the switching action $-V_{in} \rightarrow 0$ and $0 \rightarrow +V_{in}$ requires a slightly negative i_L to achieve ZVS, but the switching action $-V_{out} \rightarrow V_{out}$ requires zero or positive i_L to achieve ZVS. As a result, only the four transistors on the secondary side achieve ZVS while the four on the primary side cannot, which is indicated by the waveform of v_1 and v_R in Figure 4.8(d). When the power increases, the converter operates at the edge of the EPS mode 2. The switching action $0 \rightarrow +V_{in}$ that requires a negative i_L is still close to the switching action $-V_{out} \rightarrow V_{out}$ which requires a positive i_L, leading to the loss of ZVS for the two transistors on the primary side. However, the switching action $-V_{in} \rightarrow 0$ now obtains ZVS due to the sufficiently negative i_L. When the power further increases and the converter operates deeply in the EPS mode 2, full ZVS is achieved as shown in Figure 4.8(f).

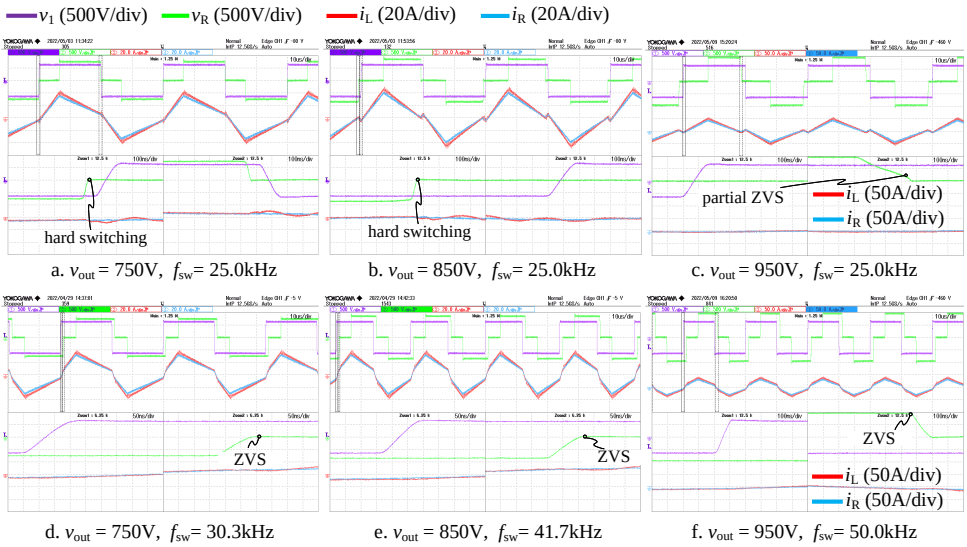
In the case where V_{out} is high, the converter only operates in the TPS mode 1 and at the edge of the EPS mode 1 region, as it can be seen in Figure 4.2 and Figure 4.8(g)-(i). Full ZVS can be easily achieved when the power level is not high and the converter is operating deeply in the TPS mode 1 region. However, as the power increases, the converter moves to the edge of the TPS mode 1 and EPS mode 1, making it challenging to maintain full ZVS performance. As can be seen from Figure 4.8(i), the switching action $+V_{out} \rightarrow 0$ occurs very close to $+V_{in} \rightarrow -V_{in}$. The prior one requires a negative current value for ZVS, while the later one requires a zero or positive current. Consequently, the two transistors of the half bridge on the secondary side achieve only partial ZVS as it can be seen in Figure 4.8(i).

In summary, the constant frequency modulation scheme operates well, and full ZVS is achieved in the majority of the operational range. However, the loss of ZVS happens when the operation is at the boundary of two modulation regions. In the case of unity voltage gain, 4 out of 8 transistors might lose ZVS, and in other boundary operation cases, 2 out of 8 transistors will lose ZVS. The loss of ZVS during full power operation is also demonstrated.

4.5.2. RESULTS OF VARIABLE FREQUENCY MODULATION SCHEME

Figure 4.9 shows the waveforms of the DAB converter operating with full power but different output voltage in the constant frequency (Figure 4.9(a)-(c)) and variable frequency modulation scheme ((Figure 4.9(d)-(f))).

It can be seen from Figure 4.9(a)-(c) that the converter in the constant frequency modulation scheme need to transition from EPS mode 2 to EPS mode 1 when V_{out} increases during full power operation. This is not beneficial for the ZVS performance because 2 out of 8 transistors will lose ZVS as explained in Section 4.3.2 and seen in Figure 4.9(a)-(c). In the case of EV charging where the full power operation takes up most



a. v_{out} = 750V, f_{sw}= 25.0kHz b. v_{out} = 850V, f_{sw}= 25.0kHz c. v_{out} = 950V, f_{sw}= 25.0kHz

d. v_{out} = 750V, f_{sw}= 30.3kHz e. v_{out} = 850V, f_{sw}= 41.7kHz f. v_{out} = 950V, f_{sw}= 50.0kHz

Figure 4.9: The waveform of the DAB converter with the proposed constant modulation scheme (a)-(c), and variable switching frequency modulation scheme (d)-(f), with V_{in} = 640V and P = 11kW (full power). v_R and i_R are the voltage and current measured from the secondary winding of the transformer

of the charging process, the loss of ZVS brought by the constant frequency modulation scheme will have a more significant impact, especially on the EMI performance.

With the variable switching frequency modulation scheme, both f_{sw} and Φ are adjusted so that the operation of the converter is kept in the full ZVS region. As shown in Figure 4.9(d)-(f), f_{sw} as well as Φ are increased compared to the constant frequency modulation scheme, moving the operation into the full ZVS EPS mode 2 region. This demonstrates that by using the variable switching frequency modulation scheme, the ZVS performance during the full power operation can be improved compared to the constant frequency modulation scheme.

4.5.3. EFFICIENCY PERFORMANCE

The measured efficiency performance of the proposed constant frequency modulation scheme in the whole operational range is shown in Figure 4.10. It is evident that the overall efficiency performance is excellent. The converter's efficiency is above 95% in the whole range, and the highest efficiency is measured to be 98.8%. Most importantly, the efficiency performance when operating above 2kW is well above 97%. This demonstrates that this modulation scheme can provide excellent efficiency performance to the DAB converter for the wide voltage range EV charging application.

Relatively low efficiency can be observed when operating at very low values of V_{out} and P, and also when V_{out} equals or close to $550V$. For the high power low V_{out} operation, the current stresses during the high power operation are problematic, leading to significant conduction losses and low efficiency performance. For the case when the power is low and V_{out} is high, the high switching losses brought by the high blocking volt-

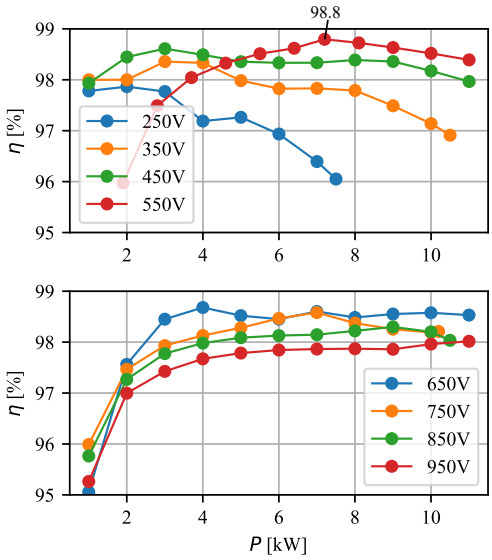


Figure 4.10: The tested efficiency of the constant frequency modulation schemes in the whole operation range

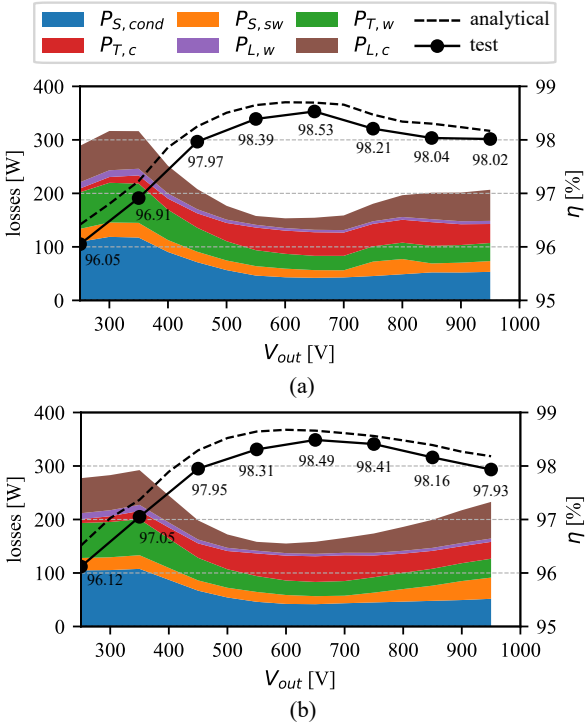


Figure 4.11: The tested efficiency, estimated losses, and estimated efficiency of the constant frequency and variable frequency modulation schemes at full power. (a) constant frequency modulation scheme. (b) variable frequency modulation scheme

age result in the efficiency drop. When V_{out} equals or close to $550V$, the voltage ratio k is close to 1. According to the constructed modulation scheme shown in Figure 4.2(c), the converter will lose ZVS during low power operation, which is verified by the test shown in Figure 4.8(d). This also contributes to the relatively low efficiency performance.

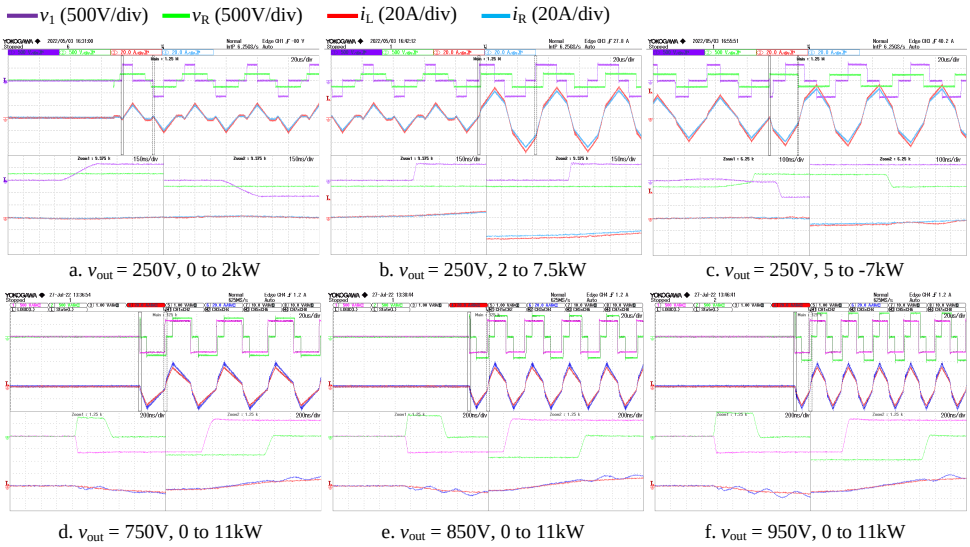
The efficiency performances of the two modulation schemes at full power operation are compared. Figure 4.11 shows the tested efficiency at the full power operation for the constant frequency and variable frequency modulation scheme. To provide more insights into the efficiency performance, the converter's losses and efficiency are also calculated analytically and plotted. The detailed losses calculation models can be found in [50, 51]. As it can be seen from Figure 4.11, the estimated efficiency matches well with the testing results. Thus, the estimated loss breakdown can be used to help interpret the efficiency performance.

It can be seen from the tested efficiency that, the variable switching frequency modulation scheme slightly improves the efficiency performance when $V_{out} > 700V$. As V_{out} continues to increase, the improvement of efficiency starts to reduce. When V_{out} is as high as 950V, the efficiency performance of the variable frequency modulation becomes slightly lower than that of the constant frequency one. The reason behind is that, the converter starts to lose ZVS when $V_{out} > 700V$ (as it can be seen in Figure 4.9(a)-(b)), causing the switching losses to increase (as it can be seen from the switching loss $P_{S,sw}$ stack plot in Figure 4.11). Whereas in the variable frequency modulation, by slightly increasing f_{sw}, the ZVS is maintained for all transistors, resulting in lower switching losses overall. As V_{out} continues to increase, the operation moves to the ZVS-beneficial region for the constant frequency scheme, but f_{sw} and $P_{S,sw}$ continue increasing for the variable frequency scheme. An interesting fact to point out is that, as f_{sw} increases, the transformer core loss $P_{T,c}$ is reduced due to the lowered flux density stress. This benefits the efficiency performance of the variable frequency scheme. Secondly, the efficiency performances for these two modulation schemes when $V_{out} < 700V$ are different. This is mainly due to the different choices of the anchor point for the EPS mode 2 region, whose reason and details are presented in Section 4.3.2.

Overall, Based on the tested efficiency, the average efficiency in full power operation for the constant frequency and variable frequency modulation schemes can be calculated to be 97.76% and 97.80%, respectively. This demonstrates that by adopting the variable frequency modulation scheme, not only full ZVS can be maintained for the whole voltage regulation range, but also the efficiency performance will not be sacrificed for the full power operation.

4.5.4. TRANSIENT BEHAVIOURS

Figure 4.12 shows the waveform of load change transient behaviours of the DAB prototype. It can be seen that, the PWM gate signal of the converter can be quickly adjusted in response to the load change. No obvious current and voltage overshoot and offset are introduced during the transient. It is worth mentioning that, the sudden load change from positive power (grid to vehicle) to negative power (vehicle to grid) as shown in Figure 4.12(c) will not happen in real scenarios. Moreover, the sudden output voltage change won't be an issue in EV charging because the EV battery voltage changes continuously and slowly during a charging session.



a. v_{out} = 250V, 0 to 2kW b. v_{out} = 250V, 2 to 7.5kW c. v_{out} = 250V, 5 to -7kW

d. v_{out} = 750V, 0 to 11kW e. v_{out} = 850V, 0 to 11kW f. v_{out} = 950V, 0 to 11kW

Figure 4.12: The waveform of transient behaviours of the DAB converter with the proposed constant frequency modulation scheme (a)-(c), and variable switching frequency modulation scheme (d)-(f), with V_{in} = 640V. v_R and i_R are the voltage and current measured from the secondary winding of the transformer

4.6. CONCLUSION

The ZVS-optimized constant and variable switching frequency modulation schemes proposed for the DAB converter aim to enhance ZVS performance in EV charging applications while concurrently maintaining high efficiency. These schemes are formulated based on ZVS boundary conditions, ensuring ease of implementation.

Contrary to existing modulation schemes that focus on optimizing current stress, the proposed constant switching frequency scheme excels in achieving extensive ZVS operation across a wide voltage regulation range, ensuring ZVS on all eight transistors for the majority of the operational span. Nonetheless, this chapter acknowledges the inevitable ZVS loss on two or four transistors during the modulation method transitions in the constant switching frequency modulation scheme, presenting challenges for EMI and efficiency.

To address this challenge, this chapter introduces a variable switching frequency modulation scheme and outlines its construction methodology. The essence of this approach lies in the dynamic adjustment of the switching frequency to strategically steer the converter's operation into ZVS-favorable regions whenever ZVS is jeopardized. This dynamic approach ensures that ZVS is maintained for all transistors. Given that power modules predominantly operate at full capacity in EV charging scenarios, this variable switching frequency scheme is specifically designed for full-power operation in this study.

Experimental testing on an 11kW, 250V-950V DAB prototype validates the efficacy of the proposed modulation schemes. The ZVS performances are verified for both modulation schemes. The extensive ZVS range of the constant switching frequency modulation scheme and the loss of ZVS during mode transitions are illustrated. The full ZVS oper-

ation of the variable switching frequency modulation scheme is also demonstrated for full power operation. The efficiency performances of both modulation schemes are presented, demonstrating successful improvement of ZVS performance while maintaining excellent efficiency.

The results of this study provide substantial evidence supporting the feasibility and effectiveness of the proposed modulation schemes. These findings indicate that the proposed modulation schemes are promising solutions for enhancing the performance and reliability of DAB converters in the context of wide voltage range EV charging applications.

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5

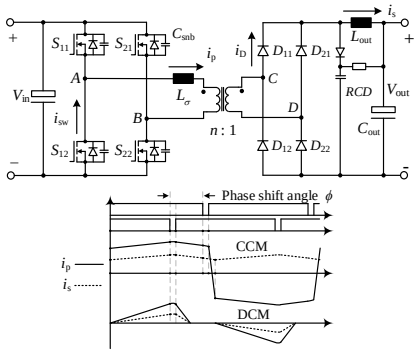
MULTI-OBJECTIVE DESIGN OF THE DC/DC CONVERTERS

This chapter presents an analysis, multi-objective design, and benchmark of three modified Phase-Shift Full-Bridge (PSFB) converters that are well-suited for Electric Vehicle (EV) battery charging applications, covering both typical battery voltage classes (400V and 800V). These three modified PSFB converters, denoted as the t-PSFB, r-PSFB, and i-PSFB converters, have the ability to reconfigure and provide better efficiency performance in the wide voltage range necessary for public EV battery charging applications. In this chapter, the characteristics and design considerations of these reconfigurable PSFB converters are discussed in detail. A multi-objective converter design process is proposed to optimize the average efficiency, normalized cost, and power density of the magnetic components and heat sinks. This design process employs the correlations between the cost and performance indexes of the key components derived based on open and accessible components data to estimate the design objectives. In this way, the design process is not constrained by certain component choices, making it easier to identify the most advantageous design. A benchmark study is conducted among the re-configurable PSFB topologies and the conventional PSFB circuit using the proposed multi-objective design process. To validate the analysis, a close-to-Pareto-front 11kW, 45kHz r-PSFB converter prototype with 640-840V input voltage and 250-1000V output voltage ranges is developed and tested.[1]

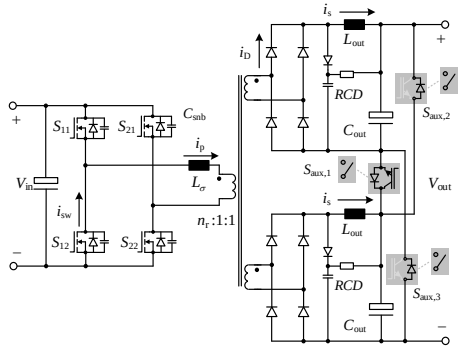
[1] This chapter is based on:
D. Lyu, T. B. Soeiro and P. Bauer, "Multi-objective Design and Benchmark of Wide Voltage Range Phase-Shift Full Bridge DC/DC Converters for EV Charging Application," in IEEE Transactions on Transportation Electrification, doi: 10.1109/TTE.2023.3254203.

5.1. INTRODUCTION

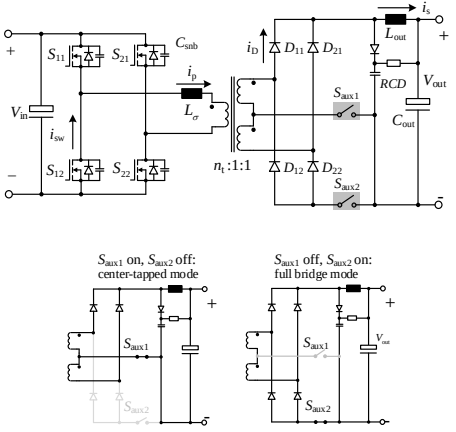
The Phase-Shift Full-Bridge (PSFB) isolated DC/DC converter shown in Figure 5.1(a) is a popular circuit in the application of Electric Vehicle (EV) charging, notably because this circuit features a current source behavior which facilitates the start-up and the control of the battery charging profile. Additionally, this circuit technology is mature, power efficient, simple to operate, and well-established in several other applications [1–12]. Unfortunately, the conventional PSFB (or conv-PSFB) topology is challenged to keep the high efficiency within an extensive output voltage range. The reason is that the efficiency of the PSFB technology drops as the phase-shift angle increases (or equivalent duty cycle and consequently the output voltage decreases).



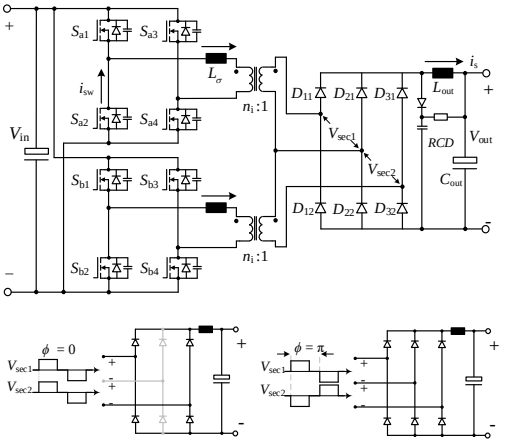
(a). The conventional PSFB converter and its typical waveform in the continuous conduction mode (CCM) and discontinuous conduction mode (DCM)



(b). The r-PSFB converter



(c). The t-PSFB converter



(d). The i-PSFB converter

Figure 5.1: The schematics of the conventional PSFB converter and three modified PSFB converters

Most EVs launched last decade have a nominal battery voltage of around 400V. As of today, the component technology for this voltage class is well-established with several automotive-qualified components available. Currently, the manufacturers of high-end

EVs are moving toward the 800V battery architectures [13–16] because the higher voltage results in weight saving across the EV and the potential reduction of the battery charging time while using a public DC-fast charging infrastructures, i.e., as the current rating of the public charger cables are limited to 350A the high voltage will potentially enable higher power injection into the battery bank where the limits will be imposed by the public charger and the thermal management of the battery. Therefore, today the public DC-type EV charging infrastructures should be able to supply power efficiently to both 400V and 800V EV battery classes.

Studies have been conducted to extend the PSFB-type converter's voltage range while keeping high efficiency. The work developed in [3] proposes a hybrid-switching PSFB converter that provides for the H-bridge converter a wide Zero Voltage Switching (ZVS) range for the leading leg and Zero Current Switching (ZCS) for the lagging leg. Interestingly, the freewheeling circulating losses can also be improved, and the undesirable voltage overshoots at the rectifying stage can be clamped well. However, additional passive components (two diodes, a capacitor, and an inductor) are needed, and the complexity of the converter increases. The work in [4] proposes a secondary-side PSFB converter that extends the soft-switching operation and improves the circulating current losses, but it comes with the cost of two additional switches and complex control. In [9], a ZVS full-bridge DC/DC converter is proposed, incorporating a diode clamping circuitry on the primary side for the voltage ringing clamping and uses an asymmetrical PWM modulation together with an additional auxiliary inductor to reduce circulating current losses. Unfortunately, none of these studies have investigated and proved with experimental results the high-efficiency performance in the voltage range of 400V and 800V EV charging.

Based on the idea of a re-configurable PSFB converter [17–20], the study in [12] provides a solution for the extensive voltage range necessary in today's market of public EV charging stations (e.g.,250-1000V).This circuit, denoted here as the r-PSFB converter, employs a two-secondary-winding transformer, two diode rectifiers, and three auxiliary switches as shown in Figure 5.1(b). By controlling the connection of the auxiliary switches, the two secondary sides can be connected in series when the required output voltage is high or in parallel when the needed output voltage is low. As a result, rectifier diodes with a halved voltage rating and transistors with a halved current rating can be utilized. Most importantly, the range of the phase shift control angle needed for the wide voltage range is also halved.

Instead of using two diode rectifiers with the two-secondary-winding transformer like the r-PSFB converter, one single diode rectifier can be used together with two additional auxiliary switches to make a re-configurable PSFB converter, as shown in Figure 5.1(c). This converter, which is first introduced in the literature by this chapter, is denoted here as the t-PSFB converter. The two-secondary-winding transformer and diode bridge of the t-PSFB converter can be configured into a full-bridge mode or a center-tapped mode by the connection of the auxiliary switches. Similar to the r-PSFB circuit, this t-PSFB converter reduces the operational phase shift control angle for the wide voltage operation. The number of rectifier diodes needed is half compared to the r-PSFB circuit, but higher voltage rating rectifier diodes are required simultaneously.

In the study of Wu et al. [21], an LLC resonant converter with a hybrid rectifier is proposed. This LLC converter has two H-bridge inverters on the primary side, two trans-

formers, and a three-leg diode bridge rectifier. By controlling the phase shift of the PWM signals of the two H-bridge inverters, the LLC converter can be operated as if the two circuits are connected in series or parallel. With this idea, the PSFB converter can be modified into an interleaved PSFB converter with a hybrid rectifier as shown in Figure 5.1(d). This converter, denoted as the i-PSFB, has the same performance regarding the reduction of operational phase shift in a wide voltage range like the r/t-PSFB converters but has doubled transistors counts and different transformer designs. 1700V rating diodes are required for the EV charging application aiming at an 800V class battery as load.

These converters shown in Figure 5.1 are well-suited for the wide voltage range public EV charging application due to their characteristic of re-configuration. However, the optimal design and benchmark of these converters in terms of the cost, power density, and efficiency performance have not been done. The cost estimation in the academic research of power electronics is challenging, primarily due to the poor avaliability of the components' cost data. In [22] component cost models of switched-mode power converters with an approximate rated power between 5 and 50 kW are derived. These models are useful for engineers as they can be incorporated into the converter design process, and they are also used in [23, 24]. These component cost models are largely dependent on variables related to physical component properties, making them not so straightforward to implement. Moreover, large database acquired from manufacturers is needed for a better fitting, which is not easily accessible.

This chapter aims to identify which one of the three modified PSFB converters is the most advantageous in the wide voltage range EV charging application, considering an 11kW power rating, 30A maximum output current, 640-840V input voltage, and 250-1000V output voltage range. To do so, A multi-objective design and benchmark process is proposed, with the normalized cost, average efficiency, and power density of the magnetic components and heatsink being the objectives of interest. Firstly, the essential data of the components are collected from the easily accessible database of the redistributors. The data includes the cost per commercial off-the-shelf (COTS) component, conduction resistance of the transistors and rectifier diodes ($R_{\mathrm{ds(on)}}$ and $R_{\mathrm{D(on)}}$), switching loss of the transistor ($E_{\mathrm{on/off}}$), the capacitive charge of the rectifier diodes (Q_{c}), weight and volume of the magnetic cores (M_{c} and V_{c}). It is worth mentioning that the data needs to cover various current and voltage ratings to compare topologies using different component requirements. Secondly, the correlation of cost versus the performance indexes of the components such as $R_{\mathrm{ds(on)}}$, $E_{\mathrm{on/off}}$, $R_{\mathrm{D(on)}}$, Q_{c}, M_{c} and V_{c} are established by proccessing the data with curve-fitting methods. Different from the physical properties based cost models used in [22–24], the correlations directly connect the cost information to the performance indexes of the components based on the open and accessible data, without having a model in between. Therefore, these correlations are more straightforward to implement. With the obtained correlations, a collection of the possible designs by sweeping through a range of $R_{\mathrm{ds(on)}}$, $E_{\mathrm{on/off}}$, $R_{\mathrm{D(on)}}$, Q_{c}, M_{c} and V_{c} can be made. In this way, the designs are not limited by certain components choices and the correlations can be directly utilized by other designers without a components database. The normalized cost of the possible designs, including the cost of semiconductors, magnetic components, gate drivers, heatsinks, and PCB boards, can be calculated, as well as the power density of the magnetic components and heatsinks. Additionally, the average

efficiency performance can be calculated based on the components chosen using the analytical models of the converters. As a result, a design space is formed based on the possible designs. Finally, the advantageous converter design can be selected.

The contribution of this chapter is as follows:

1. The design guideline of three re-configurable structure PSFB converters that are well-suited for the wide voltage range public EV charging application is elaborated. Among the three re-configurable structure PSFB converters, the t-PSFB converter that utilize two auxiliary switches with a three-winding transformer is a new PSFB converter topology that is first introduced in this chapter.

2. A multi-objective converter design process that considers the normalized cost, power density of the magnetic components and heatsinks, and the average efficiency performance is introduced. The accessible components data from the well-known re-distributors is collected and processed to uncover the correlation between the cost and the performance factors of the components.

3. The multi-objective design and performance benchmark of the 11kW t/r/i-PSFB converter and conventional PSFB converter for the wide output voltage range (250-1000V) EV charging application is presented. This design benchmark is particularly important, because it identifies the i-PSFB and r-PSFB converters as the outstanding solutions for the future EV market.

5.2. OPERATION PRINCIPLES OF THE RE-CONFIGURABLE PSFB CONVERTERS

5.2.1. THE CONVENTIONAL PSFB CONVERTER

The conventional PSFB converter, as shown in Figure 5.1(a), consists of an H-bridge inverter, a high-frequency isolation transformer with an equivalent leakage inductance L_σ referred to the primary-side and a diode-bridge rectifier on the secondary side, and a second-order low-pass output passive filter consisting of L_{out} and C_{out}. Note that the diode-bridge rectifier are sometimes replaced by a synchronous rectifier using unipolar transistors to reduce conduction losses. The optional lossless turn-off snubber capacitors C_{snb} at the full-bridge are for reducing turn-off switching losses (but it will narrow the ZVS turn-on range), and a voltage clamping RCD snubber circuit is used at the secondary-side between the terminal C and D for limiting the voltage spikes on the secondary side diodes [25].

The PSFB converter is typically controlled with fixed switching frequency by phase-shift modulation where the two half-bridge legs are operated with 50% duty cycle, as shown in the typical waveform depicted in Figure 5.1(a). The phase-shift angle Φ refers to the asynchronization between the operation of the two half-bridge legs. When Φ is null, the diagonal pair of transistors (S_{11} & S_{22}, or S_{12} & S_{21}) turn on and off synchronously, making the primary side voltage v_{AB} alternate between $+V_{\text{in}}$ and $-V_{\text{in}}$, which is equivalent to a bipolar modulation of the H-bridge inverter. When the Φ is non-null, the synchronization is broken, and the parallel pair of transistors (S_{11} & S_{21}, S_{12} & S_{22}) are able to be kept turned on at the same time, creating a third circuit state that is $v_{\text{AB}} = 0V$,

leading to a controllable unipolar modulation action. Due to the impressed i_p caused by L_σ and inverter bridge capacitance, the switching transition in each half-bridge leg creates a lowered di_p/dt and dv_{AB}/dt on the primary side, making the ZVS turn-on possible and lowering the turn-off losses of the transistors. A complete description of the operation of a PSFB converter can be found in [26].

5.2.2. THE R-PSFB CONVERTER WITH RE-CONFIGURABLE SECONDARY SIDE

Figure 5.1(b) shows the schematic of the r-PSFB converter [12]. Three-winding transformer is used, with the turns ratio of $n_r : 1 : 1$. The primary side is identical to that of the conventional PSFB converter. Each of the secondary sides is connected to a diode-bridge rectifier, an output filter (L_{out} and C_{out}), and an RCD snubber circuitry. Three auxiliary switches $S_{aux,1,2,3}$ connect the two secondary sides and enable two different configurations according to their switching states. The auxiliary switches can be implemented by either mechanical switches or semiconductor transistors.

The re-configuration of the r-PSFB converter operates as follows. When $S_{aux,1}$ is kept on and $S_{aux,2,3}$ are kept off, the two diode rectifiers are connected in series, making V_{out} twice the individual diode rectifier output voltage. When $S_{aux,2,3}$ are kept on and $S_{aux,1}$ is kept off, the two diode rectifiers are connected in parallel. As a result, V_{out} equals the individual diode rectifier output voltage, but the output current is shared by the two rectifiers.

5.2.3. THE T-PSFB CONVERTER WITH RE-CONFIGURABLE SECONDARY SIDE

Figure 5.1(c) shows the schematic of the t-PSFB converter. A three-winding transformer is used, which has one primary and two secondary windings, with the turns ratio of $n_t : 1 : 1$. The primary side is identical to that of the conventional PSFB converter. The additional secondary winding and auxiliary switches ($S_{aux1,2}$) allow the secondary side to be configured into a regular full-bridge diode rectifier or a center-tapped diode rectifier.

The re-configuration of the t-PSFB converter operates as follows. When S_{aux1} is kept off and S_{aux2} is kept on, the two secondary windings are in series, and the t-PSFB works the same as a conventional PSFB converter with full-bridge diode rectifier. When S_{aux1} is kept on and S_{aux2} is kept off, the secondary side is configured into a center-tapped rectifier. This is shown in Figure 5.1(c).

5.2.4. THE I-PSFB CONVERTER WITH HYBRID DIODE RECTIFIERS

Figure 5.1(d) shows the schematic of the i-PSFB converter. Two H-bridge inverters fed by V_{in} are connected in parallel on the primary side, and they can be interleaved. A hybrid three-legs diode rectifier is connected to the two H-bridge inverters by two transformers with the turns ratio of $n_i : 1$. Note that instead of parallel connecting the H-bridge inverters as shown in Figure 5.1(d), these could be alternatively connected in series, for instance, when connected to a bipolar dc grid.

The interleaving of the i-PSFB converter operates as follows. The two H-bridge inverters operate the same as that of the conventional PSFB converter, with an interleaving phase shift ϕ between them. When $\phi = 0$, the upper-side transformer secondary side voltage V_{sec1} is in phase with the lower-side V_{sec2}, resulting in the series connection of the two transformers' secondary windings. In this series connection mode, the

first and third diode bridge-legs ($D_{11,12}$ & $D_{31,32}$) process all the current, and rectify the sum of V_{sec1} and V_{sec2}, while the second diode bridge-leg ($D_{21,22}$) is placed in off-state. When $\phi = \pi$, V_{sec1} and V_{sec2} are in reverse polarity, resulting in the parallel connection of the two transformer's secondary windings, which is facilitated by the added diode bridge-leg as shown in Figure 5.1(d). In this parallel connection mode, the first and third diode bridge legs are in parallel and share the inductor impressed current equally, while the second diode bridge leg processes the whole inductor current. Therefore, for even power loss balance in the rectifying stage, the diodes $D_{21,22}$ could be assembled with the hard paralleling of two diodes of the same technology used in the bridge legs containing $D_{11,12}$ and $D_{31,32}$.

5.3. CIRCUIT LEVEL COMPARISON AMONG CONVENTIONAL PSFB, R-PSFB, T-PSFB AND I-PSFB CONVERTERS

Table 5.1: The equivalent parameters of the t,r,i-PSFB converters

conv-PSFB	t-PSFB		r-PSFB		i-PSFB	
	series	parallel	series	parallel	series	parallel
n_{eff}	$n/2$	n	$n/2$	n	$n/2$	n
$L_{out(eff)}$	L_{out}	L_{out}	$2L_{out}$	$L_{out}/2$	L_{out}	L_{out}
$C_{out(eff)}$	C_{out}	C_{out}	$C_{out}/2$	$2C_{out}$	C_{out}	C_{out}
$i_{D(eff)}$	i_D	i_D	i_D	$2i_D$	i_D	i_D
$i_{s(eff)}$	i_s	i_s	i_s	$2i_s$	i_s	i_s
$i_{SW(eff)}$	i_{SW}	i_{SW}	i_{SW}	i_{SW}	$i_{SW}/2$	$i_{SW}/2$

A general comparison of the components used among the conventional PSFB, r-PSFB, and i-PSFB converters are conducted. The comparison parameters include the component count and the voltage and current stresses of the components. With these parameters, the cost and losses can be calculated for these converters for a primary evaluation.

5.3.1. TRANSFORMER TURNS RATIOS n

The transformer's turns ratio n of the conventional PSFB converter can be determined with:

$$n = kV_{in(min)} / V_{out(max)} \tag{5.1}$$

where k is a tuning factor used to compensate for the voltage drop across the circuit components and also to give a margin for the feedback control dynamics. Practically, k is typically set between k= 0.85 .. 0.95.

For the t-PSFB, r-PSFB, and i-PSFB converters, the transformer's turns ratios ($n_{t,r,i}$) are doubled compared to n, since the secondary sides of these converters can operate in modes where the two secondary windings are connected in series.

5.3.2. OUTPUT FILTER L_{OUT} AND C_{OUT}

The output filter L_{out} and C_{out} can be determined by a maximum allowed current and voltage ripple stress across the converter.

OUTPUT INDUCTANCE L_{OUT}

For the conventional PSFB converter, the peak-to-peak output current ripple $I_{out,ripple}$ across L_{out} in the continuous conduction mode (CCM) operation can be calculated by:

$$I_{out,ripple} = \frac{V_{in} D(1-D)}{2nL_{out} f_{sw}} \tag{5.2}$$

The maximum output inductor ripple ($I_{out,ripple(max)}$) happens when $D = 0.5$ and $V_{in} = V_{in(max)}$. Thus, $L_{out(min)}$ could be calculated as:

$$L_{out} \geq L_{out(min)} = \frac{V_{in(max)}}{8nI_{out,ripple(max)} f_{sw}} \tag{5.3}$$

For the t-PSFB converter, the minimum output inductance $L_{out(min),t}$ equals the $L_{out(min)}$ calculated in Equation (5.3), in order to satisfy the current ripple requirement in both the full-bridge and center-tapped modes. $I_{out,ripple(max)}$ for the t-PSFB converter happens when it is in the full-bridge mode, $D = 0.5$, and $V_{in} = V_{in(max)}$. When the t-PSFB converter is in the center-tapped mode, the worst-case current ripple equals $0.5I_{out,ripple(max)}$.

For the r-PSFB converter, the minimum output inductance $L_{out(min),r}$ equals the $L_{out(min)}$ calculated in Equation (5.3), in order to satisfy the current ripple requirement in both the series and parallel connection modes. $I_{out,ripple(max)}$ happens when the r-PSFB is in the parallel connection mode, and in the series connection mode, the worst-case output current ripple is only $0.5I_{out,ripple(max)}$.

For the i-PSFB converter, the minimum output inductance $L_{out(min),i}$ equals the $L_{out(min)}$ calculated in Equation (5.3), in order to satisfy the current ripple requirement in both the series and parallel connection modes. Therefore, the worst case current ripple in the series connection mode is $I_{out,ripple(max)}$, while in the parallel connection mode is $0.5I_{out,ripple(max)}$.

OUTPUT CAPACITANCE C_{OUT}

For the conventional PSFB converter, the peak-to-peak output voltage ripple $V_{out,ripple}$ on C_{out} in CCM can be determined by:

$$V_{out,ripple} = \frac{I_{out,ripple}}{16 f_{sw} C_{out}} \tag{5.4}$$

The maximum voltage ripple ($V_{out,ripple(max)}$) happens at $I_{out,ripple(max)}$. Thus, $C_{out(min)}$ can be calculated as:

$$C_{out} \geq C_{out(min)} = \frac{I_{out,ripple(max)}}{16 f_{sw} V_{out,ripple(max)}} \tag{5.5}$$

For the t-PSFB converter, the minimum output capacitance value equals $C_{out(min)}$ calculated in Equation (5.5). $V_{out,ripple(max)}$ for the t-PSFB converter happens when the converter is in the full bridge mode, and the worst voltage ripple that can happen in the

center-tapped mode is $0.5V_{\text{out,ripple(max)}}$. For the r-PSFB converter, the minimum output capacitance value equals $C_{\text{out(min)}}$ calculated in Equation (5.5). $V_{\text{out,ripple(max)}}$ for the r-PSFB converter happens when it is in the series connection mode, and in the parallel connection mode, the worst voltage ripple is $0.5V_{\text{out,ripple(max)}}$. For the i-PSFB converter, the minimum output capacitance value equals $C_{\text{out(min)}}$ calculated in Equation (5.5).

These information are summarized in Table 5.2.

5.3.3. VOLTAGE STRESS OF C_{OUT} AND CURRENT STRESS OF L_{OUT}

The voltage stress of C_{out} is the same for the conventional PSFB, t-PSFB, and i-PSFB converters, as the output capacitor in these converters needs to withstand the full output voltage V_{out}. However, for the r-PSFB converter, each of the output capacitors only needs to block $0.5V_{\text{out}}$.

The current stress of L_{out} depends on how the voltage, current, and power rating of the converter is set. Figure 5.2 shows the operation range of the converter. If the power rating is equal to or higher than P_1, which allows the maximum output current value to be reached in the series connection mode, i.e., $P_1 = \frac{1}{2}V_{\text{out(max)}}I_{\text{out(max)}}$, then, the current stresses on L_{out} is identical for all four converters, because in the series connection mode all of the inductors of the four converters need to conduct the whole output current i_s plus the current ripple. If the power rating is smaller than P_2, which means the maximum output current that can be reached during the series connection mode is $0.5I_{\text{out(max)}}$ (i.e., $P_2 = \frac{1}{2}V_{\text{out(max)}}\frac{1}{2}I_{\text{out(max)}}$), then the current stresses on the inductors of r-PSFB converter will be half of the other PSFB converter or even less. This information is summarized in Table 5.2.

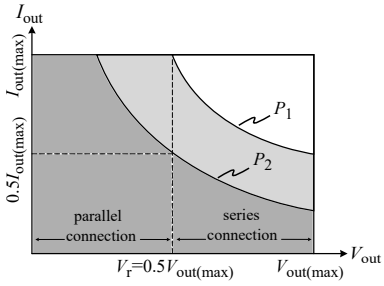


Figure 5.2: Operation range of the converters and the power limitation

5.3.4. VOLTAGE STRESS OF THE RCD SNUBBER CIRCUITRY

Due to the resonance between L_σ and the parasitic capacitance from the transformer and rectifier diodes, a voltage ringing will happen on the secondary side diodes, with a peak voltage value that could reach twice the nominal value of the secondary winding voltage [25] [12]. This can be critical for the safe operation of the rectifier diodes, and it is particularly critical for the voltage class (V_{class}) requirement of the fast-recovery diodes. Therefore, the RCD voltage clamp snubber circuitry is designed to limit the blocking voltage ringing to a reasonable value, V_{cp}, so that a safe operation for the rectifier diodes is ensured, e.g., $V_{\text{cp}} \leq 0.85V_{\text{class}}$.

Table 5.2: The summary of the components requirements for the four studied PSFB converters

	items	conv-PSFB	t-PSFB	r-PSFB	i-PSFB
transformer	turns ratio rated to n	1	2	2	2
output filter	L_{out} count	1	1	2×1	1
	C_{out} count	1	1	2×1	1
	V_{stress} of C_{out} rated to V_{out}	1	1	0.5	1
	I_{stress} of L_{out} rated to i_s	1	1	0.5 - 1	1
RCD	V_{stress} of D, C_{RCD} rated to V_{cp}	1	1	0.5	1
D_{rec}	V_{stress} of D_{rec} rated to V_{sec}	1	1	0.5	1

Table 5.3: The worst-case current stresses of the 11kW, 30A converters

	conv-PSFB	t-PSFB	r-PSFB	i-PSFB
$I_{p,rms}$ [A]	48.9	36.1	34.3	18
$I_{sw,rms}$ [A]	34.6	25.5	24.3	12.8
$I_{D,rms}$ [A]	21.1	21.2	14.8	21.2
$I_{D,avg}$ [A]	15	15	10.5	15

The voltage stress of the D_{RCD} and C_{RCD} equals to V_{cp} for the conventional PSFB converter, which could reach $2V_{sec}$ if no clamp snubber circuit is used. For the t-PSFB and i-PSFB converters, the voltage stress of the D_{RCD} and C_{RCD} equals to V_{cp} as well, since its series connection mode is equivalent to the conventional PSFB converter. For the r-PSFB converter, the RCD circuitry only needs to block half of the voltage compared to the conventional PSFB converter. However, the trade-off is that it has two sets of RCD circuitry. This information is summarized in Table 5.2. The sizing of the resistance value and the power loss calculation of the RCD snubber follows the methodology explained in [12].

5.3.5. VOLTAGE AND CURRENT STRESSES OF THE RECTIFIER DIODES AND TRANSISTORS

The voltage class of the rectifier diode of the PSFB converter needs to be paired with the V_{cp} of the RCD circuitry. Therefore, for the r-PSFB converter, the voltage class of the rectifier diode is halved compared to the other analyzed PSFB converters. This information is summarized in Table 5.2.

After designing the transformer turns ratio and output filter as introduced in the previous subsections A and B, the steady-state current stresses of the rectifier diodes and transistors of the t,r,i-PSFB, and the conventional PSFB converter can be calculated using the steady-state analytical model of the PSFB converter introduced in [12] together

with the equivalent parameters of the t,r,i-PSFB converters shown in Table 5.1. Considering an 11kW power rating, 30A maximum output current, 640-840V input voltage, and 250-1000V output voltage range, the current stresses are summarized in Table 5.3. As it can be seen from Table 5.3, the worst-case $I_{\mathrm{p/sw,rms}}$ of the t-PSFB and r-PSFB is lower than that of the conv-PSFB converter, and those of the i-PSFB converter is approximately half of those of the t-PSFB and r-PSFB. This is because the re-configuration ability of the t/r/i-PSFB converter can reduce the current stresses to the minimum half of those of the conv-PSFB converter if the power rating is chosen to be P_2 shown in Figure 5.2. However, since the chosen power rating of the benchmark study is 11kW, it lays between P_2 and P_1. Thus, the current stress of t/r/i-PSFB converter is lower than the conv-PSFB but not as low as half, as in the case shown in Table 5.3.

5.4. KEY COMPONENTS DATA COLLECTION AND PROCESSING

In order to better evaluate the performance of the PSFB converters with different circuit component requirements, data of the necessary components are obtained from the website of the well-known re-distributors, and they are further processed using a python script to obtain the correlation among the parameters regarding efficiency performance, power density, and cost as shown in Figure 5.3. Using this approach, it is no longer necessary to extract the essential data from the datasheets of components, which is highly time-consuming. And since this method is purely based on data analysis and interpretation, physical models for cost estimation is not required. Other designers can incorporate the method to process their own components database, or they can directly use the numerical coefficients presented in this paper for a primary estimation in their design stage.

The unit price per piece from the re-distributors' website is used as the cost data of the components. This data is valuable for two reasons. Firstly, it is the most accessible price data. Mass production price information is usually only available from company quote or specific supply-chain. Thus, it is hard to access especially for the academic researchers and engineers in small-scale companies. Each company will also have different mass production price based on the size of the enterprise and their negotiation power. However, for prototyping or small-scale production, the price information provided online by these re-distributors is extremely valuable for the primary estimation of the cost. Secondly, the normalized price calculated based on the price per piece is similar to the one calculated using the price for large purchase quantities. To demonstrate this idea, the price information of 12 SiC MOSFETs in the package of TO-247 from three different manufacturers, GeneSiC, Infineon, and Wolfspeed are collected from the website of the re-distributor Digikey. The part number and the price information are shown in Table 5.4, where price_1 stands for the unit price if the purchase quantity is 1, price_{1000} means the unit price if buying 1000 pieces, etc. Plotting the unit price of different purchase quantities in Figure 5.4, one can see that the unit price for larger purchase quantities drops considerably. However, instead of the exact price, this paper emphasis on predicting the normalized cost of design, i.e., how much cheaper or more expensive is one certain converter design compared to the others. By calculating the pu value of the prices for different purchase quantities, Figure 5.5 shows that the normalized cost calculated using different purchase quantities remains similar. Thus, the easy-to-access

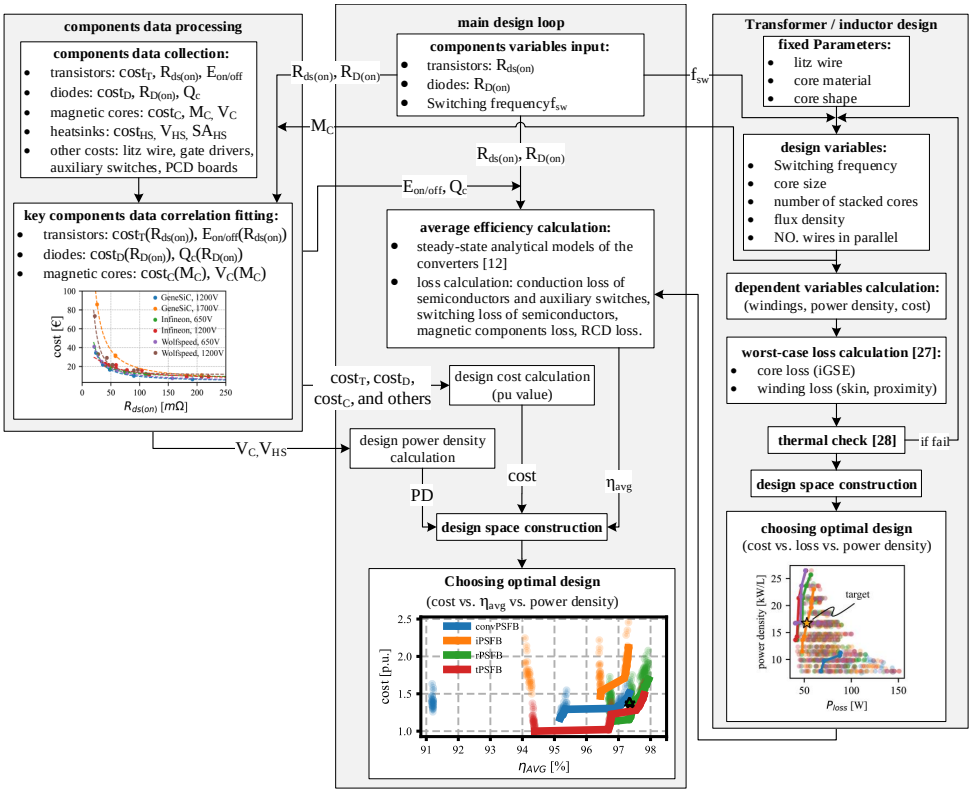


Figure 5.3: The multi-objective design process of the converters

unit price information from the well-known re-distributors enables the estimation of the relative price of the converter designs, which is insightful for the academic researchers and small-scale company engineers to make design decisions. Moreover, this price information can still be used with a scaling factor by the companies to predict the mass production price.

5.4.1. ACTIVE SEMICONDUCTORS

For SiC MOSFETs, the on-state (static) losses can be determined by their on-resistance R_{dson} and the switching (or dynamic) losses can be modelled by the accumulative energy dissipated during the on/off switching transition ($E_{\text{on/off}}$). Their cost data can be collected directly on the website of their re-distributors, e.g., Digikey website. In this work, only semiconductor devices employing TO-247 packaging are considered in the analysis. Several SiC MOSFET manufacturers are evaluated, and a statistic curve-fitting method is used to model the important parameters for the calculation of the selected design performance metrics.

Figure 5.6 shows the correlation between the R_{dson} and cost of the transistors with three voltage class devices, and Table 5.5 shows the curve-fitting numerical parameters

Table 5.4: Price of SiC MOSFETs for different purchase quantities collected on 3rd, Jan, 2023.

part_num	mfr	$R_{ds(on)}$ [mΩ]	$price_1$ []	$price_{10}$ []	$price_{100}$ []	$price_{500}$ []	$price_{1000}$ []
G3R350MT12D	GeneSiC	420.0	4.80	4.261	3.7815	3.47872	3.35618
G3R160MT12D	GeneSiC	192.0	6.61	5.921	5.3067	4.91578	4.75678
G3R75MT12D	GeneSiC	90.0	10.64	9.580	8.6284	8.01880	7.77066
G3R40MT12D	GeneSiC	48.0	17.64	16.102	14.7000	13.79436	NaN
IMW120R220M1H	Infineon	286.0	9.98	9.019	7.4672	6.50228	5.66326
IMW120R090M1H	Infineon	117.0	12.42	11.414	9.6395	8.57498	7.86534
IMZ120R060M1H	Infineon	78.0	17.37	15.969	13.4866	11.99730	NaN
IMW120R040M1H	Infineon	54.4	22.50	20.682	17.4668	15.53798	NaN
C3M0160120D	Wolfspeed	208.0	9.65	8.709	7.2106	6.27890	5.46872
C3M0075120D	Wolfspeed	90.0	17.09	15.711	13.2688	11.80356	NaN
C3M0032120D	Wolfspeed	43.0	31.42	28.979	24.7468	NaN	NaN
C3M0021120D	Wolfspeed	28.8	35.62	33.229	28.8516	NaN	NaN

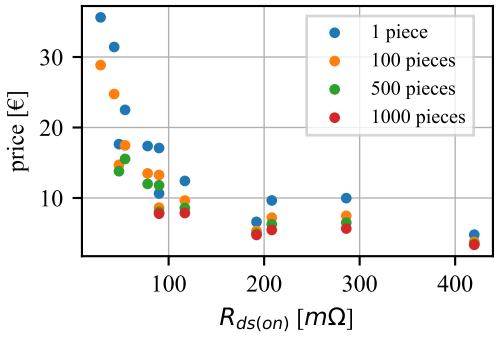


Figure 5.4: The unit price of the SiC MOSFETs in Euros. Data collected on 3rd, Jan, 2023.

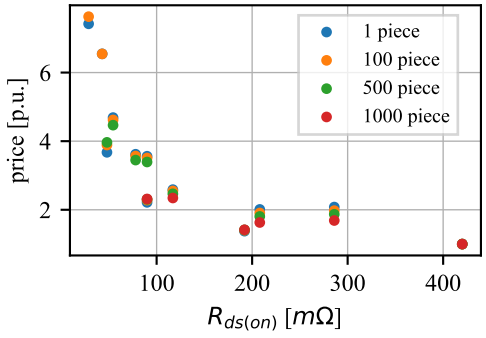


Figure 5.5: The unit price of the SiC MOSFETs in pu values. Data collected on 3rd, Jan, 2023.

of the plotted logarithmic equation. It can be seen that with the same R_{dson}, the SiC MOSFETs with higher voltage ratings generally cost more. At low R_{dson}, the cost difference between the 1700V, 1200V, and 650V classes is more significant. This may imply that circuits designed for a given target efficiency that employ 1700V semiconductors could have higher costs than the ones employing 1200V or 650V devices, but one should be careful because the total cost of a power electronic converter is highly dependent on the circuit topology selection and the complexity of the circuit. It is interesting to note that there are fewer options for the 1700V semiconductor market when compared to the 650V and 1200V classes. This indicates that topologies using 1700V SiC transistors will be more prone to supply chain problems.

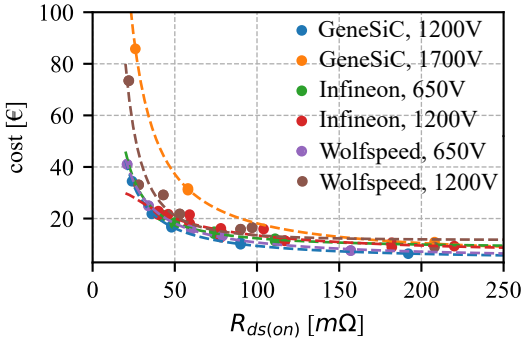


Figure 5.6: SiC MOSFET price and $R_{\text{ds(on)}}$ trend, depending on the device voltage ratings. The plotted dots are the data of a commercially available device acquired from the Digikey website on 2022-02-22, containing SiC MOSFET from 'GeneSiC', 'Infineon', 'Wolfspeed'. The device package is limited to TO-247. The dashed lines are the obtained curve-fitting correlations, whose method and coefficients are shown in Table 5.5.

Table 5.5: Curve fitting method and coefficients for the relation between price and R_{dson} of the SiC MOSFETs, depending on the manufacturers and voltage ratings. Data only include those with $R_{\text{ds(on)}} < 300 m\Omega$.

fitting method	$\text{cost}_T = a \cdot (1/R_{\text{ds(on)}})^2 + b \cdot (1/R_{\text{ds(on)}}) + c$					
Mfr	Infineon	Infineon	GeneSiC	GeneSiC	Wolfspeed	Wolfspeed
V_{rating} [V]	650	1200	1200	1700	650	1200
a	7.91e+03	-8.33e+03	4.71e+03	2.53e+04	2.15e+03	2.99e+04
b	3.66e+02	9.08e+02	5.44e+02	1.15e+03	6.78e+02	-1.34e+02
c	7.89e+00	5.21e+00	3.47e+00	4.10e+00	3.72e+00	1.19e+01

The correlation between switching losses $E_{\text{on/off}}$ and R_{dson} of several commercially available 1200V SiC MOSFETs from Wolfspeed is given in Figure 5.7. Herein, the data considers the device datasheet information: $E_{\text{on/off}}$ at 800V, 30A, 25°C of junction temperature, 5Ω external gate resistance, and a 15V/-5V gate driving voltage. Table 5.6 shows the numerical coefficients of the curve-fitting first-order linear equation.

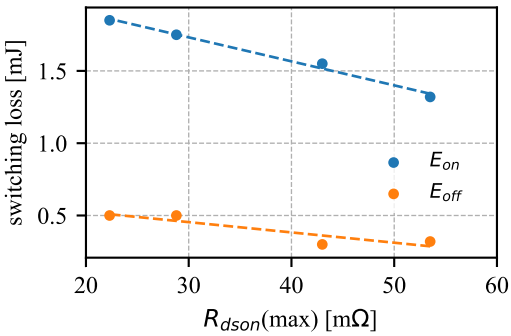


Figure 5.7: SiC MOSFET $E_{on/off}$ and $R_{ds(on)}$ trend. The dots are the data acquired from the datasheets of 1200V SiC MOSFET from 'Wolfspeed', the condition is at 800V, 30A, 25°C of junction temperature, 5Ω gate resistance, and 15V/-5V gate driving voltage. The package is limited to TO-247. The dashed lines are the curve-fitting correlations, whose method and coefficients are shown in Table 5.6.

Table 5.6: Curve fitting method and coefficients for the relation between $E_{on/off}$ and R_{dson} of the 1200V SiC MOSFETs. Data includes those from 'Wolfspeed'.

fitting method	$E_{on/off} = a \cdot R_{dson} + b$	
parameter	E_{on}	E_{off}
a	-1.66e-02	-7.11e-03
b	2.23e+00	6.67e-01

Table 5.7: Curve fitting method and coefficients for the relation between price and R_{Don} of the SiC diodes, depending on the manufacturers and voltage ratings.

fitting method	$\text{cost}_{\text{D}} = a \cdot (1/R_{\text{D(on)}})^2 + b \cdot (1/R_{\text{D(on)}}) + c$				
Mfr	Infineon	Infineon	GeneSiC	GeneSiC	Wolfspeed
V_{rating} [V]	650	1200	1200	1700	1200
a	-4.34e+02	-2.72e+02	-4.98e+03	1.11e+02	-6.17e+03
b	2.47e+02	2.97e+02	7.48e+02	5.29e+02	6.78e+02
c	3.23e+00	2.55e+00	-3.96e+00	2.30e+00	5.61e+00

It is worth mentioning that the data collected from the datasheet is under the specific conditions of 800V and 30A. Therefore, the $E_{\text{on/off}}$ for other operating points can be scaled proportionally based on the actual blocking voltage and switching current, as shown in Equation (5.6).

$$E_{\text{on/off}}(t) = \frac{V_{\text{block}}(t)}{800V} \cdot \frac{I_{\text{sw}}(t)}{30A} E_{\text{on/off(fit)}} \tag{5.6}$$

5.4.2. SiC RECTIFIER DIODES

Discrete TO-247 SiC diodes from various manufacturers from 650V to 1700V are compared using the information provided on their datasheets. The conduction loss of the diodes is typically calculated by Equation (5.7), where R_{Don} and V_{D} are the on resistance and forward voltage drop. The R_{Don} is taken from the on-state IV-curve of the device by the difference in voltage drop for two reference current values, e.g., one at half-rated current and another at full-rated current. V_{D} is the voltage drop value taken when the device conducts only a tiny fraction of the rated current.

$$P_{\text{D}} = I_{\text{D,rms}}^2 \cdot R_{\text{Don}} + I_{\text{D,avg}} \cdot V_{\text{D}} \tag{5.7}$$

Figure 5.8 and table 5.7 shows the correlation between price and R_{Don} of the rectifer diodes, grouped by the device voltage class. Note that since the SiC diodes benchmarked are of the same technology, their equivalent constant voltage drop V_{D} are similar and closely independent of the chip die area (or rated current of the device). Therefore, the R_{Don} parameter has a more logical relationship with the chip die size (or current ratings) and thus relates better with the device cost.

The switching loss of the diodes is typically calculated by Equation (5.8), where Q_{c} is the capacitive charge of the diodes, and V_{r} is the reverse blocking voltage of the diode. Figure 5.9 show the correlation between the R_{Don} and Q_{c}.

$$P_{\text{D(sw)}} = 0.5 \cdot Q_{\text{c}} \cdot V_{\text{r}} \cdot f_{\text{sw}} \tag{5.8}$$

5.4.3. MAGNETIC CORE MATERIAL AND LITZ WIRE

Magnetic components account for a significant part of the cost, loss, and power density of a power electronic converter. The magnetic core loss is generally calculated by

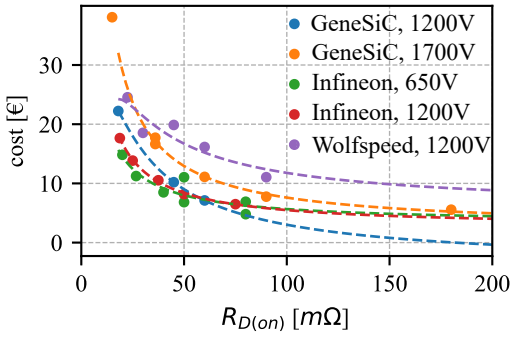


Figure 5.8: SiC rectifier diode price and R_{Don} trend. The dots are the data aquired from Digikey on 2022-02-22, containing SiC diodes from 'GeneSiC', 'Infineon' IDW series, and 'Wolfspeed'. The package is limited to TO-247. The dashed lines are the curve fitting trends of the SiC rectifier diodes, whose method and coefficients are shown in Table 5.7.

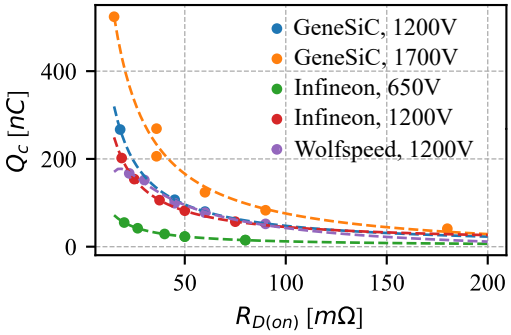


Figure 5.9: SiC rectifier diode Q_c and R_{Don} trend. The dots contain SiC diodes from 'GeneSiC', 'Infineon' IDW series, and 'Wolfspeed'. The package is limited to TO-247. The dashed lines are the curve fitting trends of the SiC rectifier diodes, whose method and coefficients are shown in Table 5.8.

Table 5.8: Curve fitting method and coefficients for the relation between Q_c and R_{Don} of the SiC diodes, depending on the manufacturers and voltage ratings.

fitting method	$Q_c = a \cdot (1/R_{D(on)})^2 + b \cdot (1/R_{D(on)}) + c$				
Mfr	Infineon	Infineon	GeneSiC	GeneSiC	Wolfspeed
V_{rating} [V]	650	1200	1200	1700	1200
a	-1.19e+03	-1.52e+03	-1.54e+03	-2.38e+04	-6.40e+04
b	1.14e+03	3.72e+03	4.92e+03	9.75e+03	7.17e+03
c	8.33e-01	7.90e+00	-1.57e+00	-1.95e+01	-2.27e+01

iGSE for non-sinusoidal excitation, which requires the Steinmetz coefficients measured for sinusoidal excitation that need to be curve-fitted based on the datasheet figures. The cost of the magnetic cores for various core shapes can be obtained through suppliers' websites, such as Digikey, and the trend of the core cost and core mass is shown in Figure 5.10. It can be seen that the core cost has a linear correlation with the amount of core material used. Table 5.9 shows the curve-fitting coefficients of the magnetic cores.

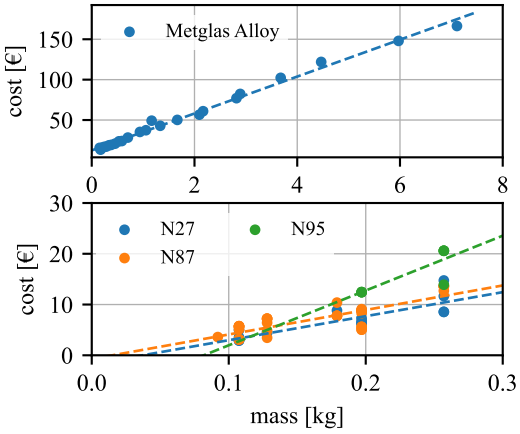


Figure 5.10: Magnetic core trend. The dots are the data aquired from Digikey on 2022-02-21, containing E shaped cores for the ferrite material N27, N87, N95, and U shaped AMCC cores for Metglas Alloy material.

Table 5.9: Curve fitting method and coefficients of the magnetic cores

fitting method	$\text{cost}_\text{C} = a \cdot \text{M}_\text{C} + b$			
material	Metglas Alloy	N27	N87	N95
a	22.85	47.31	48.29	107.97
b	12.39	-1.76	-0.73	-8.83

For the Litz wire used in the magnetic components, 5.38 Euro per kilogram is used to estimate the cost of it based on the amount of copper used. The weight of the copper can be calculated based on the number of turns and the mean-length-per-turn of the design.

5.4.4. FILM CAPACITORS

Film capacitors are usually used for the DC link capacitors of a power electronic converter. The data of the cost, volume, and ESR of the film capacitors are obtained and plotted in Figure 5.11. It can be seen that, with the same capacitance value, the film capacitors with 1300V voltage rating is usually around twice as expensive than the 650V ones, and the volume around three times larger. The ESR of the capacitors with different

voltage ratings does not have significant difference, but it is related to the capacitance value. Table 5.10 shows the curve-fitting coefficients of the film capacitors..

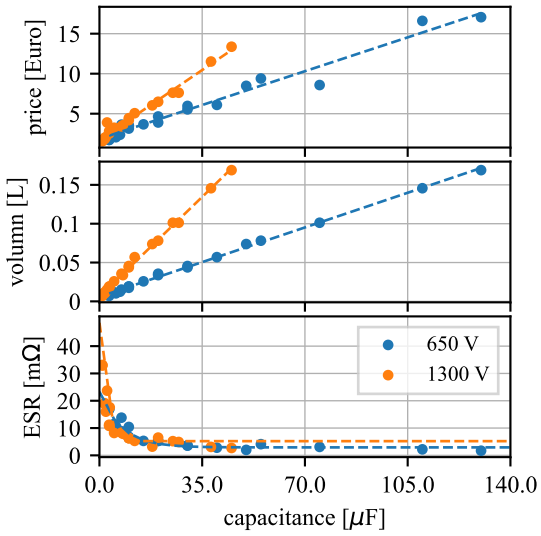


Figure 5.11: Film capacitor price, volume, and ESR trend. The dots are the data aquired from Digikey on 2022-02-22, containing C4AQ series capacitors from 'KEMET'. The dashed lines are the curve fitting trends of the film capacitors, whose method and coefficients are shown in Table 5.10

Table 5.10: Curve fitting method and coefficients of the film capacitor

fitting method	$\text{price} = a_1 \cdot \text{capacitance} + b_1$ $\text{volumn} = a_2 \cdot \text{capacitance} + b_2$ $\text{ESR} = a_3 \cdot e^{(-b_3 \cdot \text{capacitance})} + c$	
voltage rating [V]	650	1300
a_1	1.21E-1	2.50E-1
b_1	1.86	1.72
a_2	1.28E-3	3.67E-3
b_2	5.89E-3	6.14E-3
a_3	20.37	43.34
b_3	1.36E-1	5.09E-1
c	2.92	5.21

Figure 5.11 shows the properties trends for 650V and 1300V C4AQ series DC-link capacitor from KEMET. It illustrate how the price, volume and ESR of the 650V and 1300V DC-link capacitor change with different capacitance value. The data is collected from

Digikey, and the price is prone to change. As shown in fig. 5.11, the price of the 1300V capacitors are generally more expensive than the 650V ones with the same capacitance value, but not twice as expensive. The volume of the 1300V capacitors is more than twice larger than the 650V ones. The ESR does not show apparent correlation with the voltage rating.

Therefore, while the conventional PSFB, t-PSFB, and i-PSFB converters have the same C_{out} properties, the two output capacitors of the r-PSFB converter together are slightly more expensive, but less in volume compared to them.

5.4.5. HEATSINK

The heatsink is necessary for the thermal management of the semiconductors used in the studied PSFB converters. Therefore, it size will be mostly defined by the critical point in which the system can be placed into operation where the semiconductor losses are maximum. Independently on the performance of the heatsink, its minimal size will be defined by the sum of surface area required to accommodate each used TO-247 packaged device. The thermal resistance of the heatsink depends on the material used, available surface area, airflow, and equivalent pressure drop. For simplicity of comparison, only the aluminum heatsinks that are rectangular in shape with the same fin height and arrangement from the same manufacturer HS marston are considered. Table 5.11 shows the details of the chosen heatsinks. Due to the excellent performance of the selected heatsinks, the needed surface area for placing the semiconductors of each studied circuit topology defines their required size.

Table 5.11: The details of the heatsinks considered for the four converters. The price information is collected from Farnell on 2022/10/24.

topology	heatsink	SA[m^2]	volume[L]	cost[]
conv/t-PSFB	890SP-01000-A-100	0.010	0.325	50.87
r-PSFB	890SP-01500-A-100	0.015	0.488	67.87
i-PSFB	890SP-02000-A-100	0.020	0.650	79.70

5.4.6. GATE DRIVER, RELAY AND PCB

The high-side gate driver ISO5852 is considered in the benchmark study. The price per unit is 7. For the conv/t/r-PSFB converter, four gate drivers are required. And for the i-PSFB converter, eight are required. For the digital controller, the Texas Instruments TMS320F28379D is considered. The price is 27. The relays used in the r/t-PSFB converter is chosen to be the T9GV1L14-5, which is a 30A power relay with a unit price of 7.4 and a conduction resistance of about 10mΩ. These prices are based on the data from mouser/Farnell website acquired on 2022/10/24.

The price of the PCB board depends mainly on the number of conductive layers and the size of the board. Assuming that 1m^2 of the standard 4 layers 1 ounce copper PCB is used, and that the size of the PCB equals the size of the heatsink, the price of the single PCB boards for the four converters are estimated to be 8.5 for the conv/t-PSFB, 13.1

for the r-PSFB and 17.4 for the i-PSFB. This price was obtained from the manufacturer Eurocircuits on 2022/10/24.

5.5. MULTI-OBJECTIVE DESIGN OF THE CONVERTERS

To benchmark the four studied PSFB topologies in the EV battery charging application, a multi-objective design process is performed in all circuits while considering an 11kW power rating, 30A maximum output current, 640-840V input voltage, and 250-1000V output voltage range. For the EV charging application where the converter operates in a wide output voltage range and mostly in full-power/current, the averaged full-power/current efficiency η_{AVG} is used as the indicator of the system efficiency performance instead of the efficiency value for a single operational point. η_{AVG} is the average value of the steady-state efficiencies of a certain number of sampling operational points. These sampling operational points starts from the minimum output voltage and maximum output current to the maximum output voltage and maximum power, with a constant output voltage increment between two neighboring points. In this chapter, eight points are considered for the calculation. The first point is when $V_{\text{out}} = 300V$ and $I_{\text{out}} = 30A$, the second is $V_{\text{out}} = 400V$ and $P = 11kW$, the third is $V_{\text{out}} = 500V$ and $P = 11kW$, etc., and the final point is when $V_{\text{out}} = 1000V$ and $P = 11kW$. The objectives of interest are the average efficiency performance, power density of the magentic components and heatsinks, and normalized cost. Figure 5.3 shows the flowchart of the multi-objective design process.

The first step of the multi-objective design process is to design the magnetic components of the converters. Since the switching frequency f_{sw} of the converter has a significant impact on the design of the magnetic components, the magnetic components are designed for f_{sw} from 15kHz to 105kHz, and assuming the worst case scenario in terms of losses. The design spaces of the magnetic components will be formed for each of the converters, with the loss, power density, and cost being the figure of merit. Then, based on the design spaces, some advantageous transformer and inductor designs will be selected for further converter design.

The second step is to sweep through a range of $R_{\text{ds(on)}}$ and $R_{\text{D(on)}}$. Using the components correlation derived and the analytical models of the converters, the total cost and the average efficiency of the converter designs can be calculated. The calculated total costs can be further processed to obtain the normalized costs by taking the minimum value of the cost as 1. By using the normalized costs, the designs with the cost advantage can be identified, while the error of cost estimation brought by the changing market price can be reduced at the same time. As a result, the design spaces for the converters can be formed, and the advantageous converter topology and component designs can be chosen.

5.5.1. MAGNETIC COMPONENTS DESIGNS

The design of the magnetic components follows the process illustrated in Figure 5.3. In order to avoid overly large number of solutions, the Litz wire considered in the design is set to be AWG 41 and 600 strands, the core material for the transformer is the ferrite N87, for the inductor is the Metglas Amorphous Cut Core, and the core shape for the transformer is the EE cores, and for the inductor are the UU cores. Five design variables

are considered for finding the optimal design, they are the switching frequency, the core size, number of stacked cores, flux density, and the number of litz wires that can be put in parallel. The number of stacked cores can change from 1 to 8 for transformer design, and 1 to 5 for inductor design. The allowed flux density is from 10% to 80% of the B_{sat} of the core material. The number of litz wires that can be paralleled can be 1 or 2 for the ease of winding assembling. The worst-case scenarios for the designs of the magnetic components happen when the winding currents are the maximum, which results in the most losses. For the transformer design, the worst-case scenario for conv-PSFB converter is when $V_{\text{in}} = 840V$, $I_{\text{out}} = 30A$, $V_{\text{out}} = 366V$, and for the t/r/i-PSFB converter is when $V_{\text{in}} = 840V$, $I_{\text{out}} = 22A$, $V_{\text{out}} = 500V$. For the inductor design, the worst-case scenario for r-PSFB converter is when $V_{\text{in}} = 840V$, $I_{\text{out}} = 22A$, $V_{\text{out}} = 366V$, and for the conv/t/i-PSFB converter is when $V_{\text{in}} = 840V$, $I_{\text{out}} = 30A$, $V_{\text{out}} = 366V$. The loss calculation is conducted using the method from [27]. Combining the total losses P_{mag} (W) and surface area A_{mag} (m^2) of the magnetic components, the temperature rise ΔT is estimated based on Equation (5.9) [28].

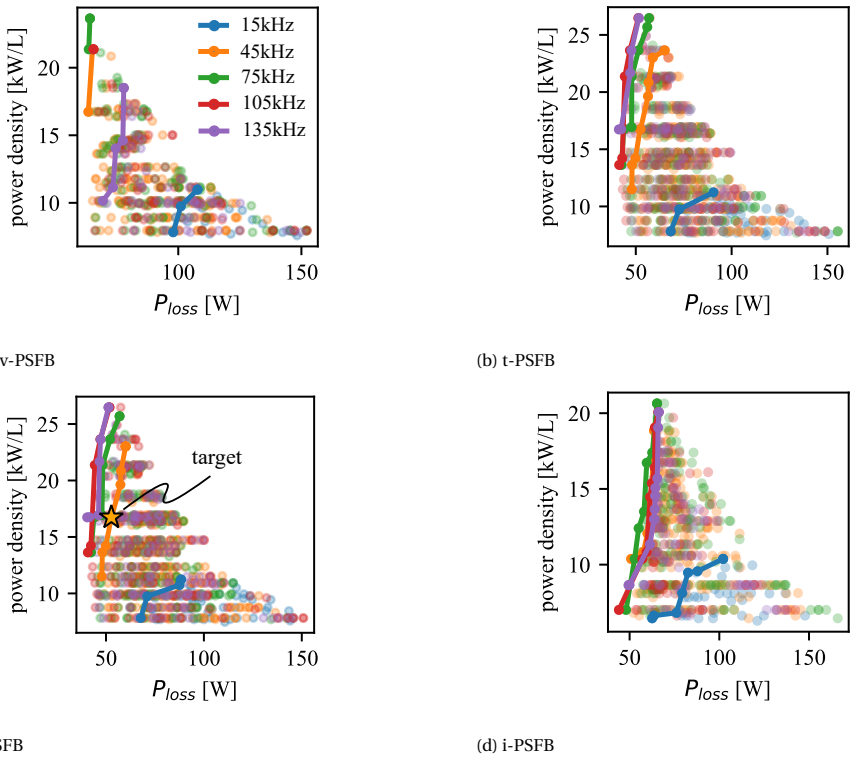
5

$$\Delta T = \left(\frac{P_{\text{mag}}}{10 \cdot A_{\text{mag}}}\right)^{0.833} \tag{5.9}$$

This temperature rise estimation equation is obtained by lumping the winding losses together with the core losses and assume that the thermal energy is dissipated uniformly throughout the surface area of the core and winding assembly at all ambient temperatures. This assumption is effective, because the majority of the transformer's surface area is ferrite core area rather than winding area, and the thermal conductivity of ferrite (around 40 mW/cm/°C) is poor at any temperature. And since the transformer uses several pairs of ferrite core stack together, the magnetic cores are carefully fix together so that the airgap is uniformed in the whole transformer. In this way, the magnetic flux and thus core loss can be more evenly distributed among the cores, which helps avoid creating hotspot. Moreover, the windings are tightly winded on the bobbin, and the gaps among the wires are kept as uniformly as possible, so that the winding losses are also distributed evenly in the winding area.

Figure 5.12 shows the worst-case transformer loss P_{loss} and the power density values of the transformer designs for all four topologies, with the switching frequency changing from 15kHz to 135kHz. It can be seen that by increasing f_{sw} from 15kHz to 75kHz, P_{loss} decreases and power density increases for all of the topologies. However, there is no apparent improvement on P_{loss} and power density anymore when f_{sw} further increase above 75kHz.

The underlining reason is that, by increasing f_{sw}, less number of turns is needed for the transformer to operate with the desired value of magnetic flux density B. As a result, a smaller winding area, which naturally means a smaller core shape, is needed to make a transformer with a higher f_{sw}. The reduced winding length and core size further contribute to the reduction of core loss. However, there is a limit to how small the transformer can become with the increase of f_{sw}, which is mostly regulated by the thermal management performance of the component. One can argue that a smaller flux density B should be used for the transformer with higher f_{sw} so that the loss-per-volume of the core does not result in overheating. Unfortunately, a smaller flux density can only



(a) conv-PSFB

(b) t-PSFB

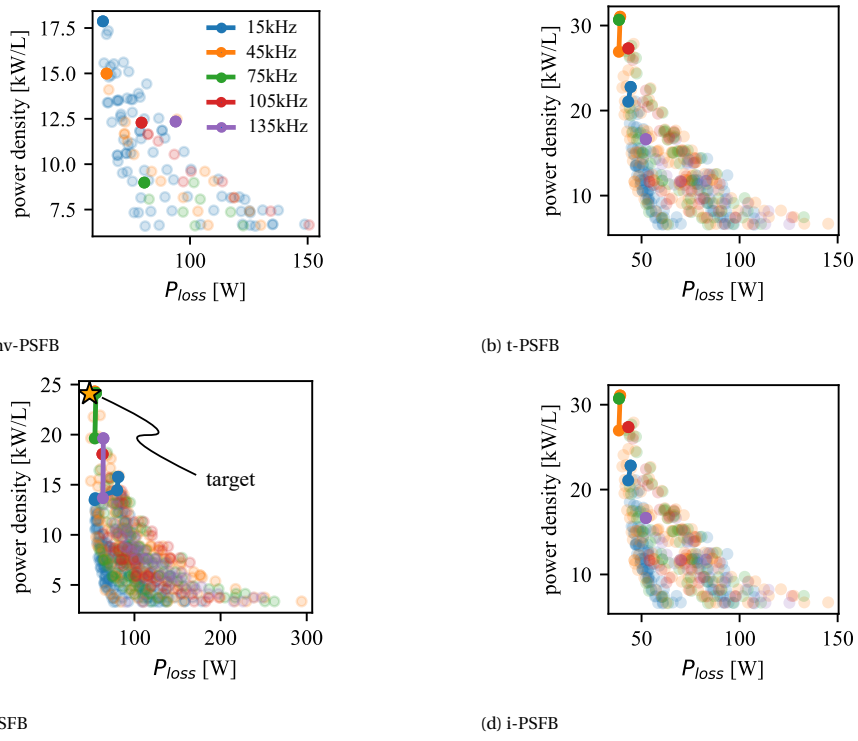
(c) r-PSFB

(d) i-PSFB

Figure 5.12: The transformer designs for the four PSFB topologies at f_{sw} = 15, 45, 75, 105, 135kHz. The design constrains are: target transformer leakage inductance L_σ=10μH (referred to the primary side), N87 as core material, winding layer arrangement is limited to first primary, then secondary 1 and secondary 2 side-by-side, calculated temperature rising limited to 80°C.

be achieved with an increased number of turns, which, again, calls for a larger winding area, as well as a larger core size. In summary, there is an optimal f_{sw}, with which the transformer design yields the advantageous P_{loss} and power density without having an over-heating problem. From Figure 5.12, it is clear that the optimal f_{sw} for the transformer designs is around 75kHz.

Based on the results shown in Figure 5.12, three advantageous transformer designs that have the highest power density and lowest power losses at f_{sw} of 15kHz, 45kHz, and 75kHz are collected for each one of the PSFB topologies. Table 5.12 shows the chosen transformer designs. It can be seen from Figure 5.12 and Table 5.12 that the transformer designs of the t-PSFB and r-PSFB is able to have lower power losses when compared to the conv-PSFB and i-PSFB. This is because the winding current stresses of these two topologies are less, as can be seen from Table 5.3. And despite having two transformers, The total cost of the transformers of the i-PSFB converter can be even cheaper than the other three PSFB converters in 15kHz and 45kHz. However, due to the added winding volume of the two transformers, the total power density of the transformers are slightly



(a) conv-PSFB

(b) t-PSFB

(c) r-PSFB

(d) i-PSFB

Figure 5.13: The inductor designs for the four PSFB topologies at f_{sw} = 15, 45, 75, 105, 135kHz. The design constrains are: Metglas as core material, maximum temperature rising lower than 80°C. Note that here f_{sw} is defined as the MOSFET switching frequency, therefore in any of the studied PSFB the equivalent frequency seeing by the inductor will be twice f_{sw}.

lower than the other three options.

Table 5.12: Detailed information of the transformer designs that are chosen for the multi-objective design process. The P_{loss}, Power Density (PD), and cost are calculated for all the transformers.

topology	f_{sw} [kHz]	P_{loss} [W]	PD [kW/L]	cost []	ΔT [°C]	shape [E core]	N_{core}	$N_{w,prim}$	$N_{w,sec}$	N_{prim}	N_{sec}	B_{op} [T]
convPSFB	15.0	107.8	11.0	123.4	78.4	E 70/33/32	5	2	2	12	19	0.248
convPSFB	45.0	65.2	21.4	66.3	73.0	E 56/24/19	8	2	2	5	8	0.248
convPSFB	75.0	64.1	23.6	58.2	78.8	E 56/24/19	7	2	2	5	9	0.155
tPSFB	15.0	90.5	11.2	122.5	69.2	E 70/33/32	5	2	1	12	10	0.248
tPSFB	45.0	56.4	19.6	56.4	72.5	E 65/32/27	3	2	2	10	8	0.217
tPSFB	75.0	52.6	21.7	49.2	77.7	E 70/33/32	2	2	2	8	7	0.186
rPSFB	15.0	88.3	11.2	122.5	67.8	E 70/33/32	5	2	1	12	10	0.248
rPSFB	45.0	57.4	19.6	56.4	73.5	E 65/32/27	3	2	2	10	8	0.217
rPSFB	75.0	53.2	21.7	49.2	78.6	E 70/33/32	2	2	2	8	7	0.186
iPSFB	15.0	102.1	10.4	99.1	72.9	E 70/33/32	2	1	1	31	25	0.248
iPSFB	45.0	71.7	18.7	40.9	76.3	E 55/28/21	2	1	2	22	18	0.217
iPSFB	75.0	65.3	20.6	50.1	74.8	E 56/24/19	3	1	2	10	9	0.186

Table 5.13: Detailed information of the inductor designs that are chosen for the multi-objective design process. The P_{loss}, Power Density (PD), and cost are calculated for all the inductors.

topology	f_{sw} [kHz]	P_{loss} [W]	PD [kW/L]	cost []	ΔT [°C]	shape [U core]	N_{core}	$N_{w,prim}$	N_{prim}	B_{op} [T]
convPSFB	15.0	63.0	17.9	86.6	79.7	U AMCC-25	4	2	42	0.936
convPSFB	45.0	64.5	15.0	99.5	67.5	U AMCC-40	4	2	21	0.468
convPSFB	75.0	80.6	9.0	136.5	60.0	U AMCC-80	4	2	14	0.312
tPSFB	15.0	44.4	22.8	65.0	70.8	U AMCC-25	3	2	42	1.248
tPSFB	45.0	39.1	31.0	43.1	79.1	U AMCC-25	2	2	29	0.936
tPSFB	75.0	38.5	30.7	43.0	78.1	U AMCC-25	2	2	27	0.624
rPSFB	15.0	53.8	13.5	87.7	54.4	U AMCC-25	2	2	49	1.248
rPSFB	45.0	48.0	24.1	44.1	70.8	U AMCC-25	1	2	45	0.936
rPSFB	75.0	55.2	24.2	43.6	79.6	U AMCC-25	1	2	34	0.780
iPSFB	15.0	44.4	22.8	65.0	70.8	U AMCC-25	3	2	42	1.248
iPSFB	45.0	39.1	31.1	43.1	79.1	U AMCC-25	2	2	29	0.936
iPSFB	75.0	38.5	30.7	43.0	78.1	U AMCC-25	2	2	27	0.624

Figure 5.13 shows the worst-case loss and power density values of the inductor designs for all four PSFB topologies, with the f_{sw} in the range from 15kHz to 135kHz. Note that here f_{sw} is defined as the MOSFET switching frequency, therefore in any of the studied PSFB, the equivalent frequency seen by the inductor will be twice f_{sw}. It can be seen that, similar to the transformer design, the inductor designs have their optimal f_{sw} for achieving the optimal loss and power density values. The conv-PSFB converter has the best inductor design at f_{sw} = 15kHz, and with higher f_{sw}, the loss increases and power density decreases. For the t/r/i-PSFB converters, the optimal inductor designs occurs around f_{sw} = 45kHz. This is because the inductor of the conv-PSFB converter suffers from higher dB/dt stress compared to the other re-configurable structure PSFB converters despite the current stresses on the inductors for the conv/t/i-PSFB are the same. This results in increased core loss on the inductor according the iGSE equation [27].

Table 5.13 shows the selected inductor designs that have the optimal loss and power density values for f_{sw} of 15kHz, 45kHz, and 75kHz for all topologies. It can be seen based on Figure 5.13 and Table 5.13 that the inductor designs of the conv-PSFB converter performs worse in terms of power losses, due to the high dB/dt stress explained before. In comparison, the t-PSFB and i-PSFB have similar inductor designs that are the most advantageous in terms of power losses, power density, and cost. For the r-PSFB converter, the total power density of the two inductors is less, and the total power losses are higher than that of the t-PSFB and i-PSFB. This is reasonable since the chosen power rating of 11kW and output current limitation of 30A makes the r-PSFB design right in between P_1 and P_2 in Figure 5.2. This makes the wors-case current stress on each the inductors of the r-PSFB converter to be less than that of the conv/t/i-PSFB converter, but also more than half of it. Therefore, the two inductors of the r-PSFB together has higher losses in the worst case, and lower power density.

5.5.2. MULTI-OBJECTIVE DESIGN RESULTS

With the magnetic components at different f_{sw} designed, the performance of these converters in different f_{sw} can be benchmarked. A range of $R_{ds(on)}$ and $R_{D(on)}$ are swept

through. And based on the cost and performance correlations of the key components and information about miscellaneous parts obtained in Section 5.4, the relative cost and losses of every design can be estimated for the different choice of components. Then combined with the magnetic components and the RCD snubber circuit, the system efficiency performance can be estimated using the analytical models of the converters. The detailed analytical model of the PSFB type converter used in this chapter is presented in [12].

Figure 5.14 shows η_{AVG} and the relative cost of all the possible designs. First of all, it can be seen from Figures 5.14a and 5.14b that by increasing the switching frequency, the cost will drop, and the power density of the magnetics will increase. However, η_{AVG} will also drop. This trade-off mainly comes from the reduction of magnetic components material and the increase of switching loss of the semiconductors when increasing f_{sw}. At 15kHz, the optimal design can be obtained from the t-PSFB converter. When f_{sw} increases to 45kHz, the designs of the r-PSFB converter start to be competitive since the power density increases and cost reduces consideraly while η_{AVG} suffers less reduction compared to the other topologies. When f_{sw} further increases to 75kHz, the gain on the power density increase and cost saving is limited, while η_{AVG} drops significantly for the conv/t/i-PSFB converters.

Secondly, in terms of the power density of the magnetic components and heatsinks and normalized price of the converters, the t-PSFB converter is able to deliver the lowest cost and highest power density designs from 15kHz to 75kHz. Even thought the conv-PSFB has the same components count as the t-PSFB, the current stress of the transformer and the dV/dt stress of the inductor of the t-PSFB is less than that of the conv-PSFB due to the feature of re-configuration. This factor benefits the t-PSFB converter to have more power efficient, smaller, and cheaper designs of magnetic components. The i-PSFB converter is the most expensive one due to the high component account. The r-PSFB converter which has 8 rectifier diodes with 1200V voltage ratings is slightly more expensive than the t-PSFB which has 4 rectifier diodes with 1700V voltage rating. This corresponds to the trend shown in Figure 5.6 that the cost of the 1200V rectifier diodes are less expensive than the 1700V ones with the same $R_{D(on)}$, but not less than half.

Thirdly, in terms of η_{AVG}, the i-PSFB and r-PSFB topology is able to provide the η_{AVG}-advantageous designs in 15kHz. The conv-PSFB generally has lower η_{AVG}, especially when f_{sw} increases. To better interpret the η_{AVG} performance of these converters, two designs of each converter topology that have the highest η_{AVG} and lowest normalized cost in 15kHz and 45kHz are selected for further analysis. The detailed information about these designs are summarized in Table 5.14, and the breakdown of the averaged losses of these designs are illustrated in Figure 5.15.

From Figure 5.15 it can be seen that the averaged conduction loss and switching loss on the transistors of the t/r/i-PSFB designs are less than that of the conventional PSFB design. This is due to the re-configuration ability, the t/r/i-PSFB topologies are able to have less current stress on the transistors in the low output voltage operation. This point is also revealed in the worst-case current stresses listed in Table 5.3. It is an interesting observation that the i-PSFB converter has the lowest transistor losses. The first reason is that the i-PSFB converter has shared current stresses on the two full-bridges, which potentially lowers the total conduction loss according to the resistive loss calculation

Table 5.14: Detailed information of the efficiency and cost advantageous designs based on Figure 5.14. PD_T is the power density of the transformers, PD_L is the power density of the inductors, PD is the power density of the magentic components together with the heatsinks.

topology	f_{sw}[kHz]	η_{AVG}[%]	cost[pu]	transistor[mΩ]	rec diode[mΩ]	PD_T[kW/L]	PD_L	PD
conv-PSFB	15	97.33	1.51	Infineon,30	GeneSiC, 30	11.0	17.9	5.67
conv-PSFB	45	95.38	1.38	Infineon, 30	GeneSiC, 30	21.4	15.0	7.00
t-PSFB	15	97.80	1.48	Infineon, 30	GeneSiC, 30	11.2	22.8	6.15
t-PSFB	45	96.78	1.22	Infineon, 30	GeneSiC, 30	19.6	31.0	8.86
r-PSFB	15	97.72	1.69	Infineon, 30	Infineon, 30	11.2	13.5	4.81
r-PSFB	45	97.24	1.36	Infineon, 30	Infineon, 30	19.6	24.1	7.31
i-PSFB	15	97.31	2.11	Infineon, 30	GeneSiC, 30	10.4	22.8	5.02
i-PSFB	45	96.45	1.53	GeneSiC, 50	GeneSiC, 40	18.7	31.1	6.91

$P_{\text{Ohmic}} = I^2R$. The second reason is that the use of transistors with relatively high $R_{ds(on)}$ brings less switching losses, as shown in Figure 5.7. The r-PSFB converter designs have higher losses on the rectifier diodes. This is mainly due to the doubled amount of diodes on the conduction path, and the current is shared only during the parallel-connection configuration when V_{out} is low. The i-PSFB converter designs have the highest transformer losses even though the current is shared between the two transformers. The main reason is that the dB/dt stress on the transformers are not shared. In terms of inductor losses, the r-PSFB converter performs better than the other three converter. By having two secondary sides, the dB/dt stress on the two inductors of the r-PSFB converter are halved in the series connection operation due to the voltage sharing, which helps reducing the averaged inductor core losses. The most significant difference in losses lays in the snubber circuitry loss $P_{RCD(avg)}$. The r-PSFB converter has significantly less $P_{RCD(avg)}$ compared to the others, while the conv-PSFB suffers the highest $P_{RCD(avg)}$. This can be explained by the equations used for calculating the resistance value and the power loss of the RCD snubber circuitry, whose details can be found in [25] [12]. Due to the split secondary sides, not only high resistance value can be used for the RCD snubber circuits of the r-PSFB converter, the voltage stress on the R_{RCD} is also much less compared to the other topology. In practical implementation, this splitting structure of r-PSFB topology also brings benefit of loss sharing on the two RCD circuitries, which means simpler thermal design as well.

Based on these observations of the multi-objective design results, the t-PSFB converter operating at 15kHz and the r-PSFB converter at 45kHz with the right choices of semiconductor components stands out as the most advantageous converter designs in terms of the normalized cost, power density of magnetics and heatsinks, and η_{AVG} performance.

5.6. EXPERIMENTAL VERIFICATION

In order to verify the multi-objective design prediction, a close-to-Pareto-front 45kHz r-PSFB prototype converter is built based on the multi-objective optimization design process described previously. Due to the availability issue of the components in today's

market, the prototype converter has to be built with some adjustments on the selection of components. The ferrite core shape used for the transformer design changes from the intended EE65/32/27 from Table 5.12 to the EE70/33/32, since the prior was out of stock in our trusted suppliers. The MOSFETs and rectifier diodes used in the prototype are IMW120R030M1H and IDW30G120C5B from Infineon, which were immediately available in the laboratory of the authors. The inductors are designed according to the optimal inductor design in Table 5.13. Table 5.15 shows the detail parameters and components used for the prototype converter. As a result, the target design is marked as the star shown in Figure 5.14, which is close to the obtained Pareto front of the design space.

Table 5.15: Specifications of the prototype

input voltage [V]	640-840
output voltage [V]	250-1000
power rating [kW]	11
f_{sw} [kHz]	45
MAX output current [A]	30
transistor	IMW120R030M1H
rectifier diode	IDW30G120C5B
transformer core material	N87
transformer core shape	3xEE70/33/32
transformer N_{prim}: N_{sec}	8:7
inductor design	refer to Table 5.13
gate driver	ISO5852
DSP controller	TMS320F28379D

Figure 5.16 shows the picture of the 45kHz r-PSFB prototype converter. The prototype converter has a power density of 2.68kW/L. Figures 5.17 and 5.18 show the operational waveform of the prototype in parallel and series connection mode with different V_{out} and I_{out}. Figure 5.19 shows the waveform of the RCD clamping circuitry of the r-PSFB prototype. It can be seen that the prototype converter is able to operate in an extensive output voltage range from 250V to 1000V with different output current conditions, and the voltage clamping circuitry functions well.

In order to verify the efficiency performance of the 45kHz r-PSFB prototype converter, the full-power/current efficiency is tested and plotted together with the estimated efficiency in Figure 5.20. Additionally, the estimated efficiency of the optimal conv-PSFB converter design at 45kHz as listed in Table 5.14 is also plotted for comparison. It can be seen that the test efficiency of the r-PSFB prototype matches well with the estimation. The peak efficiency achieved is 97.76%. The tested average full power/current efficiency is 97.25%, which is very close to the estimated value of 97.27%. The error in loss prediction is mainly due to the simplification of both analytical models for the conduction and switching losses of the semiconductors. The actual cost and average efficiency of

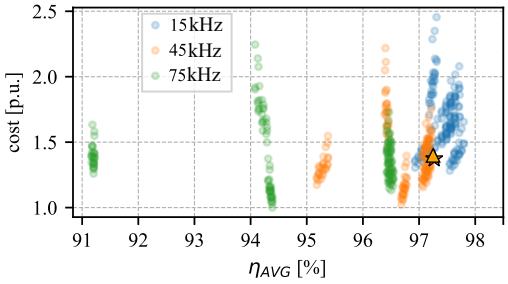
the prototype are plotted in Figure 5.14 as the triangle, and it can be seen that the prototype implementation is very close to the target. The efficiency of the r-PSFB converter drops as V_{out} decreases from 1000V to 500V, due to the increasing phase shift angle and associated circulating losses. However, when V_{out} decreases further below 500V, the r-PSFB converter re-configures from series connection to parallel connection, resetting the phase shift angle and bringing up the efficiency. In comparison, the efficiency of the 45kHz optimal conv-PSFB design drops constantly as V_{out} decreases. This demonstrate the efficiency benefit of the re-configurable structure PSFB converters.

Table 5.16: Detailed information of the target r-PSFB design and the achieved r-PSFB prototype design from Figure 5.14

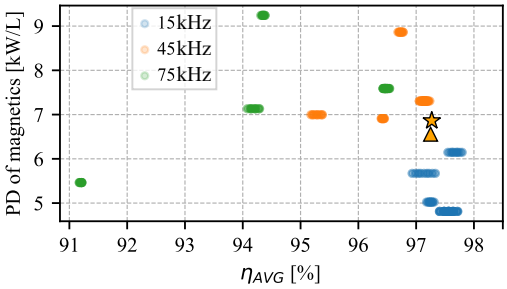
	f_{sw}[kHz]	η_{avg} [%]	cost [p.u.]	Magnetics&heatsink PD
target	45	97.27	1.37	6.86 [kW/L]
prototype	45	97.25	1.40	6.56 [kW/L]

5.7. CONCLUSION

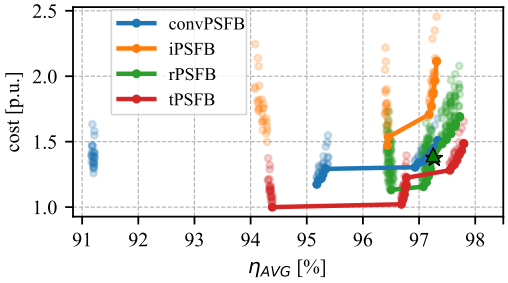
In this chapter, three re-configurable structure PSFB converters are analyzed and benchmarked for the extended wide voltage range public EV charging application. A multi-objective converter design process that considers the normalized cost, power density of the magnetic components and heatsinks, and the average efficiency performance is introduced. In this proposed design process, well-accessible data provided by the components re-distributors are utilized to establish the correlations between the cost and loss performance of the components, which are used in the design process to determine the most advantageous converter in terms of the cost, power density of the magnetics and heatsink, and the averaged efficiency. Based on the resulted design space of the converters, A close-to-Pareto-front 45kHz r-PSFB prototype converter is built to verify the analysis, and the actual cost, power density of the magnetics and heatsink, and averaged efficiency match with the design well. This proves the feasibility of proposed multi-objective design and benchmark process, and identify the t-PSFB and r-PSFB converters to be the outstanding solutions in the wide voltage range public EV charging application.



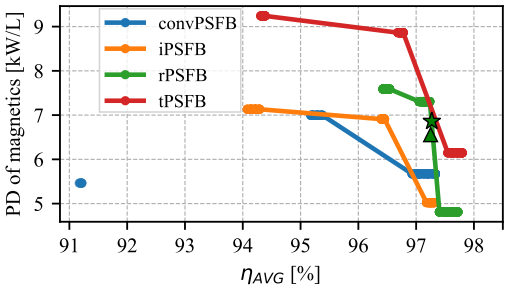
(a) cost (p.u. value) versus η_{AVG}, group by f_{sw}



(b) power density of the magnetic components and heatsink versus η_{AVG}, group by f_{sw}



(c) cost (p.u. value) versus η_{AVG}, group by topologies



(d) power density of the magnetic components and heatsink versus η_{AVG}, group by topologies

Figure 5.14: The averaged full-power/current efficiency (η_{AVG}), the cost, and the power density of the magnetic components and heatsink of the possible designs of all four PSFB topologies. The target design and the actual prototype design are marked as the star and triangle respectively.

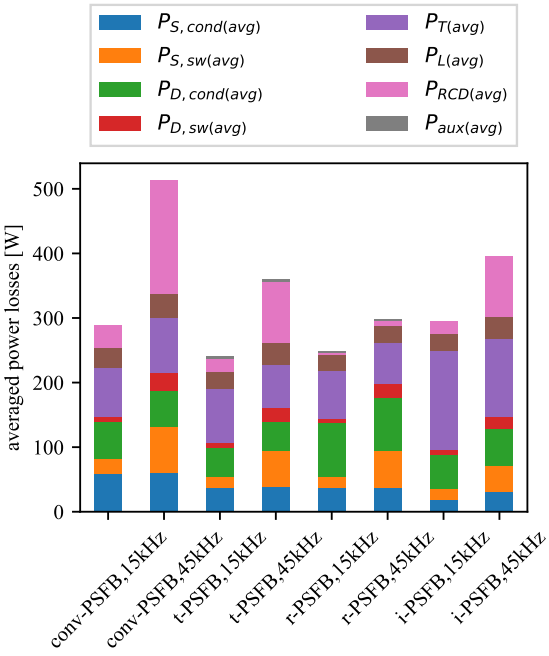


Figure 5.15: The breakdown of the averaged losses of the advantageous designs from Figure 5.14. $P_{S,cond(avg)}$ and $P_{D,cond(avg)}$ are the averaged conduction loss on the transistors and rectifier diodes, $P_{S,sw(avg)}$ and $P_{D,sw(avg)}$ are the averaged switching loss on the transistors and rectifier diodes, $P_{T(avg)}$ and $P_{L(avg)}$ are the averaged transformer losses and inductor losses, $P_{RCD(avg)}$ is the averaged RCD snubber circuitry loss, $P_{aux(avg)}$ is the averaged auxiliary switch conduction losses.

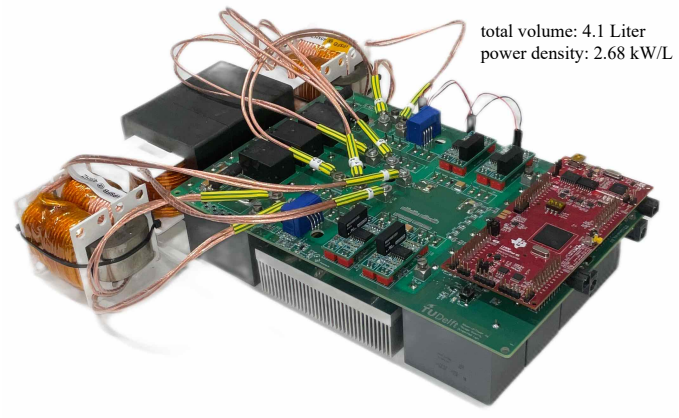
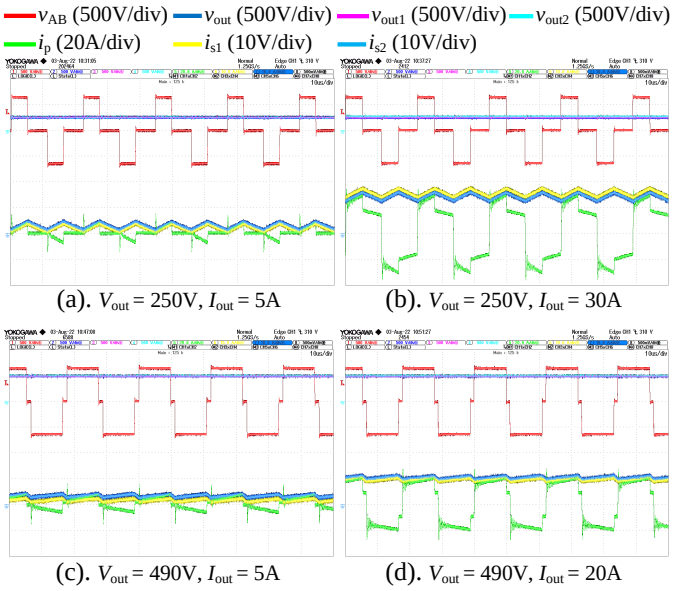


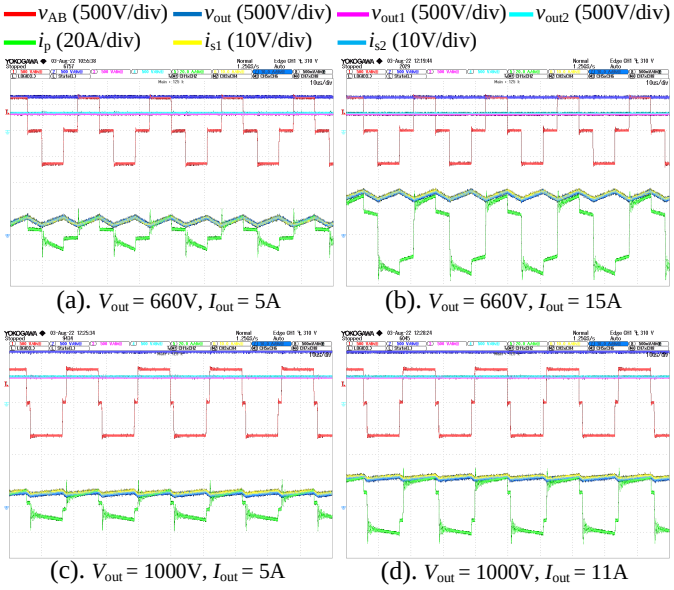
Figure 5.16: Prototype of the 45kHz r-PSFB converter



(a). V_{out} = 250V, I_{out} = 5A (b). V_{out} = 250V, I_{out} = 30A

(c). V_{out} = 490V, I_{out} = 5A (d). V_{out} = 490V, I_{out} = 20A

Figure 5.17: The operational waveform of the r-PSFB converter in parallel connection mode, with V_{in}=640V. $v_{out1/2}$ and $i_{s1/2}$ are the output voltage and current of the two secondary side rectifiers, measured after the RCD circuitry and on the output inductors, respectively.



(a). V_{out} = 660V, I_{out} = 5A (b). V_{out} = 660V, I_{out} = 15A

(c). V_{out} = 1000V, I_{out} = 5A (d). V_{out} = 1000V, I_{out} = 11A

Figure 5.18: The operational waveform of the r-PSFB converter in series connection mode, with V_{in}=640V.

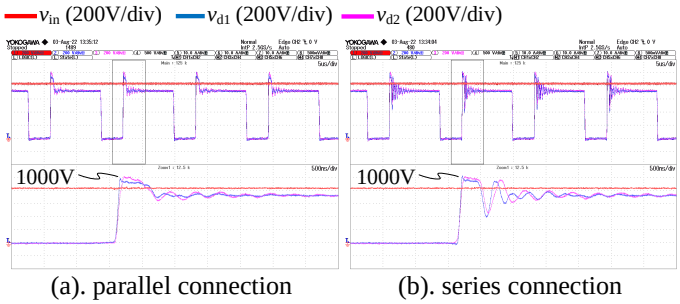


Figure 5.19: The voltage clamping waveform of the RCD snubber circuitry, with V_{in}=840V. $v_{d1,2}$ are the diode voltage of the two secondary sides.

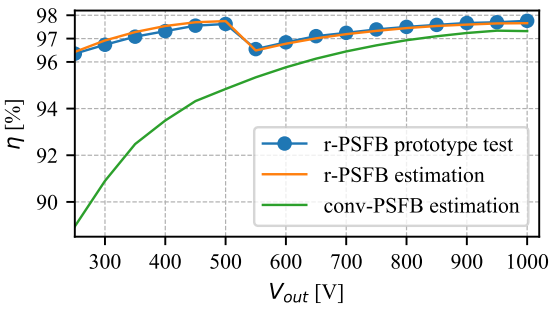


Figure 5.20: The estimated efficiency of the 45kHz r-PSFB and conv-PSFB converter designs and the test efficiency of the 45kHz r-PSFB prototype converter with full power or maximum output current, V_{in}=640V.

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6

BEYOND CONVERTER: BATTERY CHARGING STRATEGIES AND CHARGING SYSTEM

This chapter investigates the influences of different charging strategies on the performance of the Electric Vehicle (EV) charging system. A summary of the possible EV charging system structures and their pros and cons are also presented. Firstly, different types of EV charging strategies are explained. Herein, the characteristics, the influences on the EV battery, and the respective requirements for the hardware and communication of the BMS and power electronic converter are summarized. Secondly, a simulation case study is conducted to investigate the influences of two charging strategies on the performance of a typical power electronic converters employed as a back-end converter of a fast EV charger. A modular 50kW DC-DC EV charger constructed with five parallel-connected 10kW Phase-Shift Full-Bridge (PSFB) DC-DC converters is modeled with two different charging strategies, and two comparison metrics are proposed for a benchmark: the charging-cycle efficiency and the installation utilization rate. The results show that these two comparison metrics are influenced by the charging strategies of the EV.[1]

[1] This chapter is based on:
D. Lyu, T. B. Soeiro and P. Bauer, "Impacts of Different Charging Strategies on the Electric Vehicle Battery Charger Circuit Using Phase-Shift Full-Bridge Converter," 2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC), Gliwice, Poland, 2021, pp. 256-263, doi: 10.1109/PEMC48073.2021.9432497.

6.1. INTRODUCTION

As the Electric Vehicle (EV) market grows rapidly, the demand for fast and efficient battery charging services also increases. In order to meet this need, battery technology research aims to push the limits for fast charging from multiple fronts, including the electrolyte and electrode materials, material architectures, and cell-to-pack design [1] [2].

While the EV battery and the charger are two of the most important components in the EV charging process from the energy transfer perspective, the implemented charging strategies, which define the way how the electric energy is transferred from the charger to the EV battery, also have significant impacts on the whole performance metrics of the system. The charging strategy results to certain voltage and current profile during the EV charging process, denoted here as charging profile. On the one hand, the charging profile, especially the injected current, determines how fast the battery is being charged, and it affects the efficiency and aging of the cells. On the other hand, it determines how and in what range the power electronics converter of the EV charger will operate, thus affecting the efficiency and utilization rate of the circuit components. Moreover, the charging strategies require different monitoring and control methods for the power converter as well as the Battery Management System (BMS).

The standard charging strategy is the Constant Current-Constant Voltage (CC-CV) due to its simplicity and ease implementation [3]. Besides CC-CV, alternative charging strategies have been proposed and/or comparative experiments were conducted in [4] - [16]. These techniques may have multiple purposes, such as, to shorten the charging time without bringing detrimental influence on the battery lifetime, to increase the charging efficiency and/or to improve the battery capacity. Above all, the focuses of those studies were on the impacts of different charging strategies on the battery cells. The work in [1] provides an overview of charging strategies, including a summary of different experimental results from the literature. However, it misses their impacts on the BMS and power electronics. In [2] a summary of the implementation requirements for different charging strategies is given, however, the impact on the power electronics converter is not qualitatively investigated. Table 6.1 summarized the defining parameters, the impacts on the battery, the requirements for the BMS and the charger of the charging strategies. The influences on the battery are based on the experimental results from various publications as indicated in Table 6.1, and the requirements for the BMS and the charger are based on the defining parameters of the charging strategies.

In order to obtain a more in-depth understanding of the impacts of the charging strategies on the EV charger circuit, a simulation case study is conducted in this chapter. Firstly, two charging strategies, the CC-CV and Multi-Step Constant Current Constant Voltage (MSCC-CV) are reviewed. Then, the impacts of the two charging strategies on the power electronic converters is investigated by the simulation of a Phase Shift Full Bridge (PSFB) DC-DC converter, which is a conventional circuit solution employed in DC-type fast EV chargers.

These two strategies are chosen in order to achieve a fairer comparison, since they have the same requirements for the hardware of the BMS and charger, and similar performance regarding the battery and the charging process, when the charging current rate of the initial CC phase and the termination current rate are selected to be the same. The Boost Charging strategy is not considered because the high current charging in the

	CC-CV	MSCC	Boost Charging	Pulse Charging
Defining Parameters	I_{CC}, I_{end}, V_{max}	$I_{CC,n}$ $(1 \leq n \leq N)$, V_{MSCC}	$I_{b(max)}$, I_{CC}, I_{end}, $V_{b(max)}$, V_{max}	I_{CC}, V_{max}, V_{PC}
Impacts on the Battery	/	1. shorter charging time [11] 2. higher charging efficiency [11] [17] 3. longer cycle life [11] [17]	1. shorter charging time [4] [12] [16]	1. reduced charging time [10] 2. higher capacity utilization [10] 3. longer cycle life [10]
		4. prolonged charging time [16]	2. shorter cycle life [16]	4. prolonged charging time [16] 5. lower capacity utilization [16]
Requirements for the BMS	1. current sensing 2. voltage sensing	1. current sensing 2. voltage sensing	1. current sensing 2. voltage sensing 3. timer functionality	1. current sensing 2. voltage sensing 3. timer functionality
Requirements for the charger	1. voltage control 2. current control	1. current control	1. voltage control 2. current control 3. extra power capacity	1. current control

Table 6.1: The defining parameters of the charging profiles, and their impacts on the battery, requirements for the BMS and the charger. Note that the impacts on the battery are presented as compared to the CC-CV charging strategy

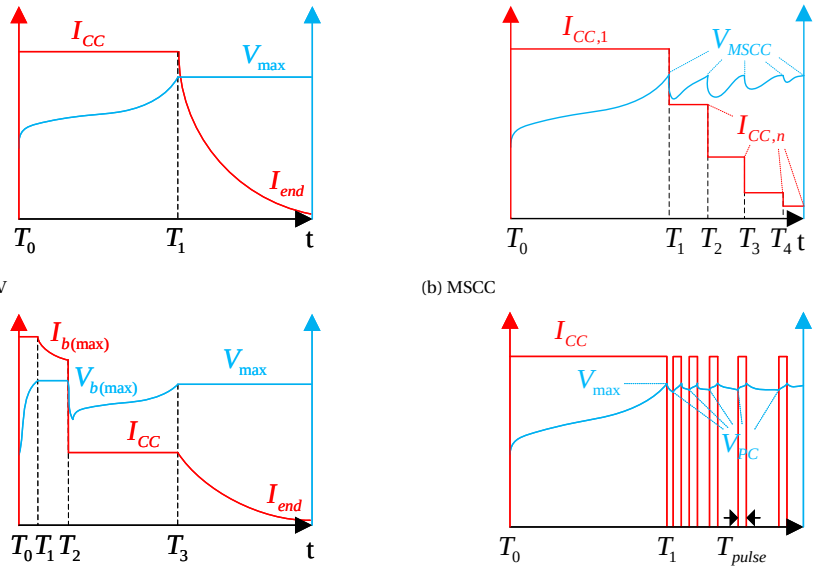
beginning requires a higher power capability of the charger compared to the other strategies, making the comparison inequitable. The Pulse Charging (PC) strategy is not considered because the current pulse is not practically acceptable without a large energy buffering device, such as a inner battery storage. Without a large energy buffer, PC will have a detrimental impact on the grid power quality caused by the intermittent power demand.

6.2. REVIEW OF BATTERY CHARGING STRATEGIES

6.2.1. CONSTANT CURRENT-CONSTANT VOLTAGE (CC-CV)

The CC-CV charging strategy features a two-stage charging process. Figure 6.1a shows the illustration of the resulted charging profile for CC-CV.

In the first stage, the battery is charged by a controlled constant current with a current rate of I_{CC}. I_{CC} can be set to be any current value allowed by the EV battery as long as it does not exceed the current limitation of the charger. In general, a higher current rate during the CC phase will result in reduced charging time. However, the gain in time would become smaller as the current rate becomes too higher due to the necessary extension of the following CV phase to reach the same final State-of-Charge (SoC) [1]. Moreover, detrimental effects to the battery may occur with high current rate, leading to the shortening of the battery cells' cycle-life [1]. The CC charging period ends when the cell voltage reaches a voltage limit V_{max}, which can be equal to the maximum voltage of the individual cell V_{cutoff} (typically $4.2V - 4.4V$ per cell, depending on the battery chemistry), and it can also be set to be lower than V_{cutoff} due to safety and to strategically extend the battery cycle-life [16]. Following that, the CV charging period begins, where the charging voltage is kept constant at V_{max} while the current injected into the battery gradually decreases. The whole charging process ends when the current falls to I_{end}. Note that the CV phase allows for the concentration gradients within the electrode particles to disperse and is usually necessary to obtain high capacity utilisation without exceeding the maximum voltage [1].



(a) CC-CV

(b) MSCC

(c) Boost charging

(d) Pulse charging

Figure 6.1: Illustrations of EV battery charging profiles

6

6.2.2. MULTI-STEP CONSTANT CURRENT

Multi-Step Constant Current strategy was proposed in [7] [8] as an alternative strategy that shortens the charging time, improves energy efficiency, and prolongs the cycle-life of valve-regulated lead/acid and Ni/MH batteries. It has been later applied to Li-ion batteries, and similar benefits were observed [11]. Figure 6.1b shows the MSCC charging profile.

MSCC is composed by $N \times$ CC phases, where N is the number of current steps. Similarly to the standard CC-CV strategy, MSCC begins the charging with a constant current $I_{CC,1}$ until the battery voltage reaches the voltage limit V_{MSCC}. Then instead of switching into a CV phase, the charging current decreases to the second step with the value $I_{CC,2}$, leading to a voltage drops below V_{MSCC}, allowing the battery to be further charged at CC. Once the battery voltage reaches the limit V_{MSCC} again, the next step takes place with another reduced current level. The charging process is terminated when V_{MSCC} is reached at the set lowest current stage $I_{cc,N}$.

A CV charging stage characterized by V_{max} and I_{end} can be added at the end of the lowest current stage in order to have better capacity utilization of the battery. This modified MSCC is denoted as MSCC-CV, and is very similar to the CC-CV charging strategy.

Yi-Hwa Liu et al. [11] compares the MSCC with CC-CV on commercially available Li-ion batteries for mobile phones (type unknown), and the test results shows that MSCC provides reduced charging time, higher charging efficiency, and longer cycle-life compare to CC-CV. An invention disclosure regarding the MSCC strategy is filed in [17], claiming to improve charging efficiency, providing longer cycle-life and better safety.

The MSCC strategy has the same requirements for the BMS as the CC-CV strategy.

However, it only requires the power electronics converter of the EV charger to be able to operate as a controlled current source since there is no CV stage involved, which means the current feedback control loop is needed. The MSCC-CV strategy, on the other hand, has the exact same requirements for both the BMS and the chargers as the CC-CV strategy. The MSCC strategy also contains partial load operation when the charging current steps down, which differs from that of the CC-CV.

6.2.3. BOOST CHARGING

The so-called "Boost Charging (BC)" was proposed in [12], and it is claimed to enhance charging speed compared to the conventional CC-CV, without introducing detrimental effects on the cycle-life of the battery. It is based on the idea that the degradation of the Li-ion battery starts at higher levels of state of charge. Therefore, this strategy uses a relatively high current level at the beginning of the charging process, especially close-to-fully discharged batteries (or at low SoC).

Figure 6.1c illustrates the typical profile of the BC. As it can be noted the BC begins with a constant current charging with a high current rate $I_{b(max)}$. During this high current level, the voltage of the battery will rise up quickly to the voltage limit $V_{b(max)}$, and after that the current rate will decrease, while the battery voltage is kept constant at $V_{b(max)}$ until the boost time T_{boost} (from T_0 to T_2) is reached. The value of $V_{b(max)}$ can be set to be the same as V_{cutoff} or even a larger value. Then a CC-CV like charging defined by I_{CC}, V_{max} and I_{end} takes place to complete the charging process. Since the whole process consists of two CC-CV stages, this strategy is also known as CC-CV-CC-CV. Similar Boost Charge idea is also proposed in [4], in which the boost period consists only of a CC step. In [18], the boost period T_{boost} does not take place in the beginning of the charging, but in the second stage.

P.H.L. Notten et al. [12] compares the BC strategy with the conventional CC-CV on cylindrical (US18500, Sony) and prismatic (LP423048, Philips) Li-ion batteries. Test results show that the BC strategy can reduce the charging time without negatively influencing the cycle-life of the batteries. In [4], a CC-CC-CV BC strategy is applied on nanophosphate high-power LFP cells manufactured by A123Systems, and the test results show great charging speeds, i.e. 20min from empty to full SoC, and no observable degradation effects are found after 4500 cycles, however, levels of capacity fade was observed. In [16], BC is compared with CC-CV charging on three different types of Lithium-ion batteries, and the results shows that compared to CC-CV, BC brings shorter charging time because of the high current level during the boost period. However, accelerated aging is observed as well.

In terms of the operation of the charger, this strategy makes the power electronics to operate in lower current than the rated value for most of the charging process, i.e. already after T_1. This may have a great impact on the converter charging cycle efficiency.

The Boost Charging strategy has all the requirements as the CC-CV for the BMS and the EV charger. Additionally, it also requires a timer functionality for the BMS to control the boost time, and during this time a higher current and power capability for the EV charger.

6.2.4. PULSE CHARGING (PC)

Pulse Charging (PC) is claimed to be beneficial for better charging efficiency, reduced charging time, and longer cycle-life by periodically interrupting the charging process with a relaxation-period of no current, or even with discharge-pulses, in which the ion concentration polarization issue of some battery technology is minimized [9] [10]. There are mainly two types of PC strategies, the first is a CC-CV strategy with the CV phase replaced by a pulse charging, denoted as CC-PC. The second one uses pulse charging throughout the whole charging process [16]. In this chapter, the first type without discharge pulse will be further investigated, since it provides a fairer comparison with the conventional CC-CV charging strategy. Figure 6.1d illustrates the CC-PC profile.

CC-PC starts with a constant current charging with the current rate I_{CC}. Once the battery voltage reaches the voltage limit V_{max}, pulse charging takes place. The time period of one current charging pulse is T_{pulse}, and after one pulse the charging stops and the relaxation period begins. The battery voltage starts to drop during the relaxation period, and If it drops to a pre-set value V_{PC}, the next current charging pulse starts. V_{PC} can be set to be the same as V_{max} to have better capacity utilization of the battery, but this would have a negative impact on the cycle-life of the battery, as the cell voltage would exceed V_{max} during the short pulse period. As the SoC increases, the cell voltage drops during the relaxation period, and the relaxation time becomes longer. The PC charging ends when the relaxation time exceeds a pre-set value $T_{pause,end}$.

6.2.5. SUMMARY

It can be seen from Table 6.1 that, some experimental results from different publications contradict with each other. Those experiments apply different cell types, testing procedures and different testing conditions such as temperature, current rate, and voltage. Therefore, it is still uncertain whether the alternative charging strategies outperform the standard CC-CV in terms of the impacts on the battery. Comprehensive experiments involving various cell types, consistent testing procedures and conditions are needed. Moreover, the experiments reported in the literature are all cell-level, this calls for further verification of the impacts using battery-pack level experiments.

In terms of the requirements for the BMS, the BC and PC require additional timer functionality compared to the CC-CV and MSCC, resulting to more complex implementation of the BMS.

As for the requirements for the charger, the MSCC and PC can be considered less complex as they do not require functional voltage control. Voltage measurements are to be used mainly for protection of the power electronics components.

Jun Li et al. [10] compared pulse charging with CC-CV charging on Sony US18650S lithium-ion cells, and the results shows that Pulse Charging achieves shorter charging time, higher discharge capacity and longer cycle-life. F. Savoye et al. [13] conducted comparable experiment on Graphite//LiFePO4 batteries, and found that the pulse charging strategy is detrimental to the battery performance compared to CC-CV with identical mean current. Paper [16] demonstrates that CC-PC strategy charges slower than CC-CV for the same amount of ampere-hour charged, and shows similar cycle-life performance between CC-PC and CC-CV. Further more, pure Pulse Charging is tested to have lower capacity utilization and similar cycle-life performance compared to CC-PC and CC-CV.

No advantages are observed for Pulse Charging compared to CC-CV charging when the mean charging currents and the cycle depths are identical.

The PC charging strategy requires charging current and battery voltage monitoring for the BMS, and also timer functionality to control the pulse time and termination of charging. Since PC charging strategy does not involve CV phase as the MSCC strategy, it only requires the charger to able to operate as a current source. The pulse charging strategy does operate at high current level, since it always charge the battery with current pulses with the same amplitude.

6.3. IMPACTS OF CHARGING STRATEGIES ON THE PERFORMANCE OF A PSFB CONVERTER

The different charging strategies will particularly influence the overall efficiency of the charger. This occurs because power electronic converters usually have a limited operation range in which the efficiency is optimal. Therefore, it is preferable to choose a charging strategy that matches, as long as possible, the converter operation within this optimal range.

The utilization rate of the charger's power capability is also affected by the charging strategies. By implementing a charging strategy that involves a long partial load operation, the charger will deliver only a fraction of its power capability.

In order to understand how would different charging strategies influence the performance of the EV charger, a 50kW DC-DC EV charger, which is constructed by paralleling five 10kW DC-DC phase-shift full-bridge power modules, is modelled with two different charging strategies, i.e., the CC-CV and the MSCC-CV.

6.3.1. PSFB ANALYTICAL MODELING

The PSFB is a popular isolated DC-DC topology for medium to high power applications. This is mainly because of the simple structure, controllable current source behaviour, good efficiency and reduced EMI emission enabled by the Zero Voltage Switching (ZVS) capability. Figure 6.2 shows the basic schematic of the PSFB converter. The detail analytical model of the PSFB converter is presented in Chapter 2.

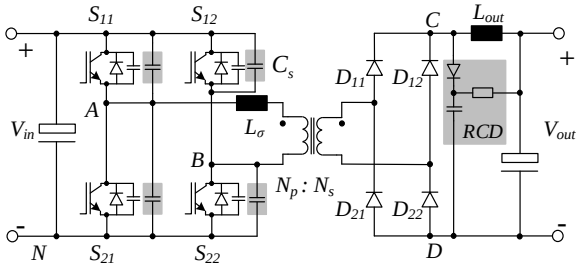


Figure 6.2: The schematic of the PSFB converter including the RCD snubber and the optional turn-off snubber capacitors C_s marked in gray boxes

6.3.2. PSFB SEMICONDUCTOR LOSS MODEL

A 10kW PSFB converter is modeled to evaluate the semiconductor losses with different charging strategies. The circuit parameters and the range of operation conditions are listed in Table 6.2.

Circuit Parameters				**Operation Conditions**			
N_p/N_s	L_σ	L_{out}	C_s	f_{sw}	V_{in}	V_{out}	P
1.235	$10\mu H$	$0.487mH$	$10.7nF$	15kHz	640V	200-500V	0-10kW

Table 6.2: Specifications of the 10kW PSFB converter

For the full-bridge the IGBT *IKW40N120CS6XKSA1* from Infineon is used, while the output diode-bridge employs the SiC diode *C4D15120A* from Wolfspeed/Cree.

The losses on the IGBT, the body diode of the IGBT, and the rectifier diodes consist of conduction and switching loss. The conduction loss can be calculated as a sum of an equivalent on-resistance loss and a forward voltage drop loss, as:

$$P_{c(IGBT/BD/D)} = I^2_{rms(IGBT/BD/D)} \cdot R_{on(IGBT/BD/D)} + I_{avg(IGBT/BD/D)} \cdot V_{F(IGBT/BD/D)}$$

The on-state resistance R_{on} and the forward voltage drop V_F For the IGBT, the body diode BD and the rectifier diodes D can be obtained from their typical on-state characteristic as stated in their datasheets, and they are listed in Table 6.3.

The switching loss of each IGBT is the sum of the turn-on and the turn-off losses:

$$P_{sw(I)} = E_{on} \cdot f_{sw} + E_{off} \cdot f_{sw} \tag{6.1}$$

where the turn-on and the turn-off losses can be calculated based on the measured switching energy loss by double-pulse testing (DPT) and the ZVS condition as:

$$E_{off} = E_{off(DPT)} - E_{oes} - E_{snb} \tag{6.2}$$

$$\begin{cases} E_{on(DPT)} = 0, & if \text{ ZVS=true} \\ E_{on} = E_{on(DPT)} + E_{oes} + E_{snb}, & if \text{ ZVS=false} \end{cases} \tag{6.3}$$

$E_{off(DPT)}$ and $E_{on(DPT)}$ is the measured switching energy loss of the IGBT, which is shown in Figure 6.3. E_{oes} is the stored energy in the equivalent instrinsic output capacitor C_{oes} of the IGBT and diode, and E_{snb} is the stored energy in the optional lossless turn-off snubber capacitor C_s. E_{oes} and E_{snb} can be roughly estimated respectively as:

$$E_{oes} = \frac{1}{2} \cdot C_{oes} \cdot V^2_{in} \tag{6.4}$$

$$E_{snb} = \frac{1}{2} \cdot C_s \cdot V^2_{in} \tag{6.5}$$

The switching loss of the diode consists of the reverse recovery loss which is relatively low in SiC diodes:

$$P_{sw(D)} = k \cdot Q_c \cdot (V_{in} \cdot \frac{N_s}{N_p}) \cdot f_{sw} \tag{6.6}$$

The Q_c is the reverse recovery charge given in the Diode datasheet. C_{oes} and Q_c are listed in Table 6.3.

components	characteristics	values
IKW40N120CS6XKSA1 (IGBT)	C_{oes}	130pF
	$R_{on(IGBT)}$	28.100mΩ
	$V_{F(IGBT)}$	1.217V
IKW40N120CS6XKSA1 (body diode)	$R_{on(BD)}$	21.900mΩ
	$V_{F(BD)}$	1.501V
C4D15120A	$R_{on(D)}$	74.806mΩ
	$V_{F(D)}$	0.795V
	$Q_{c(D)}$	65nC
	k	0.667

Table 6.3: electrical characteristics of the used components

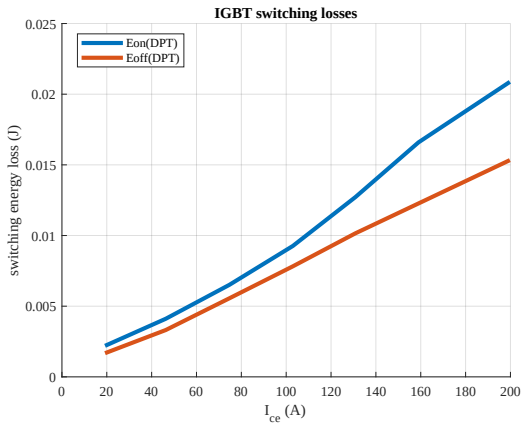


Figure 6.3: the measured switching energy loss of the IGBT

With the analytical model and the loss calculation, The efficiency map of the converter that visualizes the efficiency at each operation condition is shown in Figure 6.4.

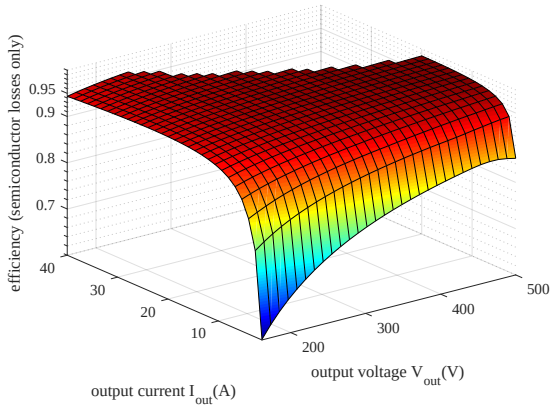


Figure 6.4: The efficiency map for the 10kW PSFB converter considering only the semiconductor losses

6.3.3. CHARGING PROFILE SIMULATION

In order to obtain the charging profile for the CC-CV and MSCC-CV strategies, an impedance-based model of a lithium nickel oxide (LNCO) Boston Power SWING 5300 given in [18,20] is used. The model is constructed by series connected impedance blocks, which is derived from a specific electrochemical equation linked to the battery operation.

Two sets of comparison simulations with different current rates are conducted. The characteristics of the CC-CV and MSCC-CV charging strategies of the two sets of simulations are listed in Table 6.4. For a fair comparison, in each simulation, I_{CC} of the CC-CV and $I_{CC,1}$ of the MSCC-CV are set to be the same. Moreover, V_{max} and V_{MSCC}, and I_{end} are set to be equal as well.

	battery specifications		**CC-CV characteristics**			**MSCC-CV characteristics**				
	nominal capacity	nominal voltage	I_{CC}	V_{max}	I_{end}	N	$I_{CC,n}$	V_{MSCC}	V_{max}	I_{end}
comparison I	44.5kWh	350V	$1C$	$4.2V$	$0.05C$	5	$1C/n$	$4.2V$	$4.2V$	0.05C
comparison II	22.2kWh	350V	$2C$	$4.2V$	$0.05C$	5	$2C/n$	$4.2V$	$4.2V$	0.05C

Table 6.4: the specifications of the battery and the two charging strategies used in the two comparison experiments

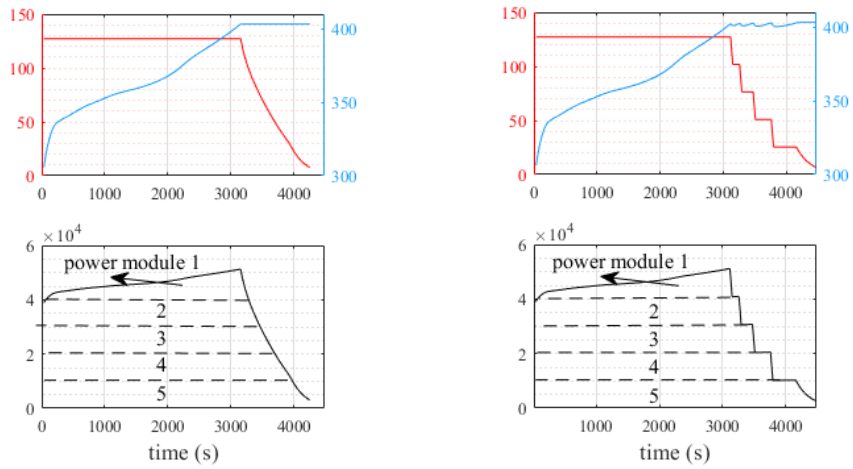
For comparison I, a battery pack with 44.5kWh nominal energy capacity, and 350V nominal battery voltage is simulated based on the cell model mentioned before. These battery specifications are similar to those of a Nissan Leaf.

For comparison II, the energy capacity is reduced to 22.2kWh, while keeping the battery rated voltage of 350V. This is to ensure that the actual charging current of comparison II is similar to that of comparison I, despite the current rate is doubled. These battery specifications are similar to those of a BMW i3 60Ah model.

6.4. BENCHMARKING RESULTS

6.4.1. COMPARISON I: 1C CURRENT RATE

Figure 6.5a and 6.5b show the CC-CV and MSCC-CV charging and power profiles with 1C current rate for the 5 parallel 10kW power modules. Assumption is made that the power modules are always operating at full power if possible.



(a) CC-CV

(b) MSCC-CV

Figure 6.5: The charging and power profiles for a 44.5kWh EV battery with 1C current rate. The red line is the charing current(A), the blue line is the charging voltage (V), and the black line is the charging power (W)

It can be seen that since I_{CC} and $I_{CC,1}$ are set to be the same, the initial CC phase of the two charging strategies are identical. While in the CV phase of the CC-CV strategy, the power modules operates in partial load condition defined by the current drop as shown in Figure 6.5a. Conversely, the MSCC-CV strategy mimics the partial load operation by turning off one-by-one the paralleled power modules once the charging voltage reaches V_{MSCC}, as shown in Figure 6.5b.

As for the individual power modules, in the case of CC-CV charging strategy, the power modules 2-5 are operating in a Constant-Power Constant-Voltage (CP-CV) manner, while the power module 1 is operating in a Variable-Power Constant-Voltage (VP-CV) manner. While in the case of MSCC-CV charging strategy, the power modules 2-4 are always operating at Constant-Power (CP), whereas module 1 is at Various-Power (VP), and module 5 is at CP-CV. This not only means the operation range of power modules 1-4 with the MSCC-CV charging strategy are narrowed compared to the CC-CV strategy, but also that each operating module have a higher power utilization.

Two quantitative indicators are suggested for comparison purpose, the charging cycle efficiency, and the utilization rate of the installed power. The charging cycle efficiency is the overall efficiency considering the whole operation range of the charging process. It can be calculated as eq. (6.7), where n is the indicator of the power modules, T_n is the operation time of the power module n, $P_n(t)$ is the charging power of the power module

n, and $P_{loss,n}(t)$ is the power loss of the power module n.

$$\eta_{cycle} = \frac{\sum_{n=1}^{n=5} \int_0^{T_n} (P_n(t) - P_{loss,n}(t)) \cdot dt}{\sum_{n=1}^{n=5} \int_0^{T_n} P_n(t) \cdot dt} \tag{6.7}$$

The utilization rate of the installed power is the indicator that shows how efficient is the installed power been used. The higher the utilization rate, the longer that converter operates in the rated power within a certain period. It can be calculated as eq. (6.8), where $T_{full,n}$ is the time of operation at rated or higher power in the total operation time of the module n.

$$\nu = \frac{\sum_{n=1}^{n=5} T_{full,n}}{\sum_{n=1}^{n=5} T_n} \tag{6.8}$$

The charging cycle efficiency and the utilization rate of the installed power are calculated for the CC-CV and MSCC-CV charging profile of comparison I and listed in Table 6.5.

	CC-CV	**MSCC-CV**
charging cycle efficiency η_{cycle}	97.51%	97.51%
utilization rate of installed power ν	78.97%	82.90%

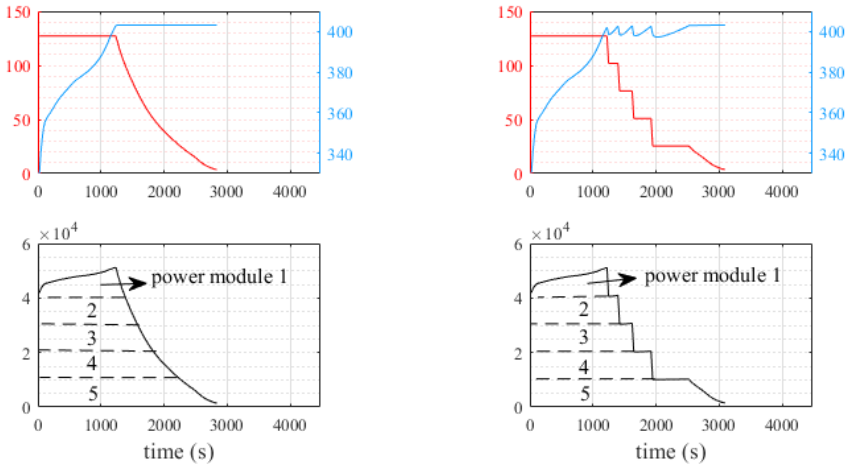
Table 6.5: The simulation results of comparison I

It can be seen from Table 6.5 that, the two charging strategies result in the same charging cycle efficiency. This will be interpreted later together with the result of comparison II. Secondly, the utilization rate of the installed power of the MSCC-CV charging strategy, 82.90%, is 3.93% higher than that of the CC-CV strategy, which is 78.97%. This is due to the fact that the MSCC-CV strategy turns off the power modules rather than trying to operate each one with lower power. This higher utilization rate of the installed power can be utilized to provide more accessible charging service if the power modules are combined together in a flexible way, in which individual power module has its own output. In this way, once a power module is turned off during a charging service, it can be used to provide another charging service, such as feeding power to another EV, thus the accessibility of a charging station is increased.

6.4.2. COMPARISON II: 2C CURRENT RATE

Figure 6.6a and 6.6b show the CC-CV and MSCC-CV charging and power profiles with 2C current rate for the 5 power modules respectively.

Compared to figure 6.5a and 6.5b, it can be seen that in the charging profiles with 2C current rate, the percentage of the CV phase compared to the CC phase is much longer,



(a) CC-CV

(b) MSCC-CV

Figure 6.6: The charging and power profiles for a 22.2kWh EV battery with 2C current rate. The red line is the charging current (A), the blue line is the charging voltage (V), and the black line is the charging power (W)

this makes the percentage of time operating at lower power condition higher. This is due the electrochemical reactions of the battery cells.

The charging cycle efficiency and the utilization rate of the installed power are calculated for the CC-CV and MSCC-CV charging profile of comparison II and listed in Table 6.6.

	CC-CV	**MSCC-CV**
charging cycle efficiency η_{cycle}	97.63%	97.65%
utilization rate of installed power ν	72.92%	82.21%

Table 6.6: The simulation results of comparison II

It can be seen that the charging cycle efficiencies for CC-CV and MSCC-CV strategies are both slightly higher than that of comparison I, and at the same time, the one of the MSCC-CV is 0.02% higher than that of the CC-CV. All these differences of charging cycle efficiency can be explained by the efficiency performance of the converter at different operation conditions as shown in Figure 6.7.

Figure 6.7 shows the efficiency map of the converter together with the CP-CV operating trajectory. It can be seen from Figure 6.7 that, as the converter operates following the CP-CV trajectory, the instantaneous power efficiency of the converter will increase during the CP phase, and it will reaches the peak in the beginning of the CV phase, and then starts dropping in the rest of the CV phase. The fact that the power efficiency is the highest at the end of CP phase and the beginning part of CP phase indicates that

the MSCC-CV strategy which operates the parallel converters mostly in the CP phase, as shown in Figure 6.5b, does not necessarily bring higher charging cycle efficiency, compared to the CC-CV strategy which involves longer partial load operation in the CV phase as shown in comparison I,

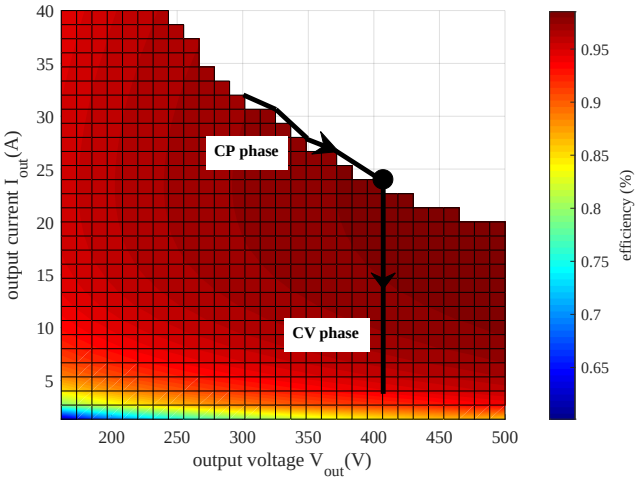


Figure 6.7: The efficiency map of the power module with the trajectory of the CP-CV charging profile

The utilization rate of the installed power for MSCC-CV with an initial current rate of 2C, 82.21%, is 9.29% higher than that of CC-CV, which is more than 2 times than the difference found in comparison I. This is due to the larger percentage of CV phase within the whole charging process with 2C current rate.

6.5. CONCLUSION

Firstly, different charging strategies might or might not lead to different charging cycle efficiency on the same power electronic converter, depending on the composition of the charging profile and the power efficiency performance of the converter on the charging profile. Charging strategies such as MSCC-CV together with the modular structure of the charger, can narrow the operation range of the converter compared to the CC-CV. However, smaller operation range does not necessarily guarantee higher charging cycle efficiency, as demonstrated by the comparison results in this chapter. Further research can investigate the forming factors of the efficiency map of the converter, and the ways to reshape it to provide better charging cycle efficiency with different charging strategies.

Secondly, different charging strategies lead to different utilization rate of installed power. This is due to the mechanism of how different charging strategies controls the charging process. For MSCC-CV or MSCC, the power modules are turned off from full power operation once the voltage has reached the set limits, rather than operated in partial power as in CC-CV, and this greatly improves the utilization rate of the installed power if combined with a flexible parallel modular multiple outputs structure. And this

higher utilization rate would bring better accessibility to the EV charging stations.

Therefore, alternative charging strategies other than CC-CV, such as MSCC-CV, can improve the performance of the power electronic converters of the EV chargers in terms of charging cycle efficiency and utilization rate of the installed power, if the converters' efficiency maps match with them, and a flexible structure of the power modules is implemented. Last but not least, as the charging current rate increase, the space of improvement for the charging cycle efficiency and utilization rate of the installed power will be larger, because the time of operating at partial power is longer.

6.6. REVIEW OF THE SYSTEM STRUCTURES OF MULTI-PORTS EV CHARGING STATION

6.6.1. TWO-STAGE LOW VOLTAGE AC GRID COUPLED STRUCTURE

In the two-stage low voltage (LV) AC grid coupled structure, every distributed power module formed by a non-isolated AC-DC converter cascaded by an isolated DC-DC converter are connected with the LV grid (below 1kV), which is created by stepping down the voltage of the medium voltage (MV) AC grid (between 1kV and 36kV) using a grid transformer. The non-isolated AC-DC converters are to rectify the AC input voltage to regulated DC output voltage while providing functions including power-factor-correction (PFC). The isolated DC-DC converters further regulate the DC voltage according to the required values for EV charging, while providing galvanic isolation between the EV and the grid, and between two of the EVs. Figure 6.8 shows the two-stage LV grid coupled structure.

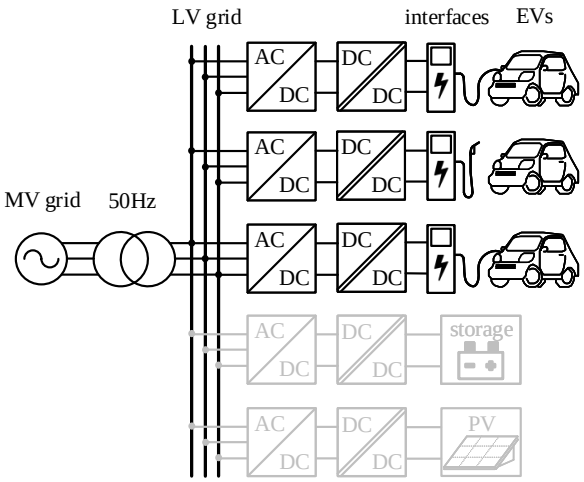


Figure 6.8: Two-stage LV grid coupled structure

The first advantage of this structure is scalability of the system. Due to the individual operation of the power modules for each ports, it is easy to expand the charging station by simply connecting new power modules to the LV grid, as long as the total power does

not exceed the power capability of the grid transformer.

The second benefit of this structure is the better availability of semiconductor components. Commercially available transistors and diodes can be utilized for the distributed power modules, since the voltage and power rating of them are not high. Therefore, shorter design and production time could be achieved.

The drawback of this structure is the exceeding number of power electronic converters. With 2 converters (an AC-DC and a DC-DC) required for every charging port, resulting in 2×N power electronic converters for a N-ports charging station. The Proportional number of semiconductor devices, gate drivers, magnetic components and control devices (sensors, controllers, etc.) implies the potentially high cost and efficiency drop of the system.

Additionally, the LV AC grid coupled structure also suffers from the complexity of control brought by the issues such as reactive power control, voltage and frequency control, and inverter synchronization during islanded operation of the system [22].

6.6.2. SINGLE-STAGE LV AC GRID COUPLED STRUCTURE

Compared with the two-stage LV AC grid coupled structure as shown in Figure 6.8, where there are two power conversion stages, the non-isolated AC-DC and the isolated DC-DC, the single-stage LV AC grid coupled structure simplifies the system by adapting isolated AC-DC converters that also has wide output voltage regulation ability. Figure 6.9 shows the single-stage LV grid coupled structure.

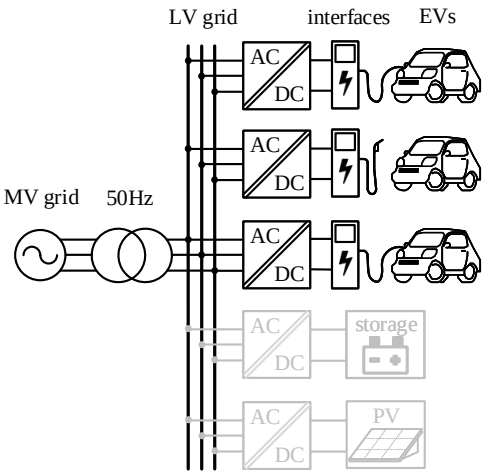


Figure 6.9: Single-stage LV grid coupled structure

A current source rectifier (CSR) topology with a high-frequency (HF) isolation transformer has been reported in [23] [35] which can perform the single-stage power conversion. The challenge for this structure is the design of the isolated AC-DC converter and the increased control complexity of it.

The advantages of this structure is the power conversion efficiency improvement and cost reduction compared to the two-stage structure, since the number of semiconductor

components in the current path is reduced [35]. Moreover, the scalability of the system and the availability of the semiconductor components are similar to those of the two-stage LV grid coupled structure.

6.6.3. DC BUS COUPLED STRUCTURE

The DC bus coupled structure reduces the required number of converters by replacing all the distributed AC-DC converters with a high-power-rated central one. The output of this central AC-DC converter supports a DC bus to which all the DC-DC converters are connected. Figure 6.10 show the diagram of this structure.

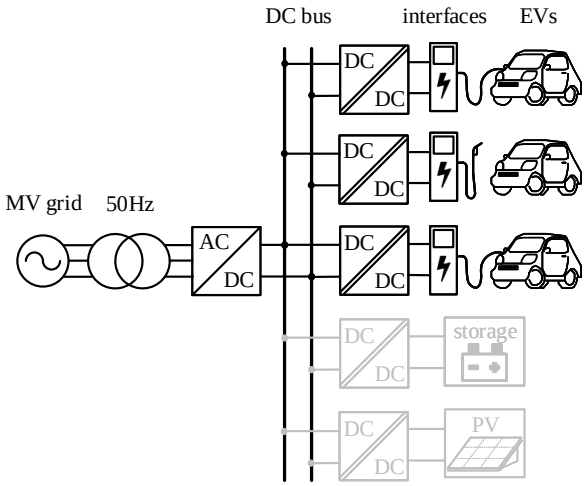


Figure 6.10: DC bus coupled structure

The scalability of the system is comparable to that of the LV grid coupled structure, providing that the power capability of the grid transformer and the central AC-DC converter is high enough.

The number of converters required reduces to N+1 for a N-ports charging station. If assuming the cost of the semiconductor devices and the magnetic components are proportional to their volt-amp (V-A) ratings, the DC bus coupled structure will have similar cost for semiconductor and magnetic components compared to the LV grid coupled structure, because the power rating of the central AC-DC converter is equivalent to the sum of the distributed ones. However, since the number of control devices could be reduced, this structure will still have cost advantage over the LV grid coupled structure. In terms of the power conversion efficiency of the system, it is uncertain which one prevails. The reason is that the central AC-DC converter runs higher risk of operating outside the optimal operation range when small number of EVs are connected, which implies potential efficiency drop.

Moreover, compared to the LV AC grid coupled structure, simpler control could be applied in the DC bus coupled structure, as the issues encountered in AC grid coupled structure are not involved anymore.

The central AC-DC converter could be implemented by an uncontrolled rectifier, which brings advantages such as reduced cost and high reliability, but at the same time, more careful control should be applied on the DC-DC converters to prevent the oscillation of DC bus voltage.

6.6.4. DC BUS COUPLED STRUCTURE WITH SST

The DC bus coupled structure could also be achieved by replacing the low frequency grid transformer and the central AC-DC converter with a Solid State Transformer (SST) [22] as shown in Figure 6.11.

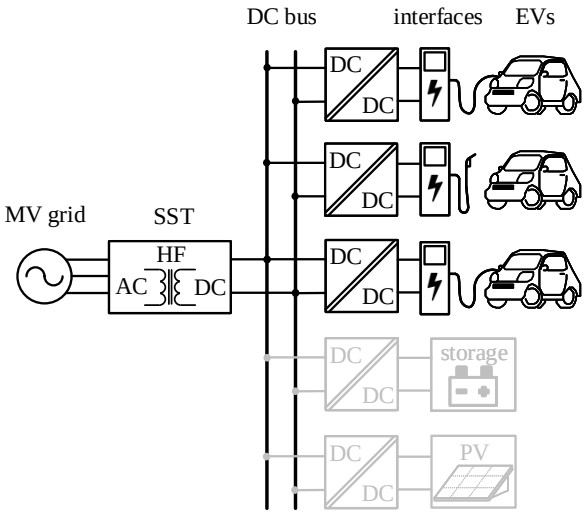


Figure 6.11: DC bus coupled structure with SST [22]

The SST realizes the AC-DC conversion by means of power electronic converter and high frequency transformer, and the way how the EVs, storage and PV connect to the DC bus remains the same. Since the high frequency transformer is smaller in size compared to the low frequency one, therefore the implementation of SST offers the benefit of size reduction of the system. Furthermore, the reduction of size results to lower installation costs per KW power capability [22]. However, the reduction of size and weight could only be achieved with careful design regarding the thermal and insulation aspects of the SST. Moreover, the cost and efficiency of the SST currently do not have benefits compared to the conventional transformers [25].

6.6.5. COMBINED DC BUS COUPLED STRUCTURE

In [26], a combined DC bus coupled structure aiming to reduce the total power capability of the converters while maintain the charging capacity is introduce, as shown in Figure 6.12.

Connected to the LV AC grid generated by the MV grid and grid transformer, the central AC-DC converters create a combined DC bus by connecting the DC outputs (V_{dc1},

V_{dc2}, V_{dc3}...) together. These output voltage of the central converters are settled. By connecting the two throws of the switches to two lines of the combined DC bus, a base DC voltage V_{base} will apply on the two poles of the switch. V_{base} could be V_{dc1}, V_{dc2}, V_{dc3}, $V_{dc1} + V_{dc2}$, $V_{dc2} + V_{dc3}$, and $V_{dc1} + V_{dc2} + V_{dc3}$, depending how the throws are connected to the combined DC bus. The distributed transformers and DC-DC converters generate flexible DC output voltage V_{flex} which is connected in series with V_{base} to charge the EV battery.

The central converters always operate in a settled operation point, and the distributed converters regulate the charging voltage and power on the basis of V_{base}. As a result, the power capability of the distributed DC-DC converters could be largely reduced.

However, several drawbacks prevent the adaption of this structure. First of all, the power balancing among the central AC-DC converters brings additional complexity. As a plurality of EVs connect to the system, the power drawn from the central converters needs to be evenly distributed among them, otherwise the overload of certain central converters will happen, resulting in shorten lifetime of the converters. Secondly, additional distributed transformers are needed for the distributed converters, which adds up the total cost of the system. Last but not the least, the EVs are not isolated with each other in this structure, which is not desired for the EV charging application.

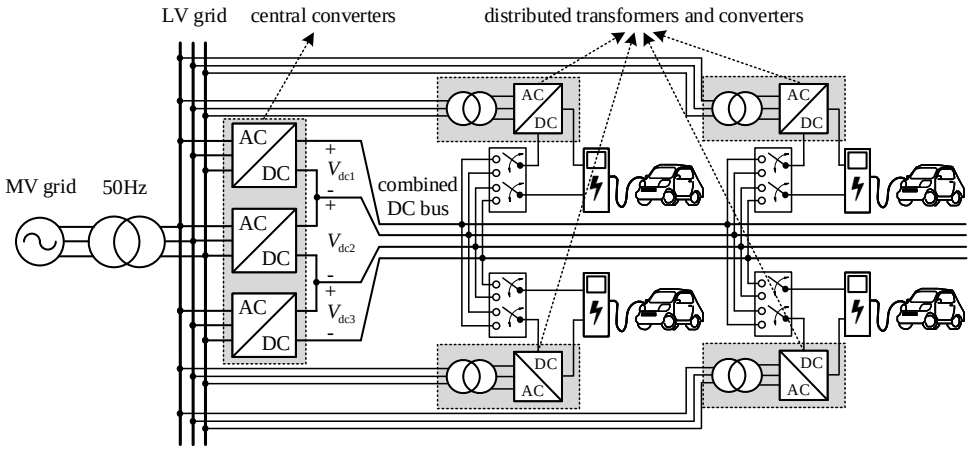


Figure 6.12: Combined DC bus coupled structure [26]

6.7. MULTI-WINDINGS TRANSFORMER STRUCTURE

By the utilization of a multi-winding transformer comprising a plurality of secondary windings, the system structure illustrated in Figure 6.13 is obtained [27].

The multi-winding transformer steps down the medium voltage in the primary side to a plurality of secondary windings, to which the distributed AC-DC converters are connected to convert the AC voltage into DC and charge the EVs. The isolation between each two ports are achieved by the multi-winding transformer, thus no isolated DC-DC converters are needed anymore.

Due to the high efficiency of the transformer, as well as the absence of the DC-DC conversion stage, the power conversion efficiency of this structure is high compared to other structures. However, the cost, size and weight of the system are strongly depended on the design of the multi-winding transformer. Moreover, the cross-coupling of power flows between ports needs to be addressed, which adds up to the complexity of the design.

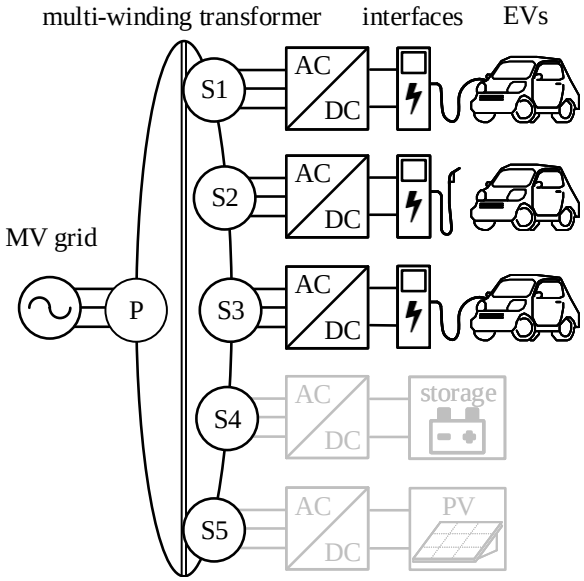


Figure 6.13: Multi-winding Transformer Structure [27]

6.7.1. SWITCH MATRIX FOR FLEXIBLE MULTI-PORTS CONFIGURATION

In the system structures of multi-ports EV charging systems and the multi-ports converters (MPCs), each of the output ports operates or tries to operate independently (in the case of MPCs, power flow coupling issue exists), and could be used to charge one EV. This independent one-port-one-EV system guarantees stable charging power for each of the output port, and simple system-level control.

On the other hand, the utilization of the installed power of the one-port-one-EV system is limited. In order to be able to charge N numbers of EVs simultaneously with the maximum power of X(kW) for each of them, N ports and a total power capability of N×X(kW) is required for the whole charging system. However, scenarios exist where not all the ports are fully utilized. For instance, there are less than N numbers of EVs connected and charging, or there are some EVs that have finished charging but stay connected to the ports, or there are some EVs charging with partial power as the state-of-charge (SoC) increases during charging. In these scenarios, the utilized power compared to the installed power capability of the system, i.e., the utilization of the installed power becomes less.

Moreover, the maximum charging power of each output ports is restricted by the power module of that port. As a result, the high power fast charging for some EVs could not be achieved.

The switching matrix is a solution to address the two limitations by enabling flexible power arrangement using switches to connect different ports, so that the idle power could be utilized to provide high power charging. Figure 6.14 shows the basic parallel switch matrix proposed in [36].

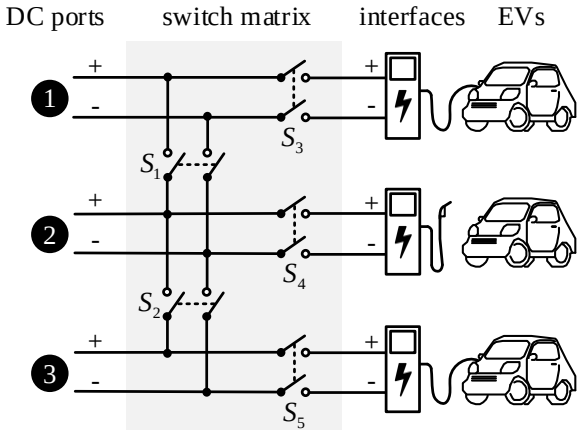


Figure 6.14: Parallel switch matrix [36]

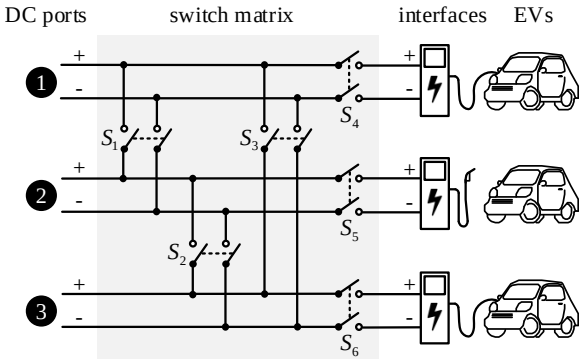


Figure 6.15: Complete parallel switch matrix

An alternative series-parallel switch matrix has been reported in [37], where it is combined with thyristor-based rectifiers for wide voltage range EV charging.

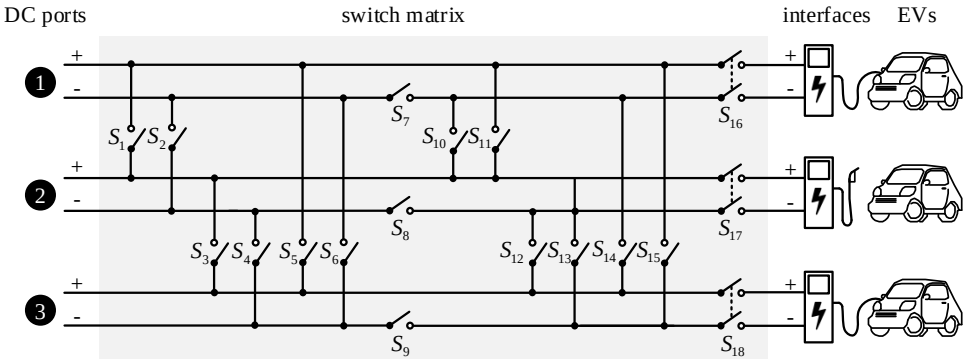


Figure 6.16: Simplified series-parallel switch matrix

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CONCLUSION AND FUTURE RESEARCH

The objective of this thesis is to investigate the design and operation of advanced DC/DC power electronic converters, which can serve as Power Electronic Building Blocks (PEBBs) for a flexible Electric Vehicle (EV) DC charger with multiple output charging points. To achieve this research objective, three research questions are posed and answered. The main conclusions of each research question are summarized in this chapter. Recommendations for future research are also given.

7.1. ADDRESSING RESEARCH QUESTIONS

- Research Question 1: *What are the suitable DC-DC converters for the back-end power modules?*

While the most common EV battery voltage architecture is 400V, new high-end EV models with 800V battery voltage architectures are introduced to the market. Therefore, the challenge for the EV chargers is clear: to provide charging services to different cars, which will demand the power electronic circuits to operate with extremely wide battery voltage ranges. However, according to the knowledge of the authors, there is no study in the literature that has provided experimentally verified isolated DC/DC converters for battery charging that are able to charge both the 400V and 800V EVs. The problem lies in the poor efficiency performance when these converters are made to operate in such a wide voltage range.

Chapters 3, 4, and 5 propose the power electronic solutions for the back-end power modules. In Chapter 3, a re-configurable PSFB converter with an extremely wide voltage range is analyzed, designed and tested. In Chapter 4, a two-stage power converter based on an LLC resonant converter followed by an Interleaved TCM buck converter is investigated. And in Chapter 5, the DAB converter with a ZVS-optimized constant and variable switching frequency modulation schemes are researched. These solutions adopt topology modifications and modulation methods, and the experimental results validate that

they can extend the operational voltage range while keeping high efficiency in the whole operating range.

In conclusion, firstly, the proposed reconfigurable structure converters are effective solutions to extend the voltage range of conventional power electronic converters and improve their efficiency performance across the whole range. Secondly, the DAB converter with the ZVS-optimized constant and variable switching frequency modulation schemes can enhance ZVS performance in EV charging applications while concurrently maintaining high efficiency performance, making it also a promising solution in the context of wide voltage range EV charging applications.

- Research Question 2: *How to conduct a multi-objective design for an optimal power module design?*

The multi-objective design and benchmark of power electronic converters in terms of cost, power density, and efficiency performance is challenging, primarily due to the poor availability of the components' data. Component cost models depending on physical component properties are typically applied in the literature, but they are not so straightforward to implement. Moreover, a large database acquired from manufacturers is needed for a better fitting, which is not easily accessible.

Chapter 6 proposes a multi-objective power electronic converter design and benchmark process, with the normalized cost, average efficiency, and power density of the magnetic components and heatsink being the objectives of interest. Firstly, the essential data of the components are collected from the easily accessible database of the re-distributors. Secondly, the correlation of cost versus the performance indexes of the components are established by processing the data with curve-fitting methods. In this way, the designs are not limited by certain component choices and the correlations can be directly utilized by other designers without a components database. Using this multi-objective design process, three re-configurable structure PSFB converters are analyzed and benchmarked for the wide voltage range public EV charging application. Based on the resulted design space of the converters, A close-to-Pareto-front 45kHz r-PSFB prototype converter is built to verify the analysis, and the actual cost, power density of the magnetics and heatsink, and averaged efficiency match with the design well. This proves the feasibility of proposed multi-objective design and benchmark process, and identify the t-PSFB and r-PSFB converters to be the outstanding solutions in the wide voltage range public EV charging application.

In conclusion, well-accessible data provided by the components re-distributors can be utilized to establish the correlations between the cost and loss performance of the components. The correlation can be used in the multi-objective design process to determine the most advantageous converter in terms of the normalized cost, power density of the magnetic components and heatsinks, and the average efficiency performance.

- Research Question 3: *How to operate the power modules in the charging system to achieve higher efficiency and utilization?*

The charging strategies, which define how the electric energy is transferred from the charger to the EV battery, significantly impact the system's performance metrics. The

charging strategy results in a certain voltage and current profile during the EV charging process, denoted here as the charging profile. On the one hand, the charging profile, especially the injected current, determines how fast the battery is being charged, affecting the cells' efficiency and aging. On the other hand, it determines how and in what range the power electronics converter of the EV charger will operate, thus affecting the efficiency and utilization rate of the circuit components.

Chapter 7 conducts a simulation case study to investigate how different charging strategies affect the performance of a modular EV charger. It is found that, firstly, the alternative charging strategies such as MSCC-CV together with the modular structure of the charger, can narrow the operation range of the power modules compared to the conventional CC-CV charging strategy. Combined with a tailored power module design, higher charging cycle efficiency can be achieved using alternative charging strategies. Secondly, alternative charging strategies can improve the utilization rates of installed power if combined with a flexible parallel modular multiple outputs structure.

To conclude, higher charging cycle efficiency and utilization rate of the power-module-based EV chargers can be achieved with the alternative charging strategies, if the converters' efficiency maps match with them, and a flexible structure of the power modules is implemented.

7.2. FUTURE RESEARCH RECOMMENDATION

This thesis focuses on the design and operation of the back-end power electronic modules of a flexible DC-type EV charging system. However, there are still research gaps in the following areas that can be further investigated:

- Benchmark of the viable power electronic solutions

  This thesis proposes the reconfigurable structure PSFB and resonant converters, and also the DAB converter with novel ZVS-optimized modulation methods as promising solutions for the wide voltage range DC-type EV charging system. But the multi-objective benchmark of these solutions has not been conducted due to time constrain. The multi-objective design and benchmark process presented in Chapter 6 can be further applied to find out the optimal solution in terms of cost, power density, and efficiency.

- AC/DC single-stage power module

  This thesis focuses on the back-end power electronic converter of the two-stage DC-type EV charging system. However, the isolated AC/DC single-stage converter can also be used as power modules for a DC-type charging system. This type of isolated AC/DC single-stage converter can perform the AC rectification and DC regulation functionalities together, and it has the potential of lower cost and high-efficiency performance, due to the fewer components account. Therefore, its design and benchmark with the two-stage solution can be an interesting research topic.

- System structures of charging system

Apart from the power electronic modules, which are the focus of this thesis, the system structures of the charging system also have significant impacts on the operation and performance of the overall charging system. Several system structures of the charging system are introduced in Chapter 7, and future research can investigate the detailed analysis and comparison regarding the cost, efficiency, and reliability of these different system structures. Moreover, the integration of battery storage and renewable energy sources are also interesting aspects to consider during the research.

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8. **D. Lyu**, C. Straathof, T. B. Soeiro, Z. Qin and P. Bauer, "ZVS-Optimized Constant and Variable Switching Frequency Modulation Schemes for Dual Active Bridge Converters," in IEEE Open Journal of Power Electronics, vol. 4, pp. 801-816, 2023, doi: 10.1109/OJPEL.2023.3319970.

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