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A 26 GHz Balun-First Three-Way Doherty PA in 40 nm CMOS with 20.7 dBm Psat and 20 dB Power Gain

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***Abstract* — This paper presents a 40 nm CMOS mm-wave 3-way Doherty power amplifier (PA) suitable for 5G mm-wave transmitters. It features a bandwidth-enhanced technique using a compact single-supply balun-first 3-way Doherty combiner. The realized front-end with a core area of 0.77 mm^2 delivers a peak power/gain of more than 20 dBm/16 dB and a drain efficiency (DE) of better than 15 %/22 %/33 % at 9.5 dB/6 dB/0 dB power back-off across a 24-to-30 GHz band. At 26 GHz, it achieves an EVM/ACLR of -23.5 dB/-29.5 dBc for an 800 MHz 64-OFDM signal with 9.8 dBm average output power and a 15 % average DE.**

***Keywords* — Doherty, 3-stage Power amplifier, Compact, Millimeter wave, Lumped components, Norton transformation.**

I. Introduction

Millimeter-wave (mm-wave) 5G transmitters (TXs) are key enablers to streamline a multi-Gbit/s data throughput. In these mm-wave TXs, high integration, compact area, low cost, and high yield are prime reasons for exploiting nanoscale CMOS technologies. Moreover, they generally utilize spectrally efficient complex modulation schemes with high peak-to-average power ratios (PAPRs) that entail the TX operating in deep power back-off (PBO), thus degrading its average efficiency. Also, these mm-wave 5G front-ends must provide sufficient power gain and radiated power so as to relax the design constraints for the preceding up-converting stages and overcome free space path loss. Accordingly, techniques such as N-way Doherty configuration [1]–[8], comprising main and peak power amplifiers (PAs), are investigated to deliver the required TX power levels and power gain with decent efficiency at peak and PBOs.

The recently published 4-way Doherty combiner for sub-6 GHz operation [5] appears superior to conventional 2-way Doherty PAs because in deep PBO, when only the main PA is active, the 4-way Doherty has a direct (uncompromised) signal path between the main PA output and the overall output of the Doherty combiner, which minimizes power loss. Furthermore, in this configuration, only the off-state impedance of the peak-1 PA affects Doherty PA's efficiency. In contrast, at mm-wave frequencies, including practical constraints for the losses in an N-way combiner, analysis of the N-way Doherty PAs shows that 3-way Doherty PA is the best candidate since at 12 dB PBO its performance is comparable to 4-/5-way Doherty networks while offering a more compact combiner and lower design complexity [8]. In addition, a 2-way Doherty PA doesn't fully address the issue of average efficiency improvement for signals with a large PAPR, while all output power must be generated using only two power devices. Furthermore, practical 3-way Doherty PAs have moderate bandwidth for drain efficiency/output power at deep PBO and full power. Besides, they typically exploit two supply voltages in their front-end stages to obtain sufficient power gain and radiated power. This paper proposes a compact single-supply three-stage balun-first 3-way Doherty PA operating in a 25-to-26 GHz band.

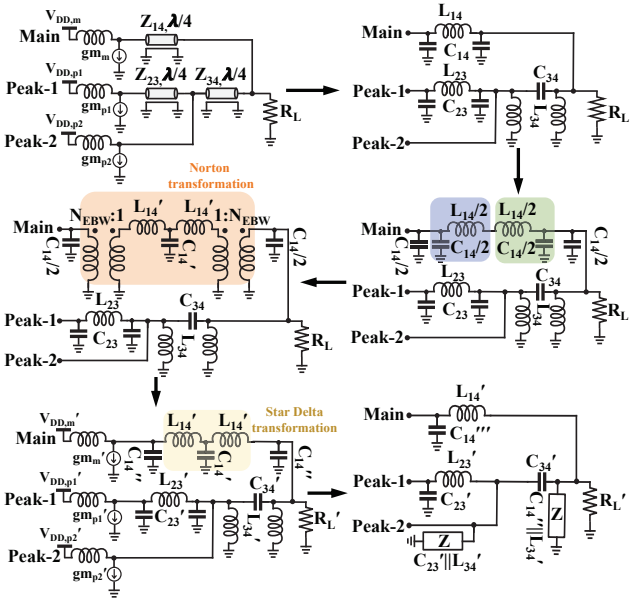

Fig. 1. The proposed compact EWB technique on a 3-way Doherty combiner.

II. Design Of the Balun-First 3-Way Doherty

Figure 1 unveils progressively how to implement the proposed 3-way Doherty network featuring an enhanced bandwidth technique (EBW). This technique is implemented on the main PA's path as it is the most dominant power loss segment. First, the three transmission lines (TLs) of the 3-way combiner are replaced by their low-pass (LP) and high-pass (HP) lumped element equivalents. Next, the inductor and the capacitors in the main path are split, and a Norton transformation [9] is applied. Subsequently, the transformer obtained by Norton transformation is supplanted by lowering the main supply source (V_{DD}) by N_{EBW}, increasing the transconductance of the power device (gm) by N_{EBW},

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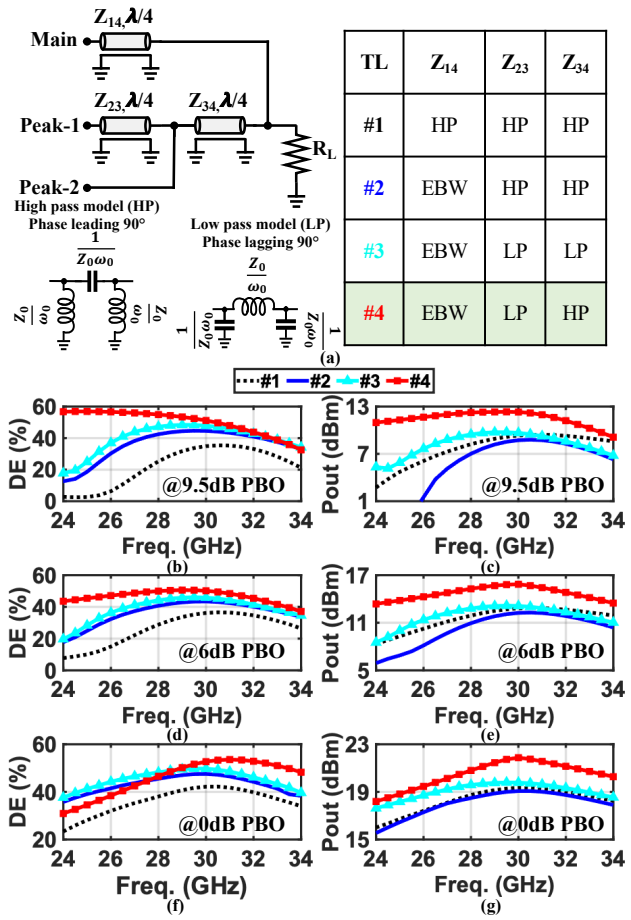

TL	Z_{14}	Z_{23}	Z_{34}
#1	HP	HP	HP
#2	EBW	HP	HP
#3	EBW	LP	LP
#4	EBW	LP	HP

Fig. 2. (a) The 3-way Doherty structure and its HP and LP options for implementing the TLs, (b) DE, (c) output power, across frequency at 9.5 dB PBO, (d) DE, (e) output power, across frequency at 6 dB PBO, (f) DE, and (g) output power, across frequency at full power.

increasing capacitors by N_{EBW}^2, and reducing inductors and impedance seen at the drain node by N_{EBW}^2. Finally, a star-to-delta transformation makes the 3-way combiner even more compact.

Figure 2a exhibits different variations of 3-way Doherty, which is obtained by alternating between the LP and HP models for the TLs. All simulations are performed with an ideal PA model and a quality factor of 25/15 for the capacitors and inductors, showing that alternative #4 in Fig. 2a has the best performance across frequency among its peers at 9.5/6/0 dB PBO. Intuitively, its equivalent passive networks' magnitude and phase variation are lower than the others since it comprises a combination of LP and HP circuits in the peak PAs, similar to an inverted 2-way Doherty PA [10], thus enhancing its operational bandwidth. Furthermore, having an LP structure adjacent to the active power devices absorbs the parasitic drain-source capacitance. Also, push-pull PAs traditionally incorporate a balanced-to-unbalanced (balun) transformer required for a single-ended antenna. However, the push-pull PAs don't see identical impedances in such designs due to unwanted coupling between the various traces of the balun. Besides, the final circuit in Fig. 1 needs additional

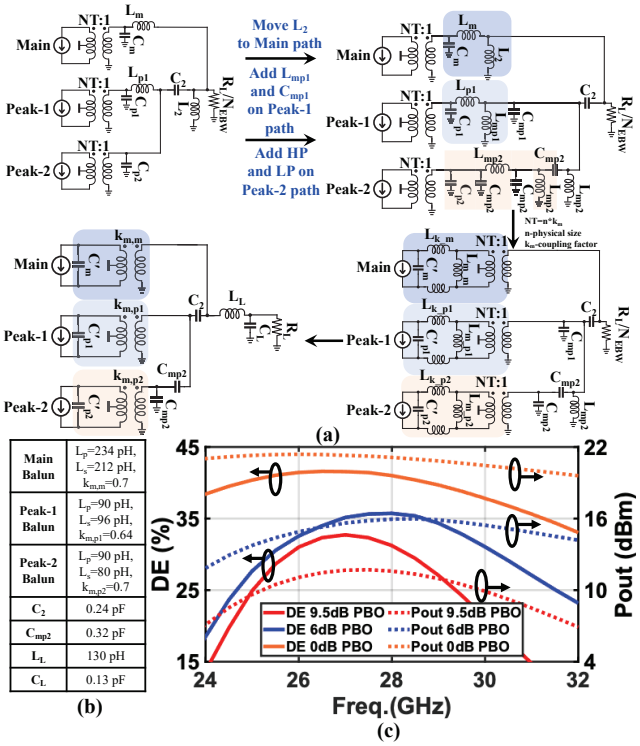

Fig. 3. (a) Procedure to design the proposed balun-first 3-way Doherty, (b) components' value, and (c) DE and output power across frequency.

RF chokes to supply DC voltages to the main and peak-1 PA, increasing the complexity of the circuit. To mitigate these issues, the output balun is split into three baluns and repositioned to the drain of the PAs [1].

Figure 3a illustrates the developing steps for designing a balun-first 3-way Doherty combiner. First, L_2 is moved to the main path. Likewise, L_{mp1}/C_{mp1} are added to the peak-1 path. Also, LP/HP models are added to the peak-2 path. Next, C_m, L_m, and L_2 are repositioned to the drain side of the main PA. Similarly, C_{p1}, L_{p1}, L_{mp1}, C_{p2}, C_{mp2}, L_{mp2}, and L_{mp2} are relocated to the drain side of peak-1/peak-2 PA. Afterward, the ideal transformer, magnetizing (L_m), and leakage (L_k) inductance are superseded with practical balun transformers with coupling factors of $k_{m,m}/k_{m,p1}/k_{m,p2}$. Eventually, an L-match (L_L and C_L) is utilized to transform R_L/N_{EBW} to R_L. The final circuit is compact, with only one inductor, four capacitors, and three baluns whose values are shown in the Fig. 3b. The baluns' turn ratio (NT), C_{mp1}, and L_{mp2} are design parameters that can be adjusted. C_{mp1} and L_{mp2} are chosen to resonate at the desired operational frequency. Additionally, single-turn baluns are exploited to achieve higher self-resonance. This arrangement demands that the NT becomes 0.67 to obtain a similar physical size (n) for the balun's primary (L_p) and secondary (L_s) inductors, making them easier to implement. The simulations with an ideal PA model, EM model of the proposed 3-way Doherty combiner, and capacitors with a quality factor (Q_C) of 25 provide drain efficiency (DE) greater than 15/20/37 % at 9.5/6/0 dB PBO across the 24-to-30 GHz band (Fig. 3c).

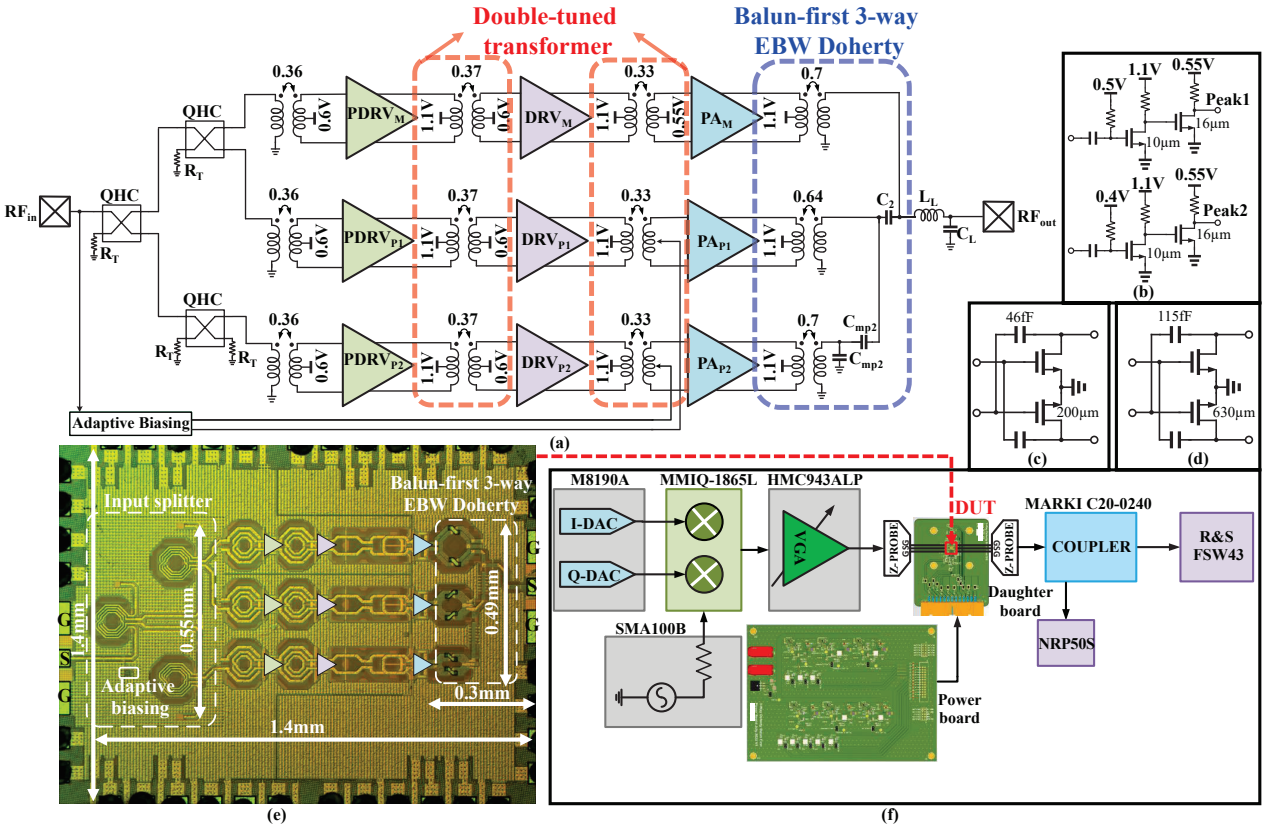

Fig. 4. (a) Top-level of the proposed PA, (b) a detailed schematic of adaptive biasing, (c) PDRV/DRV with a bias of 0.6 V, (d) PA with a bias of 0.55 V, (e) die micrograph of the proposed balun-first 3-way Doherty PA, and (f) measurement setup.

III. Circuit Implementation

Figure 4a depicts a detailed schematic of the proposed PA. The phase advance of 90° and 180° for the 3-way Doherty PA is generated using three quadrature hybrid couplers (QHCs) which also provide wideband input matching. Each branch (main/peak-1/peak-2) consists of an input balun, pre-driver (PDRV), inter-stage matching, driver (DRV), inter-stage matching, and a PA. The required power gain is achieved with a single-supply, three-stage neutralized common source PA (PDRV/DRV/PA in Fig. 4c/d using a bias of 0.6 V and 0.55 V) but at the expense of lower power-added efficiency (PAE). The inter-stage matching utilizes a double-tuned transformer network to obtain wideband matching. Furthermore, the biases of the peak PAs are modulated by using turn-on voltage of 0.5 V and 0.4 V in the adaptive biasing circuits to perform Doherty load modulation (Fig. 4b).

IV. Measurement Results

The proposed PA is fabricated in 40 nm bulk CMOS technology (Fig. 4e). The core area of the proposed balun-first 3-way Doherty is $1.4 \times 0.55\,\text{mm}^2$. Figure 4f shows the measurement setup. The small-signal s-parameters measurement results of the chip show that the proposed PA achieves more than 5 GHz 3 dB S21 bandwidth while S11/S12 are less than −10/−50 dB over a 23-to-28 GHz band (See Fig. 5a). Figure 5b indicates that the proposed PA achieves more than 20 dBm peak output power and a DE of better than 10 %/15 %/22 %/33 % at 12 dB/9.5 dB/6 dB/0 dB across the 24-to-30 GHz band. Likewise, Fig. 5c exhibits the measured DE and gain versus output power across the 25-to-27 GHz band, indicating active load modulation over the 25-to-26 GHz band. Note that the operational frequency is limited due to the high impedance transformation ratio required by the interstage between DRV and PA. Figure 6a exhibits 9.8 dBm/15 % average output power/DE are measured for a 4.8 Gb/s OFDM 64-QAM signal with 9.6 dB PAPR. Its EVM/ACLR are −23.5 dB/−29.5 dBc, respectively. Furthermore, the spectral purity and constellation of a 400 MHz OFDM 64-QAM signal is measured at 26, 25, and 27 GHz with EVM/ACLR of −24.9 dB/−28.9 dBc, −24.1 dB/−30.7 dBc and −25.4 dB/−30 dBc which are illustrated in Fig. 6b/c/d. The performance of the proposed balun-first 3-way Doherty PA is summarized in Table 1 and compared to that of the prior art. It indicates that our compact single-supply three-stage mm-wave front-end, which operates over the 24-to-30 GHz band without using any digital pre-distortion can handle 4.8 Gb/s while delivering more than 20 dBm/16 dB/33 % peak output power/power gain/DE, respectively.

V. Conclusion

This work proposes a single-supply three-stage balun-first mm-wave 3-way Doherty PA with required bias voltages. Implemented in 40 nm CMOS with a core area of

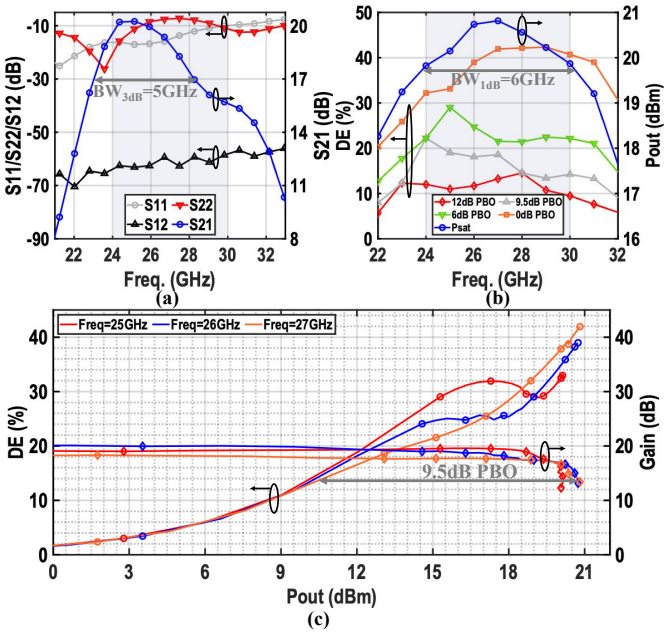

Fig. 5. (a) Small-signal S-parameters measurement results, (c) peak output power and DE across frequency at 12 dB PBO, 9.5 dB PBO, 6 dB PBO, full power, and (c) DE/gain versus output power.

Table 1. Performance summary and comparison to prior art

Specifications	This Work	Z.Ma ISSCC'22 [1]	X.Zhang RFIC'22 [2]	Pashaeifar ASSCC'21 [6]	Huang ISSCC'21 [3]
Architecture	Balun-first 3-way Parallel Doherty PA	3-way Parallel Series Doherty PA	Coupled-inductor based 3-way Doherty PA	2-step impedance inversion series Doherty PA	Continuous Coupler Doherty PA
PA structure	3-stage PAs	2-stage PAs	2-stage PAs	2-stage PAs	2-stage PAs
Technology	40 nm CMOS	55 nm CMOS	45 nm SOI	40 nm CMOS	45 nm SOI
Supply	1.1 V	2.4 V, 1.2 V*	1.8 V, 1 V	1.8 V, 0.9 V	2 V, 1 V
Freq. (GHz)	24-30	28	38	24 to 32	26 to 60
Core Area (mm^2)	0.77	0.54	1.4	0.37	0.62
Gain (dB)	20 (26 GHz)	16.1	15	17.4	15.5*
P_{sat} (dBm)	20.7 (26 GHz)	25.5	18.9	20.4	22
DE_{sat}/PAE_{sat} (%)	39/22.3 (26 GHz)	32.5/25.2	31+/23.3	46+/38.2	NA/40.5
DE_{6dB}/PAE_{6dB} (%)	24.7/11.7 (26 GHz)	25.4/20.4	20+/17.1	39+/34	NA/32.5
$DE_{9.5dB}/PAE_{9.5dB}$ (%)	18.1/7 (26 GHz)	21+/17	17+/ 13.7	25+/20*	NA/15*
DE_{12dB}/PAE_{12dB} (%)	11.7/4.2 (26 GHz)	18.2/14.2	15*/10+	10+/10*	NA/10*
Modulation Scheme	64/64/256/1024 QAM OFDM (26 GHz)	64 QAM	64 QAM OFDM	64 QAM OFDM	64 QAM
Data rate (Gb/s)	4.8/2.4/1.6/0.5	1.5#	0.6	0.6	3
Modulation BW (MHz)	800/400/200/50	250	100	100	500
EVM_{rms} (dB)	-23.5/-24.9/-26.8/-30	-25.2	-25	-24	-25
ACLR (dBc)	-29.5/-28.9/-29.9/-36	-27	-26.5*	-27.7	-28.8
P_{avg} (dBm)	9.8/9.4/9.3/8.6	17.7	11.3	9.35	13.4
PAE_{avg} (%)	15/14/13/12 (DE)	17.5	14.7	16.4	24.8
DPD	No	No	No	No	No

#limited by equipment. *Graphically estimated. +Nominal voltage of the technology.

0.77 mm^2, the realized front-end at 26 GHz exhibits a power gain of 20 dB, a peak power of 20.7 dBm, and a DE of 39 %/24.7 %/18.1 % at 0 dB/6 dB/9.5 dB PBO. It achieves EVM/ACLR of −24.9 dB/−28.9 dBc for a 400 MHz 64-OFDM signal with 9.4 dBm average output power and a 14 % average DE, making it an excellent candidate to exploit in 5G mm-wave TXs.

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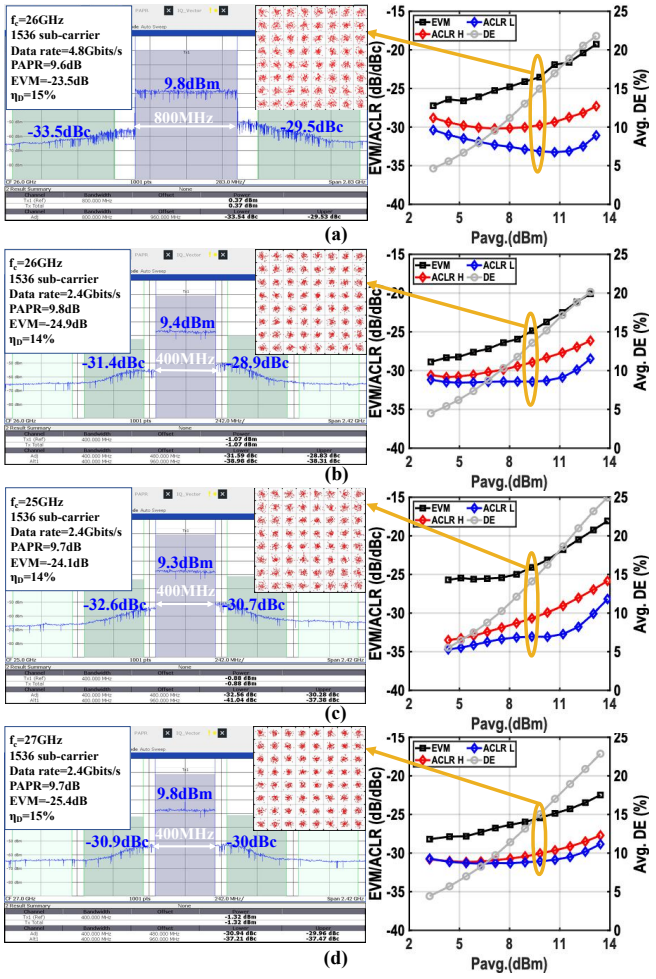

Fig. 6. (a) An OFDM 800 MHz 64-QAM at 26 GHz, (b) an OFDM 400 MHz 64-QAM at 26 GHz, (c) 25 GHz, and (d) 27 GHz measurement results.

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