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Electrostatic uniformity and two-dimensional quantum dot arrays in silicon and germanium

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DOI
10.4233/uuid:15bb07d7-83bf-40f5-ae62-1dff49dec7ce

Publication date
2024

Document Version
Final published version

Citation (APA)
Meyer, M. (2024). *Electrostatic uniformity and two-dimensional quantum dot arrays in silicon and germanium*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:15bb07d7-83bf-40f5-ae62-1dff49dec7ce

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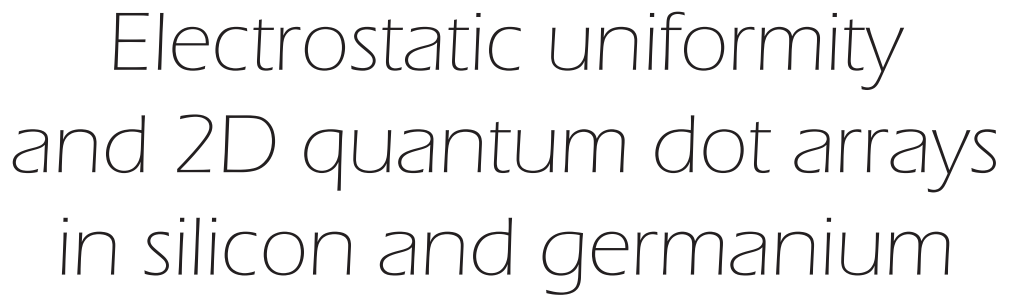
Electrostatic uniformity
and 2D quantum dot arrays
in silicon and germanium

Marcel Meyer

ELECTROSTATIC UNIFORMITY AND TWO-DIMENSIONAL QUANTUM DOT ARRAYS IN SILICON AND GERMANIUM

ELECTROSTATIC UNIFORMITY AND TWO-DIMENSIONAL QUANTUM DOT ARRAYS IN SILICON AND GERMANIUM

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus, Prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on
Tuesday, 18 June 2024 at 10:00 o'clock

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Printed by: Gildeprint - www.gildeprint.nl

Front & Back: Stylized charge stability diagram.

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ISBN 978-94-6384-599-1

An electronic version of this dissertation is available at
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Above all, don’t fear difficult moments.
The best comes from them.

Rita Levi-Montalcini

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1

Introduction

"*As soon as an Analytical Engine exists, it will necessarily guide the future course of science.*" [1] This is what Charles Babbage wrote in 1864. And he was right! Today he is considered a thought father of the computer and scientific research without the help of computers has become nearly unimaginable. For instance, computers enable the storing and processing of huge amounts of data which played a key role in the experimental discovery of the Higgs particle [2]–[5]. Also, for scientists of many fields computer simulations became a fundamental tool. For example, weather simulations now allow us to attribute specific extreme weather events to climate change [6]. Furthermore, many experimental undertakings, including the exploration of Mars by the Mars rover [7], are computer-controlled, and the internet – a network of computers – allows for rapid international scientific communication and exchange.

While computers help to push the boundaries of scientific knowledge, we run into their limitations, too, especially at the scale of the tiny, for systems governed by the laws of quantum mechanics. For instance, the best computational simulations have not yet allowed us to accurately model the underlying mechanism of nitrogen fixation in microorganisms [8], a fundamental process in the biogeochemical nitrogen cycle [9]. The quantum-mechanical nature of the reaction renders this problem intractable on a "classical" computer. Yet, there is reason for optimism. New forms of computing are proposed and under development. For example, computing inspired by the structure of the human brain, artificial neural networks [10] and neuromorphic computing [11], recently received growing attention [12] and promise to impact multiple areas of science [13], [14]. Another fundamentally different type of computer, a computer that might enlighten the processes of nitrogen fixation in microorganisms [8], was suggested by Richard Feynman who realized [15]: "*... [N]ature isn't classical, dammit, and if you want to make a simulation of nature, you'd better make it quantum mechanical ...*". But how could we make it quantum mechanical? What could a quantum computer look like?

1.1. QUANTUM BITS AND QUANTUM COMPUTING

Digital quantum computing is a concept of quantum computing based on the theory of logical circuits which conventional computing is based on [16]. The fundamental building block of such a digital quantum computer is a quantum bit (qubit). Analogous to the classical bit in conventional computing which is described by

$$b \in [0,1]\,, \tag{1.1}$$

a qubit is a quantum-mechanical two-level system with eigenstates $|0\rangle$ and $|1\rangle$. However, in contrast to a classical bit, the physics of quantum mechanics determines the states that a qubit can be in. A qubit can be in a superposition state of the 0 and 1 state. Generally, a qubit state is described by two real-valued coefficients c_i and a phase ϕ:

$$\left|\psi\right\rangle = c_0\,|0\rangle + c_1 e^{-i\phi}\,|1\rangle\,. \tag{1.2}$$

In this notation, the norm $c_1^2 + c_2^2 = 1$ is widely used. Neither a single bit nore a single qubit do allow for meaningful calculations yet, this requires multiple bits or qubits. A classical bit register of N bits can represent 2^N states of the form:

$$\mathbf{b} = (b_1, b_2, \ldots, b_N)\,. \tag{1.3}$$

Analogously, a qubit register of N qubits has 2^N eigenstates. However, in contrast to the bit string, they can exist in superposition and the general state of a qubit register is described by:

$$\left|\psi\right\rangle = \sum_{i_1=0}^{1}\sum_{i_2=0}^{1}\cdots\sum_{i_N=0}^{1} c_{i_1,i_2,\ldots,i_N} e^{-i\phi_{i_1,i_2,\ldots,i_N}} \left|i_1, i_2, \ldots, i_N\right\rangle . \tag{1.4}$$

Thus, while a classical bit-register can represent 2^N different states (000..00, 000..01, 000..10, ...), a single quantum bit register state is described by $2^N - 1$ complex numbers $c_{i_1,i_2,\ldots,i_N} e^{-i\phi_{i_1,i_2,\ldots,i_N}}$. Generally, a quantum register state is not separable. This means it can not always be written as a tensor product $\bigotimes_m \left|\psi_m\right\rangle$ of single-qubit states $\left|\psi_m\right\rangle = \sum_{i_m=0}^{1} c'_{i_m} e^{-i\phi'_{i_m}} \left|i_m\right\rangle$. When the state is inseparable, the quantum register is said to be entangled.

Entanglement and superposition are effects that enrich the complexity of systems governed by the rules of quantum mechanics. Therefore, one can imagine that – if they could be harnessed – they could provide a source for exponentially increased computing capabilities. For instance, when bringing a quantum register into a superposition state consecutive quantum operations will act on all its eigenstates. Thus, in a single run, an algorithm can be applied to multiple classical inputs (corresponding to the eigenstates), providing a quantum parallelization.

Yet, there is a catch. The outcome of the quantum algorithm has to be extracted by performing measurements to be further processed or displayed. These measurements have a classical output state. Thus, the state $\left|\psi\right\rangle$ is reduced to a bit register state **b** which probabilistically depends on the coefficients describing the quantum register state. Additionally, the quantum register itself collapses to the corresponding eigenstate $\left|i_1, i_2, \ldots, i_N\right\rangle$ upon measurement. Therefore, at first sight, the advantage of quantum parallelism is not accessible. However, for specific problems, quantum algorithms with a measurable output have been invented including simulation, number-theoretic, and optimization algorithms [17]. For instance, quantum algorithms might become a tool to address problems in computational chemistry that cannot be solved on regular computers [8] or speed up processes in drug development [18].

Thus, how can a quantum computer be built? To provide guidance for this question, in 2000 David DiVincenco published five requirements [19] which state (rephrased) that one must have:

1. a scalable physical two-level system that serves as a qubit
2. a method to initialize registers of qubits in a well-defined state
3. coherence times that significantly exceed the gate operation times
4. universal single and two-qubit gates
5. the ability to read out a qubit's state

1

1.2. QUANTUM COMPUTING WITH SPIN QUBITS

The spin states of an electron or hole form a two-level system that is governed by the laws of quantum mechanics and thus present a natural candidate for implementing a qubit. A single electron can be isolated in a semiconductor quantum dot, a small chargeable island with clear energetic separation between states of different electron counts. Such quantum dots can be created in metal-oxide-semiconductor (MOS) structures which have strong similarities with MOS field effect transistors (FETs). As MOSFET-based classical computing technology is highly scalable, it is argued that this promises scalability for quantum dot spin qubits as well. Also considering the other DiVincenzo criteria, spin qubits are an attractive candidate to realize a quantum computer. Coherence times of spin qubits exceeding single qubit gate operation times by more than 20,000 have been reported [20][1], high fidelity initialization [21]–[23] and readout [24]–[26] are possible, and universal single [20], [27], [28] and two-qubit [29]–[32] gates of high fidelity have been demonstrated.

While all five DiVincenzo criteria are fulfilled – more or less[2] – it is the word *scalable* in the first criterion that still poses numerous challenges to be overcome before a spin qubit quantum computer can be built that can solve practically relevant problems unsolvable on a classical computer:

- The characteristics of spin qubits vary inside and across devices requiring individually tuned voltages and control sequences for each qubit. How these variations can be reduced significantly to achieve high **uniformity** in spin qubit properties presents a challenge that needs to be mastered before large high-density qubit arrays can be realized.
- With a growing qubit count, **simultaneous operation** at high fidelity becomes a necessity to stay within the qubit coherence times and to avoid overheads in computation time that get out of hand. To achieve this, crosstalk effects between qubits need to be reduced or compensated for [33].
- Achieving the coherence and operational fidelities required for practical (universal) quantum computing through optimizing physical qubit error rates is thought to be impossible. Instead, the idea is to combine multiple physical qubits into a single logical qubit to which error correction protocols are applied. Quantum error correction codes that rely on **two-dimensional interconnected quantum bits**, such as the surface code [34], are among the most promising. However, realizing such arrays is challenged by the finite room on a chip to route control voltages while still maintaining individual qubit(-pair) addressability at low error rates.
- Quantum error correction protocols require that a significant amount of physical qubits can be measured repeatedly with a high repetition rate. Considering the large numbers of physical qubits required for useful universal quantum computing, a **capable readout mechanism** that integrates with the densely intercon-

[1] Derived from the Rabi frequency f_R = 3.9 MHz and Carr-Purcell-Meiboom-Gill (CPMG) coherence time T_2^{CPMG} = 3.1 ms (for 1024 π pulses): $f_R T_2^{CPMG} \approx 23,800$ [20]

[2] For instance, the fidelities of initialization, operation, and readout need to be further increased significantly.

nected qubit array and provides high-fidelity readout is demanded. This is a challenge as current techniques often rely on sensing quantum dots [35] connected to large-footprint charge reservoirs that cannot be placed inside a dense array. Also, a scalable initialization mechanism is required. However, if a capable readout mechanism is found it might be possible to utilize it for initialization, too [25].

- Quantum states are extremely fragile. Therefore semiconductor spin qubits are placed in dilution refrigerators capable of achieving millikelvin temperatures. However, reaching these temperatures is extremely energy-consuming, and thus current refrigerators only provide microwatts of cooling power at millikelvin temperatures [36], [37]. Consequently, a sophisticated **heat management** is required. Currently, most control electronics are placed outside the fridge from where they are directly wired to the cooled-down quantum chip. This approach, utilizing individual control lines per qubit, challenges scalability. On-chip and in-fridge control electronics could contribute to overcoming this challenge but need to be optimized for low-power dissipation [38]. A better understanding of heat flows in quantum devices is required and it might be necessary to increase the operation temperature of spin qubits to gain higher cooling powers [39]–[42].

1.3. WHAT CAN BE LEARNED FROM FLASH MEMORY

When working on a problem it can be beneficial to get inspiration from other areas of engineering, research, or from nature itself. There are similarities between the problems that are faced in quantum computing research today and the challenges engineers and researchers working on integrated circuits for classical computing had to overcome.

Today we often take it for granted that there exist SD cards or USB sticks with up to terabyte storage capacity [43][3], but developing the underlying technology came with considerable hurdles. Before 1970 a memory providing fast access, highly scalable capacities, and continued storage when disconnected from power (non-volatility)[4] was not invented yet. This changed during the 1970s with the development of electrically erasable programmable read-only memory (EEPROM) [44] and led to the invention of flash memory in 1984 by Fujio Masuoka [45]. Flash memory builds – among others – upon two essential ideas [46]:

1. A crossbar array of vertical and horizontal control lines (word and bit lines) provides a selection mechanism of single cells in a two-dimensional grid.

2. In a MOSFET a floating gate can be positioned in the oxide layer between the semiconductor and gate electrode. In such a structure, under large gate voltages charges can tunnel through the oxide to the floating gate. There they remain, even when the voltage is removed, and change the MOSFET threshold voltage.

The role of these two ideas is illustrated in Fig. 1.1. In flash memory, information is stored in the individual threshold voltages of floating gate FETs. For instance, a high

[3]Although, USB sticks are seeming to disappear more and more in favor of cloud storage solutions.
[4]while being reprogrammable and economic in production

1

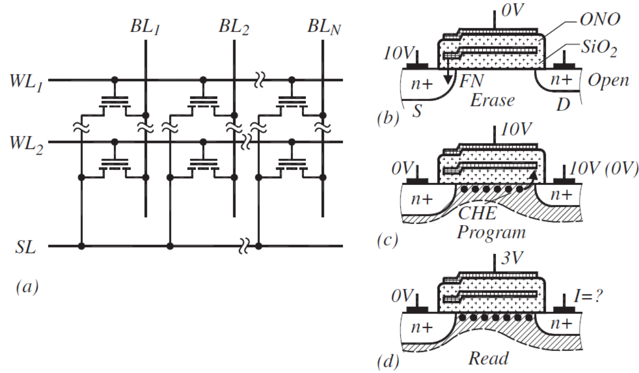

Figure 1.1: **Flash memory architecture. (a)** Scheme of electrical interconnects. Word lines WL_i and bit lines BL_i and a global source line SL are connected to the gate, drain, and source contact of floating gate FETs which are arranged in a 2D grid. **(b)-(d)** Cross-section of floating gate FETs illustrating the erase, program, and read process, respectively. **(b)** A voltage difference of 10 V applied across the source S and gate contact induces Fowler-Nordheim (FN) tunneling of electrons from the floating electrode to the source contact. This lowers the transistor threshold voltage. **(c)** A gate voltage of 10 V is applied and a high current is induced in the channel causing the injection of channel hot electrons (CHE) into the floating electrode. This increases the threshold voltage. **(d)** Probing the channel conductivity at moderate gate voltage (3 V) reveals the stored bit. Detection of (no) current corresponds to a logical (1) 0. Note that the figure only shows one specific variant of flash memory: a NOR architecture with EPROM tunnel oxide cells (ETOX). Figure reproduced from ref [46] page 353 with permission from John Wiley & Sons, Incorporated.

threshold voltage could correspond to a logical 1 and a low threshold voltage to a logical 0.

The floating gate FETs are arranged in a grid and connected to a crossbar array of control lines (Fig. 1.1.a) allowing for random access to all array sites. As an example, to read the bit stored in the upper left floating gate FET a gate voltage is applied to line WL_1 (also see Fig. 1.1.d). This gate voltage is chosen to lie in between the threshold voltages decoding a 1 or 0. Therefore, when a source drain bias is applied across SL and BL_1, the state of the upper left bit can be inferred from the presence or absence of a current flowing through the transistor.

Fig. 1.1.b and c show how bits can be erased (set to 0) and programmed (set to 1), respectively. To erase a memory bit a stress voltage, for instance 10 V, is applied to the source contact (S) upon which electrons will tunnel from the floating gate through the oxide to the source contact (Fig. 1.1.b)[5]. In contrast, to program a memory bit 10V is applied to the gate electrode and drain contact (D) to inject electrons into the floating gate via hot carrier injection (Fig. 1.1.c). The removal or addition of electrons from or to the floating gate shifts the threshold voltage of the transistor such that the stored bit is set to 0 or 1, respectively.

The crossbar arrangement of interconnects and the electrical tunability of threshold voltages lie at the heart of high-capacity flash drives but they also could play an impor-

[5]This erase process cannot be applied to individual floating gate FETs. When 10 V are applied to the SL control line the full array is erased or more colloquially the array is "flashed".

tant role in semiconductor spin qubits. While crossbar interconnects provide random access to the stored information in flash memory, in this work they enable the control over an unprecedented count of 16 quantum dots with odd charge occupation in a dense array. Furthermore, in the second half of this thesis, it is shown that stress voltages not only can shift FET threshold voltages but also allow to increase the uniformity of voltage characteristics in quantum dot arrays. This is demonstrated by reaching single electron occupation at equal plunger gate voltages in a 2 × 2 quantum dot array.

1.4. THESIS OUTLINE

The following chapters are structured as follows:

- **Chapter 2** provides a discussion of the experimental methods and theoretical background underlying this work. It presents the heterostructures utilized in this thesis, discusses mechanisms that limit the electrical uniformity in quantum dot devices, and provides details on the tuning and characterization of quantum dot arrays including a discussion on fitting the polarization of detuned double quantum dots.
- In **Chapter 3** a 2 × 2 quantum dot array in a Si/SiGe heterostructure is presented. Single electron occupation is reached in all quantum dots simultaneously and control over interdot tunnel couplings is demonstrated.
- The quantum dot array of chapter 3 comes with individual control of all plunger and barrier gate voltages. A more scalable approach based on shared plunger and barrier gate electrodes is the topic of **chapter 4**. In this chapter a 4 × 4 quantum dot array in Ge/SiGe is presented. It is shown that an odd charge occupancy of either one or three holes can be reached for all 16 quantum dots simultaneously and that a double barrier architecture allows for selective control over interdot tunnel couplings.
- Further scaling of shared gate arrays such as the one presented in chapter 4 requires improvements of the electrical uniformity in quantum dot devices. In **chapter 5** a new method to increase the electrical uniformity in quantum dot devices is presented and characterized. The method, which is purely based on stress voltage sequences, is demonstrated by equalizing the pinch-off voltages of four plunger gates in a linear array.
- In **chapter 6** the stress voltage tuning method from chapter 5 is utilized in quantum dot arrays to demonstrate control over the plunger gate voltages that are required to reach single electron occupation. It is shown that a 2 × 2 array identical to the one from chapter 3 with 1 V applied to all plunger gates can be tuned from irregular charge occupancy to single electron occupation without changing any other gate voltage.
- **Chapter 7** concludes this thesis by placing the contributions on two-dimensional arrays and voltage uniformity control into the context of recent developments in the field of semiconductor spin qubits and by providing an outlook on the near

and more distant future for stress voltage tuning and dense two-dimensional spin qubit arrays.

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2

THEORETICAL AND EXPERIMENTAL BACKGROUND

Section 2.2 of this chapter has been published as D. Degli Esposti, L. E. A. Stehouwer, Ö. Gül, N. Samkharadze, C. Déprez, M. Meyer, I. N. Meijer, L. Tryputen, S. Karwal, M. Botifoll, J. Arbiol, S. V. Amitonov, L. M. K. Vandersypen, A. Sammak, M. Veldhorst, and G. Scappucci, Low disorder and high valley splitting in silicon, *npj Quantum Inf* **2024** 10 (32) [1].

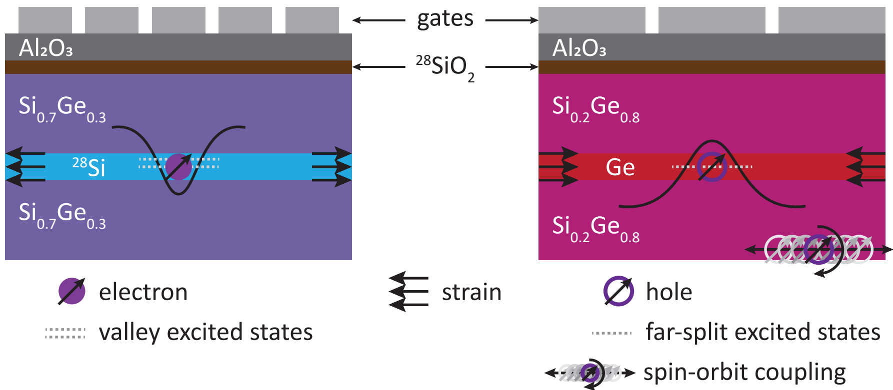

Figure 2.1: **Heterostructure schematics** Cross-sectional drawing of the Si/SiGe and Ge/SiGe material stacks of the devices in this thesis. The direction of the strain in the quantum well, the spin-carrying charge, the valley splitting, and the spin-orbit coupling are indicated by pictograms explained in the legend below. Figure inspired by ref [5].

Semiconductor spin qubits are defined in purposely designed semiconductor heterostructures on which metallic gate electrodes are deposited. Applying the right set of voltages to these gate electrodes – "tuning the device" – will isolate single electrons or holes which then can be utilized as spin qubits. This chapter presents the experimental and theoretical background on the heterostructures employed in this thesis work, the imperfections of quantum dot devices, and the tuning and characterization of quantum dot arrays.

2.1. MATERIALS FOR GATE-DEFINED QUANTUM DOTS

The heterostructures underlying the works presented in this thesis are based on silicon (Si), germanium (Ge), and silicon-germanium alloys Si_xGe_{1-x} with x the stoichiometric concentration of silicon (or SiGe in short notation). Specifically, the devices of chapter 3, chapter 5, and chapter 6 are fabricated on a $Si_{0.7}Ge_{0.3}/^{28}Si/Si_{0.7}Ge_{0.3}$ (Si/SiGe) stack [1]–[3] and the devices in chapter 5 section 5.10 as well as in chapter 4 are based on a $Si_{0.2}Ge_{0.8}/Ge/Si_{0.2}Ge_{0.8}$ (Ge/SiGe) stack [4]. A schematic representation of both systems is provided in Fig. 2.1.

High-quality heterostructures are fundamental in the development of scalable quantum dot spin qubit arrays for quantum computing. Ideally, they should provide quantum wells with high electrical uniformity, low noise levels, and a non-degenerate ground state that energetically is sufficiently separated from the first excited state. Considering these requirements, while not perfect, both Si/SiGe and Ge/SiGe devices positioned themself as highly promising candidates for scalable spin qubit processors.

ELECTRICAL UNIFORMITY

Variations in the electrostatic potential of spin qubit devices are commonly observed [6]–[8]. In devices designed for only a few qubits, these can be compensated for by indi-

vidualized control voltages. However, when scaling to large numbers of qubits, a high electrical uniformity significantly eases the operation and is likely crucial [9], [10].

A fast and robust way to characterize heterostructures is provided by Hall effect measurements from which the maximum achievable mobility and percolation density can be extracted. These serve as an indicator of electrical uniformity. Both Si/SiGe and Ge/SiGe come with (steadily improving) high mobilities μ and low percolation densities $n_\mathrm{p}/p_\mathrm{p}$ with:

- $\mu_\mathrm{Si/SiGe} \approx 10^5\ \mathrm{cm^2/Vs}$ and $n_\mathrm{p} \approx 10^{10}\ \mathrm{cm^{-2}}$ in Si/SiGe [1]
- $\mu_\mathrm{Ge/SiGe} \approx 10^6\ \mathrm{cm^2/Vs}$ and $p_\mathrm{p} \approx 10^{10}\ \mathrm{cm^{-2}}$ in Ge/SiGe [11]

at the time of writing. The high mobility and low percolation density, proofing the low disorder landscape, are possible due to the epitaxial uniformity of the quantum well/SiGe spacer interface and the considerable distance of the quantum well from the topmost dielectric layers. The combination of these two characteristics greatly increases mobility and percolation density compared to Si-MOS [12], [13]. Furthermore, careful selection of the $\mathrm{Si}_x\mathrm{Ge}_{1-x}$ alloy composition sets the band offset between the quantum well and SiGe spacer and enables to achieve low strain induced disorder while still providing electron or hole confinement [5].

Quantum dot gate structures are significantly smaller than Hall bars ($\approx 0.1 \times 0.1\ \mu$m vs. $\approx 100 \times 1000\ \mu$m). Still, the charge density in a quantum dot array will be of the same order of magnitude as the above-reported percolation densities. However, the larger surface area of a Hall bar renders mobility and percolation density a more averaged measure of the disorder. Therefore, effective potential fluctuations experienced by quantum dots can differ from those revealed by Hall effect measurements. A discussion on electrical uniformity in quantum dot devices follows in section 2.3 which also details potential physical effects causing the underlying disorder.

NOISE ENVIRONMENT

A quiet noise environment is a prerequisite for the implementation of high-fidelity initialization, manipulation, and readout in quantum devices. Semiconductor spin qubits are predominantly affected by charge noise, describing dynamic fluctuations of the electric field, and nuclear noise, describing dynamic fluctuations of the nuclear spin bath of the host material.

Charge noise couples to the electron or hole spin through exchange coupling (if dependent on the electric field) and spin-orbit interaction. A strong spin-orbit interaction is found in Ge/SiGe. In Si/SiGe, the spin-orbit interaction is significantly lower [5]. However, a micromagnet is commonly added on top of the device to induce an artificial spin-orbit field allowing for fast high-fidelity single qubit gates [14]–[17]. In one-dimensional arrays, these magnets can be designed to suppress magnetic field gradients that lead to charge noise induced dephasing [17], [18]. However, such suppression is significantly more challenging in two-dimensional arrays [19], [20]. Therefore, Si/SiGe and Ge/SiGe low charge noise characteristics are essential.

Charge noise can originate from gate voltage fluctuations but can have its source in the material stack as well. Its noise power spectral density (PSD) often is observed to

follow an inverse frequency trend (PSD $\propto 1/f$), suggesting two-level fluctuators (TLFs) as a dominant noise source [15], [21]. These can reside in the device dielectrics which are known for high charge trap densities [22]–[24]. In Si/SiGe and Ge/SiGe, the dielectrics are separated from the SiGe buffer layer reducing their influence on the quantum well. TLFs also might be present in the semiconductor layers, for instance originating from disorder induced by strain relaxation in the quantum well [3].

Magnetic noise from nuclear spins of the host material can directly couple to the electron or hole spin degree of freedom. Silicon and germanium both exhibit abundant nuclear spin-free isotopes (^{28}Si, ^{30}Si, ^{70}Ge, ^{72}Ge, and ^{74}Ge[1]) [25]. Therefore, decoherence induced by nuclear fluctuations is suppressed. Additionally, silicon quantum wells can be isotopically purified by reducing the amount of ^{29}Si [26]. Also, germanium crystals can be purified [27], [28] promising the development of heterostructures with purified germanium quantum wells.

EXCITED STATES

Low-lying excited states can be detrimental to qubit initialization, readout, and operation as they can induce leakage out of the computational Hilbert space. For instance, the presence of low-lying excited states can lift Pauli spin blockade and thus hamper its use for spin readout [29]. Low-lying excited states originate from insufficient quantum confinement or low-lying valley states. In germanium quantum wells, the degeneracy of the valence band is lifted by confinement and strain resulting in a generous energy gap of $\approx 50-100$ meV between the two topmost states (heavy holes and light holes) [4], [30]. However, in silicon, these two mechanisms only split off four of the six degenerate conduction band valleys. The remaining two-fold degeneracy is lifted by the interplay of the electron wavefunction with the Si/SiGe interface [31], [32] resulting in fluctuating valley splittings of 50-250 μeV [1], [5], [33], [34]. Engineering consistently high valley splittings is one key goal of Si/SiGe heterostructure development. For instance, the incorporation of germanium into the silicon quantum well was proposed and is explored as a means to increase the valley splitting in Si/SiGe heterostructures [35], [36]

SPIN-ORBIT INTERACTION

While spin-orbit interaction can mediate charge noise into decoherence as described above, it can also provide a mechanism for the implementation of fast, low-footprint single qubit rotations. Holes in Ge/SiGe naturally come with strong spin-orbit interaction and applying an on-resonant modulation of a nearby gate voltage allows for high-fidelity single qubit operations [37]. This eliminates the need for multi-micron large structures to induce strong oscillating magnetic fields for electron spin resonance (ESR) [38], [39]. However, the spin-orbit interaction in Ge/SiGe also induces a pronounced g-factor anisotropy with principal axes that can strongly vary from quantum dot to quantum dot [40]. This variation might pose challenges to the scaling towards large numbers of qubits. While this is not of concern in Si/SiGe heterostructures, the intrinsic spin-orbit interaction is not strong enough for sufficiently fast single-qubit rotations, either. As already mentioned, the placement of micro- or nanomagnets can provide a tailored artificial

[1] There is also ^{76}Ge which has a half-life time of 10^{21} years and thus could be considered as stable.

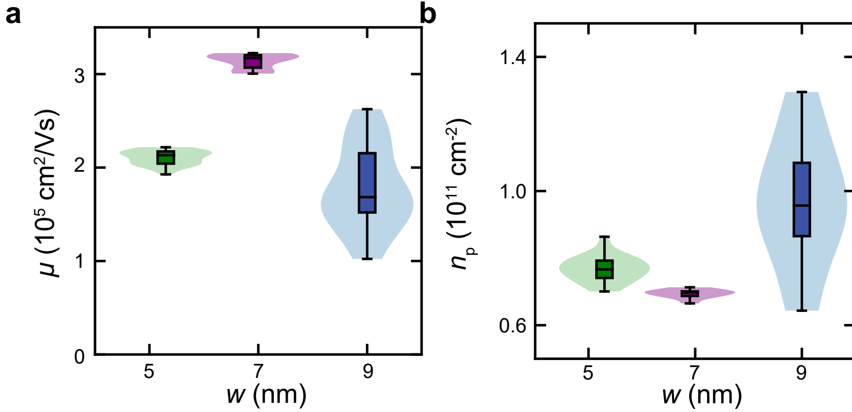

Figure 2.2: **Electrical transport characteristics. a**, **b** Distributions of mobility μ measured at $n = 6\times10^{11}$ cm^{-2} and percolation density n_p for heterostructures featuring quantum wells of different thickness w: 9.0(5) nm (blue, heterostructure A, 16 Hall bars measured and reported in ref. [3]), 6.9(5) nm (purple, heterostructure B, 10 Hall bars), and 5.3(5) nm (green, heterostructure C, 22 Hall bars measured and reported in ref. [3]). Violin plots, quartile box plots, and mode (horizontal line) are shown.

spin-orbit interaction that allows for fast high-fidelity single qubit gates, too [14]–[17]. Beyond that, architectures that do not require (artificial) spin-orbit interaction are explored. For instance, global control schemes do not require individual single qubit rotations [41], [42], and a qubit encoding with single and two-qubit gates solely based on exchange interaction requires neither spin-orbit interaction nor on-chip ESR infrastructure [43].

2.2. Si/SiGe heterostructures in this thesis[2]

The development of Si/SiGe and Ge/SiGe heterostructures is an ongoing process yielding continuous improvements. This is also reflected in the Si/SiGe devices underlying this thesis which are fabricated on two heterostructures, heterostructure A [3] is found in chapter 3 and chapter 5, and heterostructure B is found in chapter 5 section 5.10, and chapter 6. The two heterostructures differ in the thickness of the quantum well and in their dielectric interface. Heterostructure A is grown with a 9 nm and heterostructure B with a 7 nm thick quantum well and while a ≈ 1 – 2 nm thick partially oxidized silicon layer caps the Si/SiGe stack in heterostructure A, the upper SiGe buffer layer in heterostructure B is passivated in dichlorosilane at 500°C.

Improving the uniformity, noise performance, or valley splitting in Si/SiGe often requires careful trade-offs. While some instances of large valley splittings (up to 0.286 ± 0.026 meV) within a wide distribution have been measured in 3 nm ultra-thin quantum wells [44], they also may lead to increased wavefunction overlap with the quantum well interfaces enhancing scattering and reducing mobility [45]. Thicker quantum wells provide higher mobilities. However, too thick quantum wells can exhibit strain release defects which reduce the mobility again [3]. These effects also can be seen when comparing

[2]This section has been published as Degli Esposti et al. [1].

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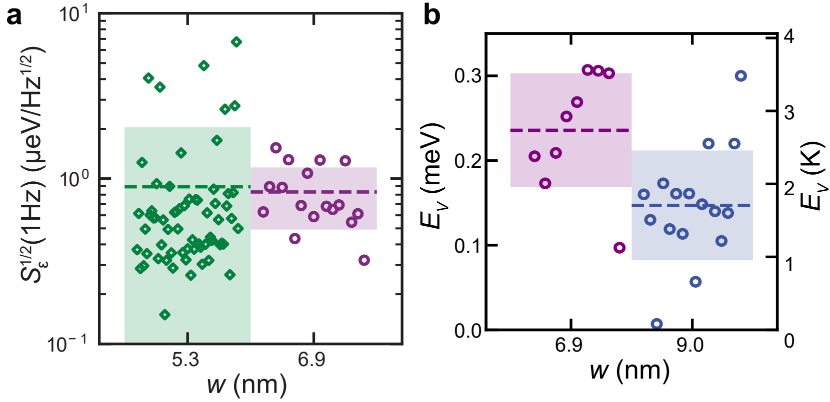

Figure 2.3: **Charge noise and valley splitting measurements.** **a** Experimental scatter plots of charge noise at 1 Hz ($S_{\epsilon}^{1/2}$(1 Hz)) for multiple devices and different electron occupancy. Data from the 6.9(5) nm quantum well (purple, heterostructure B, 2 devices, 17 spectra) is compared to data from the 5.3(5) nm quantum well (green, heterostructure C, 63 spectra, 5 devices, reported in ref. [3]). We compare single-layer devices (diamonds) and multi-layer devices featuring overlapping gate geometry and micromagnets (circles). Dashed lines and shaded areas denote the mean value and two standard deviations. **b** Experimental scatter plots of valley splitting obtained by magnetospectroscopy on complete spin qubit devices. Data from heterostructures with a 6.9(5) nm quantum well (purple, heterostructure B, 9 quantum dots from 2 devices) is compared to data from a 9.0(5) nm quantum well (blue, heterostructure A, 16 quantum dots, 3 devices, from ref. [17]). Dashed lines and shaded areas denote the mean value and two standard deviations.

the mobilities of heterostructures A and B as well as a third heterostructure (C) identical to heterostructure B but with a thinner 5 nm thick quantum well. Fig. 2.2.a shows the mobility and percolation density distribution obtained from at least 10 hall-bar-shaped heterostructure field-effect transistors per heterostructure[3]. The 6.9 nm quantum well performs the best, with a mean mobility at high densities of $\mu = 3.14(8) \times 10^5$ cm^2/Vs and a percolation density of $n_\mathrm{p} = 6.9(1) \times 10^10$ cm^2. The distributions show two notable features: a 50% boost in mobility between the 5.3 nm and 6.9 nm quantum well and a three-fold reduction in the variance of the distribution between the 9.0 nm quantum well and the remaining two. The increase in mobility is attributed to reduced scattering from alloy disorder, as the wave function delocalizes further into the quantum well instead of penetrating into the barrier [46]. The large spread in transport properties of the wider quantum well is attributed to some degree of strain relaxation and associated defects [3]. Comparing heterostructures A-C, the 7 nm quantum well provides the highest mobilities.

While mobility and percolation density serve as indicators for electrical uniformity, low-frequency charge noise measurements conducted utilizing single electron transistors (SETs) can inform about the degree of dynamical disorder. Fig. 2.3.a shows the noise power spectral density at 1 Hz of the 6.9(5) nm (B) and the 5.3(5) nm (C) quantum well obtained by tuning to multiple Coulomb peaks and recording source-drain current traces in two and six devices, respectively. Both heterostructures come without the sil-

[3]The data on heterostructure A is taken from ref. [3]

icon capping layer. Additionally, the devices on the 5.3 nm quantum well are defined by a single layer of gates, whilst the devices on the 6.9 nm quantum well are complete qubit devices featuring three layers of overlapping gates, additional dielectric films in between, and micromagnets. The noise power spectral density in the multi-layer devices (purple) and single-layer devices (green) are similar, with power spectral densities of 0.9(3)) μeV/Hz$^{1/2}$ and 0.9(9) μeV/Hz$^{1/2}$, respectively. Thus both heterostructures are characterized by low mean charge noise values values which are comparable with values reported in the literature [15], [21], [47]. Compared to heterostructure A, the power spectral density at 1 Hz was reduced by nearly one order of magnitude [3].

Lastly, the valley splitting of the heterostructures underlying this thesis is considered. Fig 2.3.b compares the valley splitting of quantum dot devices on the 6.9 nm quantum well (purple, heterostructure B) and on the 9.0 nm quantum well (blue, heterostructure A) studied in ref. [3]. The plotted values are obtained via magnetospectroscopy[48], [49] providing singlet-triplet splittings which are reliable estimates of the valley splitting energies in strongly confined quantum dots [48]–[51][4]. While the dots in all devices measured have the same nominal design and share the same fabrication process, the heterostructures further differ in the passivation of the SiGe top barrier. The heterostructure with the 6.9 nm well is passivated by an amorphous self-terminating Si-rich layer, while the 9.0 nm well has a conventional epitaxial Si cap [2]. Passivation by a self-terminating Si-rich layer yields a more uniform and less noisy semiconductor-dielectric interface, which in turn promotes higher electric fields at the Si/SiGe interface [2], [3]. A statistically significant 60% increase in the mean valley splitting in the 6.9 nm quantum well with an amorphous Si-rich termination is observed, featuring a mean value of 0.24 ± 0.07 meV.

Note that consistently achieving large valley splittings still might be an open challenge as a larger amount of data points from across the corresponding wafers is required to reach a comprehensive conclusion. Speculatively, the tighter vertical confinement within the narrower quantum well [44], coupled with the relatively wide quantum well interface width increases the overlap of the electron wavefunction with Ge atoms in the barrier. This amplifies the effect of random alloy disorder, which is known to increase valley splitting [32], [48]. Similarly, the improved semiconductor dielectric interface facilitates tighter lateral and vertical confinement of the measured quantum dots, which leads to a stronger electric field, contributing to driving the valley splitting [52], [53].

In summary, both heterostructures underlying this thesis work provide high mobilities, low percolation densities, respectable charge noise amplitudes, and respectable valley splittings. Additionally, heterostructure B which succeeded heterostructure A shows simultaneous improvements in all those characteristics achieved by carefully choosing the quantum well thickness and improvements of the semiconductor-dielectric interface [3].

[4]The singlet-triplet splitting of two electrons confined in a quantum dot is determined not only by the valley splitting but also by the orbital splitting, electron-electron interactions (on-site exchange interaction) and the valley-orbit coupling strength. However, for strong confinement and sufficiently low valley-orbit coupling, the singlet-triplet splitting can be approximated by the valley splitting [49].

2.3. IMPERFECTIONS IN THE POTENTIAL LANDSCAPE OF QUANTUM DOTS

Voltages applied to gate electrodes patterned on top of the Si/SiGe and Ge/SiGe material stacks provide confinement and define the quantum dots. This approach provides flexibility as gate structures can be designed freely within the limits of the utilized fabrication process. For instance, gates with large aspect ratios can allow for elongated quantum dots [54], [55]. However, due to their small feature size, quantum dot devices and their fabrication process are very fragile. Consequently, gate design and gate voltage configuration are not the only parameters shaping the potential landscape. Disorder and device imperfections often need to be compensated for by individualized gate voltages for each quantum dot. This challenges the scaling towards devices containing well above tens of coupled quantum dots.

Statistics on the potential variations in quantum dot arrays would be a valuable source of feedback to improve device uniformity. However, gathering such statistics is a time and resource-intensive endeavor as each device needs to be placed in a correspondingly wired dilution refrigerator and needs to be tuned to single-charge occupation. Recently, more focus has been put on efforts to automate the tuning process [56]–[64]. Yet, reliable and repeatable automatic initialization of a given charge state in quantum dot arrays remains a challenge. Until automatic tuning is applied routinely, time-intensive manual tuning is required rendering the gathering of statistics unattractive. Instead, large-scale characterizations of easy-to-measure pinch-off voltages can serve as an estimator of potential uniformity in quantum dot devices [6], [8], [65], [66]. Substantial statistics can be gained by wafer-scale characterizations in cryo-probe stations [8] or through multiplexed arrays of sparse and uncoupled single electron transistors [6], [66].

Alternatively, gate voltages can be extracted from the literature on quantum dot and spin qubit arrays. Fig. 2.4 shows the voltages required to obtain a single electron or hole per quantum dot across four material platforms and multiple research works. In the top panel, each bar shows the average real plunger gate voltage $\overline{V_\text{P}}$ of a (sub)array of N quantum dots, while in the bottom panel the voltage range $[V_\text{P}^- - \overline{V_\text{P}}, V_\text{P}^+ - \overline{V_\text{P}}]$ for which a single electron or hole is present are presented in the same color. Here, V_P^- and V_P^+ are the first and the second charge addition voltage read off directly from charge stability diagrams[5].

For 5 devices and tuning configurations with $N = 2$, the voltage ranges show an overlap in contrast to 14 devices and tuning configurations with $N = 2$ that exhibit no plunger gate voltage that is part of both voltage ranges. For the last data set (Borsoi (2023)) corresponding to chapter 4 with $N = 16$ the ranges of up to 4 quantum dots overlap. Fig. 2.4 also reveals large variations in the average plunger gate voltage $\overline{V_\text{P}}$ in a given material system. For hole quantum dots, no comparison can be carried out due to the limited number of data sets available. Furthermore, the distribution of charging voltages $V^\text{C} = V_\text{P}^+ - V_\text{P}^-$ in SiMOS devices exhibits the largest standard derivation of 144 % relative to its mean value $\overline{V^\text{C}}$. In Si finFETs, Si/SiGe and Ge/SiGe standard derivations of 70 %, 27 %, and 27 % are observed, respectively.

Highly overlapping voltage ranges $[V_\text{P}^-, V_\text{P}^+]$ and uniform charging voltages are de-

[5] For a detailed definition of V_P^- and V_P^+ see chapter 6 section 6.4.

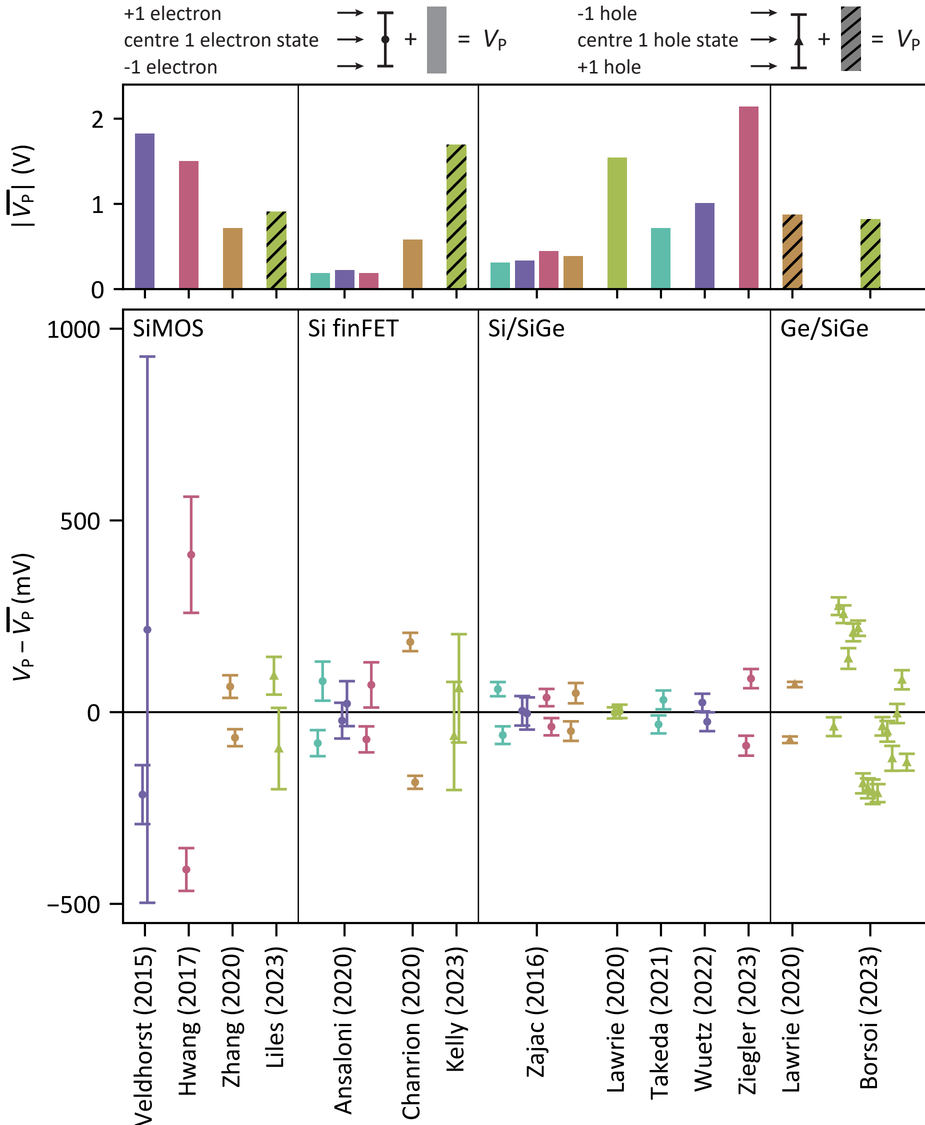

Figure 2.4: **Gate voltage variations in quantum dot devices.** The top panel shows absolute average real plunger gate voltages $|\overline{V_P}|$ for (sub)arrays of N quantum dots extracted from charge stability diagrams from the literature [13], [48], [64], [67]–[75] and chapter 4 of this thesis. The bottom panel shows the corresponding plunger voltage ranges $[V_P^- - \overline{V_P}, V_P^+ - \overline{V_P}]$ for which a single electron or hole is present. Electron device voltages are presented by solid bars in the top panel and a circle marking the center of the one-electron state in the bottom panel. Hole device voltages are presented by shaded bars in the top panel and a triangle marking the center of the one-hole state in the bottom panel. Note that in two references multiple double quantum dot voltage configurations are presented. These are presented separately as indicated by different plot colors.

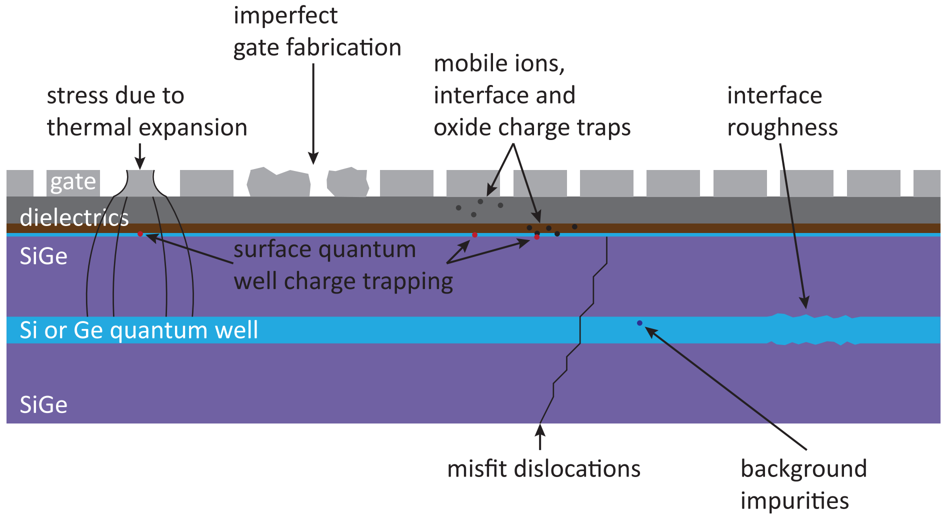

Figure 2.5: **Illustration of device imperfections affecting the potential landscape.** Schematic representation of a heterostructure with a dielectric capping layer and gate electrodes. Multiple imperfections and types of disorder are drawn and labeled. Figure inspired by ref [76].

sirable as they can relax requirements on control electronics or enable the implementation of quantum dot arrays with shared gate voltages easing voltage routing [9], [10]. Fig. 2.4 highlights the need to develop quantum dot devices with more uniform gate voltage characteristics. Generally, a spectrum of factors can contribute to the observed variations in characteristic voltages as illustrated in Fig. 2.5. In the following subsections, these will be discussed.

GATE DESIGN AND GATE SHAPE

The making of a quantum device starts with the design of a gate layout. In current devices, gate structures often are not optimized for regular quantum dot gate voltages. Individual control is prioritized and the required small feature sizes are at the limit of what can be fabricated. Readout signatures such as Pauli spin blockade sensed by a nearby sensing quantum dot require this one to be placed asymmetrically with respect to the corresponding quantum dot pair. Thus, even without any further imperfections present in the devices, non-identical required gate voltage ranges are expected. Furthermore, deviations from the designed gate structure originate from the finite grain size of the deposited metals and other variations common to the fabrication in academic settings [13], [77], [78]. However, utilizing more semiconductor foundry compatible processes promises to improve the gate uniformity [65], [79].

VOLTAGE TUNING METHODOLOGY

Also, the tuning strategy can influence the distribution of gate voltages. Multiple voltage configurations can lead to the same charge occupation and tunnel couplings but with slightly different quantum dot locations and shapes [51]. Cross-capacitive coupling

of each gate to multiple characteristic properties, like quantum dot chemical potentials or tunnel barrier heights, allows for multiple voltage configurations while maintaining charge occupation and tunnel couplings. Virtual gate voltages can compensate for this effect but they are valid for limited voltage ranges only [80], [81]. Their implementation requires the observation of clearly defined and measurable quantum dot parameters. For instance, screening gates can control the confinement and position of multiple quantum dots simultaneously while they are also used to prevent charge accumulation in the direct vicinity of the quantum dot array. This palette of functionalities cannot easily be summarized in a single continuous and measurable quantity as required for virtualization. Additionally, the gate voltage configuration corresponding to a specific system state can depend on the tuning history as will be outlined in more detail in the subsection about surface tunneling below. Overall, this highlights that tuning strategies for more uniform gate voltage configurations might become increasingly relevant when developing larger quantum dot arrays.

GATE ELECTRODE INDUCED STRAIN

The heterostructure and gate stack are composed of various materials that are characterized by a range of thermal expansion coefficients. For instance, the thermal expansion coefficient of silicon is 2.6×10^{-6} 1/K [82] in contrast to Ti/Pd gate electrodes which show a thermal expansion coefficient of $\approx 13 \times 10^{-6}$ 1/K [83]. Quantum dot devices experience significant temperature variations between 10 mK when cooled down for operation and 573 K (300 ^{o}C) during their fabrication. The differences in expansion coefficients lead to material strain that is propagated throughout the heterostructure. For SiMOS devices with thermally oxidized aluminum gates, the strain-induced shift of the conduction band is predicted to be on the order of 10 meV [82]. In a silicon quantum well buried 91 nm deep in SiGe below a Ti/Pd gate stack a strain of 0.03 % was found [84] that following ref [82] would result in a conduction band shift of ≈ 3 meV. These strain-induced alterations of the conduction band are comparable to typical charging energies in quantum dot devices which are on the order of a few meV [58], [70], [85]. Thus they can have a significant effect and even lead to the formation of spurious quantum dots or charge traps. Gate materials with a thermal expansion coefficient closer to the semiconductors are proposed to reduce stress-induced potential fluctuations [82], [86]. Alternatively, the electrode-induced stress could actively be designed to refine the potential landscape of quantum dots [82], [87].

INTERFACE CHARGE TRAPS

Potential fluctuations also originate from charge traps. These are predominantly found in the oxides and oxide interfaces that separate the Si/SiGe material sandwich from the gate stack [22]–[24]. While dependent on fabrication and tuning practices, the density of trapped charges has been estimated to be $\approx 10^{12}/\text{cm}^2$ [23], [88]–[91]. This translates to hundreds of charge traps present in the area occupied by a single quantum dot (≈ 100 nm × 100 nm). As oxide and oxide interface traps also affect the performance of established MOS technology, they have been studied extensively. Measuring the capacitance of a MOS capacitor as a function of bias voltage and frequency (CV-measurement)

established as a routine characterization tool[6] and let to the classification into four types of charge traps [93] as illustrated in Fig. 2.6.a: (1) interface traps, (2) fixed oxide charges, (3) oxide trapped charges, and (4) mobile ionic charge. Interface traps are located at or close to the semiconductor-oxide interface. This allows them to exchange electrons with the semiconductor valence or conduction band when energetically favorable. Fixed oxide charge traps are located close to the semiconductor-oxide interface, too, (up to $\lesssim$ 2.5 nm for Si/SiOx) but cannot exchange electrons with the semiconductor anymore. They are related to oxidation processes during the device fabrication and are positively charged. Oxide-trapped charges are found in the bulk part of the oxide and are attributed to post-oxidation treatments such as ionizing radiation or the application of large voltages (stress voltages). They may also be charged through hot carrier injection or quantum tunneling processes. Mobile ionic charge describes weakly bonded ions such as positively charged hydrogen and sodium which at sufficiently large temperatures become mobile and can redistribute inside the oxide under the force of an electric field.

Controlling the amount of charge traps turns out to be a complex endeavor requiring a good understanding of the underlying physical trapping mechanisms and optimization of device fabrication. Fig. 2.6.b illustrates this complexity by schematically depicting a non-exhaustive selection of potential charge-trapping mechanisms at the SiGe/oxide interface. It is based on the material composition of the devices presented in chapter 4, chapter 5 section 5.10, and chapter 6[7]. For these devices, the SiGe surface was passivated in dichlorosilane at 500 °C [2] before being oxidized in air and during the subsequent atomic layer deposition of aluminum oxide [95], [96]. Increased silicon and oxide concentration at the interface and a germanium pile up directly below indicate the predominant formation of silicon oxide between the SiGe buffer and the aluminum oxide layer [2].

In this silicon oxide layer, a range of mechanisms can lead to the trapping of charge. A few exemplary candidates are:

- Silicon and germanium dangling bonds can emerge close to the semiconductor-oxide interface to relieve strain induced by the mismatch of the SiGe and SiO_2 (average) lattice constant [92], [97]–[99].
- Strain-induced bond length and angle variations might lead to localized charge states [100].
- The rupture of a silicon-oxygen, hydrogen-oxygen, or oxygen-oxygen bond can result in an oxygen atom with an unpaired electron which is prone to trap another electron [99].

The silicon oxide layer is followed by an aluminum oxide layer. This layer and its interface with the silicon oxide can provide further charge traps. Some but not all potential

[6] An introduction to CV-measurements can be found in ref [92].

[7] The oxide-SiGe interfaces of the devices presented in chapter 3 and 5 differ by an additional partially oxidized silicon capping layer between the SiGe and aluminum oxide. However, similar considerations apply.

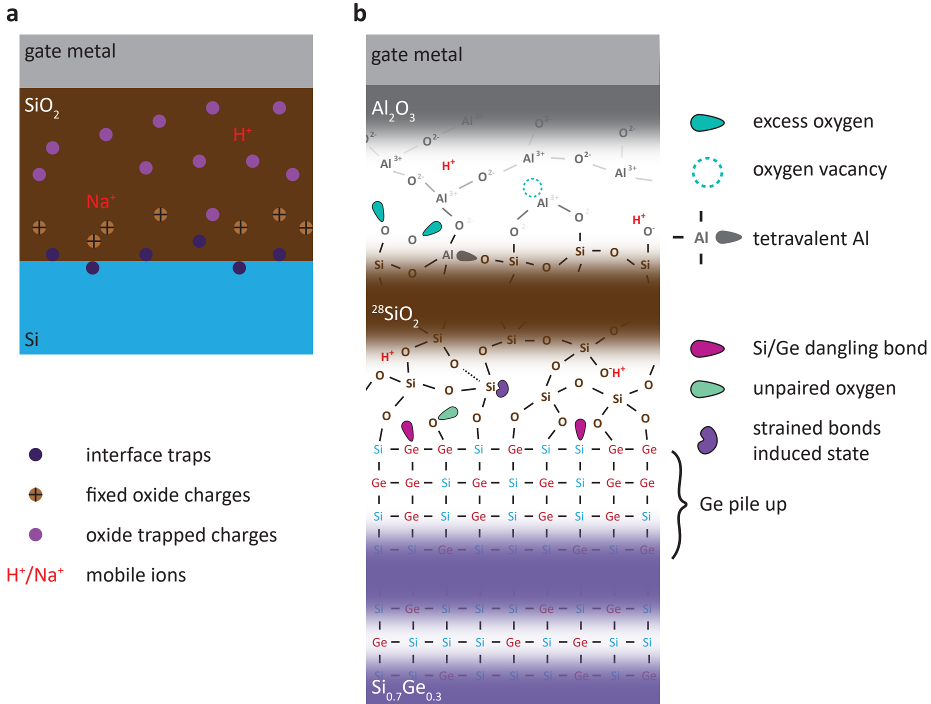

Figure 2.6: **Charge traps in the oxide layers.** **a** Schematic cross-section through a SiMOS capacitor illustrating four types of charge defects in the silicon oxide interface layer. Categorization into these four types originates from a standard developed for capacitance-voltage measurements [93]. **b** Illustration of potential charge trapping mechanisms in the heterostructures utilized in chapter 4, chapter 5 section 5.10, and chapter 6. For each interface, schematic arrangements of atoms and bonds are shown including illustrations of a selection of potential charge trapping mechanisms. Note that the depiction illustrates the complexity of charge-trapping by showing selected mechanisms reported in the literature. However, detailed studies are required to make statements about the SiGe heterostructures in this thesis or other works on quantum dot spin qubits. Panel **a** inspired by ref [93] and panel **b** inspired by ref [94].

mechanisms are:

- To match the structure of silicon dioxide, amorphous aluminum oxide might form in a tetrahedral arrangement exhibiting dangling oxygen bonds that can capture electrons [101]–[103].
- Oxygen vacancies could facilitate electron or hole trapping [104].
- Increased oxygen counts at the silicon oxide-aluminum oxide interface might be the origin of electron accumulation [105].

Note that these examples illustrate the complexity of the charge-trapping in the oxide layers but detailed studies are required to make statements about the exact charge-trapping effects in the SiGe heterostructures of this thesis or other works on quantum dot spin qubits.

FURTHER DISORDER MECHANISMS

While oxide interface defects outnumber defects in the semiconductor stack, a single misfit discoloration or impurity, if localized close to the quantum well, can reshape the quantum dot potential landscape much more drastically. For the heterostructures underlying this thesis, a low oxygen concentration around the quantum well [24] suggests a limited influence of background impurities. Misfit dislocations can induce charge trapping through dangling bonds, strain-induced potential fluctuations, or attraction of impurities that can catch holes or electrons [106]. They are found in the virtual substrate and facilitate the relaxation of strain induced by the silicon-SiGe grading. However, their influence is limited as their density decreases significantly towards the quantum well [1].

Besides misfit dislocations and background impurities, interface roughness at the silicon or germanium quantum well or an interface slightly misaligned with the crystal lattice planes could alter the potential landscape in the quantum well [45], [48], [107].

SURFACE TUNNELING

It was already mentioned that the quantum well background potential also can depend on the tuning history. Measurements of the Hall effect in Si/SiGe and Ge/SiGe heterostructures have revealed a charge tunneling process that increases peak mobility but also gives rise to hysteretic gate voltage characteristics [23], [108]–[111]. Fig. 2.7 schematically depicts the conduction band energy (E_C) and charge density (in blue) in a Si/SiGe heterostructure and illustrates the role of charge tunneling for three distinct gate voltage regimes (A-C). For low to moderate gate voltages (A) the conduction band is pulled below the Fermi energy (E_F). Provided through ohmic contacts, electrons can flow into the Si quantum well and accumulate at its top interface. When the gate voltage is further increased (B) the conduction band at the SiGe-oxide interface also approaches the Fermi energy. If the gate voltage is high enough, electrons can tunnel from the quantum well through the SiGe buffer conduction band barrier to the SiGe-oxide surface. The tunneled electrons then occupy interface charge traps if they provide energetically favorable states within reach. This charge-trapping process can compensate for potential fluctuations which for instance are induced by charged defects located deeper into the

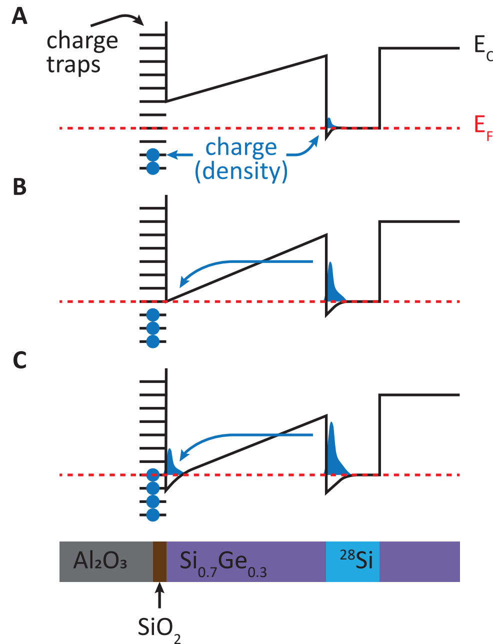

Figure 2.7: **Charge tunneling from the quantum well to the dielectric interface**. A cross-section through a Si/SiGe devices is shown (bottom). The shape of the conduction band energy (E_C) and Fermi level (E_F) in this heterostructure for three regimes (A-C) of gate voltages is drawn above. Interface traps are depicted by horizontal lines and their occupation is indicated by blue circles. The charge density across the material stack is depicted in blue. For low to moderate gate voltages (A) the conduction band is pulled below the Fermi energy and electrons accumulate in the Si quantum well. For increased gate voltages (B) electrons can tunnel from the quantum well through the SiGe buffer as indicated by the blue arrow and occupy interface charge traps. Under the application of even higher gate voltages (C) electrons accumulate directly at the silicon oxide interface. Figure inspired by refs [90], [108], [109].

oxide. Therefore an increased mobility and a concurrent density saturation can be observed [109], [110]. If at this point one would reduce the gate voltage back to the level applied in A, a charge density lower than before would be observed as electrons that are trapped close to the oxide interface cannot tunnel back and thus induce a potential offset in the quantum well. Under the application of even higher gate voltages (C) the SiGe conduction band at the oxide interface drops below the Fermi energy and electrons accumulate directly at the interface. When the mobility threshold is surpassed this can even result in a second conducting channel. All three stages are observed in Ge/SiGe heterostructures, too [90], [111]. Here the application of sufficiently low gate voltages also leads to mobility improvements and hysteretic gate voltage shifts, which are attributed to the tunneling of holes from the quantum well to interface trap states.

COMMENT ON NON-ELECTROSTATIC DISORDER AND NOISE

The discussion above is focused on electrostatic imperfections in quantum dot and spin qubit devices. However, as also discussed in section 2.1, it shall be noted that the static potential landscape is not the only aspect that is impacted by noise and disorder. Dynamic charge fluctuations (charge noise) [15], [21], [112], [113], as well as nuclear magnetic noise [114]–[116], and variations of parameters such as valley splitting [35], [36], [51], [117], [118] and g-tensor [119]–[121] also affect the performance and scalability of spin qubit processors.

2.4. TUNING AND CHARACTERIZATION OF QUANTUM DOT ARRAYS

SINGLE ELECTRON TRANSISTORS

The charge states of the quantum dots presented in this thesis are measured by sensing the conductance through a single electron transistor (SET) that is placed close to the quantum dot array. Each SET is defined by a plunger gate (S) and two barrier gates (B1 and B2). Before forming a SET a starting voltage is applied to the plunger and barrier gates inside the array which is chosen close to the expected value for quantum dot formation (e.g. $\approx 0.5 - 1$ V in the Si/SiGe heterostructures). Then, the voltages on gates S, B1, B2, and gates required to form nearby charge reservoirs are increased simultaneously until a conducting path is obtained. The resulting channel is illustrated in the inset of Fig. 2.8.a. In this state, the device functions like a field effect transistor and decreasing the voltage V_S on gate S will pinch off the conductance channel as shown in Fig. 2.8.a. Next, while continuously sweeping V_S, the voltages V_{B1} and V_{B2} on the barrier gates B1 and B2 are step-wise decreased while V_S is increased until a quantum dot with quantized energy levels forms as depicted in the inset of Fig. 2.8.b. The main pannel of Fig. 2.8.b shows the resulting Coulomb oscillations characteristic for a SET. The regularity of the Coulomb oscillations, the peak-to-valley signal ratio, and the shape of the Coulomb peaks can be fine-tuned by adjusting the barrier gate voltages as demonstrated in Fig. 2.8.c which shows the sensor conductance as a function of the voltages on gates S and B1. At $V_{B1} = -50$ mV low-quality Coulomb oscillations are observed as highlighted in the figure inset (I). Increasing V_{B1} to $V_{B1} = 50$ mV leads to more regular Coulomb peak shapes (curve II in the figure inset). Generally, the aim is to reach sharp

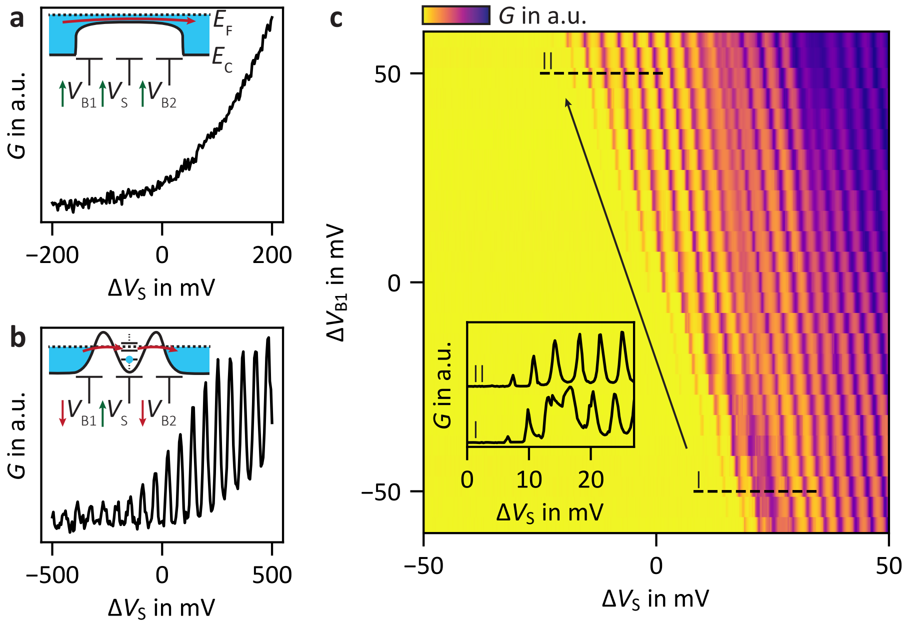

Figure 2.8: **Tuning a single electron transistor. a** Example plunger pinch-off curve of a single electron transistor (SET) tuned to the field effect transistor (FET) regime. The conductance G is shown as a function of SET plunger gate voltage V_S. The inset illustrates the conduction band edge (E_C) and the charge density (blue) in this regime. The three SET gates (S, B1, and B2) are depicted and green arrows indicate that all gate voltages are increased simultaneously from 0 V to reach the FET regime. The dark red arrow marks the current when the charge reservoirs are biased. **b** The green and light read arrows in the inset illustrate how the gate voltages (V_S, V_{B1}, V_{B2}) are changed to form a quantum dot starting from the situation depicted in **a**. The quantum dot potential landscape and its charge states are depicted above. The blue circle represents an electron occupying the quantum dot. The main graph shows typical Coulomb blockade oscillations observed when sweeping the SET plunger and indicative of quantized charge states. **c** Example SET conductance as a function of its plunger voltage V_S and a barrier voltage V_{B1}. The shape of the Coulomb oscillations varies with the barrier voltage. For two values of V_{B1} a line cut is shown in the lower left inset (I and II). Panel **a**, **b**, and **c** show data measured in a Si/SiGe 2x2 quantum dot system. The data in panel **a** and **b** belong to the same device. The data in panel **c** belongs to a different device.

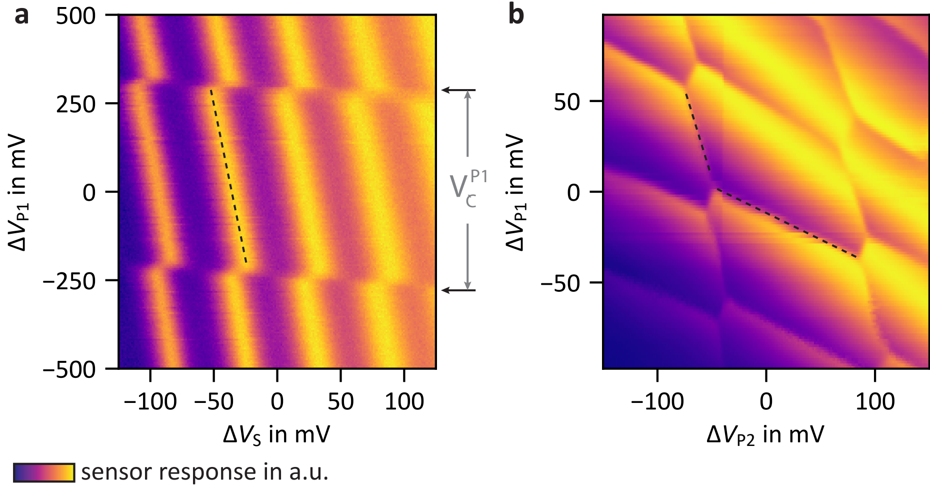

Figure 2.9: **Charge-sensed quantum dots. a** Example sensor response as a function of SET plunger gate voltage V_S and quantum dot Q1 plunger gate voltage V_{P1}. The SET Coulomb oscillations are shifted abruptly when the charge state of quantum dot Q1 is changed. These charge transitions are marked by black arrows. **b** Example sensor response as a function of two quantum dot (Q1 and Q2) plunger gate voltages V_{P1} and V_{P2}. A typical honeycomb pattern is observed. Dashed lines mark two example charge transitions. The more horizontal charge transition line corresponds to quantum dot Q1 and the more vertical charge transition line to quantum dot Q2. The continuous change in sensor response in the background is a consequence of the capacitive coupling of the two plunger gates P1 and P2 to the sensing quantum dot (SET). Panel **a** and **b** show data measured in a Si/SiGe 2x2 quantum dot system. The data in panel **a** and **b** belong to different devices.

and high Coulomb peaks as they provide the highest charge sensing contrast.

CHARGING THE QUANTUM DOTS

Next, the plunger gate of a quantum dot that lies adjacent to the SET is swept while monitoring the Coulomb oscillations as illustrated in Fig. 2.9.a. Such a scan is repeated continuously while adapting the offset of the plunger gate voltage V_{P1} and other close-by gates. Similar to the tuning of a SET, one can start increasing V_{P1} and lowering the surrounding gate voltages to shape a confining potential. When a quantum dot that is sufficiently coupled to a charge reservoir (e.g. the SET itself) is formed, jumps in the Coulomb oscillations are observed as marked by black arrows in Fig. 2.9.a. These jumps correspond to a change in charge occupancy in the formed quantum dot which leads to a capacitively induced shift of the Coulomb oscillations. The same procedure can be repeated to tune further quantum dots in the array. It is also helpful to scan the sensor response as a function of two quantum dot plunger gates as illustrated in Fig. 2.9.b which shows a honeycomb pattern, a typical signature of a double quantum dot. The charge transitions of the two quantum dots can be identified from their slopes (marked by two dashed lines). Here the steeper slope corresponds to the quantum dot formed underneath gate P1 and the less steep slope to the quantum dot formed underneath gate P2[8].

[8]A detailed review of the charge characteristics of quantum dots and how they can be modeled can be found in ref [122], [123].

To tune up an array of quantum dots as presented in chapter 3, first, all four quantum dot voltage configurations are searched for by SET plunger versus quantum dot plunger scans. The abrupt shifts of Coulomb oscillations are attributed to a specific quantum dot by comparing the charging voltages $V_{\mathrm{C}}^{\mathrm{P}i}$ obtained for sweeping all plunger gate voltages $V_{\mathrm{P}i}$. The charging voltage is defined as the voltage difference $\Delta V_{\mathrm{P}i}$ from one charge transition to the next one. Assuming that all gates have a similar effect on the quantum well potential, the quantum dot number Qi is given by the plunger gate for which the smallest charging voltage is observed. When a quantum dot is identified its plunger gate voltage is set far from charge transitions, for instance well below the last transition feature. Then the next quantum dot is searched for analogously. After the signatures of all quantum dots have been observed their presence can be confirmed by quantum dot plunger versus quantum dot plunger scans as shown in Fig. 2.9.b recorded for all plunger gate combinations.

VIRTUAL GATES

Virtual plunger gate voltages can ease the tracking of multiple quantum dots by providing voltages that independently control the chemical potentials of the involved quantum dots and by keeping the charge sensing dot at high sensitivity [56]. They are defined as linear combinations of the real gate voltages:

$$\vec{V}^{\mathrm{virt}} = \mathbb{M}\vec{V}^{\mathrm{real}} \tag{2.1}$$

Here $\vec{V}^{\mathrm{real}}$ and $\vec{V}^{\mathrm{virt}}$ contain the real and virtual gate voltages, respectively. The matrix $\mathbb{M}$ can be obtained from its inverse $\mathbb{M}^{-1}$. Its elements $\mathbb{M}^{-1}_{i,j}$ are given by the effect of gate j on the chemical potential of quantum dot i relative to the effect of gate i on the chemical potential on quantum dot i. They can be estimated from the slopes $\frac{\Delta V_i}{\Delta V_j}$ of charge transition lines in charge stability diagrams as highlighted by dashed lines in Fig. 2.9.b or to the slope of Coulomb oscillation peaks as shown in Fig. 2.9.a (also indicated by a dashed line). Note that iterative updates of the elements of $\mathbb{M}^{-1}_{i,j}$ might be required to obtain optimal virtualization [56].

ELECTRON TEMPERATURE

Determining the electron temperature(s) T_{e} in quantum dot devices can provide insights into the degree of thermal isolation and operation-related heating effects. Ideally, T_{e} is kept well below qubit energy scales E_{q} and leakage state energies E_{l} to prevent thermal occupation leading to a loss of quantum information: $T_{\mathrm{e}} \ll E_{\mathrm{q}}/k_{\mathrm{B}}$ and $T_{\mathrm{e}} \ll E_{\mathrm{l}}/k_{\mathrm{B}}$ with k_{B} the Boltzmann constant. Additionally, recent work suggests improved qubit fidelities by choosing an increased device temperature[9] at which qubit frequencies do not shift during quantum operations [124]. Beyond its direct interpretation, T_{e} also enters as a parameter during the extraction of tunnel couplings via polarization line fitting which will be discussed further below.

The electron temperature of charge reservoirs can be determined by coupling a quantum dot to a source and drain reservoir and measuring Coulomb blockade oscillations.

[9] compared to a typical dilution refrigerator base temperature

The shape of the Coulomb peaks then is determined by the dot-reservoir tunnel coupling, charge noise, and the reservoir electron temperature [125]. To measure the electron temperature the reservoir-dot tunnel coupling should be lowered until it does not affect the shape of the coulomb peaks anymore. Furthermore, the measurement time should be chosen such that charge noise has a negligible effect on the shape of the coulomb peak[10]. Also, the applied bias is kept as small as possible. Then the Fermi distributions of both reservoirs can be assumed to be approximately equal and the current through the quantum dot as a function of the quantum dot chemical potential is given by the derivative of the Fermi function [128], [129]:

$$I = A\cosh^{-2}\left(\frac{\alpha(V - V_0)}{2k_B T_e}\right) + C \tag{2.2}$$

Here, α is the lever arm of the quantum dot plunger gate (see the following subsection) and V is the potential on the quantum dot plunger gate. The coulomb peak can be fitted by equation 2.2 with the scaling factor A, the offset C, and electron temperature T_e as fitting parameters.

It is often observed that the electron temperature can not be decreased below a minimum value $T_{e,min}$ [129], [130]. If the sample temperature [11] is lowered further the electron temperature decouples from the phonon temperature T_{ph}. Phenomenologically this observation is described by:

$$T_e = \sqrt{T_{ph}^2 + T_{e,min}^2} \tag{2.3}$$

Note that it has been shown that the electron temperature of quantum dots that are not directly coupled to a reservoir can differ from the reservoir electron temperature [131], [132]. Thus, it can be useful to measure the electron temperature of these quantum dots directly. Similarly to the coulomb peak method, one can determine the electron temperature from the broadening of an interdot charge transition. To that end the detuning $V_\epsilon = V_{P1} - V_{P2}$ is swept with V_{Pi} the plunger gate voltage that controls the potential of quantum dot i. Charge sensing allows for the direct recording of the charge response. For negligible tunnel coupling and charge noise, the charge transition again can be fitted by a Fermi distribution:

$$S = \frac{A}{1 + \exp\left(-\frac{\alpha_\epsilon(V - V_0)}{k_B T_e}\right)} + C \tag{2.4}$$

with the detuning lever arm α_ϵ and A, V_0, and C as additional fitting parameters.

[10] Typical measurement times ($\mathcal{O}$(ms)), typical integration times ($\mathcal{O}(\mu$s)), and a typical charge noise power spectral density of $S_\mu \approx 1\ \mu eV/\sqrt{Hz}$ at 50 mK and 1 Hz will lead to a temperature error of $\approx$ 10 mK. Here it is assumed that the charge noise power spectral density is described by $S_\mu(f) = Af^{-1}$, the measurement bandwidth is given by $f_H - f_L$, and that the quantum dot potential is given by $\mu = \alpha V$ with V the gate voltage and α the gate lever arm. Then the charge noise induced standard derivation of the quantum dot potential is given by $\sigma_V^2 = \frac{2A}{\alpha}\log\left(\frac{f_H}{f_L}\right)$ and the effect of charge noise onto a Coulomb peak can be calculated by convolution [126], [127].

[11] often assumed to be equal to the mixing chamber temperature of the corresponding fridge

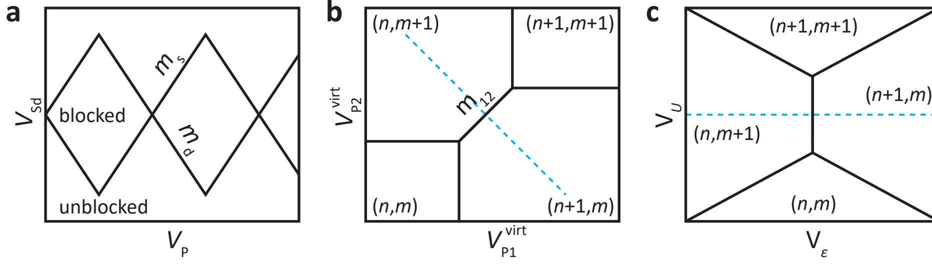

Figure 2.10: **Extraction of lever arms. a** Illustration of Coulomb diamonds emerging when the current through a SET is recorded as a function of its plunger gate voltage V_P and the applied source-drain bias V_sd. Outside the diamonds, a current is detected, inside the diamonds, no current flows. The slopes m_s and m_d allow to extract the plunger gate lever arm. **b** Charge stability diagram of a double quantum dot (Q1 and Q2). The response of a charge sensor as a function of the corresponding two virtual plunger gates vP1 and vP2 is illustrated. Charge states are labeled (m,n) with m the charge occupation in quantum dot Q1 and n the charge occupation in quantum dot Q2. The blue dashed line marks a detuning axis. The slope of the interdot transition is labeled m_{12}. **c** Illustration of the same charge stability diagram as in **b** but as a function of detuning voltage V_ϵ and offset voltage V_U. The blue dashed line is identical to the blue dashed line in **a**.

LEVER ARM

The lever arm α_i is the ratio between a voltage change ΔV_i applied to a gate electrode and the corresponding variation of a relevant energy, for instance, the change in the corresponding quantum dot chemical potential $\Delta\mu_i$:

$$\alpha_i = \frac{\Delta\mu_i}{\Delta V_i} \tag{2.5}$$

The lever arm of the plunger gate P that controls a reservoir-coupled quantum dot can be determined from Coulomb diamonds. Coulomb diamonds are observed when recording the current I flowing through the quantum dot as a function of the plunger gate voltage V_P and the source-drain bias V_sd applied to the source reservoir. Only when a quantum dot state is available between the Fermi levels of the source and drain reservoir a current can flow. This leads to blockaded regions taking the shape of diamonds as illustrated in Fig. 2.10.a. The edges of these diamonds are given by:

$$V_\text{s}(V_\text{P}) = m_\text{s} V_\text{P} + V_\text{s}^0 \quad \text{and} \quad V_\text{d}(V_\text{P}) = m_\text{d} V_\text{P} + V_\text{d}^0 \tag{2.6}$$

Here m_i[12] is the slope of the diamond edge and V_i^0 is a constant offset. m_s and m_d can be determined from Coulomb diamond measurements and allow for calculating the plunger gate lever arm:

$$\alpha_\text{P} = \| \frac{m_\text{s} m_\text{d}}{m_\text{s} - m_\text{d}} \| \tag{2.7}$$

The lever arm of a gate electrode P1 to a quantum dot Q1 also can be determined if the corresponding quantum dot is capacitively coupled to a quantum dot Q2 with

[12] $m_\text{s} = \frac{C_\text{P}}{C_\Sigma - C_\text{s}}$ and $m_\text{d} = \frac{C_\text{P}}{C_\text{s}}$ with C_P the plunger, C_s the source, and C_d the drain capacitance to the quantum dot. $C_\Sigma = C_\text{P} + C_\text{s} + C_\text{d}$. Note that a constant interaction model and thus a semi-classical description is assumed [122].

known plunger gate lever arm α_{P2}. From a virtual gate voltage scan of the respective interdot-transition as exemplary shown in Figure 2.10.b the slope $m_{12} = \Delta V_{\mathrm{P2}}^{\mathrm{virt}}/\Delta V_{\mathrm{P1}}^{\mathrm{virt}}$ can be extracted. Then the lever arm of P1 to Q1 is given by[13]:

$$\alpha_{\mathrm{P1}} = m_{12}\alpha_{\mathrm{P2}} \tag{2.8}$$

Besides quantum dot plunger gate voltages, the detuning voltage V_ϵ is frequently utilized in the tuning and operation of spin qubits. Its underlying energy ϵ is defined as the potential difference $\mu_1 - \mu_2 = \alpha_1 V_{\mathrm{P1}}^{\mathrm{virt}} - \alpha_2 V_{\mathrm{P2}}^{\mathrm{virt}}$ between two quantum dots Q_1 and Q_2. By additionally introducing the energy offset $U = \frac{1}{2}(\mu_1 + \mu_2)$ a linear transformation of the plunger gate voltage space is provided as illustrated in Fig. 2.10.b and c. Then the detuning lever arm α_ϵ can be calculated from the plunger gate lever arms $\alpha_{\mathrm{P}i}$:

$$\alpha_\epsilon = \frac{\alpha_{\mathrm{P1}} + \alpha_{\mathrm{P2}}}{2} \tag{2.9}$$

The detuning lever arm also can be determined directly by fitting the charge interdot transition at a known tunnel coupling (see section 2.4). Further methods include photon-assisted tunneling (PAT) [122] and magneto-spectroscopy [35] which require microwave excitation or magnetic field sweeps, respectively.

TUNNEL COUPLING

The implementation of exchange-based two-qubit gates as well as analog quantum simulations in quantum dot arrays requires tunnel-coupled quantum dots and ideally control over the interdot tunnel couplings. Therefore, measuring tunnel couplings can provide insights how well a quantum dot array is suited for quantum computing or quantum simulation.

The tunnel coupling between two quantum dots can be estimated by fitting the sensor response of a detuning sweep across the corresponding interdot transition (see blue dashed line in Fig. 2.10) by [133]:

$$\delta_{\mathrm{SET}} = \delta + \gamma(\epsilon) + \frac{A}{2}(1 + \frac{\epsilon}{\Omega}\tanh\left(\frac{\Omega}{2k_{\mathrm{B}}T}\right)) \tag{2.10}$$

with:

$$\gamma(\epsilon) = \begin{cases} \gamma_L\epsilon & \text{if } \epsilon <= \epsilon_0 \\ \gamma_R\epsilon & \text{if } \epsilon > \epsilon_0 \end{cases} \tag{2.11}$$

and:

$$\Omega = \sqrt{\epsilon^2 + 4t^2} \tag{2.12}$$

[13] Here it is assumed that $\mathbb{M}_{i,i}^{-1} = 1$ and thus a change of the virtual plunger gate voltage $\Delta V_{\mathrm{P}i}^{\mathrm{virt}}$ equals the corresponding change of the real plunger gate voltage $\Delta V_{\mathrm{P}i}^{\mathrm{real}}$. If this is not the case, virtual gates have different lever arms than their corresponding real gates.

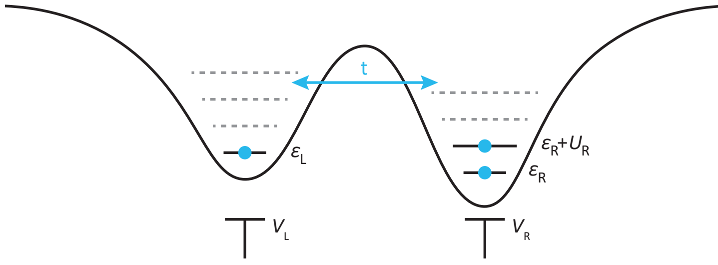

Figure 2.11: **Tunnel-coupled double quantum dot** Illustration of the parameters describing a simple double quantum dot model. ϵ_L and ϵ_R describe the on-site chemical potentials which are controlled by the gate voltages V_L and V_R. U_L denotes the on-site charging energy and t the tunnel coupling (hopping term). The undulating line illustrates the potential landscape, horizontal lines the quantum dot charge states and blue dots the charges in the quantum dots.

where ϵ is the detuning, t is the tunnel coupling, T is the electron temperature, k_B is the Boltzman constant and δ, A, ϵ_0, γ_L, and γ_R are fitting parameters describing offsets and scaling.

However, varying charge occupations, low-lying valley states, and spin-orbit interaction can add complexity not covered by this fitting function. Therefore, in the following section, the underlying physical model will be derived and discussed for multiple system properties.

2.5. POLARIZATION OF TUNNEL COUPLED DOUBLE QUANTUM DOTS

In this section, the polarization of a double quantum dot will be derived loosely following reference [133].

The polarization of a double quantum dot can be modeled starting from a tight binding Hamiltonian as illustrated in Fig. 2.11. In the second quantization formalism, it is expressed as:

$$\begin{aligned} H = {} & \epsilon_\mathrm{L} \sum_\sigma a^+_{\mathrm{L},\sigma} a_{\mathrm{L},\sigma} + \epsilon_\mathrm{R} \sum_\sigma a^+_{\mathrm{R},\sigma} a_{\mathrm{R},\sigma} \\ & + t \sum_\sigma a^+_{\mathrm{R},\sigma} a_{\mathrm{L}\sigma} + a^+_{\mathrm{L},\sigma} a_{\mathrm{R},\sigma} \\ & + U_\mathrm{L} \sum_{\sigma,\sigma'} a^+_{\mathrm{L},\sigma} a^+_{\mathrm{L},\sigma'} a_{\mathrm{L},\sigma'} a_{\mathrm{L},\sigma} + U_\mathrm{R} \sum_{\sigma,\sigma'} a^+_{\mathrm{R},\sigma} a^+_{\mathrm{R},\sigma'} a_{\mathrm{R},\sigma'} a_{\mathrm{R},\sigma} \end{aligned} \tag{2.13}$$

Here $a_{i,\sigma}$ and $a^+_{i,\sigma}$, are the fermionic annihilation and creation operators for i the left (L) and right (R) quantum dot and σ the spin up (↑) or spin down state (↓), t is the tunnel coupling strength (hopping parameter), ϵ_i is the orbital energy, and U_i is the on-site charging energy of quantum dot i. $|\mathrm{vac}\rangle$ denotes the vacuum state. Focusing on the basis $\{|\mathrm{L}\rangle, |\mathrm{R}\rangle\} = \{a^+_\mathrm{L}|\mathrm{vac}\rangle, a^+_\mathrm{R}|\mathrm{vac}\rangle\}$ which comprises a single charge located either in the

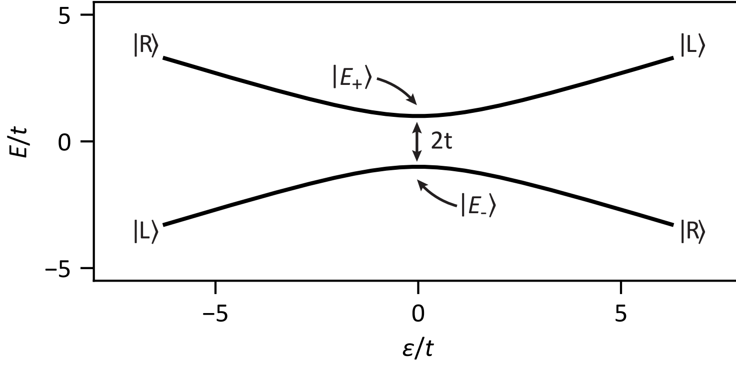

Figure 2.12: **Eigenenergy spectrum of a double quantum dot occupied by one charge.** Energy E of the ground state $|-\rangle$ and excited state $|+\rangle$ as a function of detuning ϵ, both normalized by the tunnel coupling t. At $\epsilon = 0$ an anticrossing with energy level splitting $2t$ emerges and the charge is fully delocalized across the two quantum dots.

left or right quantum dot[14] the matrix representation of H is given by:

$$H_1 = \begin{pmatrix} -\frac{1}{2}\epsilon & t \\ t^* & \frac{1}{2}\epsilon \end{pmatrix} \tag{2.14}$$

Here, $\epsilon = \epsilon_R - \epsilon_L$ denotes the detuning of the on-site orbital energies, and energy shifts (terms proportional to the identity operator) have been omitted. The eigenenergies of H_1 are given by $E_\pm = \pm\frac{1}{2}\Omega$ with $\Omega = \sqrt{\epsilon^2 + 4t^2}$. Their evolution as a function of detuning is plotted in Fig. 2.12. At the anticrossing (at $\epsilon = 0$) the $|\mathrm{L}\rangle$ and $|\mathrm{R}\rangle$ charge state hybridize and show a level splitting of $2t$.

From the eigenstates $|E_\pm\rangle$ of H_1, one can derive the conditional probabilities $P(\mathrm{L}|\pm)$ of the charge being localized in the left quantum dot.

$$P(\mathrm{L}|\mathrm{E}_\pm) = \frac{1}{2} \mp \frac{1}{2}\frac{\epsilon}{\Omega} \tag{2.15}$$

The respective occupation probabilities $P(E_\pm)$ of the ground and excited state can be described by a Boltzmann distribution when the system is at a finite temperature T:

$$P(E_\pm) = \frac{1}{1 + \exp\left(\frac{\mp\Omega}{k_B T}\right)} = \frac{1}{2}\tanh\left(\frac{\pm\Omega}{2k_B T}\right) + \frac{1}{2} \tag{2.16}$$

with k_B the Boltzmann constant. By combining equation 2.15 and 2.16 the probability of the charge being located in the left quantum dot $P(\mathrm{L})$ and thus the polarization can be described by:

$$P(\mathrm{L}) = P(\mathrm{L}|E_-)P(E_-) + P(\mathrm{L}|E_+)P(E_+) = \frac{1}{2}(1 + \frac{\epsilon}{\Omega}\tanh\left(\frac{\Omega}{2k_B T}\right)) \tag{2.17}$$

[14] Here the spin degree of freedom is neglected.

HIGHER CHARGE OCCUPATIONS

To this point, we have assumed single-charge occupancy. However, to describe charge transitions in a double quantum dot occupied by two or more electrons or holes, we must also consider the spin degree of freedom. For example, when a double quantum dot is occupied by two electrons, the ground state is a spin singlet, either localized in the left (right) quantum dot, denoted as $|S(2,0)\rangle$ ($|S(0,2)\rangle$), or delocalized across both quantum dots, represented as $|S(1,1)\rangle$. Assuming that the thermal occupation of spin-triplet states is negligible and once again disregarding constant energy offsets, the relevant Hamiltonian in the singlet basis $\{|S(1,1)\rangle, |S(0,2)\rangle\}$ is as follows:

$$H_{(1,1),(0,2)} = \begin{pmatrix} -\frac{1}{2}\epsilon' & \sqrt{2}t \\ \sqrt{2}t^* & \frac{1}{2}\epsilon' \end{pmatrix} \tag{2.18}$$

Here, to account for the on-site Coulomb repulsion in the $|S(0,2)\rangle$ state, the detuning is redefined as $\epsilon' = \epsilon + U_R$. Equation 2.18 shows that the singlet tunnel coupling is $\sqrt{2}$ times larger than the tunnel coupling for single charges. An adjusted fitting formula can be derived by substituting t with $\sqrt{2}t$ in Equation 2.17 if no magnetic field is applied and in case the temperature is significantly lower than the singlet $|S\rangle$-triplet $|T(1,1)\rangle$ energy separation ($k_B T \ll \frac{1}{2}(-\epsilon' + \sqrt{\epsilon'^2 + 8t^2})$). Otherwise, the singlet state may no longer be the exclusive ground state for all ϵ [123] or triplet states may be thermally occupied. In both scenarios, it becomes necessary to consider the occupation probabilities $P(T_j)$ and conditional polarization probabilities $P(L|T_j)$ of the triplet states.

LOW LYING VALLEY STATES

Low-lying valley states (see section 2.1), which are commonly found in Si/SiGe-based quantum dots, can alter the polarization $P(L)$ of a double quantum dot. A detailed study describing the effect of valley states on tunnel couplings as extracted from polarization measurements has been conducted by Zhao and Hu [134]. From their work, the ensuing discussion will be derived.

The degeneracy of the two low-lying z-valleys of the silicon quantum well (see section 2.1) is lifted due to the interaction between the electron wavefunction and the upper quantum well interface. This interaction leads to the mixing of the valleys, resulting in two new valley eigenstates $\{|0\rangle, |1\rangle\}$ characterized by a mixing phase ϕ, which reflects their composition from the z-valleys.

Note that the two quantum dots in a double quantum dot system can possess different z-valley compositions for their ground and excited state. The extent of overlap between the valley eigenstates of the left and right quantum dot determines the tunneling strength from one valley in the left to another valley in the right quantum dot. Consequently, when there is a non-negligible difference in the valley mixing phases between the two quantum dots $\Delta\phi \neq 0$, both intra-valley t_{intra} and inter-valley t_{inter} tunnel couplings affect the polarization.

Limiting the system description to single-charge occupancy, the Hamiltonian in the

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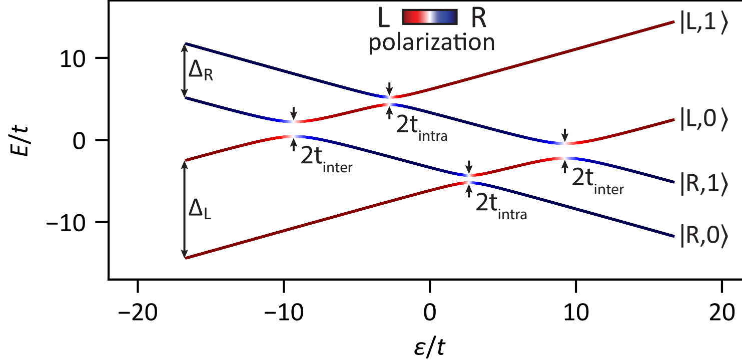

Figure 2.13: **Eigenenergy spectrum of a singly occupied double quantum dot with low-lying valley states.** Energy E of the four eigenstates of H_{valley} as a function of detuning ϵ, both normalized by the tunnel coupling t. Four anticrossings with energy level splittings $2t_{\text{inter}}$ and $2t_{\text{intra}}$ emerge at which the charge delocalizes across both quantum dots. The polarization of the double quantum dot is given by the plot color with dark red and dark blue denoting the charge being located in the left or right quantum dot, respectively. $\Delta_{\text{L}} = 6t$ and $\Delta_{\text{R}} = 3.33t$ are the left and right quantum dot valley splitting.

basis $\{|\text{L},0\rangle, |\text{L},1\rangle, |\text{R},0\rangle, |\text{R},1\rangle\}$ reads:

$$H_{\text{valley}} = \begin{pmatrix} -\frac{1}{2}\epsilon - \frac{1}{2}\Delta_L & 0 & t_{\text{intra}} & t_{\text{inter}} \\ 0 & -\frac{1}{2}\epsilon + \frac{1}{2}\Delta_L & t_{\text{inter}} & t_{\text{intra}} \\ t^*_{\text{intra}} & t^*_{\text{inter}} & \frac{1}{2}\epsilon - \frac{1}{2}\Delta_R & 0 \\ t^*_{\text{inter}} & t^*_{\text{intra}} & 0 & \frac{1}{2}\epsilon + \frac{1}{2}\Delta_R \end{pmatrix} \tag{2.19}$$

Here Δ_i is the valley splitting on site i and t_{intra} and t_{inter} relate to the tunnel coupling t as defined above by $|\, t_{\text{intra/inter}} \,| = |\, \frac{1}{2}(1 \pm e^{-i\Delta\phi}) \,|$. Fig. 2.13 illustrates the eigenenergies of H_{valley}. Four anticrossings emerge with gaps defined by t_{intra} and t_{inter}. Analogously to the simple valley-free case discussed above, the occupation probability of the left quantum dot $P(\text{L})$ can be derived from the eigenstates of the system Hamiltonian H_{valley} and by accounting for a finite temperature through the incorporation of Boltzmann factors. One can find both analytical and approximate expressions for $P(\text{L})$ in reference [134]. Numerical diagonalization of H_{valley} as utilized for drawing Fig. 2.13 provides another method to obtain $P(\text{L})$.

Fig. 2.14 shows the polarization function $P(\text{L})(\epsilon)$, the eigenenergies $E(\epsilon)$, $P(\text{L|i})$ and the thermal occupation of all eigenstates for a valley mixing phase difference $\Delta\phi$ of 0.1π, 0.5π, and 0.9π assuming H_{valley} as system Hamiltonian with $\Delta_{\text{L}} = \Delta_{\text{R}} = 100\ \mu\text{eV}$, $T_{\text{e}} = 50$ mK, and $t = 50\ \mu\text{eV}$. Additionally, $P(\text{L})$ is plotted assuming no low-lying valley states are present (using Hamiltonian H_1). For valley mixing phase differences close to 0, no significantly different behavior is observed. However, for valley mixing phase differences between the two quantum dots that are close to π, at the charge transition point the excited valley state energy gets close to the valley ground state energy and thus

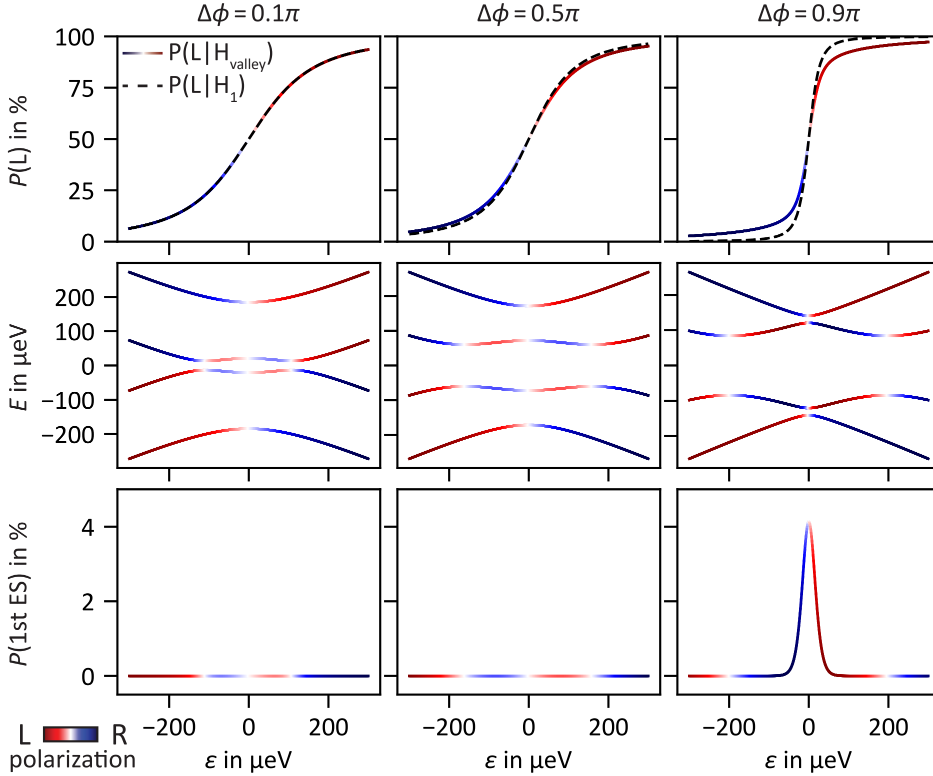

Figure 2.14: **Polarization of a double quantum dot for low, medium, and high valley-mixing phase differences.** Polarization $P(\mathrm{L})$, eigenenergy E and thermal occupation of the first excited state $P(\mathrm{1stES})$ as a function of detuning ϵ for valley mixing phase differences $\Delta\phi$ of 0.1π, 0.5π, and 0.9π. In the upper row, the dashed line depicts the polarization assuming a valley-free Hamiltonian H_1. All other plots (solid lines) assume H_{valley} with low-lying valley states. Their coloring represents the double quantum dot or corresponding state polarization as indicated by the color bar in the lower left corner. Curves are obtained numerically for $\Delta_{\mathrm{L}} = \Delta_{\mathrm{R}} = 100\ \mu\mathrm{eV}$, $T_{\mathrm{e}} = 50$ mK, and $t = 50\ \mu\mathrm{eV}$. Figure inspired by ref [134].

becomes thermally available. Additionally, the inter-valley tunneling becomes much stronger than the intra-valley tunneling and thus mixes the valley eigenstates close to the charge transition point of the ground state affecting its charge distribution. Both effects lead to an observable difference between the polarization line described by the two-level system and the polarization line described by the four-level system. This difference also gets amplified when the tunnel coupling increases or the valley splitting decreases.

SPIN ORBIT INTERACTION

Spin-orbit interaction as found for holes in Ge/SiGe or artificial spin-orbit interaction induced by a micromagnet field gradient as typical for Si/SiGe devices also affects the tunneling strength of the ground state. It can be considered by introducing spin-flip tunneling. In systems with no spin-orbit interaction, the spin is a preserved quantity

during a tunneling process from one quantum dot to the other quantum dot. Spin-flip tunneling is the tunneling process that also results in a flipped spin. The inclusion of spin-flip tunneling can be treated analogously to the treatment of different valley states by introducing t_{conserve} and t_{flip} to describe the spin-conserving tunneling strength and the spin-flipping tunneling strength, respectively. In the $\{|\text{L},\uparrow\rangle, |\text{L},\downarrow\rangle, |\text{R},\uparrow\rangle, |\text{R},\downarrow\rangle\}$ basis with $\uparrow$ and $\downarrow$ denoting the spin-up and the spin-down state the Hamiltonian then reads:

$$H_{\text{so}} = \begin{pmatrix} -\frac{1}{2}\epsilon - \frac{1}{2}E_L & 0 & t_{\text{conserve}} & t_{\text{flip}} \\ 0 & -\frac{1}{2}\epsilon + \frac{1}{2}E_L & t_{\text{flip}} & t_{\text{conserve}} \\ t^*_{\text{conserve}} & t^*_{\text{flip}} & \frac{1}{2}\epsilon - \frac{1}{2}E_R & 0 \\ t^*_{\text{flip}} & t^*_{\text{conserve}} & 0 & \frac{1}{2}\epsilon + \frac{1}{2}E_R \end{pmatrix} \tag{2.20}$$

Here E_i is the Zeeman splitting on-site i. The spin conserving and spin flipping tunnel coupling also can be expressed by $|\ t_{\text{conserve/flip}}\ | = |\ \frac{1}{2}(1 \pm e^{-i\Delta\theta})\ |$ through a total tunnel coupling strength t and the angle $\Delta\theta$ between the spin quantization axes of the two quantum dots. As this Hamiltonian has the same structure as H_{valley} the same considerations apply.

FITTING POLARIZATION LINES

The expression for the system polarization allows for the extraction of the tunnel coupling from a simple sweep of the detuning ϵ across an interdot charge transition. By tracking the resistance or impedance of a nearby SET tuned to the flank of its Coulomb peak a signal that reflects the charge distribution $P(\text{L})$ is obtained. The collected data can be fitted by:

$$S_{\text{SET}} = \delta + \gamma(\epsilon) + A\,P(\text{L})(\epsilon - \epsilon_0) \tag{2.21}$$

with:

$$\gamma(\epsilon) = \begin{cases} \gamma_L \epsilon & \text{if } \epsilon \le \epsilon_0 \\ \gamma_R \epsilon & \text{if } \epsilon > \epsilon_0 \end{cases} \tag{2.22}$$

Here, δ is a global offset, γ_i accounts for the cross capacitance effect of the plunger voltages on the SET signal, ϵ_0 translates the charge transition point and $P(\text{L})(\epsilon)$ is given by the corresponding polarization function as derived above.

Note that the sweep has to be executed sufficiently slowly (adiabatic) to always remain in the system ground state but fast enough to reduce charge noise-induced broadening. Also, when averaging several sweeps, charge noise can artificially increase the extracted tunnel coupling. It can move the anticrossing back and forth along the ϵ axis resulting in a broadened transition curve after averaging[15]. Further, note that when low-lying valley states are present the valley splittings Δ_i and the valley mixing phase difference $\Delta\phi$ are additional fit parameters. Analogously, in the presence of spin-orbit interaction, $\Delta\theta$ and the E_i become additional fitting parameters. Those additional parameters

[15] For a formal treatment see the footnotes in the subsection about electron temperature in section 2.4.

can make the fitting significantly less robust and they ideally should be obtained through a preceding experiment.

However, often the values of the inter-valley and intra-valley or spin-flip and spin-conserving tunnel coupling are not of direct interest and the two-level fitting function (based on equation 2.17) suffices to approximate the tunnel coupling strength of the ground state t_{GS}. This ground state tunnel coupling strength also is sufficient to estimate the expected exchange coupling J between two spins present in the double quantum dot [135]:

$$J = \frac{(4Ut_{GS})^2}{U^2 - \epsilon^2} \tag{2.23}$$

with U the quantum dot charging energy. Thus, for characterizing the viability of a quantum dot array for the implementation of exchange coupled spin qubits equation 2.17 and 2.21 provide an effective fitting model for polarization traces.

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3

A 2D QUANTUM DOT ARRAY IN PLANAR ^{28}Si/SiGe

Semiconductor spin qubits have gained increasing attention as a possible platform to host a fault-tolerant quantum computer. First demonstrations of spin qubit arrays have been shown in a wide variety of semiconductor materials. Advances in qubit operation have made silicon a credible platform for quantum computing, but scaling silicon quantum dot arrays in two dimensions has proven to be challenging. By taking advantage of high-quality heterostructures and carefully designed gate patterns, we are able to form a tunnel coupled 2×2 quantum dot array in a ^{28}Si/SiGe heterostructure. We are able to load a single electron in all four quantum dots, thus reaching the (1,1,1,1) charge state. Furthermore, we characterise and control the tunnel coupling between all pairs of dots by measuring polarisation lines over a wide range of barrier gate voltages. Tunnel couplings can be tuned from about 30 μeV *up to approximately* 400 μeV*. These experiments provide insightful information on how to design 2D quantum dot array and constitute a first step towards the operation of spin qubits in ^{28}Si/SiGe quantum dots in two dimensions.*

This chapter has been published as F. K. Unseld, M. Meyer, M. Madzik, F. Borsoi, S. de Snoo, S. Amitonov, A. Sammak, G. Scappucci, M. Veldhorst, and L. Vandersypen, A 2D quantum dot array in planar 28Si/SiGe, *Appl. Phys. Lett.* **2023** 123(8), 084002 [1].

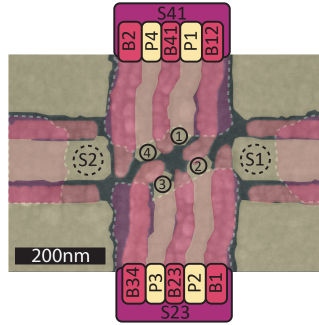

Figure 3.1: False colored SEM image of a nominally identical device to the one used in the measurements. The four quantum dots in the center are labeled clockwise 1-4 with one sensor on each side marked as S1 and S2. Dashed lines mark the boundaries of the screening gates in the first gate layer.

3

3.1. INTRODUCTION

Since the original proposal for quantum computation with semiconductor quantum dots [2], remarkable developments have been made. Quantum dot qubits are small in size, compatible with semiconductor manufacturing, and can be operated with single-qubit gate fidelities and two-qubit gate fidelities above 99.9 % [3] and 99 % [4]–[6] respectively.

The implementation of two-dimensional qubit arrays will allow this technology platform to fully utilize its advantages. In GaAs heterostructures 2x2 and 3x3 quantum dot arrays have already been demonstrated [7]–[9]. However, hyperfine interaction leads to short dephasing times, preventing high-fidelity operation of qubit arrays. In contrast, group IV materials benefit from nuclear spin-free isotopes, such that quantum coherence can be maintained over much longer times [10].

In recent years, hole quantum dots in Ge/SiGe heterostructures progressed from a single quantum dot to the 4×4 quantum dot array with shared gate control presented in chapter 4 [11], [12]. Parallel to that also silicon based devices have been pushed towards 2D arrays. Using quantum dots confined in the corners of silicon nanowires, several $2 \times N$ quantum dot arrays have been demonstrated, albeit not simultaneously at the single-electron occupancy [13]–[15]. Furthermore, these devices did not contain separate gates for independent control of the tunnel barriers between neighbouring dots. This limits the controllability for quantum simulations and prevents sweet-spot operation [16]–[18] of exchange-based quantum gates.

In this chapter, we present a 2D quantum dot array in gated planar ^{28}Si/SiGe with barrier gates to control inter-dot tunnel couplings. Four quantum dots in a 2×2 configuration are formed with occupations controlled down to the last electron. Furthermore, all inter-dot tunnel couplings are characterized as a function of all barrier gate voltages. We demonstrate control over a wide range of tunnel couplings and provide suggestions for future scalable gate designs.

3.2. RESULTS

The 2×2 quantum dot array investigated in this chapter is fabricated on a $^{28}Si/Si_{70}Ge_{30}$ heterostructure (see section 3.4). Fig. 3.1 shows a false-coloured scanning electron micrograph (SEM) image of a nominally identical device, highlighting the three gate layers of the multi-layer gate stack[19]. The screening gates in the first layer (purple) define an active area, reduce the formation of spurious dots and prohibit accumulation of a two-dimensional electron gas (2DEG) in the gate fan-out region. The second layer (yellow) consists of plunger (P) and accumulation gates. Barrier gates (B) are fabricated in the third layer (red). On top of the gate stack sits a micro magnet. The SEM image in Fig. 3.1 is taken before its deposition to highlight the quantum dot gate pattern.

The gate stack defines four quantum dots in a 2×2 grid (labeled clockwise 1-4) and two single-electron transistors (SETs) (S1 and S2). Gate and dot pitches were loosely adopted from the linear six dot array by Philips et al.[20]. The screening gates around the four quantum dots were kept grounded. Two SETs serve as charge detectors and act as electron reservoirs for the quantum dots Q2 and Q4 in the 2×2 array. The quantum dots Q1 and Q3 are loaded via Q2 and Q4 respectively. The presented data was taken exclusively with the sensor providing the highest contrast on the chosen dot pair for each measurement.

The 22.5 degree rotation of the square array relative to the micromagnets gives every quantum dot a distinct Zeeman splitting. The relative arrangement of the quantum dots and the SETs allows for sensing charge movements between all possible dot pairs. This is favorable for recording charge polarization lines and spin-to-charge conversion.

Off-chip NbTiN inductors connected to the SET reservoirs and parasitic capacitances form a tank circuit that enables radio frequency (RF) reflectometry readout, allowing for fast and accurate detection of the charge occupation of all four quantum dots.

During the device tune-up, we measure the cross-capacitive coupling of all gates to all dots and virtualise them as described in [21] with vP_i (vB_{ij}) denoting the virtualised plunger (barrier) gates. The chosen virtual gates compensate the cross-talk onto all dot potentials and maintain the operation point of the charge sensors. The cross-capacitive coupling matrix $\mathbb{M}$, translating the real gate space to the virtual gate space via $\vec{V}^{\mathrm{virt}} = \mathbb{M}\vec{V}^{\mathrm{real}}$, is provided in the section 3.6.

CHARGE OCCUPATION

To show control over the charge occupation of the entire 2×2 array, we measure four charge stability diagrams as depicted in Fig. 3.2. We acquire this data by sweeping the voltages on adjacent virtual plungers gates vP_i and $\mathrm{vP}_{(i \bmod 4)+1}$ while monitoring the response of the charge sensors. The colored circles in the top right corner of each charge stability diagram indicate the position of the quantum dots corresponding to the swept plunger gates.

A honeycomb pattern characteristic of double-dot behavior is observed for all four plunger pairs. We identify the first electron in the four quantum dots by the absence of any more charge transitions in the lower left corner. Thus we can controllably access the $(N_1, N_2, N_3, N_4) = (1,1,1,1)$ charge state, where N_i denotes the charge occupation of quantum dot $\mathrm{QD_i}$, and isolate a single spin per quantum dot. The honeycomb patterns in Fig. 3.2 also show that all four quantum dots are capacitively coupled to each other.

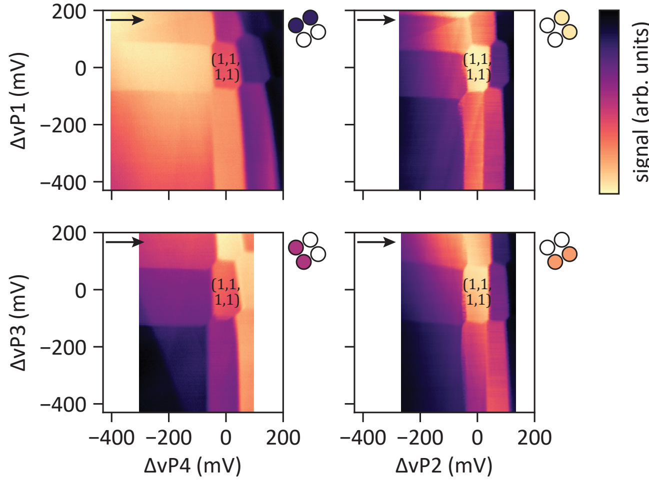

Figure 3.2: Charge stability diagrams of nearest-neighbour quantum dots. Colored circles indicate the quantum dots of the swept virtual plunger gates while the quantum dots corresponding to the white circles remained with one electron each. The point [0 mV, 0 mV] corresponds to the same gate voltages for all four scans. At this operating point, the (1,1,1,1) charge state is reached, with one electron per quantum dot. For the charge stability diagrams of Q1Q2 and Q2Q3 sensor S1 was used while for Q3Q4 and Q4Q1 sensor S2 was chosen. At $\Delta v\text{P}_i = 0$ mV, the corresponding physical voltages on the gates are set to 2566 mV, 1831 mV, 3173 mV, 2487 mV for plungers 1-4, respectively. The arrows in the top left corner of each charge stability diagram indicate the direction of the scans.

We note that there are apparent differences in the separation between the consecutive charge transition lines as well as in the slopes of successive charge transition lines. These could be caused by inherent differences and gate-voltage dependent variations in size, position or lever arm of the four intended quantum dots. Alternatively, they might be the charging signature of additional quantum dots in the close vicinity. While we cannot fully rule out the presence of such stray dots at higher occupations, we can reliably reach the (1,1,1,1) charge state in the 2×2 configuration of the array.

Next to the expected charge transitions, we observe additional diagonal features e.g. in Fig. 3.2, which we associate with spurious defects in our system. These defects capacitively couple to the charge sensor but there is no or only very weak capacitive interaction with the four intentional quantum dots of the 2×2 array.

INTER-DOT TUNNEL COUPLING

Besides a well-defined charge state, controlled inter-dot tunnel couplings are essential for the implementation of robust exchange-based quantum gates or the execution of analog quantum simulation. Therefore, we probe the system evolution as a function of the voltage applied to the virtual barrier gates vB_{ij} located between the plunger gates of quantum dot QD_i and QD_j with $j = (i \bmod 4) + 1$. The tunnel coupling diagonally between QD_1 and QD_3 and anti-diagonally between QD_2 and QD_4 has no dedicated barrier gate and thus is not independently controllable. The influence of other barrier gates on the (anti-)diagonal tunnel coupling is presented below.

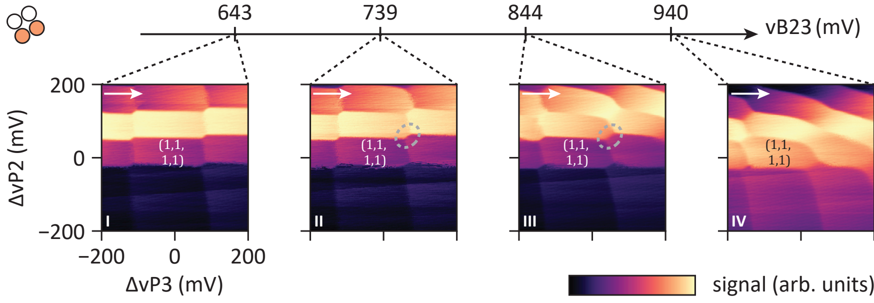

Figure 3.3: Response of the charge stability diagram of QD_2 and QD_3 to changes of virtual barrier voltage vB_{23}, as indicated by the arrow above the charge stability diagrams. Small arrows in the top left corner of each panel indicate the scan direction. From panel I to IV, we observe a gradual increase in both the capacitive and tunnel coupling between the two dots. Similar data were taken for all other nearest-neighbouring pairs and are displayed in section 3.7.

Fig. 3.3 shows the evolution of the charge stability diagram of QD_2 and QD_3 while changing the virtual barrier gate voltage vB_{23}. The sequence of panels allows us to qualitatively assess the influence of the barrier on the capacitive coupling and tunnel coupling between the involved quantum dots. From panel I through IV, we observe that the separation between the triple points increases, which indicates an increase in the capacitive coupling between the dots. In addition, we observe that the interdot charge transition is increasingly blurred (see the circled transitions) and the boundaries of the charge stability diagram are increasingly rounded. Both are indicative of an increased interdot tunnel coupling. In panel IV, for transition lines with $N_2 + N_3 \geq 4$ the rounding is so strong that the quantum dots have mostly merged into a single large dot.

To quantitatively determine the effect of the barrier voltage on the tunnel coupling, we measure polarisation lines along the detuning axis $\epsilon_{ij}/\alpha_{\epsilon ij} = \mathrm{vP}_i - \mathrm{vP}_j$, with $\alpha_{\epsilon ij}$ denoting the lever arm, across the $(N_i, N_j) = (1,0)$ to $(0,1)$ interdot transition, as shown in Fig. 3.4a. The remaining dots were kept in the (1,1) charge occupation. Scanning along this detuning axis moves the electron from dot 2 to dot 3 ($(N_1, N_2, N_3, N_4) = (1,1,0,1)$ to $(1,0,1,1)$), resulting in a step response in the sensor signal as seen in Fig. 3.4b. This step response is broadened by both the electron temperature $T_e \leq 78.5 \pm 2.2$ mK and the tunnel coupling t, and can be fitted using $S_{\mathrm{Sig}} = \frac{\epsilon}{\Omega} \tanh \frac{\Omega}{2k_b T_e}$ with $\Omega = \sqrt{\epsilon^2 + 4t^2}$ and ϵ the detuning between the two quantum dots [22]. Additional slopes and offsets of the sensor signal caused by imperfect virtualisation or drifts are taken into account in the used fitting procedure [23]. We note that the error in the extracted tunnel coupling values is dominated by the uncertainty in the lever arms.

We systematically extract the dependency of the inter-dot tunnel couplings $t_{n,m}$ between all dot pairs $(\mathrm{QD}_n, \mathrm{QD}_m)$ with respect to all barrier voltages vB_{ij}. Fig. 3.4c shows the resulting tunnel couplings $t_{n,m}$ grouped by barrier gates vB_{ij}. As in previous works, fading contrast along the polarization lines prevented us from characterizing tunnel couplings up to higher values. We observe that changing the barrier voltage vB_{ij} affects only the corresponding tunnel couplings t_{ij} significantly, while keeping the other tunnel couplings largely constant. Note that the virtual gate matrix compensates for cross-talk

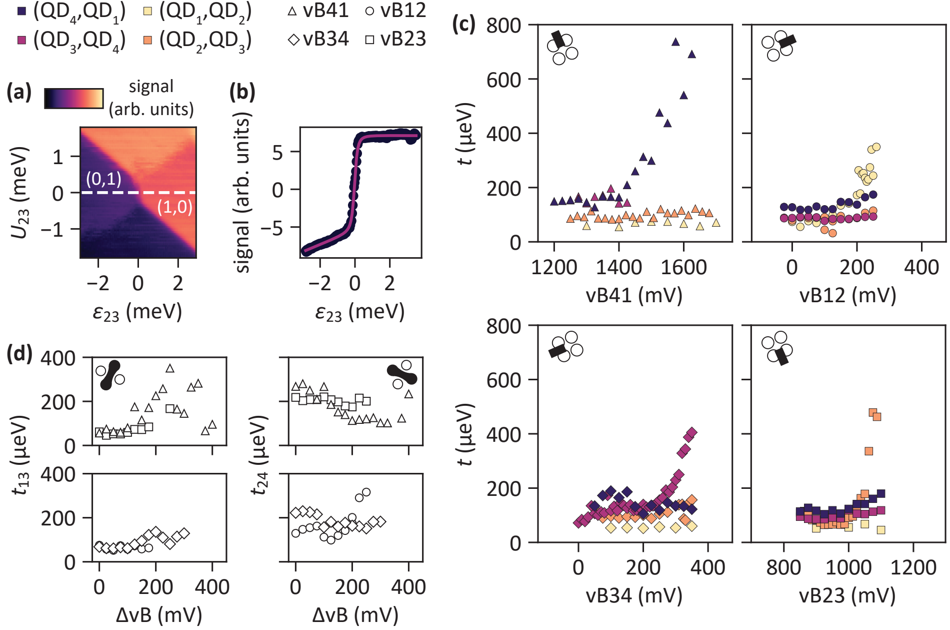

Figure 3.4: **a)** Exemplary charge stability diagram around the (1,0) to (0,1) transition for QD_2 and QD_3 as a function of the interdot detuning ϵ_{23} and $U_{23}/\alpha_{U23} = vP_2 + vP_3$. The dashed line indicates the detuning axis used to measure polarisation lines. **b)** Example of a measured (dots) and fitted (solid line) polarisation line for QD_2 and QD_3. **c)** Dependence of the tunnel couplings extracted from polarization lines between neighbouring quantum dots on each of the four virtual barrier gate voltages. The plots are ordered to follow the physical position of the barrier gate e.g. barrier vB_{41} situated in the top left corner of the quantum dot array is depicted in the top left plot. The legend for symbols and colors is shown above panels a) and b). We note that the dc voltages of barriers vB_{12} (vB_{23}) and vB_{34} (vB_{41}) are of comparable values, which is consistent with the symmetries of the gate pattern. Between scans we adjusted gate voltages of uninvolved gates to retain a high visibility. These adjustments were done in such a way that all uninvolved barrier gates remained in the small (residual) tunnel coupling regime. On several occasions, insufficient contrast between the (1,0) and (0,1) charge states limited the data we were able to reliably fit. These data points are thus not available. **d)** Diagonal tunnel coupling and anti-diagonal tunnel coupling as a function of all four virtual barrier gate voltages. The panels were split into two parts for both the diagonal and anti-diagonal coupling to keep the data points visible. The physical gate voltages used at $\Delta vB = 0$ mV varies between data sets, as the voltages were slightly adjusted. As in c) uninvolved barrier gates remained in the residual tunnel coupling regime. Note also that in c) and d) the charge states vary between scans, depending on which dots each polarization line connects.

of the barrier gates onto all dot potentials, but does not account for possible cross-talk on the tunnel couplings.

We furthermore find that below a given voltage (which is different for each vB_{ij}), the influence of the barrier gate voltage on the corresponding tunnel coupling vanishes and a residual tunnel coupling remains. Across all four neighbouring dot pairs, the residual tunnel coupling is in the range between 30 μeV and 200 μeV.

We extend this characterisation to the (anti-)diagonal tunnel couplings. Fig. 3.4d presents the influence of the four barrier gates on the diagonal and anti-diagonal tunnel coupling respectively. While the anti-diagonal tunnel coupling $t_{2,4}$ is elevated and can be modulated using vB_{12} in particular, the diagonal tunnel coupling $t_{1,3}$ is not systematically influenced by any barrier gate and remains in many cases lower than all other tunnel couplings, albeit far from zero.

3.3. DISCUSSION

We demonstrated the first 2D quantum dot array in a planar silicon technology and operated the four quantum dots in the single electron regime, consistently achieving the (1,1,1,1) charge state. Furthermore, the barrier gates allow us to independently control the interdot tunnel couplings. However, the residual tunnel couplings observed in this sample are higher than the typical tunnel coupling of 1-10 μeV used in spin qubit experiments [24]. Presumably the close proximity of the screening gates to the center of the plunger gates compresses the quantum dots towards the center of the 2×2 array and hence towards each other, leading to rather large tunnel couplings. Furthermore, we see in Fig. 3.4 that at low tunnel coupling values, the tunnel coupling barely responds to the barrier gate voltages anymore. The compressed position of the quantum dots in the center region enhances also the diagonal coupling between them. While analog quantum simulation and quantum computation can benefit from diagonal tunnel coupling, the lack of dedicated control over magnitude and directionality i.e. diagonal versus anti-diagonal, also poses limitations. Suppressing any diagonal coupling with a center gate as demonstrated in a GaAs 2×2 array could be a suitable way to circumvent this issue [25].

The encountered challenges help to identify possible improvements in the design of planar 2×2 ^{28}Si/SiGe quantum dot arrays. Specifically, moving the screening gates away from the center of the array is expected to yield lower tunnel couplings, as the electrons are not squeezed towards each other as much. The experiments also offer relevant learnings for scaling to larger arrays. For instance, changing the device architecture from a square array to a triangular array will alleviate the issues regarding undesired diagonal tunnel couplings [26], [27]. Furthermore, in order to maintain control of individual tunnel couplings, either more sophisticated patterning techniques must be applied to route gates to the inside of a larger array [28], or crossbar addressing must be employed [29], [30]. In both cases, the observations made for the present device provide guidance for suitable plunger and barrier gate pitches and dimensions.

3.4. DEVICE FABRICATION AND SCREENING

This device is fabricated on a ^{28}Si/Si$_{70}$Ge$_{30}$ heterostructure. A 2.5 μm strain relaxed Si$_{70}$Ge$_{30}$ buffer layer makes the foundation. On top of it the isotopically enriched ^{28}Si quantum well is grown. It has a residual ^{29}Si concentration of 0.08% and was measured to be 9.0 ± 0.5 nm thick. Afterward, a 30 nm thick Si$_{70}$Ge$_{30}$ spacer is grown to reduce strain relaxation in the quantum well and separate it from the gate dielectric. The heterostructure is finalized with a 1 nm silicon cap [31]. The gate stack is separated from the heterostructure by 10 nm Al_2O_3, formed by atomic-layer deposition (ALD) at 300 °C. The three gate layers of the gate stack are made from Ti:Pd with thicknesses of 3:17, 3:27 and 3:27 nm and are patterned using electron beam lithography, electron beam evaporation and lift off. Each layer is electrically isolated from the previous layer by a 5 nm Al_2O_3 dielectric grown by ALD. Above the three gate layers a micro magnet is fabricated from Ti:Co (5:200 nm).

After fabrication every device was screened by measuring turn-on curves and testing for gate leakage or shorted gates at 4.2 K with a dipstick in liquid helium. This high turnaround testing allows to verify the basic functionality of the device and quickly filter out defective devices. After verifying the functionality of all gates, NbTiN inductors are added to the ohmic contacts to enable RF-readout. To address electrostatic discharge concerns during rebonding, we screen the device a second time in liquid helium to verify that no damage has been done. Then we cool down the devices in a Bluefors LD400 dilution refrigerator to its base temperature of around 10 mK.

3.5. SETUP

The room-temperature control electronics to operate this device are separated into ac electronics in one rack and dc electronics in a second one. In the latter, several in-house built Serial Peripheral Interface (SPI) racks host 18 bit Digital to Analog Converter (DAC) modules which provide the required dc voltages. Voltage dividers were used to apply an accurate source-drain bias when needed. The currents are measured with a Keithley 2000 Multimeter (placed in the ac rack) via an in-house developed transconductance amplifier. The dc rack is powered by batteries which are continuously charged via gyrators and filters.

The ac rack comprises the host computer, a Keysight chassis (M9019A) and an additional dedicated RF SPI rack. The circuitry for RF reflectometry measurements consists of two in-house built RF sources, a combiner (Mini-Circuits ZFSC-2-5-S+), a 15 dB coupler (Mini-Circuits ZEDC-15-2B) at the mixing chamber stage, a cryo-amplifier at the 4K stage (Cosmic Microwave Technology Inc. CITLF3), a room temperature amplifier, two IQ-mixers and a Keysight digitizer (M3102A). The coaxial lines from 4 K to the mixing chamber flange are made from NbTiN to ensure a high signal quality and low thermal conductance. From 4 K to room temperature, SCuNi-CuNi cables are used. Discrete attenuators with a total attenuation of 23 dB are distributed over the various temperature stages on the downward path.

Next to the digitizer, several Keysight AWG modules (M3202A) are situated in the same chassis and connected via a PCIe connection to a host computer. SCuNi-CuNi 0.86 mm coaxial cables are used from room temperature to the mixing chamber plate.

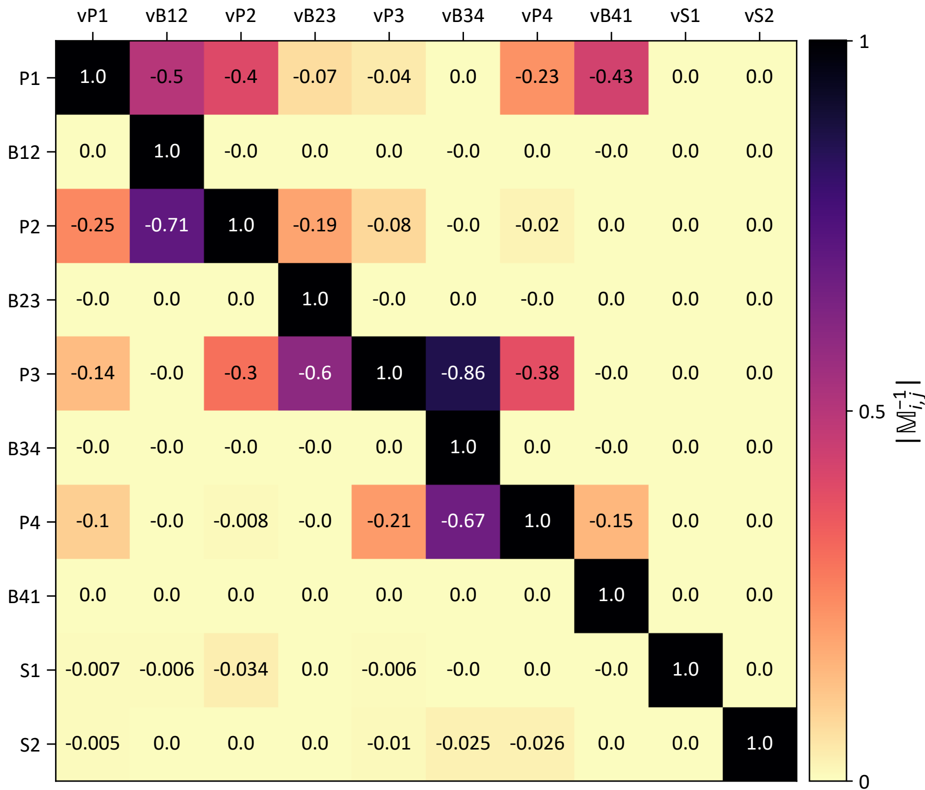

Figure 3.5: Virtual gate matrix ($\mathbb{M}^{-1}$) during the recording of the charge stability diagrams of Fig. 3.2

Also on these lines discrete attenuators are mounted, with a total attenuation ranging from 12 dB to 20 dB (typically we equip the barrier gates with lower attenuation than the plunger gates). From the mixing chamber flange to the sample printed circuit board (PCB), hand-formable 0.086" coaxial cables were used to route both RF and AWG signals. Bias tees on the sample PCB combine the ac pulses and dc voltages. Ferrite cores and dc blocks were installed at room temperature to suppress 50 Hz noise.

3.6. VIRTUAL GATE MATRIX

The virtual gate matrix defining the virtual gates in the charge stability diagrams of Fig. 3.2 is displayed in Fig. 3.5. Note that we constantly adapted the virtual gate matrices throughout the measurements to improve the compensation of cross capacitive effects on the plunger gates of the quantum dots and SETs.

3.7. QUALITATIVE TUNNEL COUPLING CONTROL FOR ALL BARRIER GATES

Fig. 3.6 shows the influence of all barrier gates on the charge stability diagrams of their neighbouring quantum dots. Fig. 3.6b is replicated from Fig. 3.3. All barriers show similar influence on the charge stability diagram as discussed by way of example for barrier vB_{23} in the results section above.

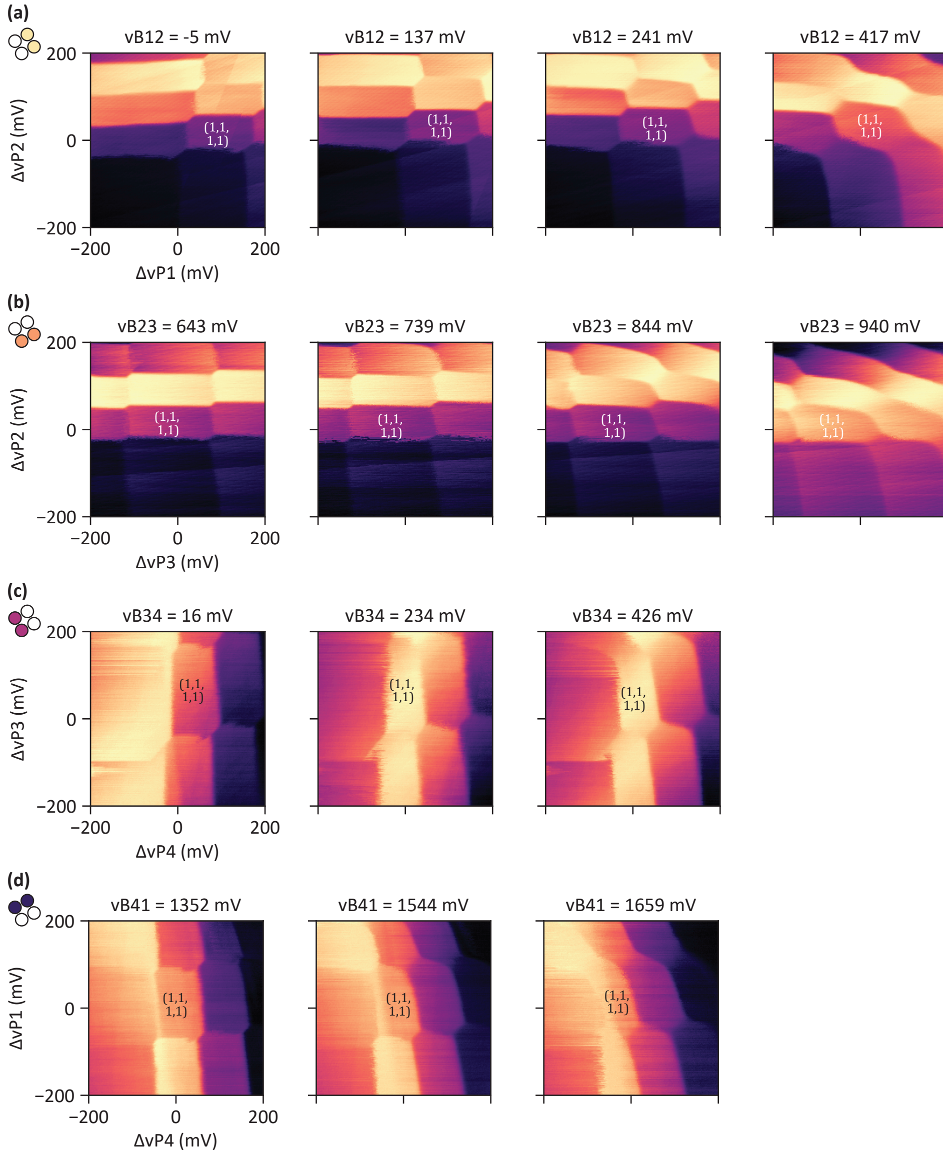

Figure 3.6: Charge stability diagrams for all four quantum dot pairs for several values of the voltage on the barrier gate between the respective dots. Pictograms on the left indicate the quantum dot pair used in the respective row. To ensure comparability every scan is around the (1,1,1,1) regime as indicated.

3.8. ELECTRON TEMPERATURE AND LEVER ARMS

To estimate the electron temperature, we measure the thermal broadening of Coulomb peaks of SET S1 using the equations provided by [32]. We sweep gate B_1 as it has a smaller lever arm compared to the SET plunger gate and therefore allows us to sweep across a Coulomb peak with a much finer resolution, improving the fit quality. Fig. 3.7a shows the Coulomb diamonds that were used to calculate the lever arm of gate B_1. We combine the slopes m_S and m_D of the Coulomb diamonds to compute the lever arm α_{B1} with $\alpha_{B1} = |\frac{m_S m_D}{m_S - m_D}| \approx 0.027 \pm 0.003$. The stated uncertainty is based on bounding the slopes extracted from the Coulomb diamond from below and from above by eye. The horizontal trace at $V_{\mathrm{SD}} \approx -1150\ \mu$V shown in Fig. 3.7c was used to upper bound the electron temperature to $\mathrm{T_e} \leq 80$ mK.

Furthermore we require the lever arms of the plunger gates to convert the detuning axis ϵ_{ij} from gate voltage to energy. Due to the high tunnel coupling, photon-assisted tunneling measurements with the available microwave source were unsuccessful. Instead we estimate the lever arms of the quantum dots via the slope of their interdot transitions.

We convert the lever arm of gate B_1 to the lever arm of virtual plunger gate vS_1 using the ratio of the sensing dot peak spacing as measured when scanning gate voltage vS_1 versus that measured when scanning B_1. We estimate the error introduced by estimating the peak spacing of the Coulomb peaks to be below 10%. From here we can successively use the angle of the interdot transitions to calculate the lever arm ratio between all other gates. For example, Fig. 3.7b shows the manually fitted interdot transition used to calculate the lever arm ratio of plunger gate of vS_1 and vP_2. Similar as before, we bound the error by over- and underestimating the slope of the interdot transition by eye. For the plunger gates vP1 through vP4 we find lever arms of 0.071 ± 0.016 (vP1), 0.073 ± 0.013 (vP2), 0.044 ± 0.009 (vP3), 0.080 ± 0.017 (vP4). The square geometry allows for a consistency check as the lever arm of e.g. Q4 can be calculated via S1-Q2-Q3-Q4 but also via S1-Q2-Q1-Q4. The found differences from using different paths fell within the error of the final value.

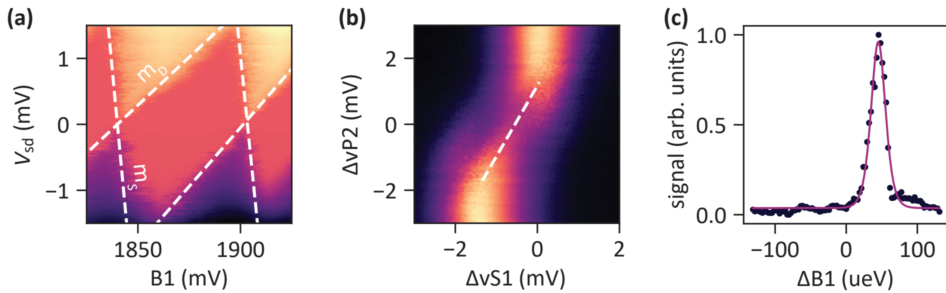

Figure 3.7: **a)** Coulomb diamonds used to extract the lever arm of gate B1. White dashed lines indicate the used slopes. **b)** High resolution interdot transition of sensing dot S1 and QD_2 showing the manual fit (dashed line) to determine the lever arm ratio between the respective plunger gates. **c)** Measured (dots) and fitted (solid line) Coulomb peak used to estimate the electron temperature. The Coulomb peak is the smallest measured peak at the effective zero bias voltage.

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4

SHARED CONTROL OF A 16 SEMICONDUCTOR QUANTUM DOT CROSSBAR ARRAY

The efficient control of a large number of qubits is one of the most challenging aspects for practical quantum computing. Current approaches in solid-state quantum technology are based on brute-force methods, where each and every qubit requires at least one unique control line, an approach that will become unsustainable when scaling to the required millions of qubits. In this chapter, inspired by random access architectures in classical electronics, we introduce the shared control of semiconductor quantum dots to efficiently operate a two-dimensional crossbar array in planar germanium. We tune the entire array, comprising 16 quantum dots, to the few-hole regime and, to isolate an unpaired spin per dot, we confine an odd number of holes in each site. Moving forward, we demonstrate on a vertical and a horizontal double quantum dot a method for the selective control of the interdot coupling and achieve a tunnel coupling tunability from less than 3 GHz to more than 10 GHz. The operation of a quantum electronic device with fewer control terminals than tunable experimental parameters represents a compelling step forward in the construction of scalable quantum technology.

This chapter has been published as F. Borsoi, N. W. Hendrickx, V. John, M. Meyer, S. Motz, F. van Riggelen, A. Sammak, S. L. de Snoo, G. Scappucci, and M. Veldhorst, Shared control of a 16 semiconductor quantum dot crossbar array, *Nat. Nanotechnol.* **2024** 19, 21–27 [1].

4.1. INTRODUCTION

A fault-tolerant quantum computer will require millions of interacting qubits [2]–[4]. Scaling to such extreme numbers imposes stringent conditions on all the hardware and software components, including their integration [5]. In semiconductor technology, several decades of advancements have led to the integration of billions of transistor components on a single chip. A key enabler has been the ability to control such a large number of components with only a few hundred to a few thousand control lines [6], [7]. In quantum technology, such a game-changing strategy has yet to be embraced owing to the fact that qubits are not sufficiently similar to each other. Nowadays, leading efforts in solid state, such as superconducting and semiconducting qubits, all require that each and every qubit component is connected to at least one unique control line [8]. Clearly, this brute-force approach is not sustainable for attaining practical quantum computation.

The development of spin qubits in semiconductor quantum dots has strongly been inspired by classical semiconductor technology [9]–[11]. Advanced semiconductor qubit systems are based on CMOS-compatible materials and even foundry-manufactured qubits have been realised [12], [13]. In addition, it is anticipated that the small qubit footprint and compatibility with (cryo-)CMOS electronics will open up avenues to build integrated quantum circuits [14], [15]. To enable the efficient control of large qubit architectures with a sustainable number of control lines, proposals of architectures inspired by classical random access systems have been put forward [16], [17]. However, their practical realisation has been so far prevented by device quality and material uniformity.

In this chapter, we take the first step toward the sustainable control of large quantum processors by operating semiconductor quantum dots in a crossbar architecture. This strategy enables the manipulation of the most extensive semiconductor quantum device with only a few shared-control terminals. This is accomplished by exploiting the high quality and uniformity of strained germanium quantum wells [18], by introducing an elegant gate layout based on diagonal plunger lines and double barrier gates, and by establishing a method that directly maps the transitions lines of charge stability diagrams to the associated quantum dots in the grid. We operate a two-dimensional 16 quantum dot system and demonstrate the tune-up of the full device to the few-hole regime. In this configuration, we also prove the ability to prepare all the quantum dots in the odd charge occupation, as a key step for the confinement of an unpaired spin in each site [19], [20]. We then introduce a random access method for addressing the interdot tunnel coupling and find a remarkable agreement in the response of two vertically- and horizontally-coupled quantum dot pairs. We also discuss some critical challenges to efficiently operating future large quantum circuits.

4.2. MAIN TEXT

A TWO-DIMENSIONAL QUANTUM DOT CROSSBAR ARRAY

Our shared-terminals control approach for a two-dimensional quantum dot array with dots Q1, Q2t,...Q7 is based on a multi-layer gate architecture (Figs. 4.1a-d). We use two barrier layers (with gates UBi and LBi with $i \in [1,8]$) to control the interdot tunnel couplings, and exploit a layer of plunger lines (Pi with $i \in [1,7]$) to vary the on-site energies (Fig. 4.1c). In contrast to brute-force implementations, here a single plunger gate is em-

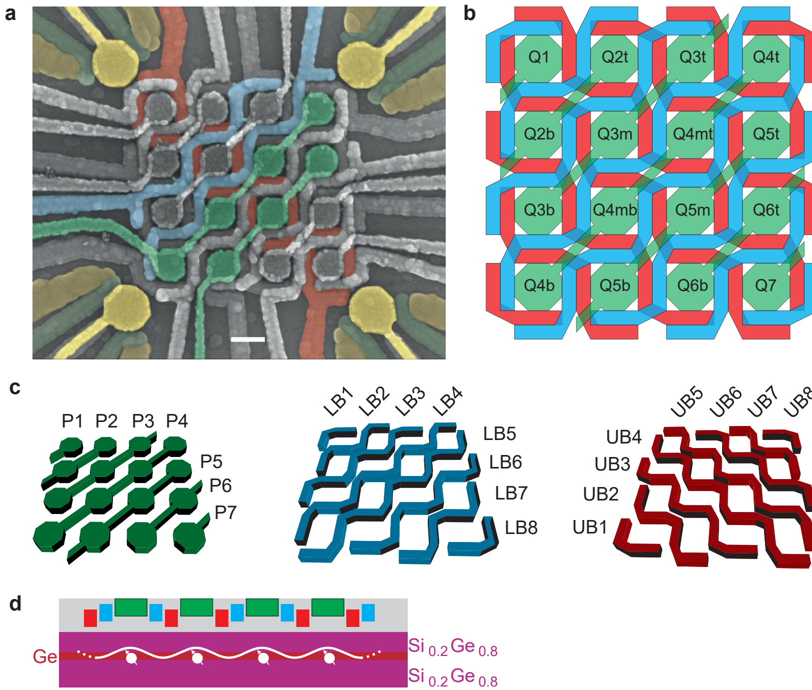

Figure 4.1: **A 16 quantum dot crossbar array. a,** False-colour scanning electron microscopy image of the crossbar array device. The architecture consists of two staircase barrier gate layers (two lines of each layer are shown in red and blue), and one plunger gate layer (two lines are illustrated in green). 16 quantum dots are defined under the plungers, while four charge sensors in the form of single-hole transistors are located at the corners (ohmic contacts in orange, barriers in dark green, and plungers in yellow). The scale bar corresponds to 100 nm, which is also the size of the designed plunger gate diameter. This shared-control approach enables to control a number of quantum dots (g) with a sublinear number of control terminals (T). Here, the scaling is given by $T = 6g^{1/2} - 1$ (Fig. 4.8). **b,** Schematic illustration of the device and labeling of each quantum dot. We choose to label the quantum dots after their positions on their controlling plunger line, e.g., the quantum dot Q6b(t) is located on the bottom (top) site controlled by the plunger line P6. **c,** Shared-control elements: from the top of the gate stack, seven P plunger gates, eight LB barrier gates, and eight UB barrier gates. The overlay of these layers is visible in **(b)**. **d,** Schematic cross-section of the device. Holes are isolated in quantum dots in a 55 nm-deep germanium quantum well in a silicon-germanium heterostructure grown on a silicon wafer.

ployed to control up to four quantum dots, and an individual barrier up to six nearest-neighbours interactions. In analogy with classical integrated circuits, this strategy enables to manage a number of experimental parameters (i.e., dot energies and interdot couplings) with a sub-linear number of control terminals, an approach that may overcome, among other aspects, the wiring interconnect bottleneck of large-scale spin qubit arrays (Fig. 4.8) [7], [8].

To monitor the quantum dot array, we make use of charge sensing techniques [19]. Four single-hole transistors at the corners of the array (named after their cardinal positions: NW as north-west, NE as north-east, SW as south-west and SE as south-east) act as charge sensors as well as hole reservoirs for the array (also see Fig. 4.9). The simultaneous read-out of their electrical response in combination with fast rastering pulse schemes enables us to continuously measure two-dimensional charge stability diagrams in real-time (i.e., in video-mode technique), while updating the dc gate voltages controlling the array [21], [22].

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To bring the device in the 16 quantum dots configuration, we identify an alternative strategy to the tune-up methods established for individually-controlled quantum dot devices [23]. We begin by lowering all gate voltages to starting values based on previous experiments and by defining a set of virtual gates (also see section 2.4) as linear combinations of real gates [23]–[25]. Such virtual gates are defined to eliminate the crosstalk to the charge sensors and to independently control the on-site energies [24], [25] (full matrix in Fig. 4.10). Here, we will refer to vPi as the virtual gate associated to the actual gate Pi.

We continue the tuning of the device by adjusting the gates controlling the quantum dots at the corner (i.e., those closest to the charge sensors) until we accumulate the first few holes as signaled by the first addition lines in charge stability diagrams. We then proceed with the tune-up of the adjacent dots and finish with the quantum dots furthest to the sensor. Owing to the homogeneity of our heterostructure [26] and the symmetry of our gate layout, the accumulation of the first few holes in quantum dots controlled by the same plungers occurs at similar gate voltages.

Rather, challenges in tuning up the array are mainly due to elements outside the array. In fact, we observe that small variations of the gate voltages impact the electrostatics of the dense gate fanout area, which in turn affects the charge sensors and the readout quality. Furthermore, specific gate settings cause unintentional quantum dots under the gate fanout, which restrict the operational window. Altogether, these issues are a challenge for the implementation of automated tuning methods [27], but we envision that the integration of a lower layer of “screening" gates or the implementation of the gate fanout in the third dimension [28] can mitigate this issue (section 4.8).

FROM MULTI-DOT CHARGE STABILITY DIAGRAMS TO QUANTUM DOT IDENTIFICATION

Moving forward, a direct result of our control approach is the fact that, upon sweeping the voltage of a plunger gate controlling n quantum dots, up to n sets of charge transitions can be observed, each associated with (un)loading an additional hole in one of the n quantum dots. For the case of vP2 and vP3, this results in the charge stability diagram shown in Fig. 4.2 where a number of vertical and horizontal charge addition lines mark-

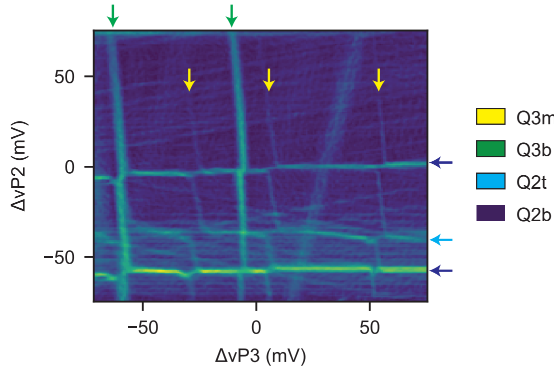

Figure 4.2: **Multi-dot charge stability diagrams** Few-hole charge stability diagram obtained by combining the signal gradients of the SW and NW charge sensors. The labels indicate for each addition line the corresponding quantum dot. At (0,0) the fillings of Q2t, Q2b, Q3t, Q3m, and Q3t are 0, 0, 0, 3, and 0, respectively.

ing well separate charge states are visible. However, because of our control approach, a priori it is unknown to which of the Q3 (Q2) quantum dots these vertical (horizontal) lines are associated.

Here, we solve this problem by establishing a statistical method that maps such transition lines to the respective quantum dot. In our protocol, we first evaluate the shift of the charge transition lines induced by a voltage variation of each barrier gate to estimate the (normalized) capacitive coupling λ between each barrier gate and the associated quantum dot (Figs. 4.3a, b). Because the two barrier layers form a grid of lines and columns, we can use their capacitive couplings to infer the spatial location of the quantum dot in the array. For this purpose, we consider the normalised capacitive couplings of the two orthogonal barrier sets, λ_{vUB} and λ_{vLB}, as two independent probability distributions. We then use λ_{vUB} and λ_{vLB} to calculate the combined probability W on each of the 16 sites (Fig. 4.3c, section 4.4). Finally, our protocol ends assigning the site with the maximum probability to the quantum dot loaded via the specific charge addition lines. In practice, W quantifies how much an electric field generated on each site is perceived by a hole in a specific quantum dot site. Hence, a low (high) W value identifies a location that is weakly (strongly) coupled to the analysed quantum dot.

In Figs. 4.3a-c, we show how this routine is effective for distinguishing and characterising the three Q3 quantum dots, whereas similar results are obtained also for the remaining dots in the grid (Figs. 4.11, 4.12-4.16, 4.17). The demonstrated ability of labelling multi-quantum dot charge stability diagrams makes this method an important tool in the tune-up of large quantum dot devices.

QUANTUM DOT OCCUPANCIES

Whilst useful in reducing drastically the number of control terminals, a crossbar approach is effective for spin-based quantum computing if it enables to isolate a single or an unpaired spin in the individual quantum dots [9], [17]. Here, we demonstrate the tune-up of the array to an odd-charge occupancy configuration with 11 quantum dots filled with one hole, and five quantum dots filled with three holes.

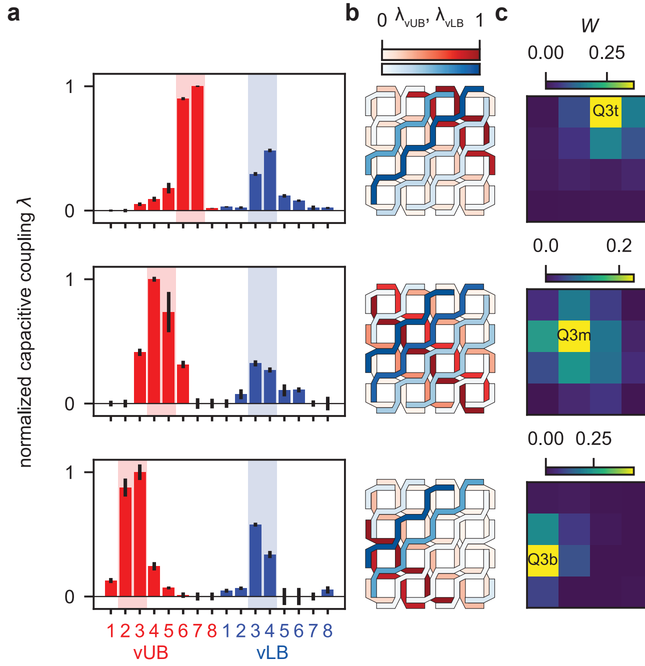

Figure 4.3: **Quantum dot identification. a,** Bar plots of the (normalized) capacitive couplings λ of the barrier gates to the transition lines (in red for the vUB, and in blue for the vLB virtual gates) obtained by analyzing three different sets of transition lines coupled to the virtual plunger vP3. Middle and bottom panels are extracted from the shift of the transition lines at ~ (-20, -63) and (-15, -7) in Fig. 4.2, respectively. The top panel (relative to dot Q3t) is obtained from a measurement shown in Figs. 4.25g,h, where the transition line is more visible. Red and blue backgrounds are added to emphasize the two barriers with the highest couplings. The data points correspond to the peak of the chart bars as well as the centers of the error bars. Each error bar is the standard deviation of the parameter obtained from the linear fit. **b,** Device layout with the capacitive couplings color-coded on the filling of the gate lines. Here, both the vUB and vLB capacitive couplings, λ_{vUB} and λ_{vLB}, are normalized to their maximum values. **c,** Visualisation of the probability (W) calculated from of the shift of the three sets of addition lines (see section 4.4 for details). The comparison of the top, middle, and bottom panels of **a, b, c** clearly distinguishes the three Q3 quantum dots.

Our setup allows for fast charge stability maps, albeit of a size that it is often insufficient to fully visualise the absence of further transition lines in the zero charge state. Therefore, we perform repeated scans of the kind ΔvPx vs ΔvPy, while increasing the dc voltage vPx in discrete steps of 10 mV. We stop the sequence when the quantum dot controlled by vPx, say Qx, is fully depleted. We present these emptying sequences in videos 1-12 described in section 4.11, where we use the addition lines or the interdot transitions to monitor the charge occupancy.

In general, multi-dot transition lines, low charge sensitivity, spurious quantum dots and low reservoir-tunnel coupling may complicate the assessment of the occupancy. In fact, quantum dots that are located in the core of the array are loaded/unloaded by means of cotunneling processes via the outer dots [29], leading to latching transition lines and elongated charge interdot transitions when the reservoir-dot tunnelling time

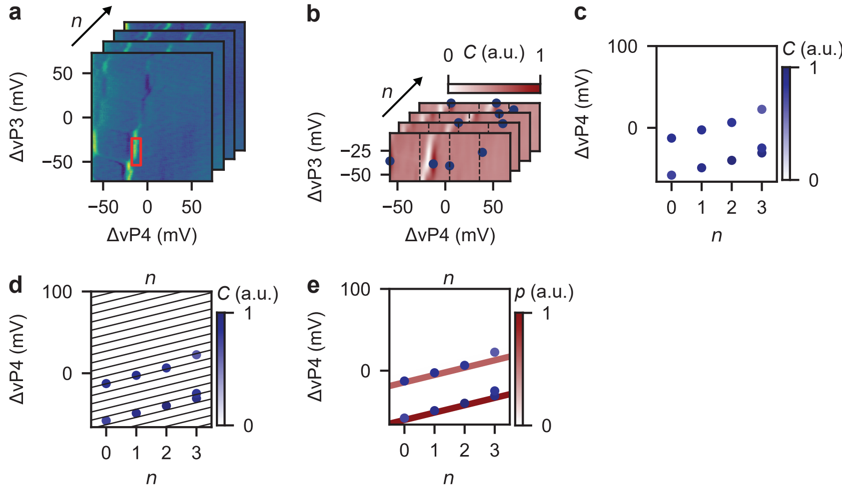

Figure 4.4: **Charge transition detection algorithm. a-e** Illustration of the detection algorithm on the Q4b charge transition lines. From the charge stability diagrams in **(a)**, labeled with the index n, we compute the image correlation (C) maps in **(b)**, with the reference feature in the red box in **(a)** containing a portion of a Q4b charge transition. After splitting the correlation maps in 4 vertical sections (dashed lines in **(b)**) we determine the local maxima in each of them (blue markers in **(b)**). We track the thresholded local maxima across all the scans of the sequence, as displayed in **(c)**. We quantify the occurrence of high-correlation features along potential lines with a fixed expected slope and varying intercept, black lines in **(d)**. In **(d)**, we show only one-fifth of the actual sampling lines for clarity. In **(e)**, we color-code all the potential lines according to their associated p. Emerging peaks in p (i.e., red traces) identify the actual first two Q4b charge transitions.

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approaches the timescale of our scan (∼ 0.01 s) [30]–[33]. We note that adding reservoirs within the array may reduce this effect and simplify the tune-up. However, optimal qubit operation and high qubit connectivity may require low tunnel coupling between qubits and reservoirs. Thus, initialising the array without having each quantum dot strongly coupled to a reservoir is highly relevant [7], [11], [34].

To track specific transition lines in complex multi-dot charge stability diagrams, we have defined an algorithm based on image correlation analysis, which may be refined by machine learning methods [27], [35]–[37]. First, we select a small window from a specific charge stability diagram in the sequence containing a Qx charge addition line. We refer to this as the Qx reference feature as shown in Fig. 4.4a for Q4b. Second, we compute digital image correlation (C) maps of all the charge stability diagrams in the sequence with respect to the previously defined reference feature (section 4.12). Then, we divide the correlation maps into four sections (delimited by the vertical dash lines in Fig. 4.4b), with a size that is smaller than the typical addition voltage. This choice results in a high probability of having, at most, a single occurrence of a Qx charge transition per section. We then select the coordinates of the points with maximum correlation in each section, and threshold them to ensure that only points with high correlation are passed.

Because of the dc voltage step between each map, the same high-correlation feature, if reproducible, is then expected to be found at a ΔvPx value that is 10 mV higher than in the previous charge stability diagram (Fig. 4.4c). Therefore, in a plot of coordinates with

high correlation vs scan index (n), we expect these points to follow a line with a well-defined slope of 10 mV/scan. To assess the presence of possible charge transition lines within the clouds of high-correlation coordinates, we consider a series of potential lines with slope 10 mV/scan and varying intercept (Fig. 4.4d). We then define the quantity p that accounts for the density of high-correlation points falling along each line. In practice, p represents a quantum dot transition-line likelihood (Fig. 4.4e), and details on its mathematical description are discussed in section 4.12).

Figs. 4.5a-u present the detected coordinates with high correlation of all the 16 quantum dots as a function of scan index and associated stepped voltage, together with all possible transition lines plotted with a colour that is proportional to their respective p. High values of p are rendered as visible lines intercepting several high-correlation features, enabling a rapid visualisation of the charge transition lines of all the quantum dots of the array.

By comparing all the panels, we can resolve a small shared-gate voltage window around the tuning point defined by ΔvPx =0 at the largest n where all the quantum dots are in the odd charge regime (also see Fig. 4.19).

While the algorithm is successful in detecting the transition lines of every quantum dot, we note that it returns a false-positive line for the case of Q3b. The first visible Q3b transition, labelled with a star in Fig. 4.5i is in reality an outlier due to a detected feature at $n = 0$ and ΔvP3 ~ 55 mV not related to Q3b, but due to an artefact of a charge sensor, that is clarified in section 4.11. While the algorithm is remarkably strong in detecting the transitions, a definite conclusion on the odd occupancy is most likely only achieved by performing coherent operation on each qubit.

INTERDOT COUPLINGS CONTROL

The ability to selectively tune the interdot coupling in a quantum dot architecture is crucial for generating exchange-based entanglement between semiconductor qubits [9]. Here, inspired by the word and bitlines approach as in dynamic random-access memories [14], [17], we exploit the double barrier design to spatially define and activate unique points in the grid structure. Conceptually, each two-barrier intersection point can be set by the respective voltages in the four configurations: (ON, ON), (ON, OFF), (OFF, ON), (OFF, OFF). For selective two-qubit operations in qubit arrays, the voltage set points should be calibrated such that only when both barriers are in the ON-state a two-qubit interaction is activated, leaving all the other pairs non-interacting (also see Fig. 4.20).
Here, we implement a proof-of-principle of this method by demonstrating two-barrier control of the interdot tunnel coupling in a horizontal and a vertical pair of quantum dots. To this end, we investigate the tunnel coupling variations of the horizontal Q6b-Q7 and vertical Q6t-Q7 quantum dot pairs as a function of the two intersecting barriers. Starting from the respective UB4 and LB7 gates, we define the virtual barriers t_{6b7} and j_{6b7} (section 4.4), which separate the quantum dots Q6b and Q7, while keeping their detuning (e67) and on-site (U67) voltages constant at the (3,1)-(2,2) Q6b-Q7 interdot transition (Fig. 4.6a). After obtaining the detuning lever arm $\alpha_{\epsilon_{67}}$ to convert the detuning voltage into an energy scale ($\Delta\epsilon_{67} = \alpha_{\epsilon_{67}} \cdot \Delta e67$), we evaluate the strength of the interdot couplings by analysing the charge polarisation lines along the detuning axis at ΔU67 = 0 (Figs. 4.6b, c) [38]. By performing this measurement systematically, we demonstrate

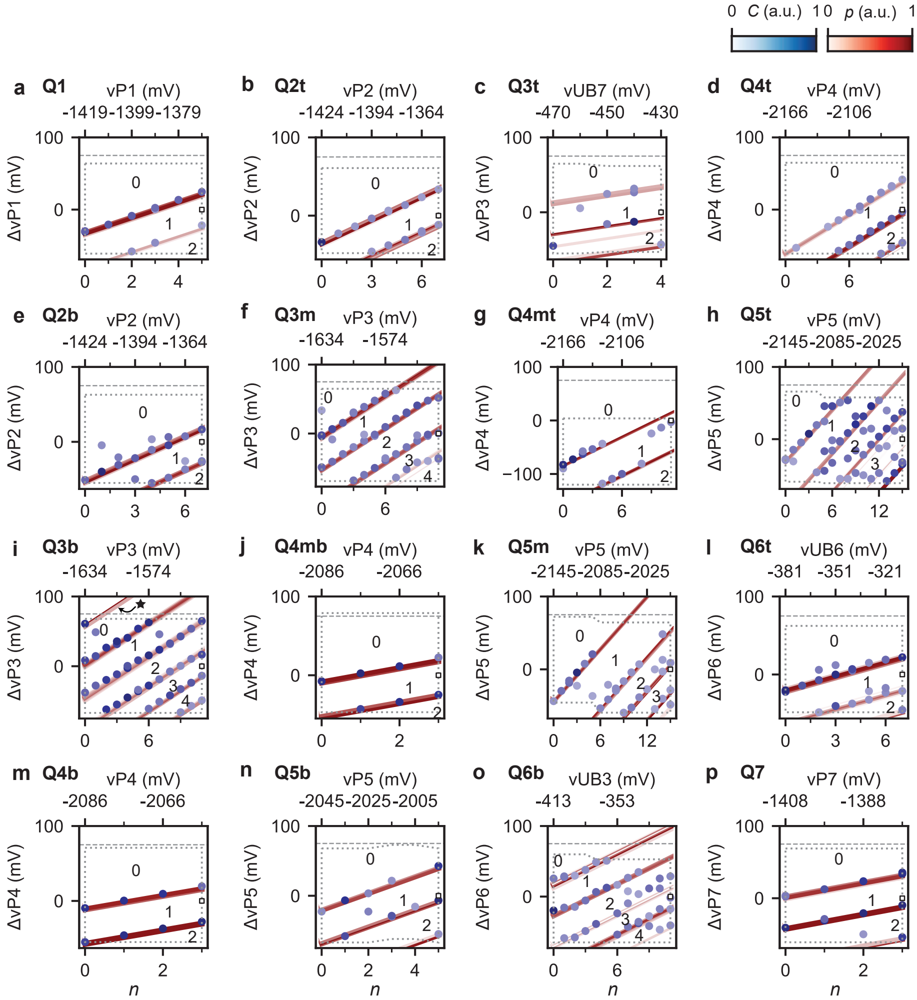

Figure 4.5: **Counting holes in a 16 quantum dot array. a-p,** Same as Fig. 4.2/e for all the 16 quantum dots. The numbers in each plot indicate the quantum dot fillings, according to the algorithm. In 3 cases (Q3t, Q6b, Q6t) out of 16, we step a barrier, rather than a plunger, to better isolate the shift of only one of the dots under the same plunger line. High-correlation features (blue points) are found up to the bounds of the area of the datasets analyzed by the protocol, highlighted by the dotted grey polygon. The horizontal dashed line indicates the actual limit of the dataset. The star in panel **(n)** indicates a false-positive transition line.

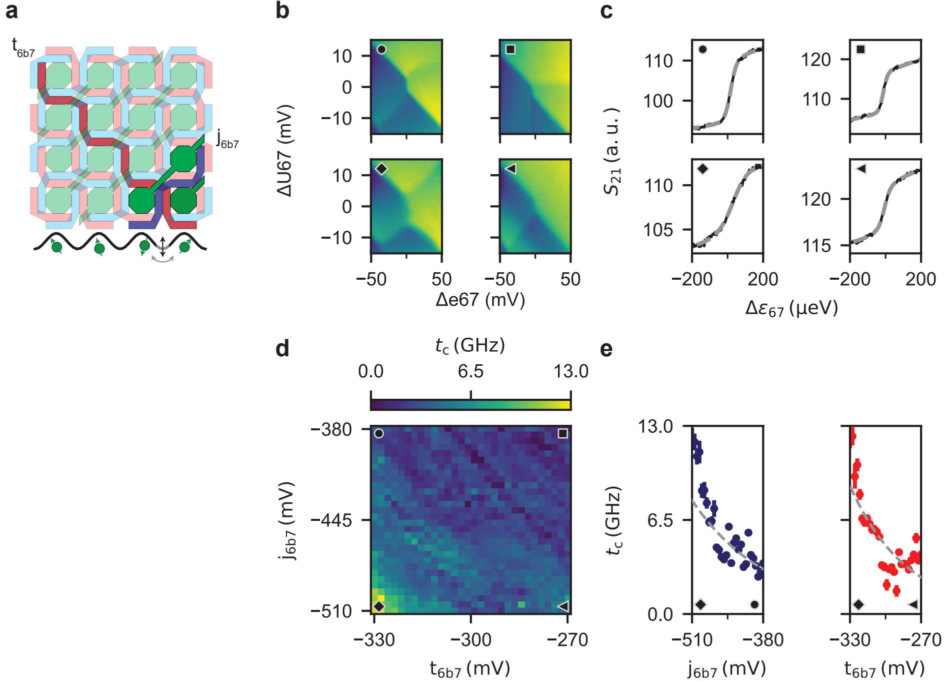

Figure 4.6: **Addressable control of the horizontal interdot tunnel coupling using double barrier gates. a** Schematics of the crossbar indicating the two intersecting barriers (in red and blue) controlling the Q6b-Q7 interdot tunnel coupling. **b** Exemplary charge stability diagrams taken via reflectometry methods showing the (Q6b,Q7) charge states at four different virtual barrier voltage configurations near the (3,1)-(2,2) transition. At the centre of the panels, the vertical interdot transition line is clearly visible. The circle, square, diamond, and triangle markers correlate each map to the voltages, $(t_{6b7}, j_{6b7}) = -(330,380), (270,380), (330,510), (270,510)$ mV, respectively. **c** Charge polarisation traces (black) relative to panel **(b)**, together with best fit (dashed grey). **d** Colour map of the two-axis controlled tunnel coupling of the systems Q6b-Q7, with markers located at the respective voltages. We note that a variation of a virtual barrier corresponds to the same variation of the real gate. **e** Vertical (left panel) and horizontal (right panel) linecuts of **(d)** at $t_{6b7} = -330$ mV and $j_{6b7} = -510$ mV, respectively. Grey traces are fits with an exponential function of the data, from which we obtain the four effective barrier lever arms (section 4.4).

that the tunnel coupling can be controlled effectively by both barriers (Figs. 4.6d,e). At values of $(t_{6b7}, j_{6b7}) = (-270, -380)$ mV, the coupling is virtually OFF, but our method is inherently not accurate for $t_c \leq 3$ GHz, because the thermal energy dominates the broadening of the polarisation line [32], [38]. In contrast, upon activating both barriers at $(t_{6b7}, j_{6b7}) = (-330, -510)$ mV, the tunnel coupling is turned on following approximately an exponential trend (section 4.4). Within the displayed voltage range, we can tune it well above 10 GHz, much higher than in the configuration in which only one barrier is activated. We perform the same experiment on the dots pair Q6t-Q7 by defining the virtual barriers t_{6t7} and j_{6t7} based on the gates UB5 and LB7, respectively (Fig. 4.7a and section 4.4). Using the same barrier voltages window as for Q6b-Q7, we find that the coupling tunability of the pair Q6t-Q7 is comparable to the previous pair, with a virtually OFF state (≤3 GHz) at $(t_{6t7}, j_{6t7}) = (-270, -380)$ mV, and with a ON state reaching 20

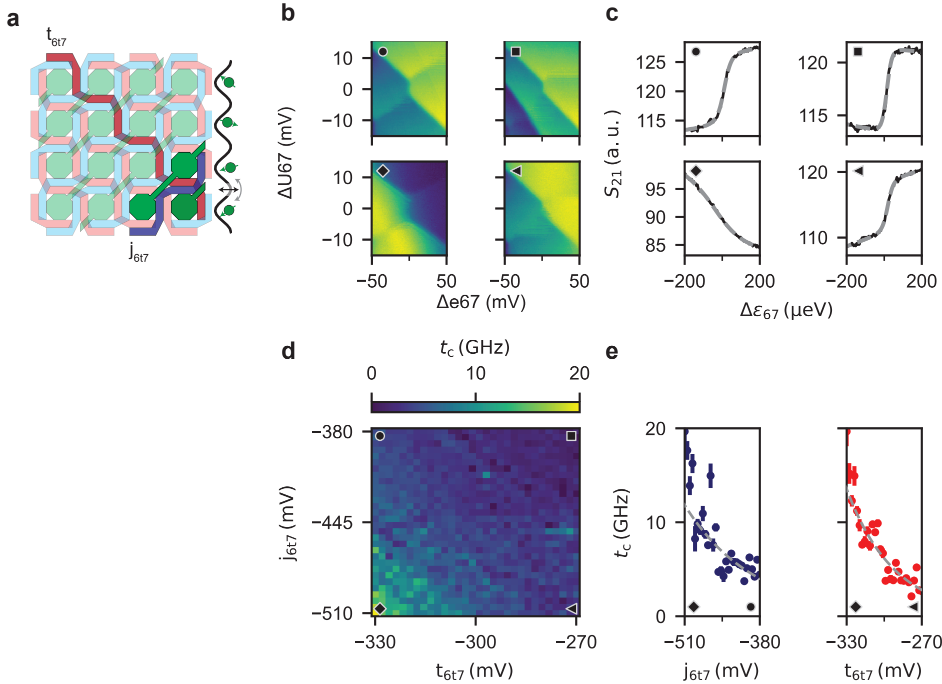

Figure 4.7: **Addressable control of the vertical interdot tunnel coupling using double barrier gates.** Analogous to Fig. 4.6 but for the vertical quantum dot pair Q6t and Q7 and barrier voltages t_{6t7}, j_{6t7}.

GHz at $(t_{6t7}, j_{6t7}) = (-330, -510)$ mV (Figs. 4.7b-e). These results are corroborated by the two-barrier tunability of the interdot capacitive coupling for both double-dot systems (shown in Fig. 4.21) and by the tunability of another dot pair (shown in Fig. 4.22). We envision that for rapid qubits exchange operations at the charge symmetry point, the required barrier voltage window might be different from our measurable window via polarisation lines. Specifically, for state-of-the-art values of ON (OFF) exchange interaction of 50 MHz (10 KHz) and a typical charging energy of 1 mV, the required tunnel coupling is ~ 2 (0.02) GHz, which can be better calibrated via qubit spectroscopy techniques [21], [39], [40].

4.3. CONCLUSIONS

By implementing a strategy that allows to address a large number of quantum dots with a small number of control lines, we have operated the most extensive two-dimensional quantum dot array so far. With this approach, the number of gate layers is independent of the grid size, which greatly simplifies the nanofabrication of quantum dot arrays. With the introduction of a double barrier paradigm and a statistical method for labelling multi-dot charge stability diagrams, we have demonstrated two critical requirements for quantum logic in shared-control architectures: the tunability of 16 interacting quan-

tum dots into an odd charge state with an unpaired spin and the proof of principle of a method for the selective control of the interdot tunnel coupling, which is crucial for the control of the exchange interaction. We envision that future crossbar arrays may find applications in large and dense two-dimensional quantum processors or as registers that are coupled via long-range quantum links for networked computing.

4.4. METHODS

FABRICATION

The device is fabricated on a Ge/SiGe heterostructure where a 16-nm-thick germanium quantum well with a maximum hole mobility of $2.5 \cdot 10^5\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ is buried 55 nm below the semiconductor/oxide interface [26], [41]. We design the quantum dot plunger gates with a diameter of 100 nm, and the barrier gates separating the quantum dots with a width of 30 nm. The fabrication of the device follows these main steps. 30 nm-thick Pt ohmic contacts are patterned via electron-beam lithography, evaporated and diffused in the heterostructure following an etching step to remove the oxidised Si cap layer [42], [43]. A three-layer gate stack is then fabricated by alternating the atomic layer deposition of a Al_2O_3 dielectric film (with thicknesses of 7, 5, 5 nm) and the evaporation of Ti/Pd metallic gates (with thicknesses 3/17, 3/27, 3/27 for each deposition, respectively). After dicing, a chip hosting a single crossbar array is then mounted and wire-bonded on a printed circuit board. Prior to the cool down in a dilution refrigerated, we tested in a 4 K helium bath two nominally identical crossbar devices following the screening procedure shown in ref. [39]. Both devices exhibited full gates and ohmic contacts functionality, and one of them was mounted in a dilution refrigerator.

EXPERIMENTAL SETUP

The experiment is performed in a Bluefors dilution refrigerator with a base temperature of 10 mK. From Coulomb peaks analysis, we extract an electron temperature of 138 ± 9 mK, which we use to estimate the detuning lever arm (Fig. 4.23 and 4.24). We utilise an in-house built battery-powered SPI rack https://qtwork.tudelft.nl/~mtiggelman/spi-rack/chassis.html to set direct-current (dc) voltages, while we use a Keysight M3202A arbitrary waveform generator (AWG) to apply alternating-current (ac) rastering pulses via coaxial lines. The dc and ac voltage signals are combined on the PCB with bias-tees and applied to the gates. Each charge sensor is galvanically connected to a NbTiN inductor with an inductance of a few μH forming a resonant tank circuit with resonance frequencies of ~ 100 MHz. In our experiment we have observed only three out of four resonances, likely due to a defect inductor. Moreover, because two resonances overlap significantly, we mostly avoid using reflectometry (unless explicitly stated in the text) and use fast dc measurements with bandwidth up to 50 kHz. The four dc sensor currents are converted into voltages, amplified and simultaneously read out by a four-channel Keysight M3102A digitizer module with 500 MSa/s. The digitizer module and several an arbitrary waveform generator (AWG) modules are integrated into a Keysight M9019A peripheral component interconnect express extensions for instrumentation (PXIe) chassis. Charge stability diagrams here typically consists of a 150x150 pixels scan with a measurement time per pixel of 50 μs. Throughout this article, we refer to Δgi to identify

a ramp supplied by an AWG to the gate gi with respect to a fixed dc reference voltage. To enhance the signal-to-noise ratio, we average the same map 5-50 times, obtaining a high-quality map within a minute.

TUNE-UP DETAILS

Throughout the experiment, we have tuned all 16 quantum dots of the device two times. In the first run, the gate voltages were optimised to minimise the number of unintentional quantum dots in order to better visualise and characterise the crossbar quantum dots (Fig. 4.2, 4.3, 4.25 and 4.26). In the second run, the stray dots were neglected to tune the quantum dot array into a global odd-occupation regime (Fig. 4.5). Between the two tune-up cycles, the gate voltages were reset to zero without thermal cycling the device. The protocol followed in the two tuning procedures was the same, but the need for emptying accidental quantum dots in the first session led to some restrictions in the voltage window of certain gates. The starting gate voltage values for the tune-up are -300 mV for the barriers and -600 mV for the plungers. In Fig. 4.27 we display the dc gate voltages relative to the measurements displayed in Fig. 4.5, with the crossbar array tuned in the odd-charge occupation. In this regime, we also study the variability of the first hole voltage onset in each dot obtaining -1660 ± 290 mV (Fig. 4.28). Furthermore, we characterise the variability of the transition lines spacing to be $\sim 10-20\%$ as a metric for the level of homogeneity of the array (Fig. 4.29) [44]. Strategies to further reduce these variations are discussed in section 4.8.

The odd charge occupancy is demonstrated by emptying each quantum dot as shown in Suppl. Videos 1-12. All the datasets underlying Fig. 4.5 and in Suppl. Videos 1-12 are taken at the same gate voltage configuration on the same day. Still, across all the maps, there are minimal voltage differences, the largest is a variation of 6 mV in vP1 that however does not affect the Q1 and Q2b, Q2t occupancies (Tab. 4.2). During the experiment, the gate UB8 did not function properly, possibly due to a broken lead. To compensate for this effect and to enable charge loading in the dots P3t and P5t, we set UB7 at a lower voltage compared to the other UB gates. Additionally, LB1 is set at a comparatively higher voltage to mitigate the formation of accidental quantum dots under the fanout of LB1 and P1 at lower voltages. The first addition line of such an accidental quantum dot is visible as a weakly interacting horizontal line in Fig. 4.4a.

VIRTUAL MATRIX

The matrix M defined by $\vec{G} = M \cdot \mathrm{v}\vec{G}$, with virtual gates $\mathrm{v}\vec{G}$ and actual gates $\vec{G}$ is shown as a colour map in Fig. 4.10. For the tunnel coupling experiments presented in Fig. 4.6 and 4.7, we employ additional virtual gate systems for achieving independent control of the detuning voltage e67 and U67, and of the interdot interactions via virtual barriers t_{6b7}, j_{6b7}, t_{6t7} and j_{6t7}. With SE_P the SE plunger gate, we write:

$$\begin{pmatrix} \mathrm{P5} \\ \mathrm{P6} \\ \mathrm{P7} \\ \mathrm{SE_P} \end{pmatrix} = \begin{pmatrix} 0.04 & -1.2 \\ -0.5 & 0.9 \\ 0.492 & 0.9 \\ -0.08 & -0.26 \end{pmatrix} \begin{pmatrix} \mathrm{e67} \\ \mathrm{U67} \end{pmatrix}$$

$$\begin{pmatrix} \text{P6} \\ \text{P7} \\ \text{UB5} \\ \text{LB7} \\ \text{SE_P} \end{pmatrix} = \begin{pmatrix} -1.28 & -0.33 \\ -1.18 & -0.72 \\ 1 & 0 \\ 0 & 1 \\ 0.15 & -0.01 \end{pmatrix} \begin{pmatrix} \text{t}_{6\text{t}7} \\ \text{j}_{6\text{t}7} \end{pmatrix}$$

$$\begin{pmatrix} \text{P6} \\ \text{P7} \\ \text{UB4} \\ \text{LB7} \\ \text{SE_P} \end{pmatrix} = \begin{pmatrix} -2.05 & -0.97 \\ -1.18 & -0.41 \\ 1 & 0 \\ 0 & 1 \\ -0.19 & -0.01 \end{pmatrix} \begin{pmatrix} \text{t}_{6\text{b}7} \\ \text{j}_{6\text{b}7} \end{pmatrix}$$

4

QUANTUM DOT IDENTIFICATION

To obtain the capacitive coupling of all the barrier gates to a set of transition lines (as shown in Fig. 4.3a), we acquire and analyse sets of 112 charge stability diagrams. The same charge stability diagram is taken after stepping each barrier gate around its current voltage in steps of 1 mV in the range of -3 to 3 mV (i.e., 7 scans x 16 barriers). The number of charge stability diagrams required to identify all quantum dots scales linearly with their total number. The number of maps results from the product of the number of plunger and barrier gates, which both scale as its square root. We emphasise that an array with individual control would also require a linear number of charge stability diagrams to infer each dot. In the analysis, we first subtract a slowly varying background to the data (with ndimage.gaussian.filter of the open-source scipy package) and then calculate the gradient of the map (with ndimage.gaussian_gradient_magnitude). For a given line cut of such two-dimensional maps, we extract the peaks position using a Gaussian fit function. Due to cross capacitance, the transition line positions manifest a linear dependence on each of the 16 barriers, which we quantify by extracting the linear slope (Fig. 4.11). After normalisation to the maximum value, these parameters are named capacitive couplings (λ), and, because of the grid structure of the two barrier layers, provide a first information of where the hole is added/removed to/from. To extract the quantum dot positions, we consider the capacitive couplings to the vUB (λ_{vUB}) and vBL (λ_{vLB}) gates as two independent probability distributions. With this approach, the integral of the λ_{vUB} (λ_{vLB}) between vUBi (vLBk) and vUBj (vLBl) returns a "probability" $p_{U,(i,j)}$ ($p_{L,(k,l)}$) to find the dot in-between these control lines. As a result, the combined probability in the site confined by these four barriers is given by the product of these elements: $w_{(i,j),(k,l)} = p_{U,(i,j)} \cdot p_{L,(k,l)}$. We note that the sum of the 16 probabilities returns 1. As already observed in ref. [33], the gates cross-coupling to a specific quantum dot defined in a germanium quantum well manifest a slow falloff in space (i.e., gates with a distance to the dot of > 100 nm still have a considerable cross-coupling to the dot). This can be attributed to the rather large vertical distance between the gates and the quantum dots (> 60 nm), and is in contrast with experiments in SiMOS devices where the falloff is rather immediate due to the tight charge confinement. This aspect explains why our probability W at the identified quantum dot reaches at a max of 0.25 – 0.5.

TUNNEL COUPLING EVALUATION

For the estimation of the tunnel coupling results presented in Fig. 4.6 and 4.7, we established an automated measurement procedure that follows this sequence: 1) we step the virtual barriers across the two-dimensional map (t, j); 2) at each barrier configuration, we take a two-dimensional (e67, U67) charge stability map (Figs. 4.6b and 4.7b); 3) we identify the accurate position of charge interdot via a fitting procedure of the map (Fig. 4.21) [45]; 4) we perform small adjustments at the e67, U67 virtual gates to centre the interdot at the (0,0) dc-offset; 5) measure the polarisation line by using ~0.1 kHz AWG ramps (Figs. 4.6c and 4.7c). For an accurate analysis, each polarisation line is the result of an average of 150 traces, using a measurement integration time of 50 μs per pixel. With this method, the full 30x30 maps are taken in a few hours. We fit the traces considering an electron temperature of 138 mK and a detuning lever arm of $\alpha_{\epsilon_{67}} = 0.012(4)$ eV/V, extracted from a thermally broadened polarisation line (Fig. 4.24). We observe that the extracted tunnel coupling follows approximately an exponential trend as a function of the barrier gates. We fit the data presented in Figs. 4.6e and 4.7e with the function $A \cdot e^{-BV_g}$, with A a prefactor, B the effective barrier lever arm and V_g the gate axis. We find that the effective barrier lever arms of j_{6b7} and t_{6b7} are 0.007 ± 0.002 and $0.021 \pm 0.003\,\mathrm{mV^{-1}}$, respectively. Similarly, we find for j_{6t7} and t_{6t7} values of 0.008 ± 0.001 and $0.026 \pm 0.003\,\mathrm{mV^{-1}}$, respectively. This indicates that the real barrier LB7 controls the vertical and horizontal coupling in a similar manner. Altogether these results indicate that the lower barrier layer of UB gates is ~ 3 times more effective than the upper barrier layer of LB gates. This is consistent with what is found in Fig. 4.3a and Fig. 4.13. We note that for qubit operations in such crossbar array, it is actually necessary to fully characterise and calibrate the two-barrier tunability of all the 24 nearest-neighbours. Performing this task requires improving further our hardware implementation and is beyond the scope of this work.

4.5. RENT'S RULE AND GATE COUNT

Scalable architectures impose stringent requirements at all layers of the quantum computing stack [5]. If we focus on the lowest layers of the computing stack, state-of-the-art solid-state quantum processors do not meet these prerequisites yet [8]. In fact, current processors still make use of a few control terminals per qubit, an approach that will lead to arduous interconnectivity and control challenges in the route toward millions qubits [46], [47]. To quantify the level of optimisation and interconnectivity of a quantum processor, we borrow the concept of Rent's rule from classical electronics [48]. In quantum dot devices, the Rent's rule can be used to correlate the number of control terminals T (i.e., gates, ohmic leads,...) and the number of active components g (i.e., quantum dots or qubits):

$$T = tg^p \tag{4.1}$$

where t is the average number of control terminals per qubit and p is the Rent exponent that lies in the range $(0, 1]$. Without any quantum hardware optimisation, the number of terminals will keep increasing linearly with the number of qubits, creating major interconnect problems in the quantum computing stack [8].

An analogous challenge emerged in the 1950s in classical electronics when every elec-

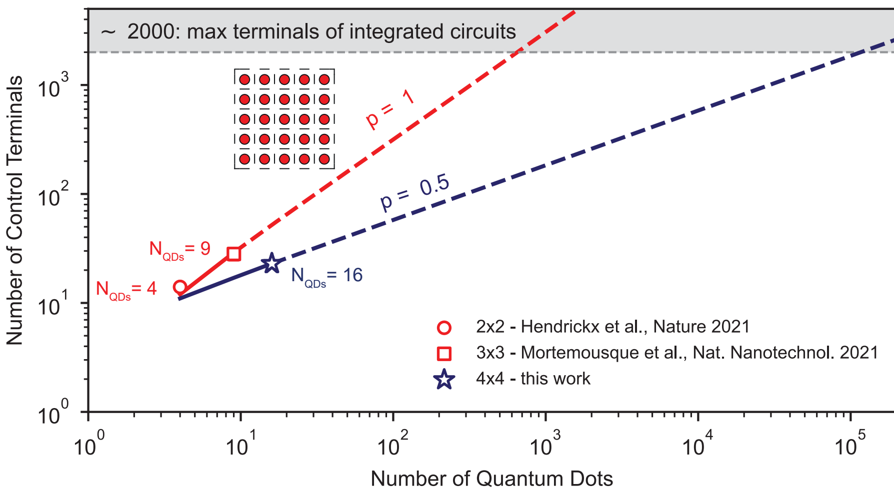

Figure 4.8: **Rent's rule in two-dimensional quantum dot architectectures and gates count.** Number of control terminals (gates) versus the number of quantum dots for a two-dimensional array. The blue trace indicates the scaling of our shared-control gate architecture. The red trace shows the scaling for an architecture with individual control (inset) of interdot couplings and quantum dot energies. Scatter points represent the gates counts of a 2x2 [39], 3x3 [49] and 4x4 quantum dot array (this chapter). We draw a horizontal line at 2000 control terminals, which currently identify the current maximum number of input/output terminals of classical integrated circuits. Assuming this as a practical limit for the control terminals of a quantum processor without on-chip control logic [7], the individual control strategy is limited to control up to a few hundred quantum dots. In contrast, the shared control approach may be able to control few hundreds of thousands.

trical component needed to be soldered to several others [50]. The turning point was the invention of the integrated circuit, which led to the realisation of the first microprocessor - the Intel 4004 - with 2300 transistors and only 16 external pins. Nowadays, integrated

circuits are at the heart of our technology and, with a Rent exponent of about 0.5 and a maximum number of input/output lines of $T \sim 2 \cdot 10^3$, present a ratio of transistor to input/output pins g/T of $\sim 10^6$ [7], [51]. On the contrary, in infant quantum chips, the g/T ratio is below 1 [8], and therefore, significant efforts have to be made to downscale the quantum Rent exponent.

In our work, we have moved from electrostatic gating strategies with individual control of every unit to crossbar architectures with shared control of quantum dots energies and interdot couplings [17]. This advance is crucial for scalability because it may enable to use $O(N^{1/2})$ terminals for $O(N)$ qubits (i.e., $p = 0.5$). The impact of this strategy can be visualised in Fig. 4.8, where we compare the different scalings of control terminals for a two-dimensional quantum dot array controlled with a shared- and with an individual-control approach. For the shared-control architecture presented in this chapter, the gates count as a function of quantum dots g is given by:

$$T = 6g^{1/2} - 1 \propto 6g^{1/2} \tag{4.2}$$

while for an architecture with individual control of all the on-site dot energies and interdot couplings (see inset of Fig. 4.8), we obtain:

$$T = 3g + 2g^{1/2} - 4 \propto 3g \tag{4.3}$$

These equations hold for square arrays with a minimum 2x2 size, i.e., $g \geq 4$.

Scaling the crossbar architecture to a 6x6 crossbar array would already result in a device with fewer gates than total number of quantum dots. In particular, a 6x6 crossbar array with 36 quantum dots requires only 35 gates. We note that while this may seem a marginal improvement, comparing the required number of gates to quantum dot devices with individual connectivity shows already a remarkable difference: a 4x4 (6x6) quantum dot device requires 23 vs 52 (35 vs 116), for the respective systems.

We emphasise that in these considerations we do not account for the terminals controlling the read-out charge sensors. In the future, a strategy for integrating charge sensors within quantum dot crossbar arrays needs to be fully worked out to establish and operate scalable modules of semiconductor qubit arrays with a Rent exponent of 0.5. We note that germanium can make ohmic contacts to metals, thus facilitating a very small footprint for charge sensors, and providing a route toward the integration of charge sensors in the quantum dot array.

4.6. TYPICAL CHARGE SENSORS RESPONSE

To read out the charge states of the 16 quantum dots, we prepare four charge sensors in the Coulomb blockade regime, as demonstrated by the transport features in Fig. 4.9, and operate them at the steepest points.

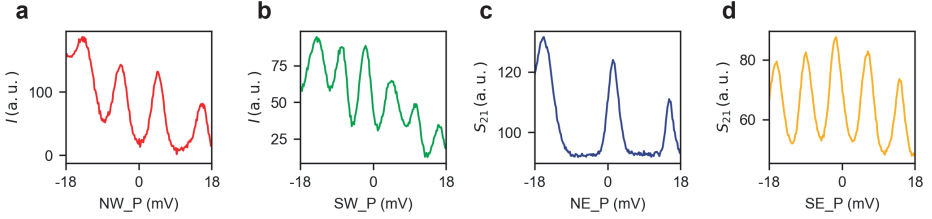

Figure 4.9: **Typical charge sensor responses. a, b** Direct-current I via the NW and SW sensor. **c, d** Reflectometry signal S_{21} of the NE and SE sensor respectively. The traces are taken as a function of the relative sensor plunger gate.

4.7. VIRTUAL GATE MATRIX

In Fig. 4.10 we display the virtual matrix used in software to define the set of virtual gates. We define the virtual gates such that their variation does not influence the position of the charge sensors Coulomb peak. Concretely, we perform in video-mode fast 2D gate scans of the kind NW_P vs LB1. We then identify the slope of the position of the sensor Coulomb peak in such a 2D map, and set this value to the matrix element (NW_P, vLB1). This method results in the definition of a virtual gate vLB1 that maintains the NW charge sensor tuned. This procedure is iterated across all plunger and barrier gates, and all the charge sensors.

Similarly, virtual plungers are also designed to be able to tune independently the on-site energies of the quantum dots by using only nearest-neighbours compensations as described in refs. [24], [25]. Because multiple sites are controlled by a single plunger line and each of the site can have a slightly different crosstalk to the surrounding gate, our procedure results in an approximation. We note that in this work we have not virtualised the barrier gates beyond the two double dots considered in Fig. 4.6 and 4.7.

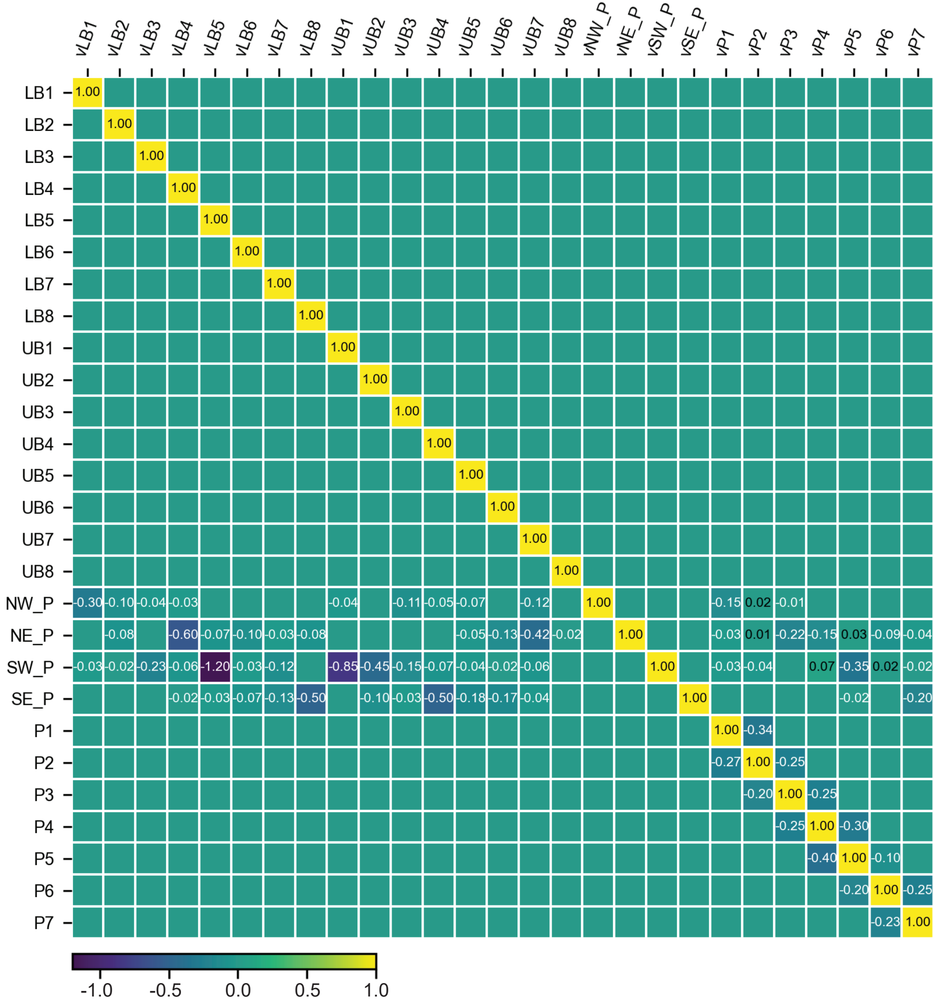

Figure 4.10: **Virtual gate matrix.** Visualization of the virtual gate matrix. Virtual barriers vLBi and vUBi are defined as combination of the relative barriers LBi and UBi with $i \in [1,8]$ and sensor plungers. NW_P, NE_P, SW_P and SE_P identify the plungers of the respective charge sensors.

4.8. PRACTICAL DEVICE IMPROVEMENTS

Here, we present a series of practical ideas to mitigate challenges observed (and not) throughout the experiment.

1. The tune-up of the current implementation is complicated by the emergence of a few (~ 5) unwanted stray dots outside the array, located under the dense gates fanout. These decrease the read-out sensitivity to the designed quantum dots and, in general, complicate the system tune-up.
   Near-term solutions can be: the addition of a lower "screening" gate layer (kept at a more positive voltage), or an upper "depleting" gate layer that prevents any charge puddles from forming in between different gate lines. A more sophisticated solution consists of the implementation of vertical interconnect access through the oxide layer that enables to fan out the gate lines at a much higher level in the stack [28]. We also envision that, in the future, boundary effects of large qubit arrays need to be accounted for (e.g., dots at the perimeter of the array experience a smaller electric field than the ones in the middle). Hence, another possibility is to neglect the dots at the perimeter completely.

2. A faster device tune-up can be achieved by using radio frequency reflectometry, which, in our experiment, worked out only partially.

3. A higher level of homogeneity and functionality than is presented here will be needed for practical quantum computation with quantum dots. Leaving aside the development on the material stack itself (Ge/SiGe) and on the device nanofabrication, there appears to still be space for improvements on the gate layout.
   Similarly to the behaviour of the turn-on voltages in transistors [52], a higher quantum dot homogeneity may be achieved by increasing their size. This will also have the beneficial effect of increasing the plunger gates lever arm, which will be less screened by the lower layers. Clearly, an excessively large quantum dot can lead to (Pauli spin-blockade) read-out problems if the energy of the first excited state is too low. Therefore a search for an optimal size needs to be performed.

4. Other strategies can be adopted in the near future to further improve the level of quantum dot uniformity. In particular, a method presented in chapter 5 and 6 relies on engineering the electrostatic landscape using the hysteretic shift of the gate voltage characteristics.

5. In the current device, we observed that the ratio of the two barrier layers lever arms is approximately 2-3. Due to imperfections in the nanofabrication and an oxide layer in between them, the top layer partially overlaps the bottom one. As a consequence, its electric field is screened. To enhance the coupling of the top layer, one can design the top layer to have a slightly larger width, or add a gap of a few nm in between the two lines.

4.9. QUANTUM DOT IDENTIFICATION

To obtain the capacitive coupling of each barrier to each dot, we analyse several charge stability diagrams as shown in Fig. 4.11a. We monitor the position of the transition lines (away from charge interdots) by fitting the derivative of the data with a Gaussian function, after subtraction of a slow-varying background. In the small voltage range that we consider, the extracted peak positions respond linearly to each barrier gate (Figs. 4.11b, c) The normalised slope of the fitted linear function is used to quantify the capacitive coupling of each gate. The latter are plotted as bar plots and visualised on the device layout in Fig. 4.12- 4.16. As described in the Methods, this information can be used to clearly assign each set of transition lines to the dot in the grid.

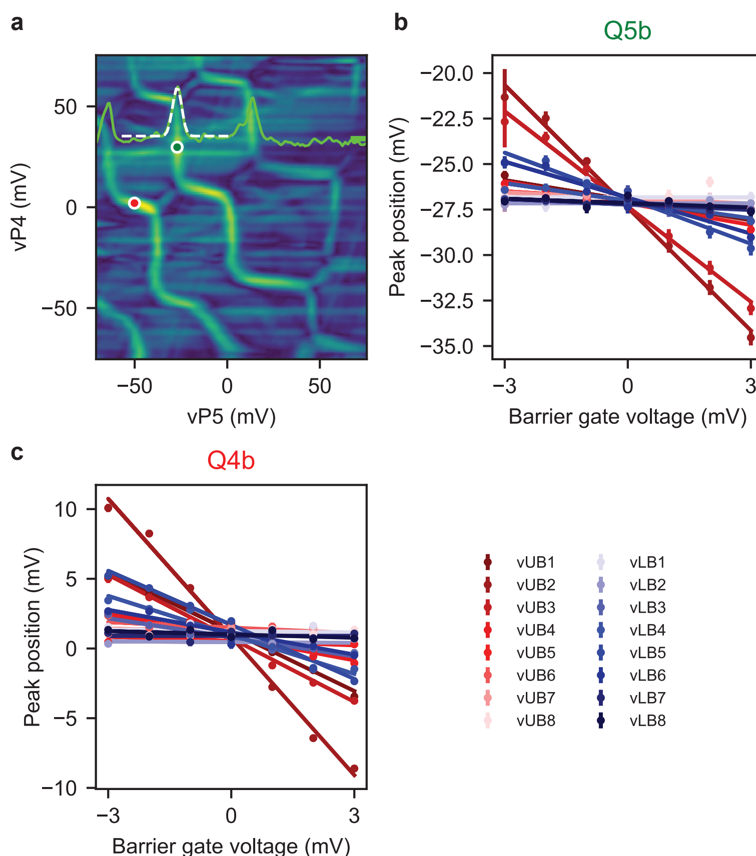

Figure 4.11: **Detecting the shift of the transition lines: an exemplary case. a,** Charge stability diagram (gradient of the SW sensor signal) showcasing a set of vertical and horizontal charge transition lines. The green trace shows the derivative of the data at the vP4 value identified by the horizontal green tick. The white dashed line is a fit of the linecut with a Gaussian function, and the green marker identifies the fitted centre of the peak. The red marker labels the fitted coordinate of a vertical transition line (not shown). **b, c,** Scatter points are the fitted positions of the green and red markers, respectively, as a function of the voltage applied at all barriers. Error bars on the points display the standard deviation of the fitted centre of the Gaussian. Dashed lines are the best linear fit to the data. The normalised absolute values of the slope parameter are taken as capacitive couplings of each gate to the specific transition line. The error bar on the capacitive coupling is taken as one standard deviation of the fitted slope parameter. The horizontal (vertical) transition line in **(a)** is attributed to the quantum dot Q4b (Q5b).

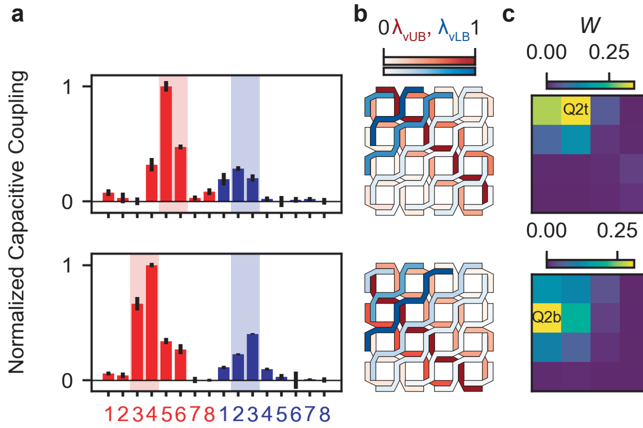

Figure 4.12: **Quantum dot identification of the Q2 quantum dots. a,** Bar plots of the (normalised) capacitive couplings (in red for the vUB, and in blue for the vLB gates) obtained by the analysis of transition lines attributed to different quantum dots as shown in Fig. 4.11. Red and blue backgrounds are added to emphasise the two barriers that surround the labeled quantum dot. **b,** Device layout with the capacitive couplings colour-coded on the filling of the gate lines. The vUB (vLB) capacitive couplings are normalised to their maximum values. Intuitively, the quantum dot associated with the analysed transition lines is located at the intersection of the two intensely coloured red and blue lines. **c,** Extracted probabilities (W) of each set of addition lines (calculated as discussed in section 4.4). The comparison of the top and bottom panels of **a, b, c** clearly distinguishes the two Q2 quantum dots. In **a** the data points correspond to the peak of the chart bars as well as the centers of the error bars. Each error bar is the standard deviation of the parameter obtained from the linear fit.

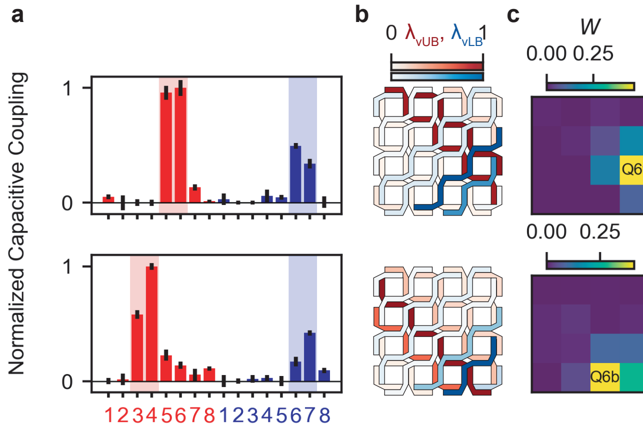

Figure 4.13: **Quantum dot identification of the Q6 quantum dots** Same as in Fig. 4.12 but applied to the Q6 quantum dots. TThe comparison of the top and bottom panels of **a, b, c** clearly distinguishes the two Q6 quantum dots.

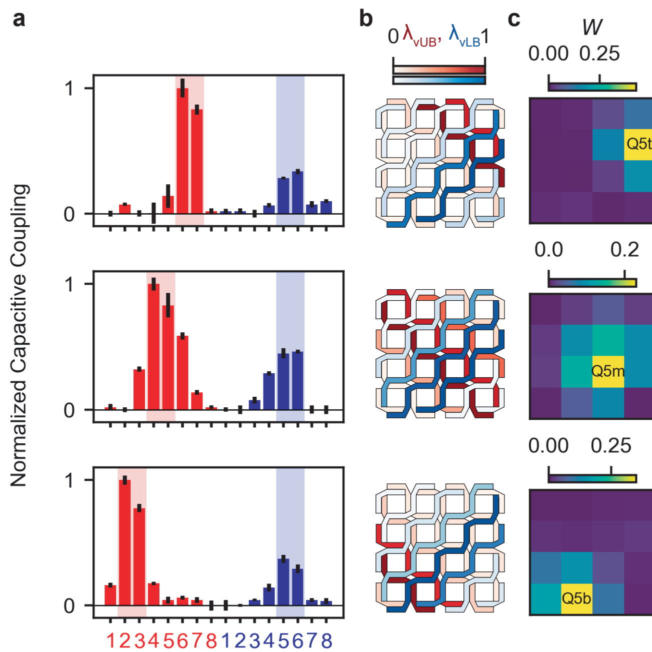

Figure 4.14: **Quantum dot identification of the Q6 quantum dots** Same as in Fig. 4.12 but applied to the Q5 quantum dots. The three different rows of panels **a, b, c** enable to label the Q5 quantum dots.

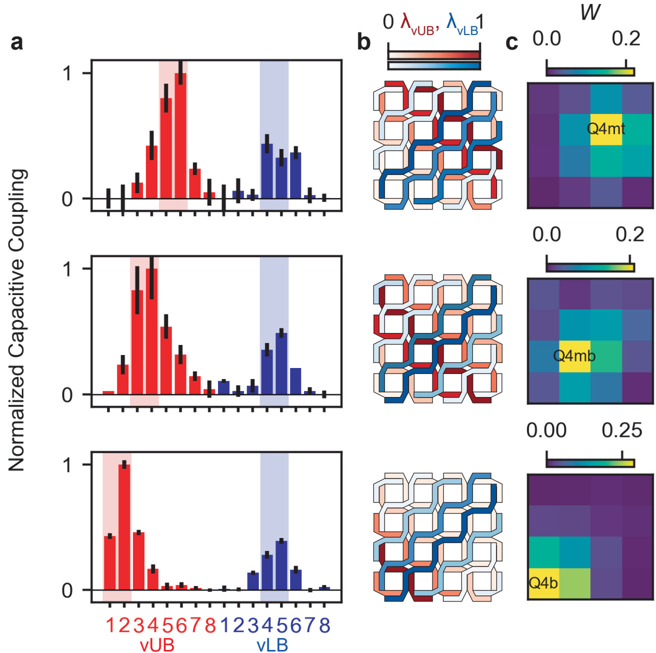

Figure 4.15: **Quantum dot identification of the Q6 quantum dots** Same as in Fig. 4.12 but applied to the Q4 quantum dots. The three different rows of panels **a, b, c** enable to label the Q4 quantum dots. The dot Q4t could not be systematically analysed because, in this gating regime, we observe a slow loading mechanism via the defective barrier UB8 with respect to the timescale of our scan (~ ms). However, because such transition lines are controlled by vP4 (labelled in Fig. 4.25), do strongly respond to vUB7 and vLB5, we can still map them to the site Q4t, in a qualitative way.

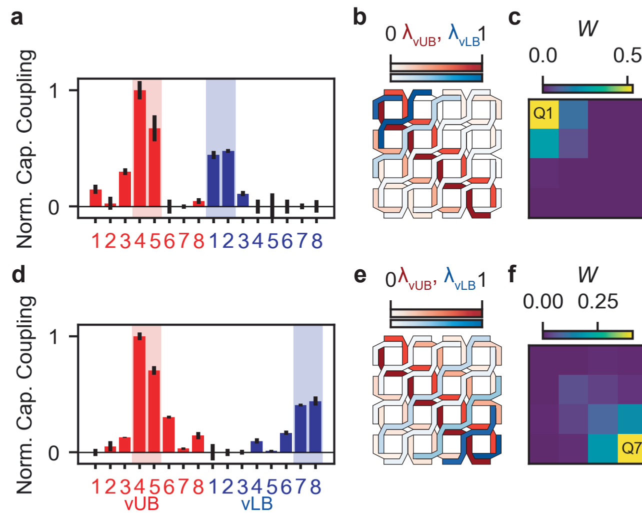

Figure 4.16: **Quantum dot identification applied to the Q1 and Q7 quantum dot** The method in Fig. 4.12 is applied to the two quantum dots controlled by independent plunger lines Q1 and Q7 in panels **a, b, c** and **d, e, f**, respectively.

4.10. SPURIOUS QUANTUM DOT IDENTIFICATION: AN EXAMPLE

We make use of the method presented above to also map the position of accidental quantum dots that arise outside the crossbar array. In Fig. 4.17a, we display the capacitive coupling of the barrier gates to a spurious quantum dot. The addition lines of such a quantum dot are mainly controlled by vP2 and are visible as quasi-vertical lines in the charge stability diagrams of the type ΔvP2 vs ΔvP3 in the Supplementary Videos (see section 4.11). In particular, from these maps, it is possible to observe a negligible mutual capacitance between this specific accidental dot and the crossbar quantum dots Q1, and Q3b. However, we emphasise that the presence of such spurious quantum dot complicates the tuning efficiency of our device, and strategies to mitigate their presence need to be in place in the near future, as already discussed in the main text. In Fig. 4.17b, we present the device layout with the capacitive couplings colour-coded on the filling of the gate lines. Here, both the vUB and vLB capacitive couplings, λ_{vUB} and λ_{vLB}, are normalised to their maximum values. Following this analysis, we can conclude that such spurious quantum dot is approximately located under the fanout of the gates UB1, LB3 and UB3. This is furthermore corroborated by the fact that this dot is well sensed by the SW charge sensor.

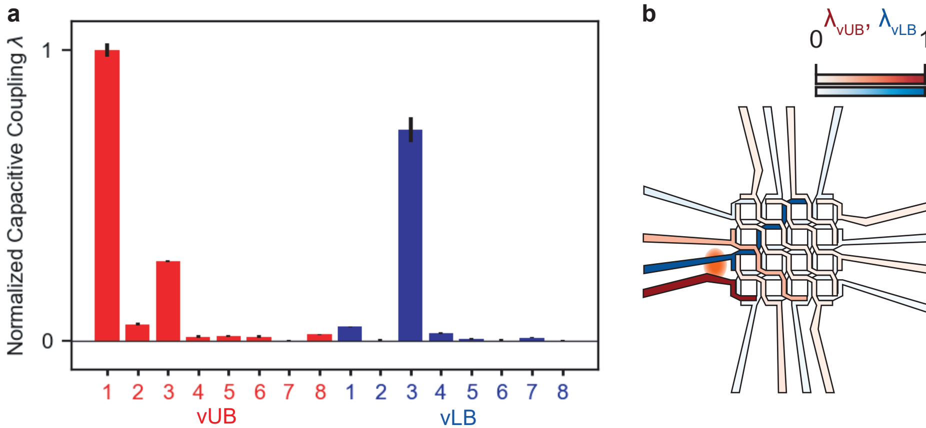

Figure 4.17: **Spurious quantum dot identification. a,** Bar plots of the (normalised) capacitive couplings (in red for the vUB, and in blue for the vLB gates) obtained from the analysis of transition lines attributed to a spurious quantum dot located under the gates fanout. The data points correspond to the peak of the chart bars as well as the centers of the error bars. Each error bar is the standard deviation of the parameter obtained from the linear fit. **b,** Device layout with the capacitive couplings colour-coded on the filling of the gate lines. The vUB (vLB) capacitive couplings are normalised to their maximum values. The orange oval in **(b)** indicates the approximate position of the quantum dot associated with the analysed transition lines (under the fanout of the barriers UB1 and LB3).

Quantum dot	Size of the visible 0th charge state (mV)	1st addition voltage (mV)	Ratio
Q1	111	49	2.3
Q2b	120	46	2.6
Q2t	116	46	2.5
Q3b	71	54	1.3
Q3m	78	46	1.7
Q3t	77	40	1.9
Q4b	96	52	1.8
Q4mb	101	52	1.9
Q4mt	105	64	1.6
Q4t	125	47	2.7
Q5b	107	48	2.2
Q5m	125	54	2.3
Q5t	125	65	1.9
Q6b	66	50	1.3
Q6t	105	50	2.1
Q7	75	44	1.7

Table 4.1: Comparison of the size of the visible 0th charge state in the charge stability diagrams with the addition voltage of each quantum dot. The range in which no transition lines are observed is always larger than 1.3 times the spacing of the first two transition lines.

4.11. DEMONSTRATION OF THE ODD OCCUPATION REGIME VIA VIDEO SEQUENCES

We have combined the stepping charge stability diagrams into videos 1-12 which can be found in the supplementary of ref [1]. In these videos, we present sequences of charge stability diagrams of the type vPx versus vPy with $x, y \in [1, 7]$ and $x \neq y$. Because the maximum amplitude of the arbitrary waveform generator (AWG) ramps at the device is at max ~ 200 mV due to the attenuation in the lines, a single two-dimensional scan is not enough to evaluate directly the number of holes in a quantum dot. Rather, we start from the gate voltage regime presented in the main text Fig. 4.5 and proceed by increasing the dc voltage vPx in steps of 10 mV toward more positive voltages until Qx is fully depleted. At every step, we take a fast two-dimensional scan that allows to label and count the number of transition lines visible in the available gate window. The size of the visible zeroth charge sector is always chosen in all the cases to be bigger than the relative first hole spacing (~ 50 mV), see Table 4.1. We present these measurements starting from an empty dot and finishing in the original configuration, with a square labelling the (0,0) point in the map signalling the odd occupancy regime. In analogy to the main text, the red, blue, green and yellow frames of the plots indicate that the data have been measured with the NW, NE, SW and SE charge sensor, respectively.

In Table 4.2, we list the dc virtual plunger voltages of the datasets presented as Supplementary Videos.

Video	vP1	vP2	vP3	vP4	vP5	vP6	vP7
1	-1369	-1354	-1527	-2056	-1995	-1612	-1380
2	-1369	-1354	-1527	-2056	-1995	-1612	-1380
3	-1363	-1354	-1527	-2056	-1995	-1612	-1380
4	-1363	-1354	-1527	-2056	-1995	-1612	-1380
5	-1363	-1354	-1527	-2056	-1995	-1612	-1380
6	-1363	-1354	-1527	-2056	-1995	-1612	-1380
7	-1363	-1354	-1527	-2056	-1995	-1612	-1380
8	-1363	-1354	-1527	-2056	-1995	-1612	-1380
9	-1363	-1354	-1527	-2056	-1995	-1612	-1380
10	-1369	-1354	-1527	-2056	-1995	-1612	-1379
11	-1369	-1354	-1527	-2056	-1995	-1612	-1380
12	-1369	-1354	-1527	-2056	-1995	-1612	-1378

Table 4.2: **Virtual plunger voltages.** Table listing all the dc voltages applied to the virtual plunger gates underlying the measurements presented in the Videos 1-12. All values are in mV. The largest variation (6 mV) on vP1 does not affect the occupancy of Q1 (neither the surrounding Q2b and Q2t quantum dots), as can be seen in Videos 1 and 2.

4

4.12. IMAGE CORRELATION TECHNIQUES FOR QUANTUM DOT DETECTION

Verifying the odd charge state requires tracking the charge addition lines of all 16 quantum dots. This can be a tedious task as the Supplementary videos in the previous subsection demonstrate because it involves studying several charge stability maps at different plunger gate configurations with varying visibility. Some charge transition lines only can be reconstructed by their interdot transitions with other dots, and slow tunnel couplings to the reservoirs (Fig. 4.18) cause postponed loading (i.e. latching) which further complicates the interpretation [30]–[33]. Therefore, we have developed an algorithm that unifies and simplifies the assessment of the first few charge transition lines of a given quantum dot to ease the determination of its charge occupation.

In order to track the transitions of a given quantum dot Qx, we acquire charge stability maps M_n^{raw} sweeping the respective plunger gate vPx against a neighbouring plunger gate vPy for N_{scan} constantly spaced offset voltages $V_{\text{off},n}$ applied to vPx or a third gate (as presented in the Supplementary Videos). The charge stability maps are preprocessed by applying an individual combination of background subtraction, derivatives, local contrast normalisation, cropping along the secondary axis (vPy) and normalisation as detailed in Table 4.4. A reference feature F is then defined as a renormalised section of one of the preprocessed charge stability maps M_n. It is chosen to uniquely identify the respective quantum dot transition line, either directly containing a section of a transition line or showing an interdot transition with an adjacent dot.

Next, we calculate the image correlation C_n of the charge stability maps M_n with the reference feature F:

$$C_n(\text{vP}x, \text{vP}y) = \sum_{\Delta\text{vP}x, \Delta\text{vP}y} M_n(\text{vP}x + \Delta\text{vP}x, \text{vP}y + \Delta\text{vP}y) F(\Delta\text{vP}x, \Delta\text{vP}y)$$

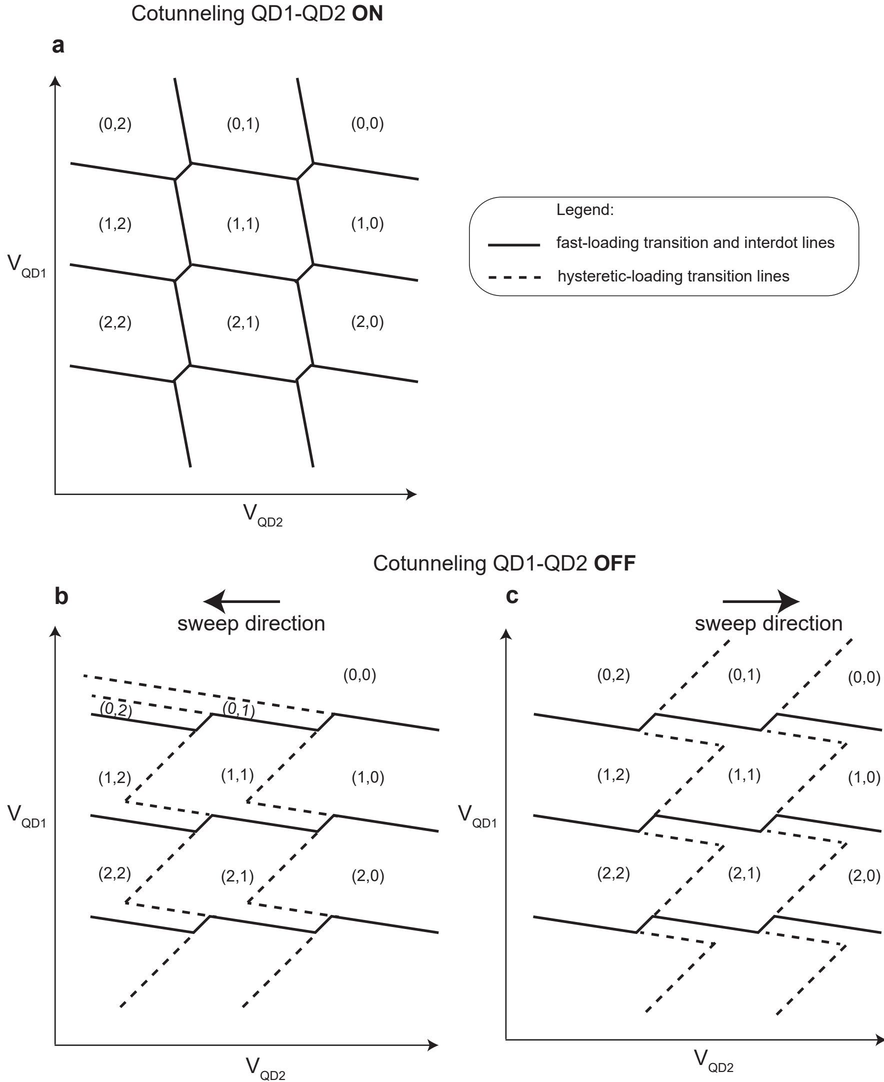

Figure 4.18: **Effects of low tunnel rate to the reservoir in charge stability diagrams. a,** Cartoon of a conventional honeycomb charge stability diagram of a double dot system where the reservoir tunnel rates to both dots Q1 and Q2 are much higher than the sweep rate of both axes. If one dot (Q2) is located further away from the reservoir than the other (Q1), loading in Q2 occurs thanks to cotunnelling events via Q1. **b, c** When Q2 is coupled to the reservoir at a rate much slower than the sweeping time, the charge stability map displays hysteretic features whose occurrences depend on the sweep direction [30]. Q2 is then loaded via the extended charge interdots of Q1-Q2, which remains active due to the finite Q1-Q2 interdot coupling. We note that when the charge stability diagrams display such features, the interdots with Q1 still enables to reconstruct the Q2 transition line at equilibrium. We also emphasise that typical maps manifest a behaviour that is in between the case displayed in **(a)** and in **(b)** (or **(c)**) depending on the sweep direction and the tunnel rate to the leads, which is typically non zero.

Typically C_n will exhibit a maximum at the gate voltages for which F was defined. However, often F also has an increased correlation with similar features of higher or lower transition lines enabling the detection of those as well. We note that in some cases we redefine the feature F to compensate for sensor shifts or features changing with the charge occupancy of the dot (e.g. growing interdot transitions). The number of feature definitions per number of charge stability diagrams is given in the last column of Table 4.4. Each correlation map C_n is then divided into sub-parts $C_{n,m}$ along the vPx axis and the maximum correlations $\hat{C}_{n,m} = \max(C_{n,m})$ and the respective coordinates $(\mathrm{v\hat{P}}x_{n,m}, \mathrm{v\hat{P}}y_{n,m})$ are determined. In particular we choose four sub-parts ($m \in \{0,1,2,3\}$) for all quantum dots corresponding to a spacing similar to typical charging voltages and thus increasing the probability of only a single transition line crossing each sub-part. To minimise the number of falsely positive detections which are not related to actual occurrences of transition lines we furthermore apply a threshold keeping only $(\mathrm{v\hat{P}}x_{n,m}, \mathrm{v\hat{P}}y_{n,m})$ with $\hat{C}_{n,m} \geq 0.35 \times \max_{m,n}(\hat{C}_{n,m})$. In Fig. 4.4 and 4.5 in the main text we plot the remaining $(\mathrm{v\hat{P}}x_{n,m}, \mathrm{v\hat{P}}y_{n,m})$ as a function of n with $\hat{C}_{n,m}$ encoded in the individual colouring of the scatter points.

The correlation maxima $\hat{C}_{n,m}$ corresponding to a specific charge transition $i \rightarrow j$ are expected to shift from charge map to charge map by a regular voltage shift $\frac{\Delta \mathrm{v\hat{P}}x_n}{\Delta n}$, thus falling on a line $\mathrm{v\hat{P}}x^{i\rightarrow j}$ given by:

$$\mathrm{v\hat{P}}x^{i\rightarrow j}(n) = \frac{\Delta \mathrm{v\hat{P}}x_n}{\Delta n} \times n + \mathrm{v\hat{P}}x_0^{i\rightarrow j}$$

Note that we dropped the m subscripts as with increasing n the transition line can shift from one sub-part to another. We utilise this predictable behaviour to increase robustness against occasionally missed features and further reduce the effect of falsely obtained correlation maxima which do not correspond to a a charge transition and thus typically shift randomly from charge map to charge map. To that end we define a dense set of potential transition lines

$$\mathrm{v\hat{P}}x^{B}(n) = \frac{\Delta \mathrm{v\hat{P}}x_n}{\Delta n} \times n + B$$

with B stepped in steps of 4 mV from $B_{\mathrm{min}} \ll \min(\mathrm{vP}x)$ to $B_{\mathrm{max}} \gg \max(\mathrm{vP}x)$. The chosen $\frac{\Delta \mathrm{v\hat{P}}x_n}{\Delta n}$ are given in Table 4.3. Most values are close to 10 mV as for most quantum dots we step the vPx gate offset with each charge stability map by 10 mV. Small deviations from 10 mV arise due to imperfect calibrations of the AWG voltages with respect to the Digital to Analog Converted (DAC) voltages. For each B we then identify all the scatter points $(\mathrm{v\hat{P}}x_{n,m}, \mathrm{v\hat{P}}y_{n,m})$ that are located in a range of ± 4 mV around $\mathrm{v\hat{P}}x^{B}(n)$. These then allow for all lines $\mathrm{v\hat{P}}x^{B}(n)$ to determine a heuristic measure of likelihood to be an actual transition line. We calculate this likelihood $p(B)$ using the following equation, that keeps into account the number of points N_B falling in that range, their correlation $\hat{C}_{n,m}$ and the

maximum number of feature occurrences that could have been detected $N_B^{\max}$:

$$p(B) = \frac{1}{N_B^{\max}} \left[-L \times (N_B^{\max} - N_B) + \sum_{\substack{\hat{C}_{n,m} \text{ if} \\ \text{v}\hat{\text{P}}x^B(n) - 4\text{ mV} \\ \leq \text{v}\hat{\text{P}}x_{n,m} \leq \\ \text{v}\hat{\text{P}}x^B(n) + 4\text{ mV}}} \max_m (\hat{C}_{n,m}) \right]$$

Here $L = 0.3 \times \max_{m,n}(C_{n,m})$ defines a penalty term lowering $p(B)$ for every potential feature occurrence that has not led to a detected correlation maximum. Fig. 4.5 in the main text shows the set of lines $\text{v}\hat{\text{P}}x^B(n)$ with $p(B)$ colour-coded in the colour of each trace. A few lines clearly emerge from the others, identifying the charge transitions of the various quantum dots. The white square with black outline marks the final voltage setpoint, which is clearly located between two dense clusters of high-$p(B)$ lines. In Fig. 4.19, we combine the results of the method applied for all quantum dots, by showing a line-cut of $p(B)$ on the rightmost part of the panels ($n = N_{\text{scan}}$) presented in main text Fig. 4.5. Charge transitions are visible as peaks, and are fitted with a Gaussian function to extract their position. From this analysis, we obtain a ~ 7 mV virtual plunger voltage range for the odd charge regime presented here. We emphasise that gate voltages have not been optimised to centre the charge symmetry points of the quantum dots at the tuning point, but this may be required for qubit operation.

The detection precision of the resulting transition voltages for each dot depends on the specific underlying set of charge stability diagrams. For transition lines perfectly aligned with the vPy-axis the potential variation of the vPx-coordinate is minimised. However, in practice residual cross capacitances not compensated by the virtual gates remain leading to sloped transition lines. As a given feature often can reappear multiple times on the same transition line at differing vPy voltages this then results in a scattering of the vPx-coordinates around the expected behaviour. Also, latching effects depending on the scan ranges of vPx and vPy can cause those variations. However, careful feature definitions and reduced vPy scan ranges lower this impreciseness. Furthermore, we also correct for constant offsets between the feature positions and the charge transition line voltages.

While here our method is utilised to unify and ease the tedious task of tracking the full spectrum of charge transitions for all dots which still requires careful prepossessing and a manual selection of features we envision that in future work it could become part of automatic tuning and verification procedures.

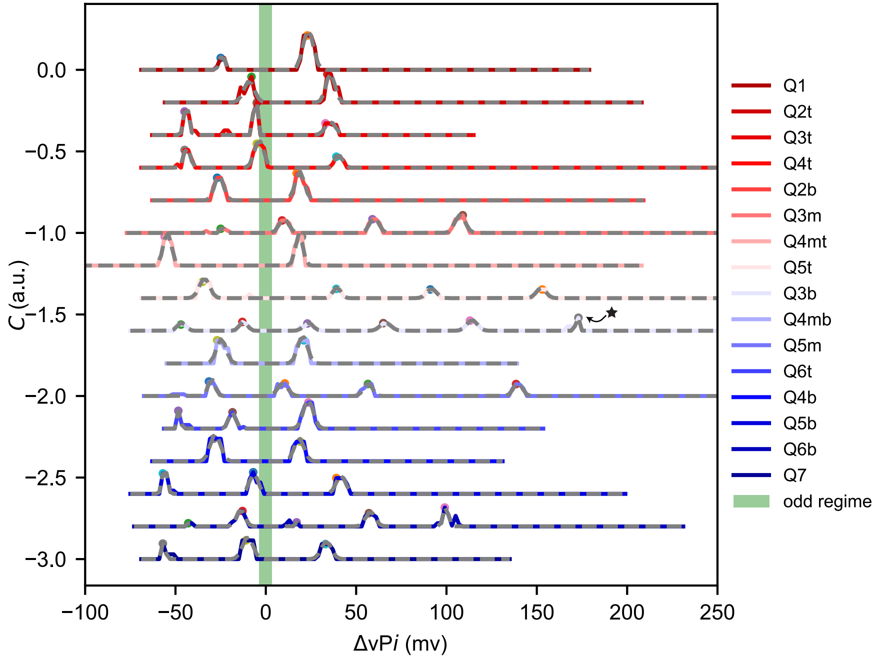

Figure 4.19: **Charge transition lines of all the quantum dots in the odd charge occupancy regime** We plot the likelihood quantity $p(B)$ for all the quantum dots taken at the position of the white square marker in the panels of main text Fig. 4.5 (i.e., at the max $n = N_{\text{scan}}$) and thus for the offset voltage configuration of the odd charge state. Charge transition lines identified via image detection methods appear as peaks. We fit the sequence of peaks with Gaussian functions to extract their position in the voltage space. The star on the first peak of the quantum dot Q3b indicates a false-positive transition line, as discussed in the main text. The green rectangle identifies the span in voltage of all the virtual plungers in which the odd occupancy is conserved. The broadening of the peaks is mainly due to the jitter in high-correlation points $(\text{v}\hat{\text{P}}x_{n,m}, \text{v}\hat{\text{P}}y_{n,m})$ as visible in main text Fig. 4.5. We note that the lines cover the range set by the algorithm, which is larger than the range spanned by the data.

Stepped gate	$\frac{\Delta \mathrm{v}\hat{\mathrm{P}}\boldsymbol{x}_n}{\Delta n}$ **(mV/scan)**
vP1	10.75
vP2	10.0
vP3	10.0
vP4	9.0
vP5	12.0
vP6	8.7
vP7	10.0
vUB3	7.5
vUB6	6.0
vUB7	5.4

Table 4.3: Slope coefficient $\frac{\Delta \mathrm{v}\hat{\mathrm{P}}x_n}{\Delta n}$ of the transition lines in the panels of the main text Fig. 4.5.

Quantum dot	background subtraction	derivative	LCN	cropping in vPy direction	number of features per charge maps
Q1	no	$\frac{dM_n}{dvPx}+\frac{dM_n}{dvPy}$	yes	yes	1/6
Q2t	no	$\frac{dM_n}{dvPx}$	no	yes	1/8
Q2b	no	$\frac{dM_n}{dvPx}$	no	yes	1/8
Q3t	no	$\frac{dM_n}{dvPy}$	yes	yes	2/8
Q3m	yes	no	no	yes	1/12
Q3b	no	$\frac{dM_n}{dvPx}$	no	no	1/12
Q4t	no	$\frac{dM_n}{dvPx}$	yes	yes	1/12
Q4mt	yes	no	no	yes	1/12
Q4mb	no	$\frac{dM_n}{dvPx}$	no	yes	1/4
Q4b	no	$\frac{dM_n}{dvPx}$	no	yes	1/4
Q5t	no	$\frac{dM_n}{dvPx}$	yes	yes	2/16
Q5m	no	$\frac{dM_n}{dvPx}$	no	yes	2/16
Q5b	no	$\frac{dM_n}{dvPx}$	yes	yes	3/6
Q6t	no	$\frac{dM_n}{dvPx}$	no	no	1/8
Q6b	no	$\frac{dM_n}{dvPx}$	yes	yes	2/12
Q7	no	$\frac{dM_n}{dvPx}$	no	no	1/4

Table 4.4: Preprocessing applied to the raw charge stability maps M_n^{raw} to obtain M_n and number of defined charge transition features. Here, background subtraction refers to subtracting a smoothed version of the charge stability map: $M_n^{\text{out}} = M_n^{\text{in}} - M_n^{\text{in}} * f_{\text{Gaussian}}$. Local contrast normalisation corresponds to $M_n^{\text{out}} = \frac{M_n^{\text{in}} - M_n^{\text{in}} * f_{\text{Gaussian}}}{\sqrt{(M_n^{\text{in}} - M_n^{\text{in}} * f_{\text{Gaussian}})^2 * f_{\text{Gaussian}}}}$. In both cases M_n^{in} and M_n^{out} refer to the charge stability diagram before and after the respective processing and f_{Gaussian} is a Gaussian distribution with a standard deviation of 7-10 pixels and 4-10 pixels respectively. The postprocessing steps are applied in the order as presented in the table (from left to right). In all cases the final charge stability map M_n is normalised such that $0 \leq M_n(\text{vP}x, \text{vP}y) \leq 1$. The last column provides the number of defined transition features F and the total number of charge stability maps M_n (N_{scan}).

4.13. ADDRESSABLE EXCHANGE OPERATIONS WITH A DOUBLE BARRIER DESIGN

The ability to control the tunnel coupling with two barriers opens the opportunity to design addressable exchange-based two-qubit gates in architectures with shared control. We envision an operation strategy in which a two-qubit gate can be activated only when both barriers are in the ON state. For a fast CPHASE gate with a duration of 5 ns, we require to activate an exchange interaction of J_{ON}/h = 100 MHz. In all other cases (i.e., when the barriers are in the configurations (ON, OFF), (OFF, ON), (OFF, OFF)), we demand a sufficiently low exchange to minimise errors. State-of-the-art values of OFF exchange interaction are in the order of $J_{OFF}/h \sim$ 10 KHz [40].

Fig. 4.20 illustrates the required barrier voltage points to obtain such exchange interactions considering symmetric lever arms, a quantum dot charging energy of U = 1 meV and operations at the charge symmetry point (i.e., at zero detuning). In Fig. 4.20, we have approximated the dependence of the tunnel coupling energy t_C with respect to the two barrier voltages B_x and B_y with [9], [21], [53]:

$$t_C = \frac{\sqrt{JU}}{2} = c_1 \cdot e^{-c_2\alpha(B_x - B_{x,ON})} \cdot e^{-c_2\alpha(B_y - B_{y,ON})} \tag{4.4}$$

with $B_{x,ON}$ and $B_{y,ON}$ the ON set-points of the two barriers.
In this example, we have set the prefactor c_1 to 5·h GHz with h the Plank constant, and the effective barrier lever arms $c_2 \cdot \alpha$ to 0.04 V^{-1}.

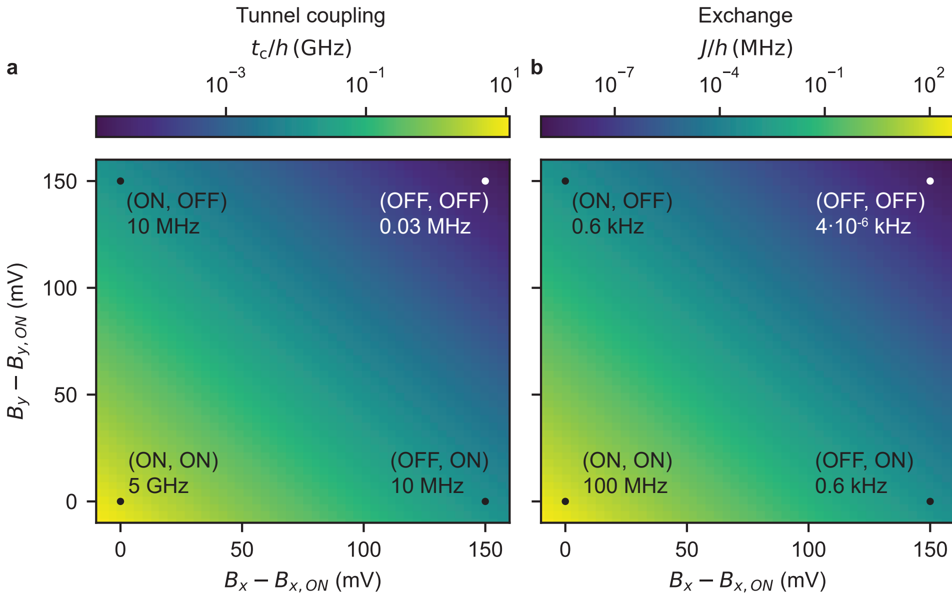

Figure 4.20: **Addressable exchange operation with a double barrier design. a, b** Target tunnel coupling and exchange required for fast two-qubit gates with interaction ON (bottom left corner), and OFF (top left, top right, bottom left corners in the map). The exchange interaction of qubit pairs at (ON, OFF) crossing points remains four orders of magnitude smaller than in the (ON, ON) cases. The parameters displayed are calculated at the coordinates (0, 0), (0, 150), (150, 0), (150, 150) mV. In reference to the experimental results of Fig. 4.6 and 4.7, the measurable tunnel coupling range (> 1 GHz) via polarisation lines is the bottom left corner of panel **(a)** extending up to +24 mV on both axes.

4.14. TWO-AXIS CONTROL OF THE INTERDOT TRANSITION LINE

By fitting the two-dimensional (e67, U67) charge stability maps (examples in Figs. 4.21a, b), we obtain an estimate of the (3,1)-(2,2) charge interdot size L for the double dot systems Q6b-Q7 and Q6t-Q7. The size of the interdot line is indicative of the capacitive coupling between the adjacent quantum dots. Consistent with the two-axis tunability of the tunnel coupling, the interdot size is varied as the effective distance between the dots is modified by the action of the two tunnel barriers (Figs. 4.21c-f).

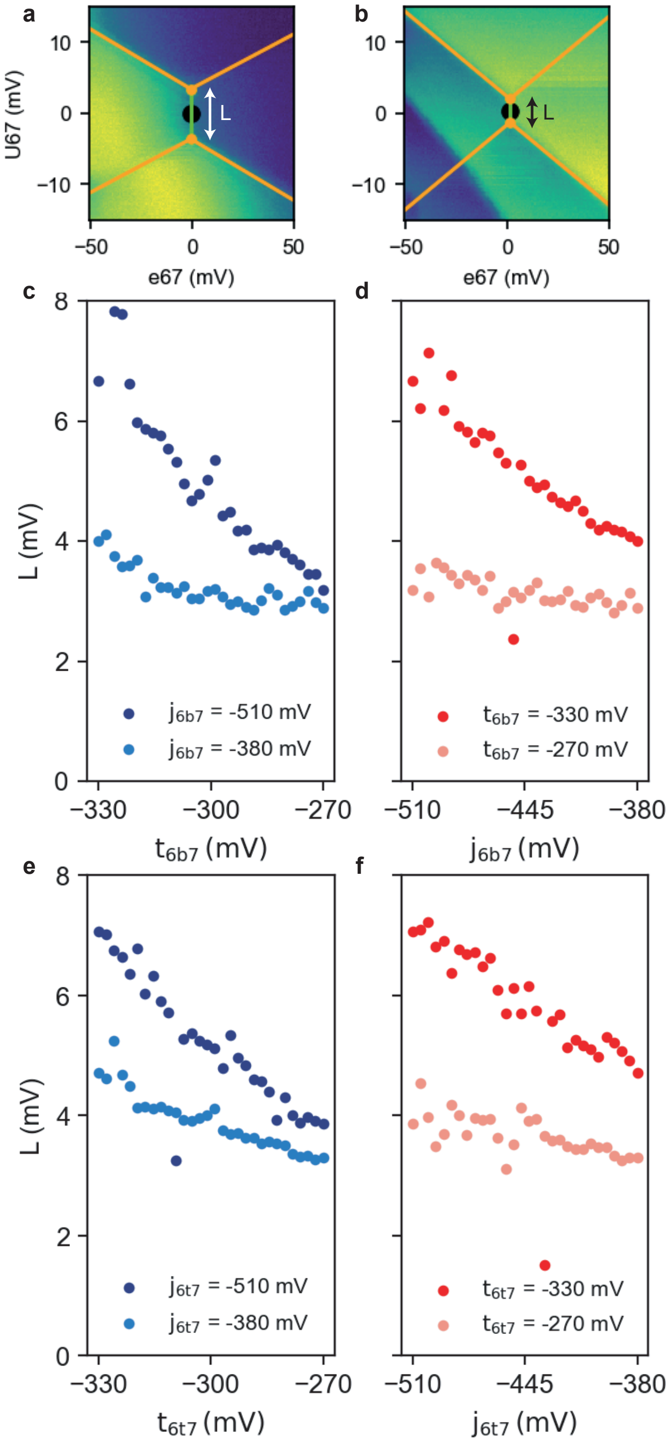

Figure 4.21: **Two-axis control of the quantum dot interdot transition line.** **a, b,** Exemplary charge stability diagrams taken at the Q6t-Q7 (3,1)-(2,2) charge interdot line. The two maps are taken at the diagonally opposite points of the two-dimensional barrier scan, at t_{6t7}, j_{6t7} = (-330, -510) and (-270, -380) mV, respectively. Orange lines represent a fit to the map following the procedure shown in ref. [45]. A black circle identifies the fitted centre of the interdot, and the arrow illustrates the size in voltage of the interdot line. **c, d,** Size of the Q6b-Q7 (3,1)-(2,2) charge interdot line as a function of the two virtual barriers. **e, f,** Same for the Q6t-Q7 (3,1)-(2,2) charge interdot line. Outliers in the plot are due to non-accurate fits of the image.

4

4.15. TWO-AXIS CONTROL OF THE Q6B-Q5M INTERACTION

We repeat the tunnel coupling experiments considering the double-dot pair Q6b and Q5m by defining the virtual barriers t_{6b5} and j_{6b5} starting from the relative UB4 and LB6 barriers (Fig. 4.22):

$$\begin{pmatrix} \mathrm{P5} \\ \mathrm{P6} \\ \mathrm{UB4} \\ \mathrm{LB6} \\ \mathrm{SE_P} \end{pmatrix} = \begin{pmatrix} -1.63 & -0.58 \\ -1.61 & -0.48 \\ 1 & 0 \\ 0 & 1 \\ -0.43 & -0.02 \end{pmatrix} \begin{pmatrix} \mathrm{t}_{6b5} \\ \mathrm{j}_{6b5} \end{pmatrix}$$

We observe that the limited sensitivity at the interdot hinders a quantitative tunnel coupling analysis. However, at a qualitative level, we still observe the expected pattern with the size of the interdot tunable by both barriers.

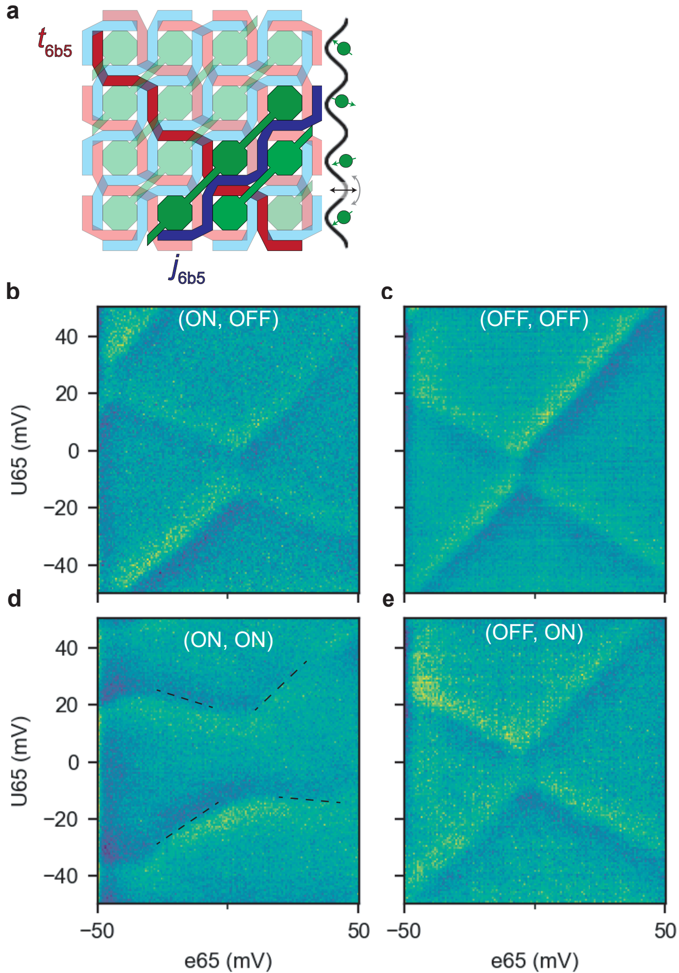

Figure 4.22: **Two-axis control of the Q6b-Q5m interdot coupling. a** Schematic of the crossbar indicating the two intersecting virtual barriers (in red and blue) controlling the Q6b-Q5m interaction. **b-e** Charge stability diagrams at different barrier voltages: **(b)** (t_{6b5}, j_{6b5}) = (-330, -380) mV, **(c)** (-270, -380) mV, **(d)** (-270, -510) mV, **(e)** (-330, -510) mV. In **(d)**, in the high interdot coupling regime, we add dashed lines as guide for the eyes on weakly visible transition lines. Here, we display the signal from the SE charge sensor after subtraction of a background.

4.16. ELECTRON TEMPERATURE EXTRACTION

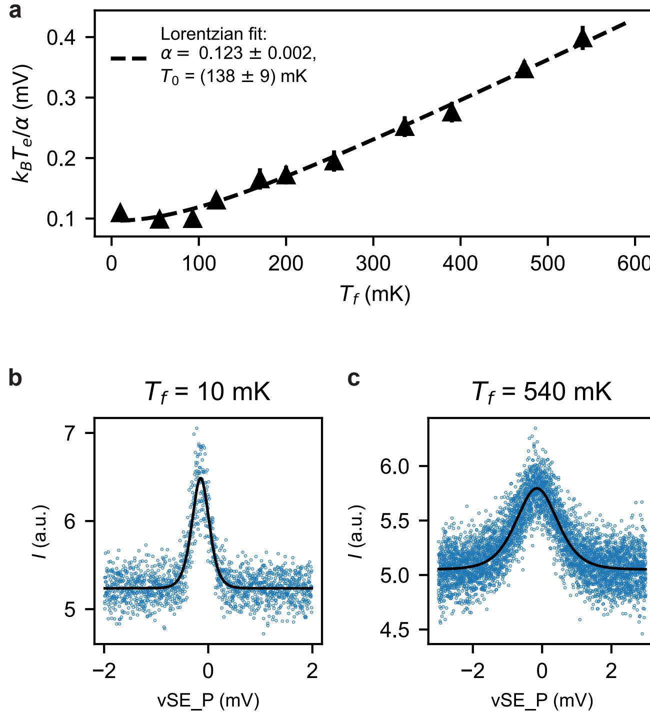

Figure 4.23: **Electron temperature extraction. a** Coulomb peak width as a function of fridge temperature. **b, c.** Exemplary data (scatter points) and best fits (black lines) collected at T_f = 10 mK and T_f = 540 mK, respectively. For every temperature, we perform five plunger sweeps across the Coulomb peak (each averaged 500 times) and, by fitting the curves, we obtain five different estimates for the Coulomb peak width. In **(a)**, we show the average width. The depicted standard deviation is determined by considering the standard deviation from the single fit itself or the standard deviation between the five different fitting estimates, depending on which is dominant.

We estimate the electron temperature of our setup by fitting a temperature broadened Coulomb peak of the SE charge sensor. We choose a source-drain voltage V_{SD} and coupling energy to the leads $h\Gamma$ such that $h\Gamma, eV_{SD} << k_B T_e$, with h and k_B the Plank and Boltzmann constants, respectively and Γ the lead-dot tunnel rate. The current I at the Coulomb peak is fitted with the Lorentzian distribution

$$I_{model} = a \cdot \cosh^{-2}\left(\frac{\alpha_{sensor} \cdot \epsilon}{2 k_B T_e}\right) + c, \tag{4.5}$$

where a is an amplitude prefactor, α_{sensor} is the lever arm of the sensor plunger gate, ϵ is the plunger gate voltage and c an offset. The full width half maximum (FWHM) of the peak is therefore given by

$$\text{FWHM} = \frac{k_B T_e}{\alpha_{sensor}} = \frac{k_B \sqrt{T_0^2 + T_f^2}}{\alpha_{sensor}}, \tag{4.6}$$

where T_f is the nominal fridge temperature and T_0 the base electron temperature [54]. We use the FWHM dependence on the nominal fridge temperature to extract both T_0 and α_{sensor}. The result can be seen in Fig. 4.23 with two exemplary fits for 10 and 540 mK. The fit with Equation 4.6 results in $T_0 = 138 \pm 9$ mK and $\alpha_{sensor} = 0.123 \pm 0.002$ eV/V, which is consistent with an independent lever arm extraction from Coulomb diamonds.

4.17. DETUNING LEVER ARM EXTRACTION

For an accurate estimation of the interdot tunnel coupling, we evaluate the quantum dot detuning lever arm by fitting the sensor signal S_{21} with a thermally limited polarisation line (Fig. 4.24) as described in [38]:

$$S_{model} = S_0 \pm \delta S \frac{\epsilon}{\Omega} \cdot \tanh\left(\frac{\Omega}{2k_B T_e}\right) + \frac{\partial S}{\partial \epsilon}\epsilon \tag{4.7}$$

with S_0 the background signal of the charge sensor, δS the signal amplitude, ϵ the detuning energy, Ω the energy difference between the two levels and the term $\frac{\partial S}{\partial \epsilon}\epsilon$ a linear slope due to cross-talk to the charge sensor. In the low-tunnelling regime, we can approximate $\Omega = \sqrt{\epsilon^2 + 4t^2} \approx \epsilon$, which reduces Equation 4.7 to

$$S_{\text{model}} = S_0 \pm \delta S \cdot \tanh\left(\frac{\alpha_{QD} \cdot \epsilon}{2k_B T_e}\right) + \frac{\partial S}{\partial \epsilon}\epsilon. \tag{4.8}$$

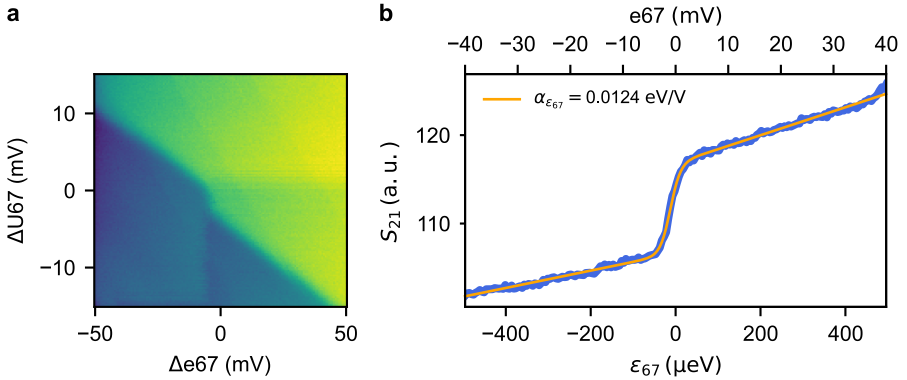

Figure 4.24: **Temperature limited polarisation line. a,** Charge stability diagram of the uncoupled Q6b-Q7 at the (3,1)-(2,2) charge interdot. In this configuration, the tunnel time in Q6b is small with respect to the ramp time of the detuning axis, therefore the interdot is extended and the Q6b addition line is not clearly visible in the map. **b,** Thermally limited polarisation line (blue trace) taken at the centre of the interdot shown in **(a)**. From the best fit (orange line), we obtain the detuning lever arm $\alpha_{\epsilon_{67}} = 0.012(4)$ eV/V.

4.18. TUNE-UP OF THE CROSSBAR ARRAY IN THE FEW-HOLE REGIME

In Fig. 4.25, we display the charge stability diagrams obtained for the first tune-up of the device with the quantum dots in the few-holes regime. These maps are part of the data sets that are used for the analysis presented in Fig. 4.12-4.16. The applied voltages at this phase of the experiment are shown in Fig. 4.26.

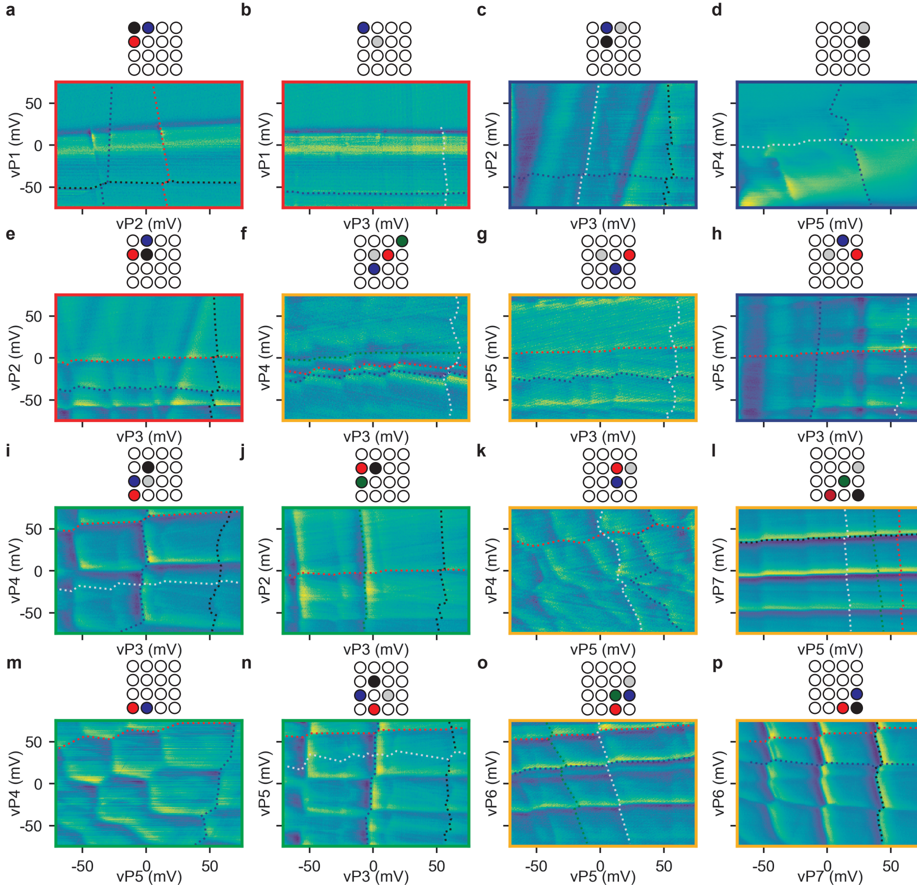

Figure 4.25: **Tune-up of the crossbar array in the few-holes regime. a-p,** Charge stability diagrams (raw sensor signal after subtraction of a background) showcasing the 16 quantum dot system in the few-hole regime. These measurements are taken in the first tune-up of the crossbar array. In each map, the first visible transition lines from the right or the top are labelled and assigned to the relative quantum dot by dashed lines with colours defined in the schematic at the top. The identification is performed via the results of Fig. 4.12-4.16. The colour of the panel frame identifies the sensor used: NW in red, NE in blue, SW in green, and SE in ochre.

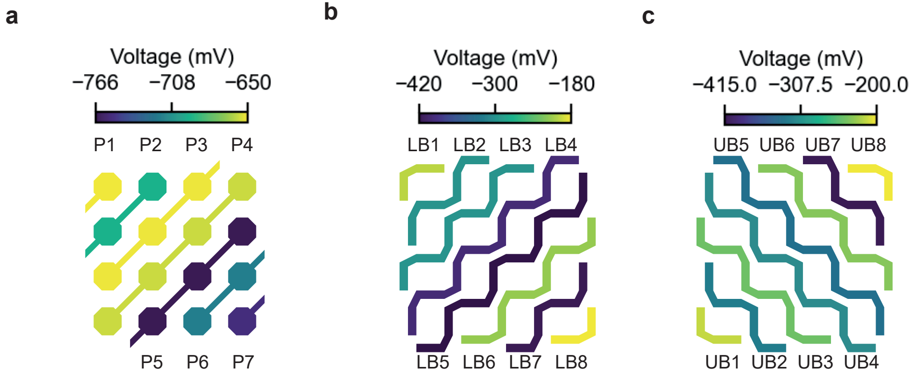

Figure 4.26: **Tune-up of the crossbar array in the few-holes regime. a-c,** Schematics of the voltage applied at all crossbar gates at the phase of the experiment shown in Fig. 4.25. The voltages are here optimised to circumvent stray dots.

4.19. GATE VOLTAGES OF THE CROSSBAR IN THE ODD-CHARGE REGIME

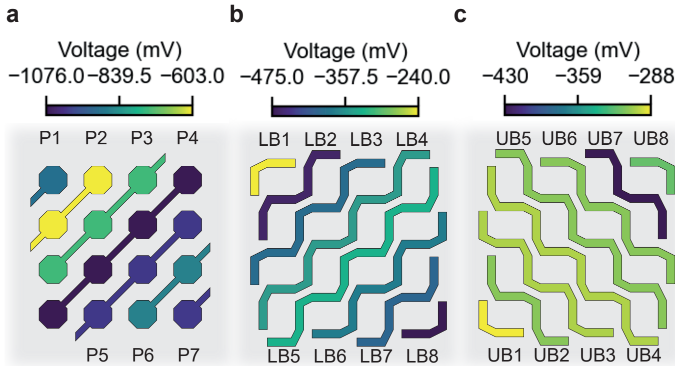

Figure 4.27: **Crossbar gate voltages. a-c,** Voltages applied at the real P, LB and UB gates, respectively, when the system is tuned in the odd charge occupation regime.

4.20. CHARACTERISATION OF THE VARIABILITY OF THE QUANTUM DOT ARRAY

We have characterised the level of homogeneity in the array considering two different metrics.

First, we consider the onset voltage of the first hole in each quantum dot, as displayed in Figs. 4.28a, b. We obtain an average first-hole voltage of -1660 ± 290 mV, that indicates a rather high variability across the quantum dot array. We also observe that a more negative voltage is required to accumulate the first hole when going toward the center of the

array (e.g. under P4 and P5). This trend is anticorrelated with the voltages set to the LB barrier gates, that run in parallel to the plunger gates (Fig, 4.28c). The higher values of LB4 and LB5 lead to more negative values of the plunger gates within the array, due to cross capacitance. We note that the need to set LB4 and LB5 to a more positive voltage comes from the demand to maintain the charge sensors well separated by the array. In practice, we have observed that the needs to preserve the quality of the charge sensors and to set the interdot tunnel barriers seem conflicting. Therefore, we suggest in future designs to dedicate to one gate the function to isolate the sensor to the dots and to another gate to determine the interdot barriers.

A second metric to asses the variability in size and in dot lever arm relies on evaluating the homogeneity in quantum dot addition voltages, i.e. the spacing between two consecutive charge transition lines [44]. We extract the charge addition voltages of all the quantum dots from the corresponding stability diagrams (Fig. 4.29), and extract the averaged spacing of the first and second hole to be 51 ± 6 mV and 50 ± 9, respectively, indicating a $\sim 10-20\%$ variability of the quantum dot confinement properties across the array.

Overall, this demonstrates that, while quantum dots are accumulated at rather different voltages under each plunger gate, their size and plunger gate coupling are similar, owing to the grid structure of our design.

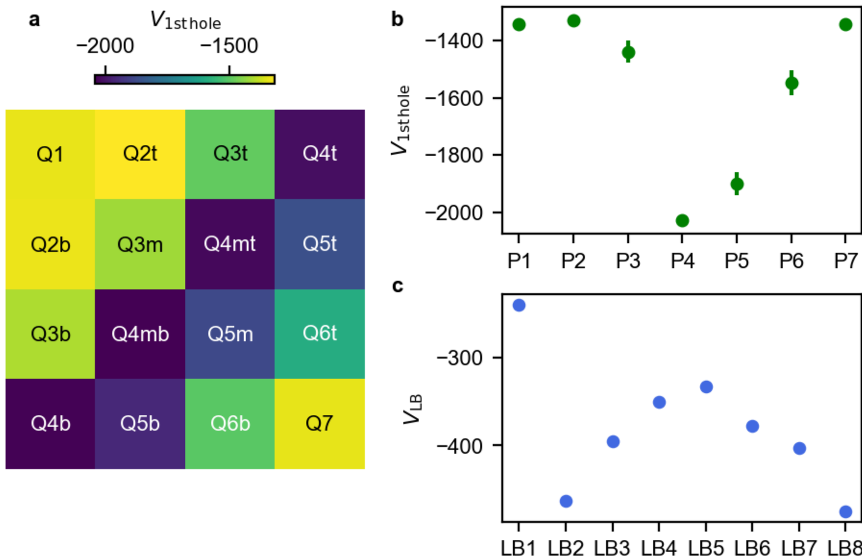

Figure 4.28: **Onset voltages for the first hole. a,** Colormap of the virtual plunger voltages required to accumulate the first hole in each quantum dot. **b,** Averages first hole virtual plunger voltages. The error bars represent the standard deviations around the mean. We note that, while the variability of dot voltages for the same plunger is rather low, the overall variability of 290 mV remains high. **c,** Voltages of the LB gates in the odd charge regime.

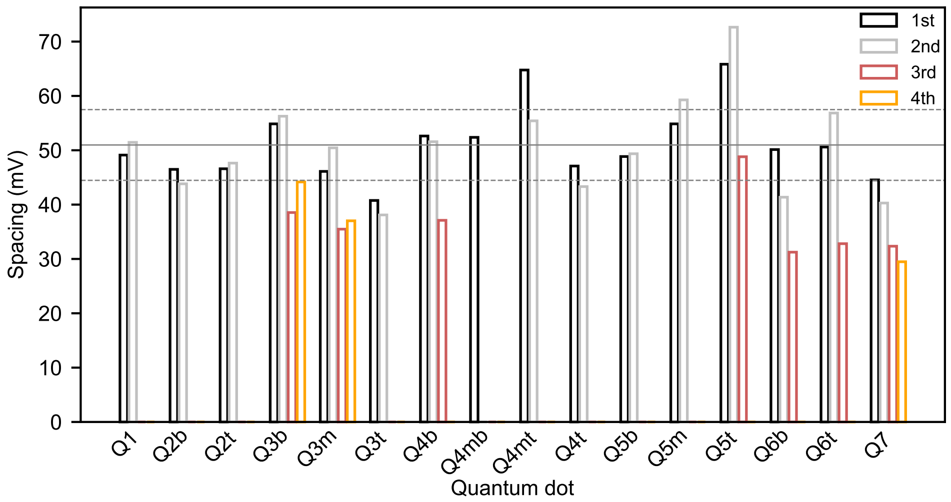

Figure 4.29: **Charge Addition voltages of all the quantum dots.** Bar plot of the addition voltages of each quantum dot considering the first spacings, when detectable in the already existing datasets. The three horizontal lines identify the spread of the first hole addition voltage of 51 ± 6 mV.

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4

5

Electrical control of uniformity in quantum dot devices

Highly uniform quantum systems are essential for the practical implementation of scalable quantum processors. While quantum dot spin qubits based on semiconductor technology are a promising platform for large-scale quantum computing, their small size makes them particularly sensitive to their local environment. In this chapter, we present a method to electrically obtain a high degree of uniformity in the intrinsic potential landscape using hysteretic shifts of the gate voltage characteristics. We demonstrate the tuning of pinch-off voltages in quantum dot devices over hundreds of millivolts that then remain stable at least for hours. Applying our method, we homogenize the pinch-off voltages of the plunger gates in a linear array for four quantum dots reducing the spread in pinch-off voltage by one order of magnitude. This work provides a new tool for the tuning of quantum dot devices and offers new perspectives for the implementation of scalable spin qubit arrays.

This chapter has been published as M. Meyer, C. Déprez, T. R. van Abswoude, I. N. Meijer, D. Liu, C. Wang, S. Karwal, S. Oosterhout, F. Borsoi, A. Sammak, N. W. Hendrickx, G. Scappucci, and M. Veldhorst, Electrical control of uniformity in quantum dot devices, *Nano Letters* **2023** 23 (7), 2522-2529 [1].

5.1. INTRODUCTION

Spin qubits in semiconductor quantum dots are a promising platform for quantum information processing [2]–[5]. Group IV semiconductors such as silicon and germanium can be isotopically purified [6], enabling long quantum coherence [7], [8], high-fidelity single-qubit [9]–[11] and two-qubit gates [12]–[14] as well as multi-qubit operation [15], [16]. Spin qubits can be operated at comparatively high temperatures [17]–[19] and their compatibility with semiconductor technologies spurred the realization of qubits made in industrial foundries [20], [21]. However, implementing more than a few qubits on a single chip remains extremely challenging.

Variations, in particular at the nanoscale, may lead to significant alterations of the relevant device metrics [2], [3], [22], such as the voltage needed to load a single electron to be used as a spin qubit. These variations can complicate the tuning of initialization, control or readout and potentially form a roadblock for larger systems. Additionally, qubit-to-qubit variability may require the use of individual control electronics for each qubit, as is common practice in current experimental implementations, thus challenging the scalability. While several proposals have been put forward to scale quantum dot qubits [3], [23]–[25], in all cases a high level of device uniformity is critical in their realization.

For semiconductor quantum dot qubits, the uniformity of the potential landscape is the key parameter that dictates the number of control voltages required per qubit. Ideally, a few voltages would suffice to induce a highly regular potential landscape as drawn in Fig. 5.1.c. Yet, potential fluctuations are naturally present as illustrated in Fig. 5.1.d. They can be caused by defects and charge traps, mechanical stress induced by the deposition of metallic gates [26], [27], as well as variations in material growth or in the exact shape of the gates. The development of devices based on quantum wells buried in heterostructures, similar to that sketched in Fig. 5.1.a, already has led to a drastic improvement of the uniformity compared to metal-oxide-semiconductor systems [28]. This has enabled the control of up to 16 quantum dots in a four-by-four array with shared gate control (see chapter 4). However, significant variations in the quantum dot potential landscape are still commonly observed [29], [30] (also see Fig. 2.4). This raises the question whether material [5] and fabrication development [21], [31], [32] will suffice to reach the required uniformity to operate large qubit arrays.

In this chapter, we present an alternative method and demonstrate electrical control of quantum dot uniformity. Our approach takes advantage of the gate voltage hysteresis, an ubiquitous effect observed in semiconductor heterostructures, that is mostly considered as a limitation in the tune-up of quantum dots. It manifests in shifts of the gate voltage characteristics and is commonly explained by a build-up of charges at the interface between the semiconductor barrier and the dielectrics which then alter the electric field in the buried quantum well [33]–[39]. We unveil the hysteresis and its effects on the potential landscape beneath the gates by studying how pinch-off characteristics evolve with the application of tailored stress voltage sequences. This method allows us to tune those pinch-off voltages over hundreds of millivolts after which they remain stable at least on the time scale of hours. We then apply our findings to homogeneize the plunger gate pinch-off characteristics in a linear quantum dot array reducing potential fluctuations in the quantum well underneath the corresponding gates.

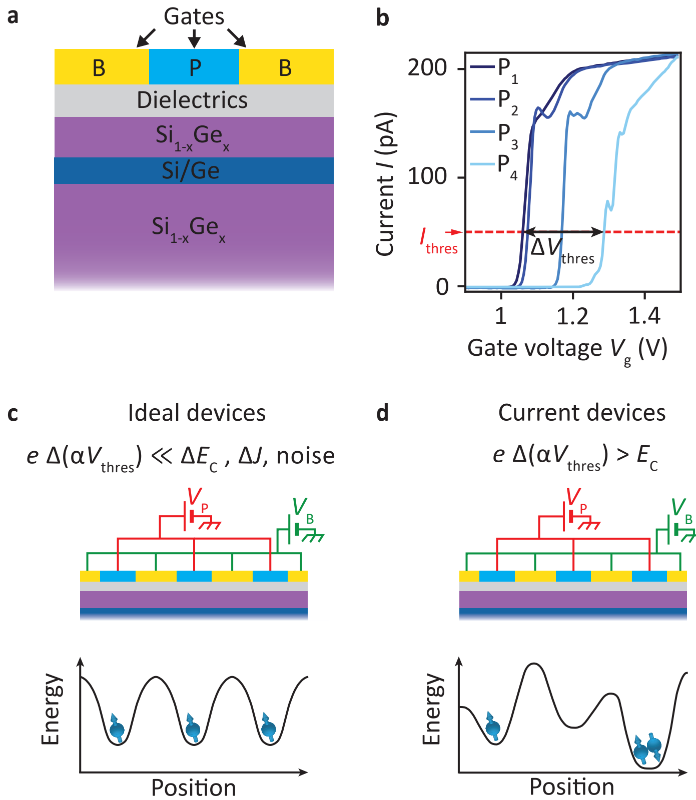

Figure 5.1: **Fluctuations in the potential landscape in semiconductor quantum dot devices. a**, Schematics of typical semiconductor heterostructures with buried quantum wells studied. The metallic gate electrodes colored in yellow and blue represent the barrier (B) and plunger gates (P) of a quantum dot array, respectively. **b**, Typical variations in the pinch-off characteristic of the plunger gates in a state-of-the-art linear quantum dot array (device A), nominally identical to the one displayed in Fig. 5.5.a, just after a cooldown. The pinch-off voltage V_{thres} is defined as the gate voltage for which the current reaches $I_{\text{thres}} = 50$ pA at a bias of $|V_{\text{sd}}| = 100$ µV. Here, the pinch-off voltages spread over a voltage range $\Delta V_{\text{thres}} = 225$ mV. **c**, Potential landscape in an ideal device with shared gate control. The application of the same voltage $V_{\text{P/B}}$ on all plunger/barrier gates leads to a regular potential landscape with fluctuations negligible compared to those of the other relevant energy scales (α denotes the gate lever arm). The quantum dots all have the same charge configuration. **d**, Potential landscape in state of the art devices with shared gate control. The application of the same voltage $V_{\text{P/B}}$ on all plunger/barrier gates leads to an irregular potential landscape due to local fluctuations which are often comparable or larger than the charging energy E_{C}. Consequently, the quantum dots have different charge configurations.

5.2. RESULTS

The gate voltage required to confine a single electron or hole typically varies between quantum dots in an array as it is dependent on the local electrostatic environment. These fluctuations also affect the pinch-off curve as exemplary depicted for sweeping the four plunger gates of a linear quantum dot device (similar to that shown in Fig. 5.5.a) in Fig. 5.1.b. The curves reveal the local depletion of a conducting path through the quantum well and experimentally can be obtained in a very short time compared to the time required for the formation of a well defined quantum dot. Therefore, we will employ pinch-off characteristics in the following to efficiently estimate variations in the potential landscape on the length scale of single quantum dots. In particular, we focus on the pinch-off voltages V_{thres} defined as the gate voltages at which a current of $I_{\text{thres}} = 50$ pA is reached for an applied source drain bias of $|V_{\text{sd}}| = 100$ μV.

GATE VOLTAGE HYSTERESIS

5

We study devices in ^{28}Si/SiGe heterostructures [40] and investigate how the pinch-off voltage of a single gate evolves depending on the previously applied gate voltages. To that end, we conduct systematic transport measurements at 4.2 K similar to sequences in [41]–[44] following the procedure depicted in Fig. 5.2.a. First a stress voltage V_{stress} is applied to the gate under study for a time $t_{\text{stress}} = 1$ min. Then the gate-voltage is swept back until the pinch-off condition $I = I_{\text{thres}}$ is met. This sequence is repeated several times with evolving stress voltages to measure the evolution of V_{thres} as a function of V_{stress}. First, the applied stress voltage V_{stress} is decreased step-wise to be increased gradually again after reaching a reversal point $V_{\text{stress}} = V_{\text{stress}}^{\text{rev}}$.

Fig. 5.2.b shows the resulting pinch-off voltage evolution for a plunger gate P_i that is part of a linear quantum dot array for two different cooldowns (light blue and dark blue curve, respectively). In these cases, V_{stress} is first lowered step-wise from $V_{\text{stress}} = 1.05$ V to $V_{\text{stress}}^{\text{rev}} = -3.7$ V. We observe that up to $V_{\text{stress}} > -2.0$ V the pinch-off voltages V_{thres} stay within ±15 mV of the first pinch-off voltage $V_{\text{thres}}^{0} = 1.06$ V forming a plateau. Then, they drop down rapidly to $V_{\text{thres}} = 0.83$ V. At $V_{\text{stress}}^{\text{rev}} = -3.7$ V, the sweep direction is reversed and we start to increase V_{stress} progressively. However, we do not observe a reversed behavior. Instead, from $V_{\text{stress}} = -2.7$ V to $V_{\text{stress}} = 0.9$ V, the pinch-off voltages increase by less than 25 mV forming a second plateau. Only when $V_{\text{stress}} = 1.0(1.1)$ V for the first(second) cooldown, V_{thres} starts to increase steeply again. The ensembles of $(V_{\text{stress}}, V_{\text{thres}})$ values draw typical hysteresis cycles with plateaus marking the ranges of applicable gate voltages over which the pinch-off voltage is not significantly changing. Furthermore, Fig. 5.2.b highlights the effect of thermal cycling on these measurements and reveals a remarkable overlap of the hysteresis cycles measured during two different cooldowns. A high degree of similarity is also observed when comparing successive measurements performed using the same stress voltage sequence as shown in Fig. 5.8 for gate S of device D. This suggests that the underlying process has a deterministic nature.

Similar experiments performed on another sample with varying reversal points $V_{\text{stress}}^{\text{rev}}$ result in the cycles plotted in Fig. 5.3. The shape of the curves is nearly identical for each iteration. Again, we observe plateaus where the pinch-off voltage deviates by less than 50 mV from its first value. Yet, the position of the plateaus varies with the chosen $V_{\text{stress}}^{\text{rev}}$. The pinch-off voltage plateaus can be shifted by up to $|\Delta V_{\text{thres}}| = 290$ mV for the

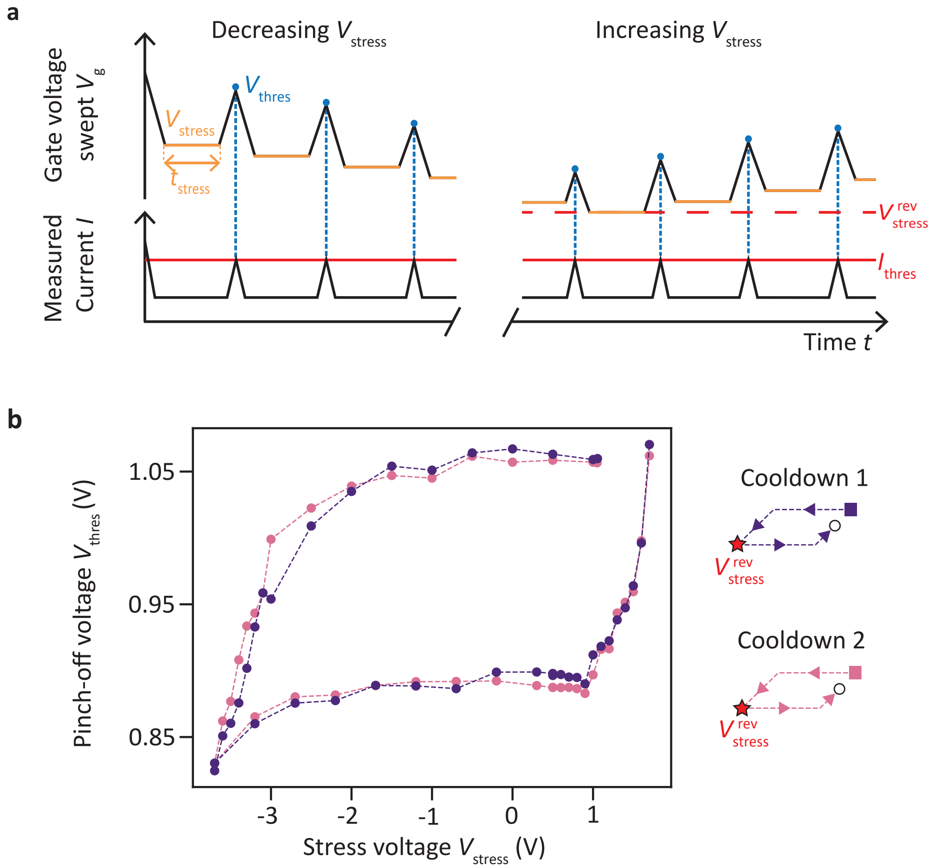

Figure 5.2: **Hysteresis of the pinch-off characteristics.** **a**, Schematics of the measurement sequence used to probe the hysteretic behavior of the pinch-off voltage V_{thres} of a single gate. V_{thres}, i.e. the voltage when the current reaches $I_{thres} = 50$ pA at a bias voltage $|V_{sd}| = 100$ µV, is measured after application of successive stress voltages V_{stress} for $t_{stress} = 1$ min. The measurements start with decreasing V_{stress}. Upon reaching $V_{stress} = V^{rev}_{stress}$, the direction is reversed and a sequence of increasing V_{stress} is applied. **b**, Evolution of the pinch-off voltage V_{thres} of the sensor plunger gate S_1 as a function of the stress voltage V_{stress} for two different cooldowns of device B. The measurement cycle is sketched on the right side. The square and the circle mark the starting point and the ending point of the cycles, respectively. The star indicates the point V^{rev}_{stress} where the stress voltage sequence is reversed. V_{stress} is first decreased before being increased again after $V^{rev}_{stress} = 3.7$ V. Both sets of points draw hysteresis cycles which overlap. The remaining gates that are needed to form a conductive channel are set to $V_0 = 1.2$ V.

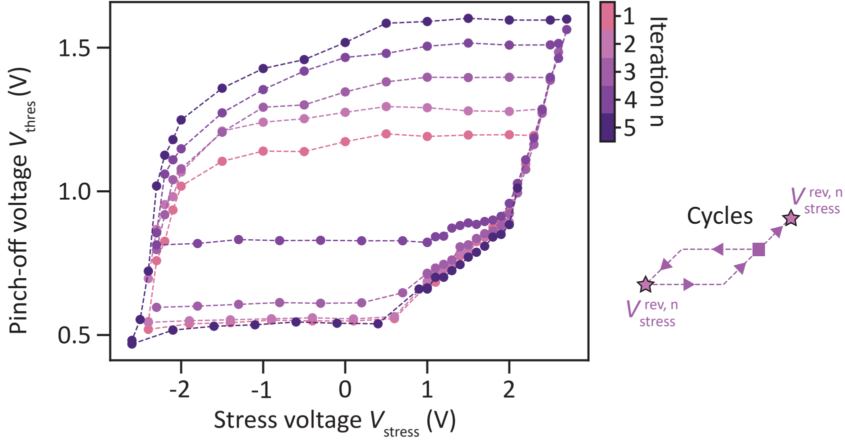

Figure 5.3: **Hysteresis with varying reversal points** (V_{stress}, V_{thres}) hysteresis cycles measured successively for plunger gate P_1 in device A. The measurement cycle is sketched in the right illustration. The square marks the starting point of the first cycle. The points where the stress voltage sequences are reversed (stars) are changed between each cycle. Note that for the fifth iteration, the stress voltage sequence with increasing V_{stress} was stopped purposely when $V_{thres} \simeq 1$ V. All other gates are set to $V_0 = 1.704$ V.

lower plateau and by up to $|\Delta V_{thres}| = 400$ mV for the upper one. Overall, Fig. 5.2.b and Fig. 5.3 suggest that by applying a dedicated voltage sequence the pinch-off voltage can be adjusted on-demand to chosen targets and thus that the intrinsic potential landscape underneath the gates can be tuned.

We also note that similar hysteretic behaviours, with sample-dependent variations of the exact shape of the (V_{stress}, V_{thres}) curves, are consistently found in several Si/SiGe devices (e.g. device D gate S shown in Fig. 5.8) as well as in samples made from Ge/SiGe heterostructures (see Fig. 5.9) suggesting a common underlying mechanism. The observed reproducibility and the large control window of the pinch-off voltage are the foundations of our approach to homogenize the potential landscape below an ensemble of gates.

STABILITY OF THE RESHAPED POTENTIAL

However, the electrical tuning of the intrinsic potential uniformity is of practical interest only if the resulting potential landscape remains stable afterwards. Therefore, we study how the pinch-off voltage evolves in time after stopping the hysteresis measurement cycle at varying points. The procedure followed is depicted in Fig. 5.4.a. The gate voltage is swept back and forth continuously to determine the voltage range $[V^{-}_{thres}(t), V^{+}_{thres}(t)]$ over which the current stays in a small range $[I_{thres} - \Delta I, I_{thres} + \Delta I]$ around the current threshold I_{thres} as a function of time t. For each sweep $[V^{-}_{thres}(t), V^{+}_{thres}(t)]$ a linear regression $I = m \times V + b$ with fitting parameters m and b is applied from which the pinch-off voltage $V_{thres}(t) = (I_{thres} - b)/m$ is extracted. Fig. 5.4.a shows the time evolution directly after the application of decreasing (violet and blue) and increasing (light pink) stress voltages. For comparison, we also plot how the pinch-off voltage evolves right after a cooldown without prior application of a stress voltage sequence (dark pink).

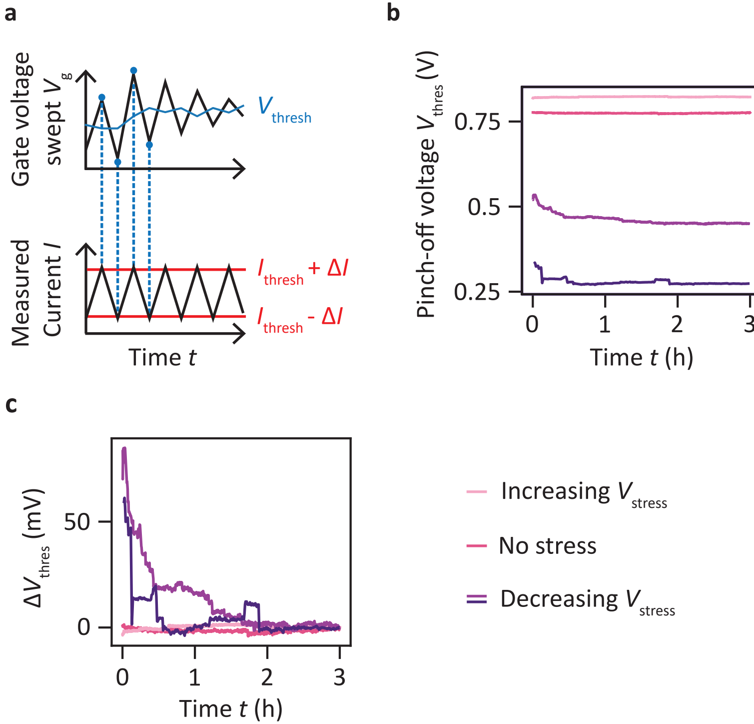

Figure 5.4: **Stability of the pinch-off voltage after tuning.** **a**, Schematical representation of the procedure used to probe the time stability of the pinch-off voltage of a single gate. The gate voltage is continuously swept back and forth to detect the voltage range $[V^{-}_{\mathrm{thres}}(t), V^{+}_{\mathrm{thres}}(t)]$ over which the current stays between $I_{\mathrm{thres}} - \Delta I$ and $I_{\mathrm{thres}} + \Delta I$ with $\Delta I \in \{10\ \mathrm{pA}, 25\ \mathrm{pA}\}$. From each sweep $V_{\mathrm{thres}}(t)$ is extracted by linear regression. **b**, Time evolution of the V_{thres} prior to any application of stress voltages (dark pink) and after tuning via application of increasing V_{stress} with $V^{\mathrm{rev}}_{\mathrm{stress}} > 0$ V (light pink) or decreasing V_{stress} with $V^{\mathrm{rev}}_{\mathrm{stress}} < 0$ V (violet and blue). The curves are obtained for sensor plunger gate S in device C, except of the pink curve which is obtained for sensor plunger gate S in device D. I_{thres} =50 pA, except for the blue curve of decreasing stress where it was defined as I_{thres} =30 pA, which provided a more robust analysis. **c**, Relative variations $\Delta V_{\mathrm{thres}}(t) = V_{\mathrm{thres}}(t) - V_{\mathrm{thres}}(t = 3\ \mathrm{h})$ of the data shown in **b**.

For decreasing V_{stress} sequences, the pinch-off voltages converge into steady states after initial decays and the time evolution exhibits random abrupt jumps. For the situation where no stress voltage or increasing stress voltages V_{stress} are applied no significant variations of V_{thres} are observed. The relative evolution depicted in Fig. 5.4.b reveals that for $t > 2$ hours, the voltage fluctuations are similar for all three situations. This is confirmed by extracting the standard deviations of V_{thres} for experiments with and without application of stress voltage sequence which are $\sigma_{\mathrm{stress}} = 0.4$ mV (increasing V_{stress}), $\sigma_{\mathrm{stress}} = 1.0$ mV and 0.6 mV (decreasing V_{stress}) and $\sigma_{\mathrm{no\ stress}} = 0.8$ mV (no stress), respectively. These experiments suggest that after a potential initial transient regime there is no change in the stability of the device due to the electrical tuning. This stability is observed for at least one hour and up to three depending on the voltage sequence applied.

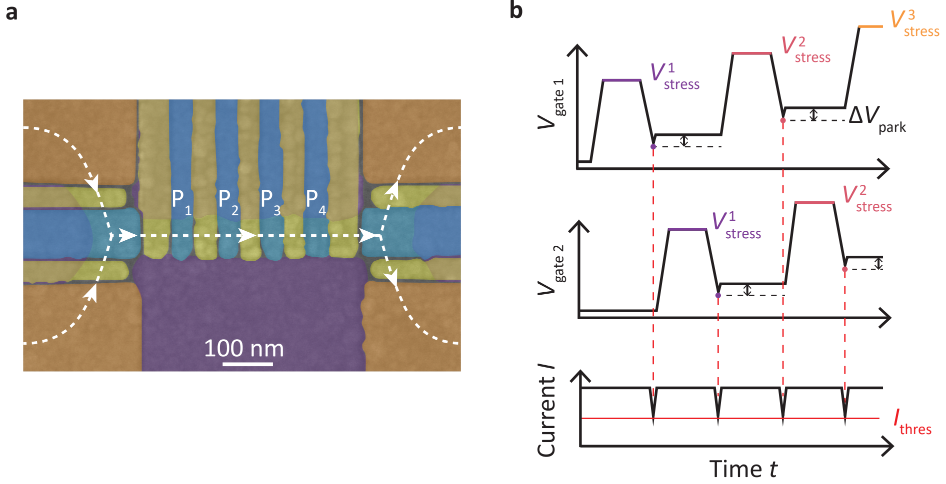

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Figure 5.5: **Stress voltage sequence to homogenize the potential landscape below the plunger gates of a linear quantum dot array. a**, Scanning electron micrograph of a linear quantum dot array. The plunger, barrier, accumulation, and screening gates are colored blue, yellow, orange, and violet, respectively. The current flow is depicted by the dashed line. We aim at equalizing the pinch-off voltages of the plunger gates P_i. **b**, Schematics of the strategy followed illustrated with only two gates for clarity. Note that here, in contrast to the illustration in Fig. 5.2.a, the pinch-off voltage V_{thres} is detected through lowering the gate voltage until $I = I_{thres}$.

HOMOGENIZATION OF PINCH-OFF VOLTAGES

Next we apply our findings and probe the capability to homogenize the pinch-off voltages V^i_{thres} of a group of plunger gates P_i with i in [1,4] in a quantum dot array. Fig. 5.5.a displays the device studied which has a geometry similar to linear quantum dot arrays in ref. [13], [16], [29], [45]. The pinch-off characteristics recorded prior to the tuning sequence are depicted in the left panel of Fig. 5.6.a and show a spread $\Delta V_{thres} = \max(V_{thres}) - \min(V_{thres})$ of 153 mV. Employing increasing gate voltage stress we tune the individual plunger pinch-off voltages to a target value $V_{target} = 1.05$ V chosen before starting the tuning. Fig. 5.5.b illustrates the procedure followed for the specific case of two gates. A schematic representation including all four gates is displayed in Fig. 5.10. V_{stress} is gradually increased in n steps. For each V^n_{stress}, the plunger gates are sequentially stressed, measured and parked $\Delta V_{park} = 50$ mV above their latest pinch-off voltage where they remain until the next stress voltage $V^{n+1}_{stress} = V^n_{stress} + \Delta V_{stress}$ is selected. When a pinch-off voltage V^i_{thres} crosses the target voltage V_{target} the corresponding plunger gate P_i is henceforth not stressed anymore. A full automated round of this sequence finishes after all pinch-off voltages are larger than the target voltage. The complete procedure is repeated two times with a stress voltage resolution of $\Delta V_{stress} = 25$ mV taking approximately 9 hours in total. All applied stress voltages and measured pinch-off voltages are visualized in the panels of Fig. 5.6.b. After each repetition a pinch-off characterization is performed with the resulting curves depicted in Fig. 5.6.a. During the first round the pinch-off voltages shift towards the target voltage V_{target} (indicated by the red dashed line) finally spreading in a range of $\Delta V_{thres} = 86$ mV around it. This spread is further re-

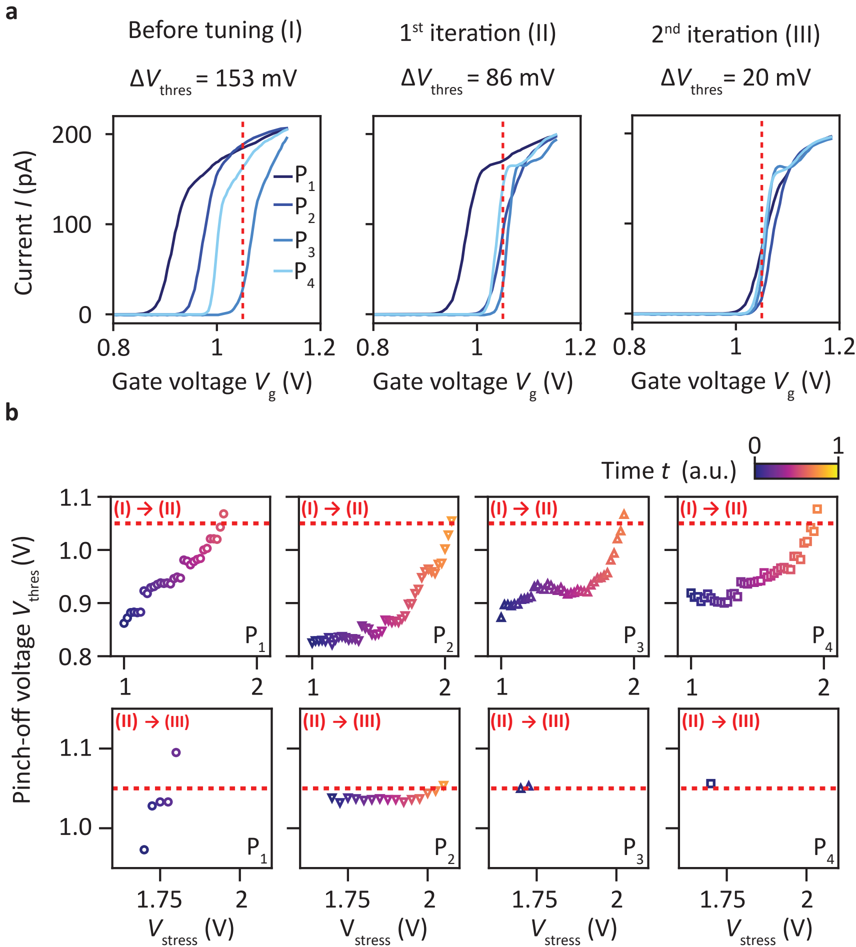

Figure 5.6: **Homogenization of plunger gate pinch-off voltages.** **a**, Evolution of the pinch-off characteristics in device A after two iterations of the tuning procedure. The target voltage V_{target} = 1.05 V is marked by a red dashed line. After two iterations the spread of the pinch-off voltage ΔV_{thres} is reduced from 153 mV to 20 mV. **b**, Evolution of V_{thres} for each gate while V_{stress} is increased during the tuning procedure. The red dashed line indicates the target pinch-off voltage V_{target} = 1.05 V. The stressing on each gate is stopped when its pinch-off voltage becomes larger than V_{target}. The coloring of the data points encodes the time evolution of the stress and pinch-off voltages of the gates during each iteration.

duced by the following iteration reaching a final value of $\Delta V_{\text{thres}} = 20$ mV. Afterwards the plunger pinch-off characteristics are observed to remain stable at least for 20 minutes (see Fig. 5.11).

5.3. DISCUSSION

To discuss our results and their implications for the tuning of quantum dot arrays, we assume that pinch-off voltages constitute a witness of the intrinsic potential landscape in the quantum well. Thus, we state that the observed tunability of pinch-off voltages also directly translates into a similar tunability of quantum dot chemical potentials. This statement is supported by a study of the effect of stress voltages on charge transitions of a quantum dot discussed in section 5.10. We find that the quantum dot potential can be tuned analogous to the threshold voltage V_{thres} by applying stress voltage sequences on the quantum dot plunger gate.

This motivates us to compare the final spread of the pinch-off voltages to the degree of uniformity needed to load an array of quantum dots with a single electron at each site using a single common gate voltage. Reaching such uniformity would require the potential fluctuations below the gates to be smaller than the average charging voltage $V_C = E_C/\alpha$ that is needed to alter the charge occupation, with E_C the charging energy and α the gate lever arm. Charging voltages typically range from 10 to 60 mV in devices similar to that under study [28], [29], [45], [46]. Consequently, the final spread $\Delta V_{\text{thres}} =$ 20 mV reached after electrical tuning promises a path towards the homogenization of quantum dot potentials inside an array. Even smaller spreads might be achievable by decreasing the stress voltage resolution ΔV_{stress}. We envision that a similar method could be used to tune the potential underneath all plunger and all barrier gates simultaneously. It could allow to also equalize the inter-dot tunnel couplings and to reach an energy landscape similar to that in Fig. 5.1.c.

At the same time, optimization of the automated procedure could lead to a significant increase of the tuning efficiency. Such an optimized procedure may be obtained by dividing the tuning into coarse and fine steps and exploring different stressing times and thereby could drastically reduce the tuning time. Additionally, utilizing a model to predict the effect of the next stress voltage, could further minimize the number of steps required to reach the target potentials and simultaneous tuning of multiple gates may be envisioned in larger quantum dot arrays.

Adapted tuning procedures may also be designed for scalable device architectures. In a crossbar gate architecture [25] such as in chapter 4, one could envision to apply different stressing voltages on different sets of gates such that only close to the crossing points of these gates the combined electric field is strong enough to shift the intrinsic potential. This would allow parallel but individual stressing of selected sites in a row-by-row manner. Another degree of selectivity might be provided through biasing of purposely isolated parts of the quantum well. Effectively, this would locally change the gates' reference potential and thereby locally alter the effect of the stressing voltages applied to them. Further work is needed to confirm the viability of these approaches.

Also, a better understanding of the underlying mechanism of the hysteresis would be valuable to exploit it most efficiently. A possible origin might be the trapping and detrapping of charge in or close to the dielectric capping layer caused by the applica-

tion of stress voltages [33]–[38]. For example, a positive stress voltage might enable the tunnelling of electrons from the quantum well or traps underneath non-stressed gates to traps underneath the stressed gate. These traps could be bound states in the non-oxidized part of the silicon capping layer or at its SiGe interface. They can be induced by charge defects in the gate oxide [47] or emerge due to mechanical stress originating from the deposition of metallic gates [26], [27]. Also, charge trapping into and out of of unpassivated silicon and germanium dangling bonds [48]–[50], charge trapping in the oxide itself mediated by leakage currents [44], [51]–[53] or movement of mobile ions [54] might be underlying the hysteresis. In all cases, when the gate voltage stress is removed the charges would be expected to be immobile at the device operation temperature and would cause local shifts in the intrinsic potential landscape observable as alterations in the pinch-off characteristics. This tunneling and trapping of charge also would be highly similar to the principle used to operate modern flash memories (based on electrically erasable programmable read only memories) which encode their stored information in pinch-off voltages and rely on gate stacks specifically engineered for that purpose [53], [55]. They could inspire new heterostructures and gate stacks with dedicated trapping layers further refining the tunability of the potential landscape using the gate voltage hysteresis.

In conclusion, we have presented a new method to increase the electrostatic potential uniformity in quantum dot devices electrically. We demonstrate that we can take advantage of hysteric shifts in gate voltage characteristics to deliberately tune pinch-off voltages across a wide range of more than 500 mV by applying stress voltage sequences. The resulting states remain stable on the time scale of hours. We also show that the chemical potential of single quantum dots can be tuned using similar procedures. Utilizing our method, we have shifted and equalized the pinch-off voltages of four plunger gates in a linear quantum dot array to a predetermined target voltage. Although most of our results were obtained in Si/SiGe heterostructures other measurements indicate that the effect and method also can be used in other heterostructure materials like Ge/SiGe. Our work opens up a new path to increase uniformity in quantum dot based spin qubits. It may enable reducing overheads in tuning and control making the implementation of scalable architectures more feasible in practise.

5.4. MATERIAL AND METHODS

MATERIALS AND DEVICE FABRICATION

The devices studied in this chapter are made from ^{28}Si/SiGe heterostructures [40]. They are grown on top of a natural Si wafer and begin by a linearly graded $Si_{1-x}Ge_x$ wafer with x varying from 0 to 0.3. A relaxed $Si_{0.7}Ge_{0.3}$ layer of 300 nm is then grown, followed by a 9 nm purified ^{28}Si layer (with 800 ppm purity) and another 30 nm thick relaxed $Si_{0.7}Ge_{0.3}$ layer. Finally, an approximately $1-2$ nm thin Si capping layer is deposited. The 2DEGs are contacted via phosphorus ion implantation. Overlapping Ti/Pd gate electrodes are deposited via electron beam evaporation. The different sets of gates are separated from each other and from the Si capping layer by 5 nm and 10 nm aluminum oxide layers, respectively, deposited through atomic layer deposition [28].

EXPERIMENTAL SET-UP

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All the measurements presented are dc-transport measurement performed at 4.2 K by dipping the devices directly in liquid helium. The gate voltages are swept using 18 bit precision digital-to-analog converters having a ±4 V range of applicable voltages. The current is measured via a current-to-voltage converter and a Keithley digital multimeter at an applied source-drain bias of $|V_{sd}| = 100\ \mu$V. The data acquisition, the application of the stress voltages and the successive pinch-off voltage measurements were performed automatically using a home-made Python program.

EXPERIMENTAL PROCEDURES

Prior to any experiment, the group and individual pinch-off voltages V_{thres} of all gates forming a given conduction channel are measured. The group pinch-off voltage is measured by sweeping all gates corresponding to the channel under investigation simultaneously until a current of typically 200 to 300 pA is reached. The corresponding voltage V_0 is the voltage at which the gates not under study are parked most of the time. The individual pinch-off voltages are then measured by sweeping each gate voltage down and back up again starting from V_0. Such measurements allow to characterize the potential uniformity just after the cooldown and to potentially discard malfunctioning devices. The measurement of individual pinch-off voltages is repeated between experiments to study how the spread of the pinch-off voltages evolves and thereby the potential uniformity. To that end, first all gate voltages responsible for forming the conducting path are set to the same value.

In most experiments, before recording a (V_{stress},V_{thres}) curve, a minimum and a maximum threshold voltage V_{thres}^{min} and V_{thres}^{max} are defined. Once $V_{thres} < V_{thres}^{min}$ or $V_{thres} > V_{thres}^{max}$ the sequence of stress voltages V_{stress} is reverted defining a reversal point V_{stress}^{rev}. Furthermore, we define minimum and maximum stress voltages V_{stress}^{min} and V_{stress}^{max} for each cycle and if $V_{stress} \leq V_{stress}^{min}$ or $V_{stress} \geq V_{stress}^{max}$ the sequence is also reversed defining a reversal point V_{stress}^{rev} as well. Tables 5.1 and 5.2 at the end of the chapter summarize the reversal points for the different experiments.

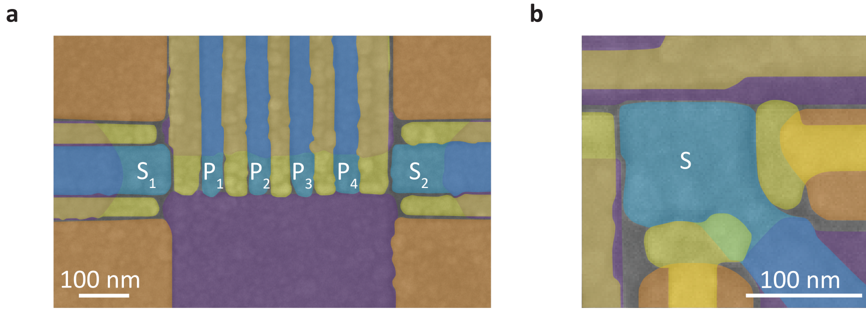

Figure 5.7: **Scanning electron micrograph of Si/SiGe devices studied.** **a**, Linear four quantum dot array, **b**, Single electron transistor at the edge of a 3×3 quantum dot array. The plunger gates are colored in blue, the barrier gates in yellow, the accumulation gates in orange, and the screening gates in violet. In **a**, the plunger gates belonging to the linear channel are labeled P_i whereas that of the charge sensors are labeled S_i. In **b**, the plunger gate of the sensor used during the experiments is labeled S.

5.5. PRESENTATION OF THE SI/SIGE DEVICES IN THIS CHAPTER

Here, we present the Si/SiGe quantum dot devices investigated in this chapter. Fig. 5.7 shows typical scanning electron micrographs of the two types of devices. They are both composed of screening, accumulation/plunger and barrier gates which are deposited in that order. The screening gates are usually kept close to 0 V to prevent the formation of conducting channels at undesired locations. The devices labeled A and B are nominally identical to the one presented in Fig. 5.7.a. It is designed to form a linear array of four quantum dots with two larger quantum dots at the ends to be used as charge sensors. The devices named C and D are of the type displayed in Fig. 5.7.b which shows a single quantum dot aimed to be a single electron transistor. It is located at the corner of a larger 3×3 quantum dot array (not shown here).

5.6. REPRODUCIBILITY OF THE ($V_{\mathrm{thres}}, V_{\mathrm{stress}}$) HYSTERESIS CYCLES

To provide further evidence of the reproducibility of the hysteresis cycles, we perform an experiment where the same sequences of decreasing and then increasing stress voltages are repeated ten times for gate S in device D. To reduce the measurement time, we focus mostly on the voltage range where V_{thres} shows a strong evolution with V_{stress}. The results are displayed in Fig. 5.8.

We recognize the left and right flanks of the hysteresis cycles as well as the end of the V_{thres} plateaus for decreasing V_{stress}. Remarkably, the data obtained for the ten iterations collapse onto single curves both for increasing and decreasing V_{stress}. This further illustrates the high reproducibility of the ($V_{\mathrm{thres}}, V_{\mathrm{stress}}$) hysteresis cycle that can be achieved.

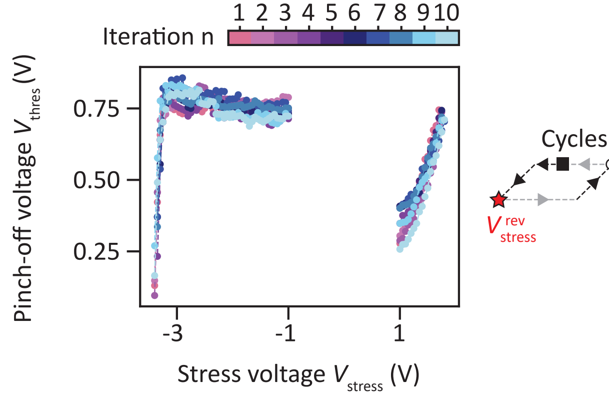

Figure 5.8: **Overlap of multiple hysteresis cycles.** Evolution of V_{thres} as a function of V_{stress} for 10 successive cycles obtained for gate S in device D. A schematic of the stress voltage sequence applied during one iteration is sketched on the right. The square and the circle mark the starting point and the ending point of the cycles, respectively. The star indicates the point where the stress voltage direction is reversed. The V_{thres} plateaus are not measured or only partially (grey dashed lines). All the curves collapse onto each other showing a remarkable reproducibility.

5.7. PINCH-OFF VOLTAGE HYSTERESIS IN GE/SIGE

The hysteretic behavior of the pinch-off voltages and its dependence on the previous stress voltages applied is not exclusive to Si/SiGe heterostructures. The same effect can be observed in Ge/SiGe heterostructures. We perform experiments similar to those discussed above in germanium single hole transistor (SHT) structures that are presented in Fig. 5.9.a. Note that these SHTs are part of a larger device presented in chapter 4.

The corresponding device is made from a strained Ge/SiGe heterostructures grown by chemical vapor deposition. Starting from a natural Si wafer, a 1.3 μm thick relaxed Ge layer is grown, followed by a 0.9 μm reverse graded $\text{Si}_{1-x}\text{Ge}_x$ (x going from 1 to 0.8) layer, a 500 nm relaxed $\text{Si}_{0.2}\text{Ge}_{0.8}$ layer, a 16 nm Ge quantum well under compressive stress, another 55 nm $\text{Si}_{0.2}\text{Ge}_{0.8}$ spacer layer and a $<$ 1 nm thick Si capping layer [56], [57]. The quantum well is contacted via 30-nm platinium contacts evaporated and diffused after etching of the oxidized Si capping layer [58]. Aluminum oxide layers of 7, 5, and 5 nm thickness grown by atomic layer deposition precede the deposition of overlapping Ti/Pd electrodes with thicknesses of 3/17, 3/27, 3/27 nm forming three different gate layers on top of the heterostructure [28].

We study the devices by applying a common gate voltage to the two barrier gates and the plunger gate defining the SHT such that a conductive channel is formed between the ohmic contacts. Fig. 5.9.b-d show typical hysteresis cycles obtained by measuring the evolution of the pinch-off voltage as function of the stress voltage applied on the three gates for each SHT. V_{stress} is first increased and then decreased in each measurement cycle contrary to the sequence followed in Fig. 5.2. These measurements are performed at base temperature of a dilution refrigerator and an estimated electron temperature of approximately 140 mK (see chapter 4) and the pinch-off voltage was defined as the voltage at which the current reaches $I_{\text{thres}} = 500$ pA at an source drain bias of $|V_{\text{sd}}| = 100$ µV.

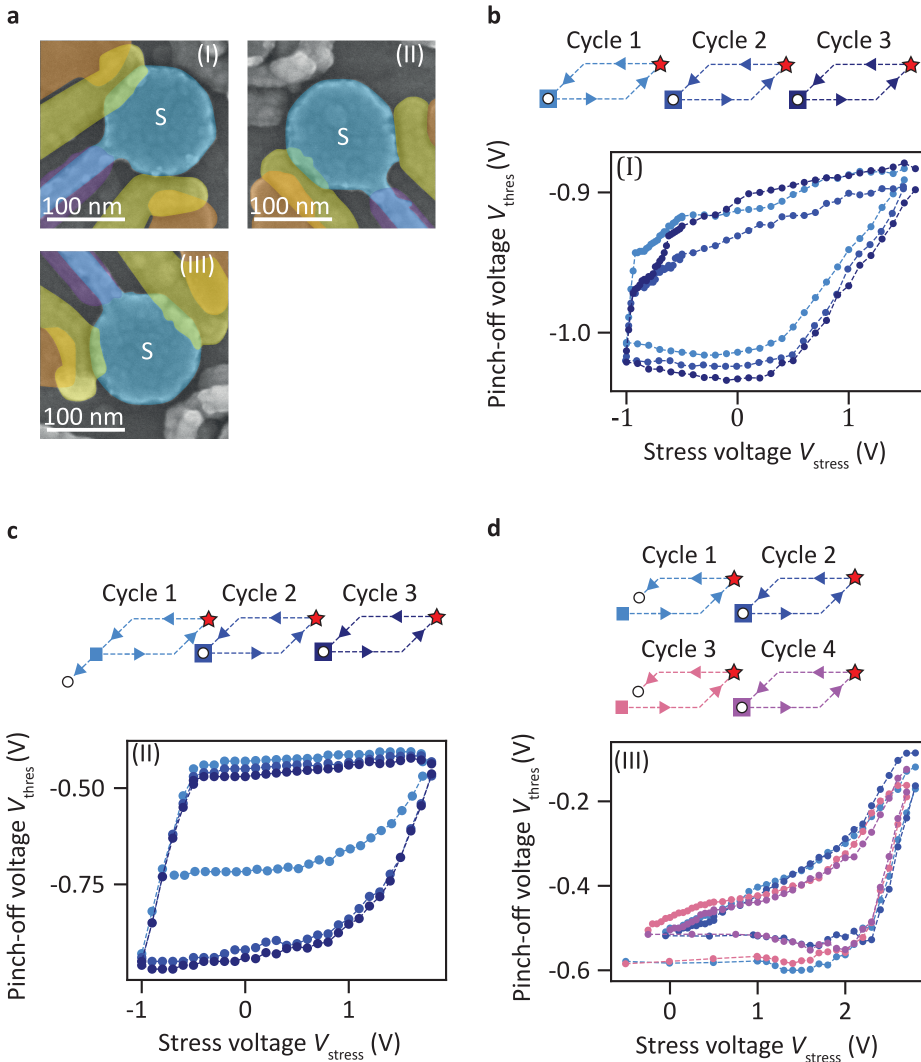

Figure 5.9: **Hysteresis of V_{thres} in Ge/SiGe single hole transistors.** **a**, Scanning electron micrograph of the SHTs studied. The plunger gates are colored in blue, the barrier gates in yellow, the ohmic contacts in orange, and the screening gates in violet. The plunger gates of the SHTs used during the experiments are labeled S while the two barrier gates are labeled as $B_{1,2}$. **b**, **c**, **d**, Evolution of V_{thres} as a function of V_{stress} for successive stress voltage cycles applied simultaneously on the barrier gates and the plunger gate forming the SHT. The stress voltage cycles are depicted schematically on the right side. The square and the circle mark the starting point and the ending point of the cycles, respectively. The stress voltage V_{stress}^{rev} upon which the stress voltage sequence is reversed is indicated by a star. For each SHT, the different data points overlap and form a hysteresis loop. In **d**, the device was kept idle for 5 hours between cycle 2 and cycle 3. This leads to a voltage difference $\Delta V_{thres} \approx -80$ mV between the last point of cycle 2 and the first point of cycle 3 similar to the time evolution discussed in Fig. 5.4. The data is taken at an electron temperature of approximately 140 mK (see chapter 4).

Overall, we observe similar features to those observed in the Si/SiGe devices i.e. overlapping hysteresis cycles with a tunable voltage range of a few hundred millivolts. These measurements highlight that the hysteresis of the pinch-off voltages is observable in multiple semiconductor heterostructures and that the tuning method presented in this chapter may be used in different materials as well.

5.8. SEQUENCE OF STRESS VOLTAGE USED FOR THE TUNING OF THE PLUNGER GATES OF THE QUANTUM DOT 1D ARRAY.

We show a schematic of the stress voltage sequence applied on the plunger gates of the quantum dot 1D array to homogenize them and obtain the data displayed in Fig. 5.6. As discussed above, the gates are sequentially stressed, one after the other, using the sequence of increasing stress voltages depicted in Fig. 5.10. After application of a stress voltage on a given gate, its pinch-off voltages is measured and then the voltage applied on it is increased by 50 mV. This voltage is kept constant during the stressing of the other gates and the characterization of their pinch-off voltage. Once the target threshold voltage is reached or exceed for one gate, we stop applying stress voltages to it.

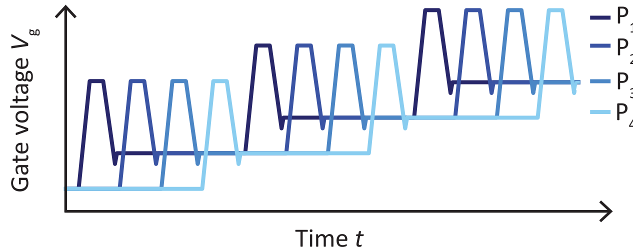

Figure 5.10: **Schematics of the voltage sequence used for the tuning of the plunger-gate pinch-off voltages.** A sequence of increasing stress voltages is applied to the plunger gates P_1-P_4 with each stress voltage being set sequentially. As soon as the pinch-off voltage of a plunger reaches the desired value the plunger is not stressed anymore (not shown).

5.9. STABILITY OF PINCH-OFF CHARACTERISTICS AFTER TUNING THEM USING THE HYSTERETIC BEHAVIOUR

Here, we discuss the stability of the pinch-off voltages after the reduction of their spread using the protocol presented in Fig. 5.5 and 5.6. Fig. 5.11 shows the pinch-off characteristics right after, 6, and 21 minutes after the tuning.

For each plunger gate considered, the three plots virtually overlap perfectly suggesting a high degree of stability. This also is in agreement with the absence of variations observed in the time stability measured after application of increasing stress voltages in Fig. 5.4. It supports our choice of using increasing stress voltages in the tuning procedure presented.

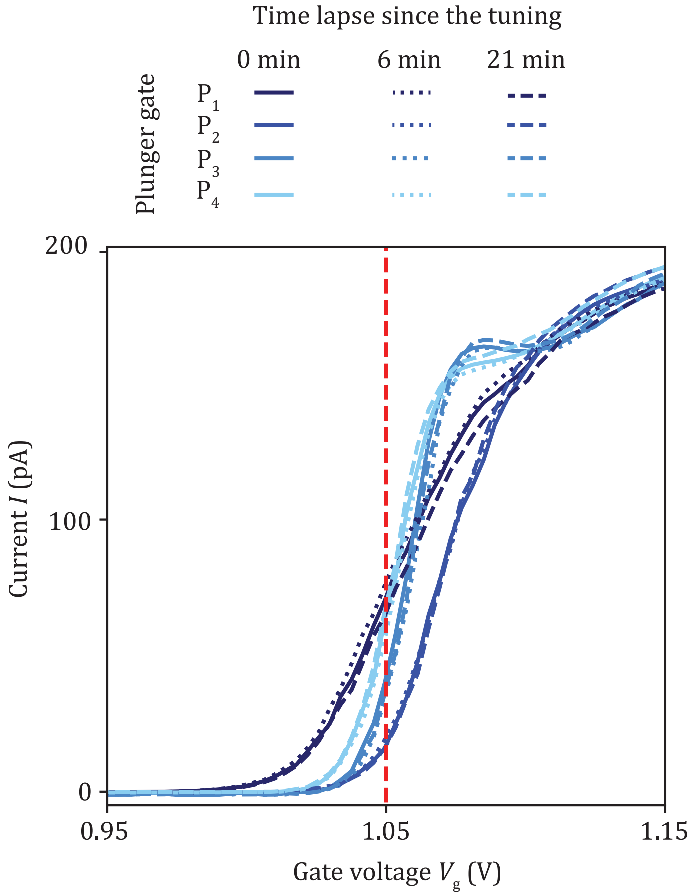

Figure 5.11: **Stability of the plunger gate pinch-off characteristics after tuning them to the target voltage.** Pinch-off characteristics measured just after (plain lines), 6 minutes (dotted lines), and 21 minutes (dashed lines) after the homogeneization procedure presented in Fig. 5.5 and 5.6 using the hysteretic shift. The red dashed line marks the target voltage of the tuning.

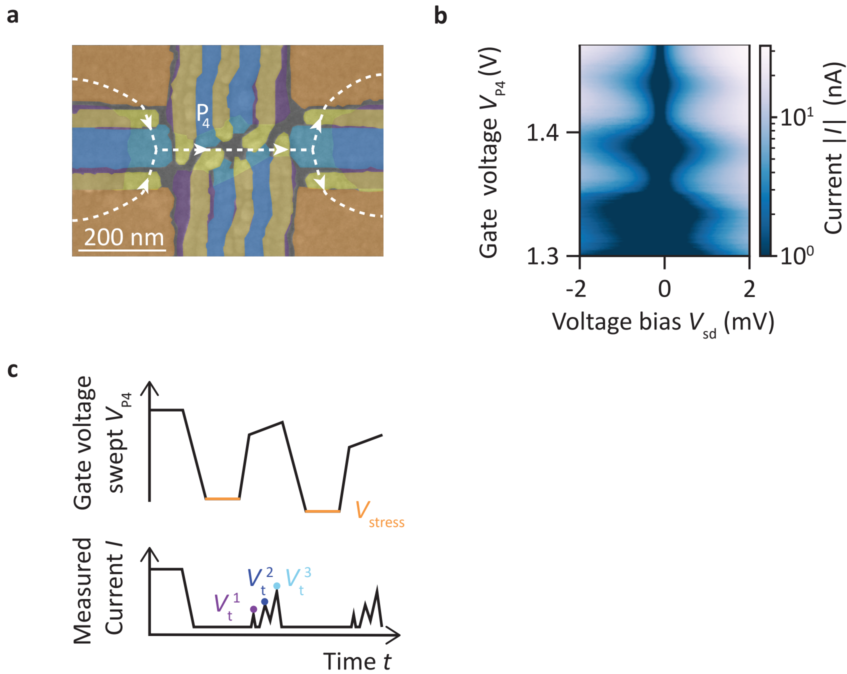

Figure 5.12: **Stress tuning a single quantum dot.** **a**, Scanning electron micrograph of the device studied (device F). The plunger gates are colored in blue, the barrier gates in yellow, the accumulation gates in orange, and the screening gates in violet. The plunger gate used during the experiment is labeled P_4. The current flow is depicted by the dashed line. **b**, Coulomb diamonds revealing a quantum dot formed under the plunger gate P_4. The color scale is cut off below 1 nA. **c**, Schematics of the stress voltage sequence applied to gate P_4 and the current measured to obtain the data displayed in Fig. 5.13.b. After the application of a stress voltage, the full pinch-off curve is taken and the first few Coulomb peaks are detected.

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5.10. COULOMB-BLOCKADE HYSTERESIS

We also investigate the effect of applying stress voltages to the plunger gate of a single quantum dot. Fig. 5.12.a shows a scanning electron micrograph of a silicon quantum dot device with the same gate layout as the device in chapter 3. The device is measured at 4.2 K and a source-drain voltage $|V_{sd}| = 100$ µV is applied from left to right. This results in a current which flows as indicated by white dashed lines in Fig. 5.12.a. We first apply a full cycle of stress voltages to the plunger gate P_4, resulting in the (V_{stress}, V_{thres}) hysteresis cycle depicted in Fig. 5.13.a which is very similar to that measured in other devices.

Next, we form a quantum dot under the plunger gate P_4 by tuning the voltages applied to P_4 and the surrounding barrier gates. The formation of the quantum dot is assessed by measuring the current flowing through the device as function of V_{sd} and the voltage applied on the plunger gate V_{P4}. Fig. 5.12.b shows the corresponding measurements. We observe Coulomb diamonds confirming the presence of a quantum dot underneath P_4. Similarly to measuring the V_{thres} hysteresis, we probe the evolution of Coulomb-blockade oscillations for a full cycle of stress voltages applied to P_4. Fig. 5.12.c contains a schematic representation of the measurement procedure. Here a full pinch-

off curve is recorded after the application of each stress voltage. This procedure is repeated multiple times for sequences of increasing and decreasing stress voltages. The resulting pinch-off curves exhibit clear Coulomb-blockade oscillations, as illustrated in Fig. 5.14.a-d, from which we extract the voltages V_t where charge transitions occur using a peak detection routine. Fig. 5.13.b depicts the evolution of the first five visible charge transitions with the applied stress V_{stress}. Like in Fig. 5.13.a, a V_t hysteresis cycle is observed which we divide in four parts (labeled I to IV). Note that the amplitude of the detected peaks can vary along the cycle and that peaks might (dis)appear. Thus, the first five peaks might not always correspond to the same five charge transitions.

To identify the evolution of a specific charge transition V_t^i, we plot the corresponding Coulomb-blockade oscillations for successive stress voltages as shown in Fig. 5.14.a-d. For parts I and III, we observe that the V_t stay approximately constant from trace to trace shifting less than their spacing. This suggest that the chemical potential in the quantum dot and the confinement remain mostly unchanged. It also allows to identify the voltages V_t^i corresponding to a specific charge transition for each stress voltage. For this purpose, we compare successive traces j and $j+1$ and we assign peak labels (coloured markers) that minimize the charge transition voltage shift $\Delta V_t^i = |V_t^i(V_{stress}^j) - V_t^i(V_{stress}^{j+1})|$. By minimizing ΔV_t^i, we also find the labelling that minimizes changes of the corresponding peak heights $I_{peak}^i = I(V_t^i)$ between two traces as depicted in Fig. 5.14.e and Fig. 5.14 g. It strengthens our confidence in the labelling of the charge transitions. We remark that in part I, around $V_{stress} = -1.2$ mV, the amplitudes of Coulomb peaks all exhibit a sudden jump. As the peak height is an indicator of the tunnel coupling between the quantum dot and its leads, we interpret this jump as a sudden change of tunnel coupling. We see no evidence for a peak shift in the corresponding Coulomb-blockade oscillation traces. This suggest the application of stress voltages can also affect the tunnel coupling independently of the quantum dot potential.

In contrast, for parts II and IV, we observe significant shifts of the charge transitions from trace to trace. Therefore, in order to identify specific charge transitions, we look for minimal shifts ΔV_t^i but we also impose a monotonous evolution of the peak height I_{peak}^i and minimize its changes $\Delta I_{peak}^i = |I_{peak}^i(V_{stress}^j) - I_{peak}^i(V_{stress}^{j+1})|$. Thus this labeling assumes that the dot tunnel coupling evolves continuously with the applied stress voltages. The assumption is strengthened by smooth I_{peak}^i evolutions depicted in Fig. 5.14.f and Fig. 5.14.h. The imposed constrains result in a peak identification with, on part II, V_t^i decreasing with decreasing stress voltages and, on part IV, V_t^i increasing with increasing stress voltages. Thus, we recover the dependence observed in Fig. 5.13.b. As the charging voltages $V_C = V_t^{i+1} - V_t^i$ plotted in Fig. 5.14.i-l remain unaffected, we attribute these shifts to changes in the quantum dot chemical potential and changes in the dot coupling to its leads.

While the identification of the charge transition voltages V_t^i (the colored markers in Fig. 5.13.b and Fig. 5.14) might not be unique for a few selected traces, overall we observe a clear trend in V_t^i. The quantum dot chemical potential follows an hysteresis cycle (Fig. 5.13.b) similar to the pinch-off voltages V_{thres} hysteresis (Fig. 5.13.a). To quantify this similarity, we extract the slopes $\mathrm{d}V_{thres}/\mathrm{d}V_{stress}$ and $\mathrm{d}V_t^i/\mathrm{d}V_{stress}$ for parts II and IV by fitting the data with linear functions. For the V_{thres} hysteresis cycle, we fit only the points marked with diamonds in Fig. 5.13.a. For the V_t^i hysteresis, we fit the charge tran-

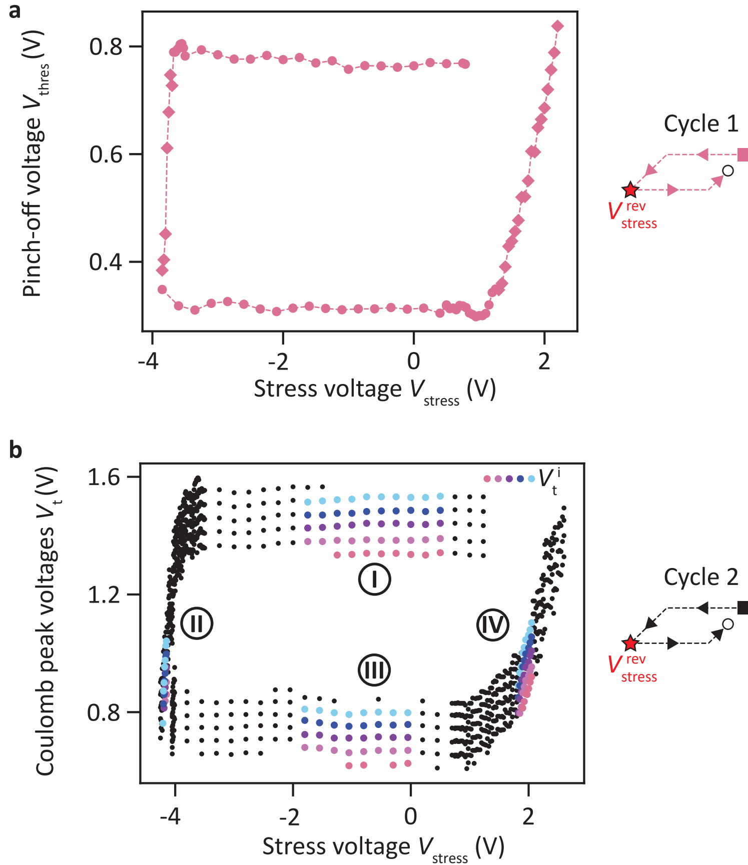

Figure 5.13: **Hysteresis of Coulomb-blockade oscillations.** **a**, V_{thres} hysteresis cycle measured before the quantum dot formation. The stress voltage cycle is depicted schematically on the right. The square and the circle mark the starting point and the ending point of the cycles, respectively. The stress voltage $V_{\text{stress}}^{\text{rev}}$ upon which the stress voltage sequence is reversed is indicated by a star. Diamonds mark the data points from which the slopes $\mathrm{d}V_{\text{thres}}/\mathrm{d}V_{\text{stress}}$ of the cycle flanges are extracted. **b**, Hysteresis of Coulomb-blockade oscillations. Black dots show the first five detected peaks of the Coulomb-blockade oscillations as a function of the stress voltage V_{stress} applied to the gate P_4. Four regimes are marked with I, II, III, and IV. For each regime individual peak voltages are colored to visualize the evolution of a specific charge transition voltage V_{t}^{i} with V_{stress}. The stress voltage cycle is depicted schematically on the right. We note that we accidentally defined a sequence that after reaching the reversal point $V_{\text{stress}}^{\text{rev}} = -4250$ mV and before applying an increasing stress voltage sequence entailed another decreasing stress voltage sequence from -4010 mV to -4050 mV.

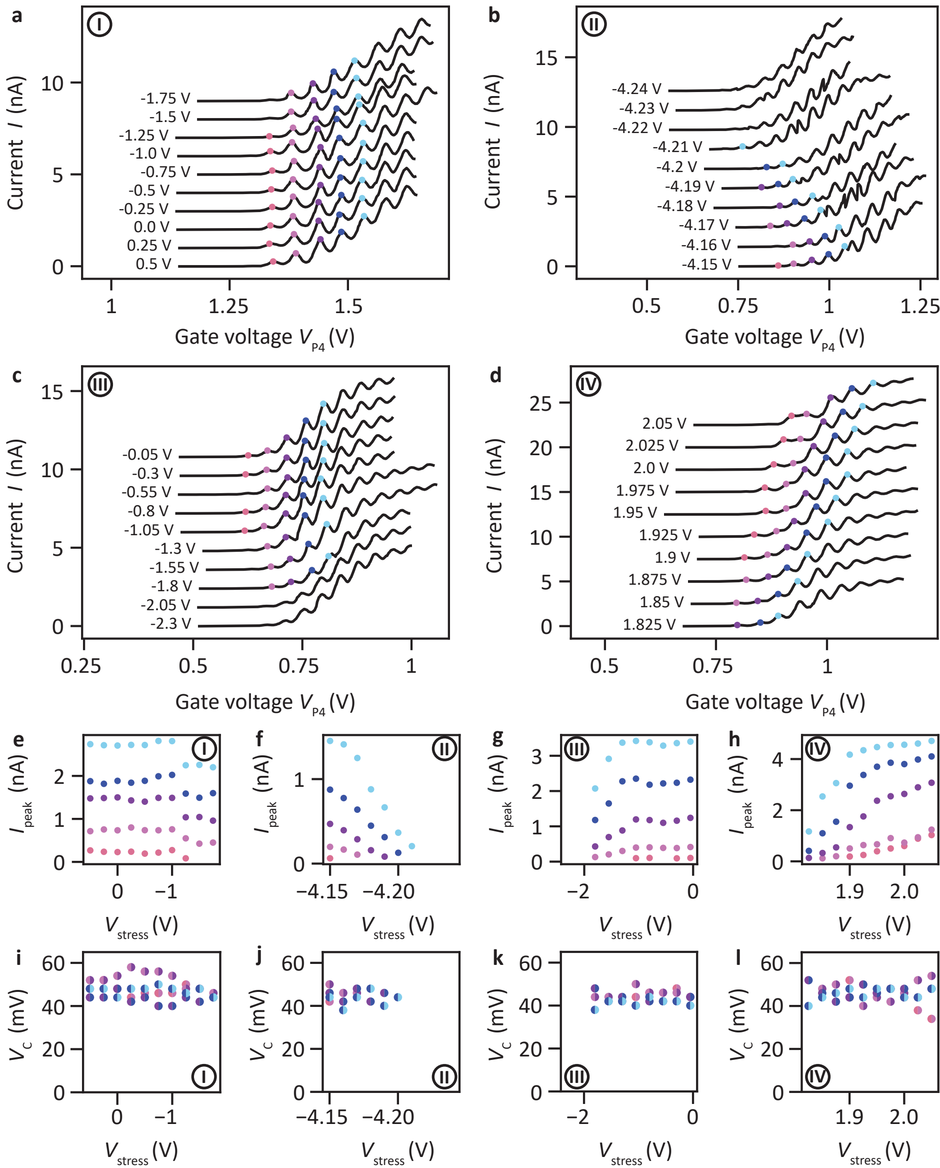

Figure 5.14: **Identification of individual transitions V_t^i. a-d**, Selected I/V-curves of the four regimes labeled in Fig. 5.13.b. The curves are offset to each other. The voltages given on the left side of the curves indicate the stress voltage V_{stress} applied just before the curve was recorded. Selected charge transitions V_t^i are identified and colored to follow their evolution with the applied voltage stress. In **a** and **c**, corresponding to parts I and III in Fig. 5.13.b, respectively, the peaks are labeled such that they show a minimal change in position. In **b** and **d**, corresponding to parts II and IV, respectively, the peaks are labeled such that their respective peak heights show a monotonous dependence with the applied stress voltages (decreasing in **b** and increasing in **d**). **e-h**, Corresponding peak heights I_{peak} of the coloured peaks in **a-d**. I_{peak} is defined as the current measured on the top of the peak. **i-l** Charging voltages $V_c = V_t^{i+1} - V_t^i$ extracted for the labeled charge transitions V_t^i in **a-d**. The two colors each marker is composed of correspond to the charge transition voltages used to calculate V_c.

sitions marked by dark blue circles. For part II, we extract $\mathrm{d}V_{\mathrm{thres}}/\mathrm{d}V_{\mathrm{stress}} = 2.77 \pm 0.35$ and $\mathrm{d}V_{\mathrm{t}}^{\mathrm{i}}/\mathrm{d}V_{\mathrm{stress}} = 3.6 \pm 0.25$. For part IV, we obtain $\mathrm{d}V_{\mathrm{thres}}/\mathrm{d}V_{\mathrm{stress}} = 0.51 \pm 0.01$ and $\mathrm{d}V_{\mathrm{t}}^{\mathrm{i}}/\mathrm{d}V_{\mathrm{stress}} = 0.87 \pm 0.06$. On both parts of the hysteresis cycles, the slopes obtained by fitting the $V_{\mathrm{stress}}/V_{\mathrm{thres}}$ and the $V_{\mathrm{stress}}/V_{\mathrm{t}}$ hysteresis cycles do not differ substantially confirming that the V_{thres} and the $V_{\mathrm{t}}^{\mathrm{i}}$ hysteresis cycles have a similar shape.

In summary, this set of measurements shows that the application of stress voltages allows to shift the chemical potential of a quantum dot. The observed hysteresis of the dot chemical potential is highly similar to that of the pinch-off voltage hysteresis for the same plunger gate. This suggests that pinch-off voltages and charge transition voltages can be equivalently utilized to witness changes in the intrinsic potential underneath a gate.

5.11. SAMPLES USED FOR EACH MEASUREMENT AND REVERSAL POINTS

Table 5.1 and Table 5.2 provide an overview of the different samples underlying the figures in this chapter, their gate design, the gates that were swept, and the reversal points $V_{\mathrm{stress}}^{\mathrm{rev}}$ after which the stress voltage sequence was reversed if applicable. The gate designs and gate names mentioned in Table 5.1 can be found in Fig. 5.7 and Fig. 5.12.a. Fig. 5.9 shows gate designs and gate names for the SHTs referred to in Table 5.2.

Figure label	Device measured	Type of device	Gate(s) swept	Cycle number	Reversal/end point(s) $V_{stress}^{rev/end}$ of the stress voltage sequence (in V)
Fig. 5.1	A	Linear array	P_1, P_2, P_3, P_4	N.A.	N.A.
Fig. 5.2.b	B	Linear array	S_1	1	-3.7 / 1.7
Fig. 5.3	A	Linear array	P_1	1	-2.4 / 2.4
				2	-2.4 / 2.5
				3	-2.3 / 2.6
				4	-2.3 / 2.7
				5	-2.6 / 2.1
Fig. 5.4 (violet, light pink, dark pink curve)	C	3 × 3 array	S	N.A.	N.A.
Fig. 5.4 (blue curve)	D	3 × 3 array	S	N.A.	N.A.
Fig. 5.6	A	Linear array	P_1, P_2, P_3, P_4	N.A.	N.A.
Fig. 5.8	D	3 × 3	S	1	-3.4 / 1.7
				2	-3.4 / 1.75
				3	-3.4 / 1.75
				4	-3.35 / 1.75
				5	-3.35 / 1.7
				6	-3.35 / 1.75
				7	-3.35 / 1.8
				8	-3.35 / 1.75
				9	-3.4 / 1.75
				10	-3.4 / 1.8
Fig. 5.11	A	Linear array	P_1, P_2, P_3, P_4	N.A.	N.A.
Fig. 5.13.a (V_{thres} hysteresis)	F	2 × 2 array	P_4	1	-3.85 / N.A.
Fig. 5.13.b and Fig. 5.14 (V_t hysteresis)	F	2 × 2 array	P_4	1	-4.25 (-4.05) / N.A.

Table 5.1: **Summary table for the Si/SiGe devices of this chapter**

Figure label	SHT measured	Type of device	Gates swept	Cycle number	Reversal/end point(s) $V_{stress}^{rev/end}$ of the stress voltage sequence (in V)
Fig. 5.9.b	I	4 × 4 array	S, B_1, B_2 (simultaneously)	1	1.5 / -1.0
				2	1.492 / -1.0
				3	-1.6 / -1.0
Fig. 5.9.c	II	4 × 4 array	S, B_1, B_2 (simultaneously)	1	1.714 / -1.0
				2	1.8 / -1.0
				3	1.8 / -1.0
Fig. 5.9.d	III	4 × 4 array	S, B_1, B_2 (simultaneously)	1	2.8 / 0.05
				2	2.8 / 0.1
				3	1.7 / -0.25
				4	2.7 / 0.0

Table 5.2: **Summary table for the Ge/SiGe devices of this chapter**

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6

SINGLE-ELECTRON OCCUPATION IN QUANTUM DOT ARRAYS AT SELECTABLE PLUNGER GATE VOLTAGE

The small footprint of semiconductor qubits is favourable for scalable quantum computing. However, their size also makes them sensitive to their local environment and variations in gate structure. Currently, each device requires tailored gate voltages to confine a single charge per quantum dot, clearly challenging scalability. In this chapter, we tune these gate voltages and equalize them solely through the temporary application of stress voltages. In a double quantum dot, we reach a stable (1,1) charge state at identical and predetermined plunger gate voltage and for various interdot couplings. Applying our findings, we tune a 2×2 quadruple quantum dot such that the (1,1,1,1) charge state is reached when all plunger gates are set to 1 V. The ability to define required gate voltages may relax requirements on control electronics and operations for spin qubit devices, providing means to advance quantum hardware.

This chapter has been published as M. Meyer, C. Déprez, I. N. Meijer, F. K. Unseld, S. Karwal, A. Sammak, G. Scappucci, L. M. K. Vandersypen, and M. Veldhorst, Single-Electron Occupation in Quantum Dot Arrays at Selectable Plunger Gate Voltage, *Nano Letters* **2023** 23 (24), 11593-11600 [1].

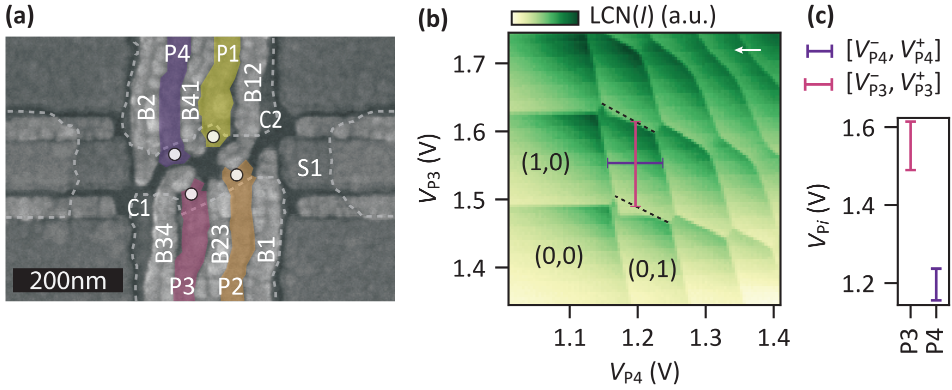

Figure 6.1: **Device and tuning of a double quantum dot.** **(a)** Scanning electron micrograph of a device nominally identical to the one under study. Confinement (Ci) and barrier (Bi and Bij) gates are designed to define four quantum dots indicated by the white circles. Their charge occupation is controlled by four plunger (Pi) gates. Confinement gates are outlined by dashed lines for clarity. A sensor quantum dot is formed under S1 and measured in transport. **(b)** Charge stability diagram showing the single-electron occupation of the Q3-Q4 double quantum dot formed underneath P3 and P4. The plotted signal is locally contrast normalized (LCN) to increase the visibility of the charge transition lines as described in section 6.4. The white arrow marks the sweep direction. Dashed lines connect charge triple degeneracy points and thereby indicate transitions of the charge ground state. These cannot be observed directly as electrons are unloaded from Q3 via Q4 leading to a dragging of charge transition lines in sweep direction (charge latching) [2]. The plunger gate voltage ranges $[V^-_{Pi}, V^+_{Pi}]$ that set a $(1,1)$ charge state are indicated by vertical and horizontal bars. The ranges are extracted around the center point of the $(1,1)$ charge region (see section 6.4). Unprocessed data shown in section 6.11. **(c)** Plunger gate voltage ranges $[V^-_{Pi}, V^+_{Pi}]$ as extracted in **(b)**.

6.1. INTRODUCTION

Semiconductor spin qubits have become a compelling platform for quantum computation. Single qubit gate fidelities of 99.99% [3] and two-qubit gate fidelities exceeding 99% [4]–[7] have been demonstrated. A moderate sensitivity to thermal effects allowed for the implementation of quantum operations above one Kelvin [8]–[10]. Furthermore, the small size of semiconductor spin qubits and their compatibility with advanced semiconductor manufacturing [11]–[13] may facilitate devices with large numbers of qubits as required for practical applications. Recent advances in the material platforms supported the realization of a 2×2 qubit array in germanium [14], a linear six qubit system in silicon [15], and the operation of a 16 quantum dot crossbar array (see chapter 4). However, scaling up the number of qubits is challenging, especially when considering the numbers needed for fault-tolerant quantum computation [16]–[18]. A particular challenge lies in the sensitivity of qubits to their environment leading to considerable variations of their properties, a notion that was already highlighted in the seminal work on quantum computation by Loss and DiVincenzo [19].

Substantial reductions in variability have been achieved through progress in heterostructure growth and device fabrication. For instance, these efforts focus on reducing material disorder [20]–[27], advancing device fabrication [28]–[30] and addressing fluctuations in mechanical stress induced by the deposition of metallic gate electrodes [31]–

[33]. However, significant variations remain observable in current devices [34], [35] (also see chapter 4) and it is an open question whether sufficient uniformity can be reached through material development alone.

Alternatively, fluctuations in the potential landscape can be compensated by temporarily applying stress voltages (see chapter 5 and refs [36]–[38]). An alternating sequence of stress voltages and pinch-off measurements has already enabled on-demand reshaping of pinch-off voltage characteristics and their homogenization without signs of reduced device stability afterwards. Furthermore, such sequences allowed to alter the potential offset of a single electron transistor (SET) at a temperature of ≈ 4.2 K (see chapter 5). Yet, this methodology has not been applied to individual electrons in a quantum dot. Also, overcoming qubit variations in quantum processors will require the tuning of multiple quantum dots.

In this chapter, we demonstrate the use of stress voltages to tune the potential landscape in a quantum dot array. We show that this approach allows to change and equalize the plunger gate voltages required to reach single-electron occupation in a double quantum dot without changing any other gate voltages. Importantly, we find that the resulting confining potential remains stable for hours afterwards. To illustrate its robustness and versatility, we demonstrate that the method employed can be applied at various barrier voltages and thus interdot tunnel couplings. Furthermore, we show that the procedure can be extended to homogenize the plunger gate voltages defining the single occupation charge state in a 2×2 quantum dot system.

6.2. RESULTS

Fig. 6.1.a shows a scanning electron micrograph of a device nominally identical to the one under study in this chapter, which is fabricated on a ^{28}Si/SiGe heterostructure [39] (see section 6.4). The gate design allows for the formation of a 2×2 quantum dot array (white circles) and two adjacent single electron transistors (SETs) on the left and right side (see chapter 3). We form the quantum dots Q3 and Q4 underneath the plunger gates P3 and P4 and also tune up the SET below the sensor gate S1. The left side of the device is operated as an electron reservoir. Fig. 6.1.b depicts a charge stability diagram recorded after the initial tuning. It shows the typical honeycomb pattern of a double quantum dot and depletion down to the $(N_3, N_4) = (1, 1)$ charge state with N_i the charge occupation of Qi.

The charge stability diagram reveals a large asymmetry in the plunger gate voltages required to reach the single-electron regime. The voltage ranges $[V^-_{\mathrm{P}i}, V^+_{\mathrm{P}i}]$ from the first to the second charge transition line of the two quantum dots are indicated by a horizontal and a vertical bar (see section 6.4 for the definition). As illustrated in Fig. 6.1.c those ranges do not overlap for the two quantum dots and in particular we find a separation of more than 2(4) times the Q3(Q4) charging voltage $V^{\mathrm{C}}_{\mathrm{P}i} = V^+_{\mathrm{P}i} - V^-_{\mathrm{P}i}$. While this is a rather extreme case, variations in the plunger gate voltages that load a single electron larger than the corresponding charging voltages are commonly observed [34], [40]–[42] (also see Fig. 2.4 in chapter 2). For instance, in chapter 4 a variability of the first charge addition voltages of 290 mV is noticed while the average charging voltage is 51 mV. Therefore, if single-electron occupation can be achieved at equal plunger gate voltages in the device of Fig. 6.1 this would provide good prospects for the homogenization of the required

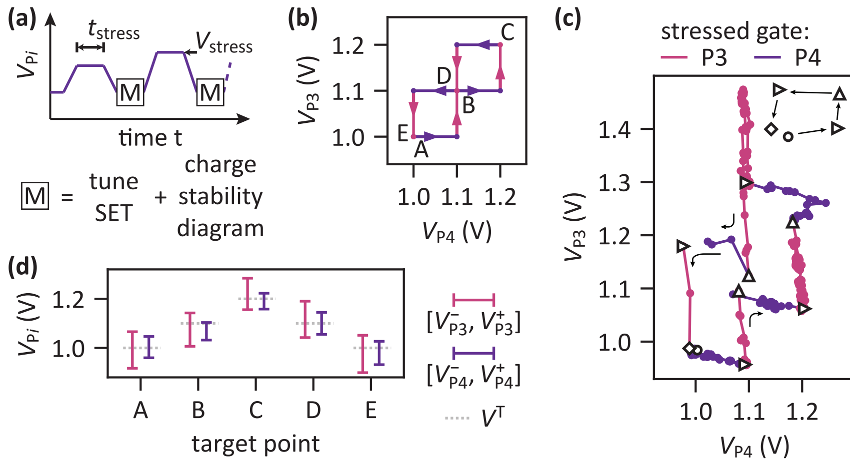

Figure 6.2: **Single-electron occupation at predetermined plunger gate voltages through voltage stressing.** **(a)** Schematic of the stress-measure sequence applied to shift the voltages required to obtain the (1,1) charge state. Increasing stress voltages V_{stress} are applied for t_{stress} = 1 min interleaved by charge stability diagram measurements. **(b)** Expected trajectory for the center of the (1,1) charge region $\boldsymbol{V}^{(1,1)}$ in the (V_{P3},V_{P4}) plane during the tuning procedure as defined prior to conducting the experiment. The color of the path refers to the plunger gate being stressed. **(c)** Actual trajectory of $\boldsymbol{V}^{(1,1)}$ followed during the tuning procedure. The triangle, circles, and diamond mark the starting point, (intermediate) targets, and the endpoint of the path, respectively. After each intermediate target, a new sequence is started as visualized by a new trace. The trace is also interrupted when insufficient contrast does not allow for obtaining $\boldsymbol{V}^{(1,1)}$. Black arrows indicate the time flow. **(d)** Plunger gate voltage ranges $[V^-_{Pi}, V^+_{Pi}]$ that keep the double quantum dot in the (1,1) charge state after tuning (see section 6.4). Targets are indicated by the dotted lines.

plunger gate voltages, also in devices that already are intrinsically more uniform.

(1,1) CHARGE OCCUPATION AT PREDETERMINED PLUNGER GATE VOLTAGE

To increase the potential uniformity, we follow the previous chapter (5) and apply stress voltages V_{stress} on gate electrodes to reshape the background potential landscape. We aim to tune the system such that the (1,1) charge state is reached at predetermined plunger gate voltage. Specifically we target to load a single electron per quantum dot for $V_{P3} = V_{P4} = V^T$ with V^T = 1 V, 1.1 V and 1.2 V by sequentially tuning the potential below the two plunger gates following the path shown in Fig. 6.2.b. Fig. 6.2.a illustrates the employed procedure for a single plunger gate Pi. We apply a stress voltage V_{stress} for t_{stress} = 1 min. Afterwards, we measure charge stability diagrams around $V_{Pi} = V^T$ and if necessary the sensor gate voltage V_{S1} is compensated to restore maximum sensitivity of the SET. From the charge stability diagrams we then extract the voltage range $[V^-_{Pi}, V^+_{Pi}]$ required to reach single charge occupation. If setting the target voltage does not yield the targeted electron occupation in Qi (V^T not in $[V^-_{Pi}, V^+_{Pi}]$) the sequence is repeated with an increased (decreased) stress voltage to shift the voltage range further upward (downward). If a single electron is loaded at the target voltage configuration we stop applying stress voltages to Pi and analogously tune the potential of the other quantum dot. After the initial tune up (Fig. 6.1), we first follow the stressing procedure to lower the required plunger gate voltage ranges $[V^-_{Pi}, V^+_{Pi}]$ to reach single-electron occupancy at 1 V. During

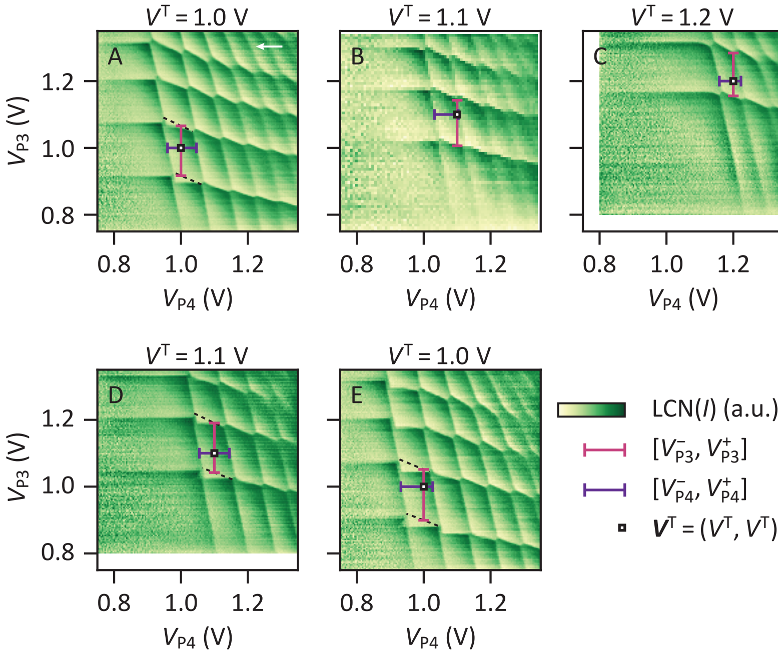

Figure 6.3: **Evolution of charge stability regions under voltage stressing.** Charge stability diagrams recorded after the application of the respective stress voltage sequences. The white square markers show the target voltages $\boldsymbol{V}^{\mathrm{T}} = (V^{\mathrm{T}}, V^{\mathrm{T}})$. Plunger gate voltage ranges $[V_{\mathrm{P}i}^-, V_{\mathrm{P}i}^+]$ that keep the system in the (1, 1) charge state are indicated by vertical and horizontal bars. Dashed lines indicate transitions of the charge ground state which cannot be observed directly due to a slow dot-reservoir tunneling time of Q3 (charge latching, see section 6.4). The white arrow marks the sweep direction which is identical for all panels. Unprocessed data shown in section 6.11.

this process we adjust the barrier gate B2 voltage in order to maintain a significant tunnel rate. Then, we perform the stressing experiment and advance from point A to E in Fig. 6.2.b. Here, we only change the sensor gate S1 voltage and keep all other gate voltages constant (see section 6.13 for the voltage settings).

Fig. 6.3 shows charge stability diagrams recorded after tuning toward the predefined targets V^{T}. A clear shift of the (1,1) charge region to higher plunger gate voltages and then back down is observable. Furthermore, after the completion of each tuning, setting the plunger gate voltages $(V_{\mathrm{P3}}, V_{\mathrm{P4}})$ to $\boldsymbol{V}^{\mathrm{T}} = (V^{\mathrm{T}}, V^{\mathrm{T}})$ (white square marker) loads a single electron per quantum dot as also highlighted in Fig. 6.2.d showing the extracted voltage ranges $[V_{\mathrm{P}i}^-, V_{\mathrm{P}i}^+]$. This demonstrates tunability of the chemical potentials and control over the electron occupation in a double quantum dot through the temporary application of stress voltage. Due to charge latching [2], for lower values of V^{T} some charge transition lines of Q3 get dragged leftwards. This suggests a crosstalk effect of the applied stress voltages on the surrounding tunnel barrier potentials.

Fig. 6.2.c shows the reconstructed evolution of the center point of the (1,1) charge region $\boldsymbol{V}^{(1,1)} = (V_{\mathrm{P3}}^{(1,1)}, V_{\mathrm{P4}}^{(1,1)})$ during the tuning procedure (see section 6.4). Overall, the experimental trajectory reproduces qualitatively the intended one shown in Fig. 6.2.b.

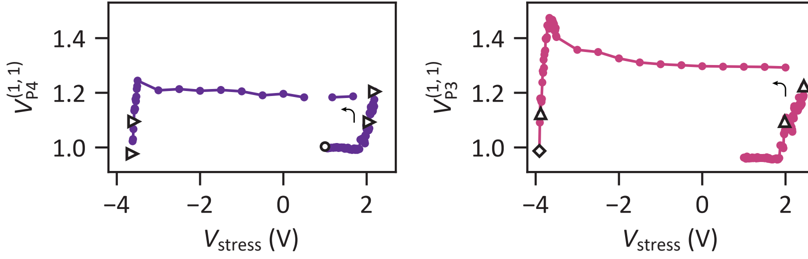

Figure 6.4: **Hysteresis of the (1,1) charge region centre voltage** $V_{P34}^{(1,1)}$ (left) and $V_{P3}^{(1,1)}$ (right) as a function of the stress voltage V_{stress} applied to P4 and P3, respectively. The triangle, circles, and diamond mark the same points as in Fig. 6.2.c and black arrows indicate the time flow.

The predominantly horizontal and vertical progressions in the $(V_{P3}^{(1,1)}, V_{P4}^{(1,1)})$ plane suggest limited crosstalk, i.e. applying stress voltages to one gate Pi only has a small effect on the charge transition voltages of the quantum dot below the other plunger gate. Quantitatively, we find slopes $dV_{Pi}^{(1,1)}/dV_{Pj}^{(1,1)}$ between −0.31 V/V and −0.04 V/V. The sign of these slopes is consistent with the sign of the capacitive shift of the transition line voltage of Qj when the plunger gate voltage V_{Pi} is changed (see section 6.5). Correcting for this effect, we obtain the change of the charge transition voltages of Qj induced exclusively by the application of stress voltages set to Pi. We find crosstalks of $(+0.37 \pm 0.03)$ V/V and $(+0.19 \pm 0.03)$ V/V for P3 on Q4 and P4 on Q3 respectively. Overall, while these crosstalk effects could be compensated for, the simple approach presented here allowed to tune the potentials of the quantum dots to the predetermined targets.

In Fig. 6.4 the center voltages $V_3^{(1,1)}$ and $V_4^{(1,1)}$ are plotted as a function of the applied stress voltage V_{stress}. We recover the typical hysteresis cycle observed when tuning pinch-off voltages using an analogous method in similar devices (see chapter 5). Noticeably, for steadily decreasing stress voltages there is an initial increase in $V_{Pi}^{(1,1)}$ before it rapidly drops to lower voltages at $V_{stress} \approx -4$ V. In Fig. 6.2.c this manifests as non-monotonic progressions of $\boldsymbol{V}^{(1,1)}$ between the target points C and D. $V_{P4}^{(1,1)}$ and $V_{P3}^{(1,1)}$ initially increase by 40 mV and 180 mV, respectively, before they decrease and approach $V^{T} = 1.1$ V.

Summarizing, Fig. 6.2, 6.3, and 6.4 demonstrate that the background potential in the quantum well can be reshaped such that each quantum dot can be occupied with one electron using uniform plunger gate voltages.

TIME STABILITY

To understand the impact of stress voltages on device stability, we record multiple charge stability diagrams as a function of time after the initial stress tuning towards $V^{T} = 1$ V (A in Fig.6.4). Fig. 6.5.a shows the extracted evolution of the plunger gate voltage range that keeps the quantum dots Q3 and Q4 in the single-electron occupation. Here, the time t refers to the time since the last application of a stress voltage and voltages are plotted relative to V^{T}. We find that the double quantum dot system remains in the (1,1) charge state for more than 15 h showing only a weak drift. This is confirmed by standard deviations of 3 mV, 3 mV, 2 mV, and 1 mV for V_{P3}^{-}, V_{P3}^{+}, V_{P4}^{-}, and V_{P4}^{+}, respectively, which remain negligible compared to the charging voltages of 148 mV and 87 mV for Q3 and

Q4, respectively. Overlaying the charge stability diagrams recorded at t = 0 h and at t = 17 h, as depicted in Fig. 6.5.b, provides further confirmation of the device stability. Additional time traces demonstrating stability up to 40 h after the application of the last stress voltages are presented in section 6.6. Moreover, we find that charge noise values sensed by the right SET are comparable to values typically observed in devices based on Si/SiGe (see section 6.8 for details).

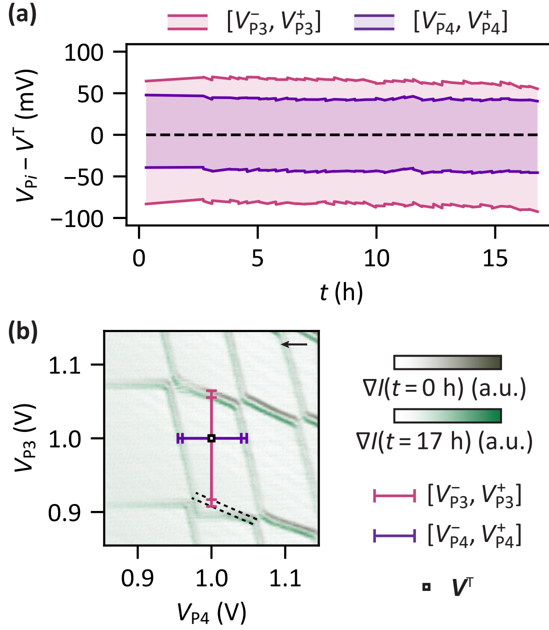

Figure 6.5: **Stability of the (1,1) charge state after stress tuning.** **(a)** Time traces of the plunger gate voltage ranges that keep the system in the (1,1) charge state (see section 6.4 for the definition) after the application of a sequence of increasing stress voltages. t is the time after the application of the last stress voltage. Note that the underlying charge stability diagram measurements were interleaved with charge noise measurements on the sensor (see section 6.8). Additional traces are presented in section 6.6. **(b)** Overlay of charge stability diagrams taken at the beginning (star, olive green) and end (hexagon, light green) of the time trace shown in **(a)**. Horizontal and vertical bars indicate the respective plunger gate voltage ranges that keep the system in the (1,1) charge state. Dashed lines indicate transitions of the charge ground state which cannot be observed directly due to a slow dot-reservoir tunneling time of Q3 (charge latching, see section 6.4). The black arrow marks the sweep direction. Unprocessed data shown in section 6.11.

PREDETERMINED PLUNGER GATE VOLTAGE FOR TUNNEL COUPLED QUANTUM DOTS

We now address the question whether single-electron occupation can still be achieved by a predetermined gate voltage, when changing the coupling between the quantum dots. In our double quantum dot system, we can control the interdot coupling by adjusting the barrier gate B34 voltage to tune the system from strong to weak coupling quantum dots. We achieve this by varying the barrier gate voltages between 0 V and −0.5 V. After setting a barrier gate voltage, we apply stress voltages to the plunger gates to obtain

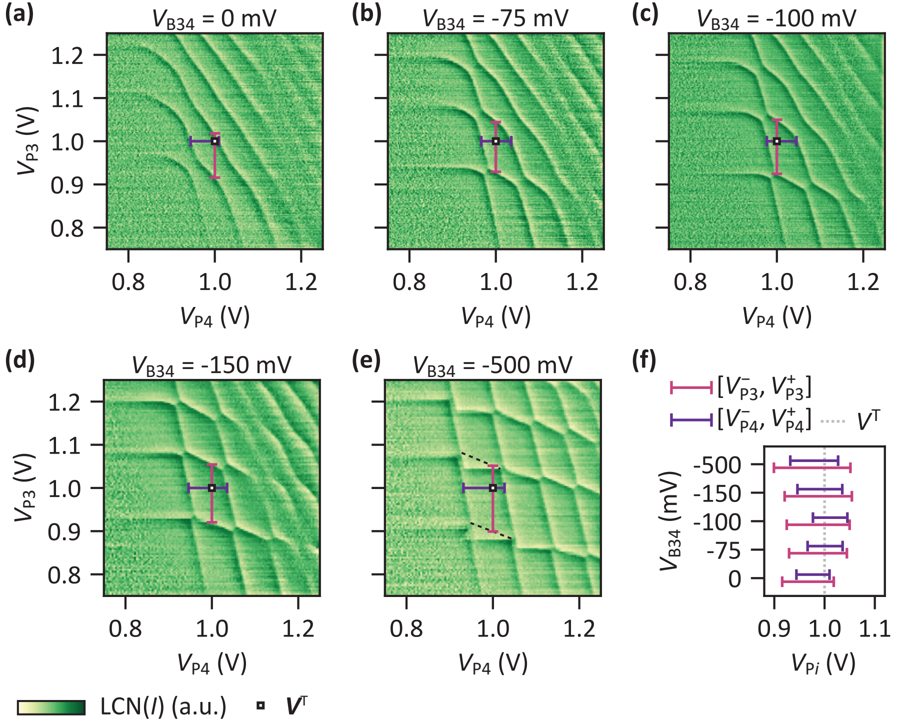

Figure 6.6: **Single-electron occupation at predetermined plunger gate voltage for high and low interdot coupling.** **(a)-(e)** Charge stability diagrams measured after tuning the system through applying stress voltages such that the (1,1) charge state is the ground state when applying the plunger gate voltages $\boldsymbol{V}^{\mathrm{T}} = (1\ \mathrm{V}, 1\ \mathrm{V})$ (white square marker). In each case a different barrier gate voltage V_{B34} is set before the tuning (labeled in the plot titles). The range of plunger gate voltages $[V^-_{\mathrm{P}i}, V^+_{\mathrm{P}i}]$ that keep the system in the (1,1) charge state is indicated by horizontal and vertical bars (see section 6.4). Dashed lines indicate transitions of the charge ground state which cannot be observed directly due to a slow dot-reservoir tunneling time of Q3 (charge latching, see supplementart section S1). The white arrow marks the sweep direction which is identical for all panels. The unprocessed data is shown in section 6.11. **(f)** Plunger gate voltage ranges $[V^-_{\mathrm{P}i}, V^+_{\mathrm{P}i}]$ extracted from **(a)-(e)**. The dotted line indicates the target voltage $V^{\mathrm{T}} = 1$ V.

the (1,1) charge state at $\boldsymbol{V}^{\mathrm{T}} = (1\ \mathrm{V}, 1\ \mathrm{V})$. Fig. 6.6.a-e shows the resulting charge stability diagrams. Note that we do not utilize virtual gates to allow for an eased identification of the stress voltage effect. The charge transition line pattern changes from exhibiting nearly diagonal lines at $V_{\mathrm{B34}} = 0$ mV towards a rectangular grid-like pattern at $V_{\mathrm{B34}} = -500$ mV, revealing the transition from high to low coupling. In all cases the application of stress voltage sequences allows to obtain the (1,1) charge state at $\boldsymbol{V}^{\mathrm{T}} = (1\ \mathrm{V}, 1\ \mathrm{V})$. This is confirmed by the extracted voltage ranges $[V_{\mathrm{P}i}^{-}, V_{\mathrm{P}i}^{+}]$ plotted in Fig. 6.6.f. We conclude that for a wide range of interdot couplings single-electron occupation can be achieved at predetermined plunger gate voltage independently of the applied barrier voltage.

(1,1,1,1) CHARGE STATE AT (1,1,1,1) V

Finally, we utilize our findings to tune a 2×2 quantum dot array such that the charge state $(N_1, N_2, N_3, N_4) = (1,1,1,1)$ is the ground state when all plunger gate voltages are set to 1 V. Starting from the Q3-Q4 double quantum dot, we form the quantum dots Q1 and Q2 which are predominantly controlled by the plunger gates P1 and P2. Then, the system is tuned solely through tailored stress voltage sequences applied to the plunger gates. Fig. 6.7 shows two charge stability diagrams recorded after this tuning process unveiling four sets of charge transition lines. These can be associated with the four quantum dots by analysing further charge stability diagrams recorded by sweeping additional plunger gate combinations (see section 6.10). Yellow, orange, red and purple dashed lines mark the first two charge addition voltages of quantum dot Q1, Q2, Q3 and Q4, respectively. The target voltage configuration $\boldsymbol{V}^{\mathrm{T}} = (V_{\mathrm{P1}}^{\mathrm{T}}, V_{\mathrm{P2}}^{\mathrm{T}}, V_{\mathrm{P3}}^{\mathrm{T}}, V_{\mathrm{P4}}^{\mathrm{T}}) = (1\ \mathrm{V}, 1\ \mathrm{V}, 1\ \mathrm{V}, 1\ \mathrm{V})$ is shown by a white square marker and the voltage ranges that keep the system in the (1,1,1,1) charge state are indicated by horizontal and vertical bars. $\boldsymbol{V}^{\mathrm{T}}$ clearly falls between the first two charge transition lines for all four quantum dots confirming that we reached the targeted configuration. Here, $V^{\mathrm{T}} = 1$ V was arbitrarily chosen but we anticipate that other target voltages can be reached as long as the crosstalk on the interdot and dot-reservoir tunnel coupling remains negligible or is compensated for. Note that all quantum dots are strongly affected by plunger gate P2 and P4 as observable in Fig. 6.7.b. However, in Fig. 6.7.a the voltages on P1 and P3 only seem to affect the charge occupation of Q1 and Q3. We speculate this behavior to originate from asymmetries in the gate layout and device imperfections (see chapter 3). Crucially, we find that the stressing procedure is effective for the tuning of a nonlinear quadruple quantum dot array.

6.3. DISCUSSION

In summary, we have shown that single-electron occupation in quantum dots can be achieved at equal predetermined plunger gate voltage, by making use of a stress-voltage based procedure. Importantly, we find that after such a tuning the systems remains stable for hours only exhibiting small progressive drifts which do not affect the charge configuration. While our experiments suggest tunability of the entire potential landscape, more research is needed to understand the level of control over the barrier potentials. We envision that the stressing methodology may find several applications in semiconductor quantum technology. For instance, it may facilitate individual control over quantum dot potentials in crossbar arrays which crucially rely on shared gate voltages [43]

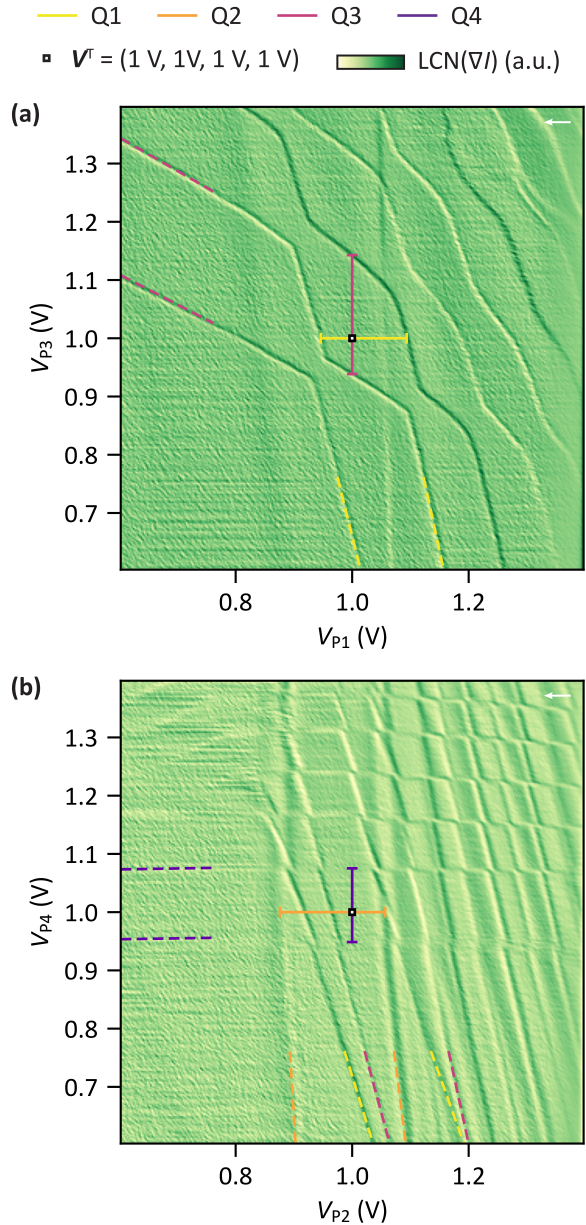

Figure 6.7: **(1,1,1,1) charge state at 1 V on all plunger gates (a), (b)** Charge stability diagrams recorded after applying stress voltage sequences to tune the (1,1,1,1) charge state to be the ground state when all plunger gate voltages are set to 1 V. The first two transition lines of each quantum dot are indicated by dashed lines. The voltage ranges to keep the system in the (1,1,1,1) charge state are indicated by horizontal and vertical bars (see section 6.4). A white square marks the point when all plunger gates are at 1 V. The plotted signal is the summation of several charge stability diagrams with identical voltage ranges recorded for slightly varied voltages on the SET plunger S1 (see section 6.12). Contrast is enhanced by a local contrast normalization (LCN). **(a)** shows charge transitions of Q1 and Q3 and **(b)** exhibits charge transition lines of all four dots. Note that in **(a)** two additional vertical transition lines are present, presumably corresponding to spurious quantum dots which however show negligible coupling to Q1-Q4. The white arrows mark the sweep direction.

(also see chapter 4). Tailored stress voltages could be applied to selected gate electrodes simultaneously. The stress voltages would be chosen to leave the background potential underneath each individual gate unaffected. However, where the selected gates are in close vicinity to each other the combined electric field would be strong enough to shift the background potential (see section 6.9). A predetermined gate voltage to set a given charge state may also relax the requirements on control electronics and facilitate their integration. For instance, lowering the required gate voltages would allow for smaller capacitors in floating gate architectures while keeping the same refresh rate [44]. Furthermore, we envision that stressing voltages can provide tunability of other parameters. For example, the g-tensor of germanium qubits is strongly dependent on the electric field [29], [45], such that stressing voltages may provide tunability over the qubit resonance frequency. We therefore envision that stressing procedures may become a standard and essential routine in the tuning of large quantum circuits.

6.4. MATERIAL AND METHODS

HETEROSTRUCTURE AND DEVICE FABRICATION

The device under study in this chapter is fabricated on a ^{28}Si/SiGe heterostructure [39] which is based on a Si wafer. First, a linearly graded $Si_{1-x}Ge_x$ buffer with x varying from 0 to 0.3 is grown followed by a 300 nm relaxed $Si_{0.7}Ge_{0.3}$ layer. A 7 nm purified (800 ppm) ^{28}Si layer defines the quantum well and is separated from the gate stack by another 30 nm thick relaxed $Si_{0.7}Ge_{0.3}$ buffer that is passivated in dichlorosilane at 500 °C. Phosphorus ion implantation is utilized to contact the two dimensional electron gas and a 10 nm aluminum oxide layer precedes the deposition of gate electrodes. The latter are spread across three layers and made of Ti/Pd deposited via electron beam evaporation. They are separated by 5 nm thick layers of aluminium oxide. In all cases aluminium oxide is deposited via atomic layer deposition [29].

SETUP AND VOLTAGE PULSES

All measurements are performed in a dilution refrigerator at a base temperature of ≈ 20 mK. The gate voltages are supplied by digital analog converters (DACs) with a resolution of 18 bit and a voltage range of ±4 V which was amplified to ±20 V for the plunger gates. The current through the SET is measured via a current-to-voltage converter connected to a digitizer module. Confinement and stress voltages are applied via the DACs while charge stability diagrams are recorded by sending fast voltage pulses. The latter are generated by an arbitrary waveform generator (AWG). DAC and AWG voltage signals are merged with a bias tee located on the sample PCB at the mixing chamber stage. AWG pulses are modified to correct for voltage drifts caused by (dis)charging of the bias tees. Furthermore, cross-capacitive shifts from P3 and P4 on the sensing dot potential are compensated for by proportionally adjusting V_{S1} when sweeping the plunger gate voltages V_{Pi} ($\Delta V_{S1}/\Delta V_{Pi} < 0.01$).

LOCAL CONTRAST NORMALIZATION

In voltage scans spanning a large range, cross-capacitive coupling of the plunger gates to the SET can cause significant variations in sensor sensitivity. This leads to contrast fluctuations across the charge stability diagram and hampers identification of charge transition lines. We compensated for this effect by applying a local contrast normalization (LCN). In essence, a smoothed charge stability map is subtracted to compensate for a slowly varying offset after which a smoothed local variance is utilized to locally normalize the signal:

$$\mathrm{LCN}(I) = \frac{I - I * f_{\mathrm{Gaussian}}}{\sqrt{(I - I * f_{\mathrm{Gaussian}})^2 * f_{\mathrm{Gaussian}}}}$$

Here, the asterisk denominates a convolution, I is the sensor signal and f_{Gaussian} refers to a normal distribution with a mean and variance chosen between 4 and 50 pixels.

EXTRACTION OF CHARACTERISTIC VOLTAGES FROM CHARGE STABILITY DIAGRAMS

For each charge stability diagram we identify the coordinates of the charge triple degeneracy points (triple points) that constitute the corners of the (1,1) charge region. From

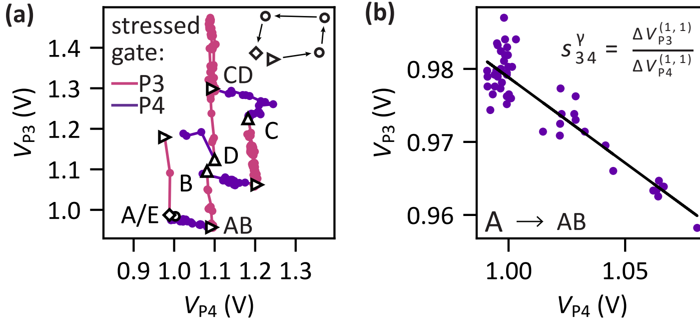

Figure 6.8: **Stress voltage induced crosstalk on quantum dots. (a)** Trajectory of the (1,1) charge state center point $\boldsymbol{V}^{(1,1)}$ in the (V_{P3}, V_{P4}) plane during the tuning experiment shown in Fig. 6.2, 6.3 and 6.4 (identical to Fig. 6.2.c). **(b)** Part of the trajectory between the points A and AB. The black line is a linear fit to the data to determine the slope s_{34}^{γ} that quantifies the crosstalk of plunger gate P4 on quantum dot Q3.

these we calculate the voltage ranges $[V_{Pi}^{-}, V_{Pi}^{+}]$ that keep the system in the (1,1) charge state around the center point $\boldsymbol{V}^{(1,1)}$ (in Fig. 6.1.b) or the target voltages $\boldsymbol{V}^{T}$ (in all other figures). The center point $\boldsymbol{V}^{(1,1)}$ of the (1,1) charge region is determined as the centroid of the triple points at the $(2,0)-(1,1)$ and $(1,1)-(2,0)$ charge transitions. Note that the voltage ranges $[V_{Pi}^{-}, V_{Pi}^{+}]$ are a measure of the maximum voltage variation on a single plunger gate for which the charge state remains constant. When taking into account more than a single gate voltage a polytope describes the applicable gate voltages that keep the charge state at single electron occupation. For instance, when considering two plunger gates the polytope would be the hexagon typically found in a double quantum dot honeycomb pattern. While we utilize one-dimensional voltage ranges $[V_{Pi}^{-}, V_{Pi}^{+}]$ to ease visualizations, after all stressing experiments the target voltage point $\boldsymbol{V}^{T}$ lies inside the single charge occupation region (inside the respective gate voltage polytope).

We have used the triple points for the analysis because of their robustness against latching effects [2]. For instance, in Fig. 6.1.b, the dashed lines show reconstructed charge transition lines of quantum dot Q3 which has a weak coupling to the nearby charge reservoir. Electrons in Q3 are unloaded via Q4 when the potential of Q4 aligns with the Fermi level. Consequentially, charge transition lines are dragged in sweep direction. Therefore, $[V_{Pi}^{-}, V_{Pi}^{+}]$ can include regions of meta-stable charge state (in between the observed and the reconstructed charge transition). This does not impact our conclusions because, at the end of all stressing experiments, the target voltage point $\boldsymbol{V}^{T}$ lies in a region of stable charge state.

6.5. STRESS VOLTAGE INDUCED CROSSTALK

A stress voltage applied to a plunger gate Pj not only alters the potential of the quantum dot Qj located directly underneath it but also affects neighbouring quantum dots Qi. We investigate this crosstalk by further analyzing the tuning of the Q3-Q4 double quantum dot presented in Fig. 6.2, 6.3 and 6.4. Fig. 6.8.a shows the trajectory of the center $\boldsymbol{V}^{(1,1)}$ of the (1,1) charge state region in the (V_{P3}, V_{P4}) plane (same as Fig. 6.2.c). The crosstalk

6

manifests as a deviation from perfectly horizontal or vertical progressions of $\boldsymbol{V}^{(1,1)}$. We quantify it by applying a linear regression as exemplary shown in Fig. 6.8.b for the section from A to AB. The extracted slope s_{34}^{γ} is a measure for the crosstalk of plunger gate P4 onto quantum dot Q3.

Two mechanisms can explain the observed crosstalk as illustrated in Fig. 6.9.a: (1) Tuning the potential landscape of Q4 through the application of stress voltages also affects the potential of Q3 even if all gate voltages are reset to their initial value afterwards. For instance, this effect could be caused by the (de)charging of traps at the interface that capacitively couple to Q3 (C_{34}^{τ}) [36]–[38], [46], [47]. (2) $V_{\mathrm{P3}}^{(1,1)}$ is defined as the middle point between the (1,0)-(1,1) and (1,1)-(1,2) charge transition at $V_{\mathrm{P4}} = V_{\mathrm{P4}}^{(1,1)}$ (and vice versa). Due to the capacitive coupling of P4 onto Q3 (C_{34}^{α}) a shift in $V_{\mathrm{P4}}^{(1,1)}$ is therefore also reflected in $V_{\mathrm{P3}}^{(1,1)}$. Fig. 6.9.b portrays the mechanism. It shows a schematic charge stability diagram before (grey charge transition lines) and after (black charge transition lines) tuning the potential below P4 through the application of stress voltages. As the Q3 charge transition lines are tilted by the cross-capacitance C_{34}^{α}, a change in $V_{\mathrm{P4}}^{(1,1)}$ also results in a change of $V_{\mathrm{P3}}^{(1,1)}$ (center point of the light and dark pink vertical bar).

To quantify the latter effect we determine the slope s_{34}^{α} of the Q3 charge transition lines at the (1,1) charge region. Fig. 6.9.c depicts an exemplary charge stability diagram during the tuning process with the respective Q3 charge transition lines indicated by dashed lines. All extracted s_{34}^{α} between the points A and AB in Fig. 6.8.a are plotted in Fig.6.9.d. We find that s_{34}^{α} remains constant throughout the entire stress voltage sequence from A to AB.

The same analysis steps are repeated for all subparts between A and D of the trajectory in Fig. 6.8.a. Fig. 6.9.e summarizes all s_{ij}^{γ} (diamonds) and s_{ij}^{α} (downward pointing triangles). The magnitude of the cross-capacitance effect s_{ij}^{α} is consistently larger than the magnitude of the measured crosstalk s_{ij}^{γ}. To estimate the stress voltage crosstalk s_{ij}^{τ} solely caused by shifts of the intrinsic potential we subtract s_{ij}^{α} from s_{ij}^{γ} and plot the difference in Fig. 6.9.e. We find a positive voltage stress related crosstalk, which has a similar magnitude as the capacitive effect s_{ij}^{α}. As s_{ij}^{τ} and s_{ij}^{α} have a different sign they partially cancel each other and lead to a reduced effective crosstalk s_{ij}^{γ} when applying stress voltage sequences.

6.6. Underlying physical mechanisms

Applying a stress voltage to a selected gate electrode possibly alters the occupation of charge traps in the gate dielectrics and heterostructure directly underneath [36]–[38], [46], [47]. As the electric field bends the conduction band electrons might tunnel into or out of these charge traps. Removing the stress voltage then effectively freezes their occupation which permanently alters the intrinsic potential landscape. Charge traps can be present in the oxide layer [48]–[51], originate from unpassivated silicon and germanium dangling bonds [49]–[51] or arise from mechanical stress induced by the deposition of metallic gate electrodes [31], [33]. Furthermore, also the relocation of mobile ions might change the intrinsic potential [52]. Note that these processes in general are independent of the quantum well material itself and stress-voltage-controlled shifts of the intrinsic

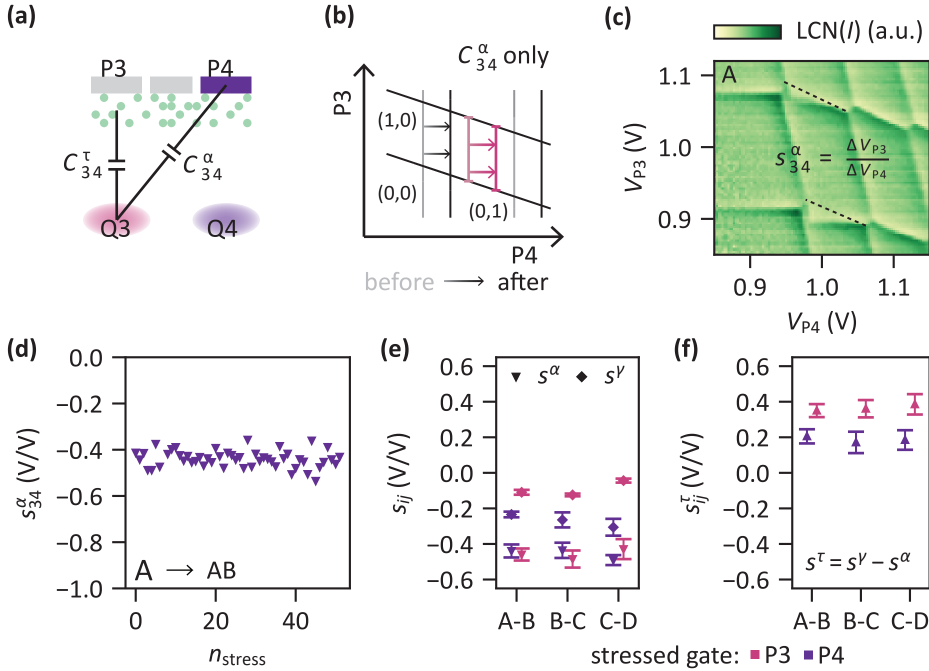

Figure 6.9: **Stress tuning crosstalk and cross-capacitance effects.** **(a)** Illustration of a device cross-section portraying the capacitive effect of the plunger gate voltage V_{P4} on the potential of quantum dot Q3 (C^{α}_{34}) and the crosstalk effect of applying stress voltages to plunger gate P4 on the potential of quantum dot Q3 (C^{τ}_{34}). **(b)** Schematic charge stability diagram illustrating how the charge transition voltages of quantum dot Q3 shift when changing the voltage on plunger gate P4. Grey lines indicate the charge transition lines before and black lines after changing the potential of Q4 through applying stress voltages. For illustration purposes, the interdot coupling between Q3 and Q4 and the capacitive coupling of P3 onto Q4 are neglected. **(c)** Example charge stability diagram taken at point A in Fig. 6.8.a. The slope s^{α}_{34} of the transition lines of Q3 (black dashed lines) are determined as a measure for the relative capacitive effect of plunger gate P4 onto the potential of quantum dot Q3. To ensure robustness against distortions from charge latching effects, the Q3 charge transition lines are defined as the lines connecting the respective triple charge degeneracy points. **(d)** All extracted s^{α}_{34} during the tuning from point A to AB in Fig. 6.8.a. **(e)** Crosstalk s^{γ}_{ij} caused by stressing plunger gate Pi (diamonds) and cross-capacitance effect s^{α}_{ij} of plunger gate voltage V_{Pj} (downward pointing triangles) onto the potential of quantum dot Qi along the trajectory in Fig. 6.8.a. Between C and CD and CD and D only the last ten points are fitted to extract s^{γ}_{ij}. Due to a limited number of data points, no values are shown for the tuning between D and E. **(f)** Stress voltage induced crosstalk effect s^{τ}_{ij} of plunger gate Pj onto the potential of quantum dot Qi corrected for the capacitive coupling of plunger gate Pj onto the potential of quantum dot Qi.

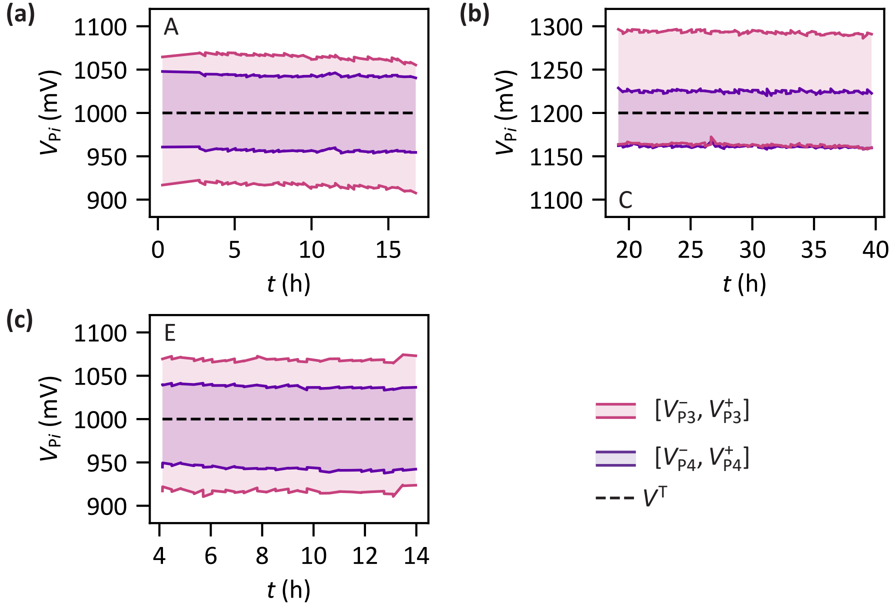

Figure 6.10: **Additional time traces after applying stress voltage sequences.** **(a)**-**(c)** Time traces of the voltage ranges $[V_{Pi}^-, V_{Pi}^+]$ after the application of a stress voltage sequence. **(a)**, **(b)** and **(c)** are recorded after tuning to the target points A, C and E as presented in Fig. 6.2, respectively. t is the time after the application of the last stress voltage. **(a)** is identical to Fig. 6.5.a. Note that the underlying charge stability diagram measurements were interleaved with charge noise measurements on the sensor (see section 6.8).

potential also have been observed in Ge/SiGe heterosturctures [53] (also see chapter 5).

6.7. ADDITIONAL TIME TRACES RECORDED AFTER THE APPLICATION OF STRESS VOLTAGES

Fig. 6.6 shows two additional time traces not shown in Fig. 6.5. Note that in Fig. 6.6.b and c the recording of the time traces was started 20 h and 4 h after the application of the last stress voltage, respectively. The additional curves confirm that after the application of a stress voltage tuning the system remains in a (1,1) charge state for 40 h at least only exhibiting small progressive drifts.

6.8. CHARGE NOISE AFTER APPLYING STRESS VOLTAGES

As the presented tuning procedure might alter the configuration of charge traps in the heterostructure (see section 6.6) we investigate the system charge noise after applying stress voltages. Specifically, we measure time traces of the current through the sensing quantum dot (underneath S1) and compute the power spectral density (PSD). To obtain maximum sensitivity of the sensor current to potential fluctuations we tune the sensor plunger gate voltage V_{S1} to the flank of a Coulomb peak. Fig. 6.11.a, b and c depict PSD spectra obtained after tuning to the target point A, C and E in Fig. 6.2.b, re-

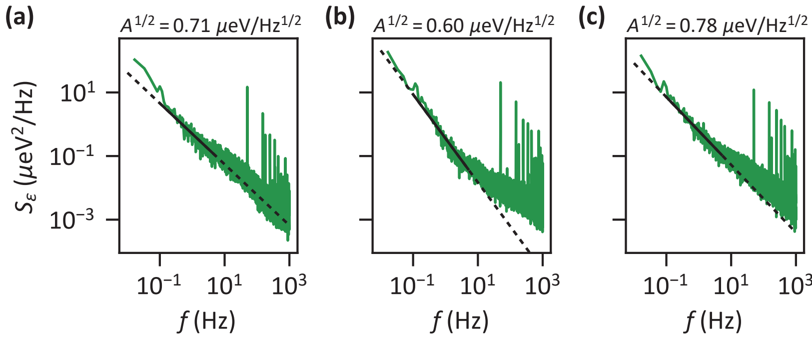

Figure 6.11: **Sensor charge noise after applying stress voltages.** **(a)** Power spectral density (PSD) extracted from sensor current time traces recorded after tuning to point A in Fig. 6.2.b. $S_\epsilon = \alpha^2 S_I/|dI/dV_{S1}|$ with α the lever arm of sensor plunger gate S1 extracted from coulomb diamonds, $|dI/dV_{S1}|$ the maximum slope of the coulomb peak and S_I the PSD of the current through the sensor [54]. For the measurement the sensor plunger voltage V_{S1} is tuned to the Coulomb peak flank, the voltage for which the sensing quantum dot is most sensitive to potential fluctuations. The black line is a fit to S_ϵ between 0.1 Hz and 5 Hz with $S_\epsilon^{\text{fit}} = A \times f^{-\kappa}$. The noise amplitude A at 1 Hz is given in the upper right. $\kappa = 0.96$ **(b)** and **(c)** Same as **(a)** but recorded after reaching target point C and E in Fig. 6.2.b, respectively. $\kappa = 1.38$ for C and $\kappa = 1.07$ for E.

spectively. Note that target points A and C are reached by applying positively signed stress voltages and target point E is reached by applying negatively signed stress voltages. The charge noise curves follow the typical $1/f$ frequency dependence. Therefore we fit them between 0.1 Hz and 5 Hz with $S_\epsilon^{\text{fit}} = A \times f^{-\kappa}$ (black line). We find noise amplitudes of $\sqrt{A} = 0.71\ \mu\text{eV/Hz}^{1/2}$, $\sqrt{A} = 0.60\ \mu\text{eV/Hz}^{1/2}$ and $\sqrt{A} = 0.78\ \mu\text{eV/Hz}^{1/2}$ as well as exponents $\kappa = 0.96$. $\kappa = 1.38$ and $\kappa = 1.07$ for target point A, C and E, respectively. These values are comparable to charge noise amplitudes in Si/SiGe reported in the literature [54]–[56] and charge noise values measured in the same device during an earlier cooldown [39]. However, further research is required as the charge noise sensed by the sensor might not be representative of the charge noise affecting qubits that are tuned in the quantum dots.

6.9. STRESS VOLTAGE TUNING IN SHARED GATE ARCHITECTURES

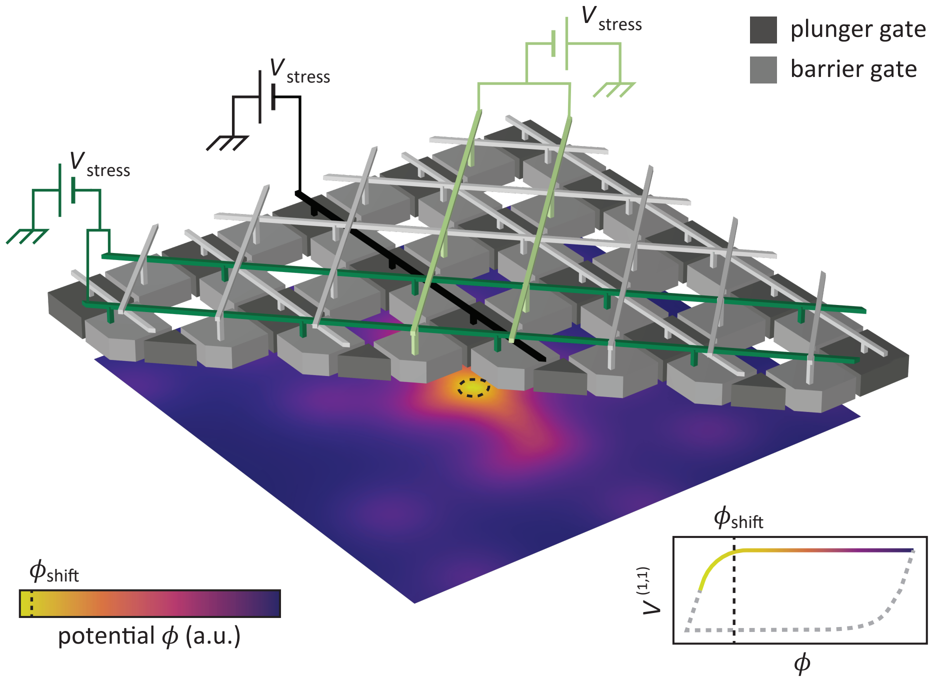

Figure 6.12: **Proposal for local tunability in a shared gate architecture.** A grid of gate electrodes intended to form a two-dimensional quantum dot array is shown in gray. Plunger gates are depicted in dark gray and barrier gates in light gray. Wires above the gates schematically indicate the routing of applied gate voltages. Plunger electrodes share voltages column-wise and barrier gates share voltages diagonally forming a crossbar architecture. Stress voltages V_{stress} are applied to a set of column wires and diagonal wires as indicated. The resulting electrical potential ϕ is illustrated below the gate electrodes. Shifting the background potential via the application of stress voltages requires that the electrical potential crosses a threshold value ϕ_{shift} as illustrated by a schematic hysteresis curve in the bottom right (also see Fig. 6.4). V_{stress} is chosen such that below each stressed gate individually ϕ does not exceed ϕ_{shift}. Thus, no hysteretic shift of the background potential is induced. However, where multiple stressed gate electrodes are in close vicinity to each other (near the crossing points of the wiring), the combined electric potential exceeds ϕ_{shift} and thus is strong enough to induce a shift in the background potential. This could enable local tunability of the electric potential, in the depicted case below the central plunger gate. A sequential application of the method to multiple combinations of gate groups may enable individual tunability of all quantum dots and tunnel barriers in a shared gate architecture.

	P1	P2	P3	P4
Q1	1	0.82	0.26	0.35
Q2	0.18	1	0.09	0.09
Q3	0.53	2.06	1	0.55
Q4	-	-	-	1

Table 6.1: **Cross coupling matrix.** The table shows the relative lever arms of the plunger gates P1-P4 to the quantum dots Q1-Q4. The displayed values are obtained by extracting transition line slopes in the charge stability diagrams of Fig. 6.13. The influence of plunger gate Pi on quantum dot Qj is given by the slope $\frac{\Delta V_{\mathrm{P}j}}{\Delta V_{\mathrm{P}i}}$ of the Qj transition line. Slopes are extracted for the first addition line at the lowest feasible charge occupation. The matrix diagonal is set to 1. Values for Q4 could not be obtained reliably as the Q4 transition is dragged due to charge latching.

6.10. IDENTIFICATION OF THE FOUR QUANTUM DOTS

In order to identify the quantum dots visible in Fig. 6.7 we measure multiple charge stability diagrams by sweeping all pairwise combinations of the device plunger gate voltages. The obtained charge stability diagrams are plotted in Fig. 6.13. The center left and bottom center panel are identical with the charge stability diagrams shown in Fig. 6.7. All maps are obtained at the same gate voltage configuration and at their center point all plunger gates are set to 1 V.

The charge stability diagrams can be analyzed starting from one charge transition line, e.g. the first vertical charge transition line in the center left panel (indicated by a yellow dashed line). Due to its strong coupling to plunger gate P1 we identify it as a charge transition line of quantum dot Q1. We mark the crossing point of this Q1 charge transition line with the $V_{\mathrm{P1}} = 1$ V line (vertical white line) by a yellow circle. Then we place another yellow circle marker at identical V_{P3} on the $V_{\mathrm{P2}} = 1$ V line in the center panel of the figure. The vertical white lines inside one row of figure panels are identical line cuts in the gate voltage space. Therefore both marked points identify the same charge transition line of the same quantum dot (Q1). Analogously two charge stability diagrams in one column of figure panels can be compared. By repeating the process for all neighbouring charge stability diagrams one can identify the charge transition lines of four quantum dots Q1-Q4. Note that the charge transition lines of quantum dot Q4 (purple) latch when the sweep direction (black arrow in the upper right of each panel) is nearly perpendicular to the charge transition lines. Therefore the crossing point of the first Q4 charge transition line with the $V_{\mathrm{P1}} = 1$ V line in the bottom left panel and the crossing point with the $V_{\mathrm{P3}} = 1$ V line in the bottom right panel differ from the crossing point with the $V_{\mathrm{P2}} = 1$ V line in the bottom center panel. Furthermore, in the left column another nearly vertical charge transition line is visible in the background. However, it shows negligible coupling to the other charge transition lines and likely is a signature of a spurious defect quantum dot outside but close to the active device region.

Additionally, table 6.1 shows the relative lever arms as extracted from the charge stability diagrams in Fig. 6.13.

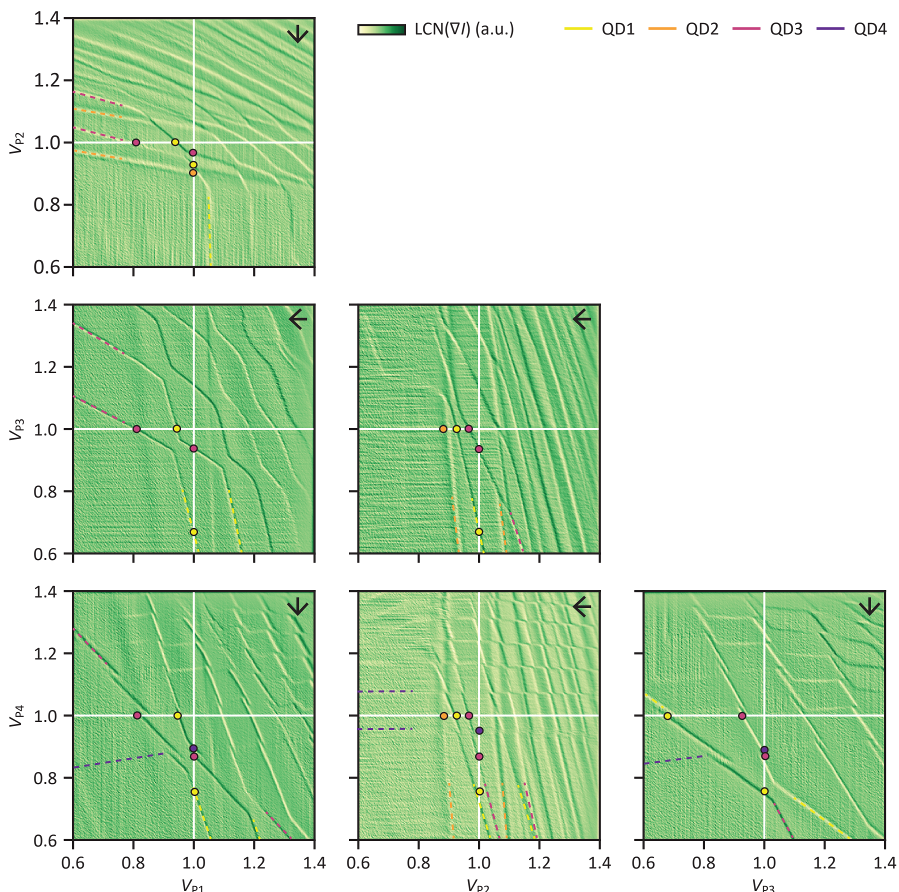

Figure 6.13: **Charge stability diagrams identifying the quantum dots Q1-Q4.** Charge stability diagrams recorded for all plunger gate combinations. The arrow in the upper left corner indicates the sweep direction. The center point (crossing point of the white lines) for each charge stability diagram corresponds to the same voltage configuration with $V_{P1} = V_{P2} = V_{P3} = V_{P4} = 1$ V. Horizontal white lines mark identical line cuts in the gate voltage space inside each column of charge stability diagrams. Vertical white lines mark identical line cuts in the gate voltage space inside each row of charge stability diagrams. Colored dashed lines indicate charge transitions and colored circles mark crossing points of the charge transitions with the white lines. Each color refers to a quantum dot as indicated by the legend in the upper right. To enhance the visibility of the charge transition lines the derivative of the sensor current was taken and a local contrast normalization (LCN) was applied.

6.11. Raw data underlying Fig. 6.1-6.6

Fig. 6.14, 6.15, 6.16, and 6.17 display the unprocessed charge stability diagram data underlying Fig. 6.1.b, 6.3, 6.5.b, and 6.6.a-e, respectively.

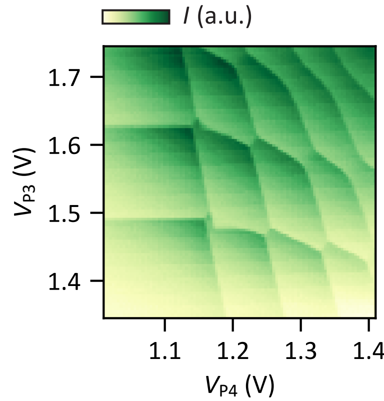

Figure 6.14: **Raw data underlying Fig. 6.1.b.**

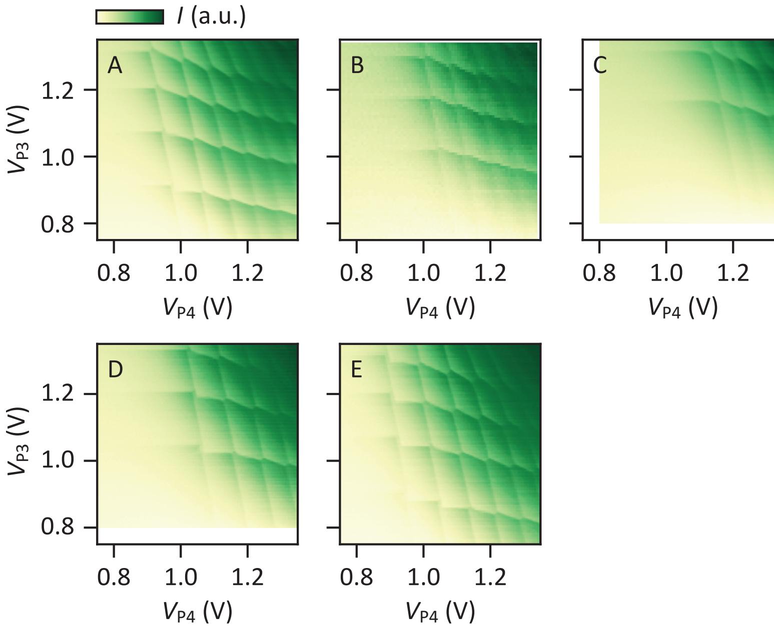

Figure 6.15: **Raw data underlying Fig. 6.3.**

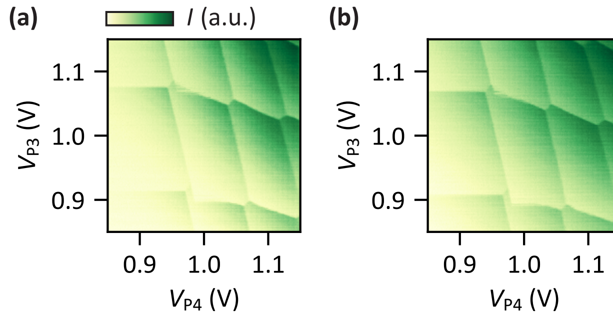

Figure 6.16: **Raw data underlying Fig. 6.5.b.** **(a)** Charge stability diagram taken at the beginning of the time trace shown in Fig. 6.5.a. **(b)** Charge stability diagram taken at the end of the time trace shown in Fig. 6.5.a.

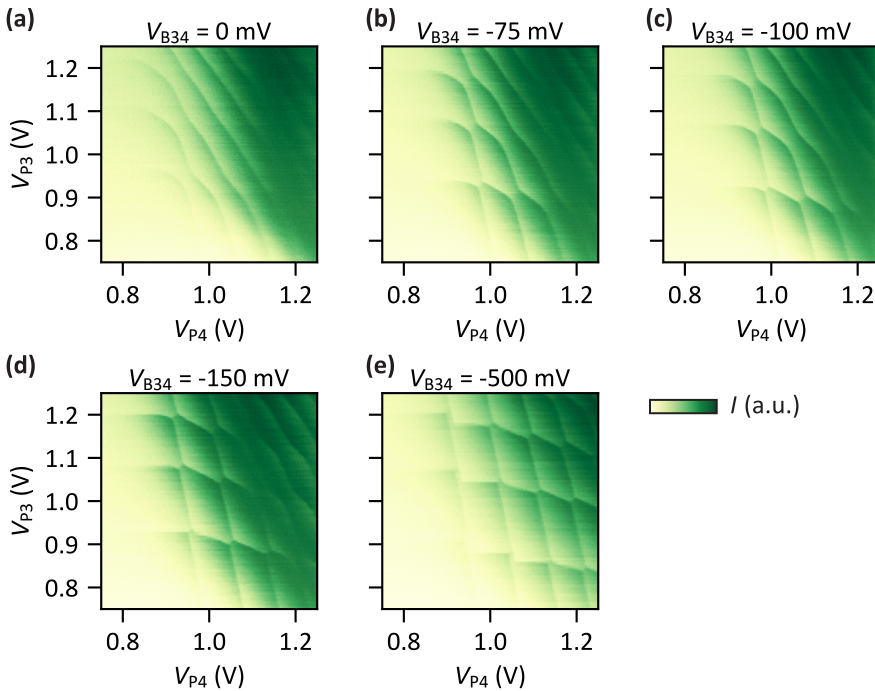

Figure 6.17: **Raw data underlying Fig. 6.6.** **(a)**-**(e)** correspond to Fig. 6.6.a-e, respectively.

6.12. RAW DATA UNDERLYING FIG. 6.7

Fig. 6.18 and Fig. 6.19 show the unprocessed charge stability diagram data underlying Fig. 6.7.a and b, respectively. Each map is recorded at a different sensor gate S1 voltage to account for the cross-capacitance effect of the plunger gates on the sensing dot potential which limits the sensing dot sensitivity to small plunger gate voltage ranges.

We combine the charge stability diagrams by summing up the sensor current signals

as exemplary shown in Fig. 6.20.a for the data shown in Fig. 6.19. Afterwards, the signal gradient ∇I is calculated as depicted in Fig. 6.20.b. Finally, a local contrast normalization (see methods section) is applied to allow for an eased identification of charge transition lines across the full map. Fig. 6.20.c depicts the resulting charge stability diagram which is identical to the charge stability diagram shown in Fig. 6.7.b.

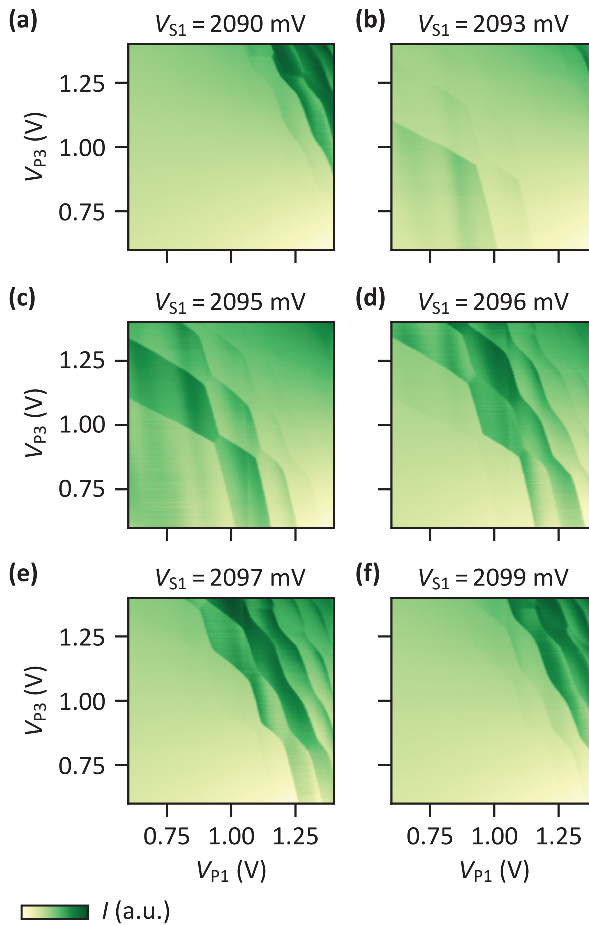

Figure 6.18: **Charge stability diagrams underlying Fig. 6.7.a. (a)-(f)** Multiple charge stability diagrams showing charge transition lines of quantum dot Q1 and Q3. Maps are taken at various sensor gate S1 voltages as indicated above the plots.

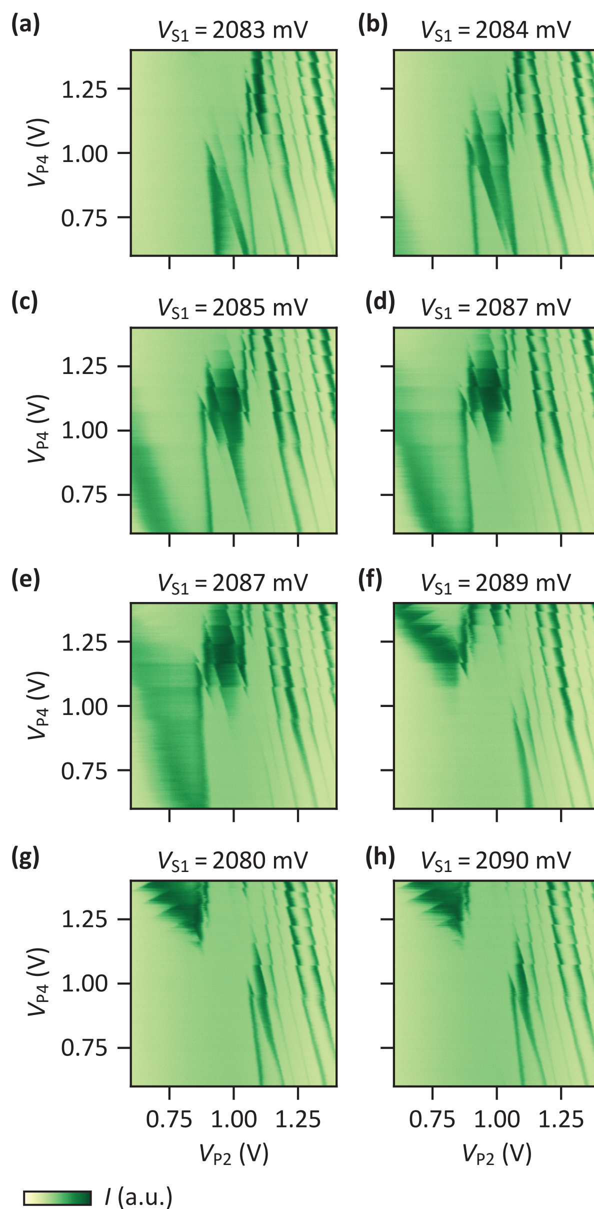

Figure 6.19: **Charge stability diagrams underlying Fig. 6.7.b. (a)-(h)** Multiple charge stability diagrams showing charge transition lines of quantum dot Q1-4. Maps are taken at various sensor gate S1 voltages as indicated above the plots.

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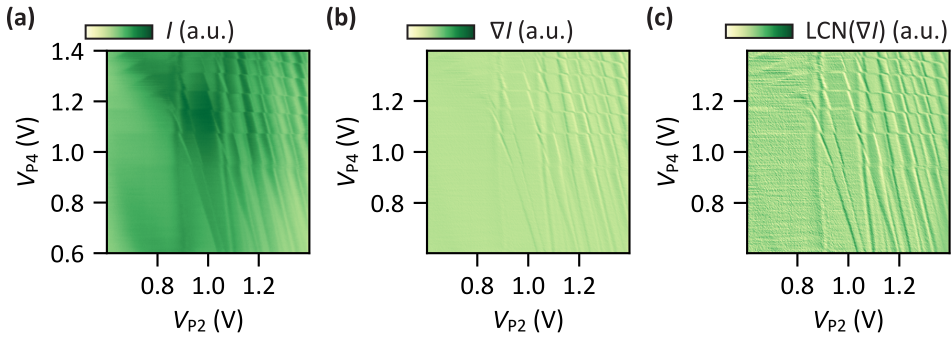

Figure 6.20: **Processing of the data underlying Fig. 6.7.b.** **(a)** Sum of the sensor response I of the charge stability diagrams shown in Fig. 6.19. **(b)** Gradient ∇I of the data shown in **(a)**. **(c)** Final signal LCN(∇I) after applying a local contrast normalization to the map shown in **(b)**.

6.13. Overview of applied gate voltage configurations

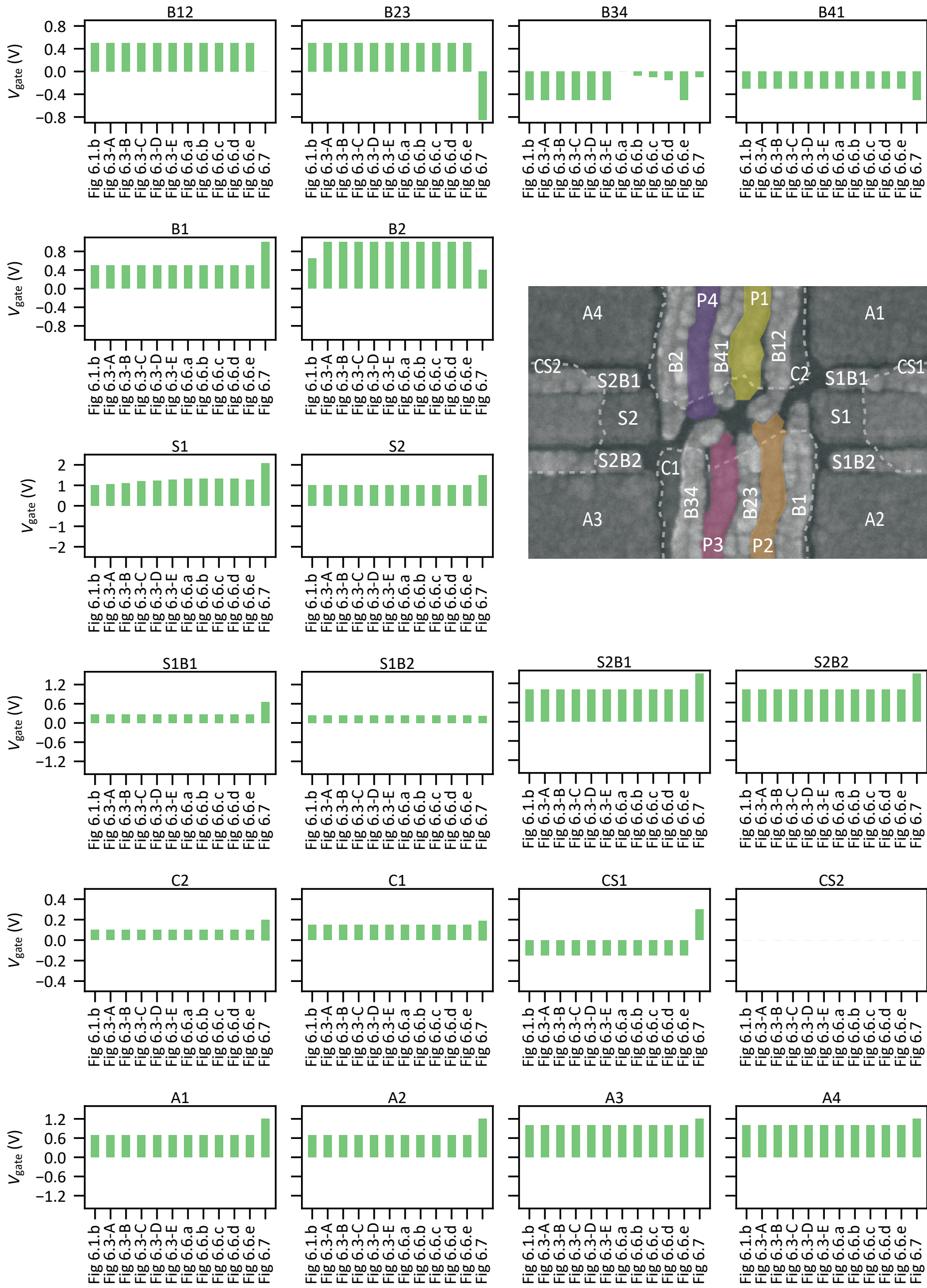

Figure 6.21: **Gate voltage evolution during the presented experiments.** Each panel shows the gate voltage evolution of a single gate during the experiments presented in Fig. 6.1-6.7 as given on the x-axis. Note that $V_{S2C} = 0$ V during all experiments. The inset shows an SEM image of a device nominally identical to the one under study. Confinement gates are outlined by a white dashed line. Labels indicate the gate electrode naming convention utilized throughout the chapter and in the panels of this figure.

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CONCLUSION

Over the last four years – the time frame of this thesis work – significant progress has been made in the field of semiconductor spin qubits. For example, industrially fabricated spin qubits became reality [1], [2], a universal gate set for exchange-only qubits was established [3] and the operability of spin qubits at elevated temperatures was demonstrated [4]–[6]. Regarding qubit count, a six-qubit quantum processor was presented [7] and germanium quantum well devices advanced from hosting a single qubit [8] to a four-qubit quantum processor [9]. Furthermore, a two-qubit gate between two distant spin qubits mediated by microwave photons was demonstrated [10] and two-qubit gates were brought to the error threshold for fault-tolerant quantum computing [11]–[13].

In this thesis, chapters 3, 4, 5, and 6 presented contributions to the development of two-dimensional quantum dot arrays for spin qubits and introduced a new method to engineer the uniformity of the required voltages in these arrays:

TWO-DIMENSIONAL QUANTUM DOT ARRAYS

The realization of two-dimensional spin qubit arrays can significantly increase qubit connectivity and qubit density compared to linear arrays. In GaAs/AlGaAs, which is often seen as a testbed for other material systems, arrays of up to 3×3 quantum dots had already been explored [14]–[16] and arrays for singlet-triplet qubits or with shared control electrodes are being engineered [17], [18]. In silicon systems, two-dimensional arrays are reported on in fin field effect transistor (finFET) devices which naturally allow for $2 \times N$ quantum dot arrays [19]–[21]. Here, the 2×2 array in Si/SiGe presented in chapter 3 presents the first realization of a two-dimensional quantum dot array in a planar silicon quantum well. Also, it is the first two-dimensional system in silicon to provide barrier voltage control over the interdot tunnel couplings. In Ge/SiGe a 2×2 quantum dot array was characterized by van Riggelen et al. [22] and advanced into a spin qubit processor by Hendrickx et al. [9]. This number of quantum dots was quadrupled with the 4×4 quantum dot array presented in chapter 4 which in contrast to conventional devices relied on shared gate electrodes for plunger and barrier gates. Additionally, a scheme to individually control the interdot tunnel couplings in such an array was introduced and demonstrated by example. For both, the Si/SiGe 2×2 (chapter 3) and Ge/SiGe 4×4 (chapter 4) quantum dot array, considerable control over the charge occupancy was shown by simultaneously reaching single charge occupation with either one or three charges per quantum dot.

GATE VOLTAGE UNIFORMITY

Increasing the electrical uniformity is a target of material development for semiconductor spin qubits and significant progress has been made during the last few years. Burying the quantum well in a semiconductor as in Si/SiGe and Ge/SiGe [23], improving the semiconductor-oxide interface [24], adjusting the buffer layer and quantum well properties [25]–[28], and Ge/SiGe heterostructures grown on germanium wafers [29] all contributed to higher mobilities and thus better electrical uniformity. A method that can be applied after growth and fabrication and that is fully based on gate voltage sequences was presented in chapter 5 and applied to quantum dots in chapter 6. It allowed to reach single electron occupation in a 2×2 quantum dot array at all equal plunger gate voltages.

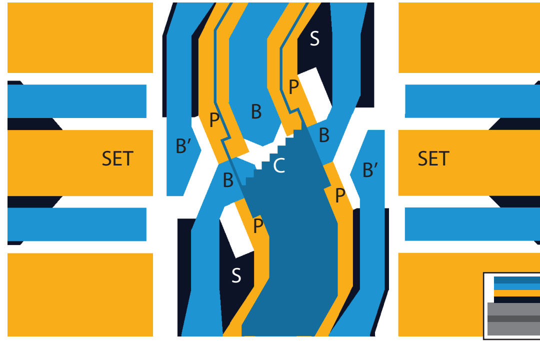

Figure 7.1: **Updated gate electrode design for a two-by-two quantum dot array.** Zoom in on the active area designed to form quantum dots. The design is mostly identical to the layout of the devices presented in chapter 3, chapter 5 section 5.10, and chapter 6. Single electron transistors (SETs) are placed on the left and right sides. Screening (S), plunger (P), and barrier (B, B') gates are designed to provide electron confinement and control over the quantum dot chemical potential and interdot tunnel coupling. A new gate (C) is placed in an additional gate layer on the top to keep the electron wavefunctions away from the device center. For the upper half only its outline is shown. The inset in the lower right corner illustrates the order of the gate layers.

The following sections present ideas for the near and more distant future on how two-dimensional arrays and their uniformity could be further advanced.

7.1. BETTER AND LARGER TWO-DIMENSIONAL QUANTUM DOT ARRAYS

In chapter 3 a two-by-two quantum dot array in a Si/SiGe heterostructure was presented. Its barrier gate electrodes allowed to individually increase the tunnel coupling of quantum dot pairs, promising the implementation of exchange-based two-qubit gates at the charge noise sensitivity sweet spot [30]–[32]. The lowest tunnel coupling that was achieved $t_{\mathrm{min}} = 30\ \mu\mathrm{eV}$ is estimated to translate to a residual exchange coupling of $J_{\mathrm{min}} \approx \frac{(2t_{\mathrm{min}})^2}{E_C} \approx$ 135 MHz with $E_C \approx 6$ meV the corresponding charging energy [33]. A lower residual exchange coupling would benefit the implementation of fast diabatic controlled phase gates [4] which already allowed to reach high fidelity two-qubit gates in Si/SiGe [11], [12].

In the near future, the gate electrode design of this 2×2 qauntum dot device could be updated to reduce the residual tunnel coupling. Speculatively, the electron wavefunctions are pushed toward the device center region which reduces the effectivity of the interdot barrier gates (B). Fig. 7.1 illustrates how a center gate (C) could be added to keep the electron wave functions below the corresponding plunger gates (P). Furthermore, in Fig. 7.1 the screening gates (S) are retracted providing an enlarged effective surface area for the plunger gates and reduced compression of the quantum dot array.

Next, a $N\times N = 3\times3$ array could be developed. It is the smallest square array with a quantum dot that has four nearest neighbors (the center dot). The array still could come with individual plunger and barrier gate control employing a design based on 3-5 gate layers. This would provide full flexibility in probing its properties before transitioning

to more scalable architectures that compromise on individual control. Si/SiGe devices with $N > 3$[1] could be based on shared gate control, for instance, a crossbar arrangement as proposed in ref [34] or presented for a germanium quantum well in chapter 4. Note that proposals of architectures based on sparse arrays and spin shuttling present an alternative (and complementary) path to the scaling of dense arrays [35]–[38].

In all material platforms, with growing array size the voltage tune-up by a human expert gets increasingly time-consuming. Chapter 4 outlined how the capacitive coupling of a quantum dot to its surrounding gate electrodes can help identify the corresponding quantum dot by monitoring charge transitions under small gate voltage changes. Also, a method based on image correlation was presented which eased the tracking of quantum dot hole occupation numbers. These methods were applied after manually tuning to a desired charge configuration. In the near future, they could be adapted and used already during the tuning process to support the human expert. They can also inspire the development of automatic tuning strategies for shared gate arrays. Generally, the field of automatic tuning methods for quantum dot arrays is growing rapidly [39]–[45] and has the potential to speed up spin qubit research. Also, with steadily improving device uniformity, the tuning should become easier, and simplified algorithms might be sufficient for initializing specific charge states and tunnel couplings.

In addition to increasing the array size N and co-developing tuning algorithms, techniques to perform in-array readout should be focused on. This is to maintain charge sensing in growing two-dimensional arrays as required for confirming the formation of quantum dots and characterizing them but also benefits spin readout down the road. In Ge/SiGe metallic gate electrodes can be diffused into the SiGe barrier to form an ohmic contact with the quantum well [46]. The footprint of such ohmic contacts is determined by the shape of the corresponding gate electrode and thus it might be possible to reduce it to the size of a single quantum dot. This then could allow for in-array placed charge sensors that do not consume more area than three regular quantum dots. Alternatively, gate-dispersive readout could be employed [47]. When a quantum dot is tuned close to a charge transition its quantum capacitance changes. This can be detected by connecting a close-by gate electrode to a tank circuit and probing the tank circuit resonance frequency by reflectometry eliminating the need for charge-sensing quantum dots.

7.2. THE ROLE OF UNIFORMITY

Fig. 2.4 in chapter 2 showed the distribution of required plunger gate voltages for singly occupied quantum dots across material platforms and highlighted the need for further material advancement. For instance, while the demonstration of a 4×4 quantum dot array in chapter 4 proofed that significant progress has been made in heterostructure development, the spread of the first hole addition voltages in Ge/SiGe needs to be reduced further to continue scaling the array size. Also, an increased chance of encountering spurious or malfunctioning quantum dots when enlarging the quantum dot count presents a challenge for tuning and operability. In chapter 5 and 6 a new method to improve electrical uniformity in quantum dot devices was presented. Applying this method to a shared gate array and aiming for a single hole per quantum dot would put the method

[1] These could also come with quantum dot arrangements different from a square lattice.

to the test and probe its potential for realizing large quantum dot arrays in disordered heterostructures.

Furthermore, there is room for advancing the stress-tuning method itself. The ramp times and stress times have not yet been optimized and the stress voltage is increased step-wise in constant steps $\Delta V_{\mathrm{stress}} \approx 10-50$ mV and without incorporating prior knowledge to find the optimal stress voltage. Therefore a significant portion of the total algorithm runtime is spent on sweeping voltages without having any measurable effect. Modeling the underlying physical process [48] could speed up the tuning by predicting the best next stress voltage. To fully automate the stress tuning also a reliable method to detect the last hole or electron state is required. It needs to be robust against varying tunnel couplings and a fluctuating contrast of charge transition features. For instance, such a method could build upon the image correlation technique presented in chapter 4 and perform cross-checks with single charge occupation voltages predicted by a physical model. Other detection schemes [40] or convolutional neural networks [39], [45] could be employed as well.

Note that Wolfe et al. [49] recently showed how threshold voltages of heterostructure field effect transistors can be manipulated via optical illumination with photon energies larger than the host semiconductor band gap. Over a range of at least 1 V, the resulting threshold voltage linearly depends on the gate voltage applied during the illumination. This positions the method as a promising alternative to increase gate voltage uniformity. Therefore, it would be insightful to apply it in a quantum dot array to probe its effect on required gate voltages.

Finally, a clear next step lies in testing the performance of spin qubits in a stress-tuned quantum dot array. Only spin qubits situated in a quiet noise environment and stable potential landscape allow for the implementation of high-fidelity operations. It has to be tested if the device stability is preserved under stress-tuning and if qubit performance metrics such as the coherence times and gate fidelities remain unaffected.

7.3. SPIN QUBITS IN TWO-DIMENSIONAL QUANTUM DOT ARRAYS

The development of two-dimensional quantum dot arrays is a precursor for demonstrating two-dimensional spin qubit arrays. A 2×2 spin qubit processor has already been shown in Ge/SiGe [9]. Also, the Si/SiGe 2×2 device structure studied in chapter 3 is designed for hosting spin qubits. It includes a cobalt micromagnet on top of the gate stack and the fanout of the screening gates comes in the form of co-planar waveguides [50] to optimize the transmission of microwave signals for electric dipole spin resonance (EDSR). Currently, spin control is put to test by Unseld et al. [51][2] by operating the device with a single electron in each quantum dot and utilizing Pauli spin blockade parity read-out and post-selection for initialization and read out [7]. Chevron patterns are obtained for all four electrons when a near-resonance EDSR pulse is applied as exemplary shown for quantum dot Q1 in Fig. 7.2.a. The Lamor frequencies of the four electron spins are distributed across a range of $\Delta f_{\mathrm{L}} \approx 309$ MHz and coherence T_2^* and Hahn echo coher-

[2] These experiments are performed in a different device than presented in chapter 3, chapter 5 section 5.10, or chapter 6 which however comes with the same gate electrode design to define the quantum dots.

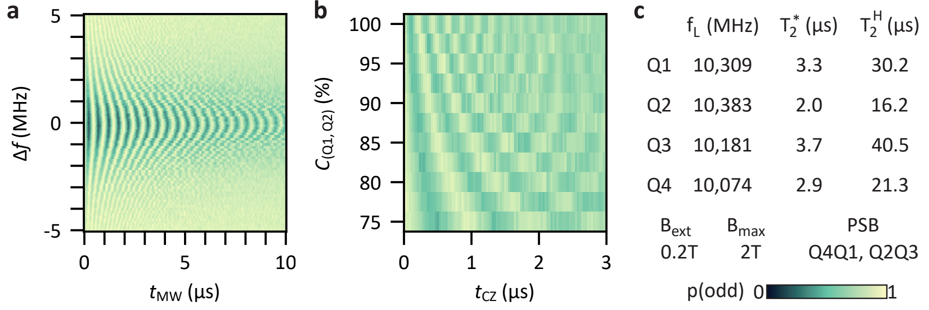

Figure 7.2: **Spin manipulation in the 2 × 2 array.** **a)** EDSR-driven Rabi oscillations of the spin in quantum dot Q1. A typical Chevron pattern is obtained as a function of pulse duration t_{MW} and the drive frequency detuning $\Delta f = f_{\mathrm{L}} - f_{\mathrm{MW}}$ where f_{L} is the qubit Lamor frequency and f_{MW} is the applied microwave signal frequency. The microwave pulse is applied to the lower screening gate labeled S23 in chapter 3. Initialization and readout are based on PSB parity readout and post-selection [7] on readout pair (Q4, Q1). **b)** Decoupled CZ gate [11] applied to Q1 and Q2 and as a function of interaction time t_{CZ} and coupling strength $C_{(\mathrm{Q1,Q2})} = (\mathrm{vB12} - \mathrm{vB12}_{\mathrm{min}})/(\mathrm{vB12}_{\mathrm{max}} - \mathrm{vB12}_{\mathrm{min}})$ with $\mathrm{vB12}_{\mathrm{min}}$ and $\mathrm{vB12}_{\mathrm{max}}$ barrier voltages corresponding to an exchange interaction of $f_{\mathrm{J}} \lesssim 20$ kHz and $f_{\mathrm{J}} \gtrsim 1$ MHz, respectively. The spins in Q1 and Q2 are initialized followed by a $\pi/2$ rotation around the x-axis of Q1 (noted as $\mathrm{X}_1(\pi/2)$). Then two adiabatic controlled phase gates of duration t_{CZ} interleaved by refocusing $\mathrm{X}_1(\pi)$ and $\mathrm{X}_2(\pi)$ pulses are applied. Finally, a $\mathrm{X}_1(\pi/2)$ and a $\mathrm{X}_2(\pi)$ pulse are followed by PSB readout on quantum dot pair (Q4, Q1). **c)** Table summarizing all four Lamor frequencies f_{L}, coherence times T_2^* and Hahn echo times T_2^{H} as well as providing the applied B-field B_{ext}, the maximum applied B-field to magnetize the micromagnet B_{max} and the quantum dot pairs used for PSB readout. The quantum dots and gate electrodes are named as in chapter 3. For instance, quantum dot Q1 is located at the upper right of the array. The device is tuned to the (1,1,1,1) charge state with one electron per quantum dot.

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ence T_2^{H} times lie between 2.0 and 3.7 μs and between 16.2 and 40.5 μs, respectively (see Fig. 7.2.c). The device allows for barrier control over all[3] two-qubit exchange interactions at the charge noise detuning sweetspot [30]–[32] as is demonstrated in Fig. 7.2.b by the example of a decoupled CZ gate [11] applied on quantum dots Q1 and Q2. In summary, these findings showcase the suitability of the 2 × 2 quantum dot array introduced in chapter 3 for the realization of a 2 × 2 spin qubit processor with individual qubit addressability.

To scale the size of two-dimensional spin qubit arrays in Si/SiGe beyond a few qubits, advanced magnet designs could be developed. Micrometer-scale magnets (micromagnets) can be optimized to reduce decoherence-inducing field gradients while providing sufficient addressability in one-dimensional arrays [7] or for small two-dimensional arrays [52]. While this approach cannot be scaled in two dimensions, a tailored pattern of nanometer-scale magnets (nanomagnets) could provide alternating qubit frequencies at reduced decoherence inducing field gradients [53]. For this approach, the length scale over which the qubit frequencies repeat should be chosen such that the effect of microwave crosstalk [54] is negligible.

It also might be worth exploring different mechanisms to drive single qubit rotations. Recently in a Ge/SiGe quantum processor, single qubit gates were demonstrated that rely on timed diabatic qubit transfers between two quantum dots with non-aligned

[3] (Q1, Q2), (Q2, Q3), (Q3, Q4), and (Q4, Q1)

quantization axes [38]. This approach comes with the advantage that all operations can be implemented at low frequencies (< 300 MHz) reducing requirements on control electronics and signal routing. Also, addressability in Lamor frequencies is not required anymore as long as the qubits come with alternating quantization axes.

It might be interesting to implement shuttling-based single qubit gates in Si/SiGe as well. As they do not require that individual qubits have different Lamor frequencies, they might alleviate requirements on magnet design. A two-dimensional array of horseshoe nanomagnets as already demonstrated in ref [53] could be placed on top of a two-dimensional quantum dot array. The quantum dots then would be positioned below the magnet geometric center and the magnet legs. At these locations, an increased field homogeneity is expected which reduces decoherence induced by charge noise. At the same time, the magnetic field direction would rotate by 90°C from quantum dot to quantum dot[4] providing 90°C angles between spin quantization and enabling shuttling-based single qubit gates. Alternatively, currents could be sent through superconducting gate electrodes to induce magnetic field gradients [34]. These gates would be arranged periodically, too, to obtain 90°C rotations in magnetic field direction from quantum dot to quantum dot.

To further scale the size of Ge/SiGe spin qubit arrays, it might be worth investigating how the spin-orbit interaction in quantum dots can be engineered, for instance through the shape of the the corresponding gate electrodes [55], [56] or through stress engineering [57]. Here the aim could be to reduce decoherence [58] while allowing for individual Lamor frequencies for EDSR control or while allowing for nonzero angles between the qubit quantization axes for shuttling-based single qubit gates [38].

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[4]in one direction of the array

The field of spin qubit quantum computing has made remarkable progress over the last years and there are no signs of stagnation. Other platforms, for instance relying on superconducting circuits [59] or ion traps [60] are progressing rapidly as well. While the road ahead of us is long, we are steadily getting closer to realizing a universal quantum computer. Certainly, some hard challenges remain but surely when Charles Babbage was working on the analytical machine in the 19th century [61] it was beyond his imagination that about 180 years later a chip significantly smaller than a single paper punch card[5] would fit a computer with gigabytes of flash memory.

[5]Charles Babbage considered paper cards with a pattern of holes to encode program operations for his analytical machines [62]. Punch cards were used extensively during the early development stages of computers [63].

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SUMMARY

The spin of a single electron or hole provides an attractive candidate for implementing a quantum bit when confined in a semiconductor quantum dot. Such a spin qubit is characterized by long coherence and short gate times. High-fidelity single and two-qubit operations have been demonstrated as well. Additionally, semiconductor quantum dots have a small footprint (≈ 100 nm × 100 nm) and their fabrication employs techniques similar to processes commonly used in modern semiconductor technology foundries. This promises the realization of dense qubit arrays, leverage through industrial fabrication, and direct co-integration with classical control circuits.

Thus far, one-dimensional quantum dot arrays have been studied extensively. Yet, only by realizing two-dimensional quantum dot arrays the small footprint of quantum dots is fully exploited. Also, due to their small size quantum dots are extremely sensitive to their local environment and fabrication imperfections. In current devices, an individually tailored set of gate electrode voltages is required for each quantum dot to confine a single charge. The limited space available for routing these voltages on the device, coupled with the associated overhead in required voltage sources, presents a challenge in scaling quantum dot arrays, especially two-dimensional arrays.

This thesis focuses on two-dimensional quantum dot arrays and gate voltage uniformity. The first part (chapter 3 and 4) reports the realization of two-dimensional quantum dot arrays in a silicon/silicon-germanium (Si/SiGe) and a germanium/silicon-germanium (Ge/SiGe) heterostructure. Afterward (chapter 5 and 6), a novel all-electric method is presented to achieve increased homogeneity of the required gate voltages.

In chapter 3 a 2 × 2 quantum dot array in a Si/SiGe heterostructure is presented. It is tuned to be occupied by a single electron per quantum dot reaching the (1,1,1,1) charge state. Dedicated barrier gate electrodes on the device allow for controlling the interdot tunnel couplings between neighboring quantum dots from about 30 μeV up to approximately 400 μeV as characterized through polarization line measurements.

In chapter 4 the focus is shifted towards a more scalable gate architecture for two-dimensional quantum dot arrays. It is inspired by random access architectures that are found in classical electronics. Specifically, a 4 × 4 quantum dot array in a Ge/SiGe heterostructure with shared gate electrode voltages is introduced. In this device, an odd charge occupancy is reached with either one or three holes in all 16 quantum dots simultaneously. Also, two shared barrier gate electrodes are placed between adjacent quantum dots. These enable selective control of the interdot tunnel coupling from less than 3 GHz to more than 10 GHz.

Spatial fluctuations in the electric background potential still limit the scalability of such a shared control array. Therefore, chapter 5 introduces a new method to increase the electrical uniformity in quantum dot devices. The presented method is based on applying stress voltages to the device gate electrodes. It enables the tuning of pinch-off voltages in quantum dot devices over hundreds of millivolts. Afterward, the new pinch-

off voltages remain stable for hours at least. The method is used to homogenize the pinch-off voltages of the plunger gates in a linear array designed for four quantum dots. It reduces their spread by one order of magnitude from 153 mV to 20 mV.

Motivated by this demonstration, in the experiment presented in chapter 6 the stress voltage tuning method is applied to control the plunger gate voltages required to reach single electron occupation in a quantum dot array. In a double quantum dot, a stable (1,1) charge state is reached at identical and predetermined plunger gate voltage and for various interdot couplings. Finally, by applying stress voltages a 2×2 quantum dot array is tuned such that the (1,1,1,1) charge state is reached when all plunger gates are set to 1 V.

SAMENVATTING

De spin van een enkel elektron of gat biedt een aantrekkelijke kandidaat voor de implementatie van een quantum bit wanneer deze wordt beperkt in een halfgeleider quantum dot. Zo'n spin qubit wordt gekenmerkt door lange coherentie- en korte rekenoperatietijden. Hoogwaardige enkele en twee-qubit rekenoperaties zijn ook gedemonstreerd. Bovendien hebben halfgeleider quantum dots een kleine voetafdruk ($\approx$ 100 nm $\times$ 100 nm) en hun fabricage maakt gebruik van technieken die vergelijkbaar zijn met processen die veel worden gebruikt in moderne halfgeleider-technologiefabrieken. Dit belooft de realisatie van dichte qubit arrays, industriële fabricage en directe co-integratie met klassieke besturingscircuits.

Tot nu toe zijn één-dimensionale quantum dot arrays uitgebreid bestudeerd. Maar pas door het realiseren van tweedimensionale quantum dot arrays wordt volledig gebruik gemaakt van de kleine voetafdruk van quantum dots. Bovendien zijn quantum dots vanwege hun kleine formaat uiterst gevoelig voor hun lokale omgeving en fabricageimperfecties. In huidige quantum chips is een individueel afgestemde set elektrodespanningen vereist voor elke quantum dot om een enkele lading te houden. De beperkte ruimte die beschikbaar is voor het routeren van deze spanningen op de chip, samen met de bijbehorende overhead aan benodigde spanningsbronnen, vormt een uitdaging bij het schalen van quantum dot arrays, vooral tweedimensionale arrays.

Dit proefschrift richt zich op tweedimensionale quantum dot arrays en uniformiteit van spanningen op de elektroden. Het eerste deel (hoofdstuk 3 en 4) rapporteert de realisatie van tweedimensionale quantum dot arrays in een silicium/silicium-germanium (Si/SiGe) en een germanium/silicium-germanium (Ge/SiGe) heterostructuur. Vervolgens (hoofdstuk 5 en 6), wordt een nieuw volledig elektrische methode gepresenteerd om een verhoogde homogeniteit van de vereiste spanningen te bereiken.

In hoofdstuk 3 wordt een 2×2 quantum dot array in een Si/SiGe-heterostructuur gepresenteerd. Het is afgestemd om bezet te worden door een enkel elektron per quantum dot, waarbij de (1,1,1,1) ladingstoestand wordt bereikt. Speciale barrière-elektroden op de chip maken de controle mogelijk van de interdot-tunnelkoppelingen tussen aangrenzende quantum dots van ongeveer 30 µeV tot ongeveer 400 µeV, zoals gekarakteriseerd door polarisatielijnmetingen.

In hoofdstuk 4 wordt de focus verlegd naar een meer schaalbare chiparchitectuur voor tweedimensionale quantum dot arrays. Deze is geïnspireerd door random-accessarchitecturen die worden gevonden in klassieke elektronica. Concreet wordt hier een 4×4 quantum dot array in een Ge/SiGe-heterostructuur met gedeelde elektrodespanningen geïntroduceerd. In dit apparaat wordt een oneven ladingstoestand bereikt met één of drie gaten in alle 16 quantum dots tegelijk. Ook worden twee gedeelde barrièreelektroden geplaatst tussen aangrenzende quantum dots. Deze maken selectieve controle van de interdot-tunnelkoppeling mogelijk van minder dan 3 GHz tot meer dan 10 GHz.

Ruimtelijke fluctuaties in het elektrische achtergrondpotentieel beperken nog steeds de schaalbaarheid van zo'n gedeelde controle-array. Daarom introduceert hoofdstuk 5 een nieuwe methode om de elektrische uniformiteit in quantum dot chips te verbeteren. De gepresenteerde methode is gebaseerd op het aanleggen van stress-spanningen op de elektroden van de chip. Dit maakt het afstemmen van pinch-off-spanningen in quantum dot chips mogelijk over honderden millivolts. Vervolgens blijven de nieuwe pinch-off-spanningen minstens enkele uren stabiel. De methode wordt gebruikt om de pinch-off-spanningen van de plunger-gates in een lineaire array ontworpen voor vier quantum dots te homogeniseren. Het vermindert hun spreiding met een orde van grootte van 153 mV tot 20 mV.

Gemotiveerd door deze demonstratie, wordt in het volgende hoofdstuk (hoofdstuk 6) de methode toegepast om de plunger-gate-spanningen te regelen die nodig zijn om enkel-elektron-occupatie te bereiken in een quantum dot array. In een dubbele quantum dot wordt een stabiele (1,1) ladingstoestand bereikt bij identieke en vooraf bepaalde plunger-gate-spanning en voor verschillende interdot-koppelingen. Ten slotte wordt door het toepassen van stressspanningen een 2×2 quantum dot array afgestemd, zodat de (1,1,1,1) ladingstoestand wordt bereikt wanneer 1 V wordt aangelegd aan alle plunger-gates.

DATA AVAILABILITY

The data and analysis scripts underlying chapters 2, 3, 4, 5, 6 are stored in public repositories. Table 7.1 provides an overview of all repositories.

Chapter	Repository
2	doi.org/10.5281/zenodo.10688909 and doi.org/10.4121/a4e3765b-9e32-492b-96fe-a9b760baef48.v2
3	doi.org/10.5281/zenodo.8226044
4	doi.org/10.5281/zenodo.8083119
5	doi.org/10.5281/zenodo.7746206
6	doi.org/10.5281/zenodo.10254611

Table 7.1: Overview of the data repositories containing the data and analysis scripts underlying this thesis.

Acknowledgements

Once I was asked about the best part of my PhD journey. The last four and a half years came with many highlights but I think the best part of my PhD were the people I got to know and work with.

Menno, I want to thank you first. As my promotor, you have guided me through my PhD studies with all the ups and downs involved. You were always generous and motivating. Your ability to generate ideas and identify interesting research directions is impressive, again and again. At the same time, you are a great mentor, always willing to provide advice and find constructive solutions in challenging situations. You make sure to provide a research environment coined by respect and acceptance and show care for every group member. My time in your group has influenced me strongly and let me grow as a scientist and person. I am deeply thankful for the opportunity to pursue a PhD in your group. From my first visit to QuTech until now I always have been convinced that it was the right decision to join your group. Thank you for your continued trust in me. I am sure your group will continue to flourish and that the new generations of group members have found an excellent promotor and mentor in you.

Lieven, in the 2D array project we worked together most closely. Thank you for pushing this inter-group collaboration and for always providing motivation as well as honest advice in difficult times. With your vast experience in the field of spin qubits and quantum computing, I am sincerely thankful for the countless times you provided feedback on our work. Also, QuTech can be proud to have you as a scientific director. I appreciate that you devote part of your directorship to scientific integrity, social safety, and the acceptance of failure. Thank you for being a driving force in the spin qubit groups, a caring research director, and for being my co-promotor.

Giordano, everyone working with spin qubit devices in Delft is very lucky to have you and your group. Without a good heterostructure, you don't get far in quantum dot and spin qubit research. Thank you for all the heterostructures you provided throughout my PhD. I also appreciate the multiple times you explained, without any haste, a material science aspect to me. You are an inspirational scientist.

Corentin and Cécile, thank you for standing by my side as my paranymphs on the day that I defend my dissertation.

Corentin, how we looked at a challenge often could not have been more different. That was great as we could complement and learn from each other. I deeply enjoyed working with you on the stress-tuning project and I am proud of what we achieved. Your motivation and dedication are contagious and there was also no shortage of laughing during our discussions. You taught me many things: project management, scientific writing, and managing the publication process, to name a few. Also, thank you for your emotional support and advice during tougher times. You are a great colleague! I wish you success with your endeavor to start your own research group. You deserve it and I am convinced you will be a great group leader.

Cécile, we did not work on a shared project during my PhD studies. Nevertheless, I enjoyed having you as a colleague. Especially, I remember our shared time at the silicon workshop in Japan. Exploring Kyoto with you and Chien-An was a highlight and so were our long conversations in the hotel at the end of the day. I told you about my future scientific plans and you shared your journey. I am really thankful for this. It helped me more than you might think. I admire your relaxed approach to life while you are doing amazing research at the same time. There is a lot one can learn from you.

Chien-An, you started your PhD journey shortly after me. During our first year, we spent some time measuring together. Working with you was fun. You are a very talented scientist. I think every future employer should fight for you. Nevertheless, you are humble and a team player. I always liked our conversations, especially on the way home after a group dinner or when leaving a party in Las Vegas early. I wish you all the best for finishing your dissertation and finding a new adventure.

Florian, when I joined QuTech, you were just about to finish your Master's thesis project. We shared an office on the first floor and you took me to Taekwondo which was really cool but unfortunately discontinued due to covid. When you began your PhD studies we started to share a project across the spin qubit groups. We experienced quite some struggles on the path to realizing a two-dimensional array in Si/SiGe, especially when looking for Pauli spin blockade. Yet, after measuring in four different fridges, dealing with a sudden helium crisis, and finding back some missing orders of magnitude we found a good device. It's great to see what you and Brennan achieved going from a 2x2 quantum dot array to a 2x2 spin qubit array. I wish you all the best with finishing your thesis and for your future journey.

Timo and Ilja, it was a pleasure to supervise you during your Master's end project. The teamwork with you and Corentin counts as one of the highlights of my PhD. You both were significantly pushing our stress voltage tuning project forward and brought in exciting new ideas.

Francesco, it was an honor to join your project on the 16 quantum dot crossbar device and it was joyful working with you. You possess strong endurance and have a clear vision for your research. After our discussions, I always walked away with new ideas.

Floor, you taught me that sometimes not following the rules is a good idea. I have to admit that I still need to practice that more. We shared the journey of writing our theses and jumping through the hoops the defense preparation comes with. Thanks, this made the process which can be stressful at times much more bearable. I wish you all the best for the final day of your PhD. Your research is impressive and I am sure you will have a great defense as well.

Luca, Nico, Gertjan, Will, Floor, Max, thank you for the warm welcome in the group when I started my PhD journey in 2019. I still remember our after-work trips to different bars in Delft.

Gertjan, I deeply appreciate the countless hours you took to train me in the cleanroom and to support me during the fabrication of my first samples. When covid hit, you even fabricated my devices as I was not allowed in the cleanroom anymore. Besides being a cleanroom mentor you also helped me to get started with my research. You always were in a good mood and your humor was a pleasant constant when working with you.

Will, thank you for checking in with me during my first weeks. You knew that moving

to a new country can be tough at the beginning and offered to listen and to share your story. Also, I feel honored to have been a guest of one of your famous shared flat parties before the pandemic hit.

Nico, I was always impressed by how efficiently you handled your research and by the breadth of your skills and knowledge. Thank you for regularly checking in when I was a young PhD student. I enjoyed our conversations and learned a lot from you.

Luca, I had the honor to look over your shoulder when you were taking the measurement for the hot qubits paper. I am fascinated by the precision and efficiency with which you follow your goals.

Max, we not only shared office B213 for a long time but also had a similar working rhythm. I believe that there was no one coming in or leaving later than us. We turned the night into our productive hours but also had some nice late-night chats. It was very exciting to follow your journey from postdoc to group leader. I am super happy for you that you made it and wish you all the best. Last but not least, thanks for the many times you took the time to explain a theoretical concept to me. I learned a lot from you.

Saurabh, thanks for the many times you went to the cleanroom to fabricate new samples for the 2D array project and the stress tuning project. The times we spent in the yellow hell together also were a pleasure. I especially enjoyed our training sessions at the dicer, the ones we never finished I believe ;).

Dave, thanks for the patience you showed when teaching us about the wild nature of charge traps in semiconductor devices. It was always fun to discuss our latest measurements and analysis together with Corentin, Saurabh, Timo, Ilja, Davide, and Mohamad. I am looking forward to hearing about your upcoming measurements once the cryo-prober is installed and fully running.

Sergey, you were a constant fellow throughout my entire PhD. Your fabrication knowledge and skills are truly impressive and so is your readiness to help newbies and more experienced users in the cleanroom.

Mateusz, thank you for supporting us during our initial measurements of the 2x2 device but also thanks for being a kitesurfing mentor. It was fun to exchange about the wind conditions, equipment, and learning progress.

Brian, thanks to you I did not end up under one of the countless bridges in Delft. You introduced me to your former shared flat and I took over your room when you decided to move to Den Haag. We had lots of interesting late-night chats, either in the office or when you picked up some mail that accidentally was delivered to our place.

Dingshan, together with Chien-An you first investigated stress voltage effects in germanium. With this, you paved the way for the measurements that made it into two chapters of this thesis. Thanks!

Valentin, our road trip through Nevada and Arizona after the APS March Meeting 2023 was an impressive experience, especially hiking into the Gran Canyon. Thanks for your patience with me as the driver and the support on the endless lanes on American highways. **Sasha**, your learning curve is steep and your scientific skills are impressive. Keep up your curiosity! **Hanifa**, you are not shy to fight for your research and yourself. Keep on going. I wish you the great results you deserve. **Job**, it was always fun to discuss your measurements. **Michael**, I liked our easy-going hallway chats. **Damien**, humor in science is important (see propositions) and you never missed a day to integrate it into

our work. **Dario**, all the best with your PhD! **Christian**, thanks for letting me join your project when covid hit and I could not go to the cleanroom anymore. **Jann**, even though your stay in our group was short it quickly felt like you were a longtime colleague.

Sander, thanks for the countless times you helped us when we faced a software or control hardware problem. Your contribution to the spin qubit group efforts is invaluable. Also, I enjoyed our chats about various topics during lunches, breaks, and group outings. **Marja**, thank you for providing advice and support from the first day of my PhD to the last. You always took the time to answer all my questions and helped with various problems. **Jason, Matt, and Olaf**, how would we run experiments without your support on the cryo systems? Thank you for your patience and for finding a solution to nearly every fridge problem we faced. **Raymond, Raymond, and Roy**, thank you for always providing new ideas and solutions when we faced challenges with the control electronics. I will also remember the ad-hoc lectures on electronics in your office. **Siebe**, thanks for your persistence with the winch installation in F016 and the opportunity to practice my Dutch at work. Also, I like to thank all the other support people at QuTech including **Aldo, Berend, Dennis, Erik B., Erik W., Hasan, Hitham, Jelle, Jenny, Nico, Pieter, Roy, Tom, and Vinod**. You make QuTech an incredible research environment.

Mohamad, thank you for the long and intense discussions on charge noise. I enjoyed them and gained new perspectives. **Grazia**, you are always spreading positive vibes. Thank you for promoting diversity and inclusion in QuTech. **Satish**, thank you for reaching out and simulating some of our 2D array devices. It was cool to see this project progressing.

Chien-An, Damien, Dave, Davide, Florian, Lieven, Max, Menno, thank you for proofreading this thesis. **Hendrik, Arne, Leo, Fabio, and Eliška** thank you for assessing my thesis and being on my PhD defense committee. **Jos**, thank you for being a reserve member.

I also would like to thank all the members of the Vandersypen, Scappucci, Rimbach-Russ, and Bosco group and all the colleagues from TNO. **Alberto, Alexandra, Amir, Asser, Brennan, Carles, Daniel, Dave, Davide C., Davide D., Delphine, Eline, Irene, Jacob, Jurgen, Karim, Karina, Larysa, Liza, Lucas, Luka, Maia, Maxim, Nienke, Önder, Oriol, Pablo, Rick, Saurabh, Sergey, Stefan, Stephan, Sugeiva, Tobias, Xiao, Xin, Yoram, and Yuta**, you all created the vibrant environment in the spin qubit groups that I enjoyed working in. I extend this thanks to all former members I had the chance to get to know including **Alice, Anne Marije, Brian, Guoji, Kostas, Jelmer, Kenji, Mario, Mateusz, Patrick, Sjaak, Stephan, Tobias, and Tzu-Kan**.

During the first year of my PhD I got the opportunity to organize the QuTech Uitje, which had to become the QuTech Thuisje (due to covid restrictions). Thank you **David, Hridya, Kian, Medina, and Sébastian**. It was a lot of fun to team up with you and organize this traditional happening in those special circumstances.

Also outside QuTech I received tremendous support from my family, my partner, friends, and flatmates. I deeply value the new friendships I made in the Netherlands during the last few years. Together with my flatmates you significantly contributed to making Delft my new home.

Alex, Max, Nick, Niek, Niels, Pablo, and Tycko, I always enjoyed the time we spent together. It recharged my batteries. Thank you for all the walks, bike rides, kite surf-

ing sessions, dinners, trips, and days spent together. I am also deeply thankful for your support from lending a drilling machine to listening to my worries and supporting me in stressful times. I hope that in the future we will stay in close touch. I would also like to thank my study friends. Cheers to **Andi, Bene, Caro, Christian, David, Freddy, Hannah, Jan-Peter, Malte, Marc, Maren, Michael, Miriam, Patrick, Paul, Sophia, Stefi, Tanja, and Thomas**. We don't see each other often but our friends group means a lot to me. A special shout-out to all my other friends outside the Netherlands including **Alex, Arne, Christian, Daniel M., Daniel P., Jan, Jonas, Justus, Maik, Marco, Martin, Rüdiger, Sascha, Simon, and Stephan**, it is great to have you in my life.

Nejc, Adeeb, Jón, Julius, Mosab, Laura, Clara, Gül, and Brooke, you have been my flatmates in Delft. I enjoyed always having someone around at home, especially during the covid period. Also, I found it cool how international our shared flat was. Thank you for the many chats in the kitchen, birthday cakes, and shared flat nights.

Last but not least I would like to thank my family and partner. **Mama, Papa, Melissa, Luisa**, egal was meine Pläne waren und egal wie weit weg sie mich führten, ihr standet immer hinter mir und habt mich in allem unterstützt. Danke, dass ihr für mich da seid. **Bodo**, du hast mich vom Bewerbungsprozess bis zur Verteidigung durch meinen ganzen PhD begleitet. Es ist unglaublich schön dich als Partner an meiner Seite zu haben und als dein Partner an deiner Seite sein zu dürfen. Danke, dass du immer für mich da bist und mich in allen meinen Vorhaben unterstützt.

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(Netherlands)

Thesis:	*Electrostatic uniformity and two-dimensional quantum dot arrays in silicon and germanium*
Promotor:	Dr. M. Veldhorst
Co-Promotor:	Prof. dr. L.M.K. Vandersypen

List of Publications

6. D. Degli Esposti, L. E. A. Stehouwer, Ö. Gül, N. Samkharadze, C. Déprez, **M. Meyer**, I. N. Meijer, L. Tryputen, S. Karwal, M. Botifoll, J. Arbiol, S. V. Amitonov, L. M. K. Vandersypen, A. Sammak, M. Veldhorst, G. Scappucci *Low disorder and high valley splitting in silicon* npj Quantum Information, **10**, 32 (2024).

5. F. Borsoi, N. W. Hendrickx, V. John, **M. Meyer**, S. Motz, F. van Riggelen, A. Sammak, S. L. de Snoo, G. Scappucci, M. Veldhorst, *Shared control of a 16 semiconductor quantum dot crossbar array*, Nature Nanotechnology, **19**, 21–27 (2024).

4. **M. Meyer**, C. Déprez, I. N. Meijer, F. K. Unseld, S. Karwal, A. Sammak, G. Scappucci, L. M. K. Vandersypen, M. Veldhorst, *Single-electron occupation in quantum dot arrays at selectable plunger gate voltage*, Nano Letters, **23** (24), 11593–11600 (2023).

3. F. K. Unseld*, **M. Meyer***, M. T. Mądzik, F. Borsoi, S. L. De Snoo, S. V. Amitonov, A. Sammak, G. Scappucci, M. Veldhorst, L. M. K. Vandersypen, *A 2D quantum dot array in planar* ^{28}*Si/SiGe*, Applied Physics Letters, **123**, 084002 (2023).

2. **M. Meyer**, C. Déprez, T. R. van Abswoude, I. N. Meijer, D. Liu, C. Wang, S. Karwal, S. Oosterhout, F. Borsoi, A. Sammak, N. W. Hendrickx, G. Scappucci, M. Veldhorst, *Electrical control of uniformity in quantum dot devices*, Nano Letters, **23** (7), 2522–2529 (2023).

1. P. Puschnig, A. D. Boese, M. Willenbockel, **M. Meyer**, D. Lüftner, E. M. Reinisch, T. Ules, G. Koller, S. Soubatch, M. G. Ramsey, and F. S. Tautz, *Energy Ordering of Molecular Orbitals*, The Journal of Physical Chemestry Letters, **8** (1), 208-213 (2016).

* equal contribution