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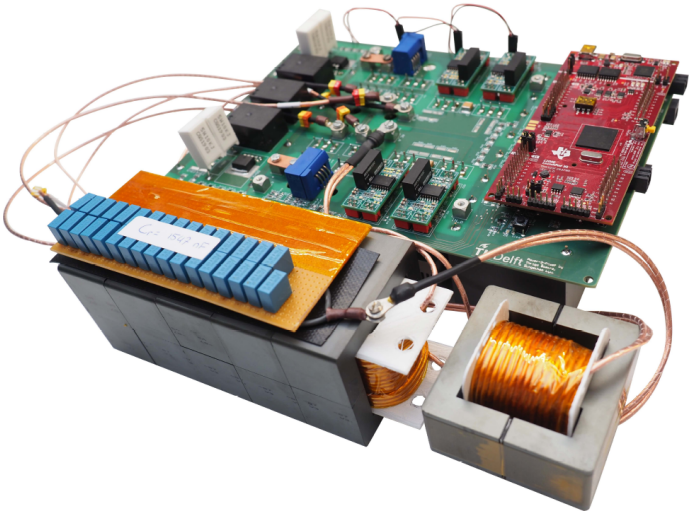

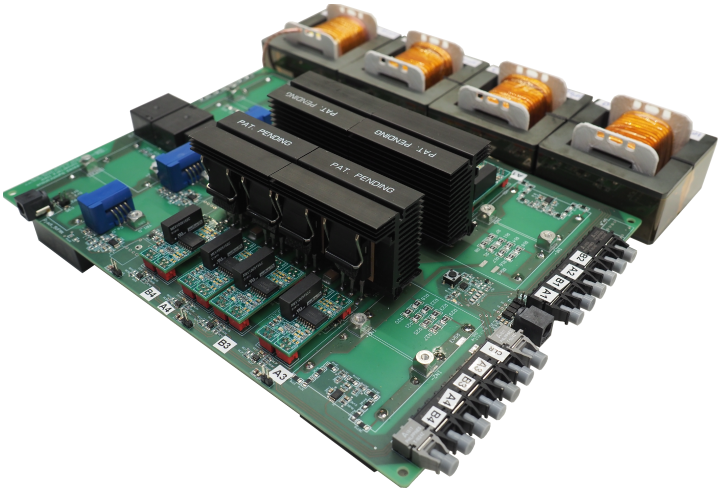

TU Delft

Design of an 11kW DC-DC Resonant Converter for EV Charging with a 150-1000V Output Voltage Range

by

Bram Oude Aarninkhof

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Whether you think you can,
or you think you can't
- you are right.

Henry Ford

CONTENTS

ACRONYMS

PWM Pulse Width Modulation
EV Electric Vehicle
RPC Resonant Power Converter
CSN Controlled Switch Network
SR Series Resonant
PR Parallel Resonant
NR Notch Resonant
CC Current Conditioning
RTN Resonant Tank Network
ZVS Zero Voltage Switching
RMS Root Mean Squared
ZCS Zero Current Switching
PFM Pulse Frequency Modulation
WBG Wide Band Gap
FHA Fundamental Harmonic Analysis
HB Half-Bridge
FB Full-Bridge
DAB Dual Active Bridge
SOC State of Charge
RFM Resonant Frequency Modulation
CCM Continous Conduction Mode
DCM Discontinuous Conduction Mode
TCM Triangular Current Mode
BCM Boundary Conduction Mode
PSM Phase Shift Modulation
SSPWM Secondary Side Pulse Width Modulation
SSPSM Secondary Side Phase Shift Modulation
PCB Printed Circuit Board

VD Voltage Doubler

CD Current Doubler

ICE Internal Combustion Engine

SDS Sustainable Development Scenario

PSFB Phase Shifted Full Bridge

KCL Kirchoffs Current Law

KVL Kirchoffs Voltage Law

DSP Digital Signal Processor

SUMMARY

The worldwide adoption of Electric Vehicles (EV) has gained momentum in recent years, with more than 30% of all EVs being sold last year. Additionally, a new trend of 800 V battery architectures has appeared to allow for faster charging than the now common 400 V architectures. Future proof charging topologies should, therefore, be able to provide a wide output voltage range. This study investigates how DC-DC resonant power converters can be employed to achieve a wide output voltage range of 150-1000 V for EV charging. After the literature study, a two-stage topology consisting of a LLC converter and Interleaved TCM Buck converter is selected for this purpose. Additionally, the competitiveness of an IGBT based solution is examined in comparison with a SiC MOSFET based solution. An analytical model is created in MATLAB and verified using LTSpice, after which different configurations of the 11 kW two-stage converter are compared analytically. This comparison is performed by developing a method to assess the efficiency of a converter based on real-world Charging cycles. A trade-off is made between efficiency and costs. In the end, one stage is equipped with IGBTs in the final design. After this, a PCB is designed and used to implement the prototype of the final design. The analytical and simulation models are verified experimentally using the prototype. The maximum measured efficiency of the converter is 97.66%, with a 95+% efficiency over the complete 150-1000 V range at full power. The obtained efficiency for the 11 kW-400 V Charging cycle is 96.85% and 95.67% for the 11 kW-800 V Charging cycle. The proposed converter in this study thus proves to be a highly efficient charging solution that is capable of charging existing, and future Electric Vehicles.

ACKNOWLEDGEMENTS

During my thesis, I had the privilege to receive the support of some absolutely wonderful people. These people have been of vital importance during the whole process of this thesis.

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My academic journey would not have remotely been possible without my parents and brother, who always inspired me to do the best I can. They provided me with unconditional support and always had my back throughout my entire education and in the years before that. A special thanks to my grandparents as well, who continue to believe in me as a person and engineer. Not to mention the rest of my family, who have always supported me.

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Hasta la vista!

Bram Oude Aarninkhof
Delft, August 2021

1

INTRODUCTION

The electrification of the world's transportation fleet has gained momentum in recent years. This trend is accompanied by an increasing demand in Electric Vehicle (EV) chargers. EV-chargers will become an essential part of the electricity grid, signifying the need of efficient charging solutions. In this study an 11 kW EV charger with a wide output voltage range based on a resonant power converter topology will be developed.

1.1. BACKGROUND / RELEVANCE

EVs are becoming more and more dominant in the transportation sector: more than ten million EVs were on the road at the end of 2020 (see Figure 1.1). Of these EVs, three million were sold in 2020 alone (4.6% of the total car sales) [1]. This shift to EVs is all in light of a global effort to reduce Global Greenhouse Gas (GHG) emissions [2]. Moreover, with the EU Commission recently proposing what is effectively a ban on new Internal Combustion Engine (ICE) car sales by 2035 [3], the shift to EVs is inevitable. In fact, car manufacturers are already responding to this transition from ICE cars to EVs: the number of available EV models is set to triple in 2021 when compared to late 2019 [4].

As a consequence, the demand for EV chargers to accommodate all these EVs will increase correspondingly. According to the Sustainable Development Scenario (SDS), 6% of the electricity consumption in the European Union in 2030 will come from EV charging, compared to 0.2% in 2019 [1]. The installation of publicly available chargers rises fast, with 45% of new chargers being installed in 2020. However, one of the main drawbacks of EVs is the relatively long charging time required compared to ICE vehicles' refuelling time [5]. Fast charging a battery pack is possible through charging with a relatively high current rate. However, this method decreases the lifetime of the battery pack [6]. Most EVs currently produced use a battery pack with a nominal voltage of 400 V [7]. However, in recent years some models, listed in Table 1.1, have been announced that use a higher voltage battery architecture [8–11].

This higher battery voltage can be one of the solutions for a faster charging time of EVs [7, 12]. A simplified example: a 400 V battery charging at 30 A charges with 12 kW,

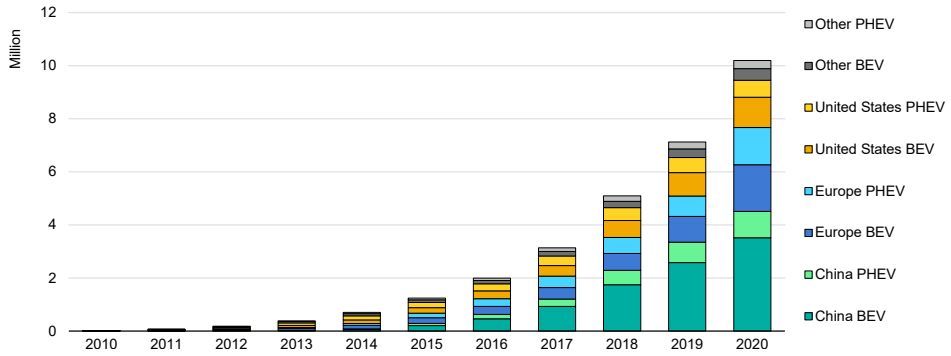


Figure 1.1: History of the Global Electric Vehicle stock between 2010 and 2020. Figure taken from the IEA [1], all rights reserved.

Table 1.1: List of recent Electric Vehicles which employ high voltage batteries.

First Delivery Year	Manufacturer	Type	Battery Voltage (V)	Source
2019	Porsche	Taycan	800 V	[8]
2020	Aston Martin	Rapide E	800 V	[9]
2021	Lucid Motors	Lucid Air	924 V	[10]
2021	Hyundai	IONIQ 5	800 V	[11]

while a 800 V battery charging at the same current of 30 A charges at double the power (24 kW). This allows for faster charging times without compromising the lifetime of the battery that would occur with increasing the charging current to increase the charging power. However, the introduction of these higher voltage battery architectures imposes a challenge on EV chargers: they need to be able of both accommodating the (common) 400 V battery architecture as well as the new high voltage battery architectures. The current study aims to design a resonant power converter capable of a wide output voltage range to meet this challenge. This wide output voltage range is particularly challenging for resonant power converters, as will be discussed in Chapter 2.

1.2. DESIGN CONSTRAINTS AND REQUIREMENTS

1.2.1. REQUIREMENTS FROM THE RESEARCH GROUP

The topology used for the EV charger in the current study is fixed to a resonant power converter topology. The current study is part of a PhD project regarding a multiport charger. This multiport charger consists of multiple 'blocks', and two topologies have already been studied for this application: the Phase Shifted Full Bridge (PSFB) and the Dual Active Bridge (DAB). The resonant power converter that is the subject of this study is the final topology to be compared for this multiport charger. Because the current study is part of this larger project, there are already some requirements on the parameters of this charger in order to make a fair comparison, listed in Table 1.2.

Table 1.2: Constraints posed by the research group.

Parameter	Symbol	Value
Topology	-	Resonant Power converter
Input voltage range	V_{in}	640-840 V
Output voltage range	V_{out}	150-1000 V
Maximum output power	$P_{o,max}$	11 kW
Maximum output current	$I_{o,max}$	30 A

The maximum output current of the converter in the current study is derived from the maximum output current of existing charging solutions, like the Terra DC wallbox from ABB [13]: it has a maximum charging current of 60 A for a 22 kW charger, thus for an 11 kW charger it would be scaled to 30 A. It is important to note that the input voltage V_{in} is not a degree of freedom for the design, but rather a constraint: the exact value of input voltage in the range of 640-840 V (see Table 1.2) cannot be freely chosen, but is dependent on the State of Charge (SOC) of the stationary battery pack. The input side of the converter is designed to be connected to a large stationary battery pack, thus the input voltage is dependent on the instantaneous voltage of this stationary battery pack.

1.2.2. ELECTRIC VEHICLE CHARGING STANDARDS

The International Electrotechnical Commission (IEC) has formulated a range of standards regarding a DC charging station in standard IEC-61851. This is a broad standard, ranging from cable specifications to communication methods and EMC requirements. Some requirements from the DC charging station standard IEC-61851-23:2014 are used in this study (see Table 1.3)[14]. This standard applies to an EV charging station that uses a conductive method to charge an EV with DC power using a maximum input voltage of 1500 V.

Table 1.3: Design requirements posed by IEC61851-23:2014 taken into account in this study [14].

Parameter	Symbol	Value
Maximum peak-to-peak output current ripple during CC phase	$\Delta I_{o,max}$	9 A
Maximum peak-to-peak output voltage ripple during CV phase	$\Delta V_{o,max}$	10 V
Operating temperature range	$T_{ambient}$	−5-40 °C

1.3. RESEARCH QUESTIONS

The aim of the current study is to design an 11 kW EV charger with a wide output voltage range based on a resonant power converter topology. This objective will be obtained by answering the following research questions:

- Which resonant power converter topologies and modulation methods are best suited for a wide output voltage range application?
- How to devise, implement and verify a multi-objective design procedure based on efficiency and cost of different design solutions?
- How does the chosen topology equipped with IGBTs compare to SiC MOSFETs with regards to efficiency?

1.4. THESIS OUTLINE

The thesis outline is provided below on a chapter-by-chapter basis.

- Chapter 2: The literature study, where suitable options for a wide output voltage range resonant power converter are explored. After this, existing resonant power converter topologies for EV charging will be compared. This results in the selection of a particular topology to be used in this study. The first research question is answered after this chapter.
- Chapter 3: The analytical model of the chosen converter is explained and verified by simulation.
- Chapter 4: A procedure for comparing the different configurations of the chosen converter (switch type and switch voltage rating) is outlined.
- Chapter 5: The procedure outlined in the previous chapter is used to assess the performance of different configurations of the selected resonant power converter topology. The best configuration is chosen as the final design.
- Chapter 6: Different component are selected for the prototype design based on the parameters from the final design in Chapter 5 and the analytical model in Chapter 3.
- Chapter 7: Outlines the main design choices for the Printed Circuit Board (PCB) design.
- Chapter 8: The procedure for testing the prototype in the lab is described. The results from the performance of the prototype in the lab are shown and interpreted.
- Chapter 9: Provides conclusions of the current study, including its implications, limitations and recommendations for future work.
- Appendix A: Contains the method of determining the losses of the semiconductor devices used in the current study.
- Appendix B: Regarding the implementation of an external transformer and inductor design script used in this study.
- Appendix C: Contains all literature sources found during the quantitative part of the literature study in Chapter 2.
- Appendix D: Provides additional experimental results not discussed in Chapter 8.
- Appendix E: Shows the difference in efficiency when half of the Interleaved Triangular Current Mode (TCM) Buck converter is used compared to when the full converter is used.

2

LITERATURE STUDY

As posed in one of the research questions in Section 1.3, a solution for a Resonant Power Converter (RPC) used for EV charging has to be conceived. The application of EV charging brings certain requirements to the RPCs:

- The converter has to operate in a wide output voltage (V_o) range at different output power (P_o) due to: firstly, the varying voltage versus SOC of Lithium-Ion battery charging [15, 16] and secondly, the different battery pack architectures as discussed in Section 2.1.
- The converter should have as high as possible efficiency due to the scale at which EV chargers will be implemented in the near future, as mentioned in Section 1.1.

2.1. RESONANT CONVERTERS

Resonant soft-switching converters can be classified into several subcategories: resonant-transition, multi-resonant, quasi-resonant and RPC. The current study focuses on RPCs because of their high efficiency and power density [17].

RPCs exhibit advantages over the traditional Pulse Width Modulation (PWM) DC-DC converters such as [15]:

- Reduced switching losses due to possibilities of Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) switching.
- Increased operating frequency due to the soft switching, which reduces the size of the passive components and thereby allows for an increase in power density
- Lower EMI emissions due to ZVS and sinusoidal drawn waveforms.

The general structure of a RPC, based on the terminology of Outeiro et al. (2016) [17] is illustrated in Figure 2.1.

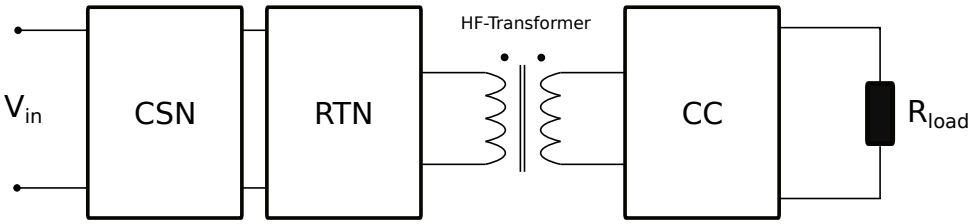


Figure 2.1: General structure of a Resonant Power Converter, based on [18].

The segments of the structure in Figure 2.1 are explained as follows:

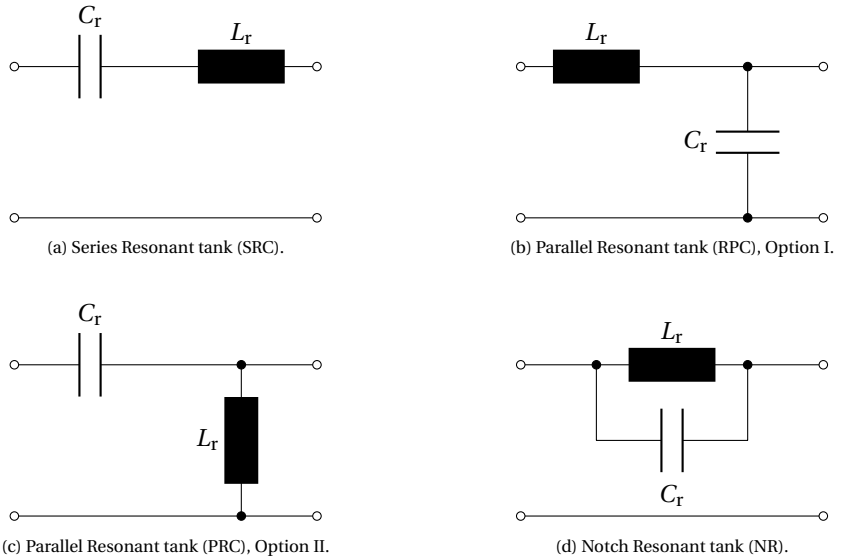
- **Input**: In this case, the input source is a DC voltage source with V_{in} = 640-840 V, as specified in Section 1.2.1.
- **Controlled Switch Network (CSN)**: The Controlled Switching Network, which can be implemented by any topology that outputs a high frequency AC voltage waveform. For example, a Half-Bridge (HB) or a Full-Bridge (FB).
- **Resonant Tank Network (RTN)**: The RTN consists of a combination of capacitive and inductive elements in series or parallel, or a combination of both. The RTN elements shape the frequency response of the resonant power converter. Besides this, the RTN also enables the soft-switching of the CSN switches.
- **HF-Transformer**: The high frequency transformer provides galvanic isolation between the input and output side of the converter. At the same time it allows for a fixed step-up or step-down of the voltage through the turns-ratio.
- **Current Conditioning (CC)**: Rectifier and output filter. The filter is, in this case, a DC-link capacitor bank to provide a constant V_o output.
- **Output**: Load resistor representing the EV.

2.2. THREE BASIC RESONANT TANK NETWORKS

The RTN determines the frequency response of the RPC, as stated before in Section 2.1. The order of the RTN is a term used for the number of capacitive and inductive elements of the RTN. For resonance to occur, one needs at least one capacitive and one inductive element. There are three basic types of second-order RTNs: the Series Resonant (SR) tank, the Parallel Resonant (PR) tank and the Notch Resonant (NR) tank. All three basic types of RTNs are shown in Figure 2.2. Each higher-order RTN consists of a combination of these three second-order types, combining the characteristics of each type. The amount of possible configurations increases when considering more reactive elements in the RTN [19]. Several parameters that are used frequently in RPCs are:

- **Characteristic Impedance** (Z_0): This depends on the ratio between the resonant capacitive- and inductive elements of the resonant converter.
- **Quality Factor** (Q_L): The ratio between the impedance of the RTN and the load resistance R_L.
- **Normalized switching frequency**: Either expressed as ω/ω_r or f/f_r, is the converter's switching frequency relative to the resonant frequency. There are multiple

f_r in case of a higher-order RTN. Which resonant frequency is used in this expression has to be indicated specifically for the type of RTN.



(a) Series Resonant tank (SRC).

(b) Parallel Resonant tank (RPC), Option I.

(c) Parallel Resonant tank (PRC), Option II.

(d) Notch Resonant tank (NR).

Figure 2.2: The three basic types of second-order RTNs, there are two options for the PRC RTN (see Figures 2.2b and 2.2c)

The voltage gain of the RTN obtained using AC analysis for the different basic building blocks is shown in Equations (2.1) to (2.3). By varying the load resistance R_L (and thereby Q_L) and the normalized switching frequency of the CSN, a 3D voltage gain plot can be created for each basic building block. This plot is shown in Figure 2.3.

$$|M_{v,SRC}| = \frac{1}{\sqrt{\frac{1}{1+Q_L^2\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)^2}}} \tag{2.1}$$

$$|M_{v,PRC}| = \frac{1}{\sqrt{(1-\frac{\omega}{\omega_0})^2+\left(\frac{\left(\frac{\omega}{\omega_0}\right)}{Q_L}\right)^2}} \tag{2.2}$$

$$|M_{v,NRC}| = \frac{1}{\sqrt{1-\left(\frac{Q_L}{\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)}\right)^2}} \tag{2.3}$$

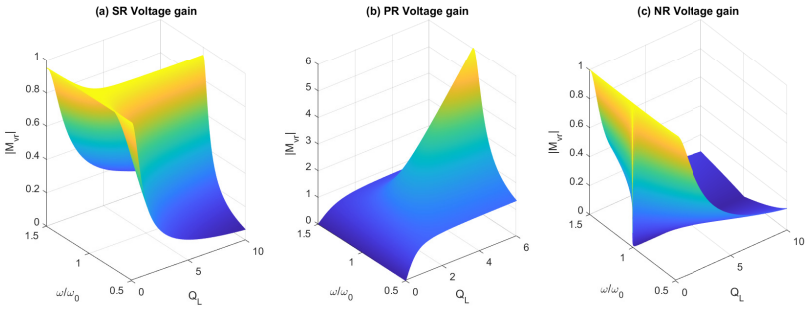


Figure 2.3: Normalized gain plot for all three basic resonant tanks. All the normalized gains are plotted against varying Q_L and ω/ω_0.

2.3. COMPARISON OF RESONANT TANK NETWORK CONFIGURATIONS

One aim of this literature study is to find a suitable RTN configuration for the proposed EV charging application. Several comparative studies have been conducted regarding configurations of the RTN, all using Pulse Frequency Modulation (PFM) as a method to control the output voltage [15, 19–21]. One study compared the performance of the following RTNs for EV charging: SRC, PRC, LCC and LLC [15]. Another study compared the performance of two higher-order variations of the LLC converter in EV charger application: the CLLC and CLLLC converter [20]. Finally, one other source compared the SRC, PRC, LLC, LCC and CLL converter [19]. As will be shown in Section 2.4, these are the most common tank configurations used in RPCs for EV charging. A comparison table based on these studies is listed in Table 2.1. A schematic of each of the six RTNs listed in Table 2.1 is given in Figure 2.4. Note that none of these RTNs contain any form of NR element: these converters require complex control circuitry due to the shape of the gain associated with a NR element (see Figure 2.3) [19].

Table 2.1: Comparison of the performance of different Resonant Tank Network configurations, based on [15, 19–21]. A schematic of each of these RTNs is given in Figure 2.4.

	SRC	**PRC**	**LCC**	**LLC**	**CLL**	**CLLC**	**CLLLC**
Switching frequency range	Widest	Narrow	Narrow	Moderate	Moderate	Moderate	Moderate
Primary Side ZVS	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Secondary Side ZCS	No	No	No	Yes	Yes	Yes	Yes
Voltage/Current stresses on components	Least	High	Most	Low	High	Moderate	Moderate
Bidirectional Operation	-	Worst	-	Poor	Poor	Good	Best
Start-Up performance	Poor	Worst	Poor	Poor	Better	Poor	Best
Control Complexity	High	High	Moderate	Moderate	Moderate	High	Moderate

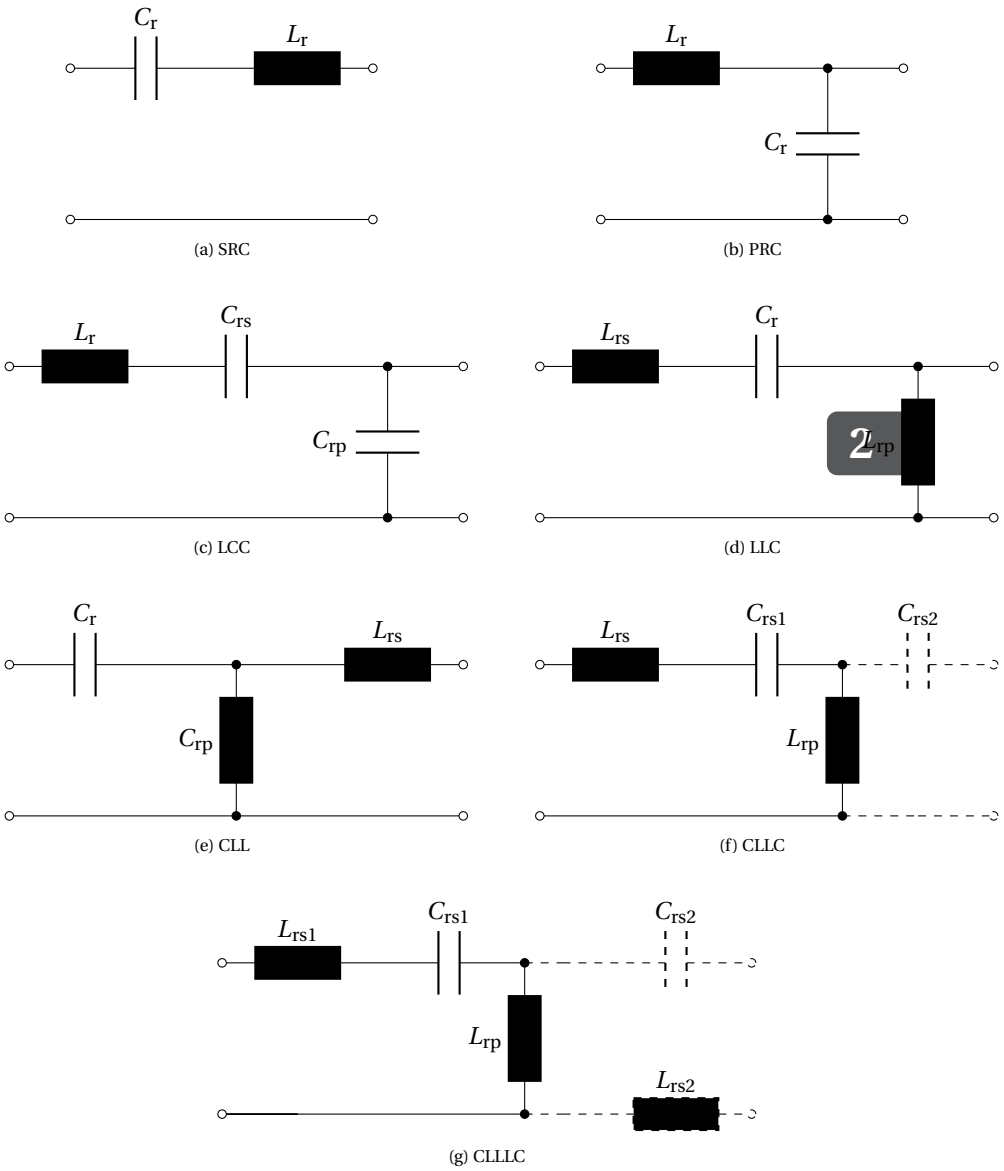


Figure 2.4: The six Resonant Tank Networks mentioned in Table 2.1. The dashed lines in Figures 2.4f and 2.4g mean that the components are located on the secondary side of the HF-transformer. Subscript $(_s)$ stands for series, while $(_p)$ stands for parallel.

Subsequently, some of the judgments made in the comparison of Table 2.1 are elaborated below.

Starting with the SRC RTN. It has poor load regulation under light loads: a large f_{sw} variation is needed for a change in gain [15]. The PRC has the disadvantage of comparatively large circulating currents in the RTN compared to the load current [17].

The next point is regarding the start-up performance of all converters. Most RPCs experience a large surge current during start-up [20]. This surge current occurs because the DC-link capacitance temporarily shorts the magnetizing inductance during start-up of the converter. However, the CLLC and CLLLC do not experience this since there is an inductor and a capacitor in the secondary side. The DC-link capacitance does not short the magnetizing inductance anymore, and therefore the tank impedance remains inductive. Meaning that even during start-up ZVS can be achieved [20].

In addition, the CLLC and CLLLC converters have another advantage over the LLC converter: the gain curve of the first two converters provides both boost/buck behaviour during both G2V as V2G operation [20]. The LLC converter, though, has no boost capabilities when used in V2G operation, thereby having an asymmetric gain [21, 22]. However, the downsides of having a higher-order RTN such as the CLLC and CLLLC are: the increased losses over all these additional resonant elements and a more complex design process [18, 20]. A downside of designing a bidirectional RPC is that the rectifier diodes used on a unidirectional RPC have to be replaced by switches (also known as Synchronous Rectification). This increases costs but decreases the conduction losses. However, the control becomes more complex due to additional control required to time the rectification switches. While the diodes did not require any control at all [23].

Finally, benefits of the LLC converter are highlighted. It integrates both the magnetizing inductance and the leakage inductance of the transformer as an resonant element. Adjusting the magnetizing inductance to the required value can be done by varying the length of a small airgap in the transformer. However, this causes additional winding losses due to the fringing effect in the airgap. The CLL converter uses a dedicated inductor for this, reducing the losses in the transformer. Nonetheless, an additional component has to be used, decreasing power density [24]. The LCC topology has comparable characteristics to the LLC converter. It differs, however, in that it requires two resonant capacitors instead of one, making it more expensive [17].

Summarizing the comparison, leads to the decision that of all the options listed in Table 2.1, the LLC converter seems to be the best. However, the LLC's performance is inferior to the higher order CLLC and CLLLC converters on the aspect of bidirectionality. The important assumption here is that the converters are controlled using PFM to adjust the gain. The LLC has, overall, the lowest design and control complexity compared to these higher-order converters. The LLC converter also offers the advantage of integration of the required inductances in the transformer, only requiring an external resonant capacitor in theory. Additionally, it can achieve a wide operation region that allows for ZVS of the primary side switches, and ZCS for the secondary side rectifier.

Besides the RTNs discussed above and in Table 2.1 there is a range of other possibilities. There are an overwhelming amount of other possible RTN configurations: there exist 182 possible configurations for the fourth-order RTN alone [25]. A selection method-

ology of the RTN for a particular application from this wide range of configurations is proposed by Huang et al. (2011) [26]. Multiple sources conclude that the performance of a higher-order RTN is superior when compared to lower-order RTNs [18, 27]. However, the analysis of those higher-order RTN configurations also becomes increasingly complex [18]. Two directions can be taken at this point of the literature study:

1. Devise a (new) RTN configuration capable of achieving a wide output voltage range, using the selection procedure outlined by Huang et al. (2011) [26].
2. Choose the optimal RTN currently known from literature (based on [15, 19–21]), and devise a new strategy based on either different modifications to the topology except for the RTN, or a control strategy to achieve the wide output voltage range.

One of the research directions mentioned above comes with a few disadvantages. It would require extensive analytical modeling of different possible new RTN candidates based on the selection procedure from [26]. Furthermore, this modelling becomes increasingly complex at higher-order RTNs. On top of this, the amount of literature available for this direction would be less, further complicating this direction. Therefore, the second direction is deemed the best option, especially for the time frame of the current study. Thus the **LLC converter** is chosen as the topology for this study.

2.4. QUANTITATIVE EVALUATION OF LITERATURE

A quantitative study is done in existing literature to get a clear outlook on the state-of-art of RPCs in EV charging. An overview of all studies conducted in the past decade (2010-2021) is created regarding RPCs and EV charging. This is done using the search terms listed in Table 2.2 during the end of 2020 using the IEEExplore database.

Table 2.2: The search terms used during this literature review are shown in this table. An asterisk (*) means that several word variations are included. For example, charg* includes both 'charger' and 'chargers'. NOT means that the search term should exclude literature with these terms in the title.

Search Term	Used on
EV charg* review NOT wireless	12-11-2020
Resonant power converter EV charg* NOT wireless NOT Inductive	12-11-2020
'Resonant power converter' battery charg* NOT wireless NOT photovoltai*	23-11-2020
Two stage resonant converter NOT quasi NOT wireless NOT single*	01-12-2020
Resonant power converter notch	01-12-2020
Resonant battery charger NOT inductive NOT wireless NOT controller*	02-12-2020

A total number of 101 studies were found. The type of RTN in each study is listed in Table 2.3. This table shows that it was found that the LLC RTN is the most used, followed by the SRC RTN and the bidirectional variation of the LLC RTN: the CLLC converter.

Table 2.3: Number of studies found for each resonant power converter topology applied to EV-charging or battery charging, in descending order. Results fell into five major topologies: the LLC, SRC, CLLC, CLLLC and CLL converter. The CLLC and CLLLC are designed for bidirectional power flow so G2V as well as V2G.

Topology	Amount of studies
LLC	57
SRC	17
CLLC	14
CLLLC	6
CLL	3
PRC	2
CLC	1
CLLL	1

The four datapoints, listed in bulletpoints below, are extracted from each of these 101 studies and compiled into Figures 2.5 to 2.8. It is important to note that not all studies listed all types of data. This results in a different number of studies per figure (for Figures 2.5 to 2.8). Only the references of specific studies discussed in this section are used in the bibliography. See Appendix C for all other references and a complete overview of the collected data.

- Maximum efficiency (Figure 2.5)
- Power density (Figure 2.6)
- Type of switch used (MOSFET/IGBT) (Figure 2.7)
- Output voltage range (Figure 2.8)

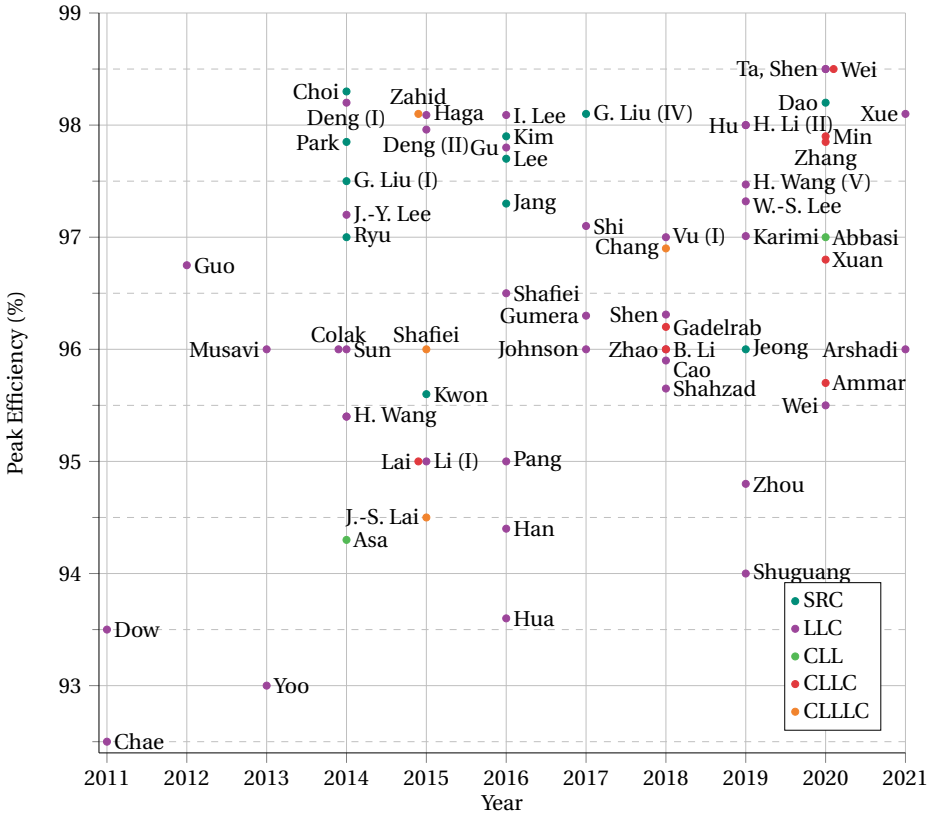


Figure 2.5: All studies that reported their η_{max}, the name of each study is next to the dot (by default on the right, if not obstructed by another name). See Appendix C for an overview of all references.

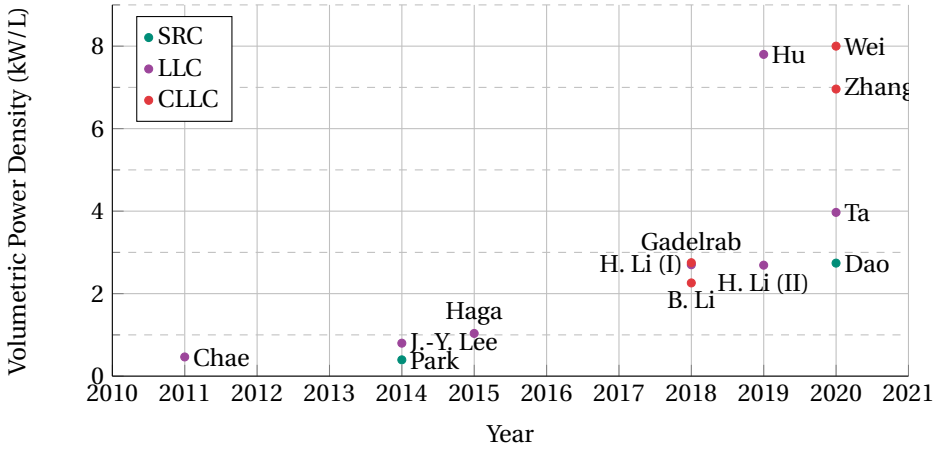


Figure 2.6: Volumetric power density as reported by the literature studies from Table 2.3. See Appendix C for an overview of all references.

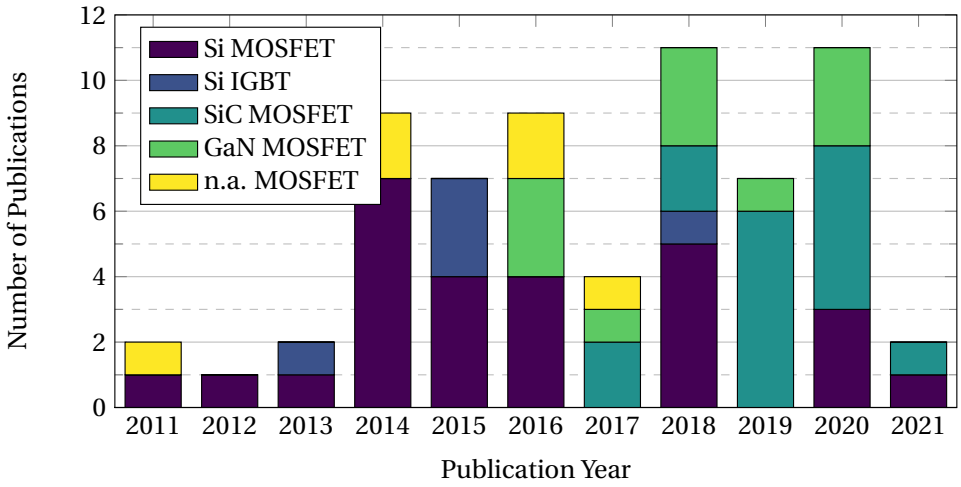


Figure 2.7: Reported switch type sorted per year of the literature studies from Table 2.3. See the legend for the switch types, where n.a. (not available) MOSFET means that the type of MOSFET (Si/SiC/GaN) is not mentioned. See Appendix C for an overview of all references.

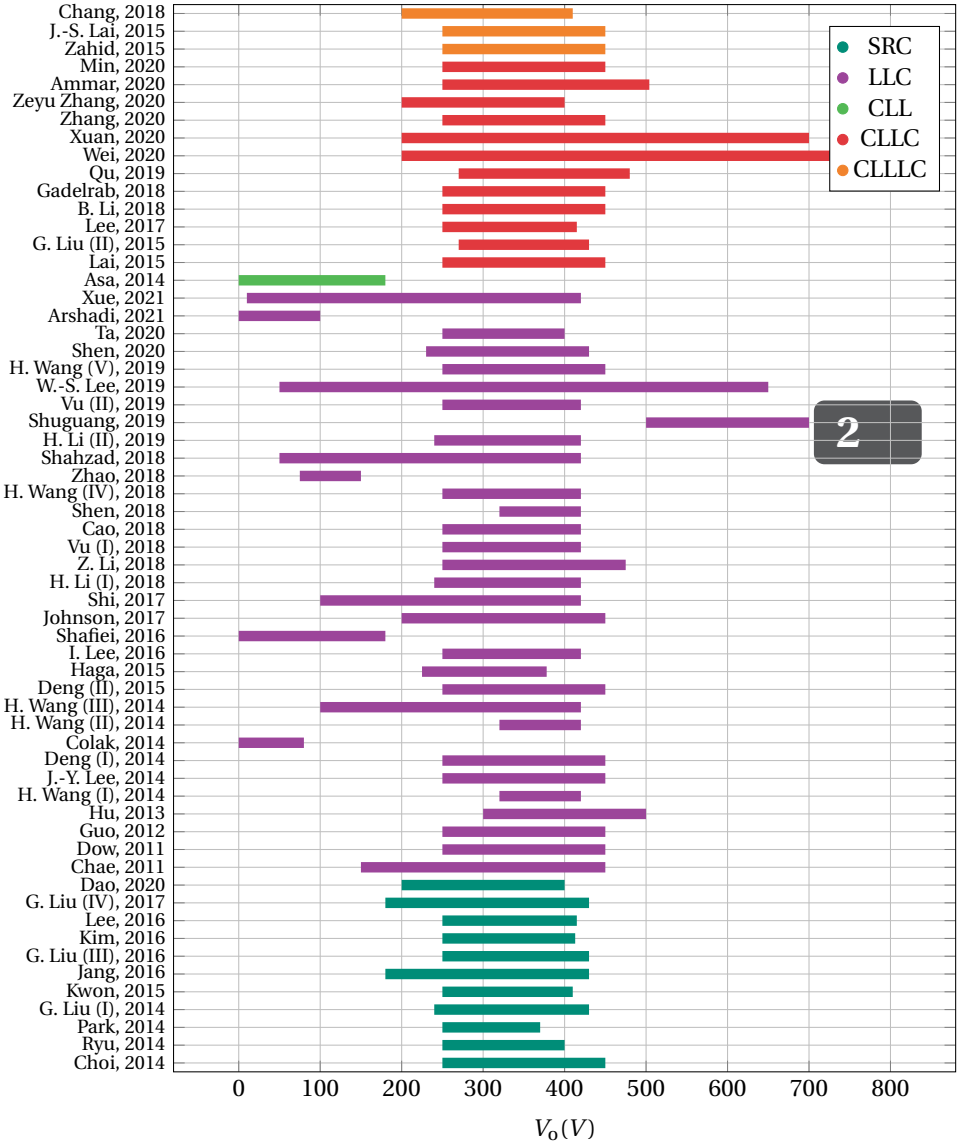


Figure 2.8: Reported V_o range of literature studies regarding an RPC for EV charging. The first author and year of the study is shown on the y-axis. Studies reporting a V_o range of <50 V are not displayed. See Appendix C for an overview of all references.

OBSERVATIONS OF QUANTITATIVE DATA

Some observations can be made based on Figures 2.5 to 2.8:

- Figure 2.5 shows an upward trend in the maximum reported efficiency η_{max}, with a maximum of η_{max} = 98.5% reported by three studies in 2020 [28–30]. These three studies are elaborated below:
  - Ta et al. (2020) proposed a hybrid LLC converter: it is possible to 'select' three different operation modes, which lead to higher efficiencies at low loads when compared to a traditional LLC converter. Besides this, the switch type used is GaN MOSFET. The most commonly found output voltage range of 250-400 V is reported [28].
  - Shen et al. (2020) proposed a operation-mode based design instead of the common Fundamental Harmonic Analysis (FHA), and implemented it in such a way as to minimize the reactive power of the design. However, the most common output voltage range of 250-400 V is reported again [29].
  - Wei et al. (2020) proposed a CLLC converter which is reconfigurable between HB and FB, and PFM in combination with PWM to control the converter. Despite this high efficiency, no wide output voltage range is reported [30].
- Figure 2.6 shows a clear increase in volumetric power density over the years. The highest value of 8 kW/L is reached by Wei et al. (2020) [30]. This information from Figure 2.6 will be used in Chapter 8 to benchmark the converter designed in this study.
- Figure 2.7 indicates that the use of Wide Band Gap (WBG) MOSFET transistors (SiC MOSFET & GaN MOSFET) has increased in popularity in the studies from Table 2.3. These transistors have lower switching losses when compared to similar Si MOSFET transistors. Four out of five studies using IGBT's show inferior η_{max}: Yoo et al. (2013): η_{max} = 93% [31], Lai et al. (2015): η_{max} = 95% [32], Kwon et al. (2015): η_{max} = 95.6% [33] and finally Zhao et al. (2018): η_{max} = 96% . However, Zahid et al. (2015) reported an η_{max} = 98.10%, by using Infineon IGBT's with reverse conducting diodes (IKW40N65F5). However, the secondary side switches were implemented using MOSFET's [20]. Zahid et al. (2015) show that it is possible to achieve high efficiency using IGBTs. Therefore, the performance of IGBTs is investigated as part of the current study.
- Figure 2.8 indicates that most studies report an output voltage V_o between 250-420 V. This is in agreement with the currently most common (400 V) battery architecture of EVs, as discussed in Section 1.1. Only six studies reported an output voltage range of >320 V: [30, 34–39].

2.5. WIDE OUTPUT VOLTAGE TOPOLOGIES

It is observed, in the last paragraph of Section 2.4, that only a minority of the studies into RPCs for EV charging reported wider output voltage ranges than 320 V. A wider output voltage range is not easily achieved using only PFM: this will result in a wide switching frequency range. A wide switching frequency range results in the following issues [40]:

- A more complicated magnetic component design.
- In some parts of the operation range, soft-switching might be lost. This degrades the efficiency of the converter in this range.
- Reduced EMI performance.

Studies that did report a wide output voltage range, therefore, either combined PFM with another control strategy or modified the some parts of the structure of the RPC. The six studies that did report V_o >320 V are further discussed in this section. Key characteristics of the wide output voltage range studies are presented in Table 2.4. These six studies are categorized into five different groups. The advantages and disadvantages of these five groups are discussed after Table 2.4. The final topology selected to achieve the wide output voltage range required in this study is selected in Section 2.6.

Table 2.4: Comparison of all wide output voltage range solutions involving an RPC. **Also counting the Rectifier diodes before the SEPIC PFC.*

	Variable input voltage SEPIC PFC + LLC [34]	Variable input voltage SEPIC PFC + LLC [35]	Two interleaved LLC converters [37]	Three level CLLC Converter [36]	Combination of Control Strategies CLLC converter [30]	Two-Stage: LLC + Buck converter [39]
Modulation	Constant f_{sw}, Variable V_{in}	Constant f_{sw}, Variable V_{in}	PSM	PFM + Variable operational modes	PFM + Variable V_{in} + reconfiguring between Half-Bridge (HB) Full-Bridge (FB)	LLC: Constant f_{sw} Buck: Duty cycle control
Output Voltage range	100-420 V	100-420 V	10-420 V	200-700 V	200-800 V	50-650 V
Switching frequency range	-	200 kHz	100 kHz	31-70 kHz 140-250 kHz	LLC: 120 kHz Buck: 50 kHz	
Number of switches	5	5	4	16	8	5
Number of Diodes	9*	9*	4	4	0	9
Number of Transformers	1	1	2	1	1	2
Peak efficiency	97.4%	88.4%	98.10%	96.8%	98.5%	97.32%
Maximum Power	3.3 kW	3.3 kW	1 kW	3.5 kW	22 kW	20 kW
Control Complexity	Moderate	Moderate	Moderate	Complex	Complex	Simple
Power Density	-	-	-	-	8 kW/L	-

The solutions they used to achieve these wide output voltage ranges for EV charging can be categorized into five different groups, presented below:

- **Variable input voltage**: Both Wang et al. (2014) [34] and Shi et al. (2017) [35] used a SEPIC PFC stage before the RPC to vary the input voltage. This stage directly controlled the output voltage of the RPC, which is operated at a constant switching frequency near the resonant frequency where it is most efficient. Both studies achieved an output voltage range of 100-420 V.
- **Interleaving two RPCs**: Xue et al. (2021) [37] put two LLC converters in parallel, which both operated at a constant frequency (their resonant frequency). The output voltage is regulated by phase-shifting the two converters relative to each other, thereby achieving an output voltage range of 10-420 V.
- **Three-level RPC**: Xuan et al. (2020) [36] used a three-level CLLC converter implemented with seven switches on each side of the converter. The optimal working mode is selected depending on the required output voltage (200-700 V). This study still used PFM to control the output voltage. The operating f_{sw} range is, however, relatively small: 38.32-50.67 kHz.
- **Combination of Control strategies**: Wei et al. (2020) [30] used a combination of control strategies to achieve a wide output voltage range of 300-800 V: re-configuring between FB and HB, PWM, a variable DC-link voltage and Phase Shift Modulation (PSM) of the CLLC converter.
- **Two-stage converter**: Lee et al. (2019) [39] proposed a two-stage structure, where the RPC is the first stage followed by a buck converter a the second stage. This two-stage solution allowed for a decoupling of the functions of the proposed converter: the resonant stage provided galvanic isolation and a constant voltage-step up through the turns ratio of the transformer. Only the buck controller controlled the output voltage, since the LLC is operated only at the resonant frequency. This two-stage solution achieved a output voltage range of 50-650 V.

The advantages and disadvantages of the five different groups of solutions to achieve a wide output voltage range are discussed step-by-step in the next paragraphs.

First, the variable input voltage solutions proposed by Wang et al. (2014) [34] and Shi et al. (2017) [35] cannot be used in this study: the input voltage is not a free variable, but rather a constraint because it varies between 640-840 V depending on the SOC of the stationary battery.

Second, the two interleaved LLC converters proposed by Xue et al. (2021) [37] show high full-load efficiency. However, as mentioned in their study, the RMS current in the RTNs increases for a decrease in output voltage, thereby increasing conduction and switching losses. These increased losses result in a decrease in efficiency at lower output voltages: at 335 V and maximum output current, the efficiency is around 95.8%. Then at 150 V and maximum output current, the efficiency is around 90.5%. This decrease in efficiency at low output voltages highlights the main disadvantage of this type of solution.

Third, the three-level RPC solution to achieve a wide output voltage range can be best described by the study by Xuan et al. (2020) [36]. They were able to achieve a wide output voltage range, however, the number of switches required is 4x larger than the original FB LLC converter, which makes it expensive. It is relatively complex in control

due to the 16 different working modes of the converter and delivers worse performance efficiency-wise compared to the other groups.

Fourth, the group of solutions where a combination of control strategies is used to achieve a wide output voltage looks promising. Wei et al. (2020) [30] were able to deliver the widest output voltage range (together with [39]) and the highest reported efficiency. However, the maximum efficiency is also to be expected because of the relatively large output power of 22 kW compared to the other studies in Table 2.4. Besides this, the main disadvantage is the higher control complexity because of the combination of different control strategies. Apart from the study by Wei et al. (2020) [30], another study recommends a combination of control strategies, for example, PFM+PWM, as well [40] for wide output voltage applications. The study by Wei et al. (2020) focused mostly on the different (non-combined) modulation strategies for LLC converters. The following strategies were investigated: PSM, PWM and Resonant Frequency Modulation (RFM). RFM involves controlling the output voltage through either modifications of the resonant capacitor or resonant inductor. Out of all eleven modulation strategies discussed in this paper, only two were recommended for wide input/output voltage range applications: Secondary Side Pulse Width Modulation (SSPWM) and Secondary Side Phase Shift Modulation (SSPSM). However, the latter complicates circuit analysis: FHA cannot be used any longer due to the distortion in the secondary side caused by the phase shift. This complicates the analytical model and is therefore not preferred. Furthermore, in SSPWM [41], the Dutycycle to gain relation cannot be determined analytically. It requires the numerical solving of 25 equations based on the seven different converter equivalent circuits, making the analytical modelling of this converter complex as well. The achieved peak efficiency in the study by Wang et al. (2018) [41] is 96.7% for a 1 kW prototype, however, the converter only operated in a voltage range of 250-420 V. Another non-EV charging study did reach a wide output voltage range of 100-500 V by combining SSPWM with PFM while achieving a relatively flat efficiency profile with a maximum of 95.3% [42]. Another study regarding an LCC converter reported a combined control strategy of Duty cycle variation and PFM to control the output of the resonant converter [43]. This strategy allowed for a narrowing of the f_{sw} range when compared to only PFM, improving the efficiency at lower output power. This group of solutions for a wide output voltage characterizes itself by promising performance, while requiring more complex analytical models and control methods.

Finally, the group of two-stage solutions to achieve a wide output voltage range. Employing another stage after the LLC converter allows for decoupling of the functions of the converter: the LLC converter provides galvanic isolation and a constant voltage gain through the turns ratio of the transformer. The second stage is used to condition the voltage according to the requirements of the EV. The LLC converter can operate at a constant frequency near the series resonant frequency, allowing for optimal design of the magnetic components. Besides this, ZVS of the primary switches is guaranteed for the entire operating range, contrary to a PFM LLC converter. An additional benefit of the LLC converter operating at constant f_{sw} near the series resonant frequency is the drawing of near sinusoidal currents. Control of the LLC converter used as such is simple, and control of one of the three basic non-isolated DC-DC converters (Buck, Boost or Buck-boost) is also straightforward, at least in Continous Conduction Mode (CCM) and

Boundary Conduction Mode (BCM). The study of Lee et al. (2019) [39] implemented a single buck converter after the LLC converter. The proposed topology achieves an output voltage range of 50-650 V and a peak efficiency of 97.32%. This peak efficiency is considerably lower than the 98.5% achieved by Wei et al. (2020) [30]. However, Lee et al. (2019) [39] used a single buck converter to handle the full 22 kW of the converter. A SiC MOSFET is used as a switch in the buck converter, but the switching losses of this single switch still contributed to 19% of the total losses. There is, therefore, room for improvement in the context of efficiency for this type of solution.

2.6. FINAL TOPOLOGY SELECTION

Of all groups of solutions listed in Section 2.5, a two-stage solution is selected as the final topology of this study. It stands out from the other groups because of its simplicity in analytical modelling and control and promising efficiency. The LLC converter operates at a fixed f_{sw} close to the series resonant frequency for minimal circulating energy in the resonant tank and maximal efficiency. One method to improve upon the design proposed in [39] is to operate the Buck converters in TCM (from here on TCM Buck converter) [44–46]. This type of buck converter differs from the regular buck converter in a few ways:

- **ZVS turn-on**: The diode of the regular buck converter is replaced by a switch. This allows the current through the inductor to go negative (reverse its direction), instead of going into BCM. This reversed current allows for ZVS turn-on of the upper switch, greatly reducing the switching losses because E_{on} is generally larger than E_{off}. The lower switch also operates in ZVS-turn on [46].
- **Large current ripple**: A large ripple current is required if the converter has to supply a large output current [47]. This is because in order to have ZVS turn-on, the current has to reverse its direction: creating a ripple of $> 2 \cdot I_o$. This increases conduction losses in the switch, which go by I_{rms}^2 for a MOSFET. It also increases the required output DC-link capacitance, thus increasing the volume of the converter.
- **Variable Switching Frequency**: Unlike the regular buck converter, the TCM Buck converter has to vary its switching frequency in order to supply different load currents. This will be explained in Section 3.2.

Furthermore, the main advantage of a TCM Buck converter is their extraordinary reported efficiency: Christen et al. (2012) reached a peak efficiency of 99.4% for a single TCM Buck converter [46]. One disadvantage is the large current ripple required for this type of Buck converter. The load can be split across multiple buck converters through interleaving. This reduces the current stresses (and thereby conduction losses) for an individual TCM Buck converter [48]. This also allows the large output current ripple of a single TCM buck converter to be partially canceled, reducing the required DC-link output capacitance. The combination of the LLC and Interleaved TCM buck converters can be implemented in multiple configurations, as will be seen in Chapter 4. Moreover, both MOSFETs and IGBTs can be used as switches for these converters. A framework to compare the different configurations and switch devices is outlined in Chapter 4, but the analytical models of the LLC- and Interleaved TCM Buck converter will first be detailed in Section 3.1 and Section 3.2 respectively.

3

Analytical Models

As concluded in Chapter 2, the selected topology for this study is the two-stage converter consisting of the LLC resonant power converter followed by an Interleaved TCM Buck converter. In this chapter, the analytical models of both converters are discussed. These models are implemented in MATLAB, providing the analytical basis of the converters. This basis is used together with a theoretical model to calculate the semiconductor- and magnetic losses (described in Appendix A) to determine the theoretical efficiency of the converters.

3.1. LLC converter

First the LLC converter; the function of the LLC converter in this design is two-fold:

1. To provide galvanic isolation.
2. To step up the 640-840 V input voltage to $2x$ 525-689 V on the DC-link between the two stages of the converter.

The implemented LLC converter is shown in Figure 3.1.

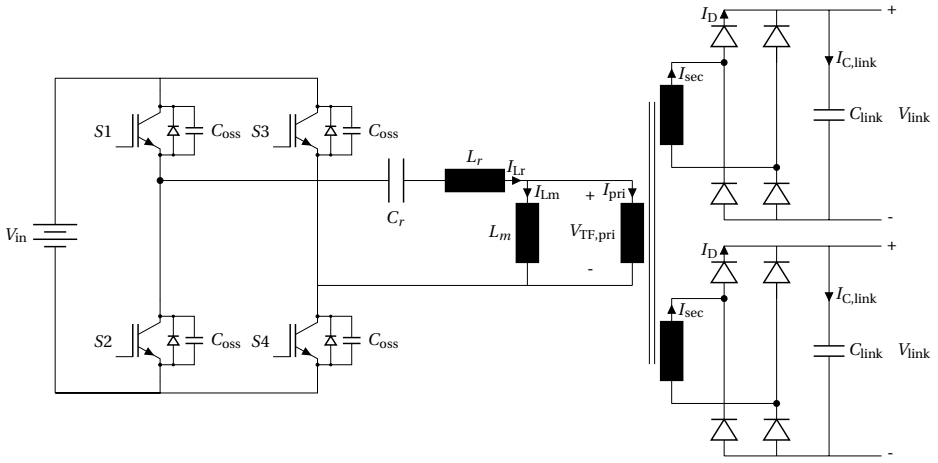


Figure 3.1: Schematic of the LLC converter with two secondary side rectifiers. This converter is equipped with IGBTs for illustrative purposes.

It was found during the quantitative part of the literature study that the most used control method for controlling the LLC converters is PFM. However, the LLC converter will always be operated at the series resonant frequency (fixed frequency) in this work. At this frequency, the gain of the resonant tank is unity (the tank $Z_{RTN} = 0\Omega$), and only the fundamental waveform of the current is flowing through the converter. A simplified analysis technique to represent the LLC converter operating at the series resonant frequency is the First Harmonic Approximation (FHA) as first proposed by R.L. Steigerwald in 1988 [27]. The core assumption of this analysis technique is that the resonant tank filters all higher-order harmonics, and therefore classical AC analysis techniques can be used, leading to the equivalent circuit in Figure 3.2.

The rectifier and load resistance is replaced by an equivalent AC resistance R_{AC} in Figure 3.2. R_{AC} is calculated in Equation (3.1).

$$R_{\mathrm{AC}} = \frac{8n^2 R_L}{\pi^2} \tag{3.1}$$

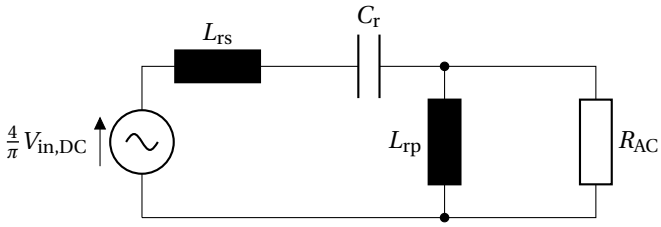


Figure 3.2: Fundamental Harmonic Approximation equivalent schematic circuit of the LLC converter.

R_L is the combined resistance of the Interleaved TCM Buck converter stage charging the EV. R_L can be expressed in terms of the output power and DC-link voltage shown in Equation (3.2).

$$R_L = \frac{\left(2 \cdot V_{\text{link}}\right)^2}{P_{\text{o}}} \tag{3.2}$$

Using the FHA representation of Figure 3.2 and the normalized quantities Q_L,l and ω/ω_0, an expression for the voltage gain of the LLC converter M_{v} can be derived, shown in Equation (3.3).

$$M_{\text{v}} = \frac{1}{\sqrt{\left(1 + l - l \cdot \left(\frac{\omega_0}{\omega}\right)^2\right)^2 + Q_L^2 \cdot \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2}} \tag{3.3}$$

The definitions of the normalized variables used in Equation (3.3) are repeated in Equations (3.4) to (3.6).

$$l = \frac{L_r}{L_m} \tag{3.4}$$

$$Q_L = \frac{Z_0}{R_{\text{AC}}} \tag{3.5}$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{3.6}$$

Where l is the ratio between the series resonant inductor L_r and the magnetizing inductor L_m (see Figure 3.1), Q_L is the quality factor, and Z_O is the characteristic impedance. As shown in Figure 3.3, the resonant tank has unity gain independent of Q_L (and thus independent of R_L) at $f = f_{\text{r}}$.

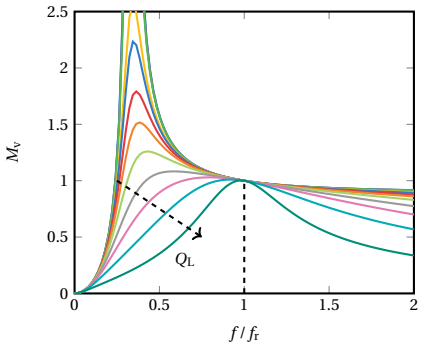


Figure 3.3: Voltage gain of the LLC converter at different operating frequencies. The voltage gain changes depending on the quality factor Q_{L}. The inductance ratio is $l = 0.15$ in this figure.

3.1.1. OPERATIONAL WAVEFORMS

The typical waveforms of the LLC converter are displayed in Figure 3.4. This figure consists of four sub-figures, which are explained below.

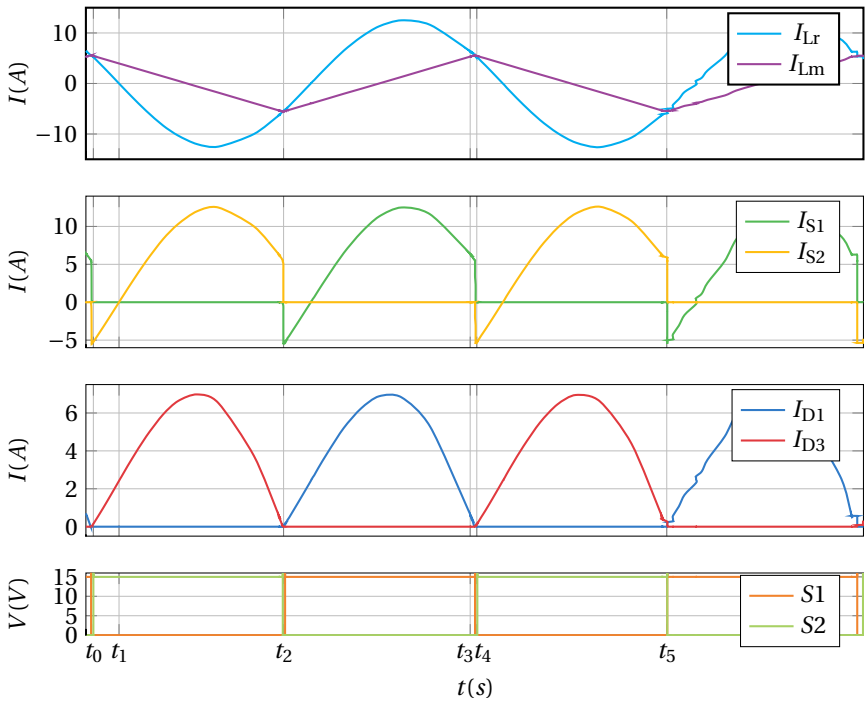


Figure 3.4: Operational waveforms of the LLC converter.

In the first figure plot in Figure 3.4, the resonant and magnetizing current I_{Lr} and I_{Lm} are displayed. I_{Lr} is perfectly sinusoidal since $f_{sw} = f_{sr}$, which improves losses in the magnetic components. The magnetizing current I_{Lm} serves to charge/discharge C_{oes} (and C_{snub}, if used) during the deadtime ($t_3 - t_4$), to allow for ZVS turn-on.

The switch current is displayed in the second figure plot in Figure 3.4. The angle $\angle Z_{in}$ (from Equation (3.8)) can be seen, for example, between t_0 and t_1. Note that the current stress on both $S1$ and $S2$ is equal for the LLC converter. Furthermore, because I_{Lm} has the same magnitude irrespective of P_o, the turn-off current $I_{sw,off}$ of the LLC converter is constant. Therefore, P_{sw} of the LLC converter is also constant over the entire load range, as shown in Figure 5.1 further on in this study.

The third figure plot shows the usual full bridge rectifier current waveforms. Note the difference in y-axis scale between this figure and the second figure. This is change is caused by the winding ratio n used to step up V_{in} to V_{link}. This reduces the current in magnitude from the primary to the secondary side.

The last figure shows the gate signals to $S1$&$S4$ and $S2$&$S3$, respectively. There is some dead time between the gate signals to allow for ZVS-turn on. Note that the Duty

cycle is fixed to $D = 0.5$ in this study.

3.1.2. ANALYTICAL EXPRESSIONS

The analytical model for the LLC converter is further explained in this section. It is required to calculate several Root Mean Squared (RMS) and average currents in the converter, in order to calculate the theoretical losses and efficiency later on in this study. Starting with the input impedance of the LLC converter. Since the LLC converter is operating at the series resonant frequency, the impedance magnitude and angle expression is simplified and given by Equations (3.7) and (3.8).

$$|Z_{\text{in}}| = \sqrt{\frac{64L_m^2R_L^2n^4}{64R_L^2n^4L_rC_r + L_m\pi^2}} \tag{3.7}$$

$$\angle Z_{\text{in}} = \arctan\left(\frac{8\sqrt{L_rC_r}n^2}{L_m\pi^2}\frac{V_o^2}{P_o}\right) \tag{3.8}$$

Equations (3.7) and (3.8) are then used to calculate the RMS current through the RTN in Equation (3.29).

$$I_{\text{Lr,RMS}} = \frac{4}{\pi}\frac{1}{\sqrt{2}}\frac{V_{\text{in}}}{|Z_{\text{in}}|} \tag{3.9}$$

The RMS current through the magnetizing inductance is constant and given by Equation (3.10).

$$I_{\text{Lm,RMS}} = \frac{4V_{\text{in}}}{\pi\sqrt{2}}\frac{M_{\text{v}}}{\omega L_m} \tag{3.10}$$

The voltage amplitude over the resonant capacitor C_r is given by Equation (3.11).

$$V_{\text{Cr,max}} = \frac{1}{\omega C_r}I_{\text{Lr,RMS}} \tag{3.11}$$

The turn-on and turn-off current of the LLC primary side switches is given by Equation (3.12) and Equation (3.13). As can be judged from these equations, $I_{\text{sw,on}} = -I_{\text{sw,off}}$. Another characteristic of the LLC converter is that both $I_{\text{sw,on}}$ and $I_{\text{sw,off}}$ remain constant over the entire operating range.

$$I_{\text{sw,on}} = -\sqrt{2}I_{\text{Lr,RMS}}\sin(\angle Z_{\text{in}}) \tag{3.12}$$

$$I_{\text{sw,off}} = \sqrt{2}I_{\text{Lr,RMS}}\sin(\angle Z_{\text{in}}) \tag{3.13}$$

The RMS and average currents through the semiconductor switches are given in Equations (3.14) to (3.17). These currents, together with Equations (3.12) and (3.13), are required for calculating the conduction losses of the switches and their reverse conducting diodes (see Appendix A).

$$I_{\text{sw,RMS}} = \frac{\sqrt{2}I_{\text{Lr,RMS}}}{2\sqrt{\pi}}\sqrt{\cos(\angle Z_{\text{in}})\sin(\angle Z_{\text{in}}) + (\pi - \angle Z_{\text{in}})} \tag{3.14}$$

$$I_{\text{sw,avg}} = \sqrt{2}I_{\text{Lr,RMS}}\frac{\cos(\angle Z_{\text{in}}) + 1}{2\pi} \tag{3.15}$$

$$I_{\text{bodydiode,RMS}} = \frac{\sqrt{2}I_{\text{Lr,RMS}}}{2\sqrt{\pi}}\sqrt{-\cos(\angle Z_{\text{in}})\sin(\angle Z_{\text{in}}) + \angle Z_{\text{in}}} \tag{3.16}$$

$$I_{\text{bodydiode,avg}} = \sqrt{2}I_{\text{Lr,RMS}}\frac{\cos(\angle Z_{\text{in}}) - 1}{2\pi} \tag{3.17}$$

The rectifier diode current stresses are calculated using Equations (3.18) and (3.19), assuming π radians conduction time for each diode.

$$I_{\text{D,avg}} = \frac{1}{2}\frac{P_{\text{o}}}{V_{\text{link}}} \tag{3.18}$$

$$I_{\text{D,RMS}} = \frac{\pi}{2}I_{\text{D,avg}} \tag{3.19}$$

The RMS current through the DC-link capacitors in terms of the total output power P_{o} is given by Equation (3.20).

$$I_{\text{DClink,RMS}} = \frac{1}{2}\frac{P_{\text{o}}}{V_{\text{o}}}\sqrt{\frac{\pi^2}{8} - 1} \tag{3.20}$$

3.1.3. SOFT-SWITCHING

The LLC converter can achieve ZVS turn-on of the primary side switches. This can greatly improve the efficiency of the converter by eliminating the turn-on switching loss. This ZVS turn-on is achieved throughout the entire operating range due to the constant f_{sw}, which is slightly above the series resonant frequency. There are a few prerequisites for ZVS to occur in the resonant converter [19]:

- An inductive input impedance is required. This means that the current is lagging the applied voltage. Consequently ensuring a current to flow through the body diode of the switches during the turn-on transient, resulting in ZVS turn-on. This is why the LLC converter is operated slightly above the resonant frequency.
- Sufficient energy in the resonant tank to discharge and charge the output capacitances of all four switches.
- Sufficient deadtime to allow the discharge/charge process of the output capacitances to be completed before turning on the switch.

Requirement two and three can be summarized in Equation (3.21), which determines the maximum magnetizing inductance L_{m} such that the output capacitances can all be charged/discharged within a given deadtime [49].

$$L_{\text{m,max}} = \frac{t_{\text{dead}}}{16 \cdot C_{\text{equi}} f_{\text{sw}}} \tag{3.21}$$

C_{equi} in Equation (3.21) is the equivalent representation of all output capacitances and snubbers (if applicable). It is given by Equation (3.22). The output capacitance C_{oss} is calculated through the method proposed by Kasper et al. (2016) [50].

$$C_{equi} = 4 \cdot \left(C_{oss} + C_{snub}\right) \tag{3.22}$$

3.1.4. VERIFICATION OF ANALYTICAL MODEL

The validity of Equations (3.1) to (3.20) is checked using an LTSpice model of the complete (not the FHA) model LLC converter. Multiple operation points from the analytical model in MATLAB are verified in LTSpice. The testing conditions are listed in Table 3.1, and the results are given in Figures 3.5 and 3.6.

Table 3.1: Selected conditions to compare the LLC converter Analytical model with the LTSpice simulation model.

Parameter	**Symbol**	**Value**
Input Voltage	V_{in}	840 V
DC-link output voltage (single winding)	V_{link}	689 V
Switching frequency	f_{sw}	50 kHz
Resonant Inductance	L_r	44 µH
Resonant Capacitance	C_r	229 nF
Magnetizing Inductance	L_m	360 µH
Deadtime	t_{dead}	1500 ns
Snubber Capacitor	C_{snub}	4.5 nF

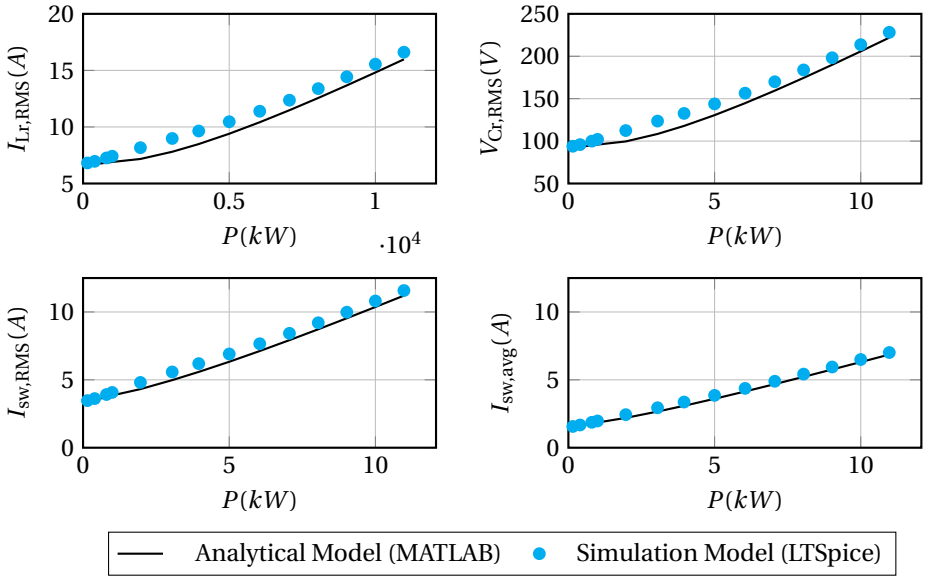


Figure 3.5: **Part 1/2** of the comparison of the analytical FHA model equations versus the LTSpice Simulation of the LLC converter.

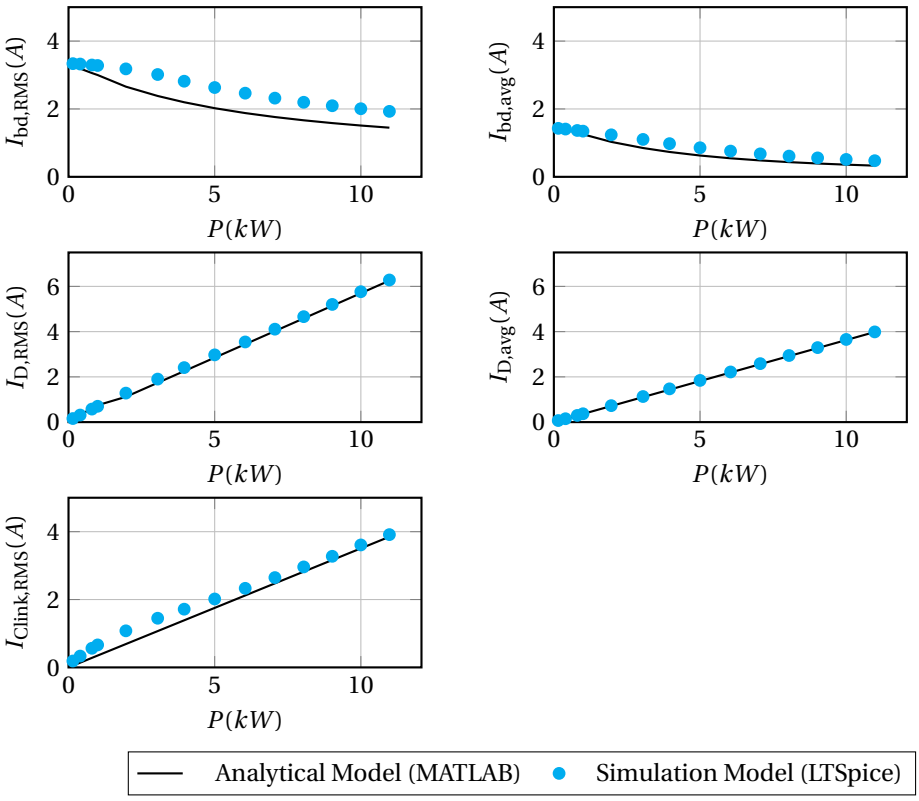


Figure 3.6: **Part 2/2** of the comparison of the analytical FHA model equations versus the LTSpice Simulation of the LLC converter.

3.1.5. EXPLANATION OF DEVIATION

As seen in Section 3.1.4, there is a slight deviation between the analytical FHA model and the values retrieved from the LTSpice simulation. There is one main cause behind this: the effect of the dead time on the continuity of the current through L_r and voltage over L_r (see Figure 3.7).

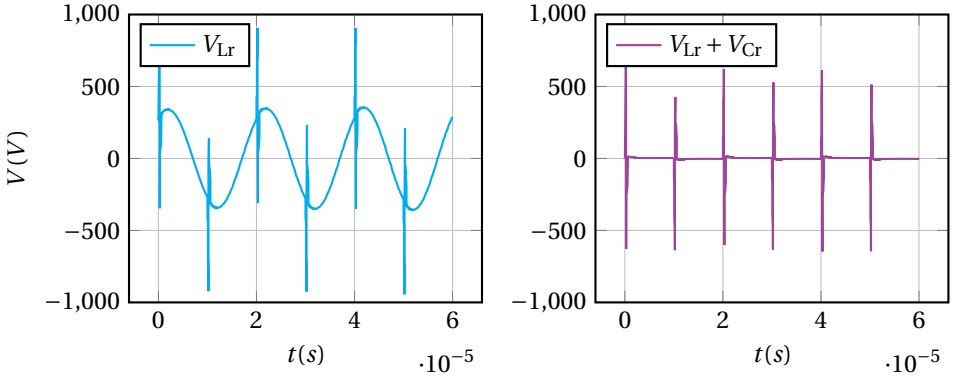


Figure 3.7: Deviations of the voltage over L_r when compared to the FHA model are displayed in the left figure. This results in a nonzero impedance/voltage over the combination of $V_{Lr} + V_{Cr}$ as seen in the figure on the right.

A zoomed-in picture of the phenomenon shown in Figure 3.7 is displayed in Figure 3.8, and explained below.

- t_0-t_1: Switch S3 is turned off (together with S2) at t_0, which starts the discharging/charging of the output capacitances (or snubber capacitances) of all four switches. This initiates the decrease in voltage applied to the resonant tank V_{AB}. Since the output diode D_3 is still conducting, $V_{TF,pri}$ remains constant and equal to $n \cdot V_{link}$. The result of both effects is that L_r is subjected to an increase in voltage, as seen in the rising of V_{Lr}.

- t_1-t_2: At t_1, the D_3 (and D_2) cease to conduct, causing the primary winding of the transformer to equal an open-circuit and $I_{Lr} = I_{Lm}$. This causes V_{Lr} to go negative since V_{AB} is still applied. Because the di/dt across L_r suddenly reduces, an additional inductive negative voltage across L_r appears, as is seen for the $V_{TF,pri}$ waveform.

- t_2-t_3: At t_2, $V_{AB} = 0$, which results in $V_{Lr} = 0$ at t_2. The voltage $V_{TF,pri}$ follows the rise in V_{AB} due to the charging/discharging of the output capacitances of the primary side switches.

- t_3-t_4: At t_3, $V_{TF,pri}$ (see Figure 3.1) has completed the commutation, allowing D_1 and D_4 to conduct.

- t_4-$t_{...}$: At t_4, all output capacitances of the switches are fully charged/discharged

to V_{in}, which ends the disturbance in V_{Lr}.

In essence, there is a nonzero voltage drop over the combination of $L_r + C_r$ in the period of t_0-t_4 during each switching instant of the converter (see Figure 3.7). Because zero impedance (and therefore, a zero voltage drop) of $L_r + C_r$ was assumed in Equations (3.7) and (3.8), all calculated parameters based on these two values will show deviations from the FHA model. This explains the deviations between the FHA analytical model and the simulations, as previously observed in Figures 3.5 and 3.6.

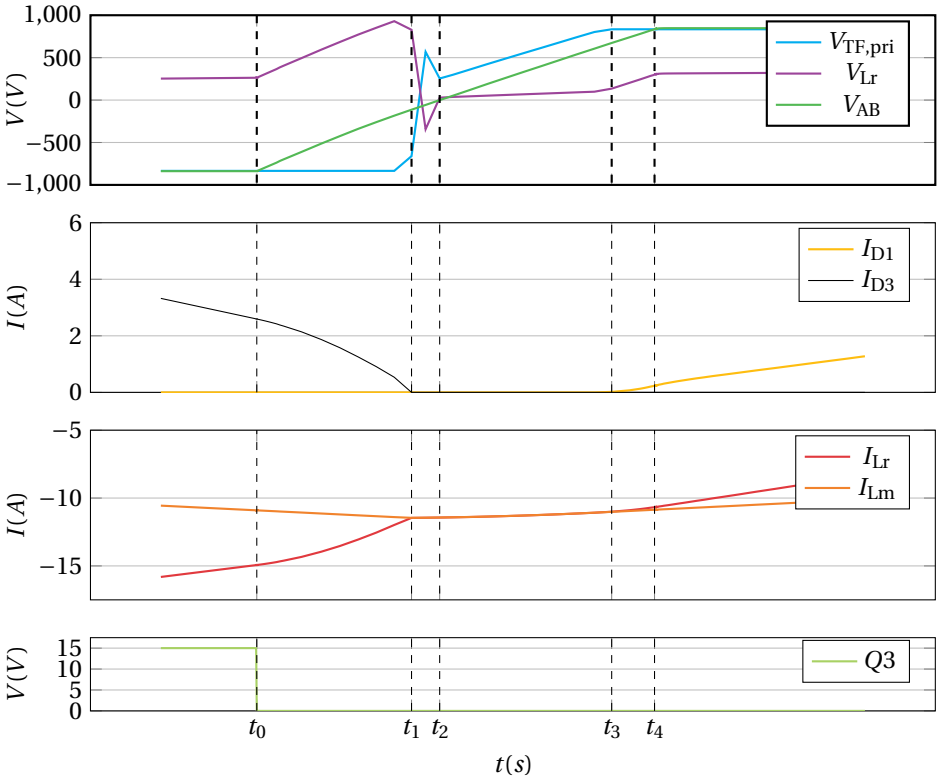


Figure 3.8: Zoom in of Figure 3.7 on different parameters during the disturbance seen in V_{Lr} during switching instances.

3.2. INTERLEAVED TCM BUCK CONVERTER

The second stage of the proposed EV charger consists of Interleaved TCM Buck converters. A regular CCM or Discontinuous Conduction Mode (DCM) buck converter would generate both turn-on and turn-off losses. Therefore, in an attempt to improve the efficiency of the two-stage EV charger, an Interleaved TCM Buck converter is implemented as the second stage. The downside of one single TCM Buck converter is the larger current ripple than the regular Buck converter, which will be addressed later in Section 3.2.2. The TCM buck converter topology is derived from the regular buck converter by replacing the diode with a semiconductor switch. This allows the current through the buck inductor to reverse its direction, which is key to the ZVS turn on operation. A schematic of a single TCM Buck converter is shown in Figure 3.9.

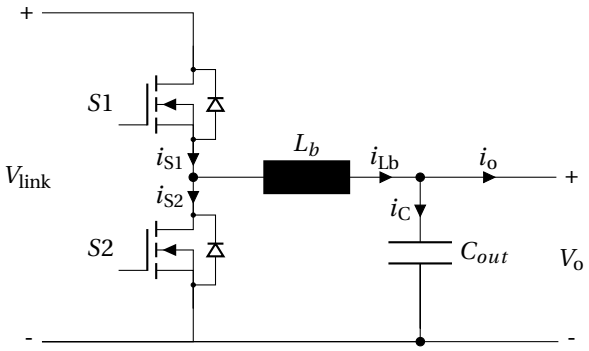


Figure 3.9: Schematic of a single TCM Buck converter.

3.2.1. OPERATIONAL WAVEFORMS

The waveforms of a single TCM Buck converter show the difference between the regular buck converter, see Figure 3.10. The current through the inductor I_{Lb} can reverse its direction, whereas in the regular buck converter, the current would seize to flow at 0 (DCM). The current continues to turn negative until $I_{Lb} = -I_R$ is reached. At this point, S2 turns off, and the converter enters a period in which resonance occurs (see Section 3.2.3). After this, I_{Lb} will flow through the body diode of S1 (see Figure 3.9), allowing for ZVS turn-on at t_1.

The duty cycle D, given by Equation (3.23), can be observed from Figure 3.10. There is always a certain amount of t_{dead} required, which limits the maximum achievable duty cycle D.

$$D = \frac{T_{on}}{T_{on} + T_{off}} = \frac{t_2 - t_1}{t_3 - t_1} \tag{3.23}$$

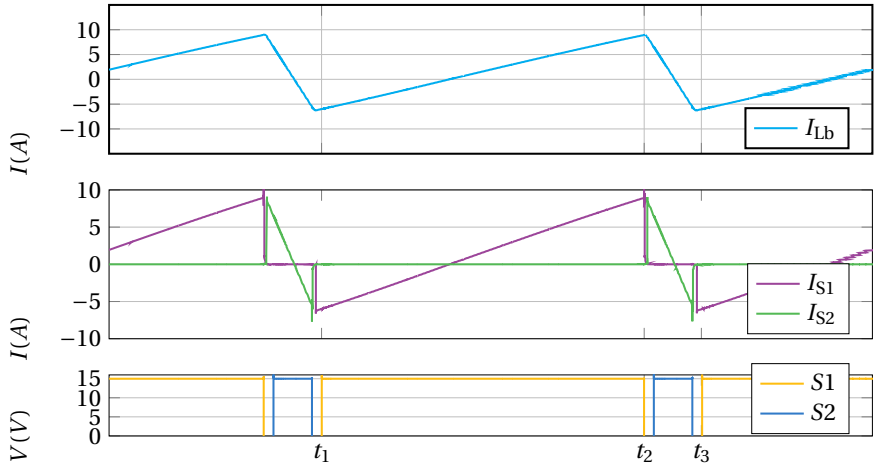


Figure 3.10: Typical operational waveforms of a single TCM buck converter. $T_{on} = t_1 - t_2$ and $T_{off} = t_2 - t_3$.

3.2.2. ANALYTICAL MODEL

The analytical model for the Interleaved TCM Buck converter is given in this section. This model is, again, implemented in MATLAB and used in combination with theoretical loss calculations (see Appendix A) to determine the theoretical efficiency of the converter. Note that all expressions are shown for a single buck converter, unless mentioned otherwise. Starting with the duty cycle in Equation (3.24).

$$D = \frac{V_o}{V_{in}} \tag{3.24}$$

Followed by the output current, which is controlled by the switching frequency (see Equation (3.25)). This in contrast to the regular buck converter.

$$f_{sw} = \frac{1}{L_b} \cdot D \cdot \frac{V_{in} - V_{out}}{2\left(I_o + I_R\right)} \tag{3.25}$$

The average current through the inductor is equal to the I_o, just as in the regular buck converter. What causes the large current ripple is that the current needs to reach $-I_R$ for every operation point to achieve ZVS turn-on. Therefore the maximum current is more than $2x$ the required I_o, resulting in large current ripples. Information about the current ripple is given by Equations (3.26) to (3.28).

$$I_{L,avg} = I_o \tag{3.26}$$

$$I_{L,pk-pk} = 2(I_o + |I_R|) \tag{3.27}$$

$$I_{L,max} = 2(I_o + \frac{1}{2}|I_R|) \tag{3.28}$$

Now using Equation (3.27), the RMS current through the inductor can be calculated by Equation (3.29).

$$I_{\mathrm{L,rms}} = \sqrt{\frac{1}{3} I_{\mathrm{L,pk-pk}}^2 - I_{\mathrm{R}} I_{\mathrm{L,pk-pk}} + I_{\mathrm{R}}^2} \tag{3.29}$$

Next are the currents through switches S1 and S2. These equations are required to calculate the conduction- and switching losses of both switches. Equations (3.31) to (3.34) are taken from the work of Christen et al. (2012) [46].

$$k_1 = \frac{I_{\mathrm{R}}}{I_{\mathrm{L,pk-pk}}} \tag{3.30}$$

$$I_{\mathrm{S1,avg}} = D I_{\mathrm{o}} \tag{3.31}$$

$$I_{\mathrm{S1,rms}} = \sqrt{\left(I_{\mathrm{R}} \sqrt{D \frac{k_1}{3}}\right)^2 + \left(I_{\mathrm{L,max}} \sqrt{D \frac{1-k_1}{3}}\right)^2} \tag{3.32}$$

$$I_{\mathrm{S2,avg}} = (1-D) I_{\mathrm{o}} \tag{3.33}$$

$$I_{\mathrm{S2,rms}} = \sqrt{\left(I_{\mathrm{R}} \sqrt{(1-D) \frac{k_1}{3}}\right)^2 + \left(I_{\mathrm{L,max}} \sqrt{(1-D) \frac{1-k_1}{3}}\right)^2} \tag{3.34}$$

$$I_{\mathrm{S1,off}} = I_{\mathrm{L,max}} \tag{3.35}$$

$$I_{\mathrm{S2,off}} = I_{\mathrm{R}} \tag{3.36}$$

Equations (3.37) and (3.38) are related to the output current ripple of an interleaved buck converter. These equations, therefore, not refer to quantities of a single buck converter, but the result of interleaving N_{phase} buck converters. The output current ripple ΔI_{o} of an interleaved buck converter is provided by Yang et al. (2017) [47], in Equation (3.37).

$$\Delta I_{\mathrm{o}} = \frac{V_{\mathrm{in}} D}{f_{\mathrm{sw}}} \left(1 - \frac{\lfloor N_{\mathrm{phase}} D \rfloor}{N_{\mathrm{phase}} D}\right) \left(1 + \lfloor N_{\mathrm{phase}} D \rfloor - N_{\mathrm{phase}} D\right) \tag{3.37}$$

N_{phase} is the number of interleaved phases and D the duty cycle. In Figure 3.11 the effect of interleaving two and four buck converters (N_{phase} =2 or N_{phase} =4) is illustrated.

If ΔI_{o} is known, the RMS current through the DC-link output capacitor attached to the interleaved buck converters is calculated by Equation (3.38).

$$I_{\mathrm{C,rms}} = \sqrt{\frac{\Delta I_{\mathrm{o}}^2}{12}} \tag{3.38}$$

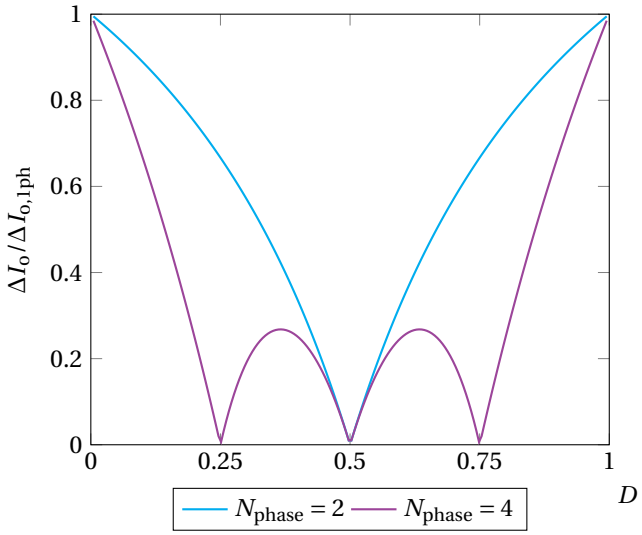


Figure 3.11: ΔI_o of two and four interleaved phases. Magnitude of the ripple is normalized to the output ripple of a single buck converter.

3.2.3. DEADTIME ANALYSIS

ZVS turn-on is achieved during the deadtime, and this period is therefore essential to the efficient operation of the Interleaved TCM Buck converter. This section explains processes occurring during the deadtime in detail. During the deadtime one of the output capacitances (C_{oss}) needs to be charged to V_{link} while the other needs to be discharged completely. This process occurs by resonance between the equivalent output capacitance C_{eq} and L_b. The equivalent capacitance is given by $C_{eq} = 2 \cdot C_{oss}$, assuming there is no snubber capacitor used.The equivalent circuit during deadtime is shown in Figure 3.12, and the waveforms are given in Figure 3.13.

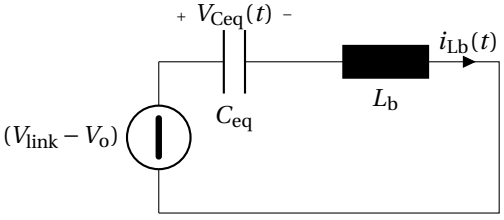


Figure 3.12: Equivalent circuit during deadtime of a single TCM buck converter, which is a series resonant circuit.

The resonant interval starts at t_0 and lasts until the output capacitances are fully charged/discharged at t_1. After t_1 the body diodes of the switches start to conduct, creating the circuit of Figure 3.9 again. During this period, the current i_{Lb} increases linearly according to Equation (3.39).

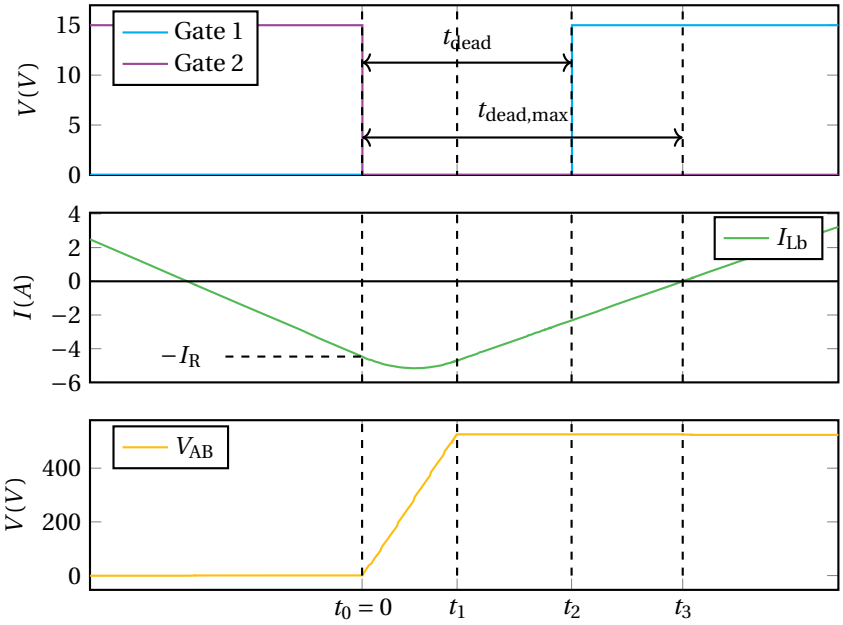


Figure 3.13: Waveform during t_{dead} in a single TCM buck converter. The resonant interval occurs between t_0 and t_1. To ensure ZVS the actual deadtime has to be kept between t_1 and t_3.

$$\Delta I_{Lb} = \frac{1}{L_b} \int (V_{in} - V_{out}) dt \tag{3.39}$$

The maximum deadtime, therefore, can be calculated as t_1 plus the time it takes to rise from $I_{Lb}(t_1)$ to 0 (t_3) (see Equation (3.40)).

$$t_{dead,max} = t_1 + \frac{L_b}{V_{in} - V_{out}} \cdot I_{Lb}(t_1) \tag{3.40}$$

If $t_{dead} > t_3$, then ZVS turn-on is lost because the body diode is not conducting anymore at time of turn-on of the respective switch. The set of allowable t_{dead} are, therefore, between t_1 and t_3. Applying Kirchoffs Voltage Law (KVL) and Kirchoffs Current Law (KCL) to the equivalent circuit results in the differential equations for $V_{C,eq}(t)$ and $I_{Lb}(t)$;

$$\begin{aligned} V_{C,eq}(t) &= (V_{in} - V_o) - ((V_{in} - V_o) - V_{c0}) \cos(t - t_0) + Z_0 \cdot I_{L0} \sin(\omega_0 (t - t_0)) \\ &= (V_{in} - V_o) + V_o \cos(t - t_0) + Z_0 \cdot I_{L0} \sin(\omega_0 (t - t_0)) \end{aligned} \tag{3.41}$$

$$I_{Lb}(t) = (V_{in} - V_o) + Z_0 \cdot I_{L0} \cdot \sin(w_0 \cdot t_{dead}) \tag{3.42}$$

Using the initial conditions $I_{Lb}(0) = I_R$ and $V_{C,eq}(0) = V_{link}$, Equations (3.41) and (3.42) are solved for time t_1 at which $V_{C,eq} = 0$. Equation (3.41) is solved to do so, using numerical methods, in MATLAB. The result is explained in the next subsection, using Figures 3.14 and 3.15 as examples of solutions based on Equations (3.41) and (3.42).

COMBINATION OF i_R AND DEAD TIME

The equivalent output capacitance C_{eq} needs to be charged/discharged within t_{dead} to ensure ZVS turn-on. However, not all combinations of I_R and t_{dead} will lead to a successful ZVS turn-on. Intuitively it might appear that, by increasing t_{dead}, one could always achieve ZVS, irrespective of I_R. However, this is not the case: by plotting Equations (3.41) and (3.42) it can be seen that C_{eq} is not always fully charged/discharged for every combination of t_{dead} and I_R (see figure 3.14). If the voltage in the right side of Figure 3.14 is able to reach V_c =0 V, ZVS turn-on can occur. On the right of the same figure the corresponding current waveform, based on Equation (3.42), is plotted. Note that the resonance for the lowest values of I_r result in unsuccessful discharging in this case in Figure 3.14.

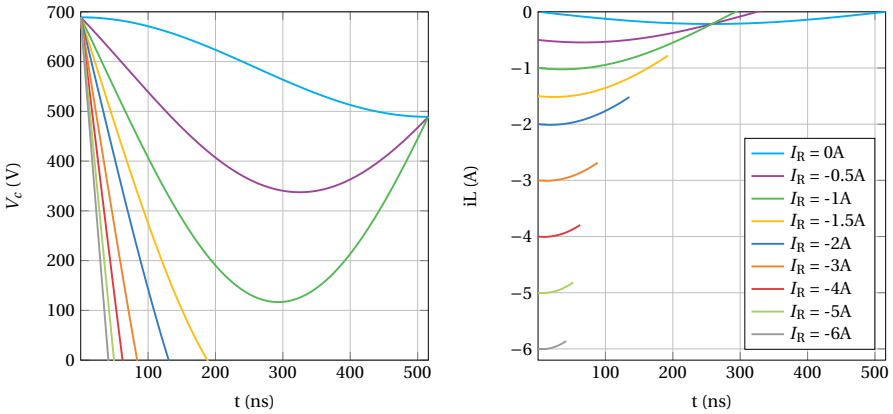


Figure 3.14: Voltage across the equivalent capacitance of Figure 3.12, and current through the inductor in the resonant interval during t_{dead}. V_{in}=689 V, V_o=100 V, C =355 pF, L =75.8 µH. The legend on the right applies to both figures.

An interesting phenomenon occurs when the duty cycle $D \geq 0.5$; any value of $-I_R$ is capable of completing the discharging/charging of the equivalent capacitance C_{eq}. This phenomenon is illustrated in Figure 3.15. This also signifies that one could implement a variable $t_{dead}/-I_R$ scheme to minimize conduction losses throughout the entire operating range of the converter.

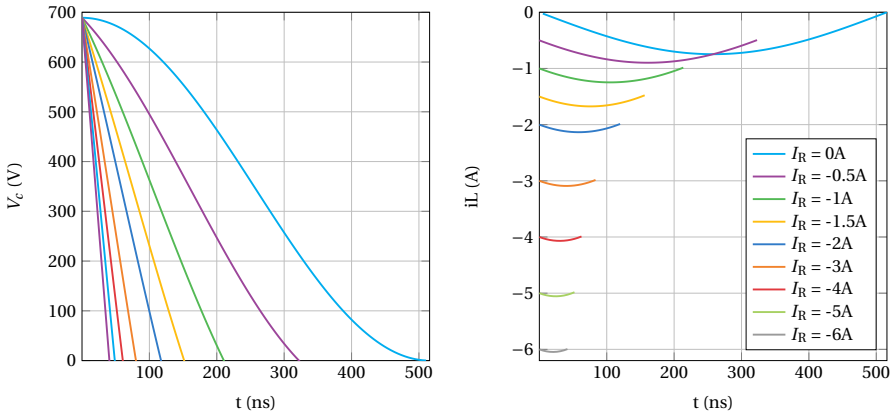


Figure 3.15: Voltage across the equivalent capacitance of Figure 3.12, and current through the inductor in the resonant interval during t_{dead}. V_{in}=689 V, V_o=344.5 V, C =355 pF, L =75.8 µH. The legend on the right applies to both figures.

3.3. VERIFICATION ANALYTICAL MODEL

The validity of Equations (3.24) and (3.38) are verified by comparing them to an LTSpice simulation of the same circuit. Different operation points are tested by varying I_o while keeping V_o constant to simplify the resulting figures in Figure 3.16. The testing conditions are listed in Section 3.3, and the results are shown in Figure 3.16. To test the effect of interleaving, N_{phase} buck converters are interleaved during the comparison (see Section 3.3).

Parameter	**Value**
V_{in}	525 V
V_o	305 V
N_{phase}	2
f_{min}	15 kHz
L_b	75.59 µH
C_{out}	30 µF
t_{dead}	100 ns

Table 3.2: Selected conditions to compare the Interleaved TCM Buck converter Analytical model with the LTSpice simulation model.

Figure 3.16 shows that the Analytical model of the Interleaved TCM Buck converter in MATLAB and its Simulation model in LTSpice lead to almost identical results. The used analytical model is therefore deemed valid.

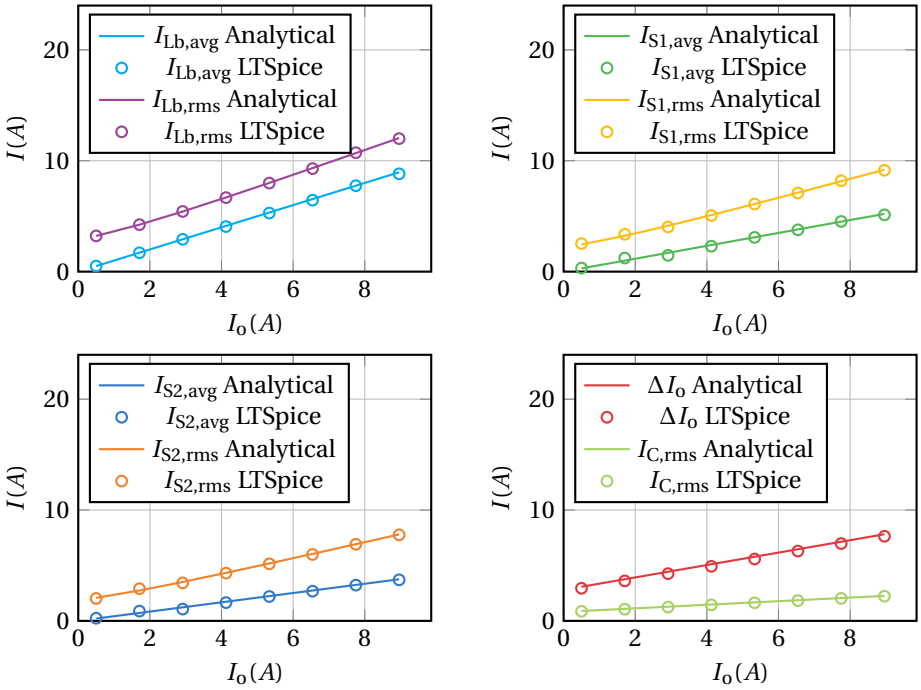


Figure 3.16: Comparison of the Analytical Interleaved TCM Buck converter model and the LTSpice Simulation.

4

Procedure for Topology Comparison

There are multiple possible configurations to implement the two-stage converter proposed in Chapter 2. One element will be used in any configuration: the two-stage converter will be equipped with a Voltage Doubler (VD)/Current Doubler (CD). This is beneficial, when the wide output voltage range of 150-1000 V is considered: the efficiency of the Buck converter decreases with decreasing duty cycle D. If this range can be reduced by half by using three relays as VD/CD structure, the maximum efficiency can be achieved twice in the whole output voltage range. This is especially advantageous, since both the 400 V as well as the 800 V battery architectures, discussed in Chapter 1, can be charged with similar efficiency. This effect of reaching the peak efficiency twice will become evident in the next chapter, for example in Figure 5.9. Moreover, this VD/CD structure can be implemented either in front of, or behind Interleaved TCM Buck converter. This will lead to two possible Configurations, which is the topic of discussion in Section 4.1.

4.1. Topology Configurations

In this study, two possible Configurations of the two-stage converter can be implemented. See Figures 4.1 and 4.2 for the proposed Configuration One and Configuration Two, respectively. As discussed before, the difference between these two Configurations lies in the order of arrangement of the VD/CD structure and the Interleaved TCM Buck converters. The location of the VD/CD structure results in different requirements for the voltage class rating of the switching devices in the Interleaved TCM buck converters, as shown in Table 4.1.

In general, a higher voltage class switch requires a longer n-doped drift layer (for N-channel MOSFETs), resulting in a larger $R_{ds,on}$ [51]. This causes more losses in the MOSFET (see Equation (A.9)). Therefore the efficiency would be lower when using a higher voltage class MOSFET in the same operating environment as a lower voltage class MOS-

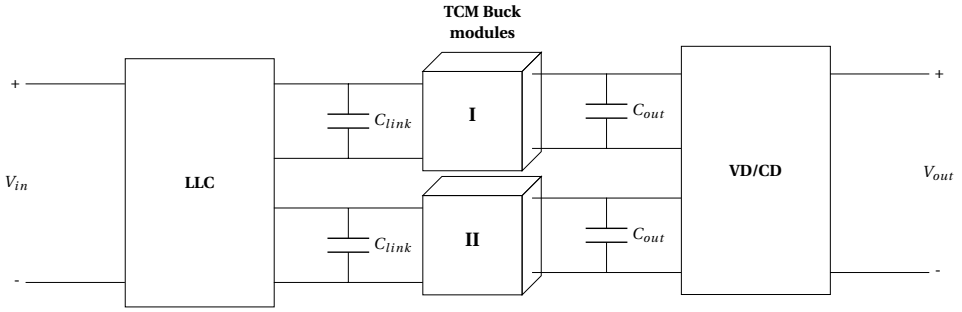


Figure 4.1: Configuration One (C1): two modules of N_{phase} Interleaved **TCM!** (**TCM!**) Buck converters followed by a VD/CD structure implemented by three relays.

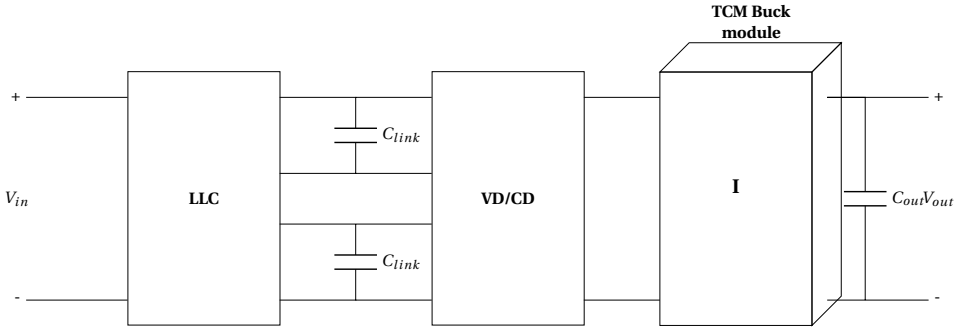


Figure 4.2: Configuration Two (C2): the VD/CD structure implemented by three relays followed by one module of N_{phase} Interleaved TCM Buck converters.

Table 4.1: Input voltages to the Interleaved TCM buck converters in the two different Configurations.

	Configuration One	**Configuration Two**
Input Voltage V_{in}	525-689 V	1050-1378 V
Required Voltage class rating	900 or 1200 V	1600 V

FET. This assumption, however, needs to be verified. Therefore a method needs to be devised to compare the performance of both Configurations operating in a real-world scenario. This method is devised in Section 4.2. Several combinations of Configuration, N_{phase} and $f_{\text{sw,min}}$ will be compared in this study (see Table 4.2). The results are discussed in Chapter 5.

Table 4.2: The combinations of Configuration and N_{phase} that will be compared in this study. ** Only the IGBT version; the current rating for the selected MOSFET does not allow for $N_{phase} = 1$.*

	$N_{phase} = 1$	$N_{phase} = 2$	$N_{phase} = 3$	$N_{phase} = 4$
Configuration One	X*	X		
Configuration Two		X	X	X

4.2. METHOD OF EFFICIENCY COMPARISON

The efficiency of a particular topology can be compared in multiple ways. Two common methods are to compare the peak efficiency or the full-load efficiency. However, both comparison methods do not reflect the efficiency during a charging cycle that would occur during the actual use of a converter for EV charging. Therefore, in this paper, the time-average efficiency of the proposed converter over the entire charging cycle is used to compare the efficiency of different topology solutions. This time-average efficiency is calculated by Equation (4.1)

$$\bar{\eta} = \frac{1}{t_{end}} \int_0^{t_{end}} \eta(t)\, dt \tag{4.1}$$

4.2.1. SELECTING CHARGING PROFILES

The majority of EV's on the road today are equipped with 400 V battery architectures. The Tesla Model 3 is the most registered EV in the Netherlands [52], and is therefore selected to represent a 400 V battery architecture in this study. The Porsche Taycan is chosen to represent the 800 V battery architecture. Almost all EVs, including these two, use lithium-ion battery cells in their battery packs. These generally have a nominal voltage of 3.7 V and a maximum of 4.2 V [53], which will be used in the charging simulations. The specifications of the battery packs are listed in Table 4.3.

Table 4.3: Key characteristics required to construct the charging cycle of the Tesla Model 3 [54] and Porsche Taycan [55].

	Tesla Model 3	**Porsche Taycan**
Number of cells	2976 (*96s31p*)	396 (*198s2p*)
Nominal V_{bat}	355.2 V (3.7 · 96)	723 V(3.7 · 198)
Maximum V_{bat}	403.2 V	831.6 V
Minimum V_{bat}	273.6 V(2.85 · 96)	564.3 V(2.85 · 198)
Battery Capacity	53.1 kWh	93.4 kWh

The two-stage converter prposed in this study is designed specifically to serve both 400 V and 800 V battery architecture EVs. The efficiency of the following charging cycles is measured:

- **Case Ia**: A single converter (11 kW) directly charging a 400 V battery.
- **Case Ib**: A single converter in a stack of five converters (55 kW) charging a 400 V battery.

- **Case IIa**: A single converter (11 kW) directly charging an 800 V battery.
- **Case IIb**: A single converter in a stack of five converters (55 kW) charging an 800 V battery.

Important to note is that in the 55 kW charging cycles, all individual converters in the stack of five converters output the same current and voltage. This simplifies the charging cycle of an individual converter, because their charging profiles are identical. One could also consider different strategies such as a modular structure where at a particular output power one converter after another is shut down until the charging process is fully complete.

Data from Table 4.3, in combination with a battery charging cycle script (created for this study), was used to simulate a CC-CV charging profile. The constraints set on these charging cycles are listed in Table 4.4.

Table 4.4: Constraints on a *single* charger used to simulate the charging profiles of all four cases.

Constraint	**Value**
I_{max}	30 A
P_{max}	11 kW
Charging strategy	CC-CV

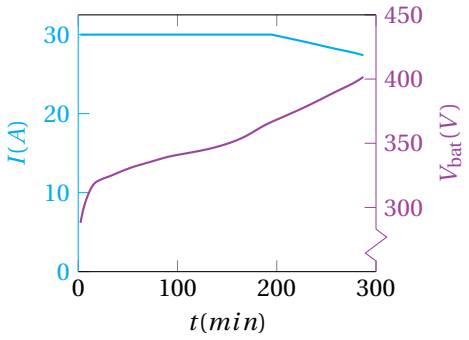
Figure 4.3 shows the four resulting charge cycles that belong to each use case (Ia, Ib, IIa, IIb) discussed in the beginning of this section. Note from Figure 4.3 that at 11 kW, both batteries reach full capacity through only the CC phase. This charging rate is so low ($I < 1C$) that the CV phase is never reached. P_{max} is reached at $V = 11000/30 = 367$ V for Case Ia, which requires I_o to reduce from that point on (see Figure 4.3a).

The theoretical efficiency of the converter is calculated at discrete operation points (V_o and I_o combinations) in MATLAB. The losses that are taken into account are (as calculated in Appendix A):

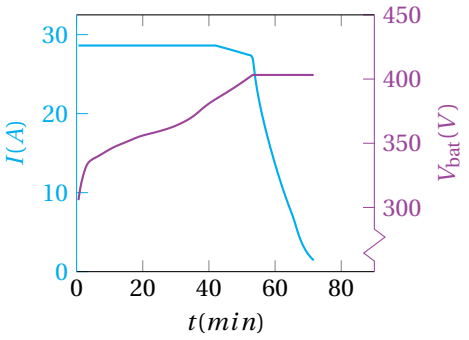
- Semiconductor Losses
  - Primary side switching losses
  - Primary side conduction losses
  - Secondary side conduction losses (rectifier)
- Magnetic Losses
  - Transformer core losses
  - Transformer winding losses (including skin and proximity losses)
  - Resonant inductor core losses
  - Resonant inductor winding losses (including skin and proximity losses)

The theoretical losses are calculated separately for both the LLC converter and the Interleaved TCM Buck converter (see Appendix A). This results in two efficiency maps, one for each converter. The efficiency map of the LLC converter is shown as an example in Figure 4.4.

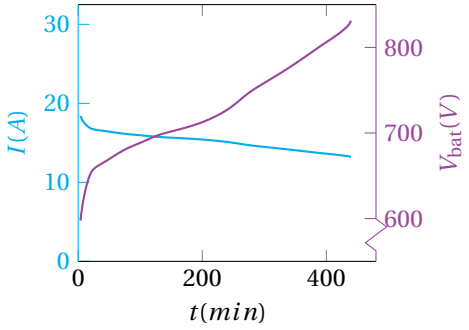
Since information about the efficiency is only calculated for discrete operating points, Equation (4.1) needs to be rewritten in discrete form. The continuous integral will be replaced using the trapezoidal rule, see Equation (4.2).



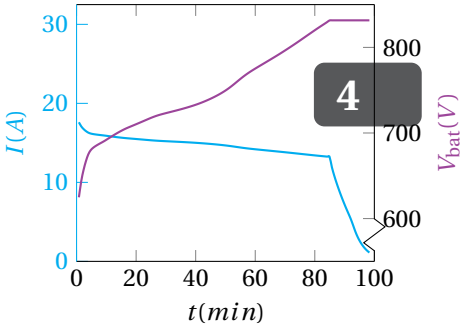
(a) Case Ia: Single 11 kW converter charging a 400 V battery.



(b) Case Ib: Single 11 kW converter in a stack of five charging a 400 V battery.



(c) Case IIa: Single 11 kW converter charging a 800 V battery.



(d) Case IIb: Single 11 kW converter in a stack of five charging a 800 V battery.

Figure 4.3: All four charging cycles upon which the charging cycle efficiency is based. All five converters in the 55 kW Configuration have equal output of voltage and current at any time, as such the charging profiles are equal and the charging profile of one single converter in this stack of five is shown.

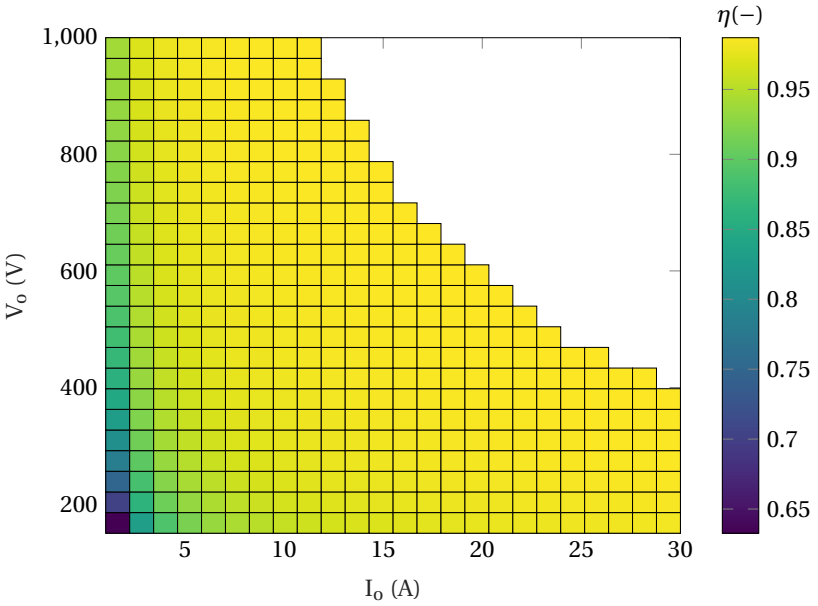


Figure 4.4: Theoretical efficiency of the LLC converter over the entire allowed operating range ($I_{o,max}$ =30 A, P_{max} =11 kW).

$$\bar{\eta} = \frac{1}{t_{end}} \sum_{n=0}^{N-1} \frac{1}{2} (\eta_n + \eta_{n+1})(\Delta t)_n \tag{4.2}$$

η is the discrete point in Figure 4.4 closest to the particular point on the charging cycle simulation from Figure 4.3. N is the total number of data points and t_{end} the time at which the charging process is complete. The efficiency of each operation point during a particular charging cycle is determined by the closest operation point on the discrete efficiency map Figure 4.4. To better understand the relation between Figure 4.3 and Figure 4.4, one could superimpose the first figure on the latter. An example of this is shown in Figure 4.5 for Case Ia and IIb.

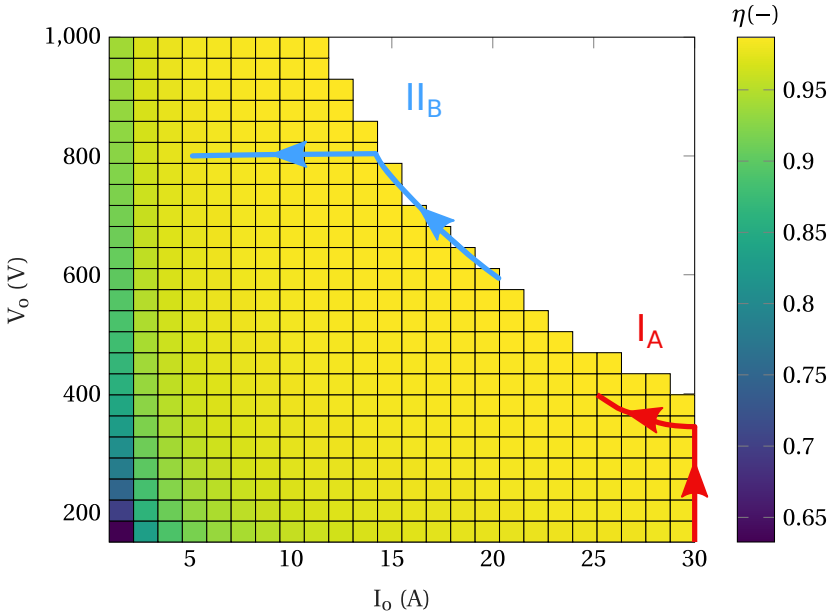


Figure 4.5: Example of the two charging cycles (see Section 4.2.1) imposed on the efficiency map of one converter.

4.3. SWITCH SELECTION

The switches available for both Configurations One and Two will have a crucial role. It is the main difference distinguishing Configuration One and Two from each other. This is because the properties of the switches play an important role in determining the losses, and thereby the efficiency of the converter. Because of this, the switches are selected upfront. Contrary to the magnetic component design procedure outlined in Appendix B, and all other component selections made later in Chapter 6. The maximum voltages are listed in Table 4.2. The required current rating for the LLC and Interleaved TCM Buck converters is determined in Sections 4.3.1 and 4.3.2.

4.3.1. LLC CONVERTER

The current rating of the LLC primary side switches is independent of the two proposed Configurations. The average switch current can be approximated by using known input values (see Equation (4.3)). In Equation (4.3), an ideal transformer and also a lossless C_r and L_r are assumed.

$$\hat{I}_{sw,avg} = \frac{1}{2} \cdot \frac{P_{max}}{V_{in,min}} \tag{4.3}$$
$$\hat{I}_{sw,avg} = \frac{1}{2} \cdot \frac{11000}{640} = 8.59A$$

An approximation is made for the current through the primary side switches. Specifi-

cally that at P_{max} each switch conducts exactly the positive half of a sine wave. However, in reality, there is still a small portion of time when the current through the switch is negative at full power. Taking this approximation, the RMS current through the switch is given by Equation (4.4).

$$\hat{I}_{sw,rms} = \frac{\pi}{2} \cdot \hat{I}_{sw,avg} = 13.5A \tag{4.4}$$

Since approximations were made to arrive at $\hat{I}_{sw,rms}$, a large safety margin is used for the rating required by the switches: $\hat{I}_{sw,rms} = 1.5 \cdot 13.5 = 20.25$ A. 1200 V MOSFET and IGBT devices that fit these requirements from the MOUSER catalog are compared in Table 4.5. Based on Table 4.5 the following switches are selected:

- LLC IGBT version: IKW40N120CS6 from Infineon [56].
- LLC MOSFET version: IMW120R060M1 from Infineon [57].

Table 4.5: Switch selection for 1200 V rated switches. **: conditions; V_{ce} =600 V, V_{ge} =15/0 V, T_j = 175 °C (except DGTD120T40S1PT, which had T_j = 150 °C) and R_g as the standard mentioned on each respective datasheet. **: Since the loss of the IGBT depends on two terms, $I_{sw,avg}$ =8.59 A and $I_{sw,rms}$ =13.5 A is used along with equation (A.17) to calculate the total conduction loss. †: V_{ds} =800 V, T_j =175 °C, and R_g & V_{gs} as the standard values listed on each respective datasheet.*

	Switch Type	**Price (€)**	$I_{c,max}$ at T_c=100 °C	$V_{ce,on}(V)$ at V_{ge} =15 V, T_j = 175 °C	$R_{ce,on}(m\Omega)$ at V_{ge} =15 V, T_j = 175 °C	$E^{*}_{off}(mJ)$	$P^{**}_{cd,tot}$
IGBT	IKW40N120CS6	7.60	40	1.18	28.5	1.66	15.32
	IKW25N120T2	5.31	25	0.84	55.1	1.75	17.28
	IKW25N120CS7	4.62	37	1	38.2	2	15.56
	IKW15N120CS7	3.88	25	1	63.4	1.87	20.15
	RGS50TSX2DHR	7.69	25	1.18	47	1.6	18.66
	STGW25M120DF3	5.77	25	1.17	38.3	1.6	17.01
	FGH25T120SMD	4.75	25	1.05	37.1	0.9	15.78
	DGTD120T40S1PT	7.56	40	1.31	26.4	0.96	16.09
			$I_{ds,max}$ at T_c = 100 °C		$R_{ds,on}(m\Omega)$ at V_{gs} =15 V, T_j = 175 °C	$E^{\dagger}_{off}(\mu J)$	
MOSFET	AIMW120R080M1	17.97	24		98	125	
	AIMW120R060M1H	15.20	26		76	112	
	AIMW120R045M1	19.51	28		55	71.4	
	IMW120R060M1	10.54	26		76	69.7	
	E3M0075120D	15.48	23		107	179	
	C2M0080120D	13.77	24		123	80	

4.3.2. INTERLEAVED TCM BUCK CONVERTER

The switches for the LLC converter were selected in the previous section. Now the selection of switches for the Interleaved TCM Buck converter is made. The maximum output current is $I_{o,max} = 30\,A$. Since $N_{phase} \geq 2$ (see Table 4.2), the average output current of a single buck converter is therefore maximum 15 A. Using Equation (3.27) and estimating $I_R = 5\,A$, the following calculation can be made:

$$I_{L,pkpk} = 2 \cdot (15+5) = 40A$$
$$k_1 = \frac{5}{40}$$

The result above is used to calculate the maximum current stress of the Interleaved TCM Buck converter switch. This is done using Equation (3.32) and taking the most conservative value for D, $D = 1$ (note that this is not physically possible, but is the worst case in this formula):

$$I_{S1,rms} = \sqrt{\left(5\sqrt{1\frac{0.125}{3}}\right)^2 + \left(35\sqrt{1\frac{1-0.125}{3}}\right)^2} = 18.93A$$

A margin of 30% is taken again. This results in $\hat{I}_{sw,rms} = 1.3 \cdot 18.93 = 24.6A$.

The requirements for the switches in the Interleaved TCM buck converter in Configuration One are equal to the requirements for the switches of the LLC converter. Therefore the same two switches are selected: as IGBT the IKW40N120CS6 [56] and as MOSFET the IMW120R060M1 [57].

The voltage rating for the switches in Configuration Two is 1700 V, as presented in Table 4.1. This limits the amount of available switches when compared to the more widely available 1200 V class switches. The available options are listed in Table 4.6. No suitable options of 1700 V IGBTs were found.

Table 4.6: Overview of the specifications of the available 1700 V rated MOSFETs.

	Switch Type	**Price (€)**	$I_{DS,max}$ at T_j =100 °C	$R_{ds,on}$ (mΩ) at T_j =150 °C, I_{DS} =30 A	E_{off} (µJ) at T_j =150 °C, I_{DS} =20 A
MOSFET	C2M0080170P	32.09	27	155	100
	C2M0045170D	72.01	48	84	240

5

RESULTS OF COMPARISON

The procedure outlined in Chapter 4 is used to determine the final solutions of both the LLC converter (in Section 5.1) and the Interleaved TCM Buck converter (in Section 5.2). The reader is encouraged to look back at Figures 4.1 and 4.2 to observe the difference in the configurations of the Interleaved TCM Buck converter in order to better understand Section 5.2.

5.1. LLC CONVERTER RESULTS

The operating frequency of the LLC converter is fixed to $f_{sw} = 15\,\text{kHz}$ in this study. As explained in Chapter 1, this is done in order to make a direct comparison with an a 11 kW PSFB EV charger possible.
The efficiency of all four charging cycles mentioned in Section 4.2.1 has been determined for both the MOSFET- and the IGBT-type LLC converter. The following switch configurations are compared, all using the same transformer design to make a fair comparison:

- IMW120R060M1 MOSFET switches
- IKW40N120CS6 IGBT switches
- IKW40N120CS6 IGBT switches and additional 4.5 nF snubbers

Table 5.1: Efficiency and Losses of the 11 kW LLC converter using either a MOSFET or an IGBT as switch (V_{in} =840 V). The average losses are measured over the 55 kW-400 V charging cycle (Case Ib), as an example.

Switch Type	**Snubber**	**Charge Cycle Efficiencies ($\eta(-)$)**					**Average losses of switch device in (55 kW-400 V) charging cycle**		
		11kW 400V	55kW 400V	11kW 800V	55kW 800V	**AVG**	$\bar{P}_{sw}(W)$	$\bar{P}_{cd}(W)$	$\hat{P}_{tot}(W)$
IMW120R060M1	-	0.9799	0.9787	0.9798	0.9795	**0.9795**	5.11	45.15	**50.26**
IKW40N120CS6	-	0.9796	0.9763	0.9795	0.9783	**0.9784**	23.11	34.28	**57.39**
IKW40N120CS6	4.5 nF	0.9809	0.9787	0.9809	0.9801	**0.9802**	8.73	34.80	**43.53**

The results of the comparison are presented in Table 5.1.Table 5.1 shows that the MOSFET is (by a thin margin) the most efficient option when the IGBT is not equipped with a snubber. However, when the IGBT is equipped with a 4.5 nF snubber it outperforms the MOSFET. The total transformer losses are not listed, but are almost equal independent of the used device. An exception to this is the IGBT version equipped with snubbers; the magnetizing inductance L_m needed to be lowered to still allow for ZVS. This results in slightly higher winding losses due to increased current through the winding (<1 W).

The loss distribution of three different switch configurations is shown in Figure 5.1. The charging cycle of Case Ib is used as an example in this figure. Note the difference in P_{cd} and P_{sw} between the MOSFET and IGBT, and also the effect of adding snubbers on P_{sw} of the IGBT. Another point of view of the performance of the converter is obtained by plotting the efficiency of the converter versus P_o over the entire operating range. This is performed for both V_{in} = 640 V and V_{in} =840 V and displayed in Figure 5.2.

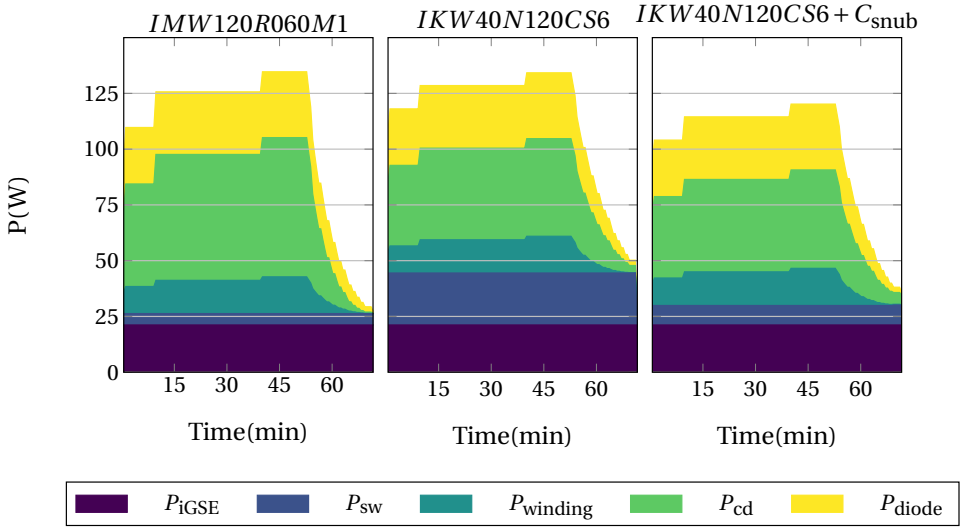
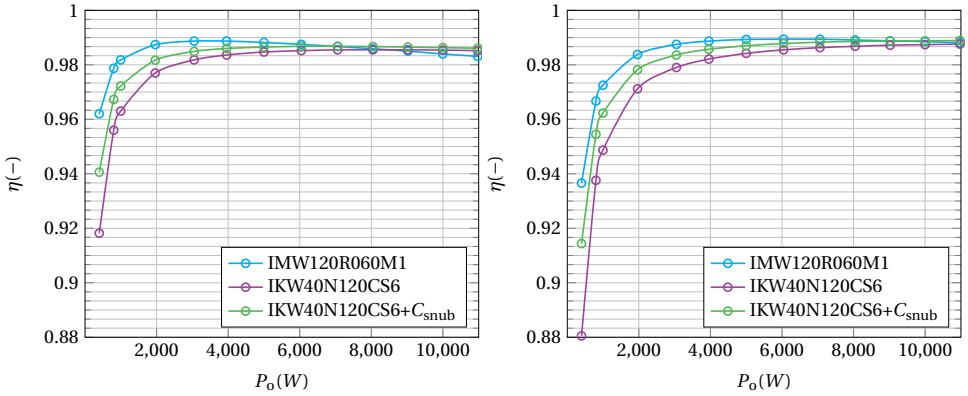


Figure 5.1: Composition of losses of one 11 kW LLC converter in Case Ib: 400V battery charged by a stack of five converters (V_{in} =840 V). Note the difference between the switching device types.

OBSERVATIONS

Some observations regarding Table 5.1 and figs. 5.1 and 5.2 are listed below.

- It is interesting to note that, based on Figure 5.2, the MOSFET version would be the most efficient solution. This is in contrast with what the data in Table 5.1 shows: that the IGBT+C_{snub} version is actually the most efficient solution if the efficiency is measured in terms of the proposed charging cycles. This is because the converter, independent of the charge cycles from Section 4.2.1, operates in maximum



(a) Efficiency when $V_{in} = 640V$.

(b) Efficiency when $V_{in} = 840V$.

Figure 5.2: Efficiency of the LLC converter over the entire operating range.

P_o for most of the time during the charging of an EV. Next to this, the point of maximum P_o is exactly the point where the IGBT+C_{snub} version is a little more efficient than the MOSFET version (see Figure 5.2).

- When looking at the differences between Figure 5.2a and Figure 5.2b it can be seen that in Figure 5.2a the IGBT gains even more advantage over the MOSFET at high P_o. Because V_{in} is lower, all currents for an 11 kW converter become higher. This causes more conduction losses, while the lower V_{in} reduces switching losses. The conduction losses for the MOSFET are higher per unit of current. This makes the IGBT an even better option.
- Figure 5.2a shows that at $P_{o,max}$ the IGBT without snubber has even lower losses when compared to the MOSFET.

5.1.1. FINAL LLC CONVERTER SOLUTION

To conclude the observations of Section 5.1, the final design of the LLC converter is chosen as the IGBT+C_{snub} solution. It is the most efficient solution, and second the IKW40N120CS6 switches are 25% cheaper when compared to the IMW120R060M1 switches. The specifications of this final solution are listed in Table 5.2. Additionally, The parameters of the magnetic components (resonant inductor L_r and the transformer) of this converter are listed in Table 5.3. The resonant inductor L_r and transformer were designed using the design procedure outlined in Appendix B.

Table 5.2: Final design specifications for the LLC converter. * *For the used charging cycles, see Section 4.2.1.*

Parameter Name	**Symbol**	**Value**
Switch Device	-	IKW40N120CS6 (4x)
Switching frequency	f_{sw}	15 kHz
Switch voltage class	V_{max}	1200 V
Price of the magnetics and switches	-	€118.72
Efficiencies*		
Case Ia	η_{11-400}	0.981
Case Ib	η_{55-400}	0.979
Case 2a	η_{11-800}	0.981
Case 2b	η_{55-800}	0.980
Peak Efficiency	η_{max}	0.989

Table 5.3: Design parameters of the resonant inductor L_r and the transformer of the selected LLC converter.

Theoretical Inductor Design		
Inductance	L_r	64.43 µH
EE Core Shape	-	EE70/33/32
# of stacked cores	n_{core}	1
Airgap length	l_g	1.3 mm
Maximum flux density	B_{max}	186 mT
# of turns	N	14
Theoretical Transformer Design		
Minimal magnetizing inductance	$L_{m,min}$	4.8 mH
EE Core Shape	-	EE70/33/32
# of stacked cores	n_{core}	5
Airgap length	l_g	0.3 mm
Maximum flux density	B_{max}	217 mT
# of primary side turns	N_{pri}	20
# of secondary side turns	N_{sec}	30 (2 · 15)

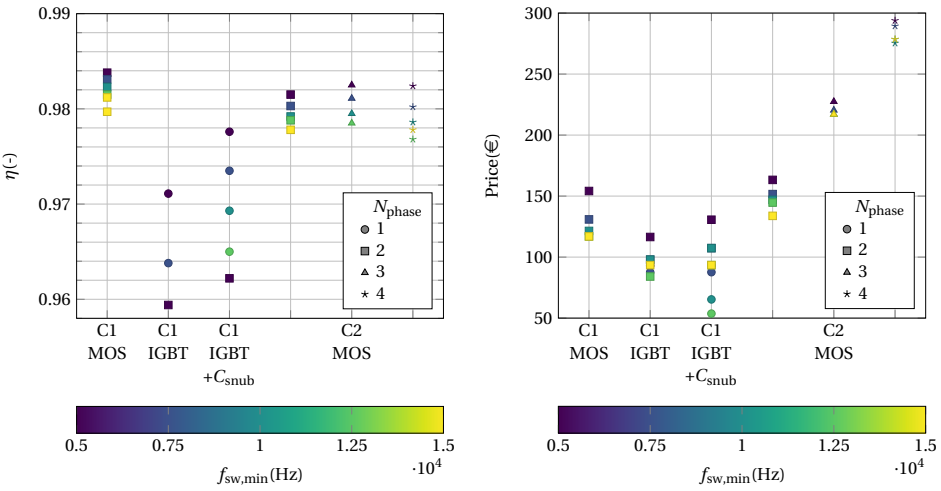
5.2. INTERLEAVED TCM BUCK CONVERTER RESULTS

The Interleaved TCM buck converter controls V_o by means of duty cycle D, and I_o by adjusting the switching frequency f_{sw}. The minimal frequency $f_{sw,min}$ determines L_b, which in term also sets the maximal switching frequency together with the chosen I_R. All configurations mentioned in Section 4.1 and their possible $f_{sw,min}$ and N_{phase} combinations are tested using the MATLAB model. This results in a range of different solutions (i.e. the '*solution space*'). The Interleaved TCM Buck converter was to be designed in a multi-objective design, focusing on (in order of importance):

1. Efficiency

2. Price
3. Power Density

The efficiency η of all solutions in the solution space is displayed in Figure 5.3a, the price in Figure 5.3b and the volume of the magnetic components in Figure 5.4. The price is composed of the price of the semiconductors and the magnetic cores. The power density is only represented by the size of the inductors used in a particular solution.



(a) Average efficiency η of **all four charging cycles** (see Section 4.2.1) for the solution space.

(b) Price in € of the different solutions.

Figure 5.3: Solution space of the different combinations of: Configurations One and Two, amount of N_{phase} and their $f_{\text{sw,min}}$.

In Figure 5.5 a closer look is taken into the distribution of losses between the most efficient solution *per switch type* of: Configuration, N_{phase} (taken from Figure 5.3a) and $f_{\text{sw,min}}$. Once again Case Ib is taken as an example of a charging cycle (see Section 4.2.1).

- IMW120R060M1 (Configuration One (C1 MOS)): $f_{\text{sw,min}} = 5\,\text{kHz}$, $N_{\text{phase}} = 2$.
- IKW40N120CS6 (Configuration One (C1 IGBT+C_{snub})): $f_{\text{sw,min}} = 5\,\text{kHz}$, $N_{\text{phase}} = 1$.
- C2M0080170P (Configuration Two (C2 MOS)): $f_{\text{sw,min}} = 5\,\text{kHz}$, $N_{\text{phase}} = 3$.

Judging from Figure 5.3a it would also be interesting to see difference in loss composition in Configuration Two for the different N_{phase}. To do this, the solutions with $f_{\text{sw,min}} = 5\,\text{kHz}$ are selected and the results are displayed in Figure 5.6.

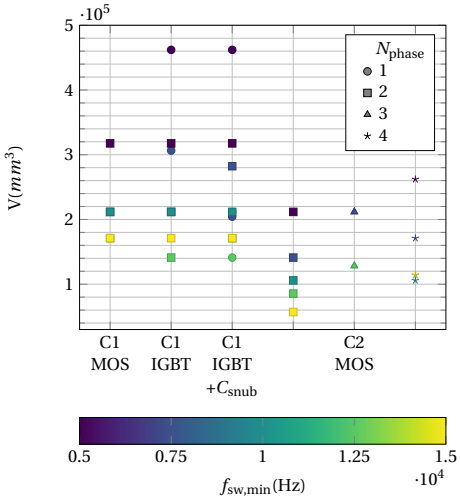


Figure 5.4: Volume of all magnetic components (i.e. inductors) for each solution in the solution space. Some solutions might overlap and therefore not be visible.

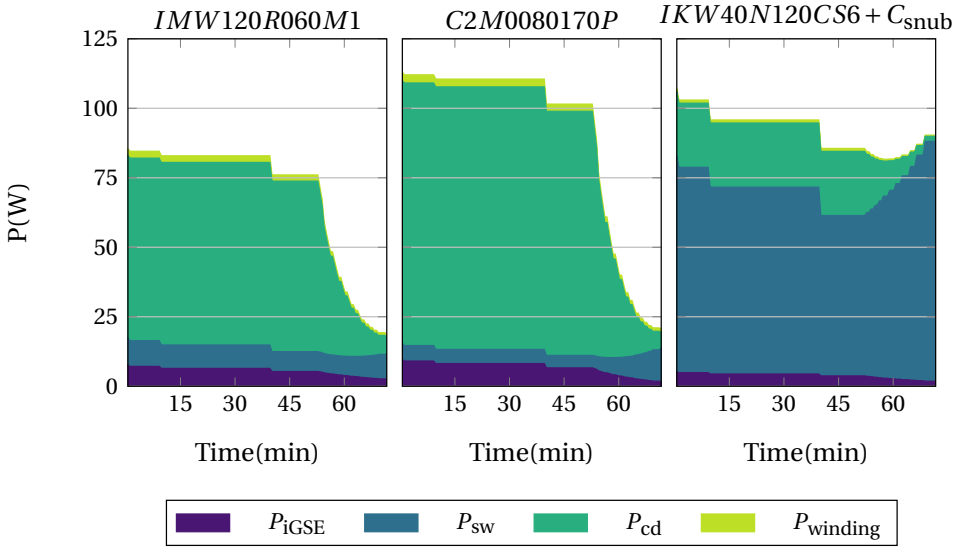


Figure 5.5: Loss composition of three of the most efficient solutions per device type (from Figure 5.3a). Charge cycle Case Ib (see Section 4.2.1) is used for this figure as an example. Configuration One MOSFET ($N_{phase} = 2$), Configuration Two ($N_{phase} = 3$), Configuration One IGBT+C_{snub} ($N_{phase} = 2$).

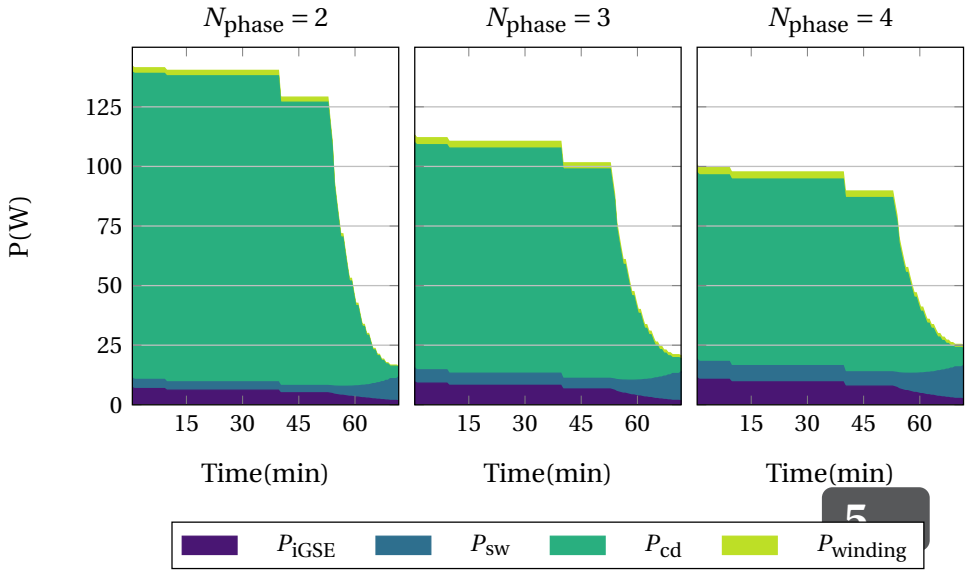


Figure 5.6: Loss distribution of Configuration Two solutions with $f_{sw,min} = 5\,kHz$. From left to right: $N_{phase} = 2$, $N_{phase} = 3$ and $N_{phase} = 4$. Once again Case Ib is taken as an example of a charging cycle (see Section 4.2.1).

OBSERVATIONS

Some observations regarding Figures 5.3a, 5.3b and 5.4 to 5.6 are listed below.

- Efficiency (η):
  - All MOSFET solutions are superior to the IGBT solutions in terms of efficiency η (regardless whether equipped with a snubber or not). Only the lowest $f_{sw,min}$ IGBT converter comes in the η range of the MOSFET solutions. This is in stark contrast with the results for the LLC converter (Section 5.1). The difference in results is based on the higher P_{sw} of the IGBT, as can be observed in Figure 5.5. The Interleaved TCM Buck converter operates at relatively high frequencies at low I_o (see Figure 5.8 and Equation (3.25)).
  - The 1200V IMW120R060M1 MOSFET solutions outperform the 1700V C2M0080170P MOSFET solutions of equal $f_{sw,min}$, as seen in Figure 5.3a.
  - The conduction losses for the MOSFET versions are dominant, as expected. This is clearly illustrated by Figure 5.6: when N_{phase} is increased, each individual buck converter phase handles less current (I_{rms} drops) and this results in lower conduction losses overall (see Equation (A.9)).
- Price
  - The difference between solutions from the *same configuration and switch device* lies in the cost of the magnetic components only: the solutions with $f_{sw,min}$ = 5 kHz have the largest magnetic components and thus the highest price.
  - The IGBT based solutions have the lowest price.
  - The 1700V MOSFETs from Configuration Two are three times more expensive than the 1200V MOSFETs, resulting in the Configuration 2 Two options to be the most expensive of all solutions.
- Power density: The power density of Configuration Two and $N_{phase} = 2$ is the highest due to only two inductors being required for these solutions. The largest volumes, and thereby lowest power densities, are required for the lowest $f_{sw,min}$ solutions.

5

5.2.1. FINAL INTERLEAVED TCM BUCK CONVERTER SOLUTION

Based on the analysis of the results in Section 5.2 the final design of the Interleaved TCM Buck converter is chosen: Configuration One: $N_{phase} = 2$, so two modules of two interleaved buck converters. Operating at $f_{sw,min}$ =15 kHz, using the 1200 V (IMW120R060M1) MOSFETs. This final design leads to the highest efficiency. This switching frequency $f_{sw,min}$ is chosen because the efficiency does not deteriorate considerably from 5 kHz, but the power density increases around two times (see Figure 5.4). On top of this, operating at 15 kHz allows the prototype to be tested without it emitting audible noise. In addition, this solution is the cheapest option as well among all MOSFET solutions, only surpassed by the low cost of the IGBT device solutions (see Figure 5.3b). A summary of the final design is given in Table 5.4.

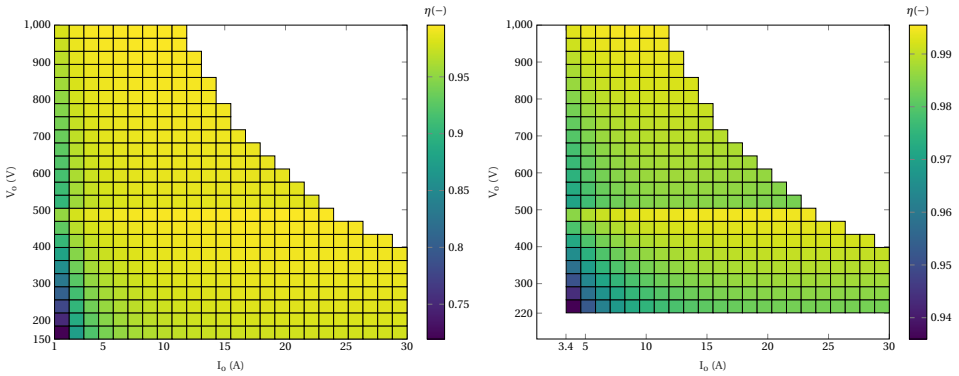
The efficiency of the selected solution over the entire operating range is shown in Figure 5.7a. This figure clearly displays the effect of the VD/CD structure on the efficiency of the Interleaved TCM Buck converter. Another important aspect of the operation of

Table 5.4: Final design parameters for the Interleaved TCM Buck converter. ** Not considering phase-shedding at low I_o.* *** For the used charging cycles, see Section 4.2.1.*

Parameter Name	**Symbol**	**Value**
Configuration	-	Configuration 1
Number of phases	N_{phase}	$2 \cdot 2 = 4$
Minimum switching frequency	$f_{sw,min}$	15 kHz
Maximum switching frequency*	$f_{sw,max}$	165 kHz
Switch Device	-	IMW120R060M1 (8x)
Switch voltage class	V_{max}	1200 V
Price of inductors and switches	-	€116.96
Efficiencies**		
Case Ia	η_{11-400}	0.982
Case Ib	η_{55-400}	0.980
Case 2a	η_{11-800}	0.982
Case 2b	η_{55-800}	0.982
Peak Efficiency	η_{max}	0.992
Theoretical Inductor Design		
Inductance	L_b	75.6 µH
EE Core Shape	-	EE70/33/32
# of cores	n_{core}	1
Airgap length	l_g	1.6 mm
Maximum flux density	B_{max}	248 mT
# of turns	N	12

the Interleaved TCM Buck converter is the switching frequency f_{sw}. This will vary not only with V_o, but also with I_o (as discussed in Section 3.2). Figure 5.8 shows the f_{sw} belonging to each operation point in the entire operating range. The design point $f_{sw,min}$ is indicated as well in the top of the figure.

Figure 5.9 shows the efficiency of the Interleaved TCM Buck converter for a set of specified values of I_o. The efficiency reduces significantly for the lower range of I_o values. This is expected due to the increase in f_{sw} (and therefore P_{sw}) as shown in Figure 5.8. Note that not all values of I_o are available at the maximum output voltage: the lines stop when maximum $P_o = 11$ kW is reached.



(a) Efficiency over the complete operating range.

(b) Zoom in of the efficiency, to allow for more contrast in higher P_o operating range.

Figure 5.7: Efficiency of the Interleaved TCM Buck converter solution with $V_{in} = 525\,V$.

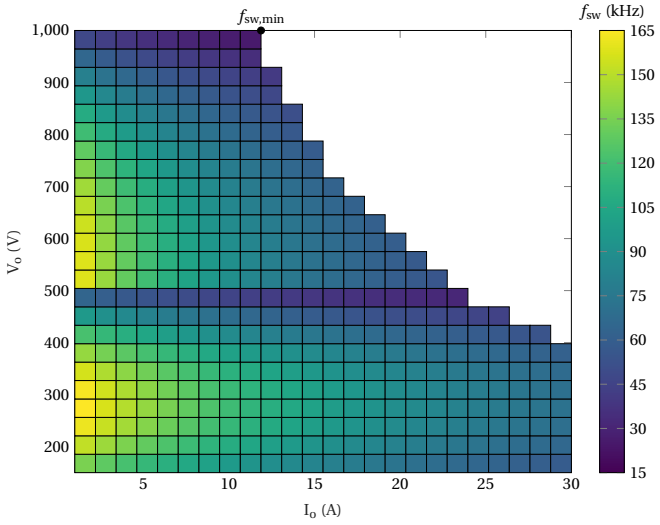


Figure 5.8: Operating f_{sw} of the Interleaved TCM Buck converter in the complete operating range with $V_{in} = 525\,V$.

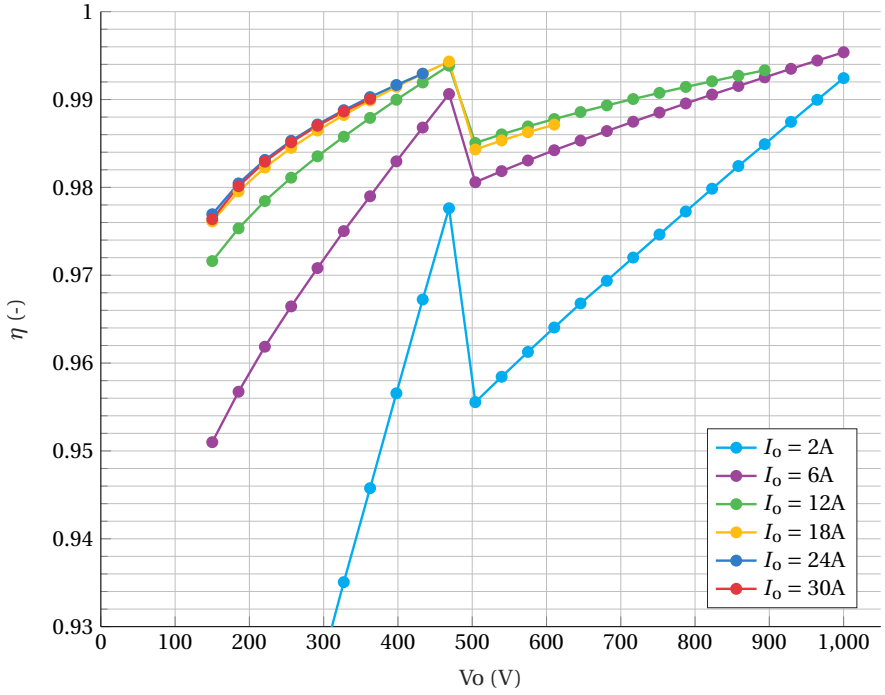


Figure 5.9: The efficiency of the TCM converter for different I_o over the entire V_o range (with $V_{in} = 525\,V$).

6

DESIGN

In order to verify the working and efficiency of the proposed design, a prototype has to be build. The semiconductor switches have already been selected in Chapter 5. Nonetheless, other components such as the DC-link capacitors, Rectifier Diodes, Resonant capacitors and relays have yet to be selected. On top of this, the procedure for the magnetic component design used to arrive at the designed inductors and transformers has not been explained in Chapter 5. The components in this chapter are dimensioned based on the worst-case stresses that apply to each component (see Section 6.1).

6.1. WORST-CASE COMPONENT STRESSES

6.1.1. LLC CONVERTER

The input voltage V_{in} to the LLC converter ranges from 640-840 V. However, the maximum output power is always P_o =11 kW. This results in the worst-case voltage stresses occurring at V_{in} =840 V, while worst-case current stresses occur at V_{in} =640 V. Therefore, Table 6.1 is split into two separate columns, one for worst-case stresses that occur at 640 V and one for worst-case stresses that occur at 840 V. These worst-case stresses are determined in MATLAB by the results of the analytical FHA model described in Section 3.1.

Table 6.1: All maximum stresses on all components of the LLC converter. Some maximum stresses occur at V_{in} =640 V (first column), while other maximum stresses occur at V_{in} =840 V (second column). ** This worst case voltage stress is determined in Section 6.3.1.*

$V_{in} = 640V$		$V_{in} = 840V$	
Parameter	**Value**	**Parameter**	**Value**
$I_{Lr,RMS}$	19.13 A	V_{sw}	840 V
$I_{Lr,max}$	27.05 A	$V_{TF,pri}$	840 V
$V_{Cr,max}$	*	V_{Clink}	689 V
$I_{sw,RMS}$	13.52 Arms		
$I_{sw,avg}$	8.60 A		
$I_{D,RMS}$	8.23 Arms		
$I_{D,avg}$	5.24 A		
$I_{DClink,RMS}$	5.06 Arms		

6.1.2. INTERLEAVED TCM BUCK CONVERTER

The Interleaved TCM Buck converter is subject to a variable input voltage (V_{link}), which is directly caused by the variable V_{in} of the LLC converter. Only the worst-case V_{sw} and maximum V_{Lb} occur at the maximum V_{link}. All other worst-case stresses occur at the minimal V_{link}. In Table 6.2 all worst-case stresses are displayed as determined using the analytical model in MATLAB. It is important to note that these are the worst-case stresses for a **single** buck converter.

Table 6.2: All maximum stresses on all components of the LLC converter. Some maximum stresses occur at V_{link} =525 V (first column), while other maximum stresses occur at V_{link} =689 V (second column).

$V_{link} = 525V$		$V_{link} = 689V$	
Parameter	**Value**	**Parameter**	**Value**
$I_{Lb,RMS}$	14.10 Arms	$V_{S1,max}$	689 V
$I_{Lb,max}$	26.54 A	$V_{Lb,max}$	689 V
$V_{Cout,max}$	500 V	$V_{S2,max}$	689 V
$I_{S1,RMS}$	9.77 Arms		
$I_{S1,avg}$	5.24 A		
$I_{S2,RMS}$	10.17 Arms		
$I_{S2,avg}$	5.60 A		
$I_{Cout,RMS}$	5.67 Arms		

6.2. MAGNETIC DESIGN

An iterative script is used to design the magnetic components; the transformer for the LLC converter and the inductors for both the LLC converter and Interleaved TCM buck converter. The input for the magnetic design scripts are the worst-case stresses for the magnetic components, shown in Tables 6.1 and 6.2. The iterative scripts iterate over the

following variables:

1. Magnetic core material.
2. Magnetic core size (EE cores).
3. Number of stacked cores.
4. Operating flux density ($0 < B_{op} < 0.8 B_{max}$).
5. Litz wire gauge and number of strands. *Only 600 strands AWG41 wire was available, therefore no loops were performed over this variable.*

A schematic representation of the iterative process of designing an inductor and a transformer is shown in Appendix B.

6.2.1. TRANSFORMER DESIGN

The operating frequency of the LLC converter is relatively low (f_{sw}= 15 kHz), as stated in Chapter 1. This naturally results in the requirement of large area-product cores. The iterative transformer design procedure uses some key formulas, starting from Faraday's Law in Equation (6.1).

$$V_L(t) = L\frac{di(t)}{dt} = \frac{d\phi(t)}{dt} \tag{6.1}$$

It should be realized that the magnetic flux in the core goes from $-\phi_{max}$ to $-\phi_{max}$ in $\frac{1}{2}T_{sw}$. This leads to Equation (6.2).

$$\int_0^{0.5\cdot T_{sw}} V_{in}\, dt = \Delta\phi_{pk,pk} \tag{6.2}$$

Evaluating the previous expression leads to the expression for the minimal number of turns in Equation (6.4).

$$\frac{V_{in}}{2\cdot N\cdot A_c\cdot f_{sw}} = 2\cdot B_{op} \tag{6.3}$$

$$N_{min} = \frac{V_{in}}{4\cdot A_c\cdot B_{op}\cdot f_{sw}} \tag{6.4}$$

6

(6.5)

An airgap might be required to lower the magnetizing inductance value L_m, required to satisfy ZVS requirements of the LLC converter. The relation between the airgap and the magnetizing inductance can be approximated by Equation (6.6).

$$L \approx \frac{N^2}{R_g} \approx \frac{N^2}{2\cdot l_{air}/\mu_0 A_c} \tag{6.6}$$

The number of secondary side turns N_{sec} is determined by the turns ratio n, shown in Equation (6.7).

$$N_{sec} = \frac{V_{link}}{V_{in}}\cdot N_{pri} \tag{6.7}$$

The winding losses are calculated in MATLAB based on the procedure described by Mühlethaler et al. (2012), and is not further elaborated upon in this work [58]. A brief description of how the the core losses are calculated is found in Appendix A.4.1.

6.2.2. INDUCTOR DESIGN

A similar iterative design procedure as used for the transformer (see Appendix B) is used for designing the four inductors of the Interleaved TCM Buck converter and the external resonant inductor $L_{r,ext}$ of the LLC converter. A few key equations of the design procedure used to arrive at the design in Table 5.4 are highlighted in Equations (6.8) to (6.11).

$$\oint \vec{H} \cdot d\vec{l} = N \cdot I \tag{6.8}$$
$$H_{core} l_e + H_{air} l_g = N \cdot I$$
$$\frac{B}{\mu_0}\left(\frac{l_e}{\mu_r} + l_g\right) = N \cdot I$$

Since μ_r is very large for magnetic materials, Equation (6.8) can be simplified into Equation (6.9).

$$B\frac{l_g}{\mu_0} \approx NI \tag{6.9}$$

The minimum number of turns can be calculated using Equation (6.10).

$$LI = NBA_c \tag{6.10}$$
$$N_{min} = \frac{LI_{max}}{B_{max} A_c}$$

Combining Equations (6.9) and (6.10) allows the airgap length l_g to be calculated, to achieve the required inductance in Equation (6.11).

$$l_g = \frac{LI_{max}^2 \mu_0}{B_{max}^2 A_c} \tag{6.11}$$

The winding losses are, again calculated in MATLAB based on the procedure described by Mühlethaler et al. (2012). The details of this are not further elaborated upon in this work [58]. A brief description of how the the core losses are calculated is found in Appendix A.4.1.

6.3. COMPONENT SELECTION

6.3.1. RESONANT CAPACITOR

The resonant capacitor is subject to the full transformer current. The maximum voltage amplitude across the capacitor is calculated using Equation (6.12).

$$V_{\text{Cr,max}} = \frac{1}{\omega C_r} \cdot \sqrt{2} I_{\text{Lr,rms}} \tag{6.12}$$

The maximum $I_{\text{Lr,rms}}$ follows from the design script and is equal to 20 Arms (see Table 6.1). $V_{\text{Cr,max}}$ does not depend on the capacitor bank configuration. The capacitor bank has to be designed in such a way that the maximum RMS current can be handled, as well as the maximum voltage that is accompanied with this current (see Equation (6.12)). The capacitor bank is arranged with N_{p} parallel capacitors to lower the RMS current on an individual capacitor. Additionally, N_{s} capacitors are placed in series to reduce the RMS voltage over each individual capacitor. See Figure 6.1 for a schematic of the capacitor bank.

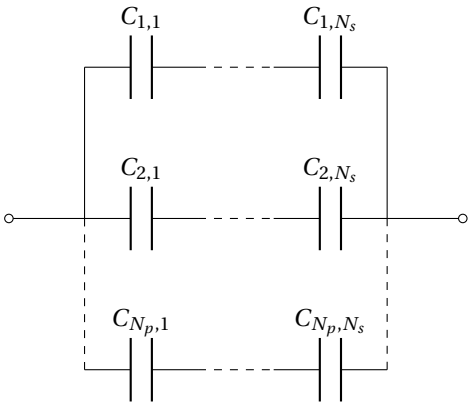


Figure 6.1: Structure of the resonant capacitor bank, consisting of N_s capacitors in series together with N_p capacitors in parallel.

After winding the LLC transformer, the primary-side referred leakage inductance L_σ needs to be measured. This leakage inductance might be instable, and therefore the external resonant inductance needs to be a multiple of L_σ to achieve stable operation in this prototype: $L_{\text{r,ext}} = 9 \cdot L_\sigma$. This is because total resonant inductance is consists of both: $L_{\text{r}} = L_\sigma + L_{\text{r,ext}}$. The primary side referred leakage inductance $L_\sigma = 6.3\,\mu$H. Using Equation (6.13) it is calculated that $C_{\text{r}} \approx 1500$ nF.

$$C_r = \frac{1}{(2\pi f_{\text{sw}})^2 \cdot L_{\text{r}}} \tag{6.13}$$

Several manufacturers have capacitors specifically designed for resonant circuits. Most often metallized polypropylene film capacitors are used by these manufacturers. The resonant capacitance series from three major manufacturers are:

- Panasonic : ECWH(C) [59]
- KEMET : R75H [60]
- TDK : B32641B ... B32643B [61]
- TDK : B32671L ... B32672L [62]

The R75H series is just released, and not yet available through suppliers. This leaves the ECWH(C) capacitances from Panasonic and the TDK capacitors. TDK offers a wider range of capacitance values. This means that more combinations are possible resulting in more possible C_r values of the resonant capacitor bank. The possible candidates for the capacitor bank are selected according to the procedure in Figure 6.2. When selecting a resonant capacitor, it is important to ensure they do not have to be derated at the required f_{sw} to minimize (dielectric) losses.

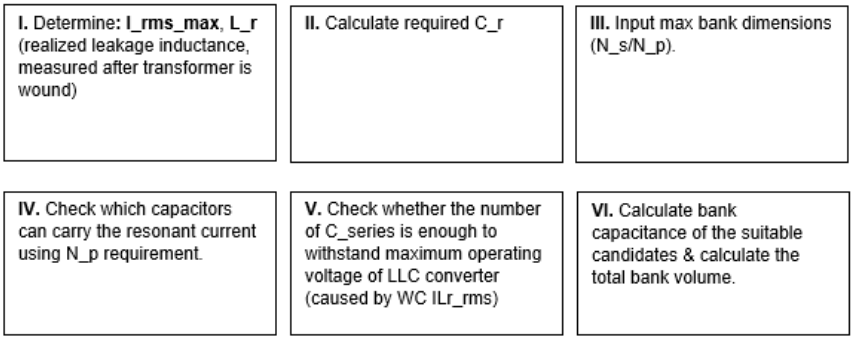


Figure 6.2: Selection procedure for finding suitable capacitors to use in the resonant capacitor bank.

Panasonic did not provide clear frequency voltage derating curves in their datasheet [59]. Therefore, a capacitor from one of the TDK series had to be selected. The selected capacitor is:

The **B32671L6473K000**: (47 nF). These capacitors have a DC voltage rating of 630 V, with no derating required at f_{sw}=15 kHz. The required voltage rating, using Equation (6.12), is only ≈200 V (peak). The number of parallel capacitors to achieve the required C_r is 33. The current rating of 20 Arms surpassed using this capacitor as well, with a current rating of 1 Arms each.

6.3.2. RECTIFIER DIODES

There are two secondary side windings on the high frequency transformer. A SiC Schottky diode is preferred due to the negligible reverse recovery current which allows for fast switching and reduced losses. The maximum average diode current occurs at the minimal V_{link} and maximum P_o and is given by Equation (6.14).

$$I_{D,avg} = \frac{1}{2}\frac{P_{o,max}}{V_{link,min}} = \frac{11000}{2 \cdot 1050} = 5.24A \tag{6.14}$$

And the RMS value for a half rectified sine wave is given by Equation (6.15).

$$I_{D,rms} = \frac{\pi}{2} \cdot I_{D,avg} \tag{6.15}$$
$$= 8.23\,\text{Arms}$$

A summary of the design requirements for the rectifier diodes is listed in Table 6.3.

Table 6.3: Design requirements for the LLC rectifier diodes.

Requirement	Value
Preferred Technology	SiC Schottky
V_{max}	689 V
$I_{avg,max}$	5.24 A
$I_{rms,max}$	8.23 Arms

The 1200 V rated IDW30G120C5B SiC Schottky Diode from Infineon is selected as the rectifier diode [63]. The maximum allowable current of these diodes is quite overrated (see Table 6.4). However, this allows the PCB to be reused for other purposes and results in lower losses in the rectifier.

Table 6.4: Specifications of the selected rectifier diode; IDW30G120C5B

Specification	Value
Technology	SiC Schottky
V_{max}	1200 VDC
$I_{F,max}$	30 A (150 °C)
$R_{th,jc}$	0.5 °C/W

6.3.3. DC-LINK CAPACITORS

LLC OUTPUT CAPACITOR

When the output voltage ripple is relatively small when compared with the output voltage it can be approximated by Equation (6.16).

$$V_{pk-pk} \approx \frac{I_{link}}{2 f_{sw} C_{int}} \tag{6.16}$$

The maximum voltage ripple in the DC-link after the LLC converter is chosen as $1V$ to ensure stable operation. The maximum load current to the Interleaved TCM Buck converter link capacitances is calculated using Equation (6.17).

$$I_{link,max} = \frac{P_{o,max}}{V_{link,min}} \tag{6.17}$$
$$= \frac{11000}{1050} = 10.48A$$

Therefore, the required DC-link output capacitance is given below, based on Equation (6.16).

$$\begin{aligned} C_{\text{int}} &= \frac{I_{\text{link}}}{2 f_{sw} V_{\text{pk-pk}}} \\ &= \frac{10.48}{2 \cdot 125000 \cdot 1} \approx 40\,\mu\text{F} \end{aligned}$$

The RMS current through the DC link capacitor bank is given by Equation (6.18).

$$\begin{aligned} I_{\text{Clink,rms}} &= \frac{P_{\text{o,max}}}{V_{\text{link,min}}} \sqrt{\frac{\pi^2}{8} - 1} \\ &\approx 5\,\text{Arms} \end{aligned} \tag{6.18}$$

The rest of the requirements are listed in Table 6.5.

Table 6.5: Design requirements for the LLC DC-link output capacitors.

Requirement	**Value**
C_{min}	40 µF
V_{max}	689 V
$f_{\text{r,min}}$	$2 \cdot f_{\text{sw,max}}$kHz
$I_{\text{rms,max}}$	5 Arms
$T_{\text{local,max}}$	60 °C

To make the PCB usable for other purposes as well, the DC-link capacitance is overdimensioned for the purposes of this project to be $2 \cdot 60uH$ per secondary side. The rest of the specifications are listed in Table 6.6.

Table 6.6: Specifications of the selected output capacitor C4AQIBW5600A3NJ.

Specification	**Value**
Manufacturer	KEMET
Series	C4AQ
Type	C4AQIBW5600A3NJ
Capacitance	60 µF (x2)
Voltage rating	800 VDC
ESR	3.3 mΩ (@10 kHz)
$I_{\text{RMS,max}}$	27.5 Arms (@ 10kHz)
R_{th}	10 °C/W
ESL	15 nH

INTERLEAVED TCM BUCK OUTPUT CAPACITORS

This section describes the selection process for the DC-link output capacitors. These capacitors will also be used on the input DC-link side for ease of design. The Interleaved TCM Buck converter generates a large output current ripple at a high frequency. Each of the two modules containing two phases (N_{phase}) has its own DC-link output capacitor, required for the VD configuration. First, the capacitor value of one DC-link output capacitor is determined based on the ΔV_o requirements. According to IEC61850 [14], a maximum of $10\,V_{\text{pk-pk}}$ is allowed for EV chargers. In order to fulfill this requirement by a substantial margin, $\Delta V_{\text{o,max}} = 4\,V_{\text{pk-pk}}$. The required capacitance is calculated using Equation (6.19).

$$C = \frac{\Delta Q}{\Delta V} = \frac{1}{\Delta V}\frac{1}{2}\left(\frac{1}{2}\cdot\Delta I_o\right)\cdot\left(\frac{1}{2}\frac{1}{2}T_{sw}\right) \tag{6.19}$$

The amount of charge ΔQ is determined geometrically judging from the interleaved current waveform (see Figure 6.3). T_{sw} is the switching frequency of a single phase. The worst-case ΔQ occurs at $\Delta I_{\text{o,max}} = 19.68\,\text{A}$ (worst-case ΔI_{o} given by MATLAB). This worst-case ΔI_{o} occurs at a frequency $f_{\text{sw}} = 7621\,\text{Hz}$.

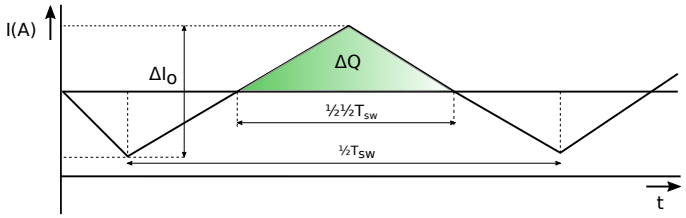


Figure 6.3: Output current ripple of one module, explaining the terms used in Equation (6.19). Note that this ripple is the product of two interleaved currents, and therefore one period in this figure equals $\frac{1}{2}T_{\text{sw}}$.

This results in a required $C_{\text{out}} = 20\,\mu\text{F}$. The maximum RMS current requirement is 5.67 Arms, calculated using Equation (3.38). The maximum switching frequency of the converter is 165 kHz. This means that the maximum frequency of the ripple current is 330 kHz since there are two parallel phases per C_{out}. The maximum output voltage per module is 500 V. To ensure proper operation of the converter, an output capacitor with a resonant frequency above 330 kHz has to be selected: this would require a low ESL (Equivalent Series Inductance) capacitor. Besides this, choosing a capacitor rated for a higher voltage than 500 V will increase the lifetime of the capacitor. According to IEC61850 the maximum ambient temperature $T_{\text{ambient,max}} = 40\,°\text{C}$ [14]. The local temperature near the capacitor on the PCB, though, might be higher and thus $T_{\text{ambient,max}} = 60\,°\text{C}$ is considered for the output capacitor. The design requirements are summarized in Table 6.7.

An important design parameter for the output capacitor is the hotspot temperature, which is the internal point in the capacitor where the maximum temperature is reached. This hotspot temperature (T_{HS}) is a determining factor in the lifetime of the capacitor, and is calculated using Equation (6.20) [64].

$$T_{\text{HS}} = T_{\text{ambient}} + R_{\text{th}}\cdot(ESR\cdot I_{\text{RMS}}^2) \tag{6.20}$$

Table 6.7: Design requirements for the Interleaved TCM Buck converter module output capacitors.

Requirement	Value
C_{min}	20 µF
V_{max}	500 VDC
$f_{r,min}$	330 kHz
$I_{rms,max}$	5.67 Arms
$T_{local,max}$	60 °C

The chosen C_{out} is from the DC-Link series C4AQ from KEMET corporation, of which the specifications are listed in Table 6.8. Two 15 µF are placed in parallel to achieve a capacitor bank of 30 µF per set of two buck converters.

Table 6.8: Specifications of the selected output capacitor C4AQILW4580A34J.

Specification	Value
Manufacturer	KEMET
Series	C4AQ
Type	C4AQILW5150A36J
Capacitance	15 µF
Voltage rating	800 VDC
f_r	433 kHz
ESR	6.2 mΩ (@10kHz)
$I_{RMS,max}$	13.7 Arms (@10kHz)
R_{th}	23 deg C/W
ESL	9 nH

Using Equation (6.20), it is calculated that T_{HS} = 62 °C (assuming ESR @ 10 kHz = ESR @330 kHz, and $T_{ambient}$ =60 °C). This hotspot temperature ensures a lifetime of 100 000+ hours according to the lifetime specification provided by the manufacturer in Figure 6.4.

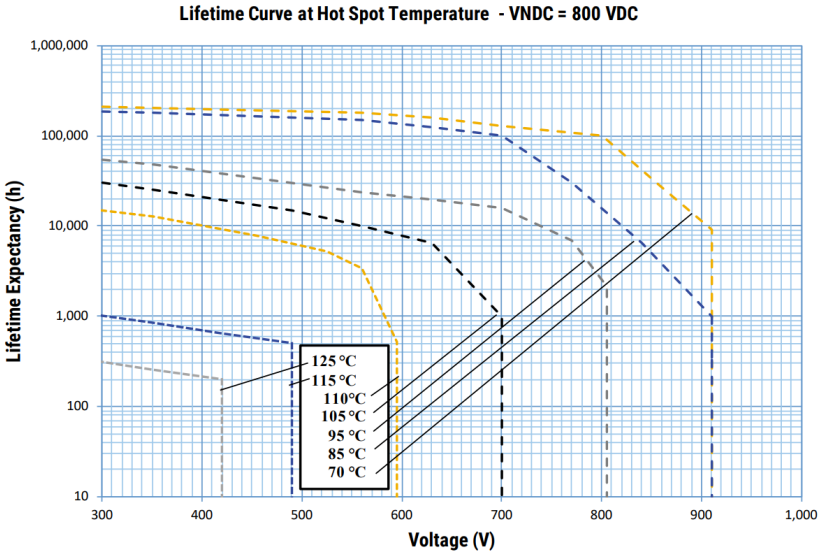


Figure 6.4: Lifetime of the C4AQILW5150A36J output capacitor [65]. Worst-case operation voltage is at 500 VDC, with a hotspot temperature below $T_{HS} = 70\,°C$.

6.3.4. POWER RELAYS

The VD/CD structure is implemented using power relays after the two modules of interleaved buck converters. These relays are only actuated pre-charging to their correct position and do not change position during the charging cycle. After all, they are solely implemented to accommodate both 400 V and 800 V battery architectures. The maximum load current carried occurs in VD configuration and is equal to the maximum output current I_o =30 A. The selected relay is from TE Connectivity; the TE-T9G is a 30 A rated NO relay, which can be operated using 5 VDC voltage. The specifications are listed in Table 6.9.

Table 6.9: Specifications of the selected relay used to implement the VD/CD structure.

Specification	Value
Manufacturer	TE Connectivity
Type	TE-T9G
Contact form	SPST-NO
Rated coil voltage	5 VDC
Rated load current	30 A
Dielectric strength between contacts	1500 V(RMS)
Dielectric strength between coil & contacts	4000 V(RMS)
Price	~€3.50

7

PRINTED CIRCUIT BOARD DESIGN

This chapter is intentionally kept concise and only describes the outline of the PCB design process. A few essential design choices are highlighted, and the functional groups of components and their location on the board are explained in this chapter.

The LLC converter can be implemented using an existing PCB previously used for a PSFB (as explained in Section 1.2.1). Only a resonant bank consisting of an external inductor $L_{r,ext}$ and the resonant capacitors forming C_r selected in Chapter 6 needs to be constructed. No PCB was yet available for the proposed Interleaved TCM Buck converter, and therefore the PCB design is included in the current study. The specifications from the PCB manufacturer Multi-CB are listed in Table 7.1. An image of the designed PCB is provided in Figure 7.1.

Table 7.1: Global parameters of the designed PCB.

Parameter	**Value**
Number of Layers	4
External Layers Copper thickness	2 Oz/ft^2
Internal Layers Copper thickness	1 Oz/ft^2
Size	191 mm x 270 mm
Material	FR4 1.55 mm

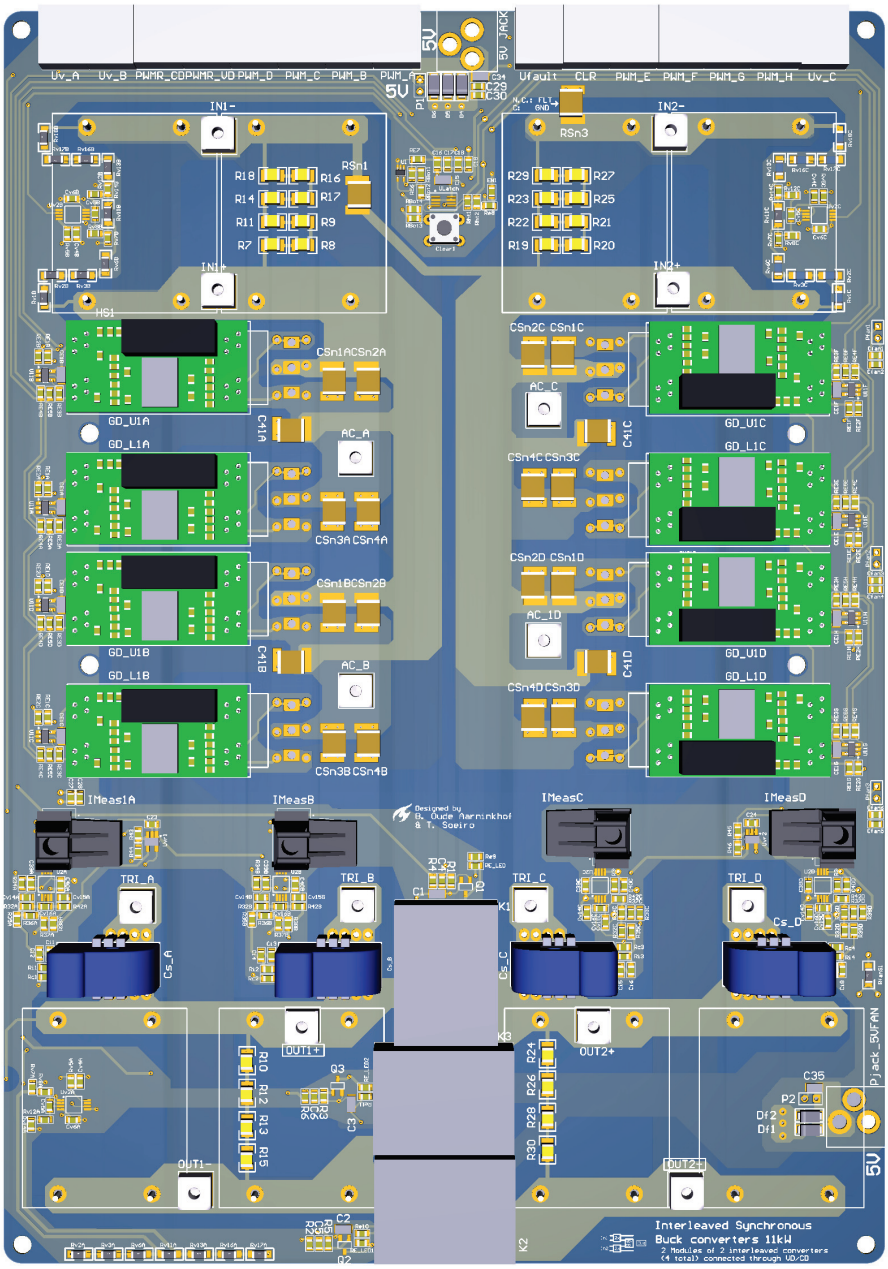


Figure 7.1: A render of the designed Interleaved TCM Buck PCB using Altium. For a specification of the different regions on this PCB, see Figure 7.2.

7.1. PRINTED CIRCUIT BOARD DESIGN CHOICES

The maximum voltage found on the PCB is V_{out} =1000 V. This has implications for the clearance and creepage constraints; see Section 7.1.1. In order to prevent excessive temperature rise of the copper traces in the PCB, a minimal trace width is calculated in Section 7.1.2 for the worst-case current stresses given in Section 6.1.2. A four-layer PCB is used for the design of this converter. The traces on the PCB containing the converters are handling the main power of the PCB. These traces are therefore named 'Power nets' or 'Power traces' for the rest of this chapter.

7.1.1. CREEPAGE AND CLEARANCE CONSTRAINTS

Creepage and clearance constraints are implemented for three different trace/net groups on the PCB:

- **A**: Between the positive of one DC-link output capacitor bank and the negative of the other DC-link output capacitor bank.
- **B**: Between a net that is part of a Power net, and every other trace on the PCB.
- **C**: Between every other net.

The clearance constraints are calculated using an online tool based on the IPC-2221B standard [66]. This online tool requires the DC or AC peak working voltage to calculate the required spacing between the traces. Furthermore, the creepage constraints are calculated using a similar tool based on the UL60950-1 standard [67]. The pollution degree for the creepage constraint is selected as I (least polluted) since the PCB will only be tested in a lab environment. The material group (I, II or IIIa/IIIb) is irrelevant for the creepage constraint if the chosen pollution degree is I (least polluted). Both the calculated clearance and creepage distances are shown in Table 7.2.

Table 7.2: Creepage and clearance distances calculated using the online tools by L. Rozenblat (2014) [66, 67] for the three different trace/net groups and the implemented design rule distance in Altium. ** The creepage distance of* 3.2 mm *is maintained for all exposed electrical contacts. For the PCB traces, which are all coated (for the outer layers) or insulated (for the inner layers),* 2.4 mm *is maintained. This distance should be sufficient considering the breakdown voltage of the insulating materials and solder mask.*

Trace Group	Clearance			Creepage		
	DC or AC peak voltage	Calculated distance (mm)	Implemented in Altium (mm)	RMS working voltage	Calculated distance (mm)	Implemented in Altium (mm)
A	1000	2.33	3	1000	3.2	10+
B	840	1.84	2.4	840	3.2	2.4*
C	5	0.05	0.2	5	0.08	0.2

7.1.2. TRACE WIDTH

An online PCB trace width calculator based on the IPC-2221 standard was used to calculate the required trace widths of different Power paths in the PCB [68]. Different types of traces and their maximum currents are listed in Table 7.3.

Table 7.3: Trace widths for different power traces. Calculated with the online calculator [68] using the worst-case currents given in Table 6.2.

Location	Maximum Current (RMS)	Required Trace Width for $\Delta T_{max} = 20\,°C$	
		Internal Layer (1 Oz/ft)	External Layer (2 Oz/ft)
Input Module Current	15 A	10.7 mm	4.13 mm
Output Module Current	20 A	16.0 mm	6.14 mm
HB Switch Node Current	15 A	10.7 mm	4.13 mm

7.2. FUNCTIONAL GROUPS OF THE PRINTED CIRCUIT BOARD

To improve the understanding of the functionality of the designed PCB, Figure 7.1 is complemented with highlighted functional groups of components and annotation in Figure 7.2. As becomes evident from Figure 7.2, the PCB can be split into half, both containing a module that exists of two HBs. The following groups can be distinguished in Figure 7.2:

- **Optical Fiber Communication Transmitters (TX) and Receivers (RX)**: These connectors receive and transmit signals from the Digital Signal Processor (DSP) are found on the top side of the PCB. The received signals (RX) are: eight PWM signals for the four HBs, two PWM signals for the CD relays and VD relay and a clear signal to clear a fault on the PCB. The transmitted signals (TX) are: the onboard measured input voltages of Input Module 1 and 2, the onboard measured output voltage of the Output Module 1 and 2 and the signal indicating fault on the board.
- **Input Module 1 and 2**: The two input modules are entirely isolated from each other. They both have a positive and negative input connector and are connected to two DC-link capacitors (the capacitors as described in Table 6.8), forming the input side of the converter. Both modules also contain discharge resistors for discharging the DC-link capacitors after converter turn-off. The voltage measurement circuitry can be found on the left and right side of Input Module 1 and 2, respectively.
- **Fault circuit**: The central part of the fault circuitry is placed between Input Module 1 and Input Module 2. The fault circuitry contains a flip-flop that determines whether all gate drivers are enabled or disabled in case of a fault. A fault can be cleared through the tactical button on the PCB or through the fiber optic CLR receiver. The decentralized parts of the fault circuitry are placed in front of each gate driver: it inputs the PWM signal and the Enable signal to an AND-gate, which then delivers the PWM signal to the gate driver. So in case of a fault, none of the PWM signals will reach the gate drivers, which means they are all deactivated.
- **Half-Bridge A, B, C and D**: Contains the Half-Bridges that are part of the Buck converters used in this study. Each Half-Bridge also contains:
  - Two (existing) gate driver PCBs that generate the gate signals based on the received PWM signals. The gate drivers can also detect faults in the operation

of the used switch: in case of a fault in one of the gate drivers, it emits a fault signal that is routed to the fault circuitry between the two Input Modules.
  - A connector (Half-Bridge Switching Node) that directly connects to the switching node of the corresponding Half-Bridge.

- **Phase A, B, C and D Output**: This region contains multiple elements:
  - Output node for each respective phase: the output of inductor L_b is connected to this connector in this study. The current then flows through the Current transducer to the respective output module.
  - Current transducer (CKSR-NP 25): can provide an onboard measurement of each phase current. The transducer is accompanied by additional circuitry required to process the signal produced by the transducer, and to convert the signal to a digital signal.
  - Optical Fiber TX (Current Measurement): Vertical optical fiber connector which can transmit the phase-current measurement signal to the DSP.
- **Output Module 1 and 2**: These two output modules are directly connected to an VD/CD structure implemented using relays. The relays can put the two modules either in series or parallel depending on the operating point. The output modules both consist of two paralleled DC-link capacitors (details in Table 6.8). The specifications of the used relays are listed in Table 6.9.

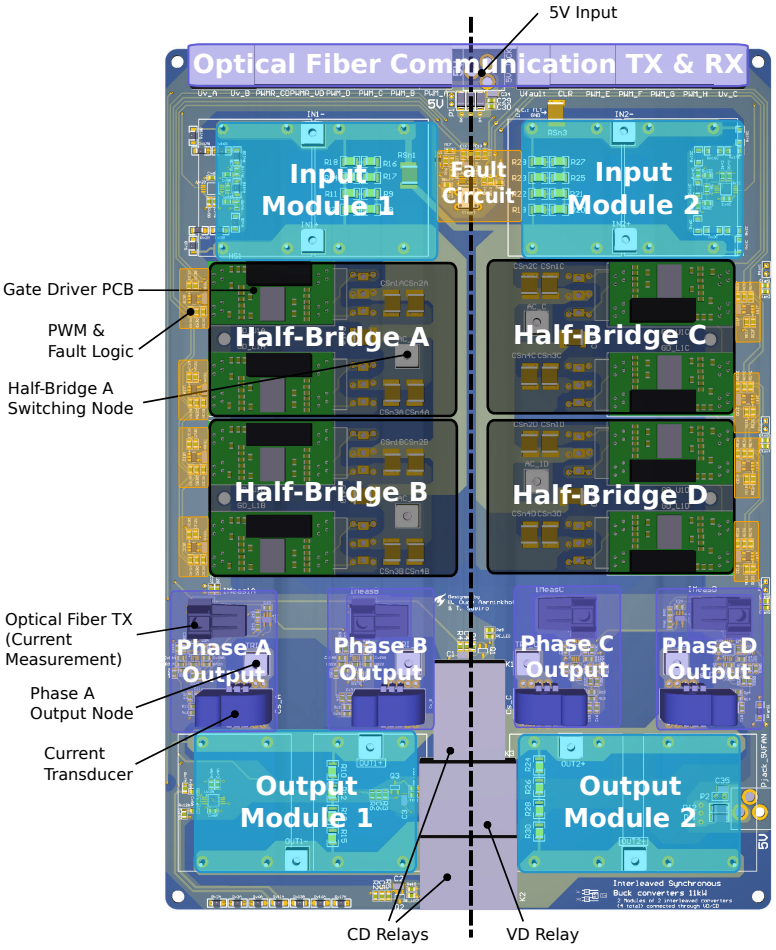


Figure 7.2: Functional regions of the designed PCB. The reader is referred to the start of Section 7.2 for a detailed explanation of the function of each of these functional regions.

7.3. PHOTOS OF FINAL DESIGNS

Photos were taken from the experimental prototypes of the LLC converter and the Interleaved TCM Buck converter, shown in Figures 7.3 and 7.4.

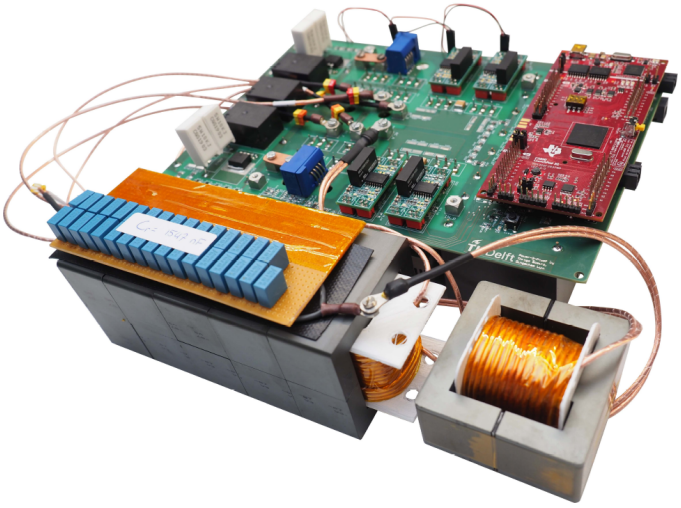


Figure 7.3: A photo of the LLC converter prototype.

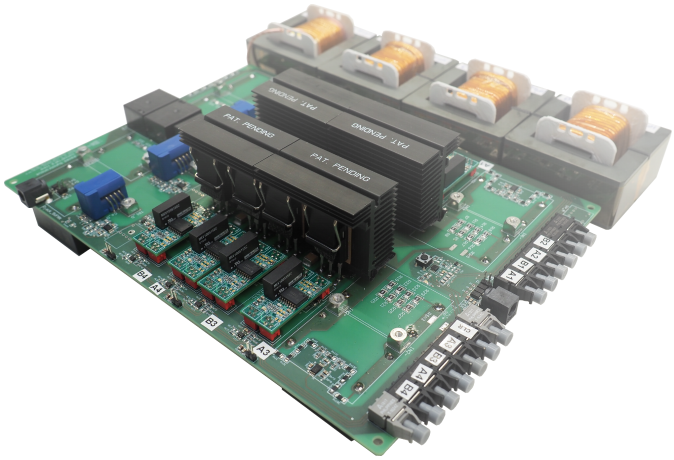


Figure 7.4: A photo of the Interleaved TCM Buck converter prototype.

8

EXPERIMENTAL VERIFICATION

The prototypes of the two converters are tested in the lab using open-loop testing. The two converters are tested separately to keep the setup in the lab manageable. The experimental verification has two main goals:

- Verifying operation of the converter as described by the analytical models.
- Determining the efficiency of both converters over the operating range to assess their performance.

Section 8.1 explains the experimental setups used to test the efficiency of the converters. The used equipment is listed in Table 8.1. The operation of the Interleaved TCM Buck converter is verified in Section 8.2, along with the measured efficiency at each point. The same is done for the LLC converter in Section 8.3. Finally, the efficiencies of the two individual converters are combined to achieve efficiency of the complete two-stage converter in Section 8.4. The achieved efficiency is compared to other wide V_o range studies listed in Section 2.5 as well. The comparison with the other two-stage converter proposed by Lee et al. (2019) [39] is highlighted. Sections 8.2 to 8.4 are accompanied by observations of the obtained results.

8.1. EXPERIMENTAL SETUP

All equipment used during the experimental verification is listed in Table 8.1, including a brief description. A picture of the experimental setup of the Interleaved TCM Buck converter is provided in Figure 8.2, including references to the used equipment from Table 8.1. The identical setup is used for testing the LLC converter. A schematic overview of the connections and all equipment is shown for the LLC converter in Figure 8.1. The setup is used in a similar manner for the Interleaved TCM Buck converter, only with different measurements connected to the oscilloscope.

Table 8.1: All equipment used to perform the experimental verification of the designed prototypes.

Label	Equipment	Type	Manufacturer	Used as / Used to
I	Bi-directional DC Power Supply	SM 1500-CP-15	Delta Elektronika	DC-input voltage source and DC-output current sink
II	Bi-directional DC Power Supply	SM 500-CP-90 (2x)	Delta Electronika	DC-input voltage source and DC-output current sink
III	150W DC Power Supply, Triple Output	EST150	Delta Electronika	Power source for: PCB, external fans DSP
IV	Power Analyzer	WT500	Yokogawa	Determine Efficiency
V	8-Channel Mixed Signal Oscilloscope	DLM4058	Yokogawa	Oscilloscope to measure and check currents and voltages
VI	Differential Voltage Probe	N2791A	Keysight	
VII	Differential Voltage probe	700924 (2x)	Yokogawa	
VIII	Current Probe	N2782B (4x)	Keysight	
IX	Microcontroller	C2000 LaunchPad XL (TMS320F283790)	Texas Instruments	Used as controller for the prototype in combination with an SIMULINK interface.
X	LCR Meter	HM8018	Hameg	Measure L and C of components

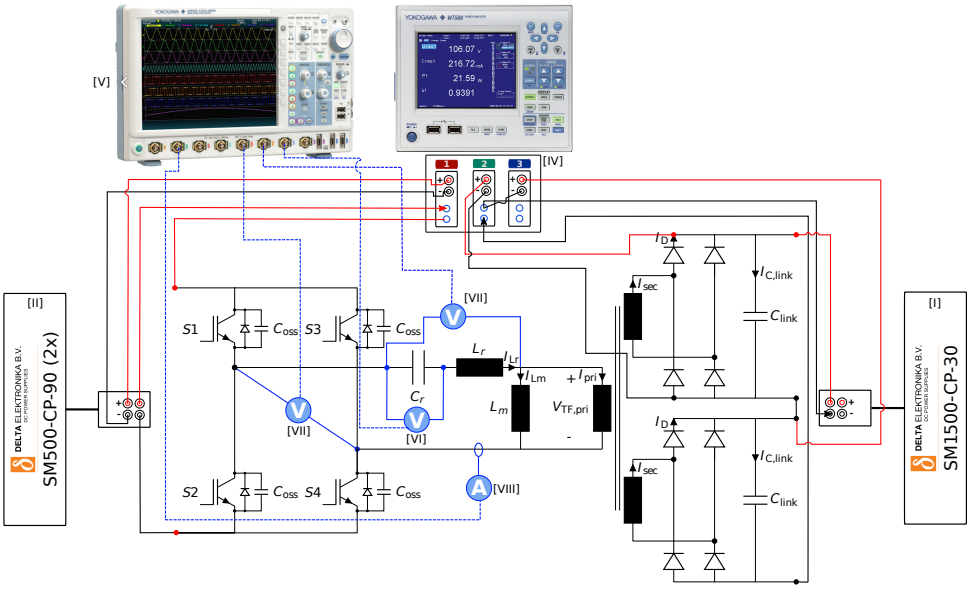


Figure 8.1: Schematic overview of the experimental setup for testing the LLC converter. Images of the oscilloscope and power analyzer are taken from https://tmi.yokogawa.com/. For the numbering of the equipment, see Table 8.1.

Figure 8.2: Picture of the experimental setup of the Interleaved TCM Buck converter in the lab. For the numbering of the equipment, see Table 8.1.

8.2. INTERLEAVED TCM BUCK CONVERTER RESULTS

A note upfront: the converter is implemented with the C2M0080120D MOSFET instead of the IMW120R060M1H MOSFET mentioned in Chapter 5. Because the first was already available in the lab. See Section 8.2.1 for further explanation of the (minimal) difference this gives analytically. All analytical calculations given in Figure 8.3 and tables 8.2 and 8.4 are given using the C2M0080120D.

The performance of the Interleaved TCM Buck converter is assessed by varying both V_o and I_o. A mesh of six steps in V_o (between 150-1000 V) and six steps in I_o (between 5-30 A) is tested experimentally to keep the number of required measurement points manageable. Note that this will result in a more coarse efficiency map compared to the analytical one in Figure 5.7. Only the results for V_{in} =525 V are given in this section to keep this chapter concise. A table with the V_{in} =689 V results is given in Appendix D. The operation points of the VD configuration are only HB-A and HB-B (half of the converter). Only half of the converter is used because two separate input power supplies would be required for these operation points, which were not available during the experiments.

The results of the experiments are shown in Table 8.2 and Figures 8.3 and 8.4. The operation of the converter at low P_o is shown in Figure 8.6. Two images showing the converter waveforms during t_{dead} are shown in Figures 8.7 and 8.8. Besides this, the output voltage ripple ΔV_o is shown in Figure 8.9. Additionally, observe the interleaved currents of the four individual HBs. Finally, all parameters and the performance of the Interleaved TCM Buck converter are listed in Table 8.4.

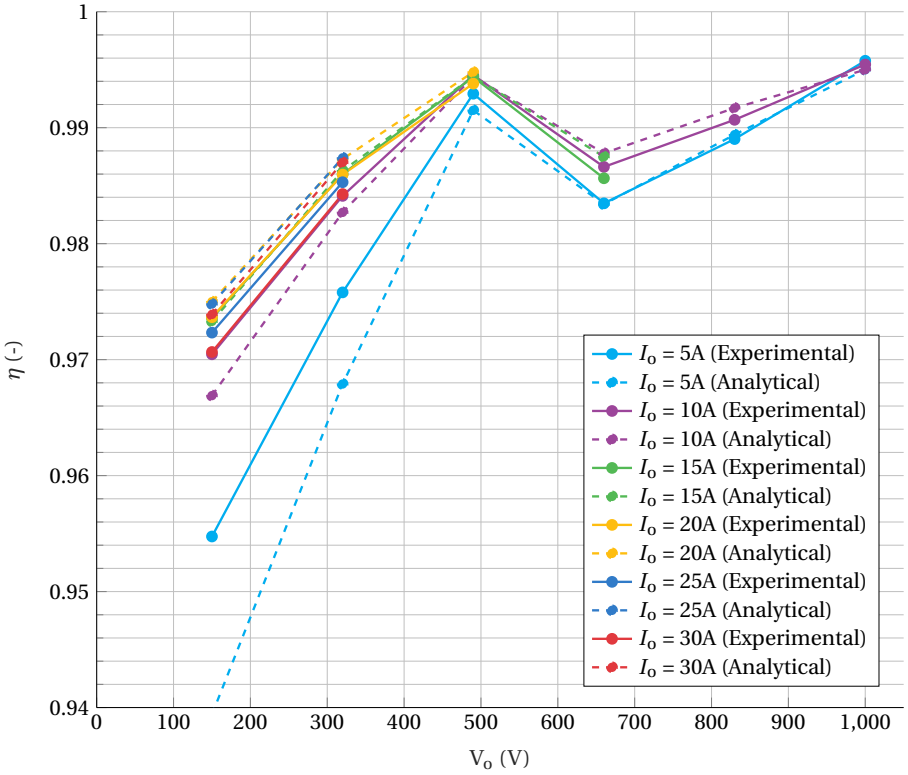


Figure 8.3: Visualization of the $\eta_{\text{analytical}}$ and η_{measured} over the entire operation range given in Table 8.2. The output voltage is on the y-axis, and the different colors indicate different I_o.

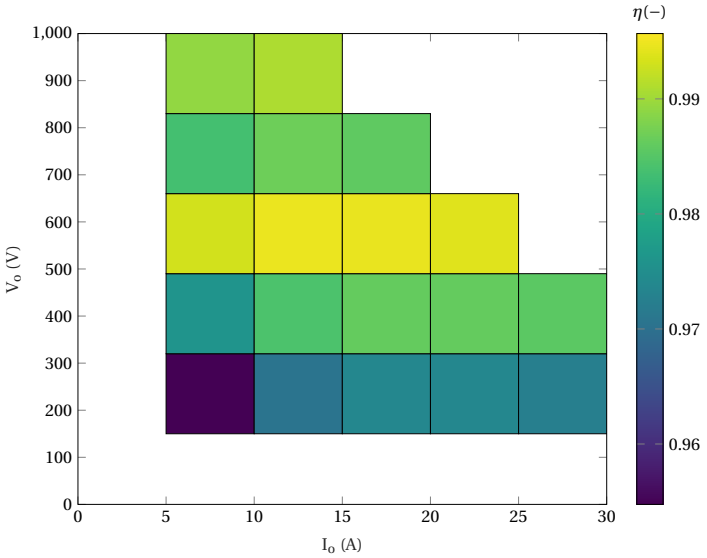


Figure 8.4: Efficiency of the Interleaved TCM Buck converter over the entire operating range, as is provided for the analytical model as well in Figure 5.7b.

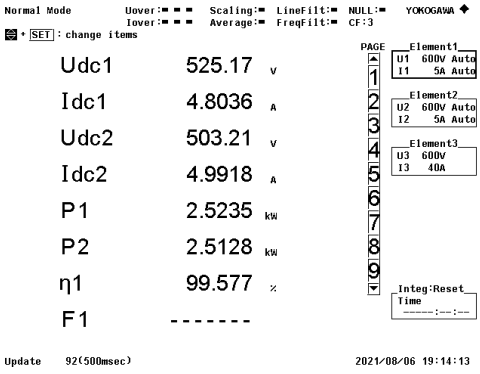


Figure 8.5: A screenshot taken on the Yokogawa WT500 Power Analyzer at the operation point with the highest measured efficiency. See Table 8.2 for the operation point details (V_o=1000 V, I_o=5 A).

Table 8.2: All operation points tested with the prototype and their respective predicted (analytical) and measured efficiency. Additional figures of a few operation points are included, which are listed in the 'Image' column. The peak efficiencies are highlighted in **bold**. V_{in} =525 V for these operation points. * *See Limitations (Chapter 9).*

VD/CD	V_o	I_o	t_{dead}	D	f_{sw}	$\eta_{analytical}$	$\eta_{measured}$	Image	Accuracy
CD	150	5	100	0.2857	113.40	0.9394	0.95475	Figure 8.6	
		10	100		94.50	0.9669	0.97046		
		15	100		81.00	0.9733	0.97358		
		20	100		70.87	0.9750	0.97366		
		25	100		63.00	0.9748	0.97235		
		30	100		56.70	0.9739	0.97066		
	320	5	100	0.6095	132.25	0.9679	0.97580		
		10	100		110.21	0.9827	0.98412		
		15	100		94.46	0.9863	0.98600		
		20	100		82.66	0.9873	0.98596		
		25	100		73.47	0.9874	0.9853		
		30	100		66.12	0.9870	0.98428	Figure 8.8	
	490	5	100	0.9333	34.57	0.9915	0.99293		
		10	100		28.81	0.9944	0.99453		
		15	100		24.70	0.9949	0.99437	Figure 8.7	
		20	100		21.61	0.9948	0.99380	Figure 8.9	
VD*	660	5	100	0.6286	108.11	0.9834	0.98348		
		10	100		81.08	0.9878	0.98662		
		15	100		64.86	0.9875	0.98564		
	830	5	100	0.7905	76.69	0.9894	0.98902		
		10	100		57.52	0.9917	0.99068		
	1000	5	100	0.9524	21.00	**0.9950**	**0.99577**	Figure 8.5	
		10	200		15.75	**0.9950**	0.99545		

To better understand Figures 8.7 to 8.9 an overview of which measured quantity is connected to which oscilloscope channel is provided in Table 8.3.

Table 8.3: Oscilloscope channels and the measured quantity connected to each channel, as a reference for Figures 8.7 to 8.9.

Channel	**Color**	**Measured Quantity**
Channel 1	Yellow	Current through Inductor A
Channel 2	Green	Current through Inductor B
Channel 3	Purple	Current through Inductor C
Channel 4	Turquoise	Current through Inductor D
Channel 5	Red	V_{DS} of High-Side MOSFET HB A
Channel 6	Orange	V_{DS} of Low-Side MOSFET HB A
Channel 7	Blue	Output voltage V_o
Channel 8	-	-

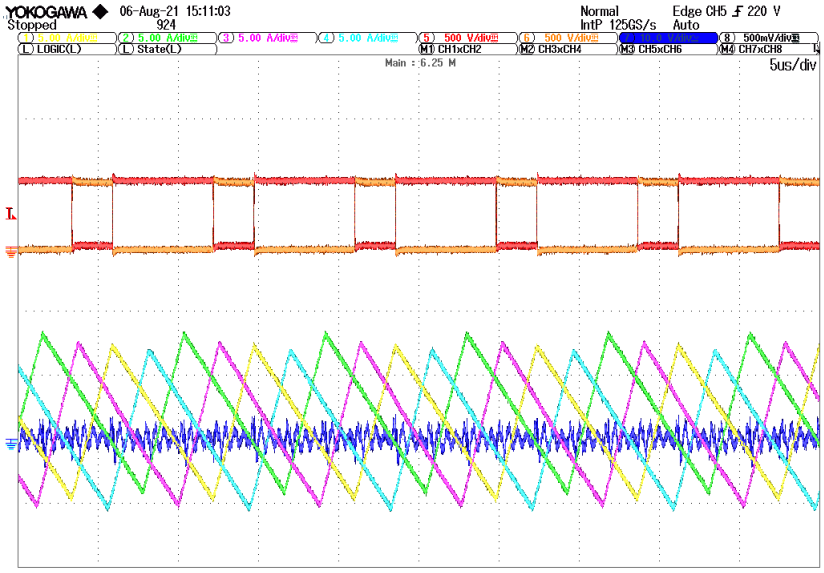


Figure 8.6: Operation of the Interleaved TCM Buck converter at low P_o. Notice the slight difference in $-I_R$ and amplitude of the different inductor currents. See Table 8.2 for the operation point details (V_o=150 V, I_o=5 A).

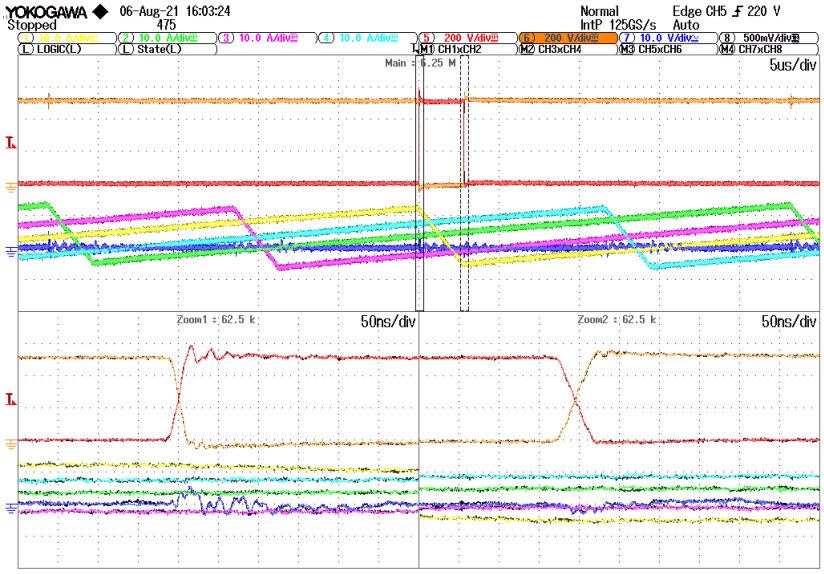


Figure 8.7: Zoom-in capture of ZVS turn-on of S2 and S1 respectively. See Table 8.2 for the operation point details (V_o=490 V, I_o=15 A).

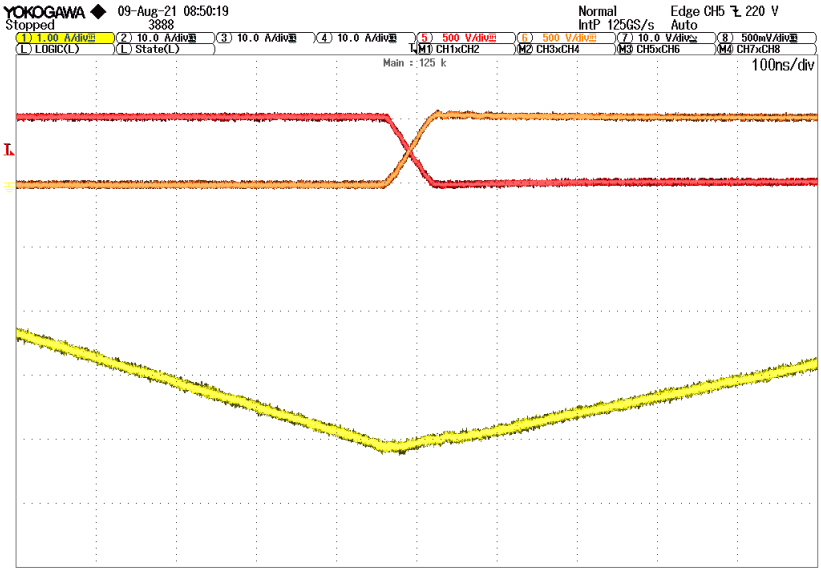


Figure 8.8: Zoom-in on the resonant period of the inductor current I_{Lb} during t_{dead}. See Table 8.2 for the operation point details (V_{o}=320 V, I_{o}=30 A).

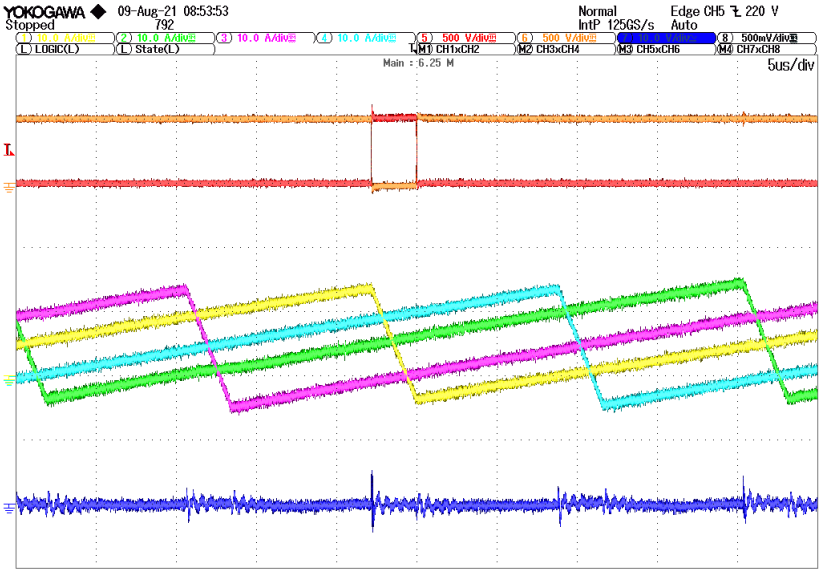


Figure 8.9: Displayed output voltage ripple on Channel 7, the dark-blue line in the bottom of the figure. Notice the interleaved currents of the four HBs. See Table 8.2 for the operation point details (V_{o}=490 V, I_{o}=20 A).

Table 8.4: Interleaved TCM Buck converter final design parameters and performance. ** Measured with LCR meter at f =10 kHz (see Table 8.1).*

Parameter	**Symbol**	**Designed**	**Experimental**
Inductance A	L_A	75.59 µH	76.23 µH*
Inductance B	L_B	75.59 µH	75.74 µH*
Inductance C	L_C	75.59 µH	76.10 µH*
Inductance D	L_D	75.59 µH	75.95 µH*
Minimum Operating Frequency	$f_{sw,min}$	15 kHz	15.75 kHz
Maximum Operating Frequency	$f_{sw,max}$	181.39 kHz	181.39 kHz
Semiconductor Switch		C2M0080120D	
Output Capacitor bank		C4AQILW5150A36J (800 V, 15 µF)	
Heat sink Thermal Resistance	R_{sa}	2.59 °C/W	
Converter Dimensions	$L \times B \times H$	-	275×263×76 mm
Maximum Power	P_{max}	11 kW	11 kW
Power Density		-	2.00 kW/L
Performance Parameter	**Symbol**	**Designed**	**Experimental**
Peak efficiency	η_{max}	0.995	0.99577
Chargecycle 11-400 Efficiency	$\eta_{11,400}$	0.9869	0.98750
Chargecycle 55-400 Efficiency	$\eta_{55,400}$	0.9850	-
Chargecycle 11-800 Efficiency	$\eta_{11,800}$	0.9875	0.98170
Chargecycle 55-800 Efficiency	$\eta_{55,800}$	0.9871	-

OBSERVATIONS

Multiple observations are made based on the results of the Interleaved TCM Buck converter presented in Section 8.2.

- In theory, Inductors A,B,C and D should have an equal inductance value. However, they are wound by hand leading to differences in inductance value (see Table 8.4). The effect of these unequal inductances can be seen in Figure 8.6: inductor current B (Channel 2) has the largest output ripple, which can be expected since it has the lowest inductance value. The load current is, therefore, not equally shared between each phase. This unequal sharing of current leads to deviations compared to the Analytical model.
- The highest efficiency is achieved at the highest duty cycle D. Because of the VD/CD structure, this converter achieves the maximum efficiency twice. This effect can be observed in Figures 8.3 and 8.4 and Table 8.2. Because of this peak efficiency being achieved twice, both 400 V and 800 V batteries can be charged near the highest efficiency of the converter.
- Note that the output power in Figure 8.5 is only half of what is expected at the mentioned operation point. This is due to a lack of bi-directional power supplies at the moment of testing in the lab. The VD configuration could only be tested using HB-A and HB-B. Otherwise, another bi-directional power supply would be required: Input Modules 1 and 2 (see Figure 7.2) were connected in parallel to the same power supply. This works while in CD mode, however it would lead to shorting the power supply if the converter were to be operated in VD mode.
- Following up on the previous point, the converter's efficiency in CD mode for only HB-A and HB-B is compared to the efficiency of the total converter (all four HBs) in CD. At low P_o, the total converter outperformed the efficiency of only half of the converter. One reason can be because the current can 'find' the path of least resistance. The effect is quite significant: at V_o=150 V and I_o=5 A the total converter achieved an efficiency of η=0.954 75, while half of the converter achieved η=0.949 98. However, at high output power this effect can also decrease the converter's efficiency: the conduction losses in all the wires used in the experimental setup increase by I^2_{RMS}. This effect is also observed: half of the converter operated more efficient than the total converter at high P_o. The effect is small; at V_o=490 V and I_o=20 A, the total converter achieved η=0.993 80, while half of the converter achieved η=0.994 85. Because of this, the efficiencies displayed in Table 8.2 for VD mode can be slightly different when the total converter would be used. See Appendix E for the comparison at each operation point.
- Observe from Figure 8.7 that ZVS is achieved in less time for turn-on of S2 when compared to turn-on of S1. This is as expected; the current magnitude is higher during t_{dead} of the first transition when compared to the latter transition when I_R =-5 A.
- The predicted $\eta_{analytical}$ does not differ significantly from the experimental $\eta_{measured}$. This substantiates the methods by which the losses of different components are calculated in Appendix A.
- The Chargecycle efficiencies of Case Ib and IIb (55 kW-400 V and 55 kW-800 V respectively (see Section 4.2.1) have, unintentionally, not been tested.

8.2.1. IMPLEMENTED MOSFET

As mentioned in the beginning of this chapter, the C2M0080120D MOSFET is implemented in the prototype of the converter. According to Table 4.5 this should give a large difference in losses: the C2M0080120D has a 15% higher turn-off loss but also an 65% larger $R_{ds,on}$ at the operation point given in Table 4.5. However, as is clear from Figure 8.10, this single operation point does not provide all information regarding the performance of the different devices. The switching losses and conduction losses of both the C2M0080120D and the IMW120R060M1H MOSFET are compared for Charging Cycle Ib (see Section 4.2.1) in the analytical model.

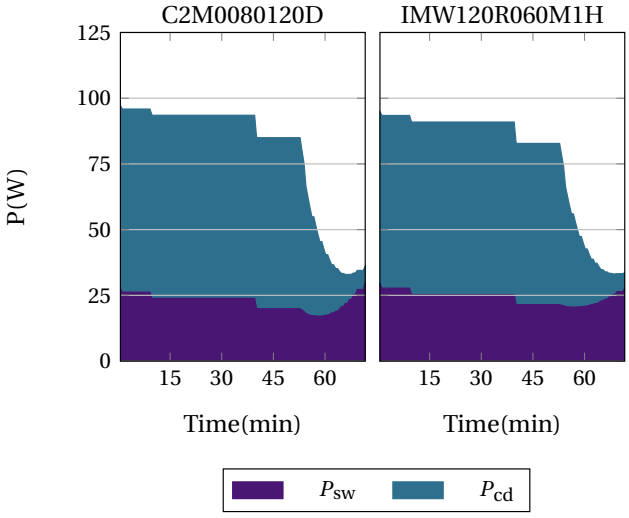


Figure 8.10: Total losses of all eight MOSFETs in the Interleaved TCM Buck converter in case of the: C2M0080120D MOSFET and the IMW120R060M1H MOSFET.

As is observed from Figure 8.10, the difference is not as large as Table 4.5 might suggest: the performance of both switches should, approximately, be similar.

8.3. LLC CONVERTER RESULTS

The LLC converter operates at constant f_{sw}. The output voltage is, therefore, constant since it is only determined by the turns ratio n. The performance of the LLC converter can, therefore, be assessed by varying only I_o. This is in contrast to the Interleaved TCM Buck converter, where both I_o and V_o have to be varied. The efficiency of the LLC converter is only determined for V_{in}=640 V due to limitations of the used Bi-directional DC Power Supplies (see Table 8.1). The tested operation points and the results are given in Table 8.5 and Figure 8.11. Additional images of the converter waveforms are given in Figures 8.12, 8.13, 8.15 and 8.16. Information regarding which oscilloscope channel measures what is found in Table 8.6. Besides this, a snapshot of the WT500 Power Analyzer at the peak efficiency is provided in Figure 8.14. The final design parameters and performance are given in Table 8.7.

Table 8.5: Tested operation points for the LLC converter and their respective predicted (analytical) and measured efficiency. Additional figures of a few operation points are included, which are listed in the 'Figure' column. The input voltage $V_{in} = 640\,V$, and the turns-ratio slightly differs from the turns-ratio in Section 6.2.1.

P_o (W)	V_o (V)	I_o (A)	t_{dead} (ns)	$\eta_{analytical}$ (−)	$\eta_{measured}$ (−)	Figure
470.2	1126.6	0.380	1200	0.9098	0.90489	Figure 8.13
849.6	1124.5	0.714	1200	0.9486	0.94546	
1066.7	1123.4	0.952	1200	0.9590	0.95688	
2132.8	1120.9	1.904	1200	0.9755	0.97420	
3202.9	1119.6	2.857	1400	0.9805	0.97919	
4265.4	1118.5	3.809	1400	0.9827	0.98125	
5318.8	1117.4	4.761	1400	0.9839	0.98209	
6374.9	1116.3	5.714	1400	0.9845	**0.98231**	Figures 8.14 and 8.15
7420.4	1114.3	6.666	1400	0.9848	0.98218	
8471.7	1112.7	7.619	1400	0.9849	0.98188	
9531.1	1112.1	8.571	1400	0.9849	0.98134	
10572.0	1110.6	9.523	1400	0.9848	0.98076	Figure 8.16

Table 8.6: Oscilloscope channels and the measured quantity connected to each channel, as a reference for Figures 8.12, 8.13, 8.15 and 8.16.

Channel	**Color**	**Measured Quantity**
Channel 1	-	
Channel 2	Green	Resonant Current I_{Lr}
Channel 3	-	
Channel 4		
Channel 5	Red	Voltage V_{AB}
Channel 6	Orange	Voltage over RTN $L_r + C_r$
Channel 7	Blue	Voltage V_{Cr}
Channel 8	Purple	Logic probe for Gate signals

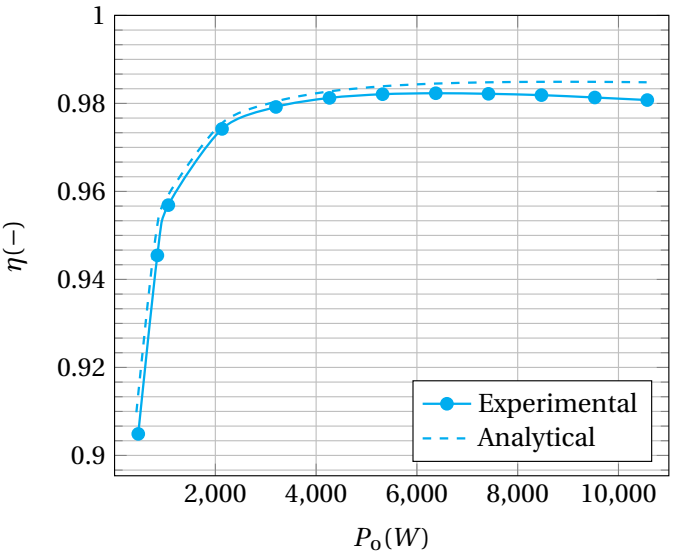


Figure 8.11: LLC converter efficiency over the entire output power range P_o as calculated analytically and measured experimentally.

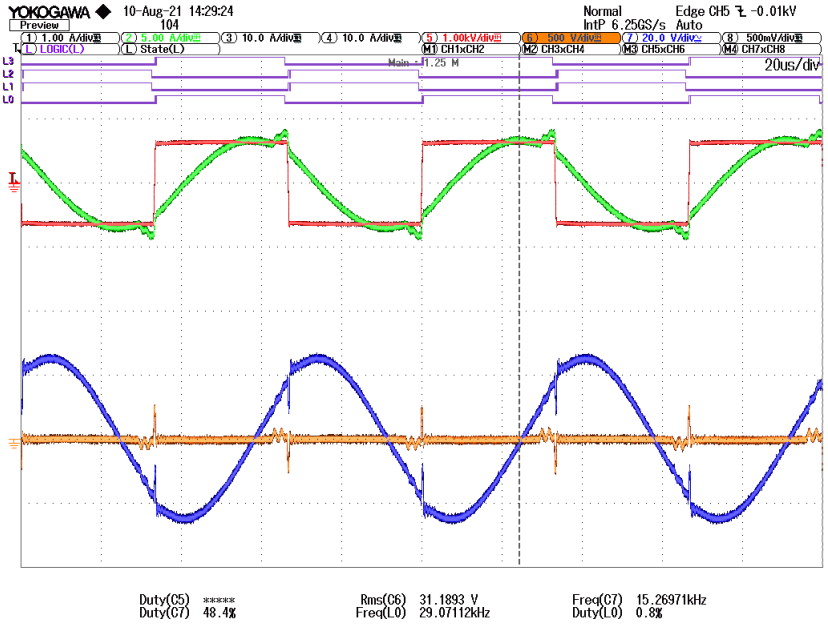


Figure 8.12: LLC resonant converter operating at low power. Note the overlap of the magnetizing current and series resonant current is visible in Channel 2 (the green waveform). Measurement of the voltage over the RTN is also shown and is nonzero due to these spikes in voltage (as is also observed in Section 3.1.5).

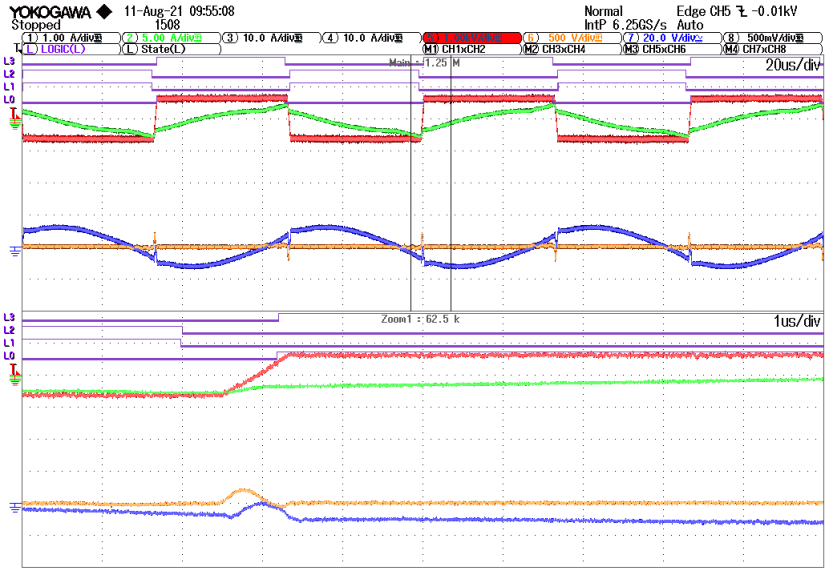


Figure 8.13: Zoom in on the deadtime period, where V_{AB} transitions from $-V_{in}$ to V_{in}. This allows ZVS turn-on for S1 and S4 (see Figure 3.1).

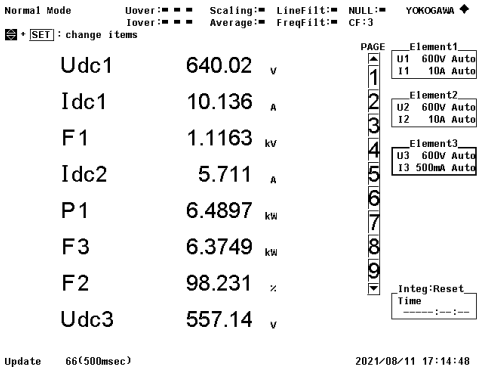


Figure 8.14: Screenshot taken on the Yokogawa WT500 Power Analyzer at the operation point with the highest measured efficiency. See Table 8.5 for the operation point details (P_o=6.37 kW).

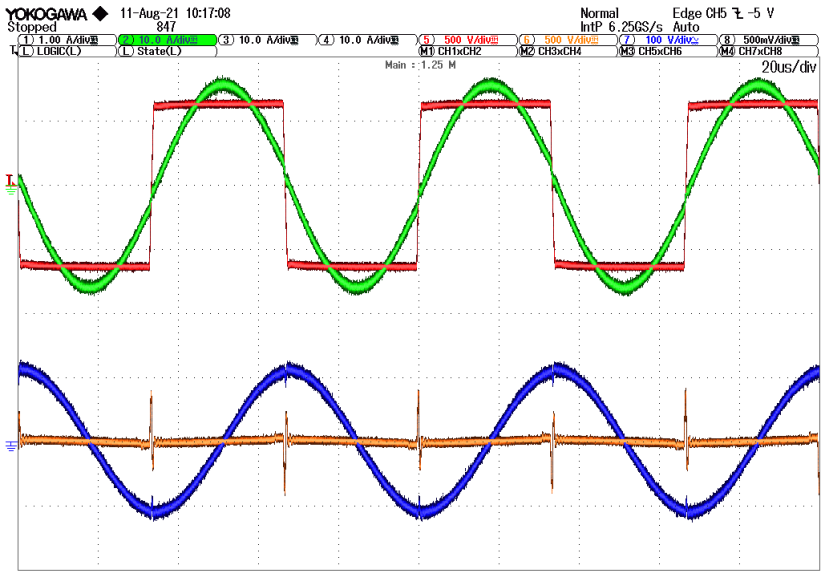


Figure 8.15: Operation waveforms of the LLC converter at the point of highest efficiency See Table 8.5 for the operation point details (P_O=6.37 kW). The spikes in voltage over the RTN during deadtime can again be observed on Channel 6.

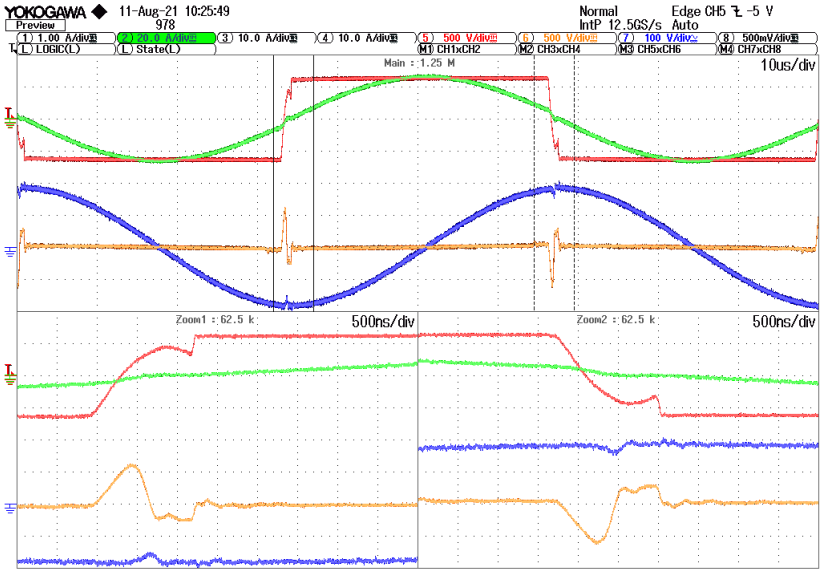


Figure 8.16: Incomplete ZVS due to the resonant current (Channel 2) dropping to zero. Therefore, the charging/discharging of the output capacitances of the semiconductor switches is seized. See Table 8.5 for the operation point details (P_O=10.57 kW).

Table 8.7: LLC converter final design parameters and performance.

Parameter	**Symbol**	**Designed**	**Experimental**
Magnetizing Inductance	L_{m}	mH	3.79 mH
External resonant Inductance	$L_{\mathrm{r,ext}}$		66.40 µH
Primary side leakage Inductance	L_{σ}		7.30 µH
Total resonant Inductance	L_{r}	75 µH	73.70 µH
Resonant Capacitance	C_{r}	1500 nF	1547 nF
Resonant Frequency	f_{sr}	15 kHz	14.905 kHz
Turns ratio	$n : s_1 : s_2$	1:0.82:0.82	1:0.88:0.88*
Semiconductor Switch		IKW40N120CS6	
Rectifier Diode		IDW30G120C5B	
Output Capacitor bank		C4AQIBW5600A3NJ (800 V, 60 µF)	
Switching Frequency	f_{sw}	15 kHz	15 kHz
Converter Dimensions	$LxBxH$	-	285x235x90 mm
Maximum Power	P_{max}	11 kW	11 kW
Power Density		-	1.82 kW/L
Performance Parameter	**Symbol**	**Designed**	**Experimental**
Peak efficiency	η_{max}	0.9849	0.9823
Chargecycle 11-400 Efficiency	$\eta_{11,400}$	0.9848	0.9808
Chargecycle 55-400 Efficiency	$\eta_{55,400}$	0.9826	0.9789
Chargecycle 11-800 Efficiency	$\eta_{11,800}$	0.9848	0.9746
Chargecycle 55-800 Efficiency	$\eta_{55,800}$	0.9839	0.9800

OBSERVATIONS

Multiple observations are made based on the results of the LLC converter presented in Section 8.3.

- The measured efficiency is slightly lower than the analytical efficiency (see Table 8.5). The lower measured efficiency is possibly due to the loss contribution of the external resonant inductor $L_{r,ext}$, of which the losses are not considered in the analytical model.
- Figure 8.12 shows that the LLC converter operates in discontinuous mode at low P_o. This makes part of the magnetizing current 'visible'. The measurement of the RMS over $L_r + C_r$ is displayed as well in Figure 8.12. It is nonzero due to the voltage spikes that were observed in Section 3.1.5 as well. These voltage spikes cause deviations between the FHA model and the actual operation of the converter. These voltage spikes can be observed at every operation point (see Figures 8.13, 8.15 and 8.16).
- The completion of ZVS turn-on can be seen in Figure 8.13, where V_{AB} changes from $-V_{in}$ to $+V_{in}$.
- The maximum efficiency ($\eta_{measured,max} = 0.9821$) is lower when compared to the Interleaved TCM Buck converter ($\eta_{measured,max} = 0.9958$). This is mainly due to the losses that the transformer and rectifier diode bridge add to the converter (compare Figure 5.1 with Figure 5.5).
- The experimental magnetizing inductance L_m is lower than the designed value (see Table 8.7). This is because the transformer with the designed L_m started to lose ZVS at relatively low P_o. This occurred in the same manner as displayed in Figure 8.16: at a given instance, I_{Lr} touches zero, stopping the commutation process of V_{AB}. This effect is resolved by reducing L_m to 3.79 mH which increased the magnetizing current I_{Lm}.
- The turns ratio $n : s_1 : s_2$ is higher in the wound transformer than designed (1:0.88:0.88 instead of 1:0.82:0.82). This caused the output voltage to be higher than the expected 1050 V (see Table 8.5). In order to provide an accurate estimation of the efficiency, the simulation is rerun to provide the analytical efficiencies in Figure 8.11 and Table 8.5.
- Observe from Table 8.5 that V_o varies with the operation point. This indicates that the LLC converter is not operating precisely at the series resonant frequency f_{sr}. This is correct since the converter is operated with f_{sw} =15 kHz, while f_{sr}=14.905 kHz (see Table 8.7). Operating slightly above f_{sr} guarantees that the impedance of the RTN is inductive, which guarantees ZVS turn-on.

8.4. TWO-STAGE RESULTS

The combined efficiency is calculated using Equation (8.1), where η_{TCM} is taken from Table 8.2. Not all values of P_o of the Interleaved TCM Buck converter and their respective efficiency are measured in the LLC converter. Therefore, interpolation is used to determine η_{LLC} of intermediate points. Figure 8.11 is divided into three individual curves, and a cubic polynomial is fitted to these sections. The results are shown in Table 8.8. The peak efficiency and Charge cycle efficiencies (based on Tables 8.4 and 8.7) are given

in Table 8.9.

$$\eta_{\text{combined}} = \eta_{\text{TCM}} \cdot \eta_{\text{LLC}} \tag{8.1}$$

Table 8.8: The three curve-fitted cubic polynomials based on the datapoints in Figure 8.11 and Table 8.5.

Polynomial	**Valid for P_o range**	**Curve-fitted equation**	R^2
I	0.47-2.13 kW	$\eta_{\text{LLC}} \approx 3.40315 \cdot 10^{-11} \cdot P_o^3 - 1.66129 \cdot 10^{-7} \cdot P_o^2 + 0.000276827 \cdot P_o + 0.809313$	1
II	2.13-5.32 kW	$\eta_{\text{LLC}} \approx 2.31641 \cdot 10^{-13} \cdot P_o^3 - 3.50146 \cdot 10^{-9} \cdot P_o^2 + 0.0000183335 \cdot P_o + 0.948779$	1
III	4.27-10.57 kW	$\eta_{\text{LLC}} \approx 1.63236 \cdot 10^{-14} \cdot P_o^3 - 4.84441 \cdot 10^{-10} \cdot P_o^2 + 4.25135 \cdot 10^{-6} \cdot P_o + 0.970681$	0.997317

Table 8.9: Performance parameters for the two-stage converter.

Performance Parameter	**Symbol**	**Designed**	**Experimental**
Peak efficiency	η_{max}	0.9789	0.9766
Chargecycle 11-400 Efficiency	$\eta_{11,400}$	0.9719	0.9685
Chargecycle 55-400 Efficiency	$\eta_{55,400}$	0.9678	-
Chargecycle 11-800 Efficiency	$\eta_{11,800}$	0.9724	0.9567
Chargecycle 55-800 Efficiency	$\eta_{55,800}$	0.9712	-

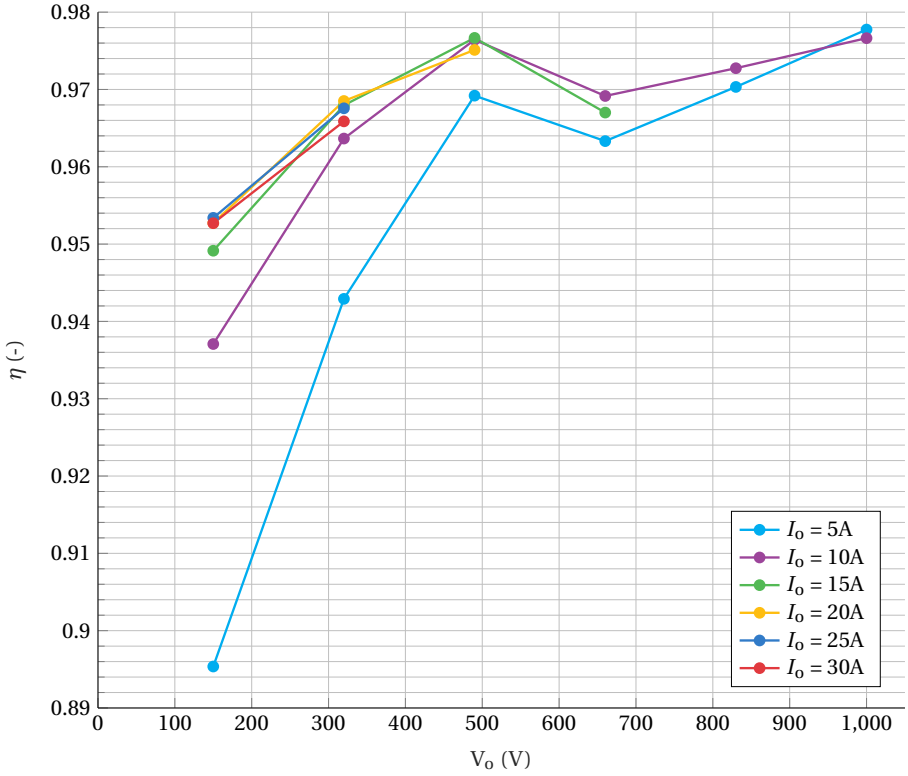


Figure 8.17: Efficiency of two-stage LLC + Interleaved TCM Buck converter over the entire operation range. The efficiencies of the Interleaved TCM Buck converter in Table 8.2 are multiplied by the (interpolated) efficiency of the LLC converter determined from Table 8.5 to obtain the efficiency of the two-stage converter.

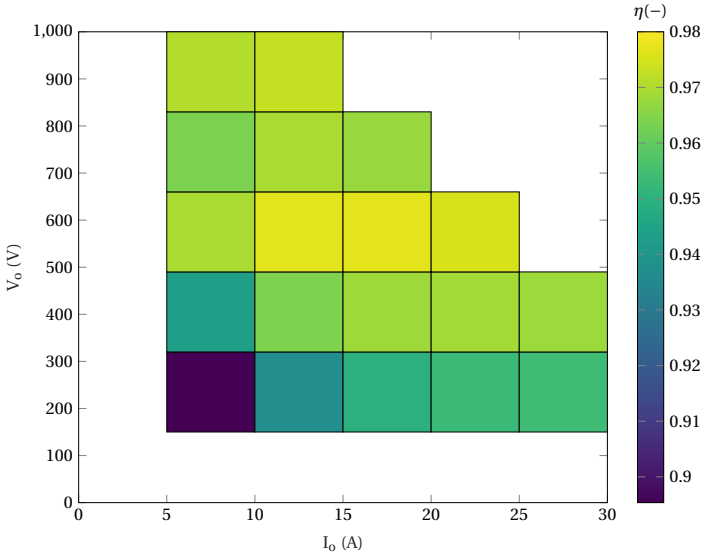


Figure 8.18: Efficiency of the two-stage LLC + Interleaved TCM Buck converter over the entire operating range.

A comparison of some performance parameters between the proposed two-stage RPC and the two-stage RPC proposed by Lee et al. (2019) [39] is provided in Table 8.10.

Table 8.10: Comparison of the two-stage RPC from Lee et al. (2019) [39] and the one designed in the current study.

	Two-stage RPC from [39]	**Two-stage RPC proposed in this study**
Output Voltage range	50-650 V	150-1000 V
Switching frequency range	LLC: 120 kHz Buck: 50 kHz	LLC: 15 kHz Buck: 15-181 kHz
Number of Switches	5	12
Number of Diodes	9	8
Number of Transformers	2	1
Number of Inductors	1	5
Maximum Power	20 kW	11 kW
Peak Efficiency	97.32%	97.66%
Power Density	-	1.05 kW/L

OBSERVATIONS

Multiple observations are made based on the results of the two-stage converter presented in Section 8.4.

- The two-stage converter is able to operate at high efficiency for almost the entire operating range. Moreover, the converter operates above 95% for any output voltage at total-power. The peak efficiency is η_{measured} =0.9766 (at V_o=1000 V, I_o=5 A) (see Figure 8.17).
- The power density of the designed two-stage converter is subpar compared to other literature studies (see Figure 2.6). Combining the power densities of the individual converters (see Tables 8.4 and 8.7), a total power density of 1.05 kW/L is achieved. Therefore, it can be concluded that the prototypes are not designed for power density, and there is room for improvement in this aspect. The LLC converter, for example, could be operated at higher f_{sw} to reduce the size of the magnetic components. Additionally, the two-stage converter could be designed on a single PCB which would improve the power density significantly.
- The proposed converter achieves the widest V_o range of all studies found regarding wide V_o solutions for RPCs (see Table 2.4). It achieves a higher peak efficiency when compared to four other studies [34–36, 39], while it is outperformed by three outer studies [30, 37, 69] with at most 0.7%. It is the only study among those listed before that uses IGBTs in the resonant converter.
- Note that the power consumption of the PCB, the control board and the external fan is not included in the efficiency calculation. The first consumed 9.12 W, the second 2.22 W and the latter 2.23 W. This would account for $(9.12 + 2.22 + 2.23)/11000 \cdot 100\% = 0.12\%$ of the power consumed at total power.

9

CONCLUSION

The aim of the current study was to design an 11 kW EV charger with a wide output voltage range based on a resonant power converter topology. The implemented solution consisted of a two-stage resonant power converter. The two-stage converter exists of an LLC converter followed by an Interleaved TCM Buck converter. The achieved output voltage range of 150-1000 V in the current study was not previously reported in literature regarding resonant power converters for EV charging. A prototype of the proposed converter was designed and used to evaluate the efficiency: 95+% efficiency was achieved over the entire output voltage range at maximum power, with a peak efficiency of 97.66%. The obtained efficiency for the 11 kW-400 V Charging cycle is 96.85% and 95.67% for the 11 kW-800 V Charging cycle.

9.1. RESEARCH QUESTIONS REVISITED

Which resonant power converter topologies and modulation methods are best suited to achieve a wide output voltage range?

Most RPCs for EV charging found in literature are based on the LLC resonant tank or a variation of it. Section 2.3 showed that this topology is popular because of its low circulating energy, wide operation range that allows for ZVS and ZCS and the possibility of incorporating the leakage inductance as the resonant inductor. The CLLC or CLLLC converter are the preferred variations of the LLC converter for bidirectional operation, such as the converter proposed by Wei et al. (2020) [30].

Quantitative research into RPCs for EV charging in Section 2.5 revealed that only a few studies in literature reported an output voltage range wider than 250-450 V. The standard control method (PFM) is not suitable to achieve a wider output voltage range on its own [40]. The following methods were discovered for achieving a wider output voltage range using RPCs: variable input voltage to the RPC [34, 35], interleaving two RPCs [37], using a hybrid topology [69], a multi-level primary and secondary side switch network [36], a combination of multiple control strategies [70] and finally a two-stage topology

[39]. The two-stage topology was selected for the current study due to its simplicity in analytical modeling, ease of control and promising efficiency.

How to devise, implement and verify a multi-objective design procedure based on efficiency and cost of different design solutions?
Two different configurations of the two-stage converter were proposed in Section 4.1. One configuration requires 1200 V rated switches, and the other configuration required 1700 V rated switches. Besides this, multiple parallel phases and different minimal switching frequencies were considered. Analytical models were developed of both converters in MATLAB, and these models were verified using LTSpice simulations. These analytical models were used to determine the losses of the converters. This was based on: the given datasheets of the semiconductors, the loss modelling of magnetic components (based on Mühlethaler et al. (2012)[58]) and the operational conditions provided by the analytical models. After this, a method was developed to assess the efficiency of different solutions based on the real-world charging cycles of a 400 V and a 800 V battery architecture. The best performing designs were chosen as final designs. A PCB was designed for the Interleaved TCM Buck converter. Finally, prototypes of both proposed converters were constructed. Experiments were done to verify the analytical models, and to determine the efficiency. A peak efficiency of 97.66% is achieved. The obtained efficiency for the 11 kW-400 V Charging cycle is 96.85% and 95.67% for the 11 kW-800 V Charging cycle. The proposed two-stage converter achieved a 150-1000 V output voltage range, which was not yet reported in literature for an EV charger based on a resonant power converter.

How does the chosen topology equipped with IGBTs compare to SiC MOSFETs with regards to efficiency?
IGBT based solutions and MOSFET based solutions were added to the comparison of the two different configurations in Chapter 5. The selected IGBT achieved similar efficiency at 15 kHz as the selected MOSFET for the LLC converter. The IGBT based Interleaved TCM Buck converter, however, showed inferior performance to the MOSFET based converter. The relatively high switching frequency required for large parts of the operation range are detrimental to the performance of the IGBT based converter. None of the six other studies regarding resonant power converters for wide output voltage EV charging reported the use of IGBTs in the converter [30, 34–37, 39], making this an unique feature of the current study. The proposed two-stage solution, using IGBTs in the first stage, achieved a high peak efficiency comparable to the efficiencies of other recent studies regarding RPCs for EV charging. It is therefore possible for an IGBT based solution to be competitive with (SiC) MOSFET based solutions.

9.2. IMPLICATIONS

The current study shows that a wide output voltage range (150-1000 V) can be achieved by using a two-stage converter for EV charging. Only a handful of studies found during the literature review are capable of a wide output voltage range [30, 34–37, 39]. However, none of those studies reported an output voltage range as wide as achieved in the current study. This wide output voltage range is important because in recent years, more

EVs are equipped with 800 V battery architectures (see Table 1.1). The higher battery voltage allows for faster charging times [12]. Reducing the charging time takes away one of the drawbacks compared to the refuelling time of ICEs [5]. Reducing the charging time for EVs would aid in accelerating the transition to widespread EV adoption. The proposed EV charger in this study can serve both the mainstream 400 V battery architectures and the upcoming new 800 V battery architectures. All this is achieved while achieving 95+% efficiency for the entire output voltage range at full power, with a peak efficiency of 97.66%.

9.3. LIMITATIONS

The current study has the following limitations:

- The performance of other non-isolated DC-DC converters instead of the (Interleaved) TCM Buck converter was not explored in this study. However, the current study did assess the performance of; different configurations, number of interleaved phases and the use of IGBTs or MOSFETs for the buck converter.
- The LLC converter was designed with a predetermined switching frequency of 15 kHz. If it were a variable, however, the design might be more power-dense. This increase in switching frequency would, nevertheless, lead to a significant increase in switching loss for the IGBT based solution. Possibly causing the IGBT based solution to not be competitive with the SiC MOSFET based solutions anymore.
- The effect of snubbers on the performance of the IGBTs was only touched upon briefly. On top of this, the working of the snubber in the LLC converter was not as expected in the analytical and simulation model. There was not sufficient time to investigate the effects of the snubber more thoroughly in the current study.
- The achieved peak efficiency of 97.66% is relatively high, judging from Figure 2.5. Nevertheless, the peak efficiency fails to provide information about efficiency during real-world charging cycles, as is proposed in this study in Section 4.2.1.
- The use of the WT500 Power analyzer used to determine the efficiency of the converter is questionable. The accuracy of the measurements starts to decline rapidly for AC measurements with a frequency above 1 kHz: a current measurement has ±(4.2% of measurement+0.3% of range) at 50 kHz [71]. Fortunately, three out of four measured quantities are DC (input- and output voltage, output current) preventing worsening of the accuracy through error propagation. However, it is still recommended to re-test the efficiencies using a power analyzer better capable of measuring high-frequency quantities. The Yokogawa PZ4000 power could be used, if it is availalable in the lab. Or the WT1800E from the same series as the WT500 could be purchased and used for re-testing the efficiencies [72].
- The IMW120R060M1 SiC MOSFET [57] was selected for the Interleaved TCM Buck converter. However, the C2M0080120D SiC MOSFET [73] was implemented in the lab because it was already available and did not have to be ordered. As shown in Table 4.5, this C2M0080120D has a 15% higher turn-off loss but also an 65% larger $R_{ds,on}$ compared to the IMW120R060M1 according to the datasheets (that is, at the operating conditions of Table 4.5). The conduction loss of the SiC switches is the most significant contribution to the total loss (see Figure 5.5) in the Interleaved

TCM Buck converter. However, as became clear from Figure 8.10, the comparison of a switch based on a single operation point does not provide all information. A selection method based on true performance by implementing each switch in the actual analytical model might, therefore, provide a more accurate comparison of performance.

- As mentioned in Section 5.2 and Table 8.5, only half of the converter was used to test the operation points that belong to the VD mode. However, to check the validity of these results for half of the converter, a comparison was made in CD mode between the efficiency of the total- and half-converter. This comparison showed that the total converter achieved superior performance (up to 0.5%) in the low output power range. While the efficiency decreased only slightly at high output power (0.1% at most) (see Appendix E). There is a small effect, and therefore it is advised to also test the total converter in VD when all necessary equipment is available.
- The power consumption of the PCB, the control board and the external fan were not included in the efficiency calculations. At full power, these three power consumptions combined would account for 0.12% of the power when the converter operates at $P_{o,max}$ =11 kW. Nevertheless, it depends on whether other studies included these losses as well, to draw a conclusion about the fairness of the comparison.
- Despite the author's best efforts and intentions, it might be that not all studies regarding RPCs and EV charging have been found during the quantitative research in Section 2.4. Furthermore, misinterpretations might have occurred while evaluating these studies. This aspect could be alleviated if in future research multiple researchers would conduct the study in a joint-effort.

9.4. RECOMMENDATIONS FOR FUTURE WORK

Further recommendations for future research are explained below.

- Investigate other non-isolated DC-DC topologies that might allow for the 650 V class rated switches in the non-isolated DC-DC converter. These switches have lower conduction losses when compared to the 1200 V rated switches used in this study. These 650 V rated switches might further improve the efficiency of the second stage.
- Develop a different method of calculating f_{sw} for the Interleaved TCM Buck converters, in such a way that it stays in a range of 15-80 kHz. This can lead to the required increment in efficiency that the single-phase (N_{phase} = 1) IGBT based solution needs (see Figure 5.3a) to achieve comparable performance to the MOSFET configurations.
- Devise a single-stage RPC based on an LLC converter, where a combination of control methods is used to achieve a wide V_o range, as it is a promising direction of research as well, as stated in Section 2.5. For example, a combination of PSM and PFM can be used to achieve a wide V_o range, as was done in [43]. Then compare this solution to the solution proposed in the current study.
- Further optimize the current LLC converter design by:

  - Altering the design of the transformer in such a way that it has a larger leakage inductance. This larger leakage inductance can facilitate the elimination of $L_{r,ext}$, thereby reducing LLC converter losses and size.
  - Investigate the use of snubbers to reduce the turn-off losses of the primary side IGBTs more thoroughly.
  - Consider different f_{sw} and the trade-off between converter size and losses and implications on the performance of both MOSFET and IGBT based solutions.
  - Considering over-dimensioning the current rating of the SiC MOSFETs to achieve lower conduction losses comparable or lower than the proposed IGBT in order to increase the efficiency of the converter.
- Test both the LLC converter and the Interleaved TCM Buck converter in a closed-loop. In the current study both converters were only operated in open-loop in the current study. This while closed-loop testing would allow to see the performance of the two-stage converter during, for example, faults and abnormal charging conditions.
- Both the LLC converter and the Interleaved TCM Buck converter have been equipped with semiconductors that can handle higher currents than occurred in this study. It would be interesting to see the efficiency at P_o >11 kW.

Appendices

A

LOSS MODELLING

In this study the losses of all semiconductor devices and magnetic components are modeled analytically in MATLAB. In order to implement this interpolation of several figures/parameters provided on the datasheet of the respective semiconductors is performed. The constructed analytical model is used to assess the theoretical efficiency of each converter at every operation point, but also to determine whether thermal limits of components (like the semiconductors or the magnetics) are violated. The losses of IGBTs and MOSFETs are treated in separate sections below.

A.1. MOSFET

A.1.1. SWITCHING LOSSES

The LLC converter is operating at the series resonant frequency for the entire operation range. As a result, the primary side switches have ZVS turn-on over the entire operating range. This leaves only the conduction and turn-off losses for the primary switches. The Interleaved TCM Buck converter also has ZVS turn-on of the switches.

The turn-off loss $P_{\text{sw,off}}$ is calculated using Equation (A.1).

$$P_{\text{sw,off}} = f_{\text{sw}} \cdot (E_{off}(V_{ds} I_{ds} T_j R_g) - E_{\text{oss,off}}) \tag{A.1}$$

E_{off} is a function of V_{ds}, I_{ds}, T_j and R_g according to the datasheet. Individual relations are determined based on the curve-fitted graphs from the datasheet of the particular MOSFET, in Equations (A.2) to (A.4).

$$E_{\text{off,Ids}} = a \cdot I_{\text{sw,off}}^2 + b \cdot I_{\text{sw,off}} + c \tag{A.2}$$

$$E_{\text{off,Rg}} = b \cdot R_g + c \tag{A.3}$$

$$E_{\text{off,Tj}} = a \cdot T_j^2 + b \cdot T_j + c \tag{A.4}$$

The combined effect of all four parameters is approximated by the interpolation given by Equation (A.5).

$$E_{\text{off}}(V_{ds}, I_{ds}, T_j, R_g) = E_{\text{off,Ids}} \cdot \frac{V_{\text{ds}}}{V_{\text{ds,data}}} \cdot \frac{E_{\text{off,Rg}}}{b \cdot R_{\text{g,data}} + c} \cdot \frac{E_{\text{off,Tj}}}{a \cdot T^2_{\text{j,data}} + b \cdot T_{\text{j,data}} + c} \tag{A.5}$$

The subscript *data* is the condition of the specific parameter (V_{ds}, T_j or R_g) as used in the datasheet curve of $E_{\text{off,Ids}}$.

A linear charge equivalent capacitance $C_{\text{Q,eq}}$ is introduced by Kasper et al. (2016) [50] which replaces C_{oss} from the datasheet. In contrary to C_{oss}, this capacitance has the same amount of stored charge as the non-linear capacitance at a given drain to source voltage V_{ds}. $C_{\text{Q,eq}}$ which is given by Equation (A.6).

$$C_{\text{Q,eq}}(V_{DS}) = \frac{Q_{oss}(V_{DS})}{V_{DS}} = \frac{\int_0^{V_{DS}} C_{oss}(v)\,dv}{V_{DS}} \tag{A.6}$$

$C_{oss}(v)$ is curve-fitted from the datasheet to the power relation in Equation (A.7).

$$C_{oss}(v) = a \cdot V_{DS}^b + c \tag{A.7}$$

Using this equivalent output capacitance $E_{\text{oss,off}}$ is calculated by Equation (A.8).

$$E_{\text{oss,off}} = \frac{1}{2} C_{\text{Q,eq}} V^2_{\text{DS}} \tag{A.8}$$

A.1.2. CONDUCTION LOSSES

The conduction losses of the MOSFET are calculated using Equation (A.9).

$$P_{cd} = R_{\text{ds,on}}(T_j) \cdot I^2_{\text{sw,rms}} \tag{A.9}$$

$R_{\text{ds,on}}(T_j)$ is determined by curve-fitting the datasheet graph to the second order polynomial given in Equation (A.10).

$$R_{\text{ds,on}}(T_j) = a \cdot T_j^2 + b \cdot T_j + c \tag{A.10}$$

A.2. IGBT

IGBTs have a relatively high switching loss compared to MOSFETs. This is a limiting factor for the operation range of the IGBT: their maximum f_{sw} is lower than for MOSFETs. The switching losses are directly related to f_{sw}, and therefore the thermal limit of IGBTs is reached at a lower frequency than MOSFETs.

A.2.1. SWITCHING LOSSES

Turn-off loss of the IGBT is determined in a similar way as for the MOSFET using Equations (A.11) to (A.16).

$$P_{\text{sw,off}} = f_{\text{sw}}(E_{off}(V_{CE} I_{CE} T_j R_g) - E_{\text{oes,off}}) \tag{A.11}$$

$$E_{\text{off,Vce}} = b \cdot V_{ce} + c \tag{A.12}$$

$$E_{\text{off,Ice}} = a \cdot I_{\text{sw,off}}^2 + b \cdot I_{\text{sw,off}} + c \tag{A.13}$$

$$E_{\text{off,Rg}} = b \cdot R_g + c \tag{A.14}$$

$$E_{\text{off,Tj}} = a \cdot T_j^2 + b \cdot T_j + c \tag{A.15}$$

$$E_{\text{off}}(V_{CE}, I_{CE}, T_j, R_g) = E_{\text{off,Ice}} \cdot \frac{E_{\text{off,Vce}}}{b \cdot V_{\text{ce,data}} + c} \cdot \frac{E_{\text{off,Rg}}}{b \cdot R_{\text{g,data}} + c} \cdot \frac{E_{\text{off,Tj}}}{a \cdot T_{\text{j,data}}^2 + b \cdot T_{\text{j,data}} + c} \tag{A.16}$$

A.2.2. CONDUCTION LOSSES

In this application, the IGBT is co-packed with a diode to allow for a negative current as well. Both conduction losses of these devices are taken into account using Equations (A.17) and (A.18).

$$P_{\text{cd,IGBT}} = R_{\text{ce,on}} \cdot I_{\text{IGBT,rms}}^2 + V_{\text{F}} \cdot I_{\text{IGBT,avg}} \tag{A.17}$$

$$P_{\text{cd,diode}} = R_{\text{D}} \cdot I_{\text{diode,rms}}^2 + V_{\text{Fd}} \cdot I_{\text{diode,avg}} \tag{A.18}$$

$R_{\text{ce,on}}$ and V_{F} are determined based on the I_{C} vs V_{CE} diagram typically found on IGBT datasheets. See Figure A.1 for how both $R_{\text{ce,on}}$ and V_{F} are derived using this figure. Both values are determined at the worst-case junction temperature $T_{\text{j}} = 175\,\text{deg}\,C$, and $V_{\text{GE}} = 15V$. The same method is used to determine R_{D} and V_{Fd} of the body diode based on a datasheet figure, of which the details here are omitted.

A.3. DIODE LOSSES

The LLC converter uses rectifying diodes. Silicon Carbide (SiC) schottky diodes are known for their fast switching capability and negligible switching loss (due to negligible reverse recovery current). These diodes will be used in the design of the LLC converter, and therefore the only loss occurring in these diodes is the conduction loss. Like the IGBT, the conduction loss of the diode consists of two terms (see Equation (A.19)).

$$P_{\text{cd,diode}} = R_{\text{F}} \cdot I_{\text{diode,rms}}^2 + V_{\text{F}} \cdot I_{\text{diode,avg}} \tag{A.19}$$

V_{F} and R_{F} are determined based on the $I_{\text{F}} - V_{\text{F}}$ diagram. An example is given in Figure A.2.

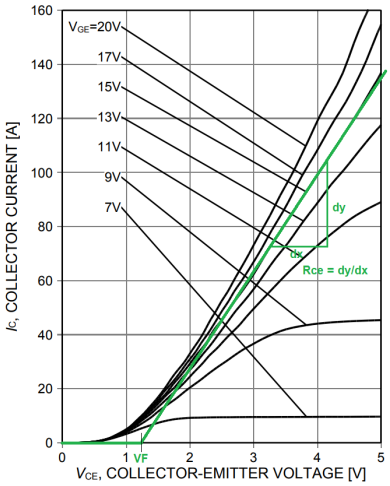


Figure A.1: Typical I_C vs V_{CE} curve taken from the IKW40N120CS6 datasheet [56]. Shows how V_F and $R_{ce,on}$ are determined.

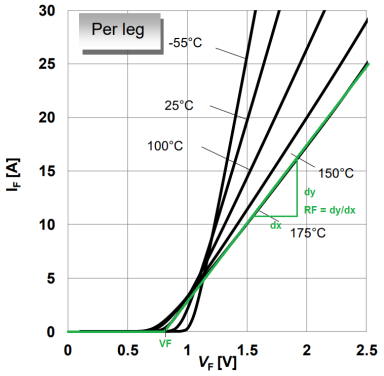


Figure A.2: Determination of V_F and R_F based on the $I_F - V_F$ curve of the IDW30G120C5B SiC Schottky diode [63].

A.4. MAGNETIC LOSSES

In this study both inductors and a transformer will be used. The losses of these magnetic components can be put in two main categories;

- Core Losses
- Winding losses
  - Skin losses
  - Proximity losses

A.4.1. TRANSFORMER

CORE LOSSES

The core losses in the high frequency transformer are constant over the entire operating range of the LLC converter. This feature is unique to a transformer when compared with an inductor. The core operates at a constant magnetic flux, independent of the current that flows through the windings. The core losses are calculated using the improved Generalized Steinmets Equation (iGSE), given in Equation (A.20).

$$P = \left(\frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B^{\beta-\alpha}) \mathrm{d}t \right) \cdot V_{\text{core}} \tag{A.20}$$

k_i is defined in Equation (A.21)

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} \left| cos\theta \right|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{A.21}$$

α and β and k are the Steinmetz coefficients mentioned on the datasheet of the respective core material.

WINDING LOSSES

The winding losses are calculated in MATLAB based on the procedure described by Mühlethaler et al. (2012) [58].

A.4.2. INDUCTOR LOSSES

CORE LOSSES

Contrary to the transformer, the operating flux of an inductor is dependent on the current through the inductor winding. In the LLC converter, the magnitude of the current through inductor L_{r} is dependent on the load current. In the Interleaved TCM buck converter, ΔI is dependent on the output current of the converter, see Equations (A.22) and (A.23).

$$\Delta B = \frac{L_b \cdot \Delta I}{N \cdot A_c} \tag{A.22}$$

$$P_{\text{loss,IGSE}} = \left(\frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha_c} \cdot \Delta B^{\beta_c - \alpha_c} \mathrm{d}t \right) \cdot V_{\text{core}} \tag{A.23}$$

WINDING LOSSES

The winding losses are calculated in MATLAB based on the procedure described by Mühlethaler et al. (2012) [58].

A.5. VERIFICATION MOSFET/IGBT LOSS USING LTSPICE

LTSpice simulation models are downloaded from both Infineon [74] and Wolfspeed [75] to verify the analytical method of calculating the losses of the IGBT and MOSFET. Using LTSpice, the total losses of a single switch ($P_{cd} + P_{sw}$) are measured at different P_o, and therefore at different I_{sw}.

A.5.1. IGBT LOSS VERIFICATION

The testing conditions are listed in Table A.1.

Table A.1: Testing conditions for comparing the analytical losses to the LTSpice losses.

Condition	**Value**
Device	IKW40N120CS6
T_j	175 °C
R_g	9Ω
V_{in}	840V
Topology	LLC full bridge

In Figure A.3, the analytical switch loss calculations of the IKW40N120CS6 are compared to the LTSpice losses. Note that $I_{sw,off}$ is constant for the LLC converter, independent of P_o. Therefore, any increase in switch losses with increasing P_o is only due to increased conduction losses.

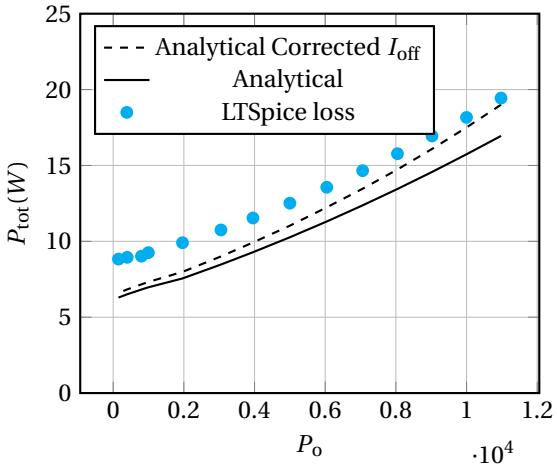


Figure A.3: Difference in loss calculated in MATLAB and the loss measured in the LTSpice simulation.

OBSERVATIONS

- There are two lines for the analytical calculations in Figure A.3. *Analytical* is for the analytical model from MATLAB using the $I_{\text{sw,off}}$ calculated in MATLAB. This is, however, not equal to the $I_{\text{sw,off}}$ in LTSpice. In theory, $I_{\text{sw,off}}$ should be independent of the output power, however, in the simulation it shows slight variations. $I_{\text{sw,off}}$ is directly related to the turn-off loss, and thereby related to P_{sw}. This is, therefore, one of the reasons that the *Analytical* line shows deviation from the LTSpice measured total switch losses. The *Analytical Corrected* I_{off} shows the analytical losses when $I_{\text{sw,off}}$ from the simulation is used. An improvement in accuracy can clearly be seen. However, at low output power the analytical model still results in approximately the same error.
- One other reason for deviation can be because of the LTSpice model of the switch. Infineon states that there are three levels of complexity for their SPICE models [74]. The model provided for the IKW40N120CS6 has the lowest level of complexity (Level 1). The influence of this on the accuracy of the LTSpice measurements is, however, unknown.

A.5.2. MOSFET LOSS VERIFICATION

The analytical model of the MOSFET is compared to the LTSpice simulation to verify its validity. The testing conditions are listed in Table A.2, and the results are plotted in Figure A.4.

Table A.2: Testing conditions for comparing the analytical losses to the LTSpice losses.

Condition	**Value**
Device	C2M0080120D
T_j	150 °C
R_g	5Ω
V_{in}	840 V
Topology	LLC full bridge

As can be seen in Figure A.4, the analytical model calculates larger total switch losses when compared to LTSpice. This might be due to deviations in the LTSpice model of the MOSFET. As the calculated analytical model loss is larger, it is safe to use it in further calculations.

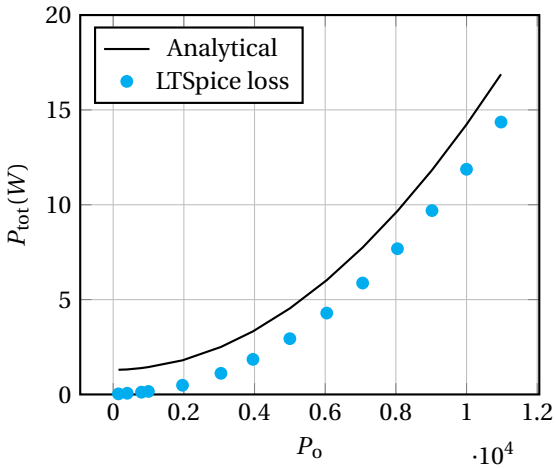


Figure A.4: Difference in total switch loss calculated in MATLAB measured in the LTSpice simulation.

B

MAGNETIC DESIGN

A simplified flowchart of the inductor design script and transformer design script is provided in Figure B.1. The AC winding losses and core losses for both designs are based on the methods described by Mühlethaler et al. (2012) [76]. A brief description of the equations used is given in Chapter 6.

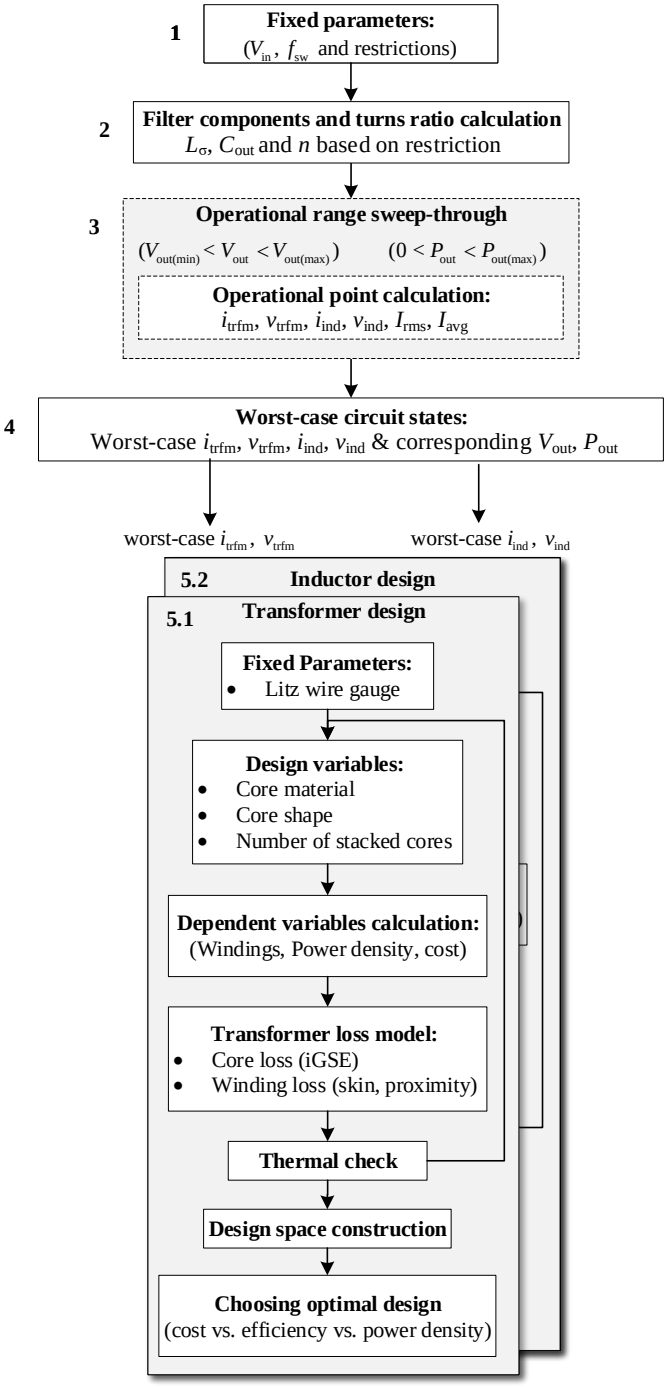


Figure B.1: Simplified flowchart of the Inductor- and Transformer design script used in this study.

C

QUANTITATIVE DATA

Table C.1: Studies using an **CLL** resonant tank found during the literature review. Studies that failed to provide both their output voltage and reported maximum efficiency were excluded from this list. Study titles in bold signify a Journal paper, while a study title in regular font signify a Conference paper.

Year	First Author	Study title	Output Voltage	$\eta_{\text{peak,experimental}}$
2014	E. Asa	Analysis of A Novel Interleaved CLL Resonant Converter for EV Battery Charger Applications	0-180 V	94.30%
2020	M. Abbasi	An SiC-Based AC/DC CCM Bridgeless Onboard EV Charger With Coupled Active Voltage Doubler Rectifiers for 800-V Battery Systems	800 V	97% (Simulation Only)

Table C.2: Studies using an **CLLC** resonant tank found during the literature review. Studies that failed to provide both their output voltage and reported maximum efficiency were excluded from this list. Study titles in bold signify a Journal paper, while a study title in regular font signify a Conference paper.

Year	First Author	Study title	Output Voltage	$\eta_{\text{peak,experimental}}$
2015	J. Lai	A High-Efficiency 3.3-kW Bidirectional On-Board Charger	250-450 V	95%
2018	R. Gadelrab	High-Frequency High-Density Bidirectional EV Charger	250-450 V	96.20%
2018	B. Li	**A High-Efficiency High-Density Wide-Bandgap Device-Based Bidirectional On-Board Charger**	250-450 V	96+%
2020	C. Wei	A SiC-Based 22kW Bi-directional CLLC Resonant Converter with Flexible Voltage Gain Control Scheme for EV On-Board Charger	200-800 V	98.5%
2020	Y. Xuan	**A Novel Three-level CLLC Resonant DC-DC Converter for Bidirectional EV Charger in DC Microgrids**	200-700 V	96.8%
2020	Zh. Zhang	**High-Efficiency High-Power-Density CLLC Resonant Converter With Low-Stray-Capacitance and Well-Heat-Dissipated Planar Transformer for EV On-Board Charger**	250-450 V?	97.85%
2020	J. Min	**Bidirectional Resonant CLLC Charger for Wide Battery Voltage Range: Asymmetric Parameters Methodology**	250-450 V	97.9%
2020	A.M. Ammar	A Bidirectional GaN-Based CLLC Converter for Plug-In Electric Vehicles On-Board Chargers	250-504 V	95.7%

Table C.3: Studies using an **CLLLC** resonant tank found during the literature review. Studies that failed to provide both their output voltage and reported maximum efficiency were excluded from this list. Study titles in bold signify a Journal paper, while a study title in regular font signify a Conference paper.

Year	First Author	Study title	Output Voltage	$\eta_{\text{peak,experimental}}$
2015	N. Shafiei	**Improving the Regulation Range of EV Battery Chargers With L3C2 Resonant Converters**	96-144 V	96%
2015	Z. Zahid	**Design of Bidirectional DC–DC Resonant Converter for Vehicle-to-Grid (V2G) Applications**	250-450 V	98.10%
2015	J.-S. Lai	A High-Efficiency 3.3-kW Bidirectional On-Board Charger	250-450 V	94.5%
2018	H. Chang	Design and Implementation of Bidirectional DC-DC CLLLC Resonant Converter	200-410 V	96.9%

Table C.4: Studies using an **SRC** resonant tank found during the literature review. Studies that failed to provide both their output voltage and reported maximum efficiency were excluded from this list. Study titles in bold signify a Journal paper, while a study title in regular font signify a Conference paper.

Year	First Author	Study title	Output Voltage	$\eta_{peak,experimental}$
2014	W.-Y.Choi	**High-Frequency-Link Soft-Switching PWM DC–DC Converter for EV On-Board Battery Chargers**	250-450 V	98.30%
2014	S.-H. Ryu	**Adjustable Frequency–Duty-Cycle Hybrid Control Strategy for Full-Bridge Series Resonant Converters in Electric Vehicle Chargers**	250-400 V	97%
2014	J.Park	**Zero-current switching series loaded resonant converter insensitive to resonant component tolerance for battery charger**	250-370 V	97.85%
2014	G. Liu	High Efficiency Wide Range Bidirectional DC/DC Converter for OBCM Application	240-430 V	97.5%
2015	M. Kwon	A High Efficiency Bi-directional EV Charger with Seamless Mode Transfer for V2G and V2H Application	250-410 V	95.60%
2016	Y.J. Kim	**Full-Bridge+SRT Hybrid DC/DC Converter for a 6.6-kW EV On-Board Charger**	250-413 V	97.9%
2016	B.-K. Lee	**A PWM SRT DC/DC Converter for 6.6kW EV Onboard Charger**	250-415 V	97.7%
2017	G. Liu	**Implementation of a 3.3-kW DC–DC Converter for EV On-Board Charger Employing the Series-Resonant Converter With Reduced-Frequency-Range Control**	180-430 V	98.1% (Si), 97.4% (GaN)
2019	S.-G. Jeong	**A Soft-Switching Single-Stage Converter With High Efficiency for a 3.3-kW On-Board Charger**	360 V	96%
2020	N. Dao	**High-Efficiency SiC-Based Isolated Three-Port DC/DC Converters for Hybrid Charging Stations**	200-400 V (2x)	98.20%

Table C.5: Studies using an **LLC** resonant tank found during the literature review. Studies that failed to provide both their output voltage and reported maximum efficiency were excluded from this list. Study titles in bold signify a Journal paper, while a study title in regular font signify a Conference paper.

Year	First Author	Study title	Output Voltage	$\eta_{peak,experimental}$
2011	H.J. Chae	3.3kW on board charger for electric vehicle	150-450 V	92.5%
2011	Y.S. Dow	A Study on Half Bridge LLC Resonant Converter for Battery Charger on Board	250-450 V	93.5%
2012	W. Guo	A 10kW 97%-efficiency LLC Resonant DC/DC Converter with Wide Range of Output Voltage for the Battery Chargers in Plug-in Hybrid Electric Vehicles	250-450 V	96.75%
2013	F. Musavi	**An LLC Resonant DC–DC Converter for Wide Output Voltage Range Battery Charging Applications**	240-430 V	96%
2013	K.-M. Yoo	**A 10-kW Two-Stage Isolated/Bidirectional DC/DC Converter With Hybrid-Switching Technique**	48-72 V	93%
2014	H. Wang	**Design and Analysis of a Full-Bridge LLC-Based PEV Charger Optimized for Wide Battery Voltage Range**	350 V	95.40%
2014	J.-Y. Lee	**6.6-kW Onboard Charger Design Using DCM PFC Converter With Harmonic Modulation Technique and Two-Stage DC/DC Converter**	320-420 V	97.2%
2014	J. Deng	**Design Methodology of LLC Resonant Converters for Electric Vehicle Battery Chargers**	250-450 V	98.20%
2014	K. Colak	A Novel LLC Resonant Converter with Semi Bridgeless Active Rectifier	0-80 V	96%
2014	H. Wang	A Novel Approach to Design EV Battery Chargers Using SEPIC PFC Stage and Optimal Operating Point Tracking Technique for LLC Converter	100-420 V	?
2014	W. Sun	Design Considerations and Experimental Evaluation for LLC Resonant Converter with Wide Battery Voltage Range	36-72 V	96%
2015	J. Deng	**Design of LLC Resonant Converters Based on Operation-Mode Analysis for Level Two PHEV Battery Chargers**	250-450 V	97.96%
2015	H. Haga	A Novel Modulation Method of the Full Bridge Three-level LLC Resonant Converter for Battery Charger of Electrical Vehicles	225-378 V	98.09%
2015	M. Li	The Integrated LLC Resonant Converter Using Center-Tapped Transformer for On-board EV Charger		95%
2016	I. Lee	**Hybrid PWM-Resonant Converter for ElectricVehicle On-Board Battery Chargers**	250-420 V	98.09%
2016	D.-J. Gu	High Efficiency LLC DCX Battery Chargers with Sinusoidal Power Decoupling Control	64-84 V	97.80%
2016	H.-G. Han	A High Efficiency LLC Resonant Converter with Wide Ranged Output Voltage using Adaptive Turn Ratio Scheme for a Li-ion Battery Charger	25-42 V	94.40%
2016	C.-C. Hua	**LLC resonant converter for electric vehicle battery chargers**	36-58 V	93.60%
2016	Z. Pang	High-frequency DC-DC Converter in Electric Vehicle Based on GaN Transistors	12 V	95%
2016	N. Shafiei	**Burst Mode Elimination in High-Power LLC Resonant Battery Charger for Electric Vehicles**	0-180 V	96.50%
2017	P.M. Johnson	A Dual-DSP Controlled SiC MOSFET based 96%-efficiency 20kW EV On-board Battery Charger Using LLC Resonance Technology	200-450 V	96%
2017	C. Shi	**A SiC-Based High-Efficiency Isolated Onboard PEV Charger With Ultrawide DC-Link Voltage Range**	100-420 V	97.10%
2017	X. Gumera	Design and Implementation of a High Efficiency Cost Effective EV Charger Using LLC Resonant Converter	43-65 V	96.30%
2018	M.I. Shahzad	**Interleaved LLC Converter With Cascaded Voltage-Doubler Rectifiers for Deeply Depleted PEV Battery Charging**	50-420 V	95.65%
2018	Z. Zhao	Efficiency Optimization Design of LLC Resonant Converter for Battery Charging	75-150 V	96%
2018	Y. Shen	**Full-Bridge LLC Resonant Converter With Series-Parallel Connected Transformers for Electric Vehicle On-Board Charger**	320-420 V	96.31%
2018	H. Vu	**A Novel Dual Full-Bridge LLC Resonant Converter for CC and CV Charges of Batteries for Electric Vehicles**	250-420 V	97%
2018	G. Cao	Design Optimization of LLC Converter for Battery Charger with Wide Output Voltage Range	250-420 V	95.90%
2019	S. Karimi	A Comprehensive Time-domain-based Optimization of a High-Frequency LLC-based Li-ion Battery Charger	45.6-50.2 V	97.01%
2019	H. Wang	**Design Considerations of Efficiency Enhanced LLC PEV Charger Using Reconfigurable Transformer**	250-450 V	97.47%
2019	R. Zhou	Natural convection cooled SiC-based LLC Resonant Converters in wide voltage range battery charger application	48 V	94.80%
2019	Y. Hu	6.6 kW High-Frequency Full-Bridge LLC DC/DC Converter with SiC MOSFETs	390-435 V	98%
2019	H. Li	A SiC Bidirectional LLC On-Board Charger	240-420 V	98%
2019	L. Shuguang	Design and Realization of High Power Density EV Charging Module	500-700 V	94%
2019	W.-S. Lee	**Design of an Isolated DC/DC Topology With High Efficiency of Over 97% for EV Fast Chargers**	50-650 V	97.32%
2020	C. Shen	**High-efficiency design method of LLC resonant converter for PHEV battery chargers (based on time-domain model)**	230-430 V	98.50%
2020	L.A.D. Ta	**High-Efficiency Hybrid LLC Resonant Converter for On-Board Chargers of Plug-In Electric Vehicles**	250-400 V	98.50%
2020	Y. Wei	**A Dual Half-Bridge LLC Resonant Converter With Magnetic Control for Battery Charger Application**	120-160 V	95.5%
2021	S.A. Arshadi	**Three-Phase LLC Battery Charger: Wide Regulation and Improved Light-Load Operation**	?-100 V	96%
2021	B. Xue	**Phase-Shift Modulated Interleaved LLC Converter With Ultrawide Output Voltage Range**	10-420 V	98.10%

D

Additional Experimental Results

Only the experimental results where V_{in} =525 V were given in Section 5.2. The results for V_{in} =689 V are presented in Table D.1.

Table D.1: All operation points that have been tested using the prototype of the current study, and their respective predicted (analytical) and measured efficiency. V_{in} =689 V for these operation points. ** See Limitations in Chapter 9.*

VD/CD	V_o	I_o	t_{dead}	D	f_{sw}	$\eta_{analytical}$	$\eta_{measured}$
CD	150	5	100	0.2177	113.40	0.9221	0.9441
		10	100		124.2	0.9594	0.9646
		15	100		103.5	0.9685	0.9696
		20	100		88.71	0.9712	0.9707
		25	100		77.62	0.9715	0.9700
		30	100		69.00	0.9708	0.9684
	320	5	100	0.4644	62.10	0.9492	0.9655
		10	100		181.39	0.9745	0.9782
		15	100		151.16	0.9809	0.9819
		20	100		129.56	0.9831	0.9829
		25	100		113.37	0.9837	0.9828
		30	100		100.77	0.9836	0.9823
	490	5	100	0.7112	149.79	0.9720	0.9796
		10	100		124.82	0.9857	0.9874
		15	100		106.99	0.9891	0.9893
		20	100		93.62	0.9902	0.9896
VD*	660	5	100	0.479	151.66	0.9752	0.9768
		10	100		113.74	0.9836	0.9828
		15	100		93.99	0.9840	0.9833
	830	5	100	0.6023	145.56	0.9809	0.9820
		10	100		109.17	0.9872	0.9868
	1000	5	100	0.7257	120.97	0.9862	0.9868
		10	200		90.73	0.9905	0.9898

E

Half Converter Operation

The VD mode could only be tested by using half of the converter (HB-A & HB-B) due to lack of equipment. It was possible, however, to test the CD mode using all four HBs (see Figure 7.2 for the location of all HBs). Table E.1 supplies evidence that the efficiency of the converter is significantly worse when operated with all HBs when compared to only using HB-A and HB-B. Even to the contrary; the efficiency at high power slightly worsens, while the improvements at low power increase by almost 0.5% in the best case.

Table E.1: Comparison between the efficiency in CD mode when only half of the converter is used (HB-A and HB-B) versus when the full converter is used.

VD/CD	V_o	I_o	t_{dead}	D	f_{sw}	$\eta_{measured}$ (1/2 Converter)	$\eta_{measured}$ (Full Converter)
CD	150	5	100	0.2857	113400	0.94998	0.95475
		10	100		94500	0.96766	0.97046
		15	100		81000	0.97281	0.97358
		20	100		70870	0.97370	0.97366
		25	100		63000	0.97364	0.97235
		30	100		56700	0.97264	0.97066
	320	5	100	0.6095	132250	0.97213	0.97580
		10	100		110210	0.98276	0.98412
		15	100		94460	0.98537	0.98600
		20	100		82660	0.98604	0.98596
		25	100		73470	0.98610	0.98530
		30	100		66120	0.98520	0.98428
	490	5	100	0.9333	34574	0.99270	0.99293
		10	100		28812	0.99486	0.99453
		15	100		24696	0.99506	0.99437
		20	100		21609	0.99485	0.99380

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