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Integrated Transceiver Circuits for Carotid and Intra-Cardiac Ultrasound Imaging

Integrated Transceiver Circuits for Carotid and Intra-Cardiac Ultrasound Imaging

Dissertation

for the purpose of obtaining the degree of doctor

at Delft University of Technology

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Chair of the Board for Doctorates

to be defended publicly on

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by

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To my parents

and

my family (Hyejin, Jaehyun and Jaewon)

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Chapter 1

Introduction

1.1 Motivation

Cardiovascular diseases (CVDs) are the leading cause of death globally [1]. However, most CVDs could, in principle, be prevented [2]. Various research activities investigating early detection of CVDs are ongoing [3], [4]. Imaging techniques often play a crucial role to aid diagnosis by visualizing the heart and blood vessels or to guide interventions [5]–[7]. Ultrasound imaging is an attractive technique in this context, as it is safer, more cost-effective, and easier to miniaturize compared to other imaging methods (e.g., CT, MRI) [8]. Therefore, ultrasound imaging is one of the most powerful diagnostic and monitoring tools for CVDs.

This thesis focuses on the use of integrated-circuit (IC) technology to enable new ultrasound imaging devices for better diagnosis and treatment of CVDs. In particular, we focus on two important applications: carotid-artery imaging and intracardiac echocardiography, which will be introduced in this section. In both cases, IC technology plays an essential role in realizing miniaturized imaging devices and enabling new imaging capabilities, such as three-dimensional (3D) imaging and high-frame-rate imaging. Although inspired by these two applications, the techniques presented in this thesis are equally applicable to other miniaturized ultrasound devices.

1.1.1 Carotid Artery Imaging

Atherosclerosis is one of the main reasons for stroke, and it is considered a disease that affects the entire vascular system, including cardiac performance. Fat, cholesterol and other substances found in the blood make plaques. The plaques harden and narrow the arteries, restricting blood flow and causing an arterial lesion with inflammation [9].

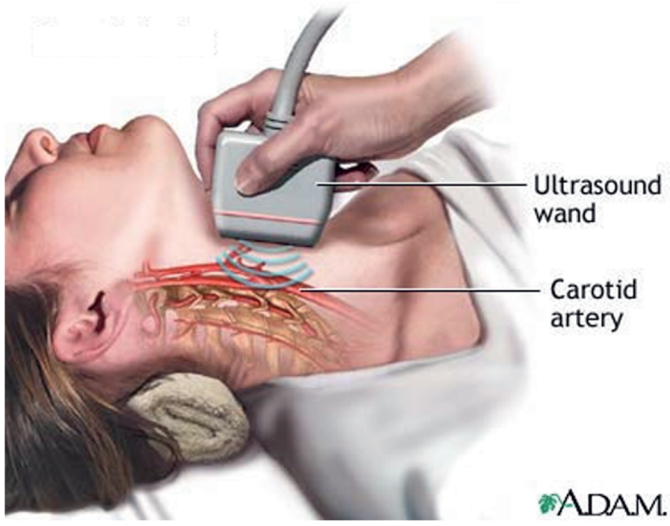


Figure 1.1 Carotid ultrasound to examine the carotid arteries
(https://medlineplus.gov/ency/imagepages/18051.htm)

As plaque development is gradual, mild Atherosclerosis usually does not lead to any symptoms. However, when there are symptoms, an artery is so narrowed or clogged that it cannot supply adequate blood. Therefore, early detection of atherosclerotic plaque is critical for preventing future cardiovascular events [10]–[12].

The left and right carotid arteries that supply blood to the head are important in this respect. Moreover, carotid artery plaques are associated with coronary artery atherosclerotic lesions. The carotid arteries are more readily assessable than the coronary arteries of the heart. Thus monitoring the carotid arteries could predict future CVD and coronary heart disease events [13].

Several modalities are used to image the carotid artery. Although Digital Subtraction Angiography (DSA) is primarily used for the assessment, DSA has risk factors due to the invasive nature of the examination, x-ray exposure, and the injection of nephrotoxic contrast agents [14], [15]. Computed Tomography Angiography (CTA) alleviates the stress of the invasive procedure, but it still relies on intravenous contrast agents and exposure to radiation. Magnetic Resonance Angiography (MRA) produces images without exposure to ionizing radiation. However, MRA is more expensive than other approaches and is less readily available [8].

Carotid imaging with ultrasound (Fig. 1.1) is a non-invasive, safe, and cost-effective technique. However, traditional two-dimensional (2D) imaging has limitations to provide accurate anatomy and orientation information. Therefore, successful 2D ultrasound imaging

of the carotid artery depends on the expertise of the sonographer, which could cause difficulties in proper diagnosis.

In this thesis, we explore integrated-circuit techniques that enable 3D imaging with a high frame rate and advanced imaging schemes. The proposed techniques pave the way towards 3D ultrasound probes that can solve the issue with 2D imaging and provide an accurate velocity profile of the blood flow. System- and circuit-level solutions will be proposed, implemented in a prototype probe, and demonstrated based on electrical and acoustical experiments.

1.1.2 Intracardiac Echocardiography

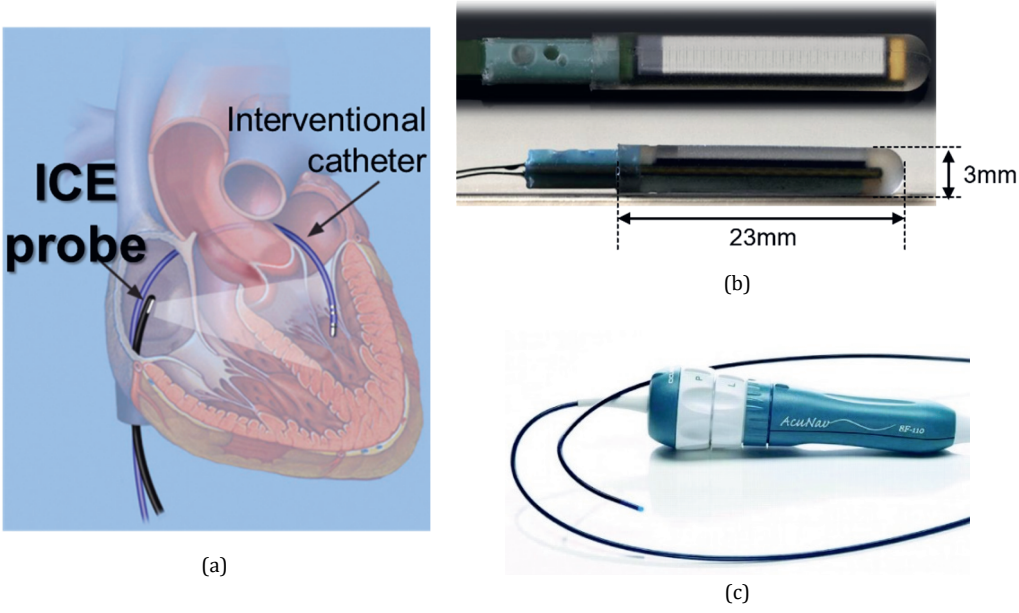
Interventional cardiology deals with the diagnosis and treatment of CVDs (e.g., coronary artery disease, heart valve disease, congenital heart disease, and vascular disease) in a minimally-invasive approach with catheter-based techniques. An accurate definition of the anatomy and precise diagnosis is essential for optimal results. Therefore, interventional cardiology procedures require advanced imaging for diagnosis and guidance of treatment [16].

Echocardiography uses ultrasound for real-time imaging of the heart. Echocardiographic images show the anatomy of the heart and motion in the heart, such as muscles, valves, and blood flow. Additionally, the images can be used to effectively detect possible blood clots inside the heart, fluid buildup around the heart, and many other cardiac problems. Hence, over the past decades, echocardiography has become an essential method to diagnose patients suffering from CVD [17].

There are two commonly-used types of echocardiography: transthoracic echocardiography (TTE) and transesophageal echocardiography (TEE) [18], [19]. In TTE, an ultrasound probe is placed on the chest to image the heart through an acoustic window in between the ribs. However, the images from TTE are sometimes not of sufficient quality because of the limited acoustic window, reflections from the ribs, and high attenuation associated with the large penetration depth from the skin to the heart. TEE resolves these issues by means of an ultrasound transducer mounted at the tip of a gastroscopic tube. The tube passes through the patient's mouth and into the esophagus to image the heart. Therefore, it does not have the issues with the window limitation and reflections from the ribs. Moreover, as the transducer is located closer to the heart, TEE can employ higher frequency transducers for better resolution. For those reasons, TEE is commonly performed for cardiac evaluation [20]. Although TEE provides superior cardiac images, it is uncomfortable for the patient and requires general anesthesia when applied during longer procedures, with the associated risk and discomfort after the procedure [21], [22].

Intracardiac echocardiography (ICE) employs a different path to approach the heart. Transducers are implemented on a catheter, and the catheter is threaded through the blood

vessels into the heart (Fig. 1.2). Thus, ICE provides images as good as or superior to TEE. ICE has additional advantages compared to TEE, such as patient tolerance, and lack of need for general anesthesia or a second operator [23]–[25].



(a) (b) (c)

Figure 1.2 (a) Application scenario of an ICE probe; (b) A catheter tip of an ICE probe (courtesy of Vermon); (c) An ICE probe (Siemens-healthineers ACUSON AcuNav 8 French ICE probe, https://www.siemens-healthineers.com/tr/ultrason-cihazlari/cardiovascular/acunav-ultrasound-catheter)

In this thesis, the electronic challenges associated with the implementation of next-generation ICE probes are discussed: the need to drive the transducers and amplify the received echo signals within the size and power constraints of a catheter. The thesis focuses on the implementation of integrated transceiver circuits to address these challenges. Solutions for both transmit and receive parts will be introduced, and the effectiveness of the proposed techniques will be verified based on experimental results from a prototype.

1.2 Background and Challenges

The vast majority of ultrasound probes for medical imaging employ piezoelectric transducer arrays to transmit ultrasonic pulses into the body and record the reflected echo signals to reconstruct images. Conventionally, the elements of such transducer arrays are interfaced to an external imaging system via cable connections. This approach is feasible when the number of elements is compatible with the number of cables that can be

accommodated in the probe's shaft, as is the case in conventional probes, of which the element count is up to 256 [20]. However, the step towards 3D imaging, which calls for the use of matrix (2D) transducer arrays, leads to a significant increase in element count [26], making direct connections to an imaging system unpractical, in particular in miniaturized probes [27]. Moreover, the smaller transducer elements used in 3D probes have a considerably higher electrical impedance than the elements of conventional probes, as a result of which the electrical loading due to cables leads to signal attenuation and loss of signal-to-noise ratio (SNR) [28]. The same problem occurs when the piezoelectric transducers that are conventionally used are replaced by capacitive micromachined ultrasound transducers (CMUTs). CMUTs are an emerging transducer type that can be produced in volume at lower cost and is thus attractive for cost-sensitive imaging devices such as disposable imaging catheters [29]. However, a challenge associated with the use of CMUTs is that they have a much higher electrical impedance than piezoelectric transducers, as a result of which SNR loss due to cable loading occurs not only for the small elements of a matrix array but even for the larger elements of a 1D array [30]. Increasingly, application specific integrated circuits (ASICs) in the probe are adopted to address these issues.

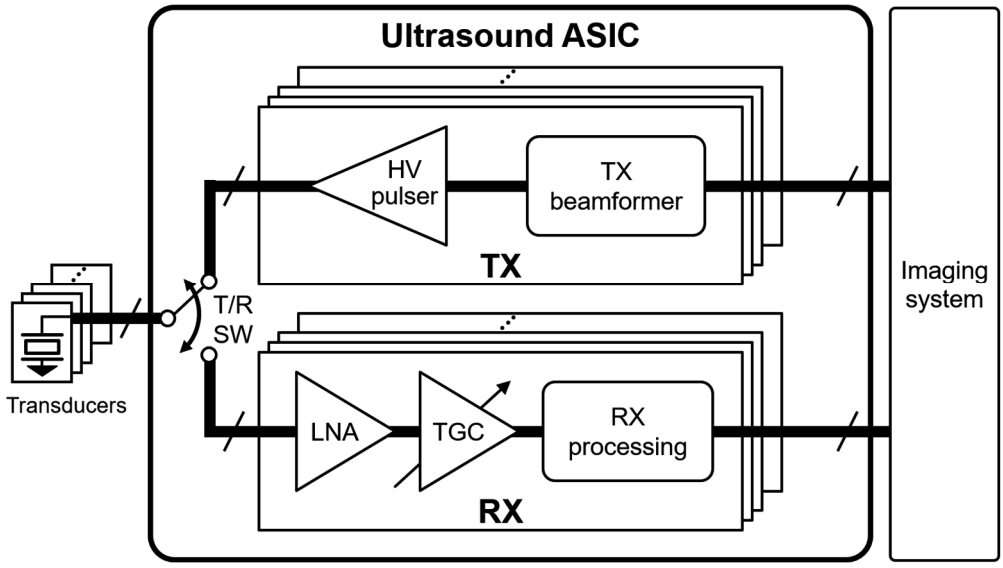


Figure 1.3 Ultrasound ASIC block diagram

Fig. 1.3 depicts a block diagram of an ultrasound ASIC that could be integrated into a probe to address the mentioned cable-count and SNR issues. The ASIC has transmit (TX) and receive (RX) circuitry for each element. The TX part consists of high-voltage (HV) pulsers and a TX beamformer to drive the elements and to generate an intended acoustic wave. It is connected

to the elements via transmit/receive (T/R) switches that prevent the HV pulses from damaging the low-voltage RX circuitry. After pulse transmission, these switches connect the elements to the RX part. This starts with a low-noise amplifier (LNA) to amplify the echo signals so that they can be further processed by the following circuitry, which may involve time-gain compensation (TGC) and further signal processing, such as beamforming and digitization [31], [32]. In this thesis, two different ASIC designs are proposed to implement optimized solutions for the carotid artery and ICE applications.

1.2.1 Ultrasound Probes for Carotid Artery Imaging

Currently, B-mode 2D ultrasound imaging is used to examine carotid arterial stenosis or dissection. For evaluation of the blood flow velocity in stenotic carotid arteries, Doppler ultrasound techniques are employed [33]–[35]. Thus, the degree of stenosis, the blood-flow distribution, and the shape of the plaque can be assessed. However, the 2D information obtained does not do justice to the 3D situation that needs to be assessed for accurate examination [36], [37]. Therefore, the 2D assessment can easily mislead the diagnosis. Mechanical 3D ultrasound approaches have been attempted to overcome this limitation [38]–[40]. But these have a low frame rate (~1 volume per second), making them poorly suited for artery assessment, and are prone to artifacts at proximal image areas. 3D ultrasound probes with matrix array transducers exist for other applications such as cardiac scanning. The matrix array reduces the processing time with phased-array beamforming and achieves a higher frame rate than mechanical probes, approximately 10~20 volumes per second [41], [42]. However, higher frame rates are desired, and the aperture of these existing probes is small compared to what is needed.

The blood velocity profiles and the wall thickness and stiffness are of utmost diagnostic interest for the accurate characterization of the carotid artery [43]. Since blood velocities are up to 1 m/s and spatial resolution in the order of 1 mm^3 is required, a very high imaging frame rate is needed, up to 1,000 frames per second [44]. Also, the assessment has to cover the bifurcation and the area of the stenosis. Therefore, a 3D probe for carotid-artery imaging needs to cover a relatively large aperture (>2 cm). It is very challenging to implement such a probe since a large matrix array is required to cover the aperture area and high-frequency operation is needed to support high frame rate images. The large matrix transducer leads to arrays consisting of thousands of transducer elements, exceeding the channel count that conventional imaging systems can handle.

Implementing ASICs into the probe enables the reduction of the required cable count. Various schemes have been reported to reduce the cable count, such as a sub-array beamforming [26], [31], [45], switch matrices [46], [47], row-by-row connection [48], [49], and reconfigurable row- or column-parallel connection [50]. In addition to the cable count reduction, [48], [49] introduced the concept of using an array of ASICs to cover a large aperture area. In [48], [49], flip-chip bonding is adopted to integrate the transducer and the

ASIC. In [31], [32], the transducers are directly implemented at the top of the ASIC, avoiding the interface complexity of the flip-chip bonding. However, even taking those efforts into account, further optimization and improvements in cable-count reduction, high-frame-rate operation, and implementation of advanced imaging schemes are required for carotid artery ultrasound imaging. In chapter 2, system and circuit design techniques to implement a 3D high-frame-rate ultrasound probe for the carotid artery will be presented.

1.2.2 Ultrasound Catheters for Intracardiac Echocardiography

Various approaches have been developed to realize ICE probes. In the early days of ultrasound catheters, the probes used a mechanically-rotating single-element transducer to achieve cardiac imaging [21]. In the early-1990s, phased-array transducers were used for ICE with Doppler imaging. ICE achieved successful clinical results, and its use expanded. Further improvements were achieved with 2D array transducers for real-time 3D imaging [28], [51]. However, the approach's drawback is a direct connection between the individual transducer elements and the external imaging system through cables. The cables form a substantial parasitic load to the elements. Especially, in a matrix transducer array, the elements are much smaller than in a linear array transducer. Thus, they have a large impedance mismatch with the cables, which causes signal loss. Moreover, the catheter diameter limits the implementable cable count, which defines the element count. These limitations make the direct connection approach unsuitable for a 3D ICE probe based on a matrix transducer array. Therefore, in recent 3D ICE devices, application-specific integrated circuits (ASIC) are implemented at the tip of the catheter to resolve these issues [20]. These ASICs include an analog front-end with an input impedance better matched to the transducer elements, thus resolving the signal loss due to loading, and can provide various cable-count reduction schemes.

In this thesis, a custom ultrasound ASIC for a 64-element ICE probe based on Capacitive Micromachined Ultrasound Transducers (CMUTs) is presented. The design focuses on realizing a transmit (TX) beamformer and a receive (RX) analog front end (AFE). The proposed TX beamformer drives the transducer elements with high-voltage (HV) bipolar pulses to generate enough pressure to get a high signal-to-noise ratio at the target imaging depth. The AFE includes a low-noise amplifier (LNA) with time-gain compensation (TGC), which reduces the echo-signal dynamic range by compensating for propagation attenuation. The key challenge is to realize these functions within the stringent size and power-consumption constraints of an ICE probe.

1.3 Organization of the Thesis

The organization of this thesis is arranged as follows.

Chapter 2 presents an ultrasound ASIC to realize a probe for high-frame-rate 3D carotid artery imaging. A row-level RX and TX bus scheme is proposed to reduce the number of cables required to connect the probe to an imaging system. An element-level switch circuit and reconfigurable logic are implemented to control which transducer elements are active and to support advanced imaging schemes. Acoustical experiments with a prototype 24 × 40 piezoelectric transducer array built on top of the ASIC show the effectiveness of the proposed techniques. Imaging experiments successfully demonstrate the 3D-imaging capability of the prototype.

Chapter 3 presents a programmable transmit beamformer with bipolar high-voltage (HV) pulsers designed for ICE. The advantage of bipolar pulsing with possible circuit configurations is discussed in detail. Based on this discussion, a compact HV pulser design including a return-to-zero (RZ) switch is constructed. The RZ switch also serves as transmit/receive switch to minimize the required chip area. A new floating-gate driver that uses only a single HV transistor provides level-shifting functionality to turn on and off the HV MOS transistors in the pulser. Electrical results obtained with the ASIC demonstrate the functionality of the HV pulser. TX beamforming experiments in combination with a 64-element CMUT array validate the capability of the TX beamformer.

Chapter 4 extends the transmit beamformer discussed in the previous chapter with receive functionality to realize a transceiver ASIC designed for ICE. This includes LNAs to amplify the echo signals and TGC to reduce their dynamic range. The chapter gives an overview of existing TGC circuits with a discussion of their advantages and limitations. Then system architecture and circuit techniques are presented to implement an LNA with built-in TGC functionality, as a more compact and power-efficient alternative to conventional solutions with a separate LNA and TGC amplifier. The operation principle of the proposed TGC scheme is described with an analytical analysis of the capacitive feedback network. Electrical measurements demonstrate continuous gain control to within ±1 dB. Imaging results obtained using a prototype employing a 64-element CMUT array demonstrate the effectiveness of the proposed techniques, showing that the proposed topology is a promising solution for ultrasound ASICs.

Chapter 5 concludes the thesis by highlighting the main contributions and the main findings. Suggestions for future improvement and research are also presented.

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Chapter 2

A Reconfigurable Ultrasound ASIC for 3D Carotid Artery Imaging

This chapter is based on the publication "A Reconfigurable Ultrasound Transceiver ASIC with 24 × 40 Elements for 3D Carotid Artery Imaging," in IEEE Journal of Solid State Circuits, vol. 53, no. 7, pp. 2065-2075, July 2018, and "A programmable and tileable PZT matrix transducer with integrated electronics for 3D real-time ultrasound imaging," in preparation.

2.1 Introduction

Atherosclerosis (the formation of plaques in the blood vessels) is the main source of cardiovascular events, such as stroke, infarct, and aneurysm, and a main cause of death worldwide [1]. The left and right carotid arteries that supply blood to the head are very important in this respect. Plaque is known to build up, especially near the bifurcation of the carotid. Such plaques may obstruct the blood flow or even be prone to rupture and are the major cause of stroke. Furthermore, the carotid arteries reflect the general progression of systemic atherosclerotic disease and are well accessible for assessing the arterial wall thickness and stiffness [2], [3].

The identification of vulnerable atherosclerotic plaques, which are susceptible to rupture and, therefore, candidates for intervention, is a central issue in vascular imaging. Plaque vulnerability is related to dimension, composition, mechanical stress distribution, and inflammation state, which are the targets for plaque assessment. Currently, no suitable method exists for large-scale early screening of patients at risk: 2D ultrasound imaging is too

limited, X-ray exposure of CT is prohibitive, and MRI is too expensive and logistically unsuited. Real-time 3D ultrasound is an ideal tool for fast, complete, and highly effective carotid screening.

Currently, B-mode 2D ultrasound imaging is used to evaluate carotid artery disease. The degree of stenosis and its impact on the local blood flow distribution, the shape of a plaque, and possible calcium deposits can be visualized by B-mode 2D ultrasound imaging. However, the 2D character of all these measurements is a serious limitation. They are performed in a single position or single plane, while, in fact, a complex three-dimensional situation needs to be assessed. Therefore, the disease can be easily under- or overestimated [4].

Accurate assessment of carotid artery disease by measuring blood flow, plaque deformation, and pulse-wave velocity using ultrasound requires real-time 3-D images [5]–[8]. To generate such images, the next generation of ultrasound probes for carotid artery imaging requires matrix transducer arrays. It is highly challenging to build such probes since the transducer array needs to cover a relatively large aperture (>2 cm) while operating at 5 MHz or higher, leading to arrays of thousands of transducer elements, far exceeding the number of channels that conventional imaging systems can handle and that can be connected using a manageable number of cables.

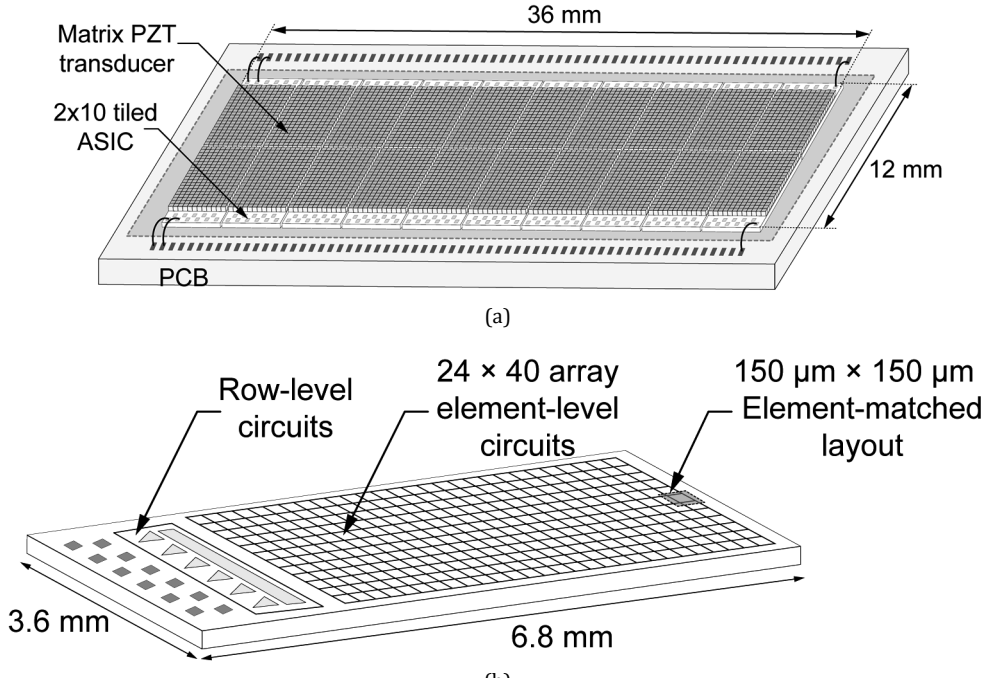


Figure 2.1. (a) Overview of the proposed matrix transducer on tiled ASICs; (b) overview of a single ASIC.

This problem can be addressed by building ASICs into the probe to reduce the number of cables. Various approaches have been reported to interface matrix transducer arrays using a reduced number of cables. Programmable pulsers have been used to locally generate the high-voltage pulses needed to drive the transducer elements [9]–[15]. Part of the receive beamforming can be performed locally in the probe to combine the signals received by a sub-array into one output signal [12], [16], [17]. Switch matrices have been proposed that connect groups of elements that transmit and receive simultaneously [18], [19]. Row-by-row scanning schemes [13], [15], and reconfigurable row- or column-parallel connection schemes [14] have also been reported.

In this chapter, we propose an ASIC with a row-level architecture for both RX and TX channels [20]. The ASIC consist of 24 × 40 element-level circuits, consisting of TX switches, RX switches and control logic, that allow each element to be selectively connected via row-level RX and TX buses to an imaging system. This leads to 40-fold channel reduction. The element-level circuitry fits in the 150 μm × 150 μm area occupied by a single 7.5 MHz transducer element, allowing the transducer array to be integrated directly on top of the ASIC. The chip-level layout allows for multiple ASICs to be tiled to form even larger transducer arrays. The on-chip logic allows a variety of different element selection patterns to be programmed.

The chapter is organized as follows. Section 2.2 describes the architecture and functionality of the ASIC. Section 2.3 presents the circuit details of the element-level and row-level circuits. Section 2.4 and 2.5 provide measurement setup and experimental results, and Section 2.6 concludes the chapter.

2.2 System Architecture

2.2.1 Matrix Transducer Configuration

To cover an aperture sufficient for carotid-artery imaging, the matrix transducer area targeted in our work is 12 × 36 mm^2. Since this area is rather large to cover with a single die, we propose to tile 2 × 10 ASICs, as shown in Figure 2.1a. Each of these ASICs, as shown in Figure 2.1b, has a die size of 3.6 × 6.8 mm2, and interfaces with a (sub-)array of 24 × 40 transducer elements through element-level and row-level circuits. Connections to the transducer elements are made through an array of bondpads, which are positioned such that a contiguous 150 μm-pitch transducer array can be built on top of the tiled ASICs. The ASICs will be arranged in a head-to-head fashion, similar to that reported in [13], [15], so that bondpads on the periphery of each ASIC allow for row-level connections to an imaging system via a PCB substrate.

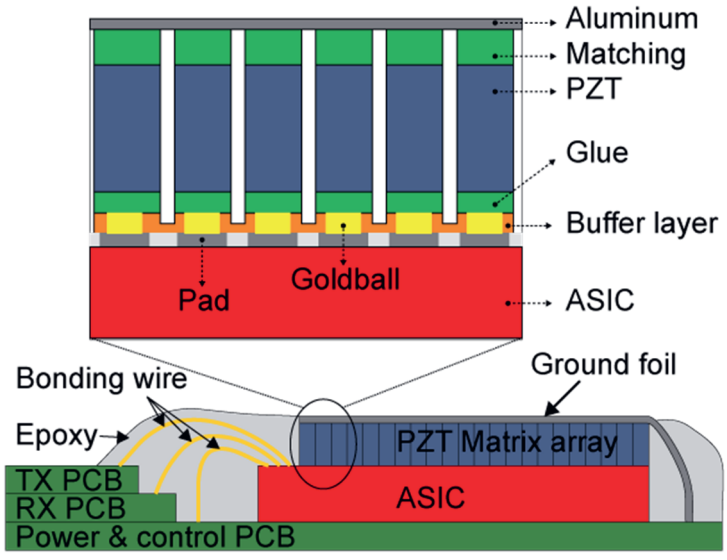


Figure 2.2. Cross-sectional view of the transducer array mounted on top of the ASIC

The transducer array is directly built on top of the ASICs using the PZT-on-CMOS integration scheme illustrated in Figure 2.2 [21]. The bond pads on the ASIC that provide electrical connections to the transducer elements are equipped with gold bumps using a wire-bonding tool. After this, an epoxy buffer layer is applied to ASIC that is grinded down to expose the gold, thus providing reliable electrical contacts for the transducer elements. The acoustic stack consisting of a piezo-electric layer (PZT) and a matching layer is glued on top of the grinded epoxy layer, which is cut into the desired 150-µm-pitch array pattern using a diamond saw. Finally, the array is covered with an aluminum foil that forms the common ground electrode of the elements.

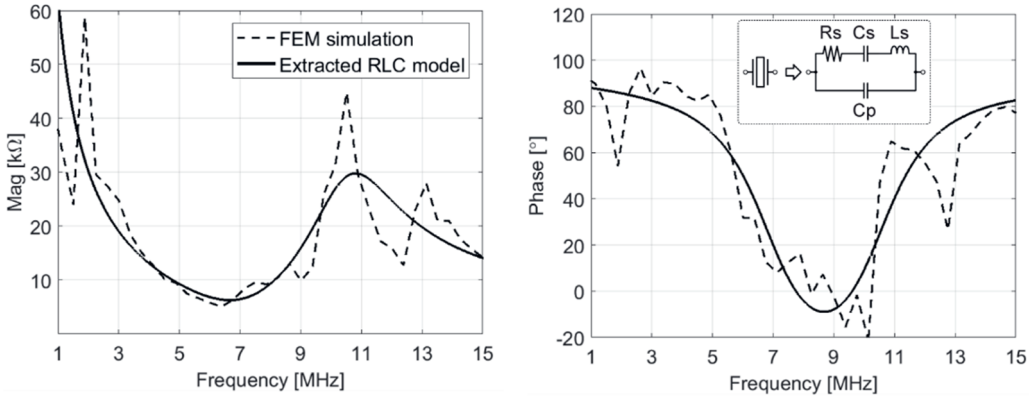


Figure 2.3. Simulated electrical impedance characteristic of a transducer element, along with a Butterworth-Van Dyke lumped-element model.

The transducers have a center frequency of 7.5 MHz and a bandwidth of about 45 %. The impedance characteristic of the transducer elements has been simulated using finite-element analysis software (PZFlex LLC, Cupertino). Their electrical impedance around resonance can be modeled with a Butterworth-Van Dyke model, as shown in Figure 2.3, with an impedance of approximately 1.2 pF // 6.8 kΩ at resonance. The elements have an estimated transmit efficiency of 20 kPa/V at 45 mm from the transducer, requiring to transmit voltages in the order of tens of Volts to generate sufficient acoustic pressure to be useful for carotid imaging. Their receive sensitivity (estimated by referring the measured output voltage of the ASIC back to an equivalent voltage at the terminals of an unloaded transducer) is around 4 μV/Pa.

2.2.2 ASIC Architecture

Figure 2.4 shows the top-level architecture of the proposed ASIC. To achieve channel count reduction, the 40 elements in each row of the matrix share a row-level RX and TX bus, thus reducing the number of channels by 40×. This approach is similar to that reported in [14]. These row-level RX and TX buses can be shared by neighboring head-to-head positioned ASICs in a tiled configuration, so that rows of 80 elements are formed that span two ASICs and share one RX and TX line. Thus, the channel count is manageable even for large arrays with tiled ASICs. Each transducer element is associated with a programmable element-level switch circuit that allows the element to be connected to the RX bus or the TX bus. The RX line connects to a shared row-level low-noise amplifier (LNA) and cable driver.

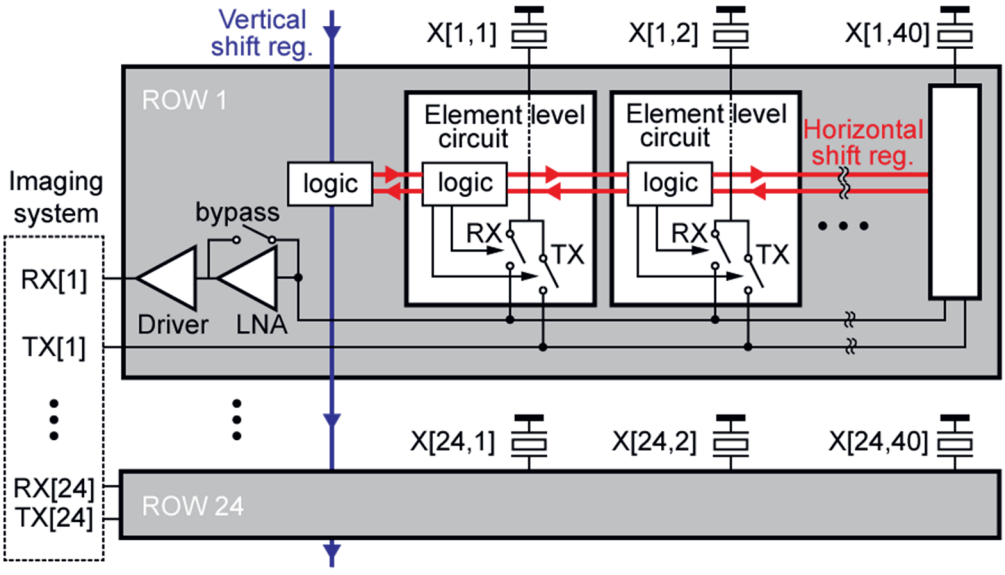


Figure 2.4. Block diagram of the ASIC.

The ASIC enables rapid reconfiguration of the selection of elements used for RX and TX, aiming for application in high-frame-rate volumetric imaging of the carotid artery. Control logic, programmed through row-level and element-level logic, determines whether an element participates in a given transmit and/or receive cycle. Element-level memory, which can be pre- loaded through a shift register, allows the selection of active elements to be rapidly changed between successive transmit/receive cycles.

To enable pulse transmission on all elements in the array, we use high-voltage (HV) switches to connect the elements to pulse generators in the imaging system via the row-level TX bus. Compared to the use of integrated pulsers [9]–[11], [16], [22], [23] or high-voltage linear amplifiers [24], [25] per element, this approach consumes less die area, thus facilitating smaller pitch arrays, and reduces power dissipation in the probe. Moreover, it allows for a broader range of transmit waveforms. After transmission, each element can be connected through a RX bus, a row-level LNA, and a cable driver to a receive channel of the imaging system. To extend the dynamic range of the receive path, the LNA can be bypassed at high signal levels or enabled at low signal levels.

2.2.3 Reconfigurablity

Through reconfigurable per-element logic, the ASIC supports a variety of aperture selections for different imaging schemes (Figure 2.5), including column-by-column selection for synthetic aperture transmission and/or reception (Figure 2.5a), full-aperture selection for plane-wave transmission (Figure 2.5b), arbitrary element selections (Figure 2.5c) and pseudo-random sparse element selections (Figure 2.5d). Each element is equipped with memory bits that define whether the element participates in TX and in RX. These bits can be loaded in various ways, allowing different trade-offs between programming time and flexibility (Figure 2.6). All element-level memory cells (flip-flops) are part of a shift register, which can be loaded in a daisy-chain fashion to be able to define arbitrary selections (Figure 2.6a). If the selection pattern is identical in all rows (like in Figure 2.5a and Figure 2.5b), the shift register can also be loaded in a row-parallel fashion (Figure 2.6b), thus significantly reducing the programming time. For even faster reconfiguration, each element is equipped with 9 memory bits for RX and 9 bits for TX, so that 9 arbitrary patterns can be pre-programmed and the ASIC can switch between these patterns with a single clock pulse (Figure 2.6c). Finally, the memory content can also be shifted to neighboring elements, from left to right (Figure 2.6d) or right to left (Figure 2.6e), to laterally translate the selected aperture. This allows the matrix transducer to be operated as an electronically-scanned linear array. Each element is also associated with an enable bit (EL_EN) that is not shifted, allowing non-functional elements to be excluded.

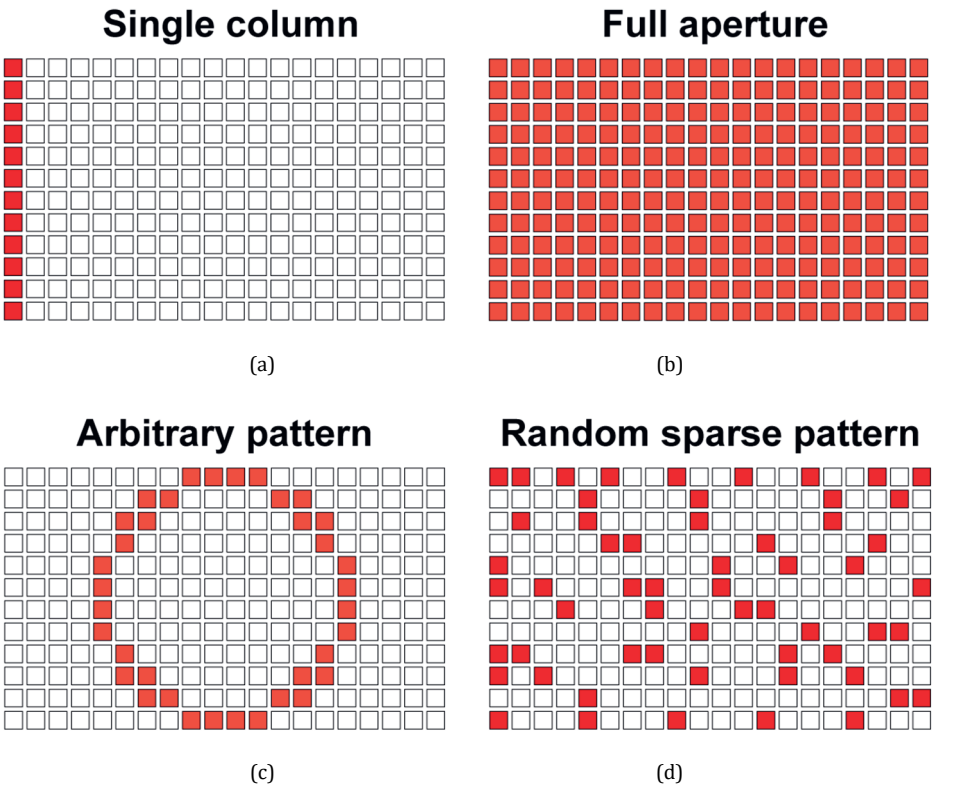


Figure 2.5. Element-selection modes supported by the ASIC: (a) single-column selection; (b) full-aperture selection; (c) selection of arbitrary sets of elements; (d) pseudo-random element selection.

The reconfigurability can be used to fulfill different imaging tasks. The plane wave transmission and column-by-column readout depicted in Figure 2.5a provides excellent spatial, almost isotropic resolution, but it comes at the cost of lower temporal resolution because of the 40 transmit/receive events needed to obtain all the signals. If a higher temporal resolution is required, for example, to capture fast transient phenomena in the carotid artery, an image mode may be selected where multiple columns are grouped together, such that fewer transmit/receive events are needed to address the complete array. Besides the gain in temporal resolution, this imaging mode would also offer a gain in SNR, since several elements signals are averaged. At the flipside, these gains come at the cost of lower spatial resolution in at least one direction. The imaging mode with random element grouping (Figure 2.5d) will enable more advanced imaging methods. By predicting the pulse-echo signals and random grouping in a linear system matrix, we can formulate the reconstruction as an inverse imaging problem, as we have recently shown in [26] by imaging a 3D volume using only one transducer.

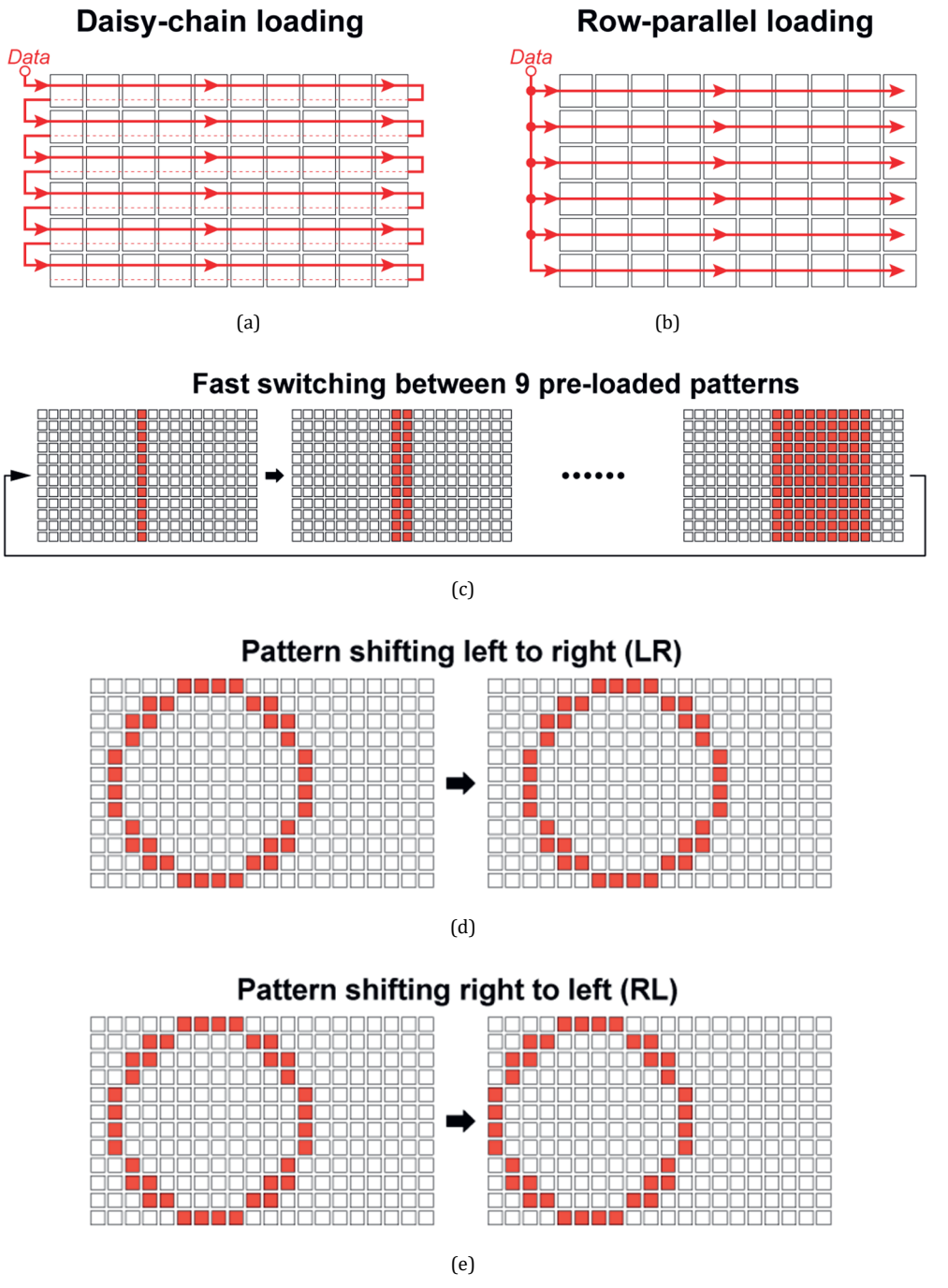


Figure 2.6. Ways of reconfiguring the element selection: (a) daisy-chain loading; (b) row-parallel loading; (c) switching between 9 pre-loaded patterns; (d) pattern shifting from left to right and (e) from right to left.

The shift register can operate at frequencies up to 50 MHz, and is buffered, so that it can be loaded during imaging without affecting the operation of the ASIC. TABLE 2-1 summarizes the amount of data that needs to be loaded in the different modes, and the associated loading time. Except when 9 arbitrary patterns are pre-loaded, the loading time is less than or comparable to a typical pulse-echo interval of 50 μs (which corresponds to an imaging depth of 35 mm), so that the imaging frame rate is not reduced by the loading operation. In the case of pre-loaded patterns, pattern switching can be done with a single clock pulse (i.e., < 1 μs), so that frame rate is also not affected.

TABLE 2-1. UNITS FOR MAGNETIC PROPERTIES CONFIGURATION DATA AND LOADING TIME ASSOCIATED WITH THE DIFFERENT CONFIGURATION MODE

Mode	Bits/element	Total bits	Loading time
Row-parallel	RX, TX, EL_EN	$3 \times 40 = 120$	2.4 μs
Daisy-chain	RX, TX, EL_EN	$3 \times 960 = 2880$	57.6 μs
Row-parallel with 9 patterns	RX[1:9], TX[1:9], EL_EN	$19 \times 40 = 760$	15.2 μs
Daisy-chain with 9 patterns	RX[1:9], TX[1:9], EL_EN	$19 \times 960 = 18240$	365 μs

2.3 Circuit Implementation

2.3.1 Element-Level Switches

Figure 2.7 shows a circuit diagram of the element-level switches with the associated timing diagram, for a transducer element X[i,j] located in row i, column j. This circuit connects the element to the row-level transmit bus TX[i] during the TX phase ϕTX if TX_en[i,j] = 1, and to the row-level receive bus RX[i] during the RX phase ϕRX if RX_en[i,j] = 1. The enable bits TX_en and RX_en are defined by the element-level memory (see Section 2.3.3).

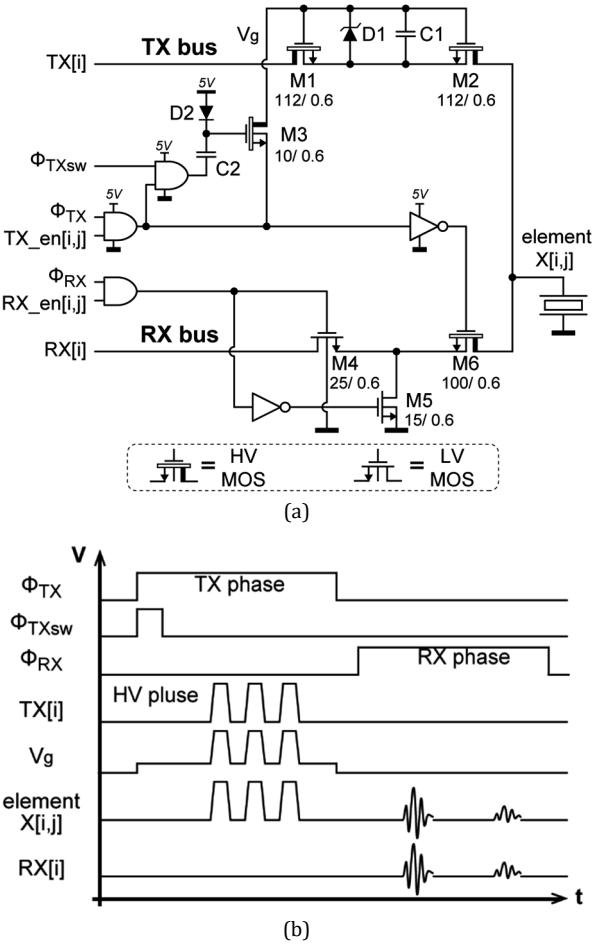


Figure 2.7. (a) Simplified circuit diagram of the element-level switches, for an element located in row i, column j; (b) associated timing diagram.

To be able to switch unipolar TX pulses with a peak value up to 30 V, two back-to-back N-type HV LDMOS transistors (M1 and M2) connect the element to the TX bus. This structure is similar to the HV switch described in [27]. Compared to a switch based on a single HV transistor, the back-to-back configuration reduces the capacitive loading of the transducer element by the switch during the RX phase, which would cause undesired signal attenuation, to about 1 pF. Moreover, it is robust in the condition in which neighboring elements are shorted together, which may occur due to transducer fabrication issues. These advantages come at the cost of a larger layout area for a given on-resistance. In principle, this configuration also supports bipolar pulses, as in [27], but this is not supported by the gate-drive circuit in our design. The size of transistors M1 and M2 is maximized within the available die size, to minimize the power loss associated with their on-resistance, leading to a combined on-resistance of about 180 Ω.

Instead of using a latch circuit to turn on the switch transistors, as in [27], we use a more compact implementation. M1 and M2 are turned on by charging a bootstrap capacitor C1 connected between their source and gate through M3 at the beginning of ϕTX. Shortly after, M3 is turned off, leaving M1 and M2 turned on and allowing them to swing up with the transmit pulses on the TX bus. At the end of the TX phase, the source of M3 is pulled down to discharge C1 and turn off M1 and M2.

Due to parasitic capacitance to ground at the gate of M1 and M2, part of the charge stored on bootstrap capacitor C1 is lost as the voltage on the TX bus rises. To ensure that M1 and M2 maintain sufficient overdrive, C1 should be made sufficiently large, 7.2 pF in our case. A MIM capacitor is used, so that this capacitor can be placed on top of the HV devices and hence does not increase the die size.

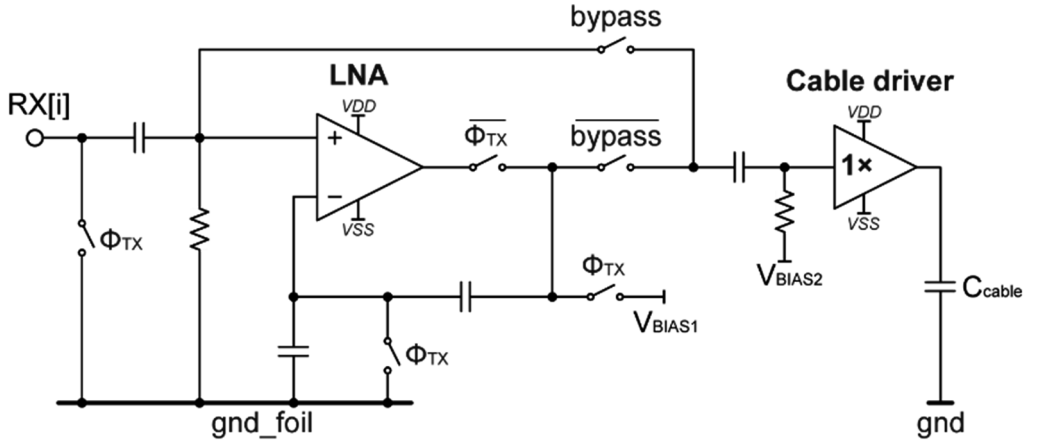
Transistor M3 is turned on through C2 and D2. When ϕTXsw is low, D2 charges C2 to 5 V. During a short pulse of ϕTXsw at the beginning of ϕTX, the voltage at the gate of M3 is pumped above 5 V to turn on M3 and thus charge C1. C2 has sufficient capacitance (1.8 pF) compared to the capacitance at the gate of M3 to ensure sufficient gate-driving voltage. A diode-connected vertical NPN device is used to implement diode D2, so as to minimize the injection of current into the substrate when this diode is forward biased.

Transistors M4 and M6 prevent the HV pulses from reaching the RX bus and connect the element to the RX bus during ϕRX. When multiple elements are selected, they are connected in parallel to the RX bus, causing their signals to be averaged. M5 prevents the signal of non-selected elements from coupling to the RX bus. Moreover, in the TX phase, M5 turns on with M6 to connect the element to ground if it is disabled. Thus, capacitive coupling from the TX bus to the disabled elements is strongly reduced. To reduce the on-resistance of the HV switches, the element-level circuit uses a 5 V supply to drive the LDMOS, while the logic operates from a 1.8 V supply. Level-shifters (not shown) interface between these supply domains. The RX switch is sized to have an on-resistance of 280 Ω. This is well below the element's resistance, so that the noise contribution of the RX switch is negligible.

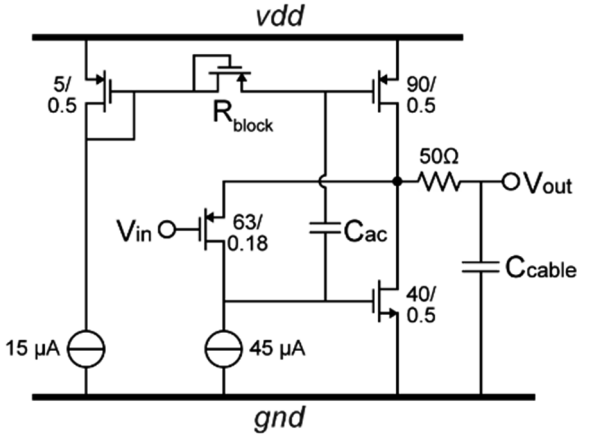
2.3.2 Row-Level Switches

To prevent signal attenuation due to the loading of the cables connecting the ASIC to the imaging system, the signal on the row-level RX bus is amplified by a row-level LNA, and buffered by a cable driver (Figure 2.8a). The LNA consists of a PMOS-input folded-cascode amplifier with non-inverting capacitive feedback, realizing a gain of 9 (19 dB) with a -3 dB bandwidth in excess of 20 MHz. To obtain an input-referred thermal noise below that of the transducer element, the input stage of the amplifier is biased at 580 μA, yielding a simulated input-referred noise level of 5.8 nV/√Hz at 7.5 MHz. The total current consumption of the amplifier is 790 μA. To avoid noise coupling or interference, the capacitive feedback network is connected to the ground foil of the transducer array, rather than to the (analog) ground of

the ASIC. The signal is AC coupled at the input of the LNA. During the transmit phase ϕTX, when the receive path is not active, the RX bus is grounded, and the capacitive feedback network of the LNA is pre-charged so that its output is biased close to mid-supply, to maximize signal swing. To prevent the LNA from limiting the dynamic range, it can be bypassed at high signal levels, at the cost of a higher input-referred noise level, to implement a rudimentary single-step time-gain compensation (TGC) function. A TGC implementation involving finer gain steps and a larger gain range, e.g. as in [17], would enhance the dynamic range and improve the image quality but was not implemented in this prototype for simplicity.



(a)



(b)

Figure 2.8. (a) Simplified circuit diagram of the row-level receive circuits;
(b) Schematic of the cable driver. The transistor sizing is in µm.

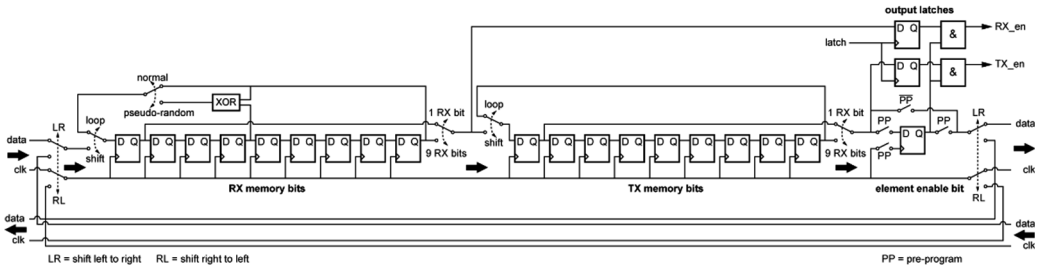


Figure 2.9. Simplified circuit diagram of the element-level logic.

The LNA is A coupled to a unity-gain cable driver, based on a class-AB super source-follower topology [17], [28], shown in Figure 2.8b. Biased at 285 μA, it is capable of driving the capacitive load of up to 300 pF of the cable connecting the probe to the imaging system. The complete receive path consumes 2 mW per row from a 1.8 V supply.

As the row-level architecture shares an LNA through RX switches and an RX bus, the associated parasitic capacitance at the input of the LNA results in signal attenuation. This capacitance includes the capacitance of the RX switch, of the TX switch, of the RX bus and of the RX switches of the non-selected elements in the row. This amounts to approximately 4.5 pF and causes about 5.6 dB signal attenuation in the band of interest if a single element is selected per row. If multiple elements are selected, this attenuation becomes less. For instance, it decreases to 3.1 dB for four elements.

2.3.3 Logic

To implement the element-selection modes described in Section 2.2.3, each element is equipped with a reconfigurable logic circuit (Figure 2.9), which determines whether the element participates during transmit (TX_EN) and receive (RX_EN). The core of this circuit is a shift register consisting of 9 flip-flops for 9 RX-enable bits, 9 flip-flops for 9 TX-enable bits and 1 flip-flop for an element-enable bit (EL_EN), which allows a defective element to be disabled independent of the TX and RX enable bits. This element-enable bit is only part of the shift-register chain when PP=1, otherwise it is bypassed. This allows the element-enable bits to be pre-programmed only once, after which patterns can be updated without re-loading these bits. The output of the shift register is latched using two additional flip-flops, allowing the shift-register content to be updated without affecting the operation of the element. New content only becomes active after a rising edge of the latch signal.

The shift register is daisy-chained between neighboring elements in a row. The daisy-chain connection of the shift register allows the configuration bits to be shifted into a neighboring element, so as to realize the pattern-shifting operation shown in Figure 2.6. To be able to shift both left-to-right (LR) and right-to-left (RL) (cf. Figure 2.6d and Figure 2.6e), logic is included

that can reverse the shift-register connections between neighboring elements, which is conceptually represented using switches in Figure 2.9.

In the simplest mode of operation, only one of the 9 RX flip-flops and one of the 9 TX flip-flops is used; the remaining 8 bits are by-passed, so that only one RX bit and one TX bit need to be loaded per element to define whether the element is enabled during RX and TX. In order to pre-program 9 different patterns for fast pattern switching, as in Figure 2.6c, this bypass is not used, allowing 9 bits to be loaded for RX and 9 bits for TX. After loading, the output of RX section of register is looped back to its input, as is the output of the TX section. Thus, the 9 pre-loaded enable bits can cyclically be applied.

Finally, the RX section of the register has a pseudo-random mode, in which this section is turned into a 9-bit linear-feedback shift register (LFSR) in which an XOR combination of two shift-register bits is fed back to the input. This causes the elements to be enabled for RX in a pseudo-random manner, which can be used to implement compressive sensing schemes. The 9 bits that are initially loaded into the RX-section act as a seed value for this LFSR. This allows different seed values to be used for different elements, causing them to exhibit a different pseudo-random pattern.

The various control signals needed to define the operating mode of the element level logic are provided by row-level logic. The row-level logic circuits together form a vertical shift register (see Figure 2.4) through which each row can be configured independently.

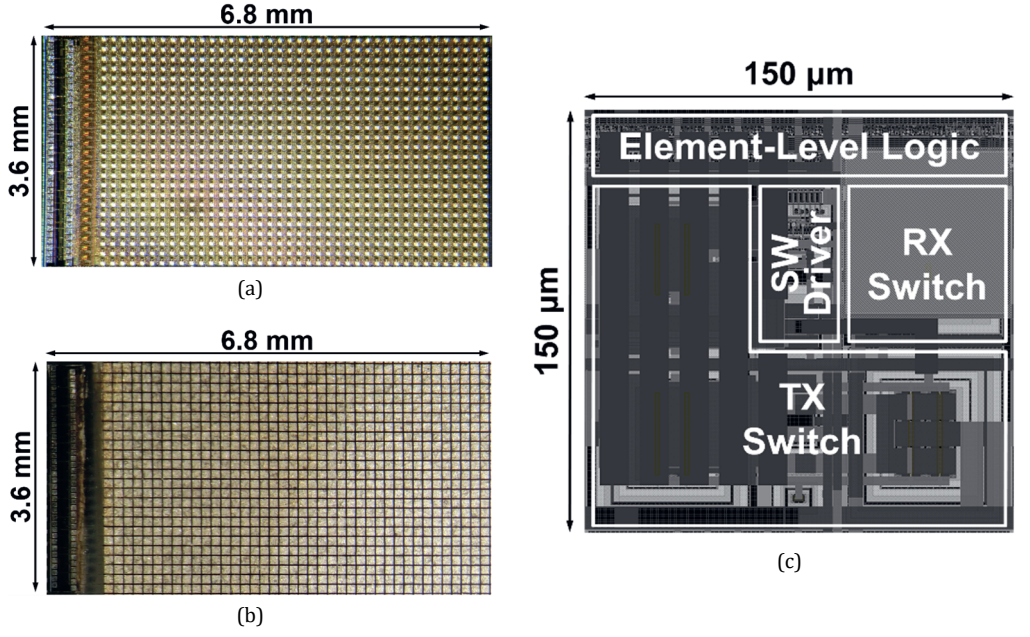


Figure 2.10. (a) Chip photo of the ASIC; (b) with transducer array; (c) layout of the pitch-matched element-level circuit.

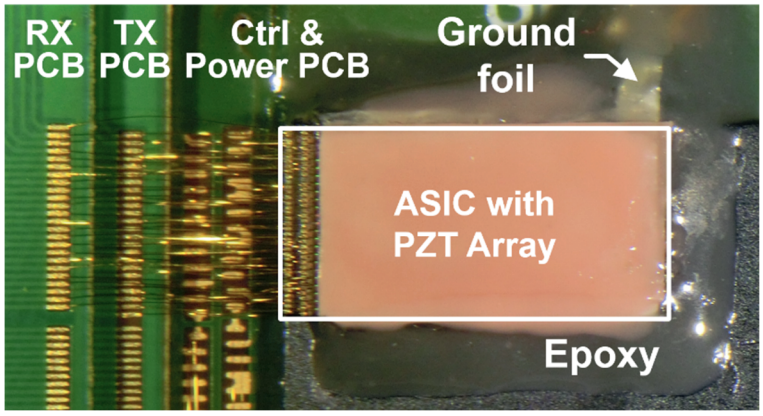


Figure 2.11. Photograph of an ASIC with transducer array bonded to a stack of PCBs and protected with epoxy.

2.4 Measurement Setup

2.4.1 Experimental Prototypes

The ASIC has been fabricated in 0.18 µm high-voltage BCDMOS process. Figure 2.10 shows a photograph of a bare die and of a die after fabrication of the transducer array, and the floor-plan of a single element. The layout of the element-level TX and RX circuits is matched to the 150 µm transducer-element pitch.

The ASIC is wire-bonded to a stack of three printed-circuit boards (PCBs) with cable connectors (Figure 2.11), which provide connections for the RX and TX channels as well as for power and control signals. After assembly, the prototype is covered by a ground foil that forms the common ground electrode of the transducer elements, and by a moisture protection layer.

2.4.2 Electrical Characterization

We mounted a bare ASIC (without PZT array) on a daughterboard. This was used as a test sample to evaluate the electrical performance of the ASIC and the whole signal chain from the ASIC to the ultrasound machine, including the cables and the motherboard. A wire bond was made between a randomly selected element bond-pad on the ASIC and an externally accessible test pad on the daughterboard. The transmit, receive, power and control bond-pads on the ASIC were wire bonded to the daughterboard in the usual way. After programming the ASIC a known signal from an AWG was applied to the test bond pad and the corresponding output signal was recorded. In this way we could assess the electrical

performance of the ASIC and the signal chain in different modes, e.g. with the LNA active or bypassed, and with the TX and RX switches on or off.

2.4.3 Acoustical Characterization

Figure 2.12 shows a schematic diagram of the setup for the acoustical evaluation of the transducer. For this purpose, the daughterboard was mounted in a box with an acoustically transparent window (25 µm thick polyimide) and the whole setup was submerged in a tank filled with deionized water. To test the transmit performance, the Verasonics was used to excite the matrix transducer. To prevent undershoot or overshoot voltages which could cause latch-up or junction breakdown, matching networks are included on the motherboard. The RX signals from the ASIC are buffered on the motherboard and fed into the Verasonics. The motherboard also provides supply voltages for analog, digital and 5V circuitry. The board also contains digital buffers to transfer control signals for row-level logic and element-level logic from the FPGA board.

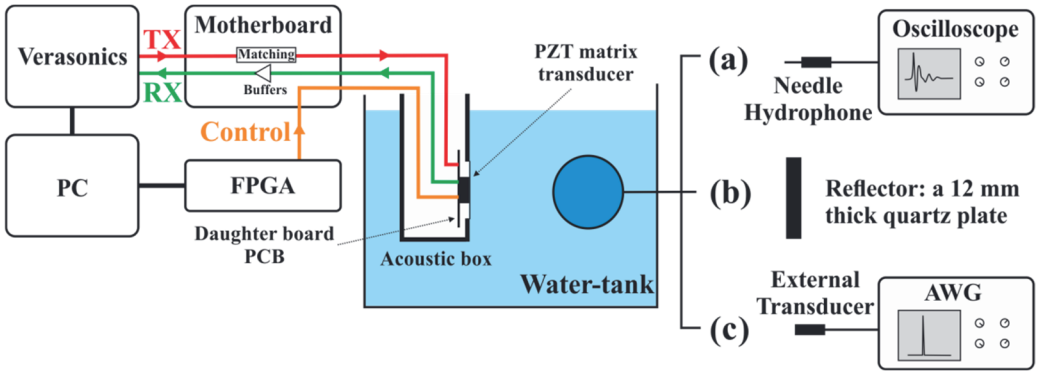


Figure 2.12. A schematic drawing of the acoustical measurement setup. (a) Transmit performance: a needle hydrophone is connected to a digital oscilloscope to measure the transmit pressure from the transducer. (b) Pulse-echo performance: a 12 mm thick flat quartz plate is used to reflect the pressure pulse back to the transducer. (c) Receive performance: an external transducer is excited with an arbitrary waveform generator to obtain a known incident wave on the transducer.

The produced pressure was detected by a calibrated 1 mm needle hydrophone (Precision Acoustics, Dorchester, UK), and the hydrophone output was recorded using a digital oscilloscope (DSOX4054A, Keysight Technologies, Santa Rosa, CA, USA), see option (a) in Figure 2.12. To test the pulse-echo performance of the transducer, a 12 mm thick quartz plate was placed in the far field of the transducer (at 100 mm), see option (b) in Figure 2.12. The transducer was excited by the Verasonics and the reflected pressure was detected by the transducer at different settings. To test the receive performance, a 0.5 inch 7.5 MHz transducer (V320, Olympus Corporation, Tokyo, Japan) was excited by an arbitrary

waveform generator (33250A, Agilent Technology, Santa Clara, CA, USA), and the generated pressure was detected by the matrix transducer, these option (c) in Figure 2.12.

2.5 Experimental Results

2.5.1 Electrical Characterization Results

For electrical characterization, a die without transducer array was used on which selected transducer bond pads were wire-bonded to the lowest PCB, to be able to apply external test signals to the ASIC and to measure the TX voltage produced by the ASIC.

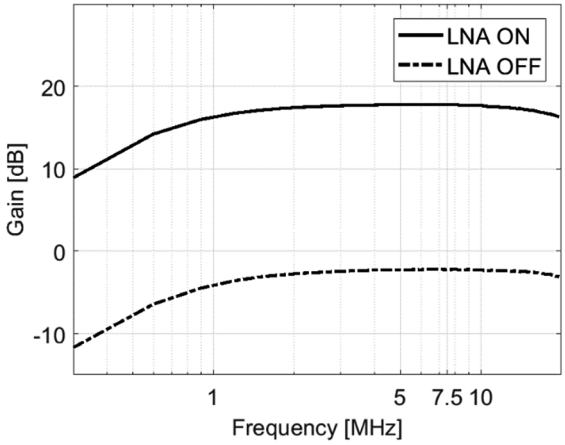


Figure 2.13. Measured transfer function of the receive path.

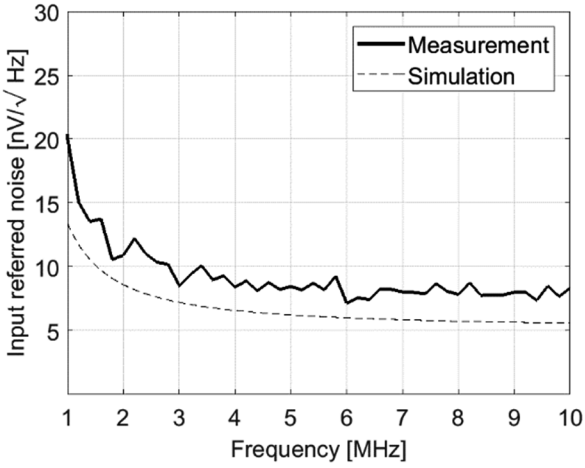


Figure 2.14. Measured input-referred noise spectrum of the LNA, along with the corresponding simulation result.

Figure 2.13 shows the measured transfer function of the receive circuit with the LNA in the signal path (LNA ON) and with the LNA bypassed (LNA OFF). The measured gains at the center frequency of 7.5 MHz are 18 dB and -2 dB, respectively. The gain step is in good agreement with the designed 20 dB gain of the LNA. The small attenuation observed for LNA OFF is due to capacitive division associated with the AC-coupling capacitors at the input of the LNA and the cable driver. The 1dB compression point is reached at a peak-to-peak input voltage of 74 mV with LNA on and at 750 mV with LNA off.

The noise performance of the LNA was measured by shorting the input of the LNA, measuring the output noise and referring this back to the input by dividing it by the transfer function. The resulting noise spectrum, shown in Figure 2.14, is in good agreement with simulations. The measured input-referred noise density is 7.9 nV/$\sqrt{}$Hz at 7.5 MHz. Although this is higher than the noise level expected based on simulations, it is still less than the noise associated with the 6.8 kΩ impedance of the transducer (and substantially better than the noise level reported in [20], which was dominated by noise of off-chip components in the measurement setup). The difference with the simulated noise level may be due to noise picked up at the input of the LNA. In the electrical test, the LNA input was ground by wire-bonding a transducer bond pad to gnd on the PCB, instead of to gnd_foil, to which the LNA input is referenced (as shown in Figure 2.8a). This was done because gnd_foil is not readily accessible for wire-bonding. We suspect that this different reference point is responsible for the additional noise. Integrated over the 40% fractional bandwidth of the transducer, the measured noise density leads to an input-referred rms noise of 13.7 μV, which is equivalent to an acoustic noise floor of 7.2 Pa.

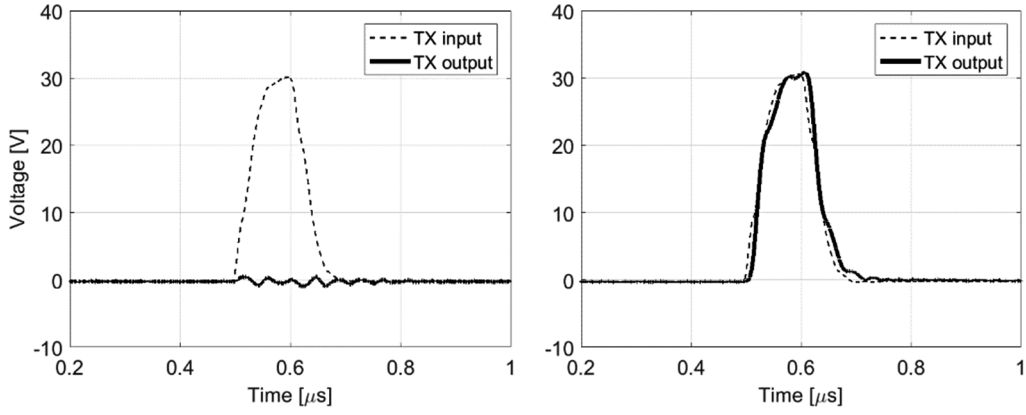


Figure 2.15. Measured input and output of the transmit path, showing the operation of the high-voltage TX switch: (a) TX switch off; (b) TX switch on.

To verify the operation of the bootstrap switch, we applied a 30 V peak-to-peak 200 ns pulse to one of the TX channels and probed the transducer bondpads. As Figure 2.15 shows, the switch successfully propagates and isolates the HV signal.

To explore the linearity of the electronic system and the saturation limit of the chip, test signals were applied to the test bond pad of the daughterboard, and the resulting output signals were recorded at three different locations: (1) at the input of the buffer on the motherboard, (2) at the output of the buffer on the motherboard (i.e. at the input of the Verasonics), and (3) at the output of the analog-to-digital (A/D) converter inside the Verasonics. The measurements were performed for two ASIC settings (LNA on and LNA off) and five Verasonics settings (constant TGC gains 100, 300, 500, 700, and 900). All other receive settings of the Verasonics were kept at the default values. A 50 cycle sinusoidal signal with 7.5 MHz frequency was used as a test signal. The amplitude of the test signal was increased in steps until the output signal was saturated. The output amplitudes are obtained from the spectral peak of the windowed output signal.

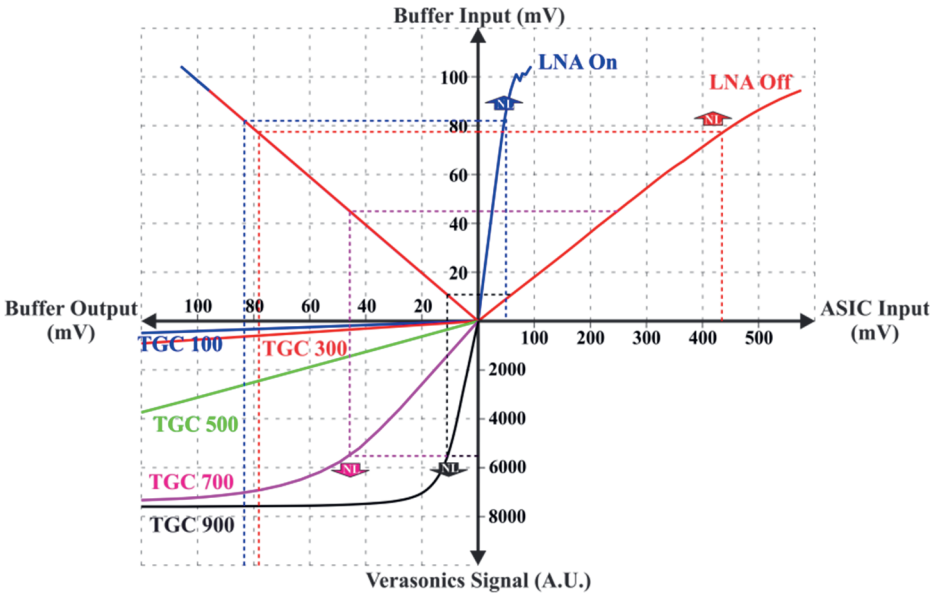


Figure 2.16. Performance of the electronics chain from ASIC input to Verasonics A/D converter output. The first quadrant shows the relation between the ASIC input and the ASIC output for LNA on and LNA off. The second quadrant shows the linear performance of the buffers. The third quadrant shows the relation between the input and the A/D converter output of the Verasonics, for several TGC gains.

The results of the electrical characterization are presented in Figure 2.16. In the first quadrant, the relation between the input and output of the ASIC is given for both LNA settings.

At high voltages, nonlinear deformation of the signal is observed, which is due to the saturation of the chip. The saturation level is defined here as the level where the higher harmonics rise above -20 dB (relative to the amplitude of the fundamental). The saturation input voltage for LNA on is 48 mV and for LNA off is 443 mV. Both values correspond to an output signal of approximately 80 mV. In the second quadrant, the performance of the buffer on the motherboard is analyzed. The two curves verify that the buffer is performing in the linear regime, and the buffer gain is 1. In the third quadrant, the relation between the input voltage and the A/D output signal of the Verasonics is shown for different TGC gains. The curves show that with TGC gains of 700 and 900, the signals above 5500 units are nonlinear, which is caused by saturation of the Verasonics electronic system. For the TGC gains of 100, 300, and 500, the Verasonics signal are always in the linear range, and they are limited by the saturation of the ASIC.

In a separate measurement, the frequency response of the ASIC was examined for LNA on and LNA off. For this purpose, a 50 cycle sine signal with an amplitude of 10 mVpp was applied to the test pad on the motherboard, and the frequency was swept from 0.5 MHz to 20 MHz in steps of 0.1 MHz. The output signal of the ASIC was measured with a digital oscilloscope (DSOX4054A, Keysight Technologies, Santa Rosa, CA, USA). The variations in the frequency responses for both LNA settings are within -1 dB between 1.3 MHz and 20 MHz, which means a reasonable flat frequency response in the frequency range of interest. Furthermore, a gain of 20 dB is measured for LNA on.

2.5.2 Acoustical Experiments

2.5.2.1 Element Configurations

To test the configurability, the FPGA was programmed to activate different patterns of transmit elements on the ASIC. In every test all 24 rows were excited in parallel with a unipolar pulse with a center frequency of 7.5 MHz and an amplitude of 25 V, generated by the Verasonics. Similar to option (a) in Figure 2.12, a hydrophone was mounted on a controllable xyz positioning stage, and used to measure the pressure in a plane parallel to the transducer at approximately 2 mm distance. To observe the pattern of active elements, the pressure was recorded in this xy plane, using 30 points at 0.3 mm increment in both x and y directions. After scanning, the maximum of the envelope of the pressure was calculated for all measurement points. The results are shown in Figure 2.17. The dashed rectangle in the figure shows the size and approximate position of the transducer array, and the element configurations are indicated in the insets at the top-right corners.

Figure 2.17a, 17b, and 17c show the ability to electronically change the width of the aperture. Figure 2.17d, and 17e show the possibility of electronically shifting a selected aperture. In Figure 2.17f, a random selection of five elements was chosen. The transmit

beams from the single elements are quite similar, which implies a low sensitivity variation between these elements.

The effect of aperture width on the transmit beam in the xz plane was also investigated by both simulation and measurement. First, the ASIC was programmed to transmit with 8, 16, 24, and 32 active columns. The hydrophone was used to scan the xz plane with 30 points at 0.3 mm increment in the x-direction and 50 points at 2 mm increment in the z-direction. Similar to the xy scan, the maximum of the envelope of the pressure is computed for each measuring point. The results are shown in Figure 2.18a to 18d.

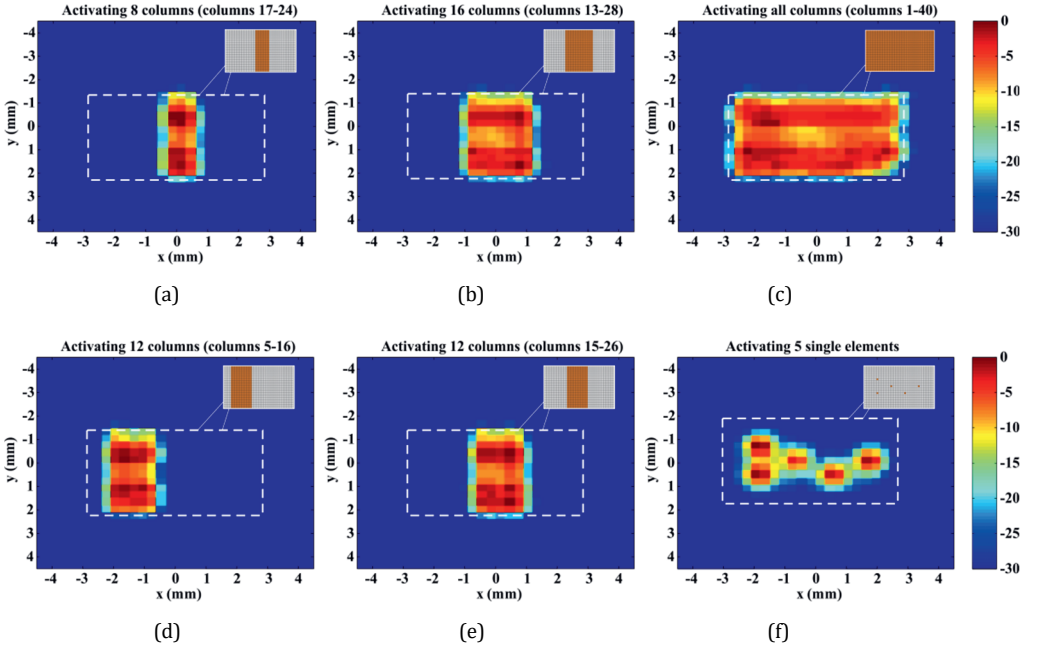


Figure 2.17. Transmit pressure measured by a hydrophone in the xy plane at approximately 2 mm from the transducer surface, for different element configurations, (a) selection of 8 columns (columns 17-24), (b) selection of 16 columns (columns 13-28), (c) selection of all columns (columns 1-40), (d) selection of 12 columns (columns 5-16), (e) selection of 12 columns (columns 15-26), (f) selection of 5 elements with random location.

Second, a simulation in Field II was performed for comparison. For this purpose, a 2D matrix array with 24 rows and j columns (j=8,16,24,32) is defined, with 130 µm wide elements and 20 µm wide kerfs in both x and y direction. A Gaussian modulated sinusoidal signal with 3 periods and 7.5 MHz center frequency was considered for the impulse response of the elements. The xz plane was discretized by using grid points from -4.5 mm to 4.5 mm with 0.1 mm distance in the x direction, and from 1 mm to 100 mm with 1 mm distance in the z direction. Again, the plots of the transmit beam were based on the maximum envelope of

the pressure in the grid points. The resulting simulated beams for different aperture sizes are shown in Figure 2.18e to 18h.

For all cases, the shape of the measured beam is qualitatively in good agreement with the simulated beam. Since the measurement is done with a 1 mm needle hydrophone, the plots of the measured beam show an averaged pressure over the aperture of the hydrophone. Therefore, as compared to the simulation, the measurement results are smoothened in the x direction. By increasing the width of the aperture, the natural focus of the beam shifts to higher depths. This is observed for both the measured and the simulated results.

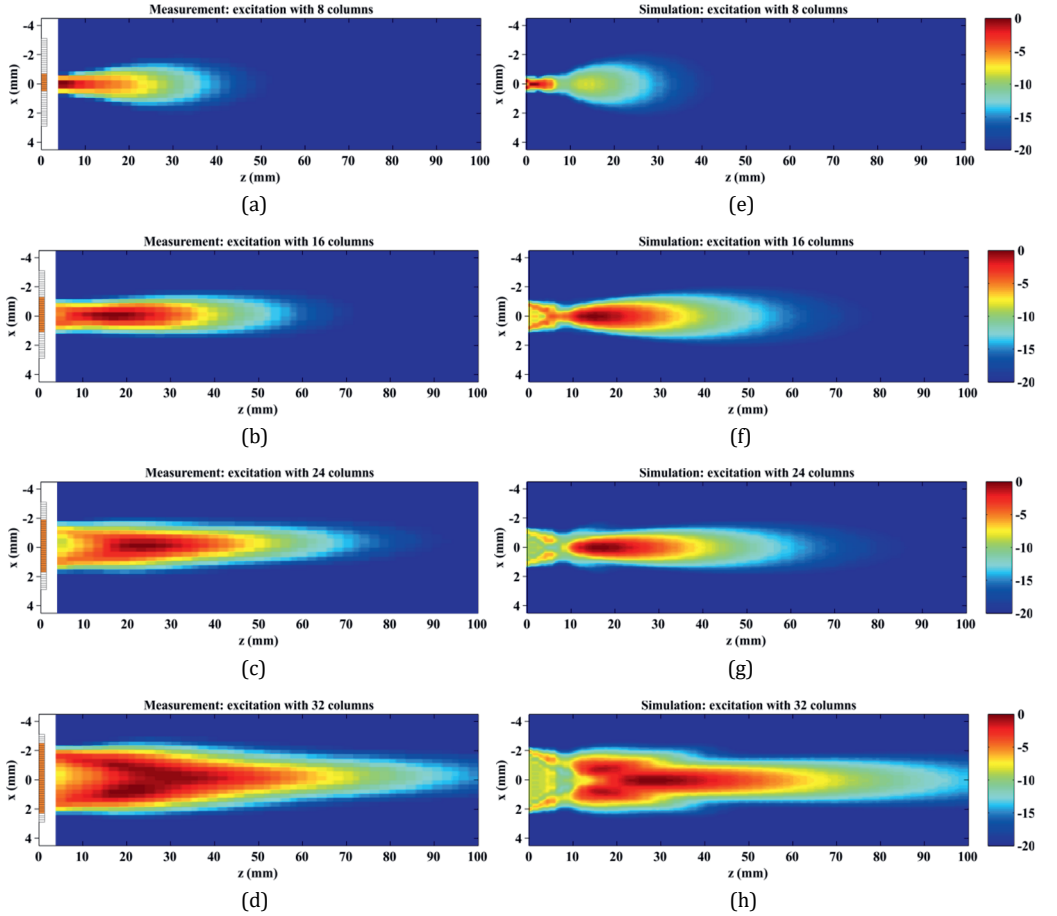


Figure 2.18. Simulation and measurement results for the transmit beam in the xz plane, for with different apperture widths. (a) measurement with 8 active columns (columns 17-24), (b) measurement with 16 active columns (columns 13-28), (c) measurement with 24 active columns (columns 9-32), (d) measurement with 32 active columns (columns 5-36), (e) simulation with 8 active columns, (f) simulation with 16 active columns, (g) simulation with 24 active columns, (h) simulation with 32 active columns.

To demonstrate fast reconfigurability of the ASIC, 9 different TX patterns were programmed in the element-level memory, allowing the ASIC to cyclically switch between these patterns in response to a single clock pulse (cf. Figure 2.6c). The pressure in a C-plane (i.e. parallel to the transducer) at 2 mm from the transducer was recorded using a needle hydrophone placed on an x-y stage. Figure 2.19 shows, for each of the 9 patterns, the measured peak acoustic pressure distribution in this plane, confirming that the ASIC is activating the elements in agreement with the pre-programmed patterns.

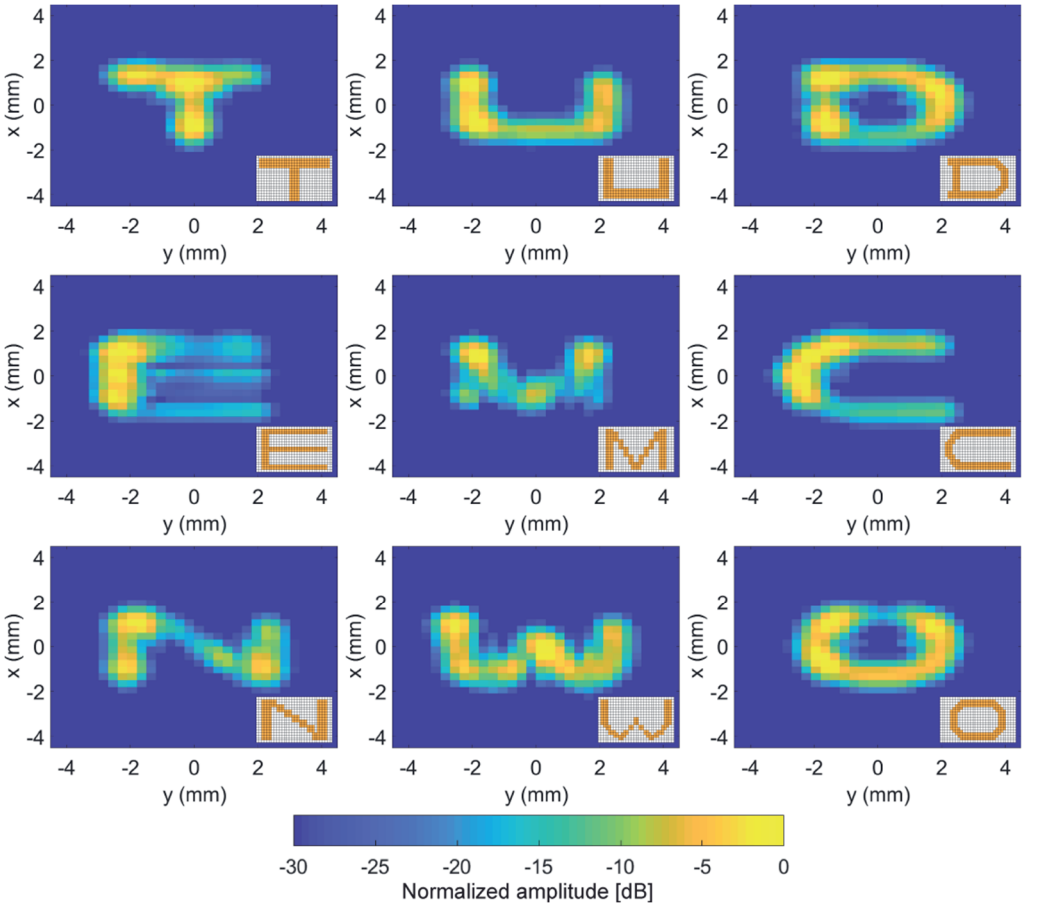


Figure 2.19. Peak pressure recorded at 2 mm from the transducer array, using a hydrophone scanning a plane parallel to the array, for 9 pre-programmed transmit patterns.

2.5.2.2 Sensitivity and Efficiency Analysis

To measure the sensitivity variations between different elements, the prototype transducer was used in a pulse-echo measurement, see option (b) in Figure 2.12. An acoustic

pressure wave was generated by sending a unipolar pulse with center frequency of 7.5 MHz, and 30 V amplitude to all the elements of the transducer array. A quartz plate with 12 mm thickness was placed at 100 mm away from the transducer. The distance of the reflector was chosen to be far enough to mimic a plane wave coming back to the transducer. The reflected echo signals from all individual elements were recorded separately by the Verasonics. The amplitude of the signal received by each element was determined from the first reflected pulse. To normalize the sensitivity of the elements, the maximum amplitude among all elements was used. The resulting sensitivity plot is given in Figure 2.20a.

Row 7 suffers from a problematic wire-bond and therefore there was no meaningful output from the daughterboard for that row. The first two columns and some elements on the edges of the array have suffered some damages during the fabrication process. Figure 2.20b shows the number of elements within 1 dB sensitivity ranges. In this plot, row 7, and columns 1 and 2 have been excluded. This figure shows that the majority of the elements are within the 0 dB to -6 dB level of two-way (pulse-echo) sensitivity range.

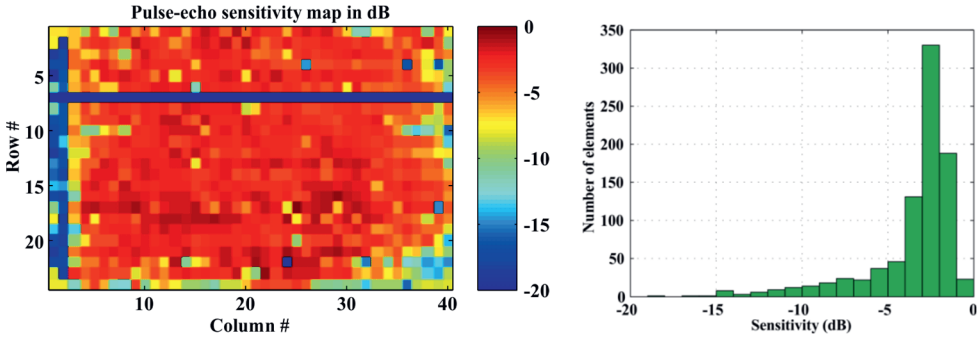


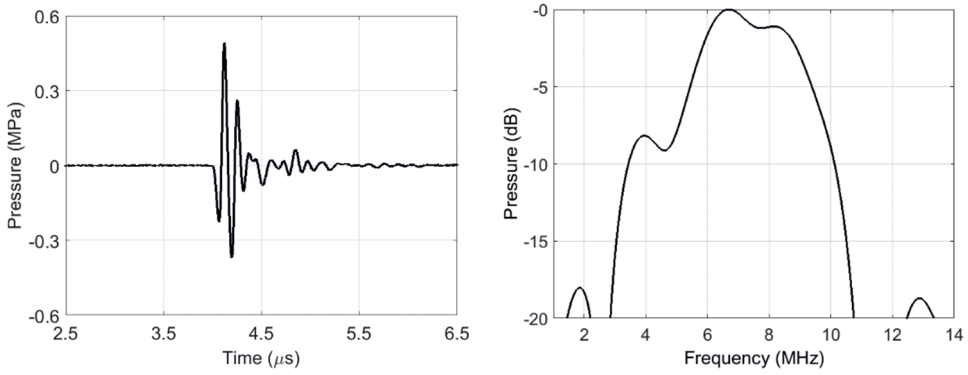
Figure 2.20. (a) Pulse echo sensitivity map, (b) number of elements within different sensitivity ranges.

2.5.2.3 Time and Frequency Response

Figure 2.21 presents the acoustic pressure recorded with a 1 mm needle hydrophone placed at 50 mm when all elements are pulsed simultaneously. The TX signal is a unipolar half-cycle 7.5 MHz pulse with a peak value of 25 V. The recorded pressure has a maximum of 0.5 MPa. Its frequency spectrum shows a central frequency of 7.4 MHz and a -3 dB bandwidth of 44%. The measured bandwidth is in agreement with the expectation for a transducer built on top of an ASIC [21]. The measurement presents ringing after the main pulse due to acoustic reflection from the backside of the chip.

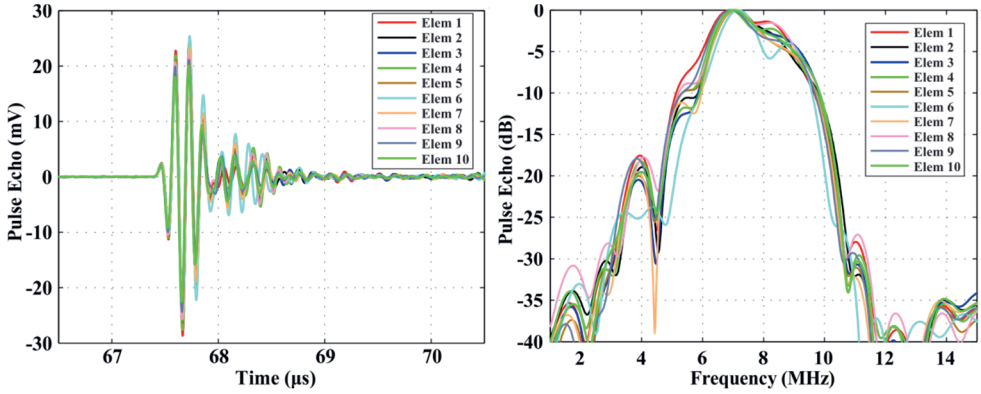
To perform pulse-echo measurements, the 12 mm thick quartz plate was placed at approximately 100 mm from the transducer. All elements were excited simultaneously with the pulse described above, and the reflected pressure was measured by individual elements.

The resulting time and frequency responses for 10 randomly selected receive elements are plotted in Figure 2.22. The measured responses for the elements are similar.



(a) (b)

Figure 2.21. Measured acoustic pressure recorded with a hydrophone:
(a) time-domain waveform, (b) frequency spectrum.



(a) (b)

Figure 2.22. Receive pressure from the pulse-echo measurement, measured by 10 randomly selected individual elements, (a) time response, (b) frequency response.

2.5.2.4 Directivity Pattern

The directivity of a single element was measured and compared with finite element simulations in PZFlex. As schematically indicated by option (c) in Figure 2.12, an external transducer was placed at approximately 100 mm from the matrix array, and excited by two cycles of a 7.5 MHz sine, generated by an AWG. This produces a plane, pulsed wave at the array surface. The matrix array was then rotated from -60o to 60o with steps of 1o, and the pressure was recorded by all transducer elements and averaged. The directivity pattern was

obtained from the peak of received signals at each angle, and normalized to the value at zero degree. The resulting directivity pattern is the blue curve in Figure 2.23.

Also, a finite element model similar to Figure 2.2 was constructed in PZFlex to analyse the directivity of a single element in the matrix array. Two cases were considered for the simulation study: (1) loading the transducer elements directly with water, and (2) considering an intermediate layer (25 µm thick polyester sheet, mimicking the acoustically transparent window in the acoustic box) between the transducer elements and the water. The obtained directivity patterns for case 1 and case 2 are indicated by the green and red curves, respectively, in Figure 2.23.

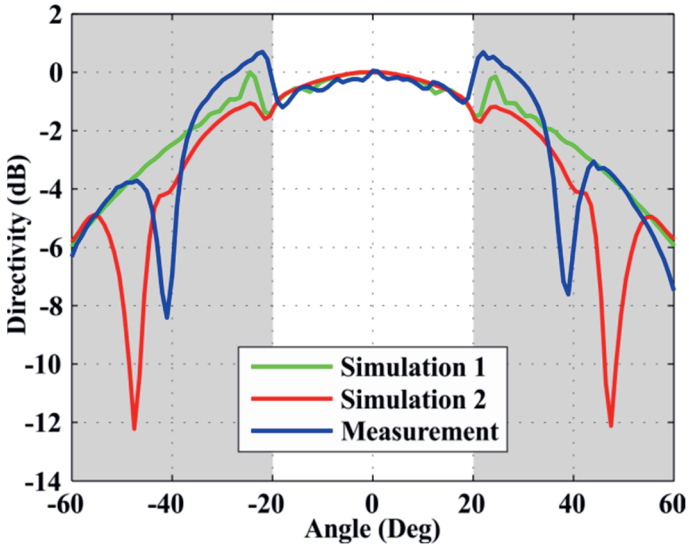


Figure 2.23. Directivity pattern of elements from measurement results and PZFlex simulations for 2 cases: simulation 1 involves water loading of the transducer element, and simulation 2 includes an additional 25 µm thick polyester layer between the transducer elements and the water.

2.5.2.5 Dynamic Range

The dynamic range is defined as the difference between the highest and the lowest detectable pressures. To measure the overall dynamic range, we transmitted a wave with a known pressure with a well-defined external transducer and used the matrix transducer in receive mode. For this purpose, a single-element transducer with 1 mm aperture size (PA865, Precision Acoustics, Dorchester, UK) was placed in the water-tank at 150 mm from the matrix transducer. Using excitation voltages from 2 mV to 150 V, we first performed hydrophone measurements of the amplitude of the transmitted pressure wave at the intended location of the matrix transducer. Moreover, we measured the linearity and the width of the transmitted

beam. Then we replaced the hydrophone with the matrix transducer and recorded the received voltages in the Verasonics, both with LNA on and LNA off. With this described excitation approach we could increase the pressure from 1.8 Pa to 136 kPa at the surface of the matrix transducer. Since the noise floor and the saturation levels of the Verasonics varies at different TGC gain settings, we repeated the measurements for TGC settings 500, 700, and 900. The received signal amplitudes at different TGC gain settings were then translated back to the output voltage of the ASIC using the plot in Figure 2.16. The relation between the pressure at the matrix elements and the recorded voltage at the output of the ASIC is plotted in Figure 2.24.

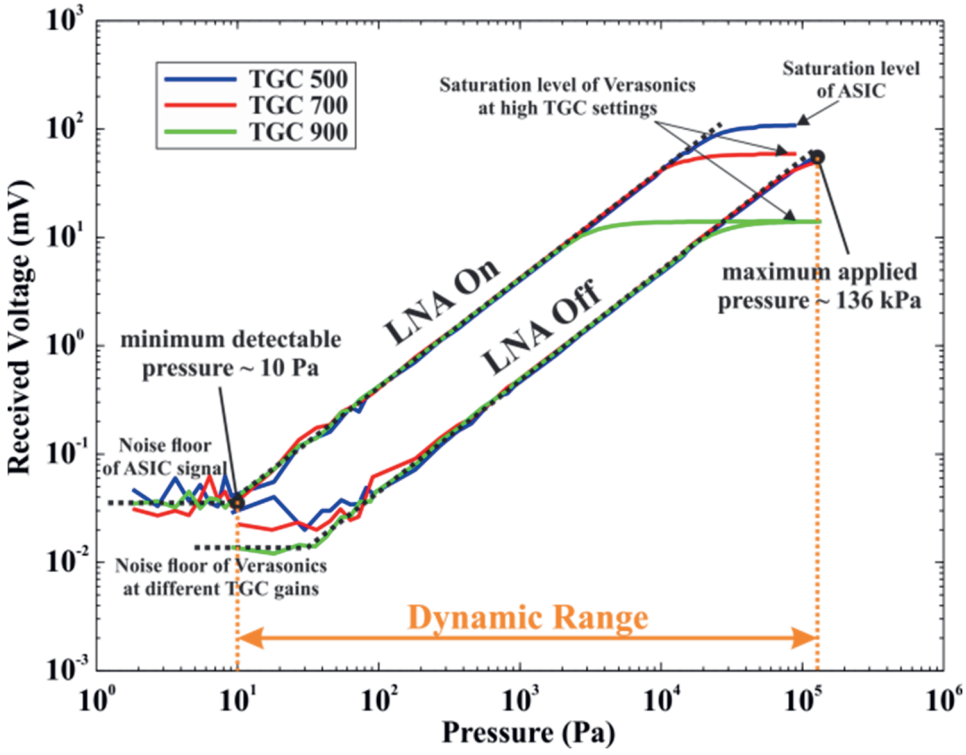


Figure 2.24. The relation between the pressure at the matrix elements and the recorded voltage at the output of the ASIC, for LNA on and LNA off. The difference between the lowest and the highest measureable pressure is the dynamic range of the matrix transducer.

The different noise levels of the Verasonics at different TGC gains are visible in the curves for LNA off. The noise level for LNA on, is higher than the Verasonics noise level, and is similar for all the three-gain setting. This is the ASIC noise level for LNA on. The minimum detectable pressure is approximately 10 Pa, which is limited by the noise floor level for LNA on. On the other hand, the maximum pressure is about 136 kPa, which is the saturation level of the signal of the ASIC for LNA off. In this case the maximum pressure is still in the linear regime

of the ASIC, but we stopped generating higher pressures to avoid damage due to high voltage on the transmitting transducer. Thus, the overall dynamic range is measured to be more than 83 dB. The difference between the two curves for LNA on and off shows the expected 20 dB gain effect of the LNA. Furthermore, an overall receive sensitivity of 0.5 μV/Pa for LNA off and 5 μV/Pa for LNA on is measured.

2.5.2.6 Imaging

We tested the single tile matrix array in an imaging experiment using the setup shown in Figure 2.25. We imaged four static needles in water by applying plane waves in transmission and column-by-column read-out as illustrated by the plane wave imaging scheme in Figure 2.5. Element-selection modes supported by the ASIC: (a) single-column selection; (b) full-aperture selection; (c) selection of arbitrary sets of elements; (d) pseudo-random element selection. Every transmit-receive acquisition took 100 μs, which yields a volume-rate of 250 Hz for this 40 column matrix array. The volume reconstruction involving 321 × 481 × 801 (X × Y × Z), isotropic voxels of 50 μm), was done using a conventional delay-and-sum algorithm implemented on a GPU using CUDA and MATLAB software. Figure 2.25 shows a 3D rendering of the needles in water, and 3 orthogonal mean intensity projections of the reconstructed volume in water.

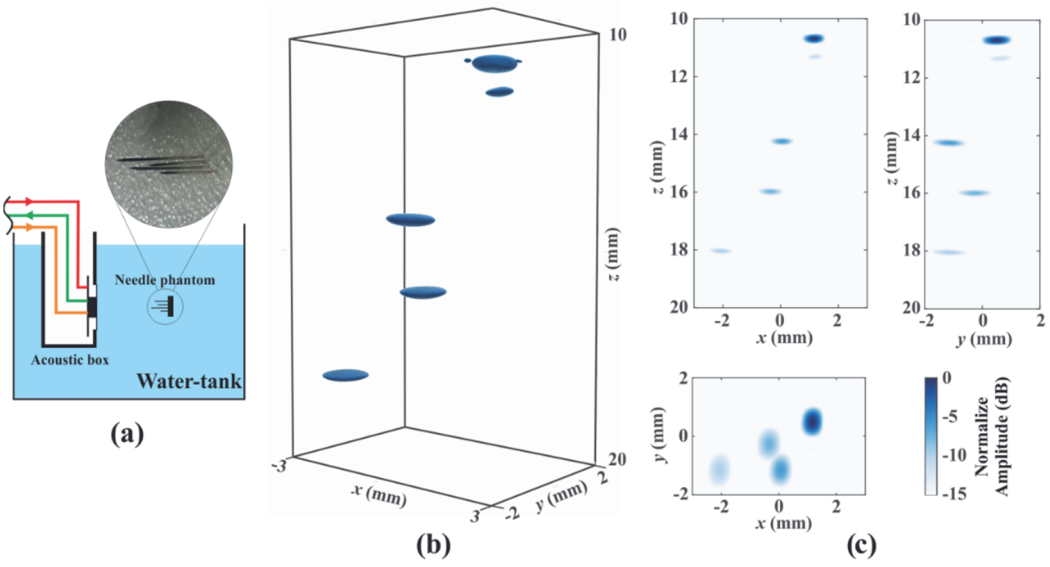


Figure 2.25. Volume reconstruction of needles in water: (a) the imaging phantom composed of four needles in space, (b) 3D rendering, (c) maximum projections on three orthogonal planes.

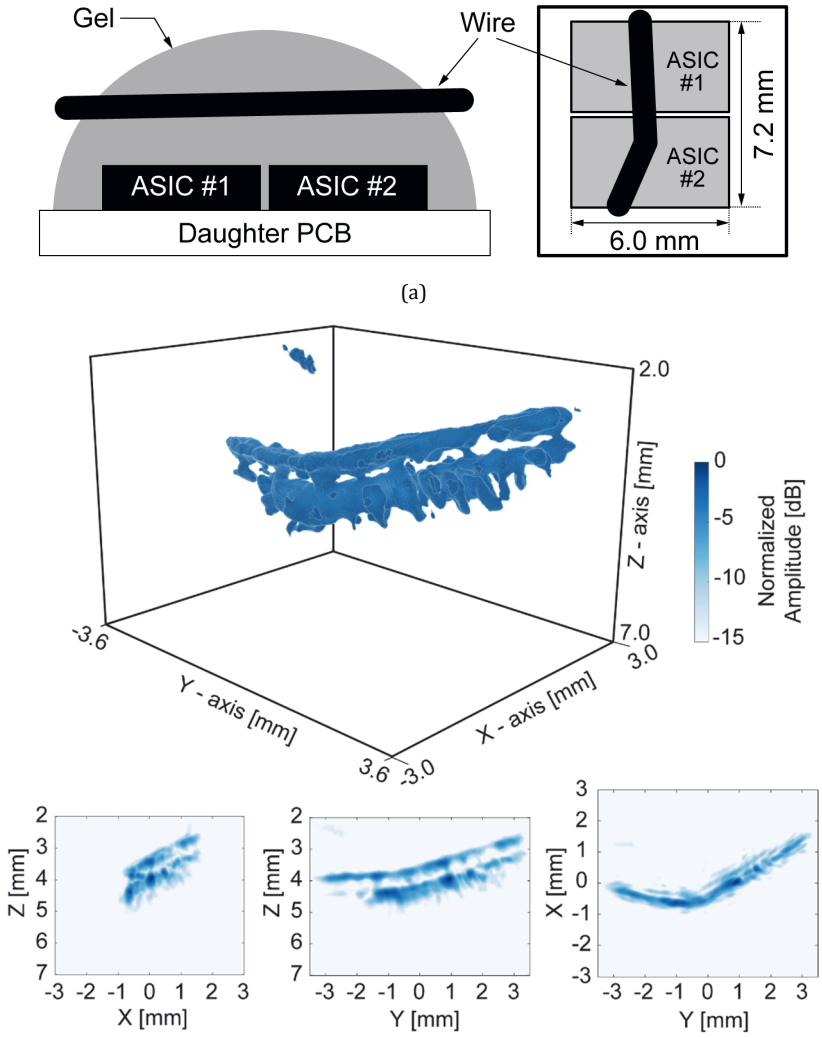


Figure 2.26. (a) Setup with two ASIC tiled side-by-side for a 3D imaging experiment; (b) reconstructed volumetric images along with maximum projections.

Figure 2.26 shows an imaging experiment with a prototype consisting of 2×1 tiled ASICs. It demonstrates the 3D-imaging capability with a total of 1920 individual elements. A bended metal wire phantom was placed above the prototype through acoustically transparent coupling gel, as illustrated in Figure 2.26a. In this imaging experiment, we transmitted plane waves by enabling all elements for TX (cf. Figure 2.5b), and received the echo signals column by column, by selecting one element per row for RX (cf. Figure 2.5a), and shifting this pattern

in 40 successive pulse-echo cycles (cf. Figure 2.6d). Figure 2.26b shows the volumetric image reconstructed from the recorded RX data set by means of standard delay-and-sum beamforming, envelope detection, log compression and 3D rendering using a 15 dB dynamic range. The wire is clearly visible, including strong acoustic reverberations behind the wire, attributed to the high acoustic-impedance mismatch between the metal and the gel. This imaging experiment successfully demonstrates the 3D-imaging capability of the prototype. Note that the imaging quality of a complete 2 × 10 tiled array will be significantly better.

TABLE 2-2. PERFORMANCE SUMMARY AND COMPARISON

	[10]	[14]	[17]	**This work**
Transducer	CMUT	CMUT	PZT	**PZT**
Array size	32 × 32	16 × 16	32 × 32	**24 × 40**
Center freq.	5 MHz	5 MHz	5 MHz	**7.5 MHz**
Element Pitch	250 µm	250 µm	150 µm	**150 µm**
# of TX el.	960	256	64	**960**
# of RX el.	64	256	864	**960**
TX architecture	Element-level pulsers	Column/row parallel with element-level pulsers	Hard-wired TX sub-array	**Row-parallel with element-level HV SW**
RX architecture	Diagonal elements only	Column/row parallel with element-level LNAs	Sub-array beam-forming	**Row-parallel with row-level LNAs**
Pre-programmable element patterns	-	2	-	**9 (shift pattern)**
RX channel bandwidth	20 MHz	10.8 MHz	6.0 MHz	**20 MHz**
RX power/ch	4.5 mW	1.4 mW	0.27 mW	**2 mW**
RX input referred noise (mPa/√Hz)	-	2.3	1.0	**4.2**
TX amplitude	60 V	30 V	50 V	**30 V**
Process	0.25 µm HV	0.18 µm HV	0.18 µm LV	**0.18 µm HV**
ASIC size	9.2 × 9.2 mm²	6 × 5.5 mm²	6.1 × 6.1 mm²	**3.6 × 6.8 mm²**

2.6 Conclusion

A reconfigurable ultrasound ASIC intended for 3-D volumetric imaging of the carotid artery has been presented in this chapter. The ASIC, realized in a high-voltage 0.18 µm BCDMOS process, interfaces with an array of 24 × 40 transducer elements directly integrated on top of the ASIC, and can be tiled to realize larger apertures.

Table 2-2summarizes the ASIC's features and compares them with prior ASICs for 3D ultrasound imaging. This work stands out in its reconfigurability and integration density,

with an element-matched layout with a 150 μm pitch. By using the proposed row-level architecture, the number of channels required to connect the 960 transducer elements to an imaging system is substantially reduced. Although the row-level architecture is less flexible in terms of possible element connections than the row-column-parallel architecture described in [14], it enables seamless tiling of multiple ASICs to realize large-aperture arrays. Every element is associated with a compact and power-efficient bootstrapped high-voltage TX switch and an RX switch. Compared to the pulsers used in [10], [14], [15], this allows for a broader range of transmit waveforms. The use of row-level LNAs rather than element-level LNAs, as in [14], [15], allows for more compact element-level circuits, at the expense of some attenuation associated with the loading presented by the RX bus. Element-level logic with programmable memory allows the selection of elements used for transmit and receive to be quickly reconfigured, allowing various focal depths and imaging modes to be implemented. Compared to the design described in [14], which supports rapid switching between two pre-programmed patterns, more patterns can be pre-programmed, and more flexible pattern loading and shifting modes are supported, as well a pseudo-random selection mode. Acoustic measurements demonstrate the 3D-imaging capability of the implemented prototype.

References

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Chapter 3

A 64-Channel Transmitter with ±30V Bipolar High-Voltage Pulsers for Ultrasound Imaging

This chapter is based on the publication "A 64-Channel Transmit Beamformer with ±30V Bipolar High-Voltage Pulsers for Catheter-Based Ultrasound Probes," in IEEE Journal of Solid-State Circuits, vol. 55, no. 7, pp. 1796-1806, July 2020.

3.1 Introduction

Ultrasound imaging is a safe, cost-effective, and widely-used imaging modality for the diagnosis and treatment of cardiovascular conditions. Miniaturized ultrasound devices mounted at the tip of a catheter or endoscope are becoming increasingly important as they can provide better image quality than external hand-held probes, for instance, to guide minimally-invasive cardiac interventions [1]. A prime example is intra-cardiac echocardiography (ICE) probes, which generate ultrasound images from inside the heart using a transducer array mounted at the tip of a catheter [2]. The image construction relies on the transmission of acoustic waves and post-processing of the reflected echo signals. The acoustic waves are generated by exciting the elements of the transducer array with voltage pulses. Typically, these pulses are timed such that an acoustic beam is formed that is focused and steered at a particular angle. Different pulse timing in successive pulse-echo cycles allows the beam to scan the region of interest to form an image. Since the acoustic signal will be significantly attenuated as it propagates through tissue, high-voltage (HV) pulses (with amplitudes of tens of volts) are required to generate enough pressure so that the overall signal-to-noise ratio is sufficiently high at the largest imaging depth [3].

In most commercial ICE catheters, the elements in the transducer array are connected to transmit (TX) and receive (RX) circuitry in an imaging system through long micro-coax cables. Given the signal attenuation caused by such cables and difficulties of the cable assembly,

application-specific integrated circuits (ASICs) have been integrated closely to the transducer array to reduce the number of cables and increase the signal-to-noise ratio by locally amplifying the echo signals [4]–[9].

An important challenge in the design of such in-probe ASICs is that the required HV TX circuitry cannot be implemented in standard CMOS technologies. This applies to the HV pulsers as well as to the transmit/receive (T/R) switches needed to protect the low-voltage (LV) RX circuitry during pulse transmission. Therefore, HV BCD technologies are usually adopted in which HV MOS transistors are available [4], [5], [8]. Such transistors, however, tend to occupy a large die area while the available area is limited in catheter-based devices. This calls for a compact pulser and T/R SW design.

Unipolar pulsers have been applied (which can only generate positive HV pulses), as they can be implemented using a small number of HV transistors [10], [11]. However, this comes with several disadvantages. In contrast with the bipolar pulses commonly generated by conventional imaging systems, unipolar pulses contain more low-frequency out-of-band energy, and thus lead to lower SNR for the same peak-to-peak amplitude [12]. Moreover, many image-enhancing techniques, such as pulse inversion and coded excitation, are easier to implement using bipolar pulses [13]. Therefore, it is worthwhile to design an on-chip bipolar pulser although the architecture is more complicated.

An added benefit of using bipolar pulsing is that it can reduce the dynamic power consumption of the pulser by at best a factor of 2 compared to a unipolar pulser with the same peak-to-peak output voltage, provided a return-to-zero (RZ) pulser is used[14]. This is an important advantage, since the overall power consumption of the ASIC should be minimized to avoid tissue over-heating.

In this chapter, we present a front-end ASIC for a 64-element transducer array that includes an on-chip transmit beamformer and programmable bipolar pulsers. The chapter extends on our previous work [15], [16], in which the bipolar pulser has been described. Here, we present a complete ASIC intended for a CMUT-based 2D ICE probe. With a width of less than 2 mm, the ASIC is suitable for catheter integration and directly connects to the transducer elements in a pitch-matched fashion through a PCB interposer. The ASIC only needs two low-voltage differential signalling (LVDS) clock and data lines to program the on-chip transmit beamformer. Electrical and acoustical measurement results are presented that successfully show the functionality of the bipolar pulser and the complete TX beamformer.

This chapter is organized as follows. Section 3.2 describes the system architecture. Section 3.3 discusses the design of the bipolar pulser, while Section 3.4 presents details of the circuit implementation. Sections 3.5 and 3.6 present the experimental results and conclusions.

3.2 System Architecture

Figure 3.1 shows a block diagram of the proposed system. It consists of a 64-element CMUT transducer array, a front-end ASIC and the imaging system. The elements of the transducer array are directly connected to channels of the ASIC at the tip of the catheter, while a bundle of micro-coax cables (~ 2-m long) is used to connect the ASIC with the imaging system.

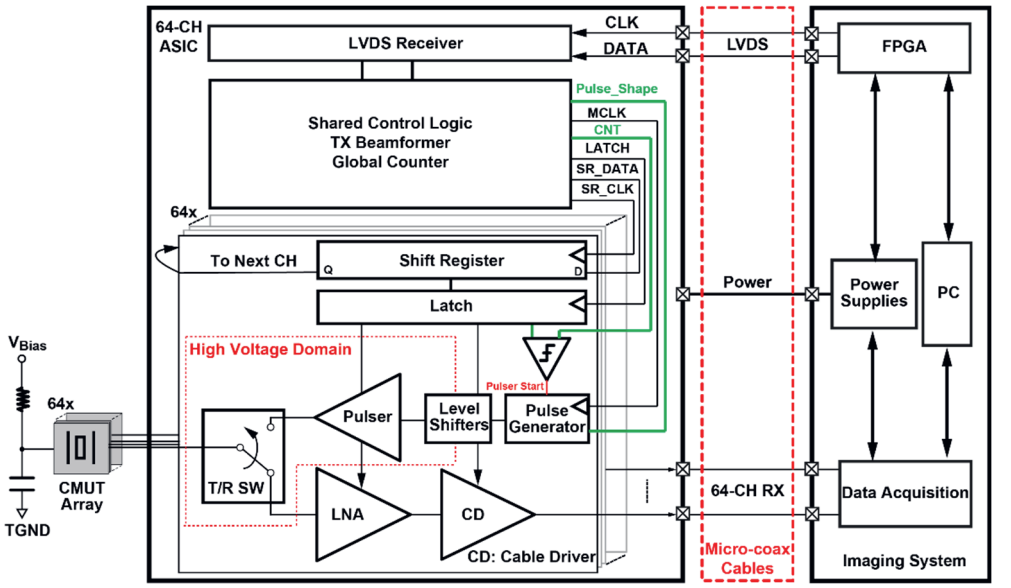


Figure 3.1. System Architecture

We employ a CMUT transducer array with a center frequency of 7.5 MHz, targeting ICE applications [9], [11]. All the CMUT elements are DC-biased at Vbias and AC-coupled to the transducer ground (TGND) through a shared RC network. To interface with the CMUT elements, each channel of the ASIC contains a T/R switch, a HV TX pulser with associated level shifters and pulse generator, a low-noise amplifier (LNA), a cable driver (CD), and a latched shift register (SR) for the configuration.

Clock and data are provided to the ASIC by an FPGA through LVDS signals, which are first converted to 1.8 V standard logic levels through an on-chip LVDS receiver. Then, shared control logic will generate a clock (SR_CLK) and data (SR_DATA) for the element-level SRs, a latch signal (LATCH) for the element-level latches, and a master clock (MCLK) and counter (CNT) for the timing control of the pulse generators. The SR of each channel provides the configuration data for the RX amplifiers and HV pulsers, as well as a counter value, which is compared to CNT to define the start time of the pulse. The SRs are daisy-chained to allow the element-level configuration data to be loaded sequentially from the shared control logic.

According to the loaded data in the SR, the pulse generator will generate low-voltage (LV) signals to control the HV pulser through the level shifters with a proper timing.

When the CMUT transducer element is excited by the HV pulses, ultrasonic waves are emitted into the medium. The resulting echo signals are amplified by the low-noise amplifiers (LNAs), which are connected to the transducer elements via the T/R switches after pulsing, and then transferred to the imaging system through micro-coax cables with the help of cable drivers (CD). The details of the LNA and CD are presented in [17]. The imaging system will record the echo signals and process them for image reconstruction.

3.3 Bipolar Pulser Design

Figure 3.2 shows the simplified block diagram of a single ultrasound transceiver channel of the ASIC. To generate RZ bipolar pulses, the pulser consists of a pull-up switch that drives the CMUT transducer to a positive HV supply (HV_VDD), a pull-down switch that drives it to a negative HV supply (HV_VSS), and a RZ switch that pulls the transducer back to ground. The impedance of the CMUT element used in this work can be modelled as 18 pF//17 kΩ.

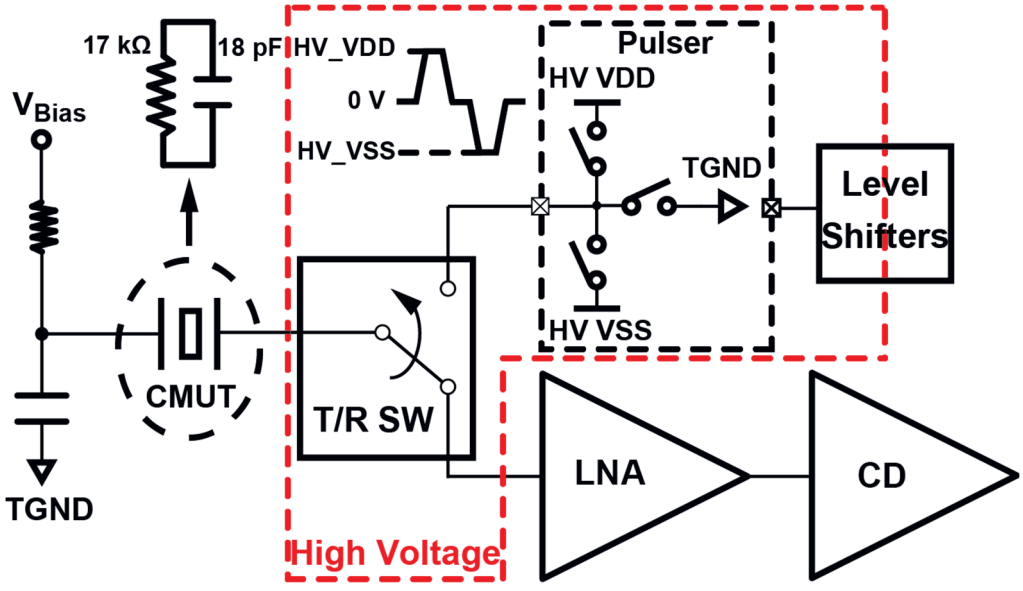


Figure 3.2. Simplified block diagram of a single transceiver channel of the ASIC.

3.3.1 Switch Configurations with Bidirectional Isolation

The RZ switch needs to provide bidirectional HV isolation, in the sense that when it is off, it should be able to handle both positive and negative voltage drop. Similarly, the T/R switch, which connects the transducer to the LNA during echo reception, needs to provide bidirectional HV isolation during pulsing. Two technology-related limitations of the HV MOS transistors in BCD technologies, the body diode and the limited gate-oxide breakdown voltage, increase the implementation complexity of the T/R switch and the RZ switch. The presence of the body diode implies that two back-to-back connected HV transistors are needed to provide bidirectional isolation. The relatively low gate-oxide breakdown voltage requires a more complicated gate-driver design compared to HV technologies with thick gate oxide.

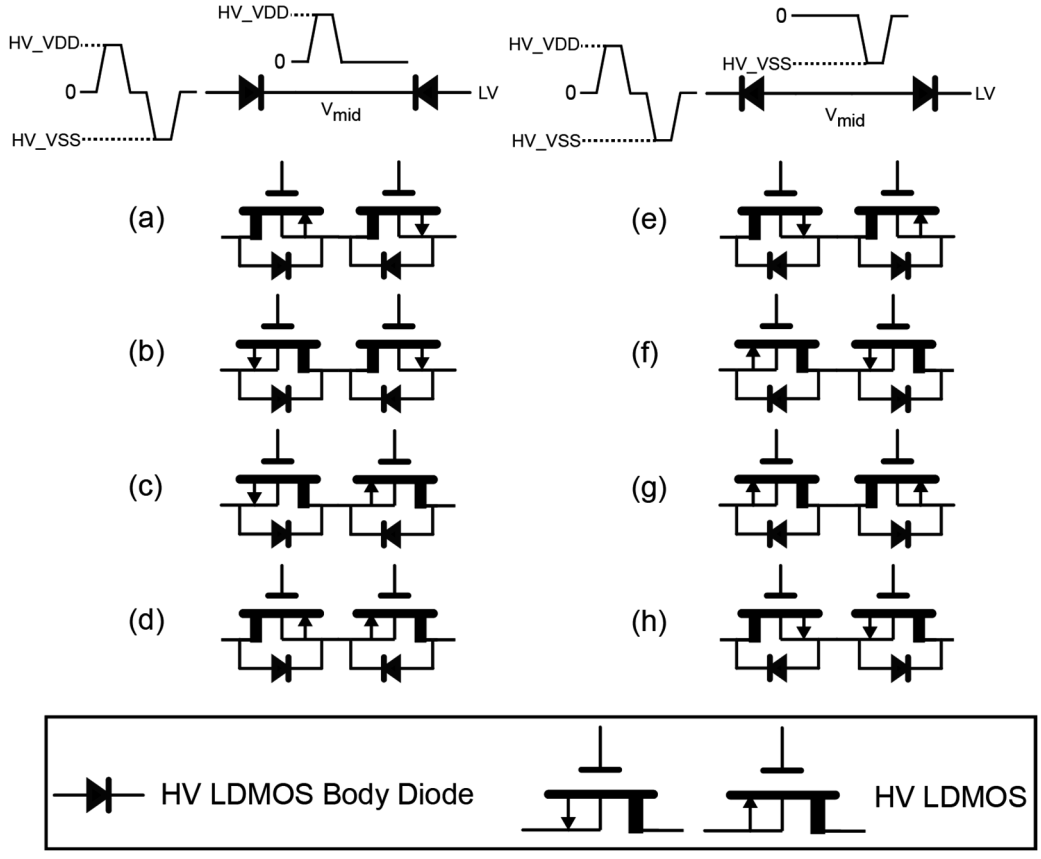


Figure 3.3. Overview of HV MOS configurations that can provide back-to-back isolation.

Figure 3.3 shows the eight possible back-to-back configurations of HV NMOS and PMOS transistors. The body-diode orientation in configurations (a)-(d) is such that the middle node

between the transistors (Vmid) swings up with the positive HV pulse, while in configurations (e)-(h) it swings down with the negative HV pulse. In all configurations, at least one of the sources of the transistors swings up and/or down with the HV pulse, implying that a HV gate driver is needed that keeps the gate-source voltage below the gate-oxide breakdown limit (5.5V in our technology). To prevent this HV floating-gate driver from having to operate at both positive and negative high voltages, configurations in which the source of the left-hand transistor connects to the transducer should be avoided. Driving the source of the right-hand transistor is easier if it connects to the low-voltage circuitry rather than to Vmid. This leaves configurations (a) and (e) as the preferred choice, both of which are applied in parallel in our implementation.

3.3.2 Floating-Gate Driver

In previous HV switch designs [5], [8], [18], bootstrapped gate drivers have been employed. However, they cannot be applied in an RZ switch, because they only allow the switch to be turned on when it is at ground level, while the RZ switch needs to be turned on when the pulser output is at HV_VDD or HV_VSS. Therefore, we propose a compact and energy-efficient floating-gate driver that utilizes parasitic capacitance to control the gate-source voltage and requires only one additional small HV MOS transistor.

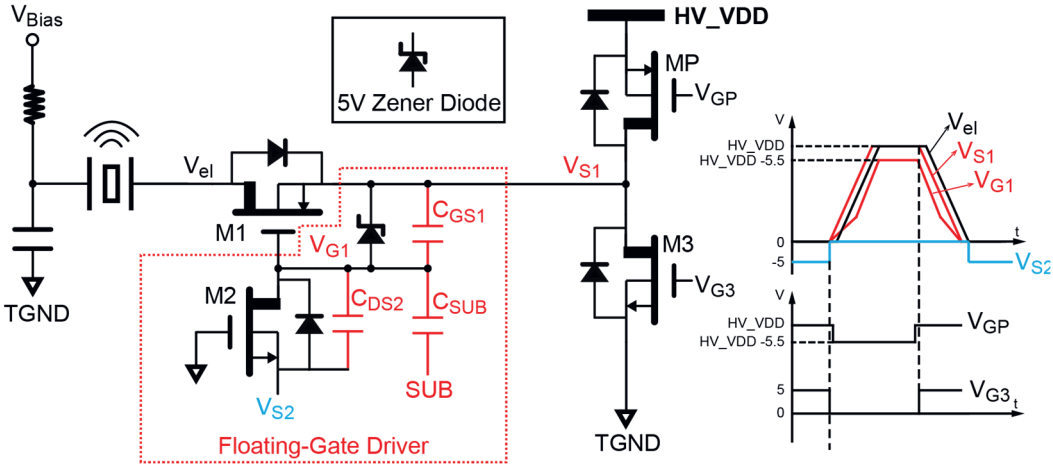


Figure 3.4. Circuit diagram of a high-side pulser employing the single-transistor HV floating-gate driver circuit.

This circuit is shown in Figure 3.4, in the context of a unipolar (high-side) pulser. HV transistors MP and M1 are used to pull the transducer to HV_VDD, while M1 and M3 together form the switch configuration of Figure 3.3a to provide the return-to-zero switching. The gate of MP is driven relative to HV_VDD using a conventional level-shifter circuit. The gate of M1 is driven by our new gate-drive approach using transistor M2. Initially, to short the

transducer to ground, M3 and M1 are turned on. M1 is turned on through M2 by connecting M2's source to -5 V and its gate to ground, so that the gate of M1 is pulled to -5 V. Before the HV pulsing starts, the source of M2 is switched to ground, so that the gate of M1 is discharged to ground through the body diode of M2. After this, M2 is off and the gate of M1 floats. When MP is turned on and M3 is turned off, the voltage step on V_{S1} will also create a step on the gate of M1 because of the capacitive divider formed by C_{GS1} and C_{DS2} + C_{SUB}, where C_{SUB} is the capacitance from the gate of M1 to the substrate. By properly sizing M2 to make C_{DS2} + C_{SUB} larger than C_{GS1}, V_{GS1} will increase, turning on M1 and thus allowing the transducer to be charged to HV_VDD. A Zener diode prevents V_{GS1} from exceeding the breakdown voltage. At the beginning of the RZ phase, MP is turned off and M3 is turned on, while M1 remains on. This discharges the transducer until V_{el} reaches the threshold voltage of M1 of 0.7 V (~85 times smaller than the pulse peak-to-peak amplitude), thus realizing an almost complete RZ operation. Finally, the gate of M1 is pulled to -5 V through M1.

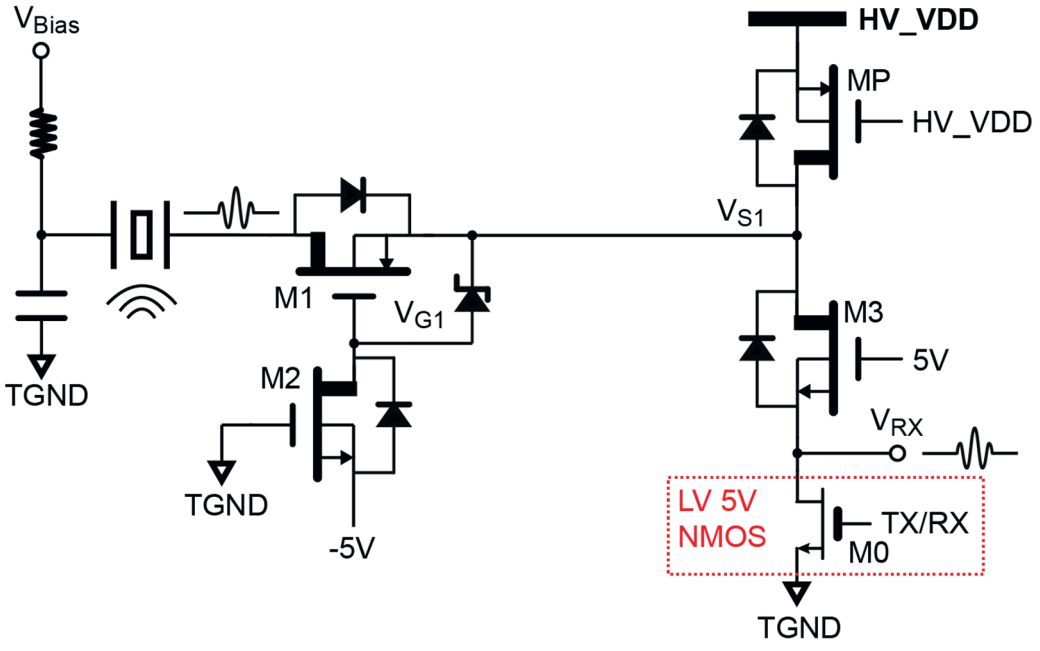


Figure 3.5. Circuit diagram of the high-side pulser with embedded T/R switch.

3.3.3 Embedded T/R Switch

The circuit of Figure 3.4 can be extended with one additional low-voltage transistor M0 to allow it to act also as a T/R switch, as shown in Figure 3.5. This transistor is placed in series with the source of M3 and is turned on during the TX phase, allowing the circuit to operate as before and preventing any feedthrough of the HV pulse from reaching the RX circuitry. Although M0 will increase the total series resistance for the RZ phase, it can be sized to have a low on-resistance compared to that of M1 and M3 without significantly affecting the total die area since it is an LV MOS transistor. During the TX phase, when the HV pulsing finishes and VS1 and VG1 are at ground level, M1, M3 and M0 are turned on to short the transducer to TGND. During the RX phase, M0 is turned off so that the received echo signal can pass through M1 and M3 to the LV receive circuitry. Since the parasitic capacitance of the LV transistor M0 is relatively small, the transient introduced by the switching of M0 is negligible. Turning on M1 through M2 requires the source of M2 to be -5 V, which is realized using a simple low-voltage charge-pump-based level shifter (see Section 3.3.2). Thus, only 4 HV transistors are used to implement HV pull-up, return-to-zero, and T/R switch functionality.

3.3.4 Complete Bipolar Pulser

To realize a complete bipolar pulser, the high-side circuit of Figure 3.5 is combined with a complementary low-side version. Figure 3.6 shows the resulting circuit, including the various level-shifters and the associated timing diagram. During the TX phase, M2 and M5 are turned off to float the gate of M1 and M4. Pulling up the pulser output from ground to HV_VDD and pulling down the output from HV_VDD to ground (RZ phase) are done by turning on MP and M3, respectively, as discussed in Section 3.3.3 The same concept is applied in the complementary low-side pulser for the transition from ground to HV_VSS and HV_VSS to ground, by turning on MN and M6, respectively. After the TX phase, the two sets of RZ switches (M1, M3) and (M4, M6) are turned on in parallel to serve as a T/R switch, reducing the on-resistance (and the associated noise) by 2x, and saving substantial area compared to a separate T/R switch.

Depending on configuration bits stored in the element-level SR, the pulse generator can provide the following operating modes: A) bipolar RZ pulsing as shown in the timing diagram of Figure 3.6; B) bipolar non-RZ pulsing (by setting the RZ time to 0); C) unipolar pulsing (by setting the pull-up time or the pull-down time to 0). Moreover, the width of the pulses can be defined (in terms of cycles of the 200 MHz clock) to enable pulse-width programming, allowing the pulser to be used at different frequencies.

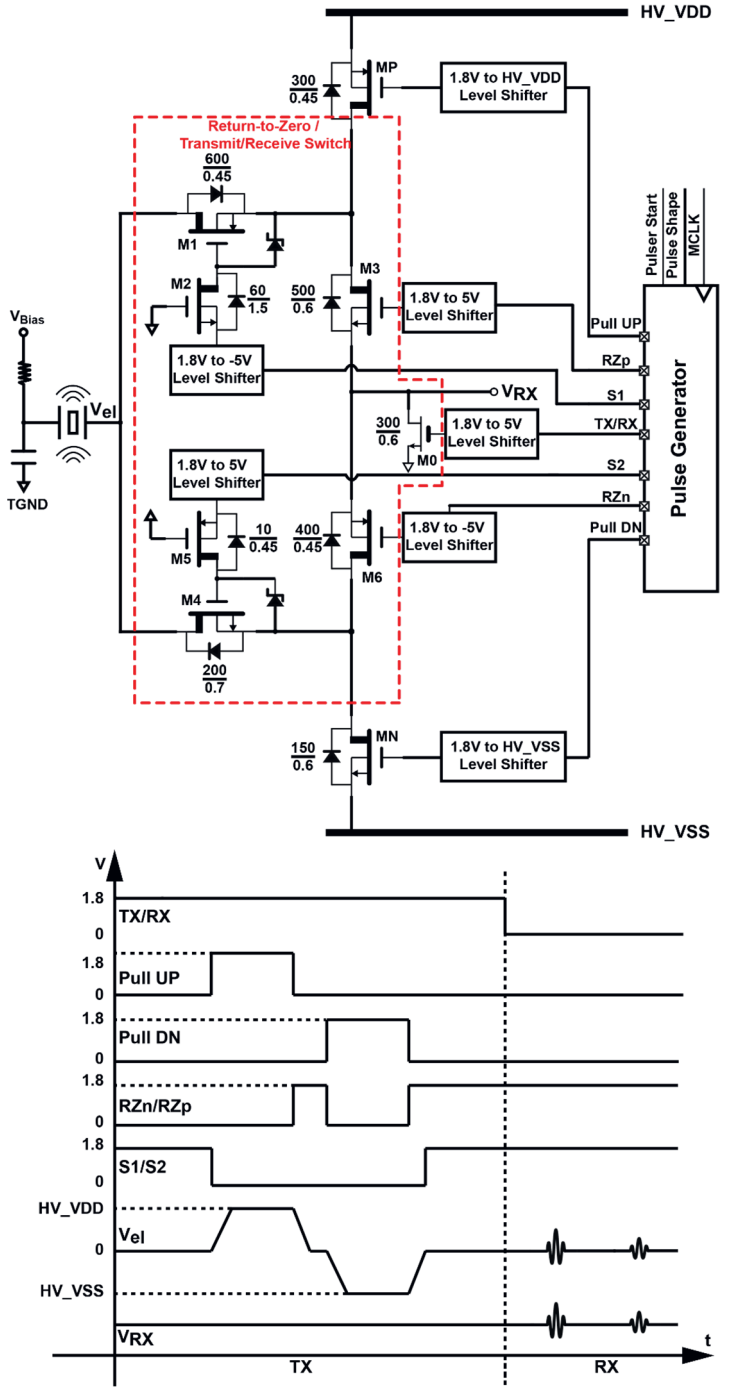


Figure 3.6. Circuit diagram of the complete pulser, with associated timing diagram.

3.4 Circuit Implementation Details

3.4.1 Supply Domains

Figure 3.7 shows the power supplies used in the proposed system. The power supply for the digital blocks (DVDD) is locally decoupled to the digital ground (DGND) on the PCB, while HV_VDD, HV_VSS and the 5 V supply for the level shifters (VDD5V) are locally decoupled to TGND. These supplies and grounds are connected to the system side through cables. To prevent transients associated with the operation of the digital circuits from affecting the analog circuitry, DGND and TGND are joint together on the system side. A limited set of decoupling capacitors, sized to be able to fit inside a catheter, are placed as close to the ASIC as possible to provide transient supply currents. Nevertheless, there is still certain inductance between these decoupling capacitors and the on-chip circuitry, which will give rise to di/dt transients on the supplies. The level shifters need to be designed to be immune to these transients.

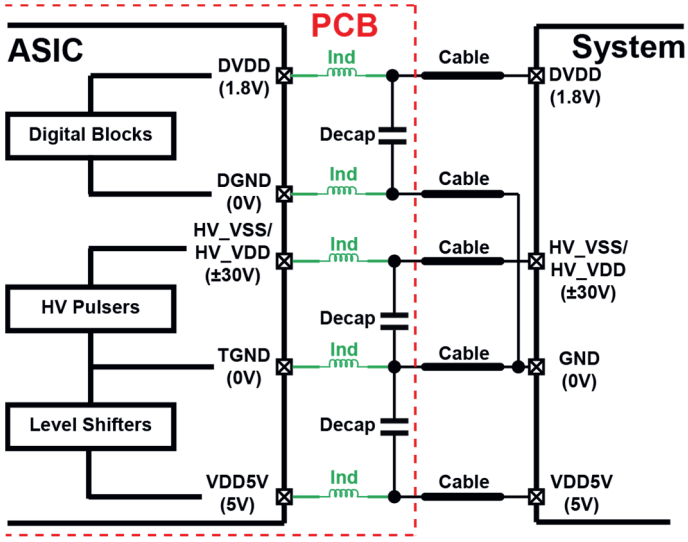


Figure 3.7. Overview of the power supplies in the proposed system.

3.4.2 Level Shifters

The level shifters shift the 1.8 V logic-level signals to 5 V signals relative to ground, HV_VDD and HV_VSS to drive the gates of the HV MOS transistors (see Figure 3.6). To reliably level-shift logic-level signals in the DGND-DVDD domain to the TGND-VDD5V domain, in the presence of potential voltage transients between DGND and TGND, we propose the current-

mode level-shifter architecture shown in Figure 3.8a. When the logic input is high, a current provided by M1 is copied to the 5 V domain by current mirror M2, M3, causing a high level on diode-connected transistor M4, which is buffered to a proper 5 V level to drive HV MOS MN. When the logic input is low, the absence of current in M4 leads to a low level that turns off MN.

To turn on HV PMOS M6 in Figure 3.6, a negative 5 V level is required. Instead of using an external –5 V supply, a charge-pump based architecture is used. Figure 3.8b shows the circuit diagram. During the start-up, V_G is discharged to TGND through diode leakage. Then, the bootstrap capacitor is pre-charged to VDD5V through a 1.8 V to 5 V level shifter. Therefore, V_G will be pulled down to –5 V when the levels shifter output is 0 V in the ideal case. The bootstrap capacitor C_B is sized to ~5.4 pF so that MP gets enough over-drive voltage even though some charge will be lost due to the gate capacitance at node V_G.

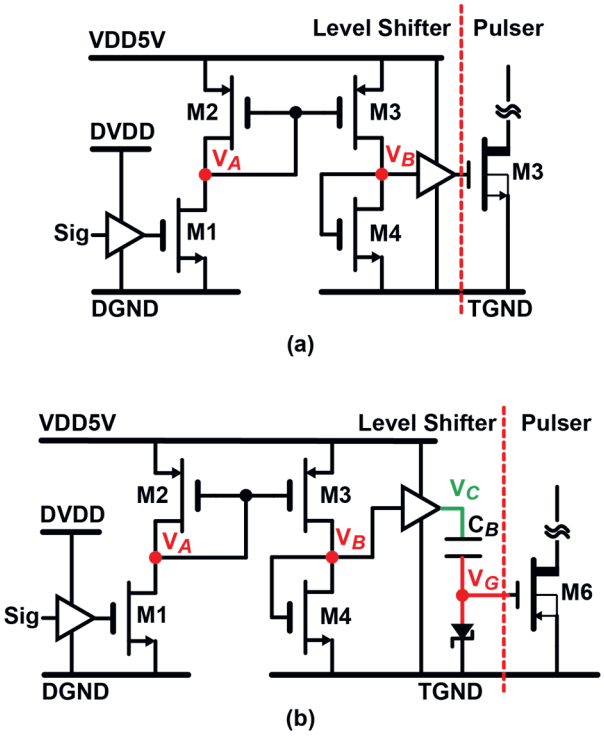


Figure 3.8. (a) 1.8 V to 5 V level shifter; (b) 1.8 V to –5 V level shifter.

Because HV_VDD and HV_VSS are also suffering from di/dt noise, the 1.8 V to HV_VDD and HV_VSS level shifters also apply a current-mode architecture, as shown in Figure 3.9. The V_{GS} of MP and MN in the pulser is determined by the IR drop on resistors R1 and R2, while the current mainly depends on the over-drive voltage and the transistor size of M1 and M2. By applying the architecture shown in Figure 3.8a for the 1.8 V to 5 V level shifter, an over-drive

voltage that is insensitive to the di/dt noise of HV_VDD/HV_VSS is obtained. Thus, MP and MN of the pulser can be turned on or off safely. Monte Carlo simulations indicate that the expected channel-to-channel mismatch introduced by the level shifters is less than 1% of the cycle time of the 7-MHz pulse, which has a negligible impact on the beamforming.

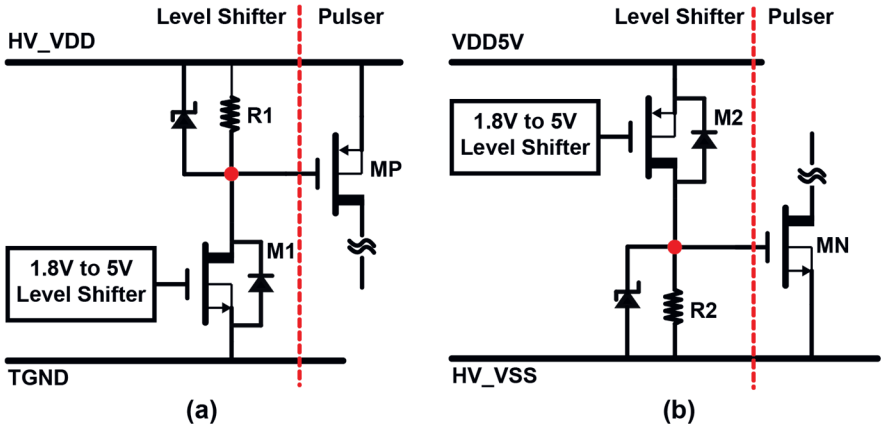


Figure 3.9. (a) 1.8 V to HV_VDD level shifter; (b) 1.8 V to HV_VSS level shifter

3.4.3 TX Beamforming Logic

For TX beamforming, the pulser in each channel should start generating a HV pulse at a well-defined time. This is done by comparing the start time pre-programmed in each channel with a global counter output (CNT in Figure 3.1), clocked at 200 MHz (MCLK). Figure 3.10 illustrates the block diagram and associated timing diagram of the TX beamformer logic. At the start of the RX period, configuration data (SR_DATA) is loaded sequentially into the daisy-chained shift registers of the shared logic and the 64 channels. The data for controlling the pulse shape and the pulse start time are loaded first and latched by LATCH_TX. These data will be used in the TX period and updated in the next RX period. During the remaining part of the RX period, the SR clock, SR data and the global clock are quiet unless RX control data (like the gain setting of the LNAs) needs to be updated. This leads to low average power consumption and minimizes the interference with the sensitive RX circuitry. At the start of the TX period, the global counter starts to run at the frequency of MCLK of 200 MHz. The counter output is distributed across the 64 channels and is compared to the start time which is pre-stored in the latch of each channel. If the counter output matches the stored start time and the channel is enabled, a pulser start signal will be generated to start the HV pulsing with a pre-defined pulse shape determined by the pulse-shape configuration data stored in the shared logic. Approximately 10 μs is needed to load all the configuration data with a SR_CLK of 100 MHz. This leads to a maximum pulse-repetition frequency (PRF) of 100 kHz, which is sufficiently high in this application.

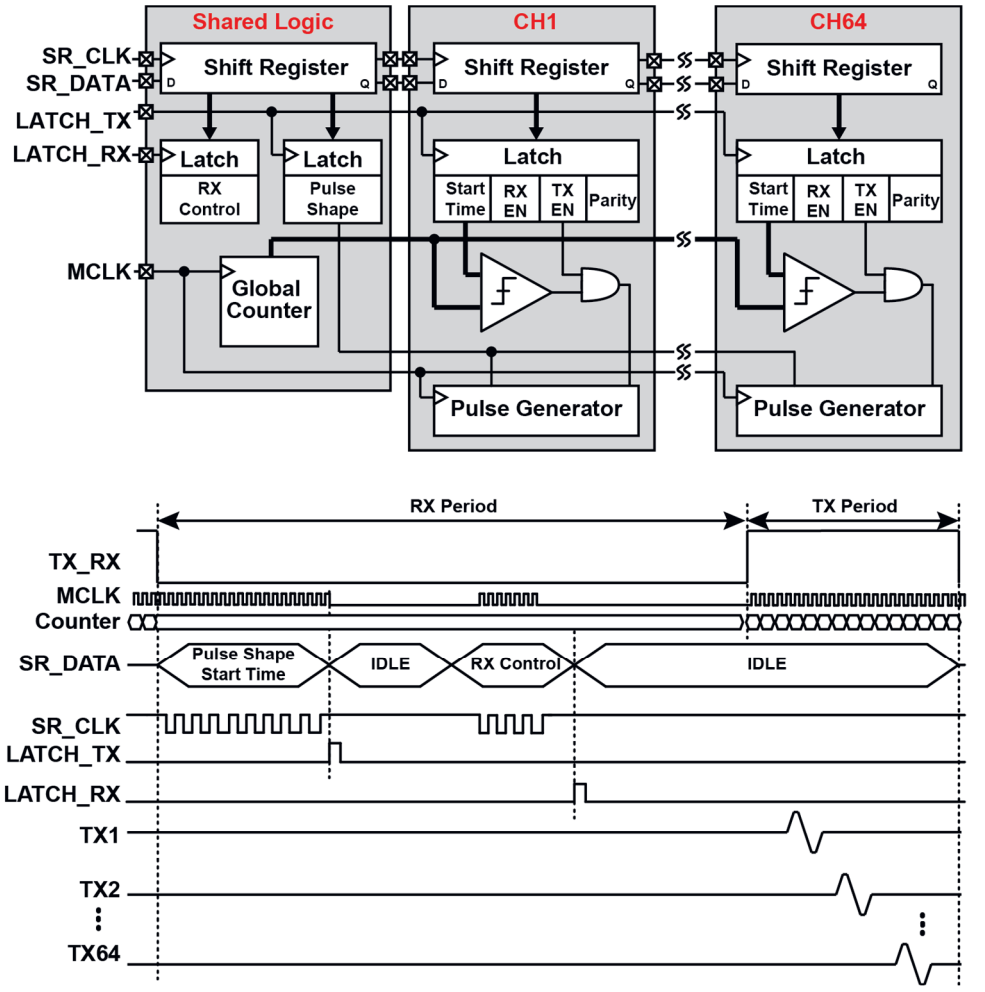


Figure 3.10. Block diagram and timing diagram of the TX beamformer logic.

3.4.4 Shared Digital Logic

Figure 3.10 shows that a total of 5 signals are needed for the TX beamformer, which are SR_CLK, SR_DATA, LATCH_TX, LATCH_RX and MCLK. To avoid an unnecessary increase in the cable-count, the SR_CLK, SR_DATA, LATCH_TX and LATCH_RX are encoded into the LVDS data line, while MCLK is derived from the LVDS clock line. Figure 3.11 illustrates the decoder and associated finite-state machine (FSM). The LVDS clock and data are first converted to single-ended signals by the LVDS receiver. The single-ended clock output serves as MCLK and as the clock of the FSM, while the singled-ended data output controls the state transitions of the FSM.

As shown in the state diagram in Figure 3.11, the bit sequence of “010” corresponds to the latch signal for the RX shift registers (LATCH_RX), while the bit sequence of “011” generates the LATCH_TX signal for the TX shift registers. The data loading of the shift register starts with a bit sequence of “100”. After that, the bits are loaded sequentially with the DATA bit ‘0’ and ‘1’ being encoded as “00” and “01” respectively. When the data loading finishes, the FSM will return to the IDLE state in which both clock and data lines remain quiet.

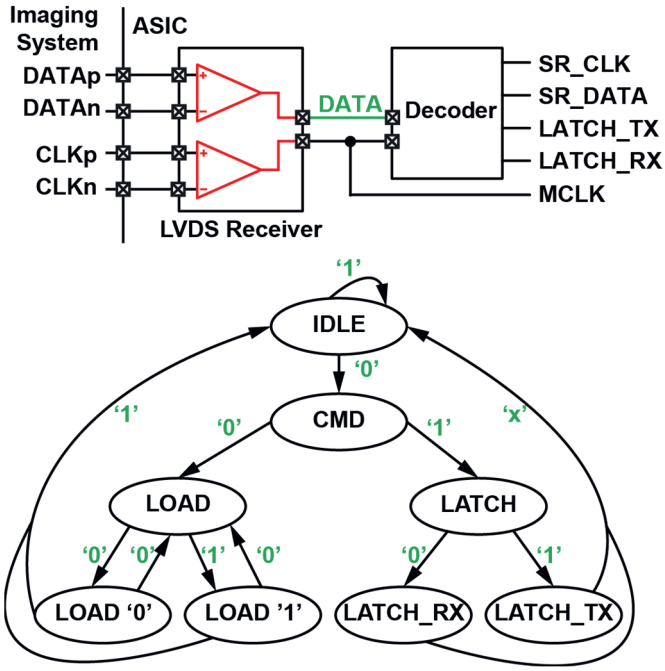


Figure 3.11. Shared control logic, with state diagram of the associated FSM.

3.5 Experimental Results

3.5.1 Experimental Prototype

The ASIC has been realized in TSMC 0.18-µm HV BCD technology with a total area of 1.8 x 16.5 mm^2, as shown in Figure 3.12. The 64 element-level circuit blocks (TX beamformer, HV pulsers, LNAs and cable drivers) are located at the center of the chip, occupying an area of 1.8 × 13.12 mm^2. They are arranged in two rows of 32 blocks with a pitch of 410 µm, allowing direct connections to the 64-element CMUT transducer. Figure 3.12(b) shows a zoom-in view of the element-level TX circuitry, which occupies an area of 410 × 408 µm^2. The power supplies and grounds are routed horizontally across the chip in the top metal. The power

consumption strongly depends on the ultrasound imaging mode and is dominated by the dynamic power consumed in driving the transducer capacitance.

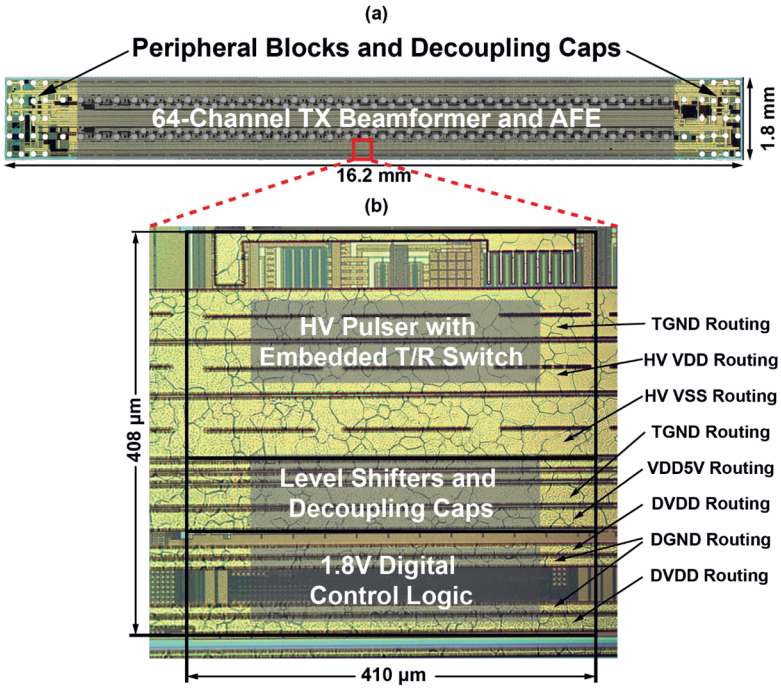


Figure 3.12. (a) Chip photograph of the 64-channel ASIC with (b) zoom-in of the element-level transmit circuits.

3.5.2 Electrical Measurement Results

To electrically characterize the prototype, an 18 pF capacitor is used as the load of the HV pulser, mimicking the transducer capacitance. To demonstrate the programmability of the proposed bipolar pulser, different configurations are applied to the pulser via the shift register. Figure 3.13 shows the measured output voltage of a single pulser channel with RZ times of 50 ns, 25 ns and 0 ns. The pulser can also be configured to generate pulses with different frequencies, allowing it to interface with different transducer elements for different applications. Figure 3.14 shows the measured output voltage for 4 MHz, 7 MHz and 9 MHz RZ and NRZ pulsing. Moreover, the proposed pulser can also be programmed to generate bursts of up to 63 pulses, which is suitable for Doppler imaging, as shown in Figure 3.15a. It is also possible to trade-off power consumption with penetration depth by configuring the pulser to generate unipolar negative or positive pulses, as shown in Figure 3.15b. Note that there is some slew-rate mismatch between the rising and falling edges of the pulses. The associated second-order harmonic content of the pulse can be an issue in harmonic imaging, but this is

not targeted in this work. If needed, slew-rate matching can be improved by optimizing the sizing of the high-voltage pull-up or pull-down transistors, or by trimming their overdrive voltages by means of adjustable level-shifters.

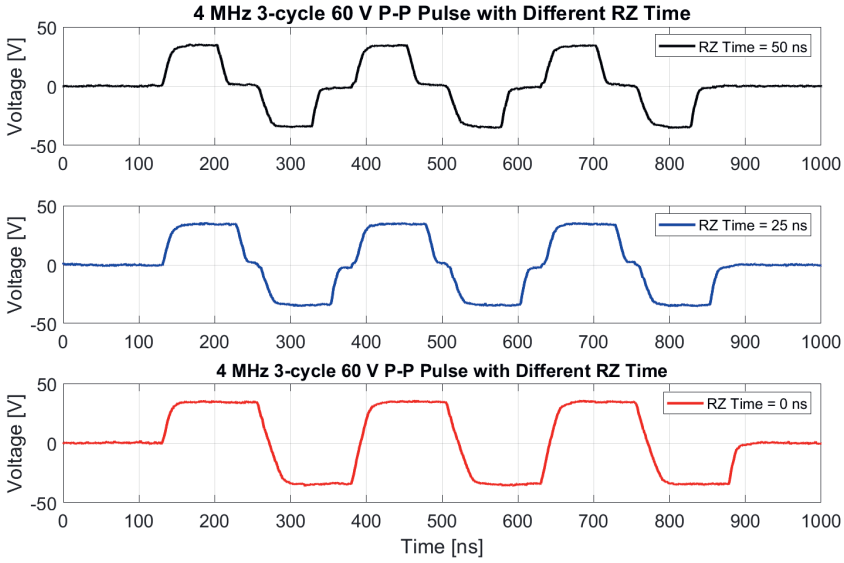


Figure 3.13. Measured output voltage for different programmed RZ times.

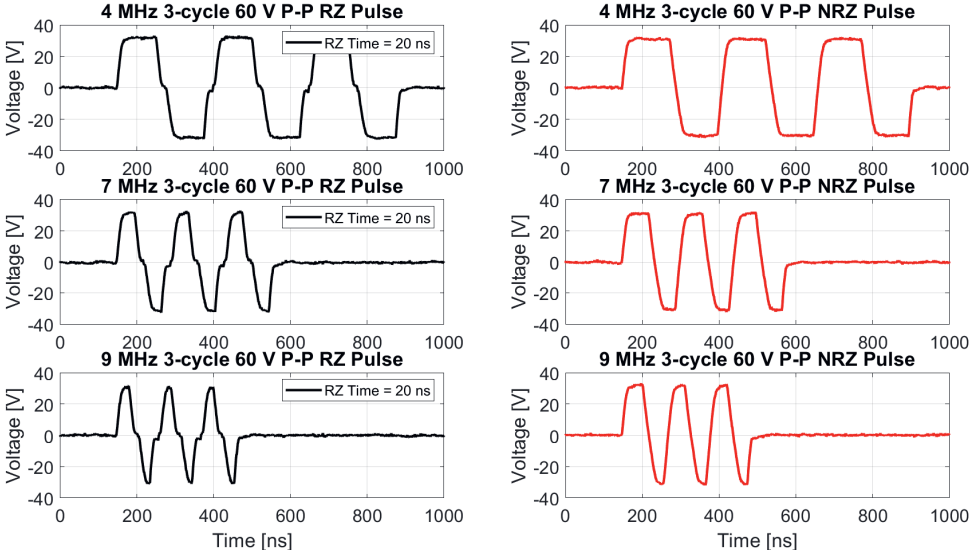
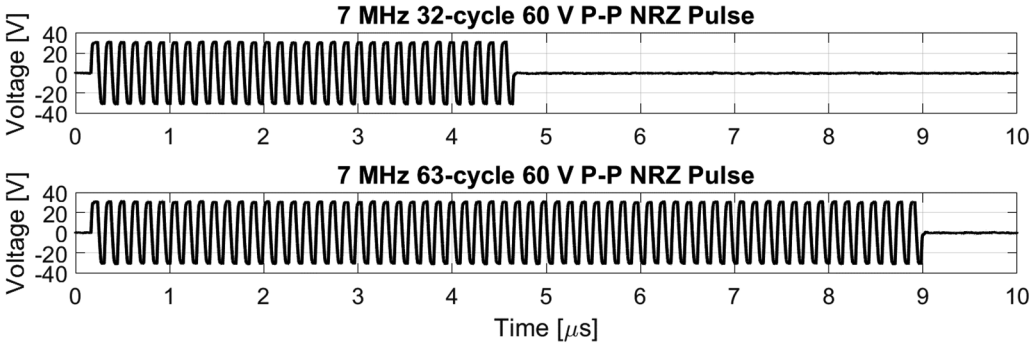
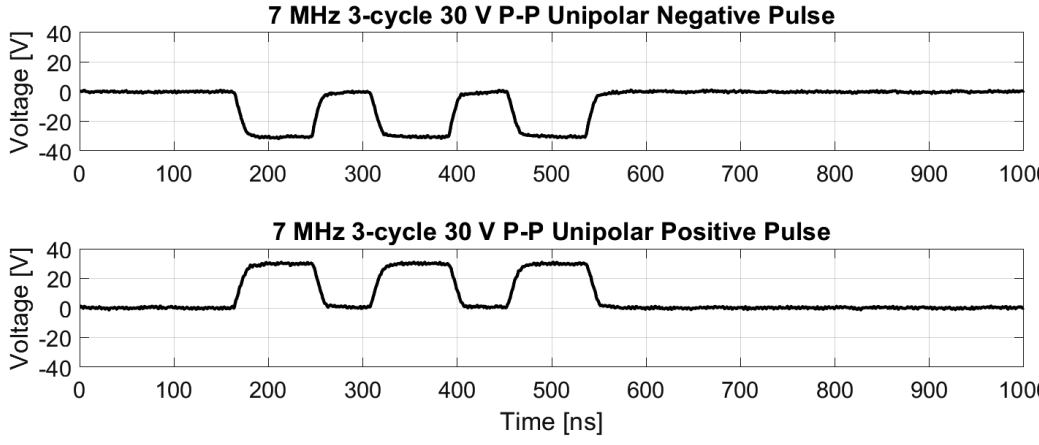


Figure 3.14. Measured output voltage for different programmed pulse frequencies.

To electrically demonstrate the delay-control functionality of the beamformer, different start times are programmed into the shift registers of two channels in the ASIC. When the start time difference is set to a minimum value of 1 for channel 1 and channel 2, the measured delay is around 6.3 ns as shown in Figure 3.16a. which is slightly larger than the intended delay of 5 ns. When the start time difference is set to a maximum value of 4093 for channel 1 and channel 2, the measured delay is around 20.4714 μs as shown in Figure 3.16b, which is slightly larger than the intended value of 20.465 μs. The mismatch between the measured and intended delay is less than 5% of the cycle time of the 7-MHz pulses and has a negligible impact on the beamforming. It is likely caused by the imperfect clock distribution across the ASIC and mismatch of the level shifters among different channels.



(a)



(b)

Figure 3.15. Measured output voltage for (a) 7-MHz 32- and 63-cycle NRZ pulses, and (b) 7-MHz 3-cycle 30-V unipolar negative and positive pulses.

Crosstalk performance has also been evaluated by disabling one channel and pulsing on an adjacent channel. The measured output voltages and the corresponding spectra of both channels are shown in Figure 3.17. The measured crosstalk is around -66 dB at 7 MHz, which makes its impact on the beamforming negligible.

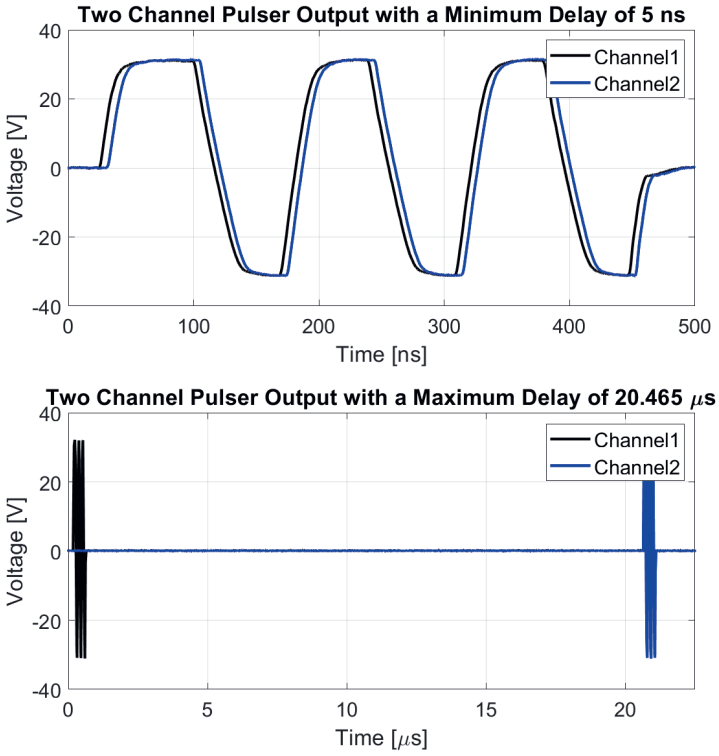


Figure 3.16. Measured minimum and maximum delay of two pulser channels.

An important performance metric of the T/R switch is its on-resistance. Since the T/R switch is placed in between the CMUT element and the TIA, its finite on-resistance adds noise to the received echo signal. This should be smaller than the noise of the CMUT element (which in our design can be modelled as 18 pF//17 kΩ at resonance) so as to not degrade the noise figure. The measured on-resistance of 180 Ω is in reasonable agreement with the simulated value of 155 Ω. At this level, T/R switch increases the noise figure by 4.7 dB, which indicates there is room of improvement by reducing the on-resistance of the switches.

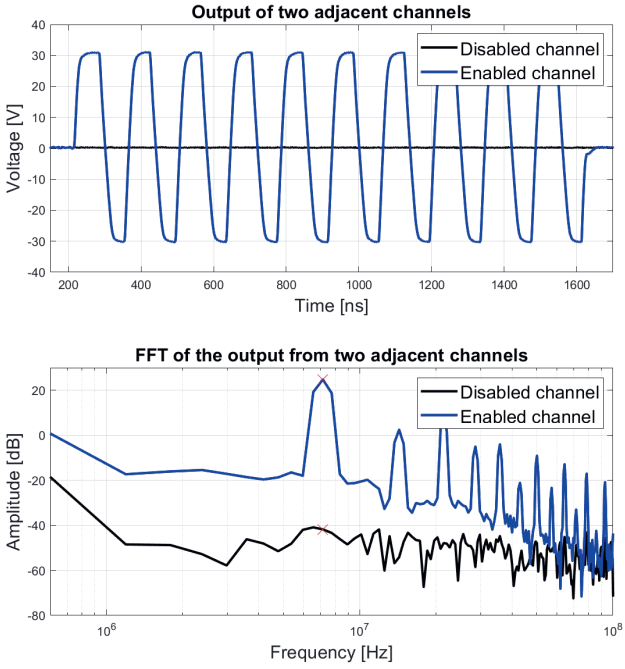


Figure 3.17. Measured crosstalk between two adjacent channel.

The ASIC's power consumption is highly dependent on the pulse repetition frequency (PRF) and the number of pulse cycles programmed. The power consumption of the TX circuitry strongly depends on the ultrasound imaging mode and is dominated by the dynamic power consumed in driving the transducer capacitance. The RX circuitry, which is described in more detail in [17], consumes on average 4.9 mW per channel. Figure 3.18 shows the power breakdown for 3-cycle pulses at a PRF of 4 kHz. The total TX power per channel is then around 1 mW, which is dominated by the pulser.

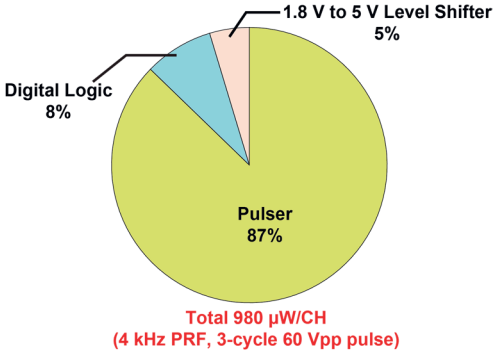


Figure 3.18. Power-consumption breakdown of TX

3.5.3 Acoustical Measurement Results

To acoustically evaluate the transmit beamforming, the ASIC and the CMUT transducer have been flip-chip mounted on two sides of a printed circuit board (PCB), as shown in Figure 3.19. To provide a test medium that is acoustically similar to the human body, this prototype was placed at the surface of a water tank, with the CMUT side immersed. Via a connector on the PCB, the ASIC was connected to power supplies, an FPGA that provides the clock and data signals to program the ASIC, and a Verasonics imaging system that records the received echo signals.

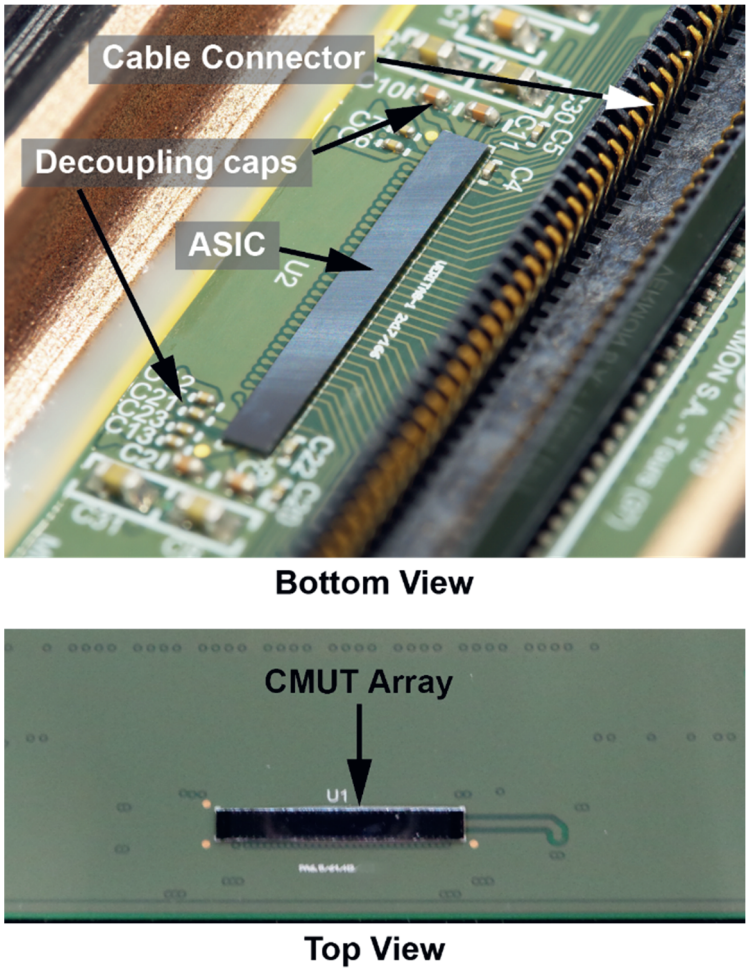


Figure 3.19. Assembled ASIC-PCB-CMUT prototype.

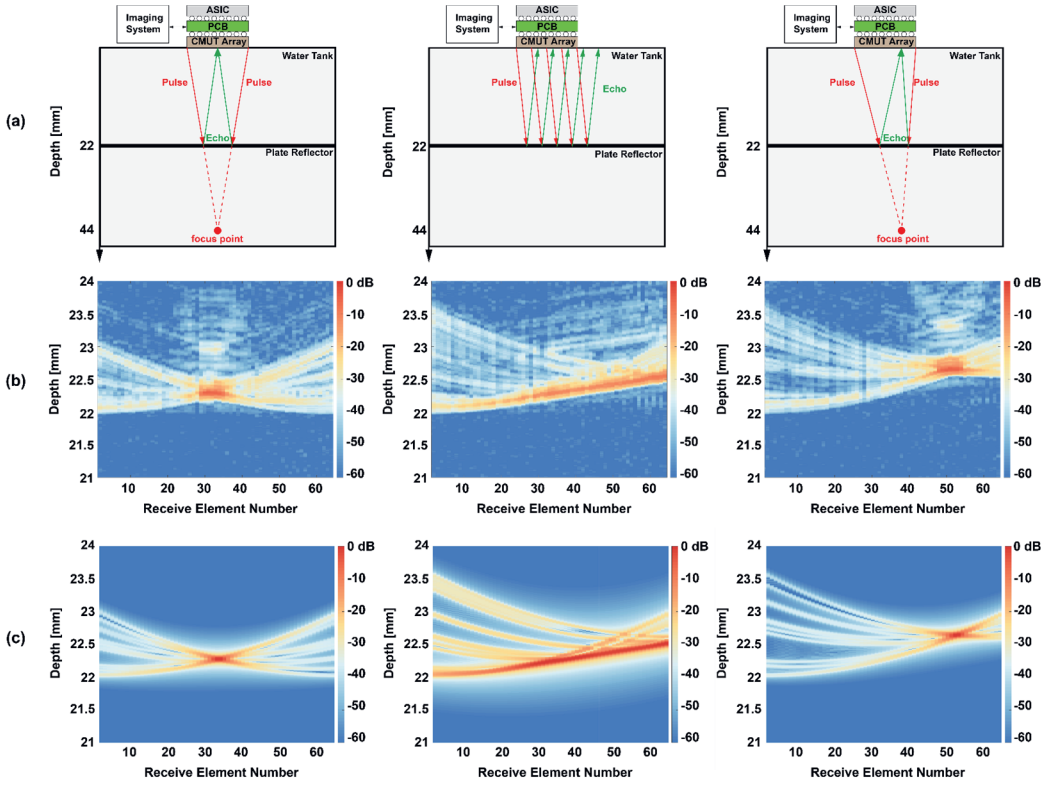


Figure 3.20. Acoustic transmit beamforming experiment with a focused beam (left), steered beam (middle) and focus and steered beam (right): (a) acoustic measurement setup with a sketch of the beam, (b) measured echo signals from a pulse-echo experiment using the ASIC, (c) simulated echo signals.

To demonstrate the beamforming capability, the ASIC was configured to drive the CMUT array so that it generates various ultrasound beams (focused, steered, both), as shown in Figure 3.20a. A plate reflector was placed at 22 mm from the transducer array, causing the transmitted acoustic waves to reflect back to the transducer array, where they are recorded through the RX channels of the ASIC. As shown in Figure 3.20b, programming the TX beamformer to focus at 44 mm (round-trip distance between the transducer and the plate reflector) causes the reflected pulse to focus at the transducer array, as expected, even when steering delays are added. Transmission of a plane wave at an angle of 5 degrees results in the reception of the expected reflected plane wave at the same angle. Figure 3.20c shows, for comparison, echo signals are simulated using DREAM Matlab toolbox [19]. It should be noted that 9 elements in the array were not working, which was also taken into account in the simulation. (These missing elements (spread across the array) are responsible for additional edge waves that can be observed both in the measurements and simulations.) The measurement results are in very good agreement with the simulations, confirming the correct operation of the beamformer.

TABLE 3-1. COMPARISON WITH THE PRIOR ART

HV 3-level Pulser			
	This Work	JSSC'19 [4]	JSSC'13 [19]
Technology	TSMC 180nm HV BCD	XFAB 180nm HV SOI	TSMC 180nm HV CMOS[a]
T/R embedded	Yes	No	No
Bipolar pulse	Yes	Yes	No
# HV MOS[b]	10	10[c]	10[c]
# HV diodes	0	2	0
Max output	60 V_{pp}	138 V_{pp}	30 V_{pp}
Pulse freq.	9 MHz @ 18pF	2 MHz	3.3 MHz @ 40pF
Area	0.167 mm^2	0.09 mm^2 [d]	0.33 mm^2 [d]
Floating-Gate Driver			
	This Work	ESSCIRC'18 [18]	JSSC'18 [5]
Technology	TSMC 180nm HV BCD	N/A	TSMC 180nm HV BCD
Application	RZ & T/R switch	HV switch (bipolar)	HV switch (unipolar)
# HV MOS	1	3	1
# HV diodes	0	3	0
# Passives[e]	1	6	4
Transmit Beamformer			
	This Work	TBCAS'18[11]	JSSC'19 [4]
Delay Resolution	5 ns	5 ns	25 ns
Delay Dynamic Range[f]	72 dB	66 dB	54 dB
# Channels	64	64	3072

a) Gate-oxide can handle 30 V swing. b) Including HV MOS in level shifters.
c) excluding HV transistors in T/R switch. d) Area for RX circuitry also included.
e) Capacitors, resistors and Zener diodes. f) Delay Dynamic Range = 20 · log10(max_delay / min_delay).

TABLE 3-1 compares the proposed HV pulser, floating-gate driver and transmit beamformer with the prior art. In contrast with earlier pulsers [4], [20], this chapter provides embedded T/R switch functionality without increasing the number of the HV transistors. Note that an area comparison is somewhat arbitrary, given the different pulser specifications and given that [4] uses SOI technology with smaller lateral dimensions for HV isolation than the junction-isolated technology used in this chapter. We expect our proposed pulser topology is equally applicable in such technology and would provide an area benefit when optimized for the much smaller matrix transducer elements used in [4]. Moreover, the floating-gate driver requires fewer HV components than those used in earlier HV switches [5], [18]. The transmit beamformer achieves the same delay resolution of 5 ns and the same number of elements of 64 with the highest delay dynamic range of 74 dB.

3.6 Conclusion

This chapter has described a 64-channel transmit beamformer with programmable bipolar pulsers for catheter-based ultrasound probes. The transmit beamformer is programmed and configured through a single clock and data line to steer and focus an ultrasound beam at an

angle and depth that is defined in the imaging system. The compact HV pulser design includes an RZ switch that has been constructed such that it can also serve as T/R switch. A new floating-gate driver that uses only a single HV transistor provides level-shifting functionality to turn on and off the MOS transistors in the switch. Thus, the number of HV transistors and passive components required is reduced. Electrical and acoustical experimental results obtained in combination with a 64-element CMUT array successfully demonstrate the functionality of the HV pulser and TX beamformer.

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Chapter 4

An Ultrasound Analog-Front-End with Variable-Gain Low-Noise Transimpedance Amplifier

This chapter is based on the publication "A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes," in IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3157-3168, Dec. 2020.

4.1 Introduction

Ultrasound imaging is a safe and cost-effective tool for the diagnosis of medical conditions and the guidance of treatment. Size reduction of imaging devices has enabled ultrasound imaging from the tip of a mm-size catheter, for instance for intracardiac echocardiography (ICE), as illustrated in Figure 4.1(a) [1], [2]. Applications of ICE probes include guidance and monitoring of catheter ablation for the treatment of atrial fibrillation, guidance of closure of atrial septal defects, and guidance of transcatheter valve implantation [3], [4].

ICE probes, and other miniature ultrasound probes alike, employ an array of ultrasound transducer elements to transmit ultrasonic pulses and record the resulting echo signals, from which an image is reconstructed using beamforming techniques [5]. In many probes, each transducer element is electrically connected via a cable to the external imaging system [5]–[7]. However, this approach limits the number of transducer elements due to the limited number of cables that can be accommodated, and results in signal attenuation due to the fact

that the cables load the elements. Increasingly, application-specific integrated circuits (ASICs) are integrated in the probe close to the transducer array to address these issues [8]–[13].

Figure 4.1(b) shows a block diagram of the front-end of such an in-probe ASIC. For each transducer element, it contains transmit (TX) and receive (RX) circuitry. The former tends to include a high-voltage (HV) pulser that drives the element to generate a pressure wave [8]–[11]. At the start of the RX signal path, a low-noise amplifier (LNA) amplifies the echo signal so that it can be further processed by the following circuitry, which may involve beamforming, multiplexing and digitization [12], [13].

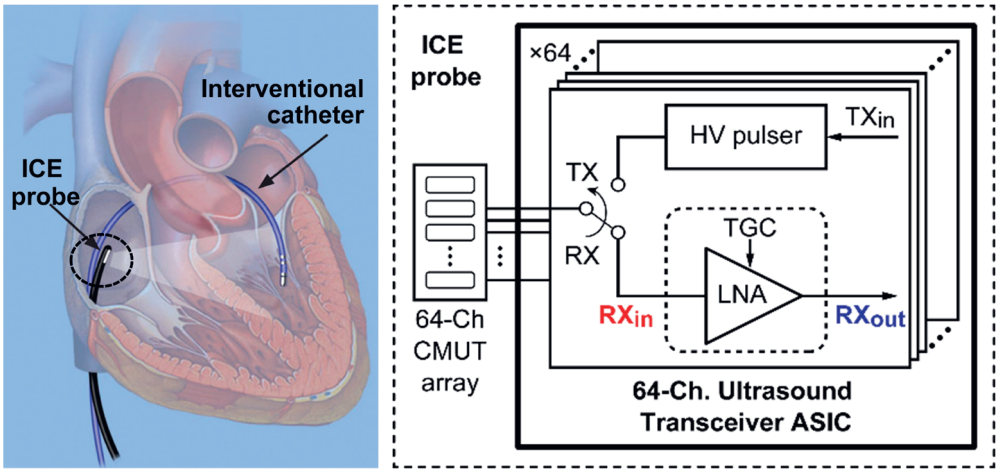


Figure 4.1 (a) Application scenario of an ICE probe; (b) block diagram of the transceiver ASIC with the proposed TIA.

An important function in the RX signal path is time-gain compensation (TGC), which reduces the echo-signal dynamic range (DR) by compensating for the propagation attenuation experienced by the acoustic waves as they travel through the body [14]. Due to this attenuation, echo signals from deep tissue, which need to travel longer than echoes from nearby structures and therefore arrive later, are more attenuated. This leads to an exponential decrease in echo amplitude with time, as illustrated in Figure 4.2(a). Since propagation attenuation increases with frequency [14], this is particularly significant at the relatively high frequencies (>5 MHz) typically used in miniature probes. The attenuation may amount to 40 dB at the largest imaging depth. It can be compensated for by providing a gain that increases linearly in dB as a function of time, thus providing a uniform echo amplitude across depth, as illustrated in Figure 4.2(b).

The impact of TGC on the signal DR is further illustrated in Figure 4.2(c), which shows how the range of echo-signal levels (the instantaneous DR) varies as a function of time (or, equivalently, depth) before and after TGC, demonstrating that the time-dependent

attenuation is corrected for, thus reducing the overall DR to a level similar to the instantaneous DR. In conventional ultrasound systems, TGC is typically performed after the LNA [15], as shown in Figure 4.3(a), implying that a power-hungry LNA is required that is capable of handling the full DR of the echo signal at its output.

In this chapter, we present an LNA with a built-in continuous TGC function that mitigates this problem, as shown in Figure 4.3(b) [16]. The LNA is a transimpedance amplifier (TIA) optimized to amplify the signal current of a capacitive micro-machined ultrasound transducer (CMUT). We demonstrate its integration into a 64-channel ASIC for a CMUT-based ICE probe, as shown in Figure 4.1(b). While the LNA has been designed for application in an ICE probe, the presented amplifier architecture is applicable to ultrasound front-ends for miniature ultrasound probes in general.

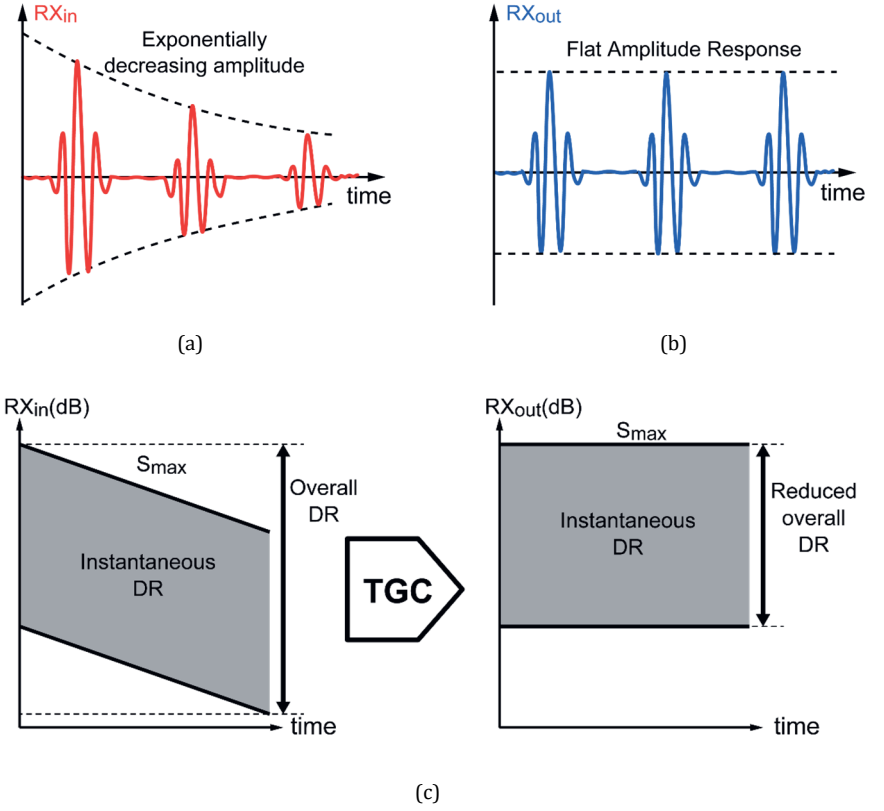
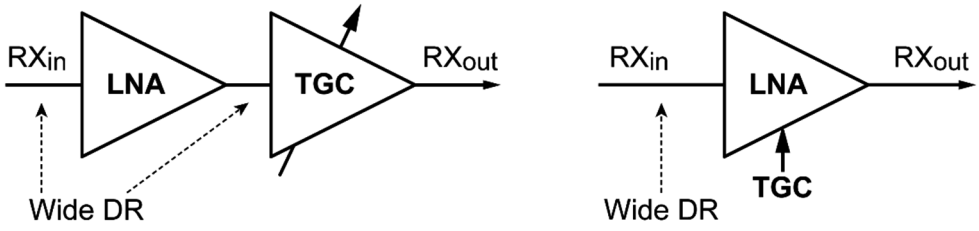


Figure 4.2 (a) RX signal before time-gain compensation (TGC); (b) RX signal after TGC; (c) RX input and output signal range as a function of time with ideal time-gain-compensation.

This chapter is organized as follows. Section 4.2 reviews the existing approaches for TGC. Section 4.3 describes the proposed TIA architecture. The circuit implementation details of

the TIA are presented in Section 4.4. Electrical measurements and imaging experiments are presented in Section 4.5. The chapter ends with a comparison with the state-of-the-art and conclusions.



(a) (b)

Figure 4.3 (a) block diagram of the conventional solution of an LNA followed by a TGC amplifier; (b) block diagram of the proposed LNA with embedded TGC function.

4.2 Comparison of TGC Circuits

Various approaches have been taken to realize amplifiers suitable for TGC. They can globally be divided into two groups: amplifiers with discrete gain steps and amplifiers with continuous gain control.

Amplifiers with discrete gain steps approximate the ideal exponentially - varying gain by a number of discrete gain steps that are sequentially applied. An important advantage of this approach is that the gain steps can be accurately defined by means of a digitally - programmable resistive feedback network, as illustrated in Figure 4.4(a) [17]–[21], a digitally - programmable capacitive feedback network [12], [13], [22], or a digitally - programmable current - steering feedback network [23]. Moreover, the gain steps can be divided among multiple amplifier stages, with course gain steps realized in the low - noise amplifier (LNA) at the input of the receive signal path, which enables the realization of highly power - efficient amplifiers [12], [19]. Switching from one discrete gain step to the next, however, is typically associated with a switching transient that can lead to artefacts in the ultrasound image at a depth that corresponds to the gain - switching moment. Such artefacts can be made negligible by making the gain steps small [20], but this requires a large number of gain steps to cover the gain range, leading to a complex circuit that requires substantial die area.

Amplifiers with continuous gain control are also referred to as variable - gain amplifiers (VGAs) and typically have a gain that can be set by an analog control input, typically a control voltage. The gain tends to depend (approximately) exponentially on the control voltage,

giving a linear - in - dB gain control. By ramping the control voltage linearly as a function of time, the gain can be swept across a desired range to realize TGC without the disadvantages associated with discrete gain steps. The many ways in which this can be realized can be roughly divided into two categories: amplifiers with an approximately exponential transfer function, and amplifiers with interpolation between discrete gain steps.

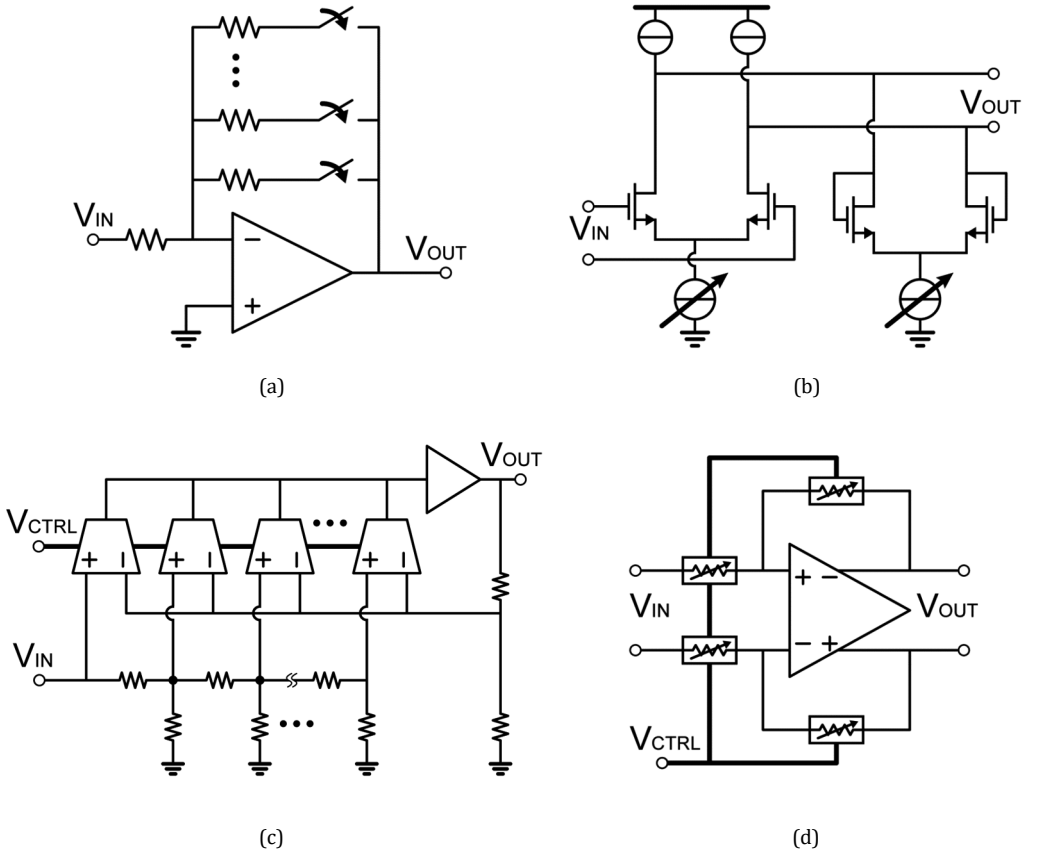


Figure 4.4 Circuits to realize time-gain compensation: (a) amplifier with discrete gain steps [17]-[21]; (b) amplifier with time-varying biasing [24]; (c) amplifier that interpolates between the outputs of a resistive ladder attenuator [29]; (d) amplifier using a feedback network with MOS variable resistors [23].

Amplifiers with an approximately exponential transfer function typically exploit the non - linear characteristics of MOS or bipolar transistors to realize variable gain. This can be done, for instance, by changing the operating point of a differential pair as a function of a gain - control voltage, leading to a variable transconductance. Combined with a load with an impedance that is also dependent on the control - voltage, for instance, by changing the operating point of diode - connected transistors as a function of the same control voltage, an

amplifier with a non‐linear transfer function is obtained, as shown in Figure 4.4(b) [24], [25]. However, this non‐linear transfer function only approximates an exponential across a limited gain range, and tends to be sensitive to process, supply voltage and temperature (PVT) variations. Multiple stages can be cascaded to extend the range [26], [27].

Another approach to approximate an exponential transfer function is to use the exponentially increasing output voltage of a positive‐feedback amplifier during a well‐defined time window [28]. This approach, however, requires that the signal is sampled at the amplifier's input, allowing each successive sample to be amplified using the positive‐feedback amplifier, and the gain to be varied from sample to sample by changing the positive‐feedback time window.

A TGC amplifier topology with interpolation between discrete gain steps has been reported in [29], [30]. As illustrated in Figure 4.4(c), the input signal is attenuated by a resistive ladder network, each section of which provides a fixed attenuation step in dB. These attenuated signals are fed to an amplifier with multiple input stages, the bias currents of which are controlled in order to gradually change from one step to the next. Another topology that employs multiple inputs stages with controlled biasing has been reported in [31], where the attenuating network is part of the feedback of the amplifier, and the input stages directly connect to the input in order to provide not only variable gain, but also simultaneously varying input noise and signal swing.

Interpolation between discrete gain steps can also be achieved by smoothly changing the components values in a passive attenuator network by including MOS transistors that act as variable resistors, as illustrated in Figure 4.4(d) [23], [32]. Special biasing circuits are needed in order to mitigate PVT dependence.

A third approach to achieve interpolation between discrete gain steps is to use a differential pair as a current‐steering device. In [33], a differential pair at the output of an amplifier directs a fraction of the output current back to the input, and a fraction towards the output. Thus, the current gain of this amplifier can be continuously controlled through the voltage applied to the differential pair. In an amplifier with two parallel input stages, [34] uses current steering to control how much of the output current of the current produced by these input stages are added to the output.

Compared to the prior art, the amplifier proposed in this work has three appealing features. Firstly, it provides continuous TGC, avoiding the switching artefacts associated with discrete gain steps. Secondly, as the TGC function is realized in the LNA, it does not rely on a preceding (fixed-gain) LNA to obtain a good noise figure and/or to obtain a suitable input impedance, like in e.g. [23], [29], [30], [35]. Such a fixed-gain LNA has an output DR that equals the large input DR, which tends to be associated with additional power consumption in the output stage to achieve acceptable distortion at the largest signal levels, or with additional power consumption to reduce noise in the stage after the LNA if the LNA's gain is kept limited to

avoid distortion. Thirdly, as it relies on capacitor ratios to define the gain, it avoids the additional noise associated with a resistive feedback network, and the PVT dependence of approaches that rely on non-linear device characteristics.

4.3 Architecture of the TIA with TGC

4.3.1 Current Amplifier based TIA

As mentioned, the proposed TIA has been designed to interface with a CMUT transducer. Such a transducer consists of a flexible micro-machined membrane that forms one of the electrodes of a parallel-plate capacitor. In response to an incoming pressure wave, the membrane is moving, leading to a small change in the capacitance. When the CMUT is DC biased, this change can be detected as a signal current [36]. The CMUT can then modeled as a signal-current source Iin shunted by a capacitance CCMUT modeling the transducer's electrical capacitance, and a resonator representing its mechanical resonance, as shown in Figure 4.5. The transducer used in this work is operated at 5 MHz and has a capacitance of 15 pF.

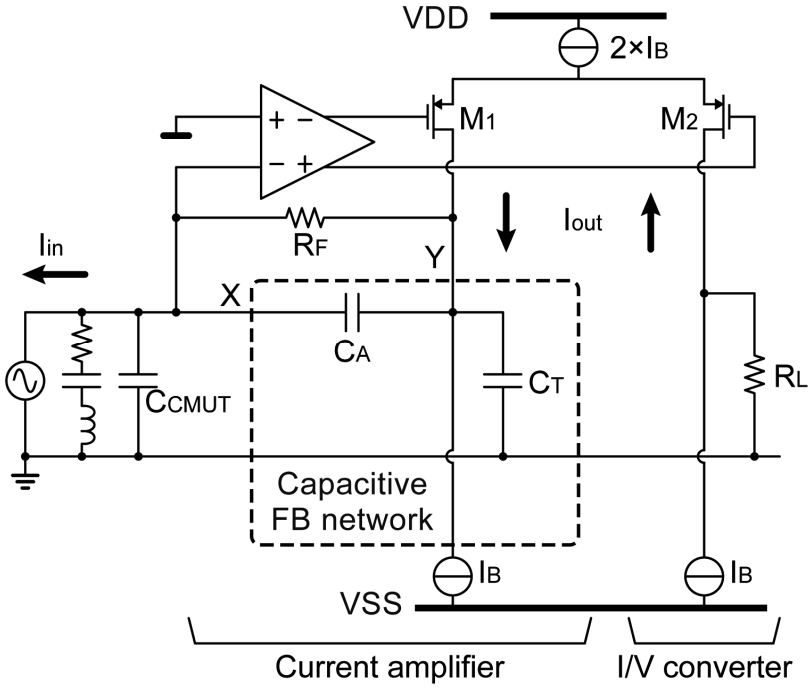


Figure 4.5 Simplified circuit diagram of the proposed TIA with a fixed-gain capacitive feedback network.

To detect the signal current, a low-noise amplifier with a low input impedance is needed, making a TIA is a suitable choice [37]. In this work, an input-referred noise level of 2 pA/√Hz and a maximum signal current of 100 µA is targeted. A TIA with resistive feedback is commonly used [38], but does not readily support the widely variable gain needed for TGC. Moreover, resistive feedback contributes additional noise.

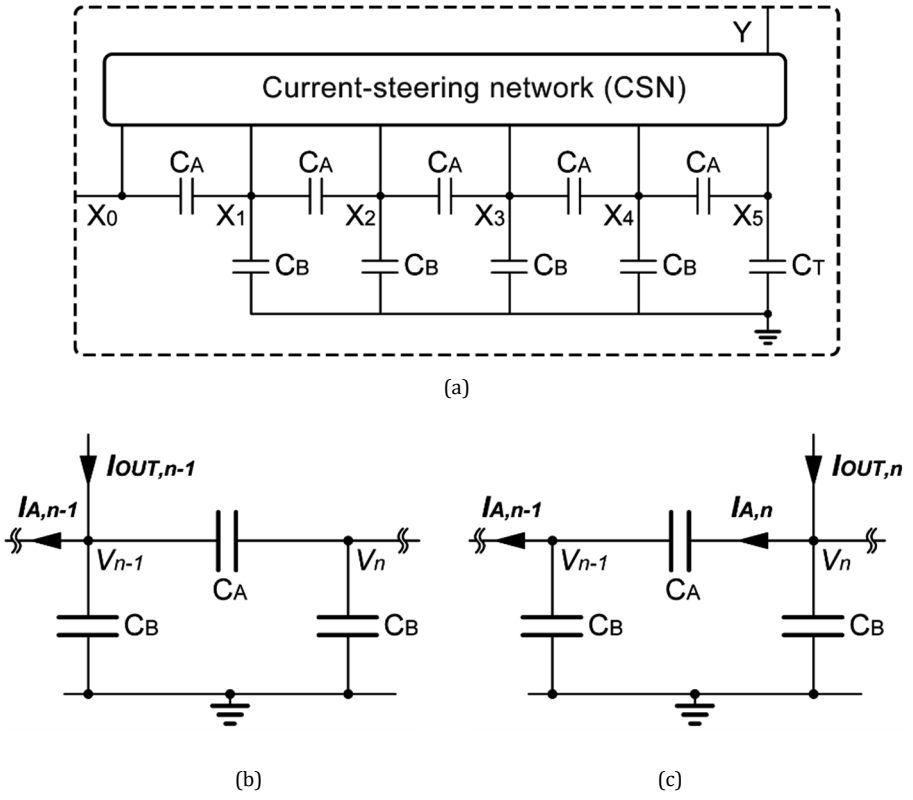


Figure 4.6 (a) Capacitive ladder feedback network with CSN to realize variable gain; (b) an arbitrary section of the ladder network, with a feedback connection to node *n – 1*, and (c) to node *n*.

Therefore, instead, we use a TIA based on a current amplifier with capacitive feedback as a starting point, based on [39]. As shown in Figure 4.5, this TIA consists of a current amplifier with a gain defined by capacitors CA and CT, followed by a resistive load RL that turns the amplified current into an output voltage. A high-ohmic feedback resistor RF serves to set the DC operating point and plays a negligible role at the signal frequencies of interest. A loop amplifier senses the input voltage V_X so as to maintain a virtual ground at the input. As a

result, the input current I_{in} is integrated on capacitor CA, leading to a voltage V_Y across capacitor CT, and an amplified output current

$$I_{OUT} = \left(1 + \frac{C_T}{C_A}\right) I_{IN} = \alpha I_{IN} \qquad (1)$$

Thus, the circuit provides a current gain of $\alpha = 1 + C_T/C_A$. We use this current gain mechanism to implement the required 40 dB gain range, as will be discussed shortly.

In contrast with [39], in which a single-ended loop amplifier and a source follower with a resistive load are used, we employ a fully-differential loop amplifier, and a differential pair (M1 and M2) that provides equal currents of opposite polarity to the feedback network and to RL, to convert the amplified current to an output voltage. To avoid clipping, the bias current I_B should be larger than the maximum amplified current. The resulting overall transimpedance is $(1 + C_T/C_A)R_L$. This differential topology helps to reduce power-supply sensitivity and increases output voltage headroom.

4.3.2 Capacitive Ladder Feedback Network

Although variable gain could be realized by adjusting C_T/C_A, this would require a large capacitor ratio to achieve a 40 dB range, and dense gain steps to minimize switching artefacts between the gain steps. This would be unattractive in terms of die size and complexity. Therefore, as shown in Figure 4.6(a), we realize gain steps covering a wide range by means of a ladder structure, and then interpolate between these steps by means of a current-steering network.

Ignoring the interpolation for now, let us assume that the feedback node Y is connected to one of the nodes of the ladder network X_n ($0 \leq n \leq 5$ in our design). The ladder capacitors CA, CB and CT are dimensioned such that the capacitance to ground at each node X_n equals C_T, which implies

$$C_B + \frac{C_A C_T}{C_A + C_T} = C_T \Rightarrow C_B = \frac{C_T^2}{C_A + C_T} \qquad (2)$$

We will now show that this choice causes every ladder section to contribute an additional gain factor $\alpha = 1 + C_T/C_A$. If the feedback is connected to node X_0, the output current $I_{OUT,0}$ equals I_{IN}, corresponding to a gain of 1 ($= \alpha^0$). The ladder network then merely forms an additional capacitive load at the input. If the feedback is connected to X_1, the topology is the same as in Figure 4.5, and the output current equals $I_{OUT,1} = \alpha I_{IN}$.

Now consider a feedback connection to an arbitrary node X_{n-1}, associated with an output current $I_{OUT,n-1}$, as shown in Figure 4.6(b), and a feedback connection to the next node X_n,

with output current $I_{OUT,n}$, as shown in Figure 4.6(c). Given that the feedback network is a linear passive network, the current $I_{A,n-1}$ flowing back towards the input and the voltage V_{n-1} at node X_{n-1} must be equal, implying

$$I_{A,n-1} = I_{OUT,n-1} - sC_T V_{n-1} = I_{A,n} - sC_B V_{n-1} \qquad (3)$$

where $I_{A,n}$ is the current flowing in Figure 4.6(c) through the capacitor CA connecting node X_{n-1} to node X_n. This current can also be expressed in terms of $I_{OUT,n}$:

$$I_{A,n} = \frac{C_A}{C_A+C_T} I_{OUT,n} - s\frac{C_A C_T}{C_A+C_T} V_{n-1} \qquad (4)$$

where the first term represents the fraction of $I_{OUT,n}$ that would flow to node X_{n-1} if V_{n-1} would be zero, and the second term represents the current flowing from node X_{n-1} to node X_n if $I_{OUT,n}$ would be zero. Substituting (2) and (4) into (3) gives

$$I_{OUT,n} = \left(1 + \frac{C_T}{C_A}\right) I_{OUT,n-1} = \alpha I_{OUT,n-1} \qquad (5)$$

which proves by induction that $I_{OUT,n} = \alpha^n I_{IN}$.

Thus, by an appropriate choice of the capacitor values, exponential gain steps can be realized without requiring large capacitor ratios. In our implementation, we adopted a 5-section ladder network with $\alpha = 2.5$ (i.e. gain steps of 8 dB covering 40 dB) realized using integer multiples of a unit capacitor C_U: $C_A = 10C_U$, $C_B = 9C_U$ and $C_T = 15C_U$. This allows for a compact and well-matched layout. The value of C_U should be sufficient to keep the voltage swing in the network limited, and to make the impact of parasitic capacitance on the gain negligible. We use 0.3 pF to limit the swing to 360 mV at a maximum I_{IN} of 100 µA at 5 MHz.

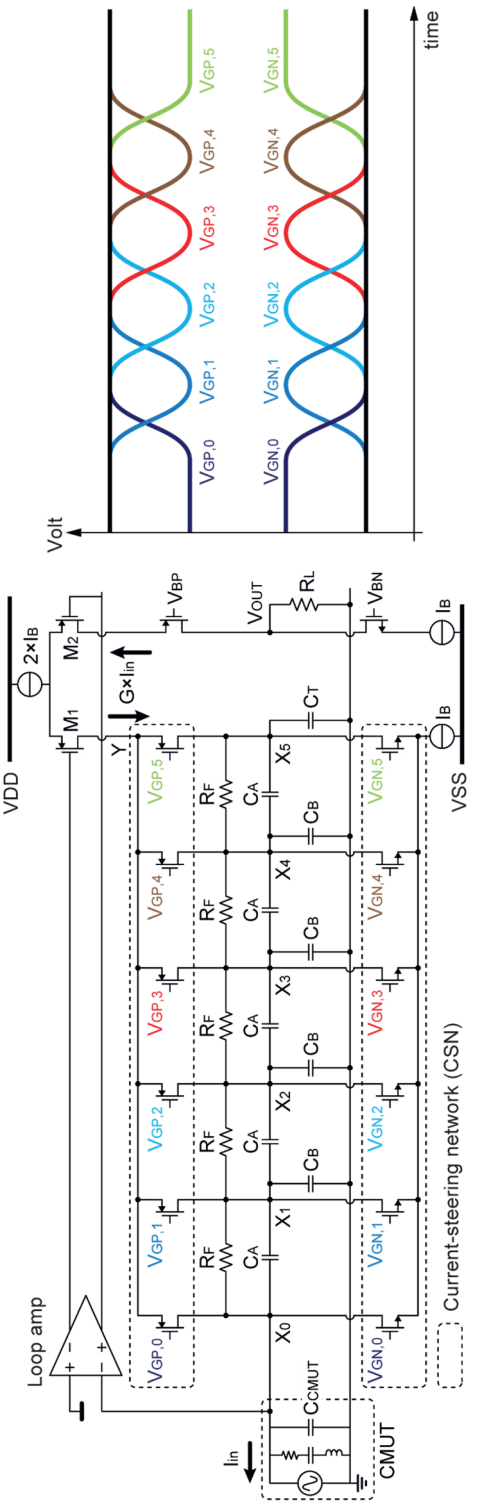
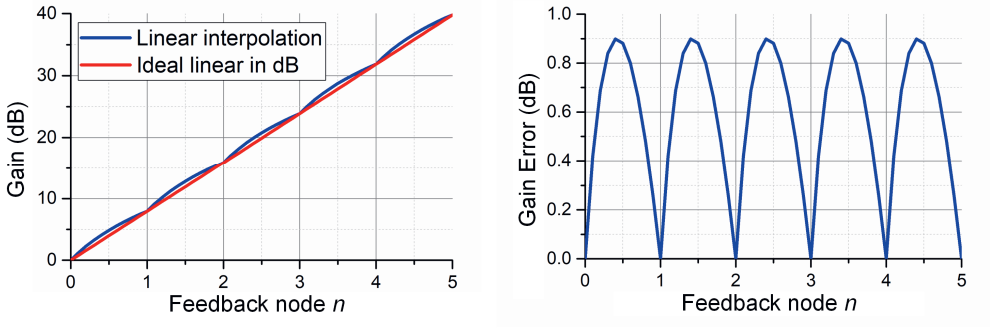


Figure 4.7 (a) Circuit diagram of the proposed TIA; (b) the gate-control voltages for the CSNs for continuous gain control.

4.3.3 Interpolation by means of Current Steering

To interpolate between the gain steps of the ladder network, we propose a current steering network (CSN) as shown in Figure 4.7(a). A set of PMOS transistors directs the feedback current at node Y to the ladder nodes Xn. The feedback current is initially steered completely to the input node X0, by providing a lower gate voltage V_(GP,0) to the corresponding PMOS transistor, as shown in Figure 4.7(b). The feedback current then gradually shifts from node to node, by alternately pulling down the gate voltages V_(GP,n), effectively linearly interpolating between the exponential gain steps of the ladder network. Finally, the feedback current is steered entirely to the last tap, providing maximum gain. To bias the circuit, a complementary NMOS CSN, with similar complementary gate-drive voltages V_(GN,n), steers a bias current IB to the nodes of the feedback network. High-ohmic resistors RF in the feedback network prevent charge accumulation due to small current differences between the CSNs, without affecting the in-band AC current gain.



(a) (b)

Figure 4.8 (a) Gain as a function of the selected feedback node Xn, for linear interpolation and for an ideal linear-in-dB curve; (b) Corresponding gain error relative to the linear-in-dB curve.

The CSN provides an approximately linear interpolation between exponential gain steps. The resulting error with respect to an ideal linear-in-dB (exponential) gain curve is shown in Figure 4.8. A ladder network consisting of 5 sections with a gain step of 8 dB each has been chosen to achieve a gain error less than 1 dB, in line with the requirements of the imaging application. This can be reduced by increasing the number of ladder sections. Note that the sharp dips in the gain-error curve in Figure 4.8(b) are due to the ideal linear interpolation applied. The actual implementation using PMOS transistors and smoothly-varying gate voltages as illustrated in Figure 4.7(b) will lead to less sharp transitions in the gain-error curve.

4.3.4 Noise Analysis

To be able to detect the smallest echo signals at the highest gain, the TIA's noise contribution should not exceed that of the transducer. At the high end of the gain range, the noise contribution of the load resistor, the output differential pair and the bias-current sources is negligible, because they are attenuated by the 40 dB current gain when referred to the input. The feedback network, due to its capacitive nature, does not contribute in-band noise. This leaves the loop amplifier as the dominant noise source. Its input-referred voltage noise appears at the virtual ground and leads to an equivalent input current noise due to the total impedance to ground at the input. This impedance is dominated in our design by the CMUT capacitance of about 15 pF, and amounts to about 2 kΩ at 5 MHz. To achieve an equivalent input current noise below 1.5 pA/√Hz, the loop amplifier's input voltage noise should be below 3 nV/√Hz. Note that this noise levels only needs to be achieved at the highest gain level. At lower gain levels, the input signal is bigger, and so proportionally larger noise can be accepted without loss of SNR. Achieving this noise level in a power-efficient manner is one of the key design objectives for the loop amplifier implementation, as will be elaborated in the next section.

4.4 Circuit Implementation

4.4.1 Gain-Control Circuit

To generate the gate-control voltages $V_{GP,n}$ and $V_{GN,n}$ for the CSNs in Figure 4.7(b), an external gain-control voltage V_{TGC} is compared to a set of reference voltages generated using a stack of cascaded PMOS differential pairs, as shown in Figure 4.9. The reference voltages $V_{REF,i}$ are generated using a resistive divider.

Thus, as V_{TGC} is swept, the tail current is steered from drain to drain. The drain currents are mirrored to diode-connected PMOS and NMOS transistors at appropriate common-mode levels to generate $V_{GP,n}$ and $V_{GN,n}$, respectively, resulting in the voltages shown in Figure 4.7(b) when V_{TGC} is linearly ramped down.

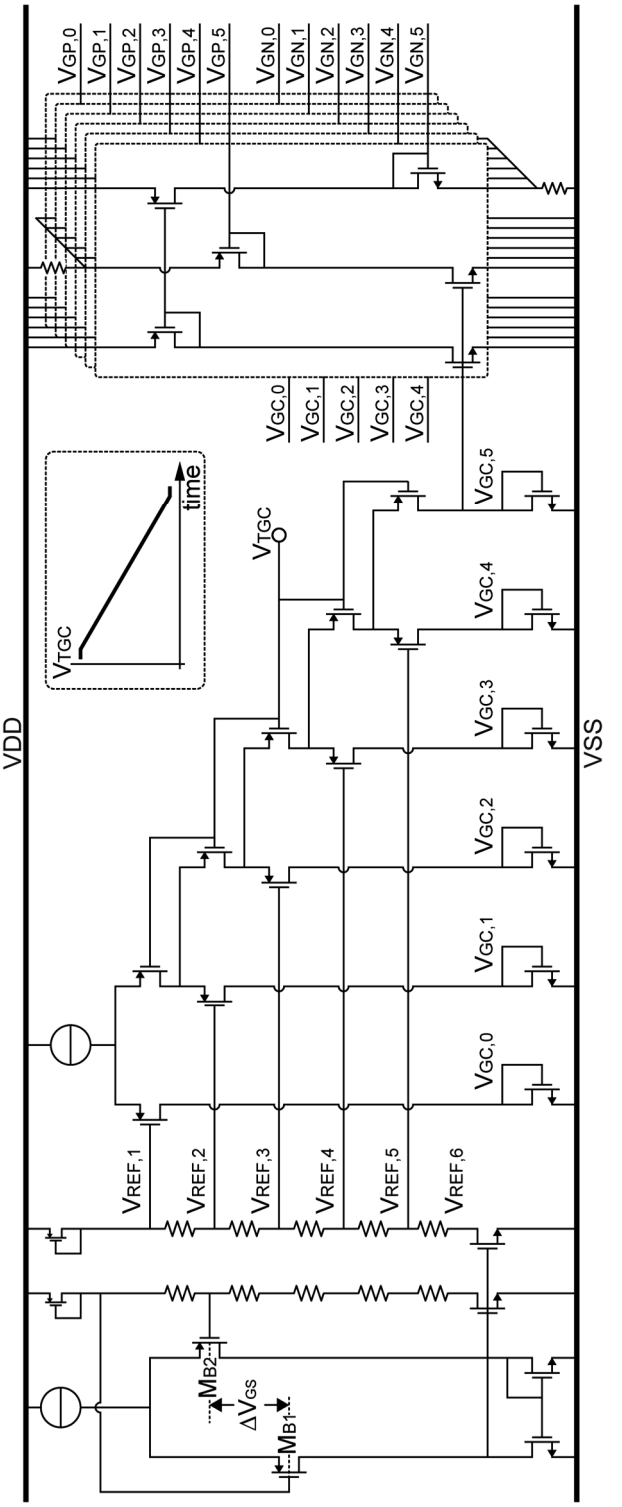


Figure 4.9 Circuit diagram of the gain control circuit

In this circuit, all PMOS differential pairs have identical sizes and have bulk connections to the source to mitigate the body effect. The bias current of the gain-control circuit is chosen such that the bandwidth of the circuit is sufficient to track the required V_{TGC} transient, while avoid excess bandwidth, as this would add undesired in-band noise to the signal path. The bias current for the resistive ladder is generated using the bias circuit shown in the left-hand side of Figure 4.9. This bias circuit employs a feedback loop to generate a current proportional to the difference in gate-source voltage ΔV_{GS} of ratioed PMOS transistors M_{B1} and M_{B2}. The bias circuit employs a replica of the resistive ladder, so that the voltage steps between the reference voltages equal ΔV_{GS}, making the current division in the PMOS differential pairs as a function of V_{TGC} insensitive to process and supply variations.

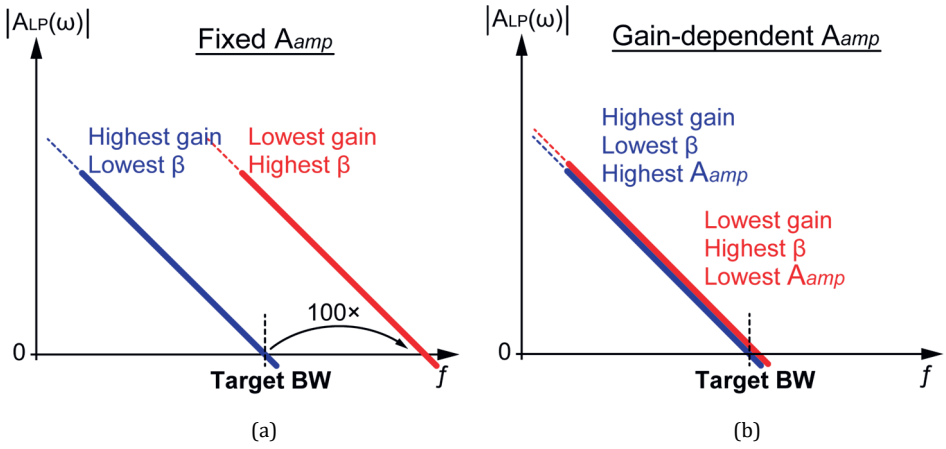


Figure 4.10 Magnitude of the loop-gain as a function of frequency, showing (a) a strongly gain-dependent unity-gain frequency for a fixed-gain loop amplifier, and (b) a constant unity-gain frequency for a loop amplifier with variable gain.

4.4.2 Loop Amplifier Design

A key challenge in the design of the loop amplifier is to maintain sufficient loop gain in the presence of the widely-varying current gain. We analyze the loop gain by breaking the feedback loop at the input of the loop amplifier. The resulting loop-gain $A_{LP}(\omega)$ consists of the product of the loop amplifier's voltage gain $A_{amp}(\omega)$ and the transfer function from the output of the loop amplifier back to the input:

$$A_{LP}(\omega) = A_{amp}(\omega) \cdot \frac{g_{m,out}\beta}{j\omega C_{in}} \qquad (6)$$

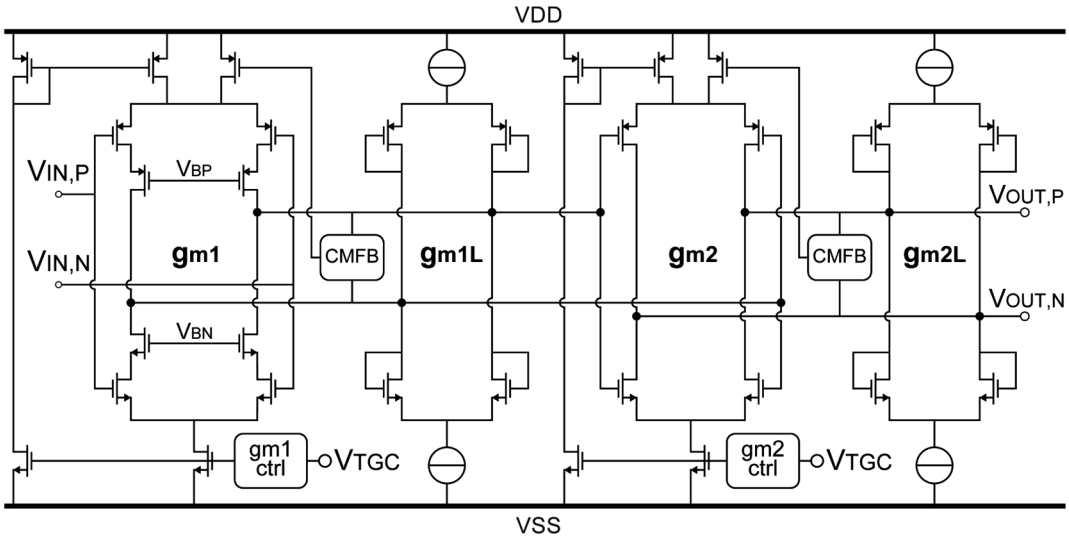


Figure 4.11 Circuit diagram of the loop amplifier.

where $g_{m,out}$ is the transconductance of the differential pair M1,2 (see Figure 4.5), β is the fraction of that differential pair's output current that makes it back to the input, and C_{in} is the total capacitance at the input, which is dominated by the CMUT capacitance C_{CMUT}. The fraction β is related to the closed-loop current gain, which in Section 4.3.2 has been shown to be αn. While the closed-loop current gain is independent of C_{in}, because $C_{in}$is at the virtual ground in the closed-loop configuration, C_{in} does influence the fraction β. However, if $C_{in} \gg C_T$, we can approximate the input as being shorted to ground by C_{in}, and the factor β is then by good approximation the inverse of the current gain α^n. If we assume that the loop amplifier has a constant gain and a wide bandwidth, i.e. that $A_{amp}(\omega)$ is constant across the frequency range of interest, this implies that for a 40 dB variation in current gain, the unity-gain frequency of $A_{LP}(\omega)$, which sets the closed-loop 3 dB bandwidth, would vary by a factor 100, as illustrated in Figure 4.10(a). In order to achieve enough bandwidth at the highest current gain, which corresponds to the lowest β, we would obtain a bandwidth that is 100 times larger than needed at the lowest current gain, which corresponds to the highest β. To realize this, the loop amplifier would need to have an unrealistically wide bandwidth.

Therefore, instead, we employ a loop amplifier whose gain $A_{amp}(\omega)$ is adjusted to compensate for the varying β. For the highest current gain (i.e. the lowest β), we make the DC gain of the loop amplifier roughly 100 times higher than for the lowest current gain (i.e. the highest β). This gives the loop an approximately constant unity-gain frequency, corresponding to an approximately constant closed-loop 3 dB bandwidth, as illustrated in Figure 4.10(b). Any poles in the loop amplifier should be sufficiently above this frequency to maintain stability.

Since the required gain-bandwidth product of the loop amplifier is hard to realize with a single-stage amplifier, we use a cascade of two stages, as shown in Figure 4.11. A fully-differential amplifier structure is adopted. The first stage consists of a current-reuse input stage with diode-connected load transistors, resulting in a gain set by the transconductance ratio g_{m1}/g_{m1L}. The transconductance of the input stage g_{m1} is defined by the tail current, which is shared by the NMOS and PMOS pair to improve power efficiency [40]. This tail current is varied as a function of the gain-control voltage V_{TGC} (details provided in Section 4.4.3) to obtain the required variable gain. Besides maintaining constant bandwidth, this scheme also saves power, by ensuring that the input stage is biased at the highest current level only at the high end of the gain range, where the lowest input noise is required, in line with the noise requirement discussed in Section 4.3.4. For lower gain levels, at which a higher input noise is acceptable, the bias currents are reduced.

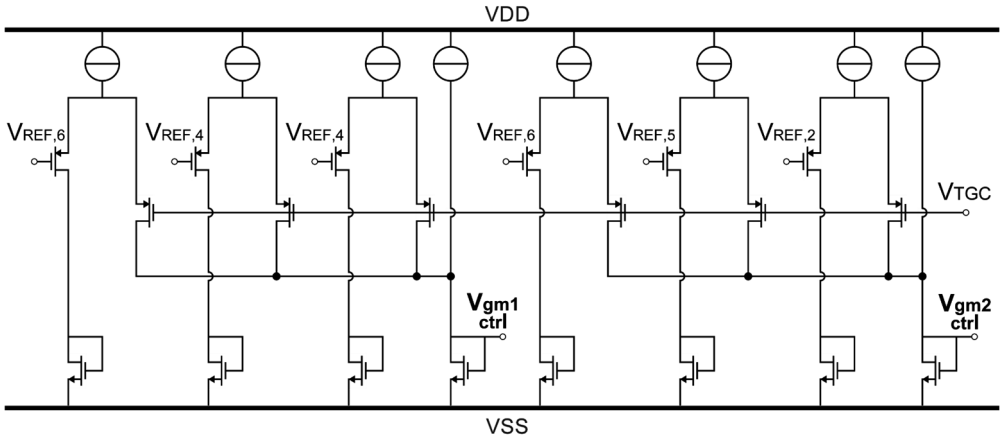


Figure 4.12 Circuit diagram of the transconductance-control circuit.

At the chosen bias point, the input transistors suffer from relatively low output impedance and large gate-drain capacitance, which degrades the gain and increases the input-referred noise. To mitigate these effects, cascade transistors are employed.

A similar second stage provides additional gain g_{m2}/g_{m2L}. In this case, the input is a current-reuse stage without cascoding for simplicity. Again, a tail current dependent on V_{TGC} is used to obtain the overall desired variable gain. Each stage has its own common-mode feedback circuit (CMFB) to maintain a proper DC biasing point.

4.4.3 Transconductance-Control Circuit

The circuit that generates the bias currents for the loop amplifier as a function of V_{TGC} is shown in Figure 4.12. A current steering mechanism similar to that used in the Gain-Control Circuit (Figure 4.9) is employed, in which V_{TGC} is compared to reference voltages by means of differential pairs. For each stage of the loop amplifier, three PMOS differential pairs are

used of which the tail currents add to the bias current when V_{TGC} drops below the respective reference voltage. The tail current levels and reference voltage levels (derived from the resistive divider shown in Figure 4.9) have been chosen based on simulation to obtain a near-constant closed-loop bandwidth and sufficient phase margin.

4.5 Experimental Results

4.5.1 Experimental Prototype

The ASIC has been fabricated in 0.18 µm HV BCDMOS process. The ASIC consists of 64 RX and TX channels, each of which interfaces with one element of a 64-element CMUT transducer array. Each RX channel consists of the proposed TIA and a cable driver [41], and is powered by a ±0.9 V analog supply and a 1.8 V logic supply. Each TX channel has a programmable high-voltage (HV) pulser to generate pulses with a maximum amplitude of ±30 V, and a HV transmit/receive (T/R) switch to protect the low-voltage RX circuits during pulse transmission. Details of the TX-channel circuitry have been reported in [42]. The channels are arranged in two rows with 32 blocks in each row. This arrangement enables direct pitch-matched connection to the 64-element CMUT transducer array. Figure 4.13 shows a photograph of the chip. The proposed TIA occupies an area of 0.12 mm^2.

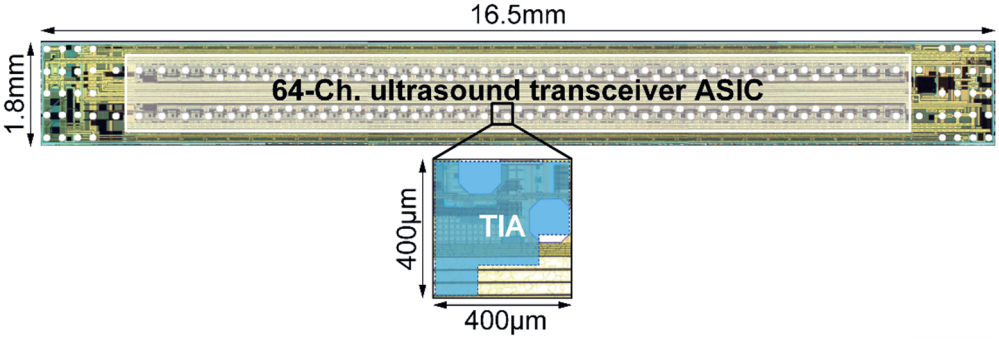
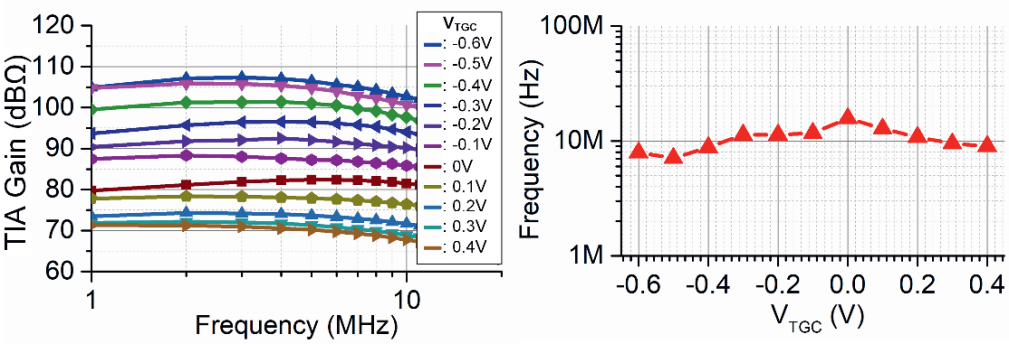


Figure 4.13 Chip micrograph of the 64-channel transceiver ASIC, with inset showing the element-level TIA.

4.5.2 Electrical Characterization Results

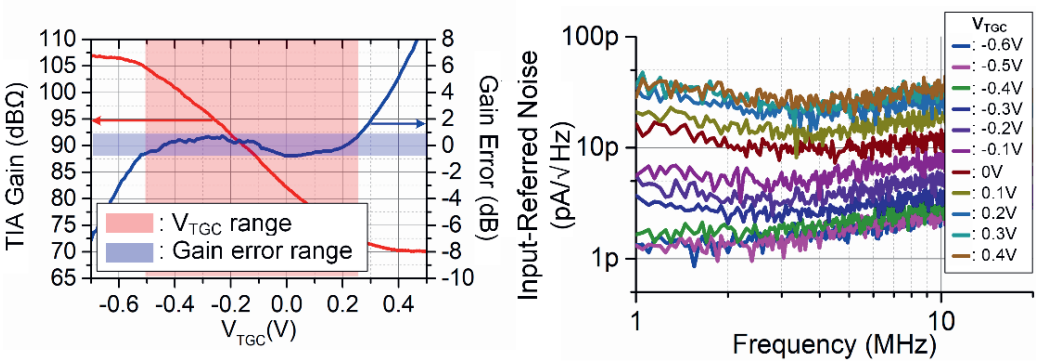
To measure the TIA's transfer function, an input current was generated by applying a voltage signal to a 15 pF off-chip capacitor, which mimics the CMUT capacitance, connected to the TIA's input. Figure 4.14(a) shows the measured transfer function over the whole gain range. As shown in Figure 4.14(b), the -3 dB bandwidth varies between 7.1 MHz and 15.7 MHz across the gain range. Compared to the gain variation of almost 40 dB, the bandwidth is

kept relatively constant, in good agreement with the designed adaptive gain operation of the loop amplifier.



(a) (b)

Figure 4.14 (a) Measured transfer function, and (b) corresponding -3dB bandwidth as a function of V_{TGC}.

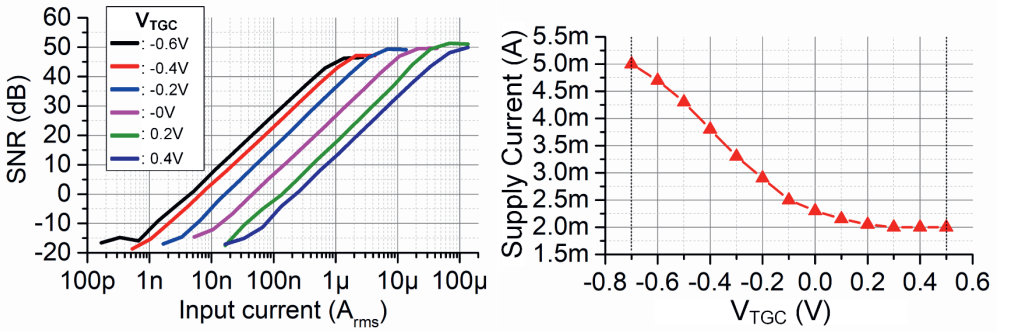


(a) (b)

Figure 4.15 (a) Measured gain at 5 MHz as a function of V_{TGC}, with the associated error compared to a linear-in-dB curve; (b) input-referred noise spectrum

Figure 4.15(a) shows the TIA gain at 5 MHz as a function of the TGC control voltage (V_{TGC}). Note that, as expected, the gain decreases with increasing values of V_{TGC}, which in combination with a V_{TGC} that decreases with time leads to the desired gain that increases with time. The TIA gain can be varied continuously across a 37 dB range. The corresponding gain error with respect to an ideal linear-in-dB curve is less than ±1 dB across the middle 33 dB of the gain range.

The input-referred noise of the TIA was determined by connecting the same off-chip capacitor at the input of the TIA, measuring the output noise, and dividing it by the measured transfer function. The resulting input-referred noise spectra for different values of V_{TGC} are shown in Figure 4.15(b). The noise floor is 1.7 pA/√Hz at 5 MHz at the highest gain, which is comparable to the CMUT noise floor. The measured spectra also demonstrate that the noise floor increases for lower TIA gains, as expected due to the adaptive biasing of the loop amplifier. At the lowest gain, the noise floor is about 30 pA/√Hz at 5 MHz. This increase of about 25 dB is less than the expected increase in the signal level of about 40 dB. Therefore, the signal-to-noise ratio (SNR) is not degraded by this gain-dependent noise floor.



(a) (b)

Figure 4.16 (a) Measured SNR as a function the signal amplitude for different values of V_{TGC}; (b) measured supply current as a function of V_{TGC}.

This is confirmed by the DR measurement shown in Figure 4.16(a), which shows the measured output SNR as a function of the input signal current for different values of V_{TGC}. The overall input DR, defined as the ratio between the input level at which

1 dB compression occurs at the lowest gain and the input level at which the SNR reaches zero at the highest gain, amounts to 82 dB. The variable gain reduces this to 46 dB at the output.

As expected, due to the adaptive biasing, the TIA supply current also changes in a gain-dependent manner, as shown in Figure 4.16(b). Assuming a linear variation of V_{TGC} as a function of time to cover the gain range, the variable supply current leads to an average power consumption of 5.2 mW.

Figure 4.17 shows the measured transient behavior of the continuous TGC operation. A continuous sinusoidal input current with a frequency of 7 MHz and an exponentially decreasing amplitude, and a corresponding ramp signal are applied to the TIA's input and the gain-control port, respectively. The measured output has an approximately constant and smoothly-compensated output swing. The gain error extracted from the output amplitude

variation is less than ± 1 dB, demonstrating the intended continuous linear-in-dB TGC operation.

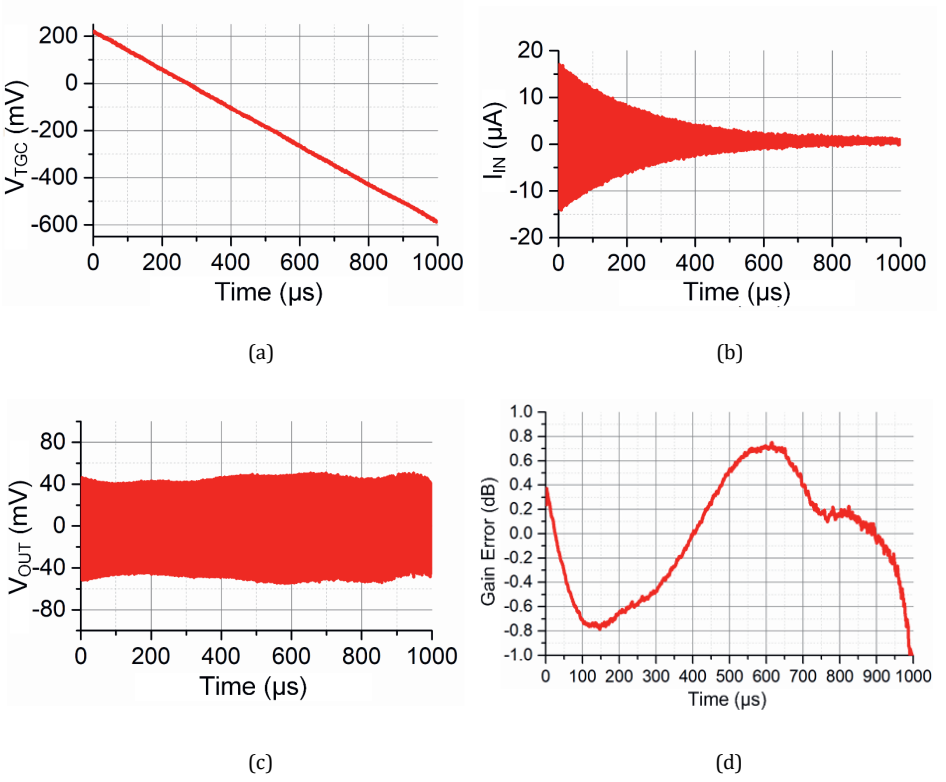


Figure 4.17 Measured transient TGC operation: (a) applied TGC control voltage; (b) applied exponentially decreasing input signal; (c) measured output signal; (d) corresponding error with respect to a linear-in-dB gain curve.

4.5.3 Acoustical Experiments

Figure 4.18(a) shows a fabricated prototype in which the ASIC and CMUT have been flip-chip bonded on a Flexible Printed Circuit Board (flex PCB). Each TX/RX channel on the ASIC directly interfaces with a CMUT element. The TIA outputs, buffered by the cable drivers, go to a Verasonics imaging system (Verasonics Inc., Redmond, WA) [43] to record the received echo signals. The flex PBC also connects the power supplies, with local decoupling capacitors, to the ASIC, as well as digital control signals, which are provided by an FPGA.

The test-bench for imaging experiments is shown in Figure 4.18(b). The implemented prototype is placed at the surface of a tissue-mimicking phantom (GAMMEX SONO404) with

an attenuation coefficient of 0.5 dB/cm/MHz. The phantom contains nylon wires acting as point reflectors and grey-scale targets to evaluate the SNR in the image.

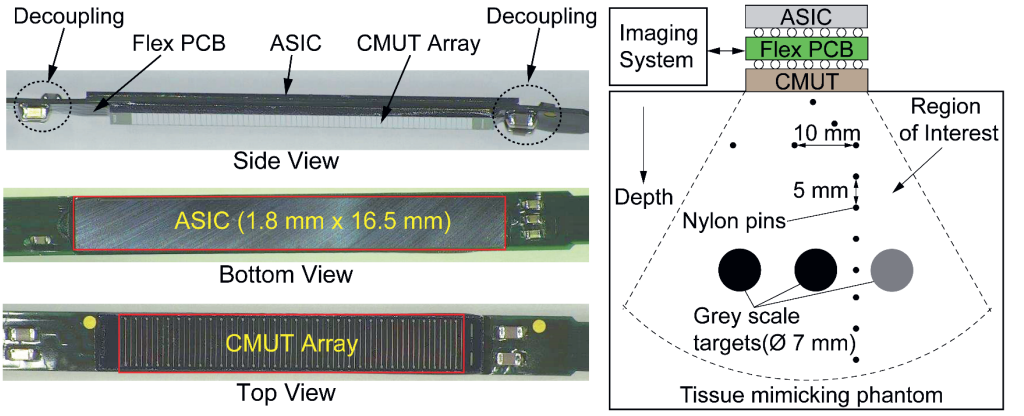


Figure 4.18 (a) Implemented prototype; (b) overview of the measurement setup used for acoustic characterization.

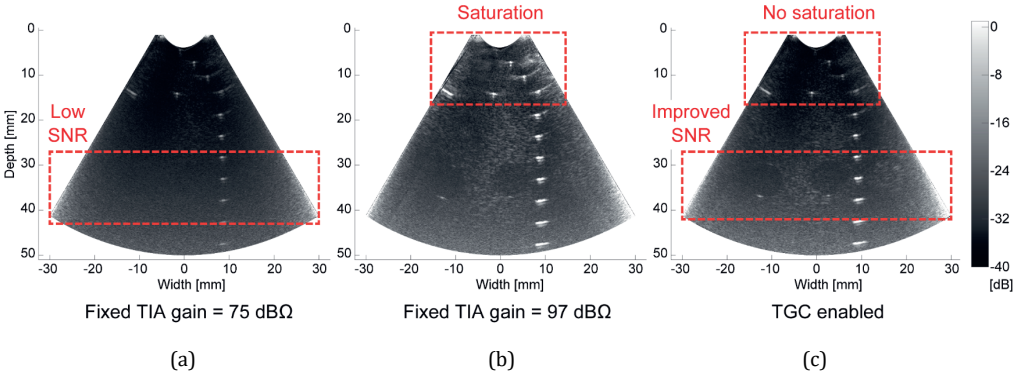


Figure 4.19 Phased-array B-Mode images with a ±45° opening angle, obtained with (a) fixed low gain, (b) fixed high gain, (c) the proposed continuous TGC operation.

Figure 4.19 shows ±45° phased-array B-mode images of the phantom with 64-channel TX and RX operation. Figure 4.19(a) is obtained using a fixed TIA gain of 75 dBΩ. As this gain is optimized for the near field, the circular grey-scale targets at larger depth are hardly distinguishable. When the gain is fixed at a higher value of 97 dBΩ to improve SNR at larger depth (Figure 4.19(b)), the RX signal at the shallow depths suffers from saturation, leading to a too bright image. With continuous TGC, these issues are mitigated, leading to a higher-quality image in which no saturation occurs and the grey-scale targets can be clearly

distinguished from the surrounding speckle pattern (Figure 4.19(c)). This imaging experiment successfully demonstrates the continuous TGC capability of the prototype.

TABLE 4-1 PERFORMANCE SUMMARY AND COMPARISON

	This work	[22]	[46]	[47]	[48]	AD8332 [44]	VCA2617 [45]
Process	0.18 μm HV BCDMOS	0.18 μm HV BCDMOS	0.18 μm HV CMOS	0.35 um CMOS	BCD-SOI	-	-
-3dB BW	7MHz	16MHz	10MHz	40MHz	11MHz	100MHz	50MHz
LNA type	TIA	TIA	TIA	TIA	TIA	Voltage amp	Voltage amp
Max gain	107dBΩ	119dBΩ	116dBΩ	106dBΩ	78.4dBΩ	68.5dB	38dB
Full gain range	37dB	12dB	12dB	0dB	0dB	48dB	48dB
Gain error(1) (gain range)	± 1dB (33dB)	± 3dB(2) (12dB)	± 3dB(2) (12dB)	-	-	± 0.3dB (42dB)	± 0.9dB (37dB)
Gain control	Continuous	Discrete	Discrete	Fixed gain	Fixed gain	Continuous	Continuous
Transducer capacitance	15pF	0.7pF	2 pF	0.09pF	9.2pF	-	-
Input referred noise	1.7pA/√Hz @5MHz	2.0pA/√Hz @13MHz	0.41pA/√Hz @ 5MHz	0.31 pA/√Hz @ 20MHz	5.1pA/√Hz @10MHz	0.74 nV/√Hz @5MHz	4.1nV/√Hz @5MHz
Power consumption	5.2mW	0.42mW	1.4mW	0.8mW	1mW	138mW	52mW
NEF'(3)	0.78(4)	1.23(4)	2.7	-	0.55	-	-

(1) Maximum deviation from the ideal linear-in-dB curve across the mentioned gain range
(2) Estimated from the discrete gain step
(3) NEF' = $p_{n,in}\cdot\sqrt{Power_{tot}}$ [mP·√(mW/Hz)] [46] where $p_{n,in}$ is the input-referred acoustic pressure noise spectral density averaged inside the passband
(4) Calculated by referring the measured noise to an equivalent pressure noise using the estimated transducer sensitivity

TABLE 4-1 compares the proposed TIA with the prior art. Compared to commercial LNAs with continuous TGC function [44], [45], >10× lower power consumption is achieved. While some of this difference may be attributed to the proposed circuit architecture, it should be noted that these parts have quite different noise and bandwidth specifications, and are not intended for in-probe integration. Compared to prior in-probe TIAs, which employ discrete

steps or fixed gain [22], [44]–[48], comparable performance is obtained, but with much wider gain range and without the imaging artefacts associated with gain switching.

4.6 Conclusion

This chapter has presented a low-noise TIA with continuous TGC for ultrasound imaging applications. The TIA employs a capacitive ladder feedback network and interpolation by means of current steering to provide linear-in-dB gain control. The proposed architecture combines LNA and TGC functionality in a single feedback loop, leading to better power efficiency than solutions that employ a fixed-gain LNA followed by a TGC stage, in which the LNA needs to be able to handle the full input DR at its output. In order to accommodate the large variation in the feedback factor, a current-reuse loop amplifier with adaptive biasing has been introduced, which provides approximately constant closed-loop bandwidth and saves power by allowing higher input noise at the lower part of the gain range.

Compared to prior in-probe TIAs, which employ discrete steps or fixed gain, competitive noise efficiency and a wider gain range are obtained without gain-switching transients. The presented electrical measurements demonstrate continuous gain control that is linear-in-dB to within ±1 dB. Imaging results obtained in combination with a 64-element CMUT transducer show reduced imaging artefacts and highlight that the presented topology is a promising solution for future in-probe ultrasound ASICs.

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Chapter 5

Conclusions

This chapter summarizes the original contributions and the main findings of this thesis. It also discusses opportunities for future work.

5.1 Main Contributions

- Implementation of an ultrasound transceiver for carotid artery imaging (Chapter 2).

  This design has demonstrated an ultrasound transceiver ASIC designed for 3-D ultrasonic imaging of the carotid artery. The proposed ASIC interfaces a piezo-electric transducer array of 24 × 40 elements, directly integrated on top of the ASIC, to an imaging system. The ASIC consists of row-level TX and RX circuits and a reconfigurable switch matrix. The row-level architecture uses only 24 channels for each TX and RX circuits. The reconfigurability enables tiling of multiple ASICs to form an even bigger array. Electrical and acoustic experiments have successfully demonstrated the functionality of the ASIC. Besides, the ASIC has been successfully used in a 3-D imaging experiment.

- Realization of a programmable high-voltage bipolar transmitter with embedded transmit/receive switches (Chapter 3).

  This design has demonstrated a fully-integrated 64-channel programmable ultrasound transmit beamformer for catheter-based ultrasound probes. The proposed design consists of pulsers that have a compact back-to-back isolating HV switch topology with only one HV transistor. Moreover, the embedded T/R switch architecture achieves further layout area reduction. Acoustic results obtained in combination with a 64-

element CMUT array demonstrate the ability to generate steered and focused acoustic beams.

- Implementation of a transimpedance amplifier for ultrasound front-end with continuous time-gain compensation (Chapter 4).

  This design has demonstrated a low-noise transimpedance amplifier (TIA) designed for miniature ultrasound probes. It provides continuously variable gain to compensate for the time-dependent attenuation of the received echo signal. Embedding the TGC function in the TIA reduces the output DR, saving power compared to prior solutions. The TIA employs a capacitive ladder feedback network and a current-steering circuit to obtain a linear-in-dB gain range of 37 dB. In addition, a variable-gain loop amplifier based on current-reuse stages maintains constant bandwidth in a power-efficient manner. It achieves a gain error below ±1dB and a 1.7pA/√Hz noise floor and consumes 5.2mW from a ±0.9V supply. B-mode images of a tissue-mimicking phantom have been presented that show the benefits of the TGC scheme.

5.2 Main Findings

- System-level
  - A row-parallel architecture can be used to address the interconnection challenges associated with a 2-D ultrasound transducer. The proposed architecture interfaces a 2-D transducer array to a conventional imaging system by making the array appear like a linear array that can be electronically translated in the elevation direction. Although it supports fewer options for transducer connections than row-column architectures [1], it allows for more compact circuit implementation and seamless tiling of multiple ASICs to realize large-aperture arrays. This is particularly important to implement a probe with several thousands of transducer elements (Chapter 2).

  - Tiling enables the realization of large matrix transducer arrays with smaller ASIC modules, offering a better trade-off in terms of cost and yield compared to a single ASIC covering the full array. It also provides flexibility for the area of the transducer array by adjusting the number of tiling ASICs (Chapter 2).

  - Reconfigurability allows the transducer array to perform different functions to support different imaging schemes. When it is implemented with a tiled transducer, reconfigurability can help to make the set of tiled appear seamlessly as one large-aperture array (Chapter 2).

- An in-probe ASIC can be used to mitigate the signal loss due to parasitic loading of a transducer element by a cable by sensing the element's signal with an amplifier with an appropriate input impedance and driving the cable with an appropriate output impedance. Thus, an in-probe ASIC can help to fully utilize the performance of the transducer (Chapter 2, 4).

- Circuit-level
  - Embedding T/R switching functionality into the design of a HV pulser can reduce the die area associated with HV TX circuitry (Chapter 3). The HV pulser with embedded T/R switching presented in Chapter 3 exploits the existing HV transistors of the pulser for the T/R switch implementation. Thus, it reduces area for the HV T/R switch, which is especially relevant in pitch-matched designs interfacing with small transducer elements.

  - Integrating the TGC function into the LNA helps to improve power efficiency compared to the conventional solution of a fixed-gain LNA followed by a TGC amplifier. The proposed circuit reduces power consumption by eliminating a power-hungry LNA to handle the full DR of the echo signal at its. In addition, the use of a capacitive feedback network provides the required gain range without additional noise contribution.

  - Adaptive biasing of the LNA is an effective and efficient approach to reduce average power consumption while maintaining sufficient signal-to-noise ratio in ultrasound receive circuits (Chapter 4).

  - The use of an LNA with a current-reuse input stage helps to reduce the power consumption needed to meet a given noise requirement compared to conventional amplifier topologies based on an input stage employing a single differential pair (Chapter 4).

  - Besides designing the core amplifier for TGC, the design of auxiliary circuitry, such as voltage reference, current steering, and bias adjusting circuitry, is also essential to maintain the stability and noise requirement over the whole gain range (Chapter 4).

5.3 Future Work

- Incorporation of an advanced HV process to simplify and improve TX circuits

The HV TX circuits presented in this thesis, i.e., the HV switch in Chapter 2 and the HV pulser in Chapter 3, have been implemented in a junction-isolated HV technology. The constraints of this technology lead to relatively large circuits, due to the lateral spacing required for the isolation junctions. Moreover, relatively complex circuits are required, such as the bootstrap circuit presented in Chapter 2 that works around the fact that the technology does not offer a HV diode that is allowed to be forward biased. By using a more advanced silicon-on-insulator (SOI) technology, the lateral spacing between the HV device can be reduced by using oxide isolation, and a simpler and more compact bootstrap circuit can be implemented with an oxide-isolated HV diode. Thus, the area required for HV switches or pulsers could be reduced. Depending on the application, the reduced area could be used for implementing advanced control circuits, or a smaller on-resistance could be realized within the same area, or transducers with a smaller pitch could be accommodated.

- Further cable-count reduction with on-chip ADCs

  While the row-parallel architecture already reduces the required channel count, further reduction could be achieved with additional circuit design. As the proposed ASICs transfer analog RX signals, the time-multiplexing [2]–[5] of the received signals in the analog domain can readily be adopted. This technique merges multiple RX channels onto a single cable and thus reduces cable count. One issue with the approach is that it is sensitive to cross-talk between the channels. To implement more advanced cable-count reduction, in-probe digitization can be adopted [6]–[9]. This can support various digital data compression techniques in the probe, which will achieve further cable count reduction. Moreover, it takes away the need for ADC on the system side, making a step towards probes with a fully-digital interface.

- Incorporation of integrated power converters to reduce the complexity of power supplies

  The implemented ASICs are powered through direct cable connections to the external system. However, this comes at the cost of using a dedicated cable for each supply. The design presented in Chapter 4, for instance, requires about ten cables for the supply which is about 12% of the total cable count [10]. In [11], a similar fraction of the cables are used for power supply. This fraction will increase when cable-count reduction techniques are applied to reduce the number of signal cables, making it worthwhile to also invest in reducing the number of power-supply cables. Integrated power converters could generate multiple supplies from a single external supply line. Thus, it reduces the cable count for the supply lines. Recent publications [12], [13] demonstrate the feasibility of supplying power to TX circuits by means of integrated DC-DC converters. If RX circuits are also powered using integrated converters, care

must be taken to prevent unwanted interference (e.g., switching noise) from the converters.

- Ultrasound ASIC for wearable devices

  Currently, ultrasound imaging is almost exclusively available in hospitals. Continuous monitoring using ultrasound would extremely valuable for monitoring or prevention. Wearable devices offer a convenient means of monitoring real-time health parameters of a patient. Ultrasound patches with stretchable transducers arrays [14]–[16] have demonstrated the feasibility of implementing wearable devices for ultrasound imaging. However, the existing approaches only focus on the transducer implementation. Therefore, it is an open question on how to build a wearable ultrasound probe with the required control, interface, and power supply electronics. In [13], a TX-oriented ultrasound ASIC has been reported for a portable ultrasound imager. This work used external amplifiers and ADCs for the RX chain. Hence, the device is still bulky and suffers from non-optimized power consumption. A fully-integrated ultrasound transceiver for a wearable ultrasound device is a promising approach to obtain low-power consumption, small form-factor, and optimized control schemes.

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Summary

This thesis describes the design and realization of integrated ultrasound transceivers for carotid artery imaging and intracardiac echocardiography (ICE). The goal of this work is to investigate system- and circuit-level techniques to address requirements and implementation bottlenecks in these applications. Prototype chips are presented to demonstrate the effective of these techniques. The first prototype provides cable-count reduction and the capability to interface with a large-aperture transducer array for 3D carotid artery imaging. The second prototype is targeted at a 2D ICE probe, and features a novel bipolar high-voltage (HV) pulser, and an analog front-end with continuous time-gain compensation while achieving a superior noise efficiency factor.

Chapter 1

Chapter 1 introduces the motivation of this thesis work and the background of the target applications. Then, a review of the prior art is presented for both target applications. The review reveals that integrated in-probe transceivers have unique advantages to implement probes for these applications. 3-D ultrasound imaging of the carotid artery requires a large-aperture transducer array with thousands of small transducer elements. This makes direct cable connections to an imaging system impractical due to the high cable count and SNR loss from the cable loading. Integrating ASICs in the probe is a promising approach to address these issues. ICE probes also benefit from in-probe ASICs to get SNR improvement within the stringent form factor and power constraints of an imaging catheter.

Chapter 2

In chapter 2, an ultrasound transceiver ASIC designed for 3-D ultrasonic imaging of the carotid artery is presented. This application calls for an array of thousands of ultrasonic transducer elements, far exceeding the number of channels of conventional imaging systems. The 3.6 × 6.8 mm^2 ASIC interfaces a piezo-electric transducer array of 24 × 40 elements, directly integrated on top of the ASIC, to an imaging system using only 24 transmit and receive channels. Multiple ASICs can be tiled together to form an even bigger array. The ASIC,

implemented in a 0.18 μm high-voltage BCDMOS process, consists of a reconfigurable switch matrix and row-level receive circuits. Each element is associated with a compact bootstrapped high-voltage transmit switch, an isolation switch for the receive circuits, and programmable logic that enables a variety of imaging modes. Electrical and acoustic experiments demonstrate the functionality of the ASIC. In addition, the ASIC has been successfully used in a 3-D imaging experiment.

Chapter 3

Chapter 3 presents a fully-integrated 64-channel programmable ultrasound transmit beamformer for ICE probes, designed to interface with a capacitive micro-machined ultrasound transducer (CMUT) array. The chip is equipped with programmable HV pulsers that can generate ±30 V return-to-zero (RZ) and non-return-to-zero pulses. The pulsers employ a compact back-to-back isolating HV switch topology that employs HV floating-gate drivers with only one HV MOS transistor each. Further die-size reduction is achieved by using the RZ switches also as the transmit/receive (T/R) switch needed to pass received echo signals to low-voltage receive circuitry. On-chip digital logic clocked at 200 MHz allows the pulse timing to be programmed with a resolution of 5 ns while supporting pulses of 1 cycle up to 63 cycles. The chip has been implemented in 0.18 μm HV BCDMOS technology and occupies an area of 1.8 mm x 16.5 mm, suitable for integration into an 8 F catheter. Each pulser with embedded T/R switch and digital logic occupies only 0.167 mm^2. The pulser successfully drives an 18-pF transducer capacitance at pulse frequencies up to 9 MHz. The T/R switch has a measured on-resistance of ∼180 Ω. Acoustic results obtained in combination with a 7.5-MHz 64-element CMUT array demonstrate the ability to generate steered and focused acoustic beams.

Chapter 4

Chapter 4 presents a low-noise transimpedance amplifier (TIA) designed for the same CMUT-based ICE probe. It provides variable gain to compensate for the time-dependent attenuation of the received echo signal. The presented time-gain compensation (TGC) continuously compresses the echo-signal dynamic range while avoiding imaging artefacts associated with discrete gain steps. Embedding the TGC function in the TIA reduces the output dynamic range, saving power compared to prior solutions that apply TGC after the low-noise amplifier. The TIA employs a capacitive ladder feedback network and a current-steering circuit to obtain linear-in-dB continuous gain control with a gain range of 37 dB. A variable-gain loop amplifier based on current-reuse stages maintains constant bandwidth in a power-efficient manner. The TIA has been integrated together with the transmit beamformer presented in Chapter 3 in a 64-channel ultrasound transceiver ASIC in a 0.18 μm BCDMOS process and occupies a die area of 0.12 mm^2. It achieves a gain error below ±1 dB and a 1.7 pA/ √Hz noise floor and consumes 5.2 mW from a ±0.9 V supply. B-mode images of a tissue-mimicking phantom are presented that show the benefits of the TGC scheme.

Chapter 5

Chapter 5 summarizes the original contributions of this thesis and discusses the main findings at both system-level and circuit-level. For application in carotid artery imaging, a transceiver architecture has been presented that provides a solution for the interface challenges associated with a large transducer arrays. For the ICE application, a compact HV TX structure and a low noise RX AFE with continuous TGC have been presented that are compatible in terms of size and power with catheter-based application. Suggestions for future work are also provided: further cable-count reduction with on-chip ADCs and integrated power converters; adoption of an advanced HV process to simplify and improve TX circuitry; and investigation of ultrasound ASICs for wearable devices.

Samenvatting

Dit proefschrift beschrijft het ontwerp en de realisatie van geïntegreerde ultrasone transceivers voor beeldvorming van de halsslagader en intracardiale echocardiografie (ICE). Het doel van dit werk is om technieken op systeem- en circuitniveau te onderzoeken om de eisen en implementatieknelpunten van deze toepassingen aan te pakken. Chip-prototypes worden gepresenteerd om de effectiviteit van deze technieken te demonstreren. Het eerste prototype zorgt voor een vermindering van het aantal kabels en de mogelijkheid om een array van transducenten met een grote apertuur voor beeldvorming van de halsslagader te verbinden met een imaging systeem. Het tweede prototype is gericht op ICE-probes en brengt een nieuwe, bipolaire hoogspanningspulser en een analoog front-end met time-gain compensatie terwijl een superieure ruisefficiëntiefactor wordt bereikt.

Hoofdstuk 1

Hoofdstuk 1 introduceert de motivatie van dit proefschrift en de achtergrond van de beoogde toepassingen. Vervolgens wordt een overzicht van de stand van de techniek gepresenteerd voor beide beoogde toepassingen. Uit dit overzicht blijkt dat een geïntegreerde transceiver in de probe unieke voordelen heeft om probes voor deze toepassingen te implementeren. 3D-echografie van de halsslagader vraagt om een transducer met een grote apertuur, bestaande uit duizenden kleine elementen. Dit maakt directe kabelverbindingen met een imaging systeem onpraktisch, vanwege het grote aantal kabels en het verlies in signaal-ruis-verhouding door de kabelbelasting. Het integreren van chips (ASIC's) in de probe is een veelbelovende benadering om deze zaken aan te pakken. ICE probes hebben ook baat bij in-probe ASIC's om de signaal-ruis-verhouding te verbeteren, binnen de strikte afmetingen- en vermogensbeperkingen van een imaging katheter.

Hoofdstuk 2

In hoofdstuk 2 wordt een ultrasone transceiver ASIC gepresenteerd, ontworpen voor 3D ultrasone beeldvorming van de halsslagader. Deze toepassing vraagt om een array van duizenden ultrasone transducerelementen, veel meer dan het aantal kanalen van conventionele imaging systemen. De ASIC van 3,6 × 6,8 mm^2 koppelt een piëzo-elektrische transducerarray van 24 × 40 elementen, direct geïntegreerd bovenop de ASIC, aan een beeldvormingssysteem dat slechts 24 zend- en ontvangstkanalen gebruikt. Meerdere ASIC's kunnen worden samengevoegd om een nog grotere array te vormen. De ASIC,

geïmplementeerd in een 0,18 µm BCDMOS-proces dat hoge voltages (HV) ondersteunt, bestaat uit een herconfigureerbare schakelmatrix en ontvangstcircuits op rijniveau. Elk element is gekoppeld aan een compacte bootstrap HV-zendschakelaar, een isolatieschakelaar voor de ontvangstcircuits en programmeerbare logica die een verscheidenheid aan beeldvormingsmodi mogelijk maakt. Elektrische en akoestische experimenten demonstreren de functionaliteit van de ASIC. Bovendien is de ASIC met succes gebruikt in een 3D-imagingexperiment.

Hoofdstuk 3

Hoofdstuk 3 presenteert een volledig geïntegreerde 64-kanaals programmeerbare ultrasone zendbundelvormer voor ICE-probes, ontworpen om te communiceren met een capacitieve micro-machined ultrasound transducer (CMUT)-array. De chip is uitgerust met programmeerbare HV-pulsers die ±30 V return-to-zero (RZ) en non-return-to-zero pulsen kunnen genereren. De pulsers maken gebruik van een compacte back-to-back isolerende HV-schakelaartopologie die floating-gate drivers gebruikt met elk slechts één HV MOS-transistor. Verdere reductie van het benodigd chipoppervlak wordt bereikt door de RZ-schakelaars ook te gebruiken als zend/ontvangst (T/R) schakelaar die nodig is om ontvangen echosignalen door te geven aan laagspannings-ontvangstcircuits. Digitale logica op de chip, geklokt op 200 MHz, maakt het mogelijk om de pulstiming te programmeren met een resolutie van 5 ns, terwijl pulsen van 1 tot 63 cycli worden ondersteund. De chip is geïmplementeerd in 0,18 µm HV BCDMOS-technologie en beslaat een oppervlakte van 1,8 mm x 16,5 mm, geschikt voor integratie in een 8 F-katheter. Elke pulser met ingebouwde T/R-schakelaar en digitale logica neemt slechts 0,167 mm^2 in beslag. De pulser stuurt met succes een 18 pF transducercapaciteit aan bij pulsfrequenties tot 9 MHz. De T/R-schakelaar heeft een gemeten aan-weerstand van ca. 180 Ohm. Akoestische resultaten verkregen in combinatie met een 7,5 MHz 64-elements CMUT-array demonstreren het vermogen om gestuurde en gefocusseerde akoestische bundels te genereren.

Hoofdstuk 4

Hoofdstuk 4 presenteert een ruisarme transimpedantieversterker (TIA) ontworpen voor dezelfde CMUT-gebaseerde ICE probe. Deze versterker biedt een variabele versterkingsfactor om de tijdafhankelijke verzwakking van het ontvangen echosignaal te compenseren. De gepresenteerde tijd-versterkingscompensatie (time-gain compensation, TGC) comprimeert continu het dynamische bereik van het echosignaal en vermijdt beeldartefacten die gepaard gaan met discrete versterkingsstappen. Door de TGC-functie in de TIA in te bedden, wordt het dynamische uitgangsbereik verminderd, waardoor energie wordt bespaard in vergelijking met eerdere oplossingen die TGC toepassen na de ruisarme versterker. De TIA maakt gebruik van een capacitief ladder-terugkoppelnetwerk en een stroomstuurcircuit om een continue lineair-in-dB versterkingsregeling te verkrijgen met een versterkingsbereik van 37 dB. Een lusversterker met variabele versterking op basis van

current-reuse trappen handhaaft een constante bandbreedte op een energiezuinige manier. De TIA is geïntegreerd, in combinatie met de programmeerbare zendbundelvormer uit hoofdstuk 4, in een 64-kanaals ultrasone transceiver ASIC in een 0,18 µm BCDMOS-proces en beslaat een chipoppervlak van 0,12 mm^2. De versterker bereikt een versterkingsfout van minder dan ±1 dB en een ruisvloer van 1,7 $pA/\sqrt{Hz}$ en verbruikt 5,2 mW van een voeding van ±0,9 V. B-mode beelden van een weefsel-nabootsend fantoom worden gepresenteerd die de voordelen van het TGC-schema laten zien.

Hoofdstuk 5

Hoofdstuk 5 vat de oorspronkelijke bijdragen van dit proefschrift samen en bespreekt de belangrijkste bevindingen op zowel systeem- als circuitniveau. Voor toepassing in beeldvorming van de halsslagader is een transceiver-architectuur gepresenteerd die een oplossing biedt voor de interface-uitdagingen van grote transducerarrays. Voor de ICE-toepassing is een compacte HV TX-structuur en een geluidsarme RX analoog front-end met continue TGC gepresenteerd die geschikt zijn voor toepassing in een katheter in termen van hun afmetingen en vermogensverbruik. Er worden ook suggesties gegeven voor toekomstig werk: verdere vermindering van het aantal kabels met on-chip ADC's en geïntegreerde vermogensomvormers; gebruik van een geavanceerd HV-proces om TX-circuits te vereenvoudigen en te verbeteren; en onderzoek van ultrasone ASIC's voor apparaten die op het lichaam gedragen kunnen worden.

List of Publications

Journal Articles

E. Kang, M. Tan, J. An, Z. Chang, P. Vince, N. Sénégond, T. Mateo, C. Meynier, and M. A. P. Pertijs, "A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 12, pp. 3157-3168, Dec. 2020.

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