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Integrated Power Flow Control and Short Circuit Protection

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Low-voltage direct current (LVdc) systems are a promising technology for systems with a high penetration of renewable sources and storage that operate with bidirectional power flow. In this article, a fundamental building block for LVdc is presented for different applications, such as charge controllers, voltage regulation in street-lighting systems, and current limiters in meshed dc grids. The developed building block integrates a solid-state circuit breaker (SSCB) and partially rated power flow control converter (PFCC) capable of achieving the given control objectives with extremely high system efficiency and full short circuit protection.

Overview

LVdc systems were the pioneer systems providing public lighting based on Edison's incandescent electric light. They were more efficient than the first single-phase ac systems. However, they were soon outperformed by Tesla's polyphase ac systems. While, in 1887 in United States, there were five times more LVdc than ac central stations for light, in 1890, there were 30% more ac central stations [1]. The efficiency and ability of ac systems outweighed any concerns about ac safety, which were especially amplified by Edison to help the commercial growth of his systems. Already at the end of 19th century, it was clear that, without a device to arbitrarily control the voltage level, LVdc systems could not outperform ac polyphase systems.

Power electronics in the past two decades brought forth significant changes to electric power distribution. Primarily, the rise in the energy and cost efficiency

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of power electronics contributed to the increase of devices that internally utilize dc, and this trend is expected to continue. The increased economic competitiveness of renewable energy sources (RESs), such as photovoltaics (PVs), led to the extensive use of these sources. PVs and other RESs either internally produce dc or are using power electronic converters (PECs) to control their power output, which has an internal dc link. Moreover, the emergence of prosumers and energy storage is fundamentally reshaping the landscape of both electric energy production and distribution. Under the new conditions, LVdc became a viable option in many energy distribution markets.

In this article, firstly, the benefits and opportunities of using LVdc in secondary and tertiary energy distribution system are presented (Figure 1). The LVdc systems considered have bus voltages up to 1.5 kV and operating currents up to several hundred amperes. A survey of pilot projects implementing these systems and their potential markets is provided to better demonstrate the LVdc potential.

To work with well-defined interfaces, the concept of building blocks is introduced. A building block is a well-defined functionality block that is well recognizable by domain experts. It evolves with the technology and standards, and it can be assembled from other building blocks; it may be a subassembly of other building blocks and is reusable as well as replaceable.

Two types of building blocks can be distinguished—system building blocks (SBBs) and function building blocks (FBBs). SBBs are the highest level of abstraction; they define what function will be implemented and specify the power and communication interface as well as the market requirements. FBBs, on the other hand, define how the functions are implemented. That means which technologies and components will implement the functionality of an SBB.

Then, an integrated SBB for LVdc systems is presented with a simple equivalent model. Three of the surveyed markets are chosen as case studies to demonstrate the potential benefits of the proposed building block: streetlight, battery charging, and meshed power distribution systems. The article closes with an experimental section that validates the steady-state operation of the proposed SBB. Moreover, the ability of the building block to withstand bolted short circuits on its terminals is experimentally validated.

LVdc Promise and Outlook

Enabling Benefits in Energy Distribution Technologies

Several modeling- and demonstration-based studies show potential energy savings when LVdc is adopted instead of LVac [3]–[6]. For example, one of the studies in [3] identifies that an energy storage system (ESS) has a strong influence on improving the efficiency in the range of 2–18% and correlates this tendency with the power mismatch between RESs and the load profile. The discussion highlights that this advantage of LVdc systems in residential and commercial buildings correlates with a minimization of the energy exchange with the ac grid that is interfaced using an active front-end converter.

While operational costs can be reduced by increasing the size of the ESS, the achieved gain in tradeoff with the initial costs of the infrastructure is relevant. This includes the storage element as well as the PEC that interfaces the ESS with the LVdc system. This article suggests a promising method to downsize the interfacing PEC for the given rated power.

A strong dependence arises from the assumed component efficiencies, which usually increase directly in relation to the power rating (P_{rated}) [7], [8]. For

instance, it is reported in [8] that a converter with $P_{\text{rated}} < 1$ kW has an average efficiency $\eta_{\text{ave}} \approx 90\%$; for converters with a power rating between 1 and 5 kW, the average efficiencies are $\approx 97.5\%$.

The converter efficiencies are also dependent on the operating conditions, such as unbalanced load conditions, the chosen voltage level, and the system configuration [7], [9]. The dc nature of key components in ESSs and RESs offers an advantage if LVdc is used instead of LVac as the integrating technology. In this article, the PEC component rating is dissociated from the actual system size such that it is a small fraction of the actual processed power, thus shifting the associated benefits further to the side of LVdc.

However, at the early stage of LVdc adaptation, the up-front cost is increased due to a lack of economies of scale and the specific protection requirements of LVdc [8], [10]. A significant advantage that is often discussed in the literature is the ability of dc technologies to work synergistically within the existing ac distribution infrastructure. Such LVdc systems are decoupled from the ac grid, and, thus, they are relatively isolated from the effects of voltage sags or frequency disturbances in the main grid. High resiliency is a key benefit of LVdc in applications that require extremely high availability, such as data centers or some critical production lines.

Applications, Pilot Projects, and Market Readiness

Several municipalities in The Netherlands have LVdc-based streetlight

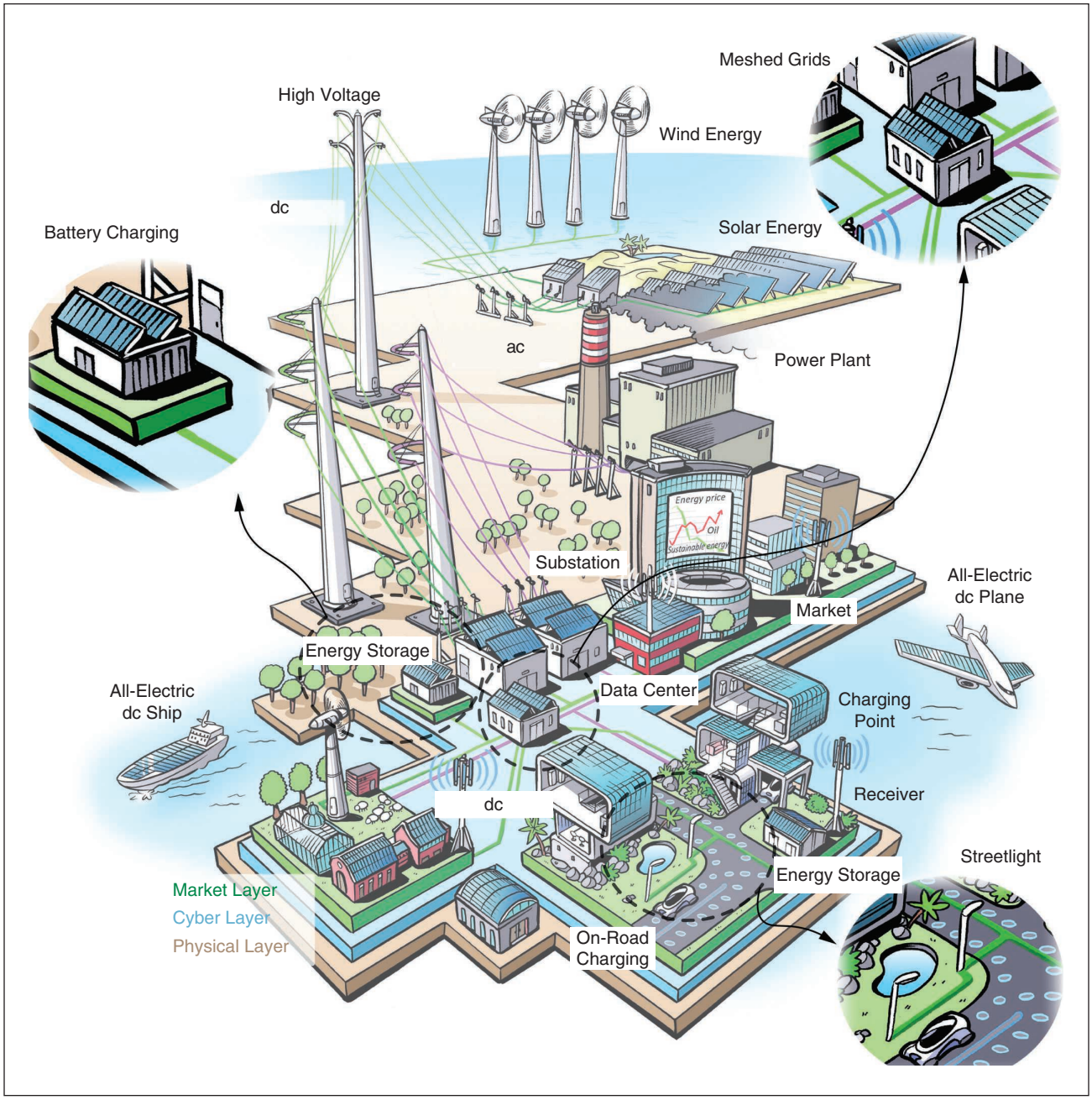

FIGURE 1 – A future smart city based on LVdc distribution microgrids. (Source: [2].)

systems [11]. The port of Amsterdam has also adopted the use of dc technologies [12]. A PV-powered dc testbed with an office LED lighting system showed a potential electricity savings of up to 5% [13]. Using LVdc in data centers can double the mean time between failures when a single uninterruptible power supply per path is used [14].

Moreover, pilot projects, such as [15] and [16], exhibit efficiencies increased by 7–10%. The LVdc office building in [6] demonstrated up to 5.5% energy savings compared to a comparable ac system. An energy-neutral teaching facility that uses LVdc distribution was also demonstrated [17]. One of the first field demonstrations with a 100-kW LVdc bipolar power distribution system was shown to maintain a continuity of supply despite several medium-voltage ac interruptions [18]. A larger system with 160-kW installed PVs, which integrates LEDs, air conditioning, and electric vehicle (EV) charging, was demonstrated in [19].

Figure 2 shows an overview of the current status of LVdc adaptation in different power distribution applications [20]. The first of the three

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defined technology readiness levels is the pilot phase, in which the feasibility of LVdc for a given market is experimentally demonstrated on a small scale. Next is the market-ready phase, in which the first commercialized systems start to appear, followed by the maturity stage at a selected threshold level of 10% market share. LVdc, at the present moment, has a strong foothold in niche markets, especially in private-owned energy distribution systems [20], [21]. Furthermore, LVdc market growth is expected, especially in RESs and ESSs, electromobility, data centers, and utility buildings [21].

Development Challenges and Opportunities

A lack of cost-competitive, market-ready components is one of the major barriers in accelerating the adoption of LVdc technologies in utility and office buildings because the cost of retrofitting is high. This can be addressed with incentives, such as power over Ethernet and the new USB standards [21]. Another significant drawback is the lack of standards and good practices, which are relevant for the installation, operational know-how, and maintenance of these systems [8], [20], [22].

The solutions offered in this article particularly consider the technological challenges that stem from the specific protection requirements of LVdc systems and bidirectional power flow (PFC). The implementation of both of these operational objectives must maintain adequately high efficiency. Furthermore, short circuit protection must conform to selectivity

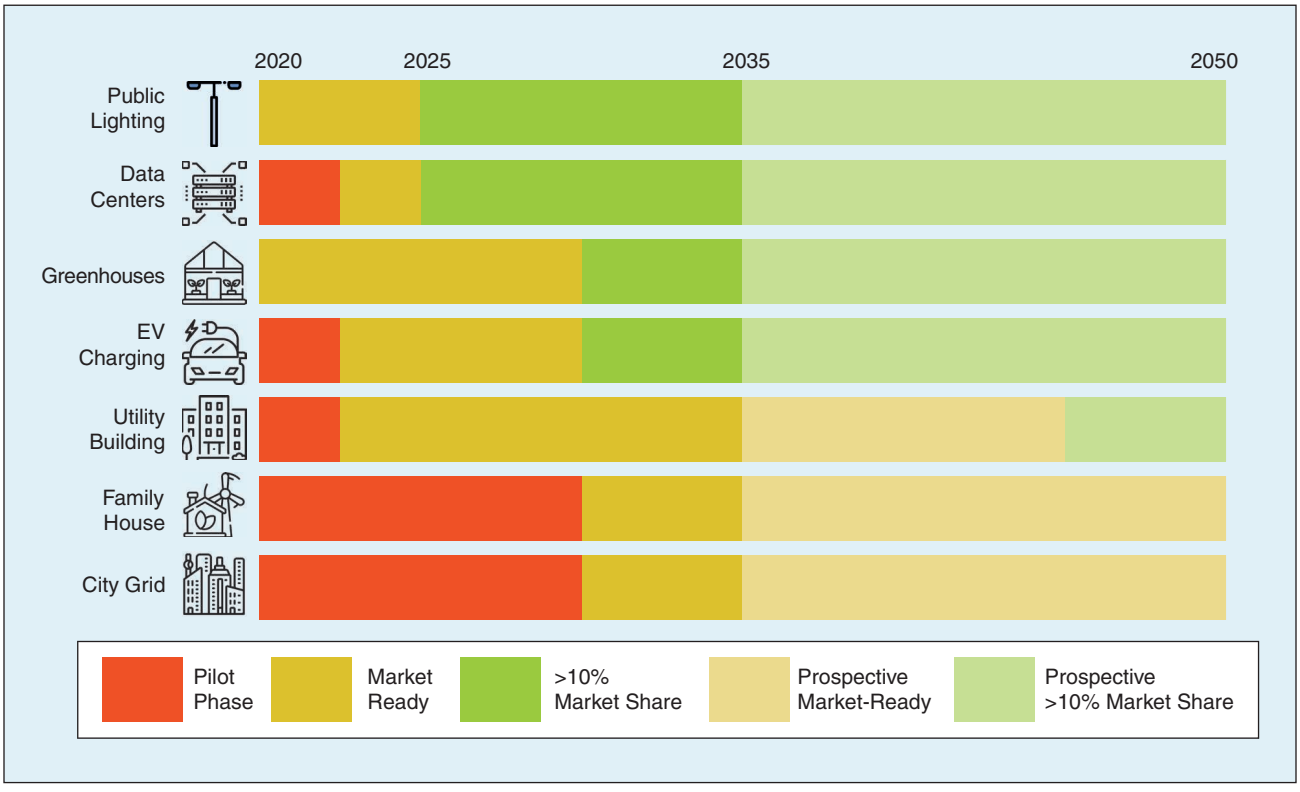

FIGURE 2 – The status of dc applications and outlook on their market readiness.

The solutions offered in this article particularly consider the technological challenges that stem from the specific protection requirements of LVdc systems and bidirectional power flow.

requirements and have rapid interruption capability to limit the sharp rise in fault currents and the energy supplied in this duration. Therefore, in the following sections, an SBB is presented that offers a solution for both technological challenges.

The power flow in a single nonradial dc microgrid can be controlled by coordinating the operation of the participating nodes [23]. If multiple dc microgrids are connected, then the power flowing between the two microgrids is given by the bus voltages. This is potentially undesirable, e.g., the bus voltages are the same when power transfer is needed. Similarly, when multiple paths exist for the current to flow through, the control over the power flow in some lines is lost. An undesirable consequence can be the overheating of these lines. Even if the electrical spring concept is used, such as in [24], the control over the power flow in the interconnection line is not gained. Therefore, PFC devices are necessary.

The three conceptual solutions for PFC are illustrated in Figure 3. The variable line resistance method shown in Figure 3(a) is inherently inefficient [25]–[27]. A high-potential solution is a dedicated dc–dc converter. In the meantime, several solutions have been proposed. Simpler nonisolated topologies for PFC were proposed in [28] and [29]. The advantage of these is the reduced number of components; however, the functionality is also reduced.

In [30], a high-ratio, capacitively isolated dc–dc converter was proposed for PFC. A flyback-based topology was proposed in [31]. Thanks to its versatility and robustness, a dual-active-bridge converter showed promise for application in dc microgrids, and its operation was described in [32] and [33]. The disadvantage of a dedicated dc–dc converter, as shown in Figure 3(b), is that it must be rated for the maximum power transferred (P_{flow}) between the two nodes [30], [34]. The cost and losses can be prohibitive for such a fully rated PEC solution.

The solution shown in Figure 3(c) is a compromise between the prior two concepts, wherein a controlled floating voltage (V_{series}) mimics the drop across a variable virtual resistance. The approach to inject series voltage [35] or current [36] avoids the problem of using fully rated components. Since the required PEC components are rated only for a fraction of P_{flow}, it is referred to as a *partially rated PFC converter* (*PFCC*) [27], [35], [37], [38]. Later, the stability of this approach was investigated in [39], and small-signal modeling was performed in [40]. The proposed concept of a PFCC for dc systems is complementary to the so-called unified power flow controller-based flexible ac transmission systems in traditional ac distribution grids [41]–[43].

Considering short circuits, the consensus for LVdc protection converges to two solutions: hybrid circuit breakers (HCBs) [44] and SSCBs [45], [46]. The main advantage of HCBs is their low on-state losses and ability to interrupt short circuits in the range of milliseconds [44]. However, this fault clearance time can result in short circuit current peaks that are hundreds of thousands of times higher than the nominal currents [47], which necessitates significant oversizing of all of the grid components [48].

Therefore, for small dc nanogrids or microgrids, fast SSCBs are preferred [49]. Two main challenges regarding the use of SSCBs are the on-state losses [50], [51] and overvoltage suppression [45]. A popular choice for SSCBs are silicon (Si) insulated-gate bipolar transistors [45], Si MOSFETs [49], and their Si carbide (SiC) counterparts. Integrated gate-commutated thyristor-based solutions prove to be more efficient in systems with a nominal current in the range of kiloamperes [52].

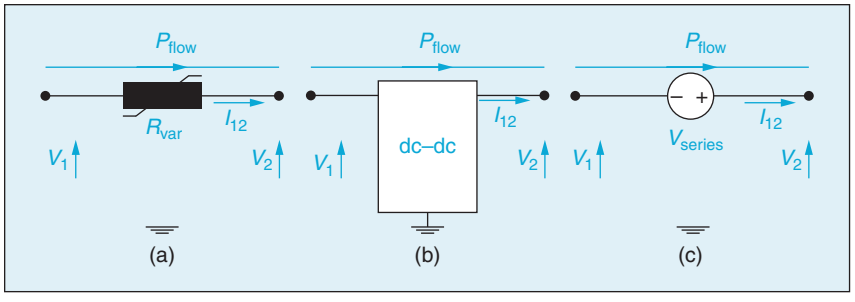

FIGURE 3 – The LVdc microgrid basic PFC options showing the (a) variable resistor, (b) fully rated dc–dc converter, and (c) floating voltage source.

SBBs

The schematic of the partially rated PFCC composed of power electronic switch-based high-voltage (HV) and LV sides (HVSs and LVSs, respectively) is shown in Figure 4. The purpose is to regulate the power flow (P_{flow}) between two nodes (n_t, n_2) with voltages V_1 and V_2 by injecting a relatively small controlled series voltage V_{series}.

It will be shown that the power processed by the PFCC (P_{PFCC}) is a relatively small fraction of P_{flow}. Consequently, it can be inferred that components used for composing the HVS and LVS can be derated in accordance with the respective partial current and voltage requirements during full load operation. A more detailed working principle as well as system protection during short circuit faults at n_1 and n_2 is experimentally described in the "Experiments" section.

Equivalent Circuits

The full PFCC circuit is shown in Figure 4. The PFCC injects a stable dc voltage in

series with the line. Therefore, the LVS can be represented by a voltage source. The power that the PFCC injects in the form of series voltage is taken from the system by the HVS. The HVS does not regulate the bus voltage; however, it behaves as a current source that sinks power. The two sources are coupled. The power that is taken from the dc system by the HVS is reinjected by the LVS, and part of it is dissipated.

The equivalent circuit of the PFCC is shown in Figure 5. The presented abstraction is used as the key building block for different system-level applications proposed in this article.

The current I_{PFCC} drawn by the building block is given by

$$I_{\text{PFCC}} = \frac{P_{\text{PFCC}}}{V_t} = \frac{P_{\text{flow}} V_{\text{series}}}{\eta V_t V_t'}, \qquad (1)$$

where V_{series} is the control action that results in the desired P_{flow} between terminals with voltages V_t and V_t'. It must be noted that P_{flow} and V_t' are intimately related and govern the current flow I_{flow} between the two terminals. Therefore, the PFCC block can be used in different applications that require the functionality to regulate these three operating parameters in the system as a function of V_{series}.

Operating Efficiency and Loss Breakdown

The factor η in (1) is the efficiency of the PFCC building block that relates the block power loss P_{loss} to the processed PFCC power, including the component losses in HVS, LVS, and SSCB, as described by

$$P_{\text{loss}} = (1-\eta) P_{\text{PFCC}}. \qquad (2)$$

For the defined system-level efficiency η_{sys}, neglecting the losses due to the line impedances, the equality described by (3) must be followed:

$$(1-\eta_{\text{sys}}) P_{\text{flow}} = (1-\eta) P_{\text{PFCC}}. \qquad (3)$$

Since $P_{\text{PFCC}} \ll P_{\text{flow}}$, it is inferred that $\eta_{\text{sys}} \gg \eta$ as can be observed from the simulated efficiency curve shown in Figure 6.

The presented results are based on a detailed switch model developed in the Power Electronics Simulation Platform. The HV switches used in the PFCC are C3M0030090K and IPB017N10N5 for the LV part of the PFCC.

While the shown results are representative and can be different depending on the design considerations, the highlighted principle is that the system-level efficiency for achieving the desired control objective is high even if the actual converter efficiency itself is relatively lower. The loss breakdown for different block components is shown in Figure 6(c). In addition to the potential system-level efficiency improvement, the material usage, size, and—inevitably—cost of the PFCC building block is lower compared to a fully rated dc–dc converter, considering that the passive as well as active components in the HVS and LVS are derated.

Scalability

In the next section, a wide spectrum of applications is discussed that spans across power levels. The PFCC building block has a HVS and LVS where different requirements are placed on the semiconductor. On the HVS, the semiconductor switch has to be rated for the system voltage. In this article, only systems with

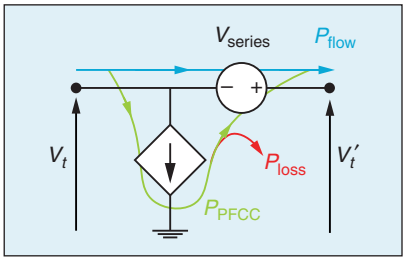

FIGURE 5 – An equivalent circuit of the proposed building block.

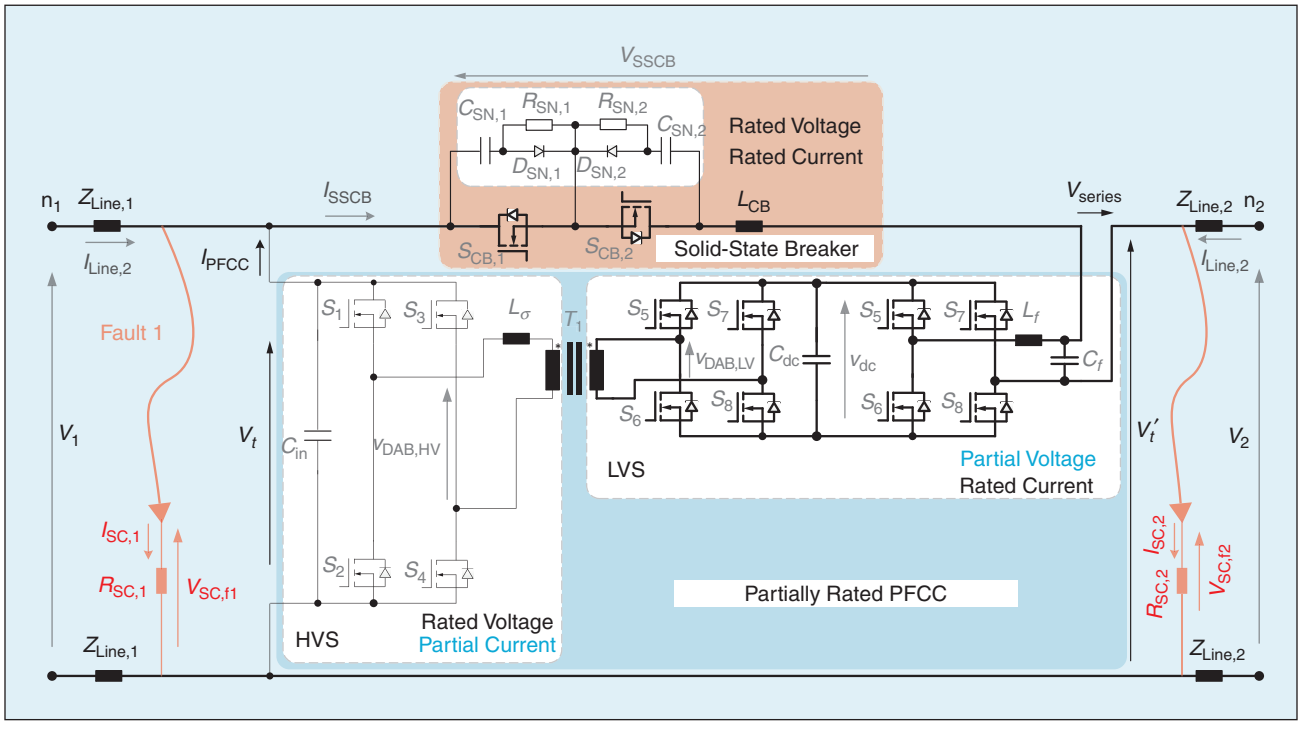

FIGURE 4 – The PFCC for LVdc grids with integrated short circuit protection.

Considering short circuits, the consensus for LVdc protection converges to two solutions: hybrid circuit breakers and SSCBs.

voltages under 1.5 kV are assumed. The HVS in the proposed concept can be scaled to these system voltages with emerging SiC MOSFETs that go beyond the 1.7-kV rating. Since the current flowing through the HVS is only a fraction of the system current, higher-voltage SiC MOSFETs are ideal candidates.

On the LVS, semiconductors conduct the system current; however, the operating voltage is in the range of tens of volts for the considered systems. The state-of-the-art Si MOSFETs rated under 100 V have very low on-resistance and are easy to parallel. Therefore, the semiconductor components used in the PFCC do not prohibit scaling the building block for systems with operating currents up to 500 A. Moreover, the PFCCs can be easily paralleled to increase the power rating, as shown in [35].

The passive components are high-frequency transformers and capacitors used within the dual active bridge (DAB) converter. As discussed previously, the voltage ratio is relatively high; however, the operating requirements placed on the passive components within the DAB are well within the operating areas described in the literature. The block has a filter on the output that consists of an inductor and a capacitor. The voltage rating is relatively small. However, the current flowing through the filter is the full system current. The inductor size rises with the current peak, and a careful design is needed to avoid saturation. The capacitor, on the other hand, benefits from a very small operating voltage, and standard multilayer ceramic capacitors can be used.

Based on the discussion, the system is scalable within the scope of LVdc systems. However, works such as [53] show that similar concepts can find applications even in medium-voltage dc or HVdc systems.

The SSCBs must be rated for the full system voltage and currents. An exhaustive discussion on the limitations of SSCBs is out of the scope of this article. However, the SSCB prototypes reviewed in the "LVdc Promise and Outlook" section show the feasibility of their application in LVdc systems.

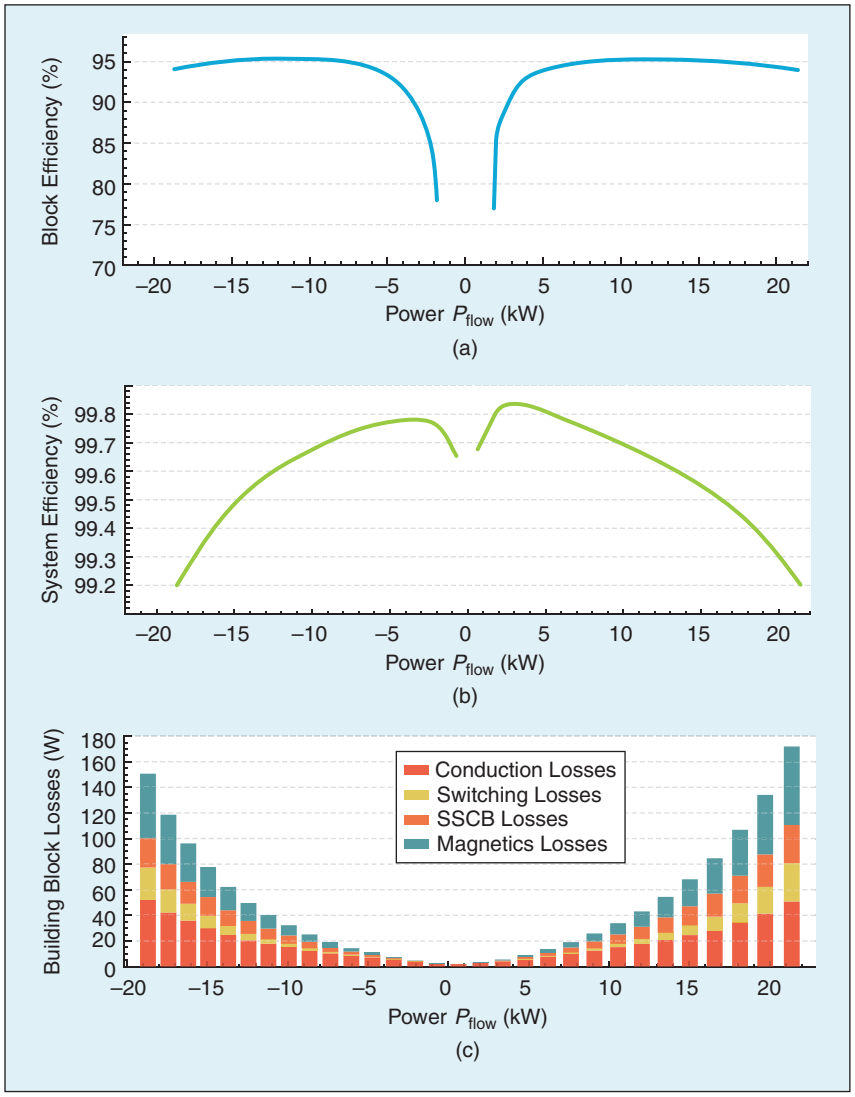

FIGURE 6 – The SBB efficiency: the (a) building block level efficiency η, (b) system efficiency η_{sys}, and (c) loss breakdown.

Applications

In the previous section, the key benefits and operation principle of the developed building block were presented. Now, the equivalent circuit is used in three different applications, which are at different market adaptation levels. They were chosen such that they represent three different control roles and have different sizing requirements. Thus, each example reveals new insights about the proposed building block.

DC Charging

Interfacing batteries with dc systems is often done via synchronous buck converters when galvanic isolation during

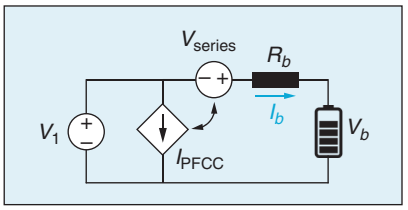

FIGURE 7 – A simplified equivalent circuit representing dc charging with a PFCC.

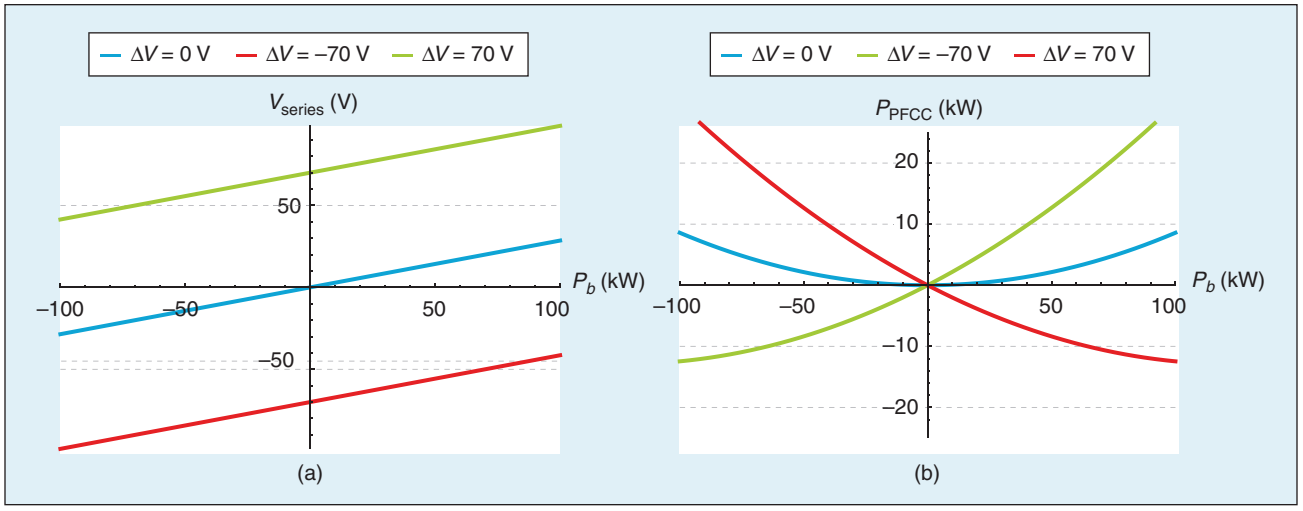

FIGURE 8 – The dc battery charging with PFCC: the (a) series voltage of and (b) power processed by the PFCC as a function of the battery power.

normal operation is not required. The galvanic isolation during faults is provided by external circuit breakers and mechanical contactors. The proposed building block can interrupt faults, and only mechanical contactors are added to ensure galvanic isolation. A simplified circuit of battery charging with a PFCC is shown in Figure 7. For simplicity's sake, the battery is assumed to behave like a voltage source with small internal resistance. Furthermore, no resistance between the source and PFCC is assumed. By analyzing the circuit in Figure 7, the following equations can be written:

$$V_{\text{series}} = \frac{P_b R_b}{V_b} - \underbrace{(V_1 - V_b)}_{\Delta V}, \tag{4}$$

$$P_{\text{PFCC}} = \frac{P_b}{\eta V_b} V_{\text{series}}, \tag{5}$$

where P_b is the battery power, and V_b is the battery terminal voltage.

Figure 8 shows the results of the simplified system when the nominal dc voltage is $V_1 = 350$ V, and the internal battery resistance is $R_b = 0.1\,\Omega$. Figure 8(a) illustrates the series voltage injected by the PFCC during charging at different voltage drops. The voltage drop range is 40%, which is the maximum operating voltage drop of most batteries.

The first observation from Figure 8(a) is that the maximum required series voltage for the given range of P_b is smaller than one fifth of the nominal grid voltage. The total range of the series voltage is, therefore, within one third of the nominal voltage; i.e., for the system used in this example, the operating voltage of the PFCC on the LVS is only ± 100 V. This small processed voltage translates to small power processed.

Figure 8(b) shows the power processed in the PFCC as a function of the charging power. For the nominal case, when the battery voltage is the same as the source voltage, the power processed is 10-times smaller than the charging power. This ratio is less favorable in extreme cases when the battery voltage is 20% higher or smaller than the grid voltage. However, even in extreme cases, the PFCC processes only one fifth of the total charging power. The PFCC maintains the advantage of partial processing. It should also be noted that, normally, the batteries are operated with smaller voltage drops to prevent fast battery degrading.

DC Streetlights

Street lighting was, historically, the first major application of electricity that brought major benefits in terms of increased life quality. Street lighting also seems to be the first major application opened for dc distribution. The motivation to use dc in street lighting stems from the decreased use of incandescent and high-pressure sodium bulbs due to concerns about their negative impact on the environment. Municipalities are seeking to retrofit lights with more energy-efficient LEDs as well as install a remote monitoring and control system. Already-existing dc pilot projects are in the port of Amsterdam and A4 highway in Delft, The Netherlands.

Consider only the shaded gray region of the equivalent circuit shown in Figure 9. This is representative of a street-lighting system of N poles equally spaced $d = 20$ m apart without a PFCC. The lumped power drawn by N lamps in such a system can be represented by a current sink $I_{\Sigma,1}$ and is given by

$$I_{\Sigma,1} = \frac{NP_{\text{lamp}}}{v_t}. \tag{6}$$

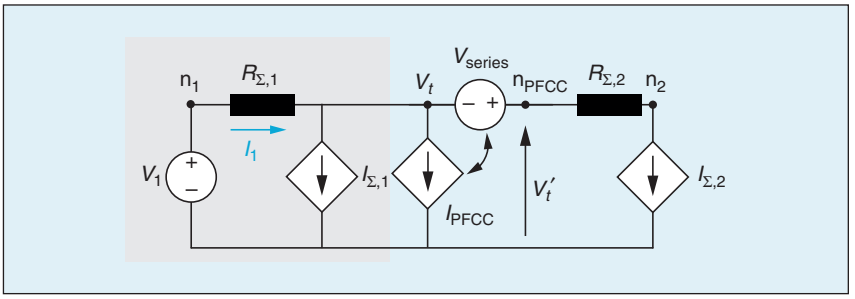

FIGURE 9 – An equivalent circuit of a streetlight system with a PFCC. The shaded gray part can be considered as the equivalent circuit of a streetlight system without a PFCC installed.

The motivation to use dc in street lighting stems from the decreased use of incandescent and high-pressure sodium bulbs due to concerns about their negative impact on the environment.

Here, the rated power drawn by a single lamp is taken as $P_{\text{lamp}} = 50$ W. The lumped resistance $R_{\Sigma,1} = NdR$ is estimated assuming a line resistance $R = 6.57\ \Omega$/km. The voltage profile along the feeder line in the absence of PFCC-based voltage regulation is shown with a solid black line in Figure 10(a). It can be observed that the allowable drop in line voltage (V_{min} assumed at 10% of V_{nom}, shown by the red line) limits the line length to approximately 800 m corresponding to $N = 40$ for the considered parameters, as given by

$$N \leq \underbrace{\sqrt{\frac{V_{\text{nom}} - V_{\text{min}}}{dRi_{r,\text{max}}}}}_{N_{\text{max}}}, \tag{7}$$

where $i_{r,\text{max}} = P_{\text{lamp}}/V_{\text{min}}$ is the maximum operating current of a single lamp. In case the PFCC element is added to regulate V_t' to the nominal system voltage (V_{nom}), as shown in Figure 9, the number of series-connected lamps can be extended to $N_{\text{ext}} = N_{\text{max}} + \Delta N$. It can be inferred that N_{max} lamps can be installed between the output terminal of the PFCC and the end node n_2.

Correspondingly, the lumped resistances in such a system are given by $R_{\Sigma,1} = \Delta NdR$ and $R_{\Sigma,2} = N_{\text{max}}dR$. The currents $I_{\Sigma,1}$ and $I_{\Sigma,2}$ are related to the lumped power drawn by $N = \Delta N$ and $N = N_{\text{max}}$ lamps, respectively, as described by (6). The maximum possible line extension corresponds to the maximum lamps Δn_{max} between the source node n_1 and input terminal of the PFCC such that the limit $V_t \leq V_{\text{min}}$ is not breached.

It can be seen from Figure 10(a) (blue line) that the length can be increased by about 50% to approximately 1,260 m, corresponding to $\Delta n_{\text{max}} = 23$ for the given operating conditions. It should be noted that, in this article, only a single PFCC is considered, and further extension is possible if multiple PFCCs are used.

Assume that the voltage-regulating PFCC is installed such that N_{max} lamps exist between its output node n'_{pfcc} and the end node n_2. The operating PFCC voltage (V_{series}) and processed power (P_{PFCC}) as a function of the extended number of lamps (Δn) in the system is shown in Figure 10(b) and (c), respectively. For example, if the streetlight system is extended to power 10 extra lamps ($\Delta n = 10$), the PFCC needs to inject a small $V_{\text{series}} \approx 10$ V such that $V_t' = V_{\text{nom}} = 350$ V. The corresponding power processed $P_{\text{PFCC}} \approx 50$ W is one tenth of the additional load power associated with the extra lamps installed.

Consequently, it can be inferred that benefits in terms of the installation cost and operating efficiency of the system can be attractive as compared

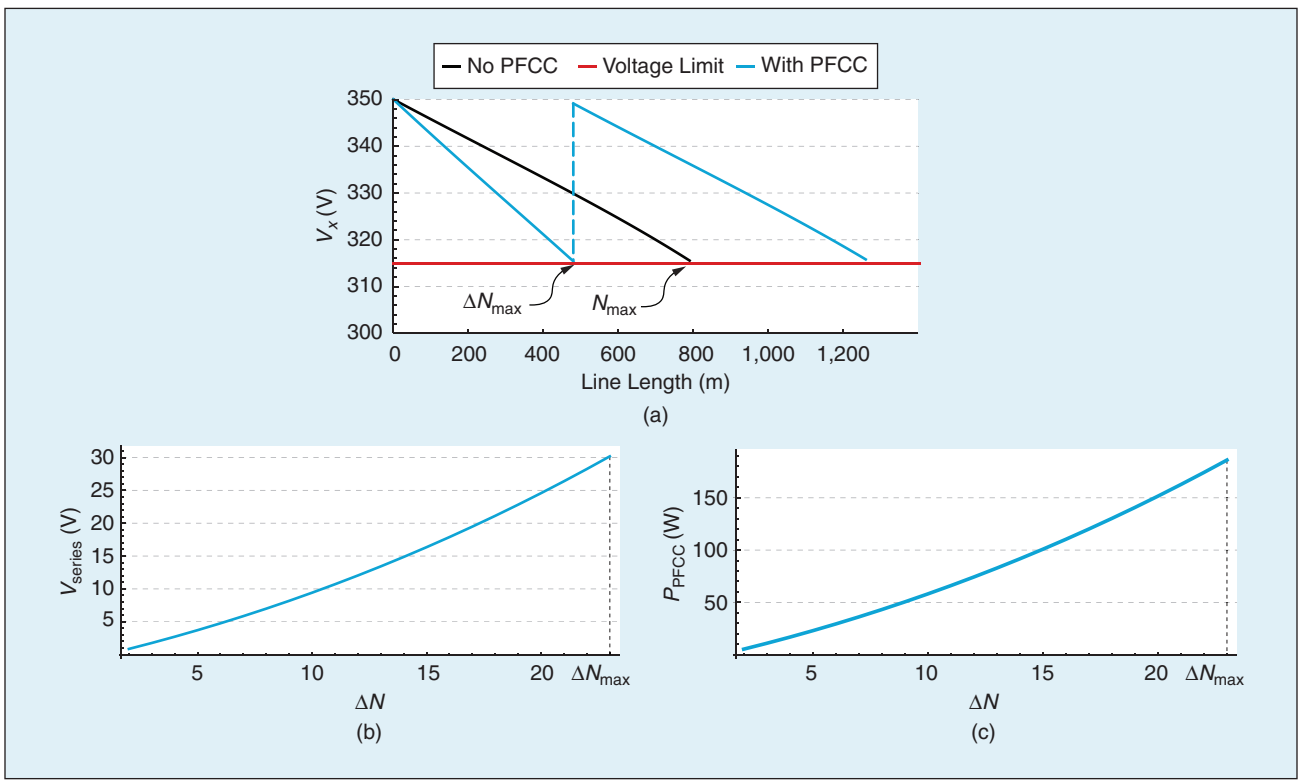

FIGURE 10 – The voltage drop compensation in the street-lighting system: the (a) voltage profile of the system without (black) and with the PFCC (cyan) as well as the (b) series voltage and (c) power processed by the PFCC, both shown as functions of the number of added lamps.

to conventional solutions, such as reconductoring, multiple parallel paths, or the use of a fully rated converter. The limit for $\Delta n_{\max}$ can further be increased if $V_t' > V_{\text{nom}}$ is permissible. The discussed use of a PFCC building block specifically for line voltage regulation can be similarly conceptualized for other dc applications, such as power distribution to residential buildings.

Figure 11 shows an outlook on the possible line extension when multiple PFCCs are used in the same system. The trend in the figure shows saturation after several PFCCs are added. However, it is worth underlining that, in theory, it is possible to extend the line length by 400%, see (8) at the bottom of the page.

Meshed dc Networks

Considering the potential benefits of dc technologies in markets like streetlights, charging stations, data centers, and utility buildings, it is anticipated that interconnecting such systems to form a dc distribution grid is plausible, as illustrated in Figure 1. The possible advantage of this strategy is improved system availability and efficiency, particularly when meshed topology is employed. When several paths for current to flow along exist, extra care must be taken to ensure that no line is overloaded. A PFCC can enhance the power capacity of the meshed system and ensure that the interconnecting lines are not overloaded.

Figure 12 shows a simplified schematic of a basic meshed network. If V_1 is assumed to be the same as V_2, two paths exist for the current to flow along from the voltage source V_1 to the load, represented by the power source $I_N = P_N/V_N$. The power source can both sink and source power.

If the voltage V_{series} is zero, the current flow in the two paths is given by the resistance ratio $k = R_{\text{line},2}/R_{\text{line},1}$. For the sake of this example, in the following analysis, the ratio is assumed to be equal to two, implying that the current flowing in line 1 will be two times as high as the current flowing in line 2. If the system further operates at a nominal voltage $V_1 = V_2 = 350$ V, and the line resistance $R_{\text{line},x} = 6.57$ (Ω/km), line 1 is 100 m long. The maximum carrying capability of the line is 35 A. Figure 13(a) shows the currents in a network defined by these parameters and assumptions.

A PFCC can enhance the power capacity of the meshed system and ensure that the interconnecting lines are not overloaded.

As expected, the current in line 1 in Figure 13(a) has double the amplitude compared to the current in line 2. The current in line 1 also reaches the maximum current-carrying capability faster than the current in line 2 for both scenarios when the power source P_N is sourcing, i.e., $P_N > 0$, and when it sinks power, i.e., $P_N < 0$. The voltage of the series source is calculated as shown in (8).

The series voltage can be calculated by solving Kirchhoff's current equations for the maximum line current $I_{1,\max}$ for the circuit in Figure 12. The series voltage is a function of the line's maximum current-carrying capability, ratio of the path resistances k, system voltage V_1, and power transferred P_N. The series voltage is zero, while the maximum current limit in the line in which it is installed is not breached. The series voltage has a maximum limit that ensures that the current in line 2 is not breached either; the voltage limit is expressed in (9). The maximum

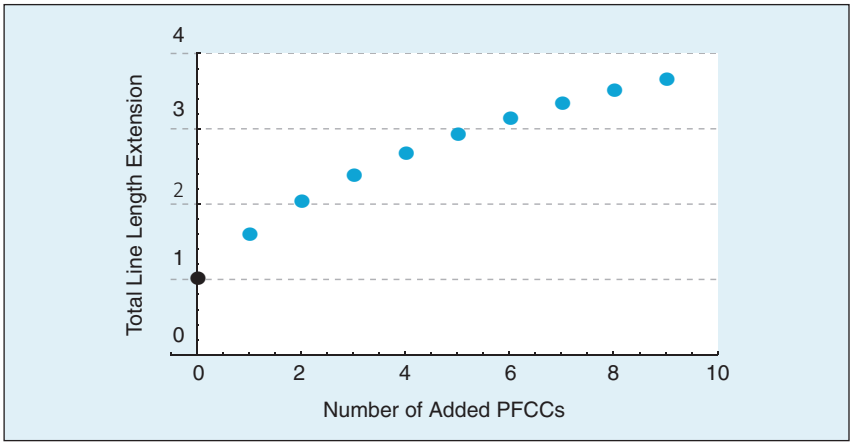

FIGURE 11 – A possible streetlight line extension with multiple PFCCs.

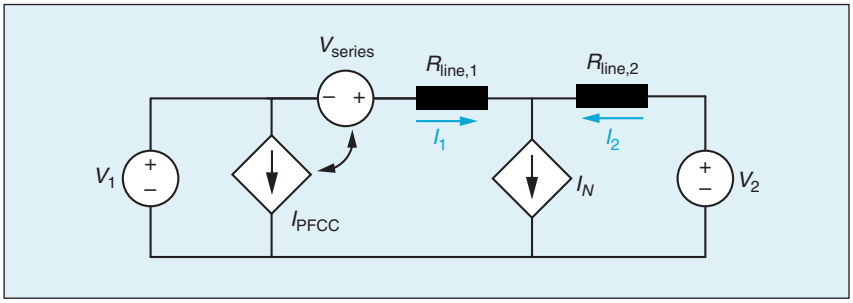

FIGURE 12 – An equivalent circuit of a three-node meshed LVdc grid with a PFCC.

$$|V_{\text{series}}| = \begin{cases} \frac{1}{2}\left((2+k)I_{1,\max}R_{\text{line},1} - V_1 + \sqrt{(kI_{1,\max}R_{\text{line},1} + V_1)^2 - 4kP_N R_{\text{line},1}}\right) & \Longleftrightarrow |I_1| \geq I_{1,\max} \\ 0 & \Longleftrightarrow I_{1,\min} \geq I_1 \geq I_{1,\max} \end{cases}. \quad (8)$$

allowed series voltage is calculated from Kirchhoff's current equations of the circuit in Figure 12 when solved for $I_{1,\max}$ and $I_{2,\max}$:

$$|V_{\text{series},\max}| = R_{\text{line},1}\left(\frac{P_N}{V_1 - kI_{2,\max}R_{\text{line},1}} - (1+k)I_{2,\max}\right). \quad (9)$$

Figure 13(b) shows the voltage V_{series} as a function of power P_N; clearly, the series voltage needed to ensure the current limit in both lines is less than 10% of the nominal grid voltage. Figure 13(c) shows the power processed by the PFCC, which is less than 1 kW for both directions of power flow. The gain in the power transfer capacity is 2.5 kW and 8 kW for power sinking and sourcing by I_N, respectively.

The difference in the power enhancement capability, in this particular case, stems from the placement of the controlled current source I_{PFCC}. When power node P_N is sinking power, the current flows from the voltage source V_1. The current I_1 is a combination of the current supplied to the load and I_{PFCC}. If the current is supplied from V_1, then, in addition to I_N, I_{PFCC} also has to be supplied, thus reducing the net amount of power that can be supplied to power source P_N via line 1. In the opposite direction, the effect is reversed. To gain the most power enhancement, the PFCC should be installed in both lines. Given that the very low power rating of the PFCC is sufficient, such installations are feasible.

Experiments

The goal of the experiment is twofold. The first aim is to demonstrate the operation in a simple two-node connection, similar to a dc charging application. The second is to closely emulate the conditions during a bolted short circuit, i.e., almost zero fault resistance. The short circuit emulation demonstrates the capability of the proposed combination to protect the derated components from failure during grid faults.

The PFCC prototype electrical parameters and those of the SSCB and line are summarized in Table 1. A controllable short circuit is created with a MOSFET with an $R_{\text{ds,on}}$ of 20 mΩ, which creates a good approximation of a bolted short circuit. The nodes V_1 and V_2 are emulated using the Delta Elektronika SM15K series power supplies. The nominal voltage during all experiments is 350 V on both nodes. A simplified schematic of the experimental setup is shown in Figure 14.

PFCC Operation

The experimental results obtained during normal operation of the PFCC are shown in Figure 15(a) and (b). The PFCC controls the power flow between two nodes n_1 and n_2, as illustrated in the schematic in Figure 4. The experiment starts when both nodes n_1 and n_2 reach the nominal voltage, i.e., 350 V. The SSCB is closed and remains in the conducting state during the experiments, i.e., MOSFETs $S_{\text{CB},1}$ and $S_{\text{CB},1}$ are turned on.

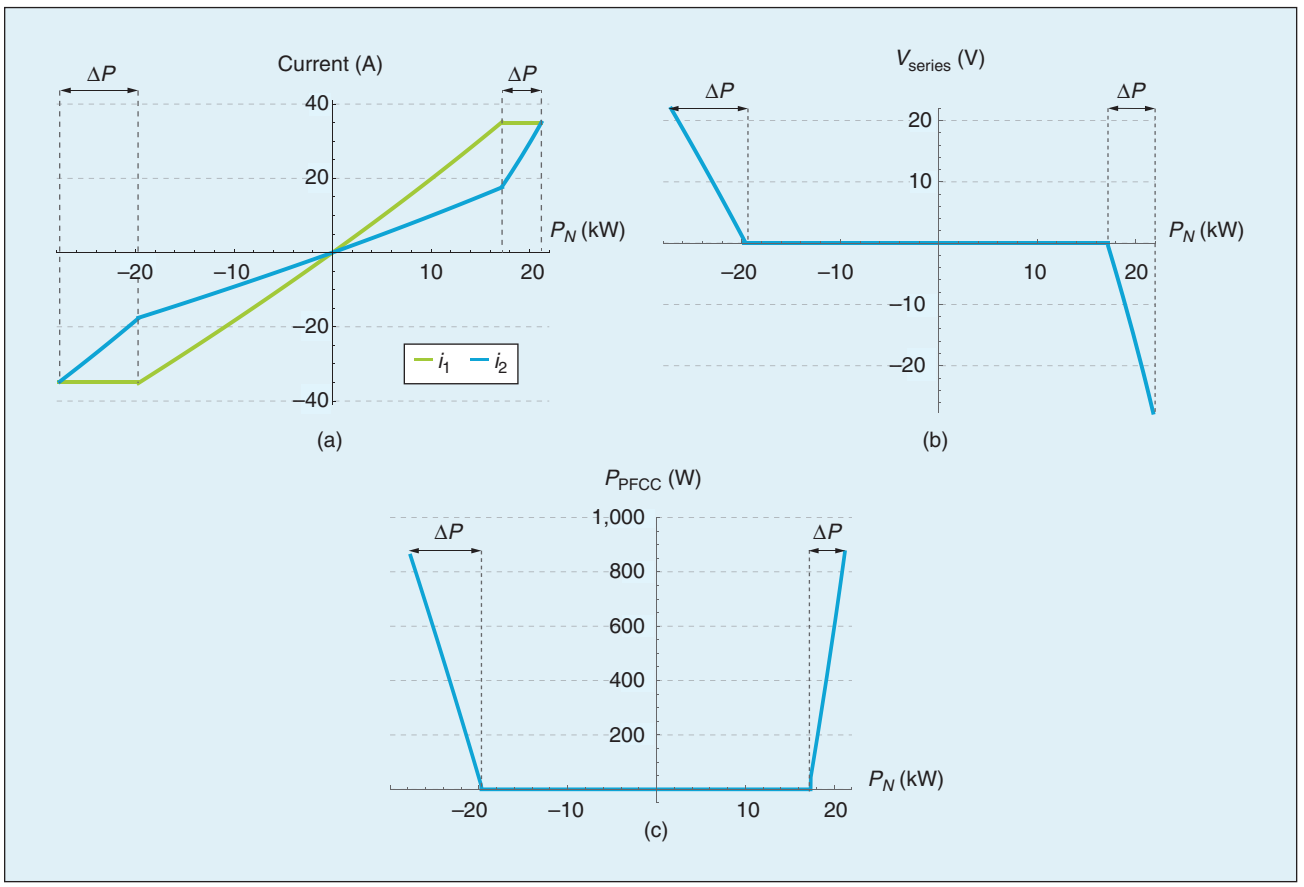

FIGURE 13 – The current rerouting in a meshed LVdc microgrid: the (a) line currents as a function of the transferred power as well as the (b) series voltage of the PFCC and (c) PFCC processed power, both shown as a function of the transferred power P_N.

- Intervals t_1 and t_3: The PFCC is inactive, and the voltage on nodes n_1 and n_2 is equal. In such a case, no current flows between the nodes, and no power is exchanged. This represents the potentially undesirable case described in the "Overview" section to motivate the introduction of PFC devices.
- Interval t_2: The PFCC is activated. The voltage V_{series} of the PFCC is controlled to be −10 V. From node V_1, current $I_{\text{Line},1}$ starts to flow to node V_2. The power P_1 supplied by node n_1 is around 800 W, while the power P_{PFCC} injected by the PFFC is only around 25 W.
- Interval t_4: The PFCC is activated. Compared to the interval t_2, the voltage V_{series} has the opposite polarity. It is regulated to be 10 V. Therefore, during the time interval t_4, it is the node V_2 supplying the power. This demonstrates the ability of the PFCC to regulate bidirectional power flows.

Short Circuit Withstand Capability

As discussed in the "Overview" section, handling short circuits is a challenge in LVdc systems. The following two experiments show that the proposed building block is capable of withstanding short circuits on both sides. The short circuit locations are shown in Figure 14.

Fault 1

Figure 15(c) shows the waveforms during the clearing of short circuit fault 1. Immediately after the inception of fault 1, it can be observed that the voltage $V_{\text{sc,f1}}$ drops. The capacitor C_{in} is quickly discharging into the short circuit, as is demonstrated by the rise of the current I_{PFCC}. The short circuit current that is supplied from the capacitor C_{in} peaks at more than 400 A.

The fact that this capacitor current is limited only by the impedance of the short circuit path during fault 1 is not problematic, as there is no critical equipment in the pathway, and the capacitor can supply a high current only for a short period; i.e., the energy dissipated is small. The short circuit current is also supplied from node n_2. The supplement is visible by the current I_{SSCB}, which flows in the reverse direction. The rise of this current is slower compared to the current I_{PFCC}, as it is limited by the line inductance $L_{\text{Line},2}$ and SSCB limiting inductance L_{CB}.

The voltage $V_{\text{CB,gs}}$ is the gate source voltage on the MOSFET $S_{\text{CB},2}$. This voltage marks the start of the clearing process $\tau_{\text{turnoff},1}$. After SSCB MOSFETs are turned off, the current I_{SSCB} continues to rise for a short period defined by the size of the snubber capacitor $C_{\text{SN},2}$. Figure 15(c) shows the rise of the voltage V_{series} as well. The notable sharp rise of V_{series} after the fault inception is also visible on the voltage across the SSCB $-V_{\text{SSCB}}$. The voltage V_{SSCB} continues to rise to negative values until it reaches approximately 400 V, which is the difference between the short circuit voltage $V_{\text{sc,f1}}$ and node voltage V_2.

Fault 2

Figure 15(d) shows the waveforms during the clearing of short circuit fault 2, which is located at the point of injection of V_{series}. During fault 2, the capacitor C_{in} contributes to the short circuit current, which is visible from the rise of the current I_{PFCC}, and the rises of the currents I_{PFCC} and I_{SSCB} are slower than during fault 1. This is a consequence of using limiting

TABLE 1 – PARAMETER SPECIFICATIONS.

PARAMETER	SYMBOL	VALUE
PFCCs		
Nominal input voltage	$V_{\text{DAB,in}}$	350 V
PFCC dc-link voltage	V_{dc}	50 V
Switching frequency	f_{sw}	62.5 kHz
Parasitic inductance	L_{σ}	72 μH
Input dc capacitor	C_{in}	16 μF
DC-link capacitor	C_{dc}	1.22 mF
Unfolder bridge inductor	L_f	47 μH
Unfolder bridge capacitor	C_f	1.22 mF
SSCBs and lines		
Nominal current	I_{SSCB}	36 A
on resistance	R_{on}	8 mΩ
Maximum pulse current	$I_{\text{SSCB,pulse}}$	378 A
Limiting inductance	L_{CB}	3 μH
Snubber capacitance	$C_{\text{SN},x}$	0.32 μF
Snubber resistance	$R_{\text{SN},x}$	10 Ω
Line resistance	$R_{\text{Line},x}$	1.3 Ω
Line inductance	$L_{\text{Line},x}$	1.4 μH

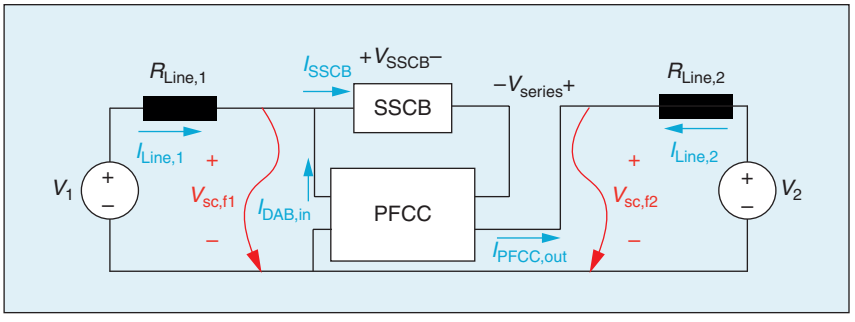

FIGURE 14 – A simplified schematic of the experimental setup.

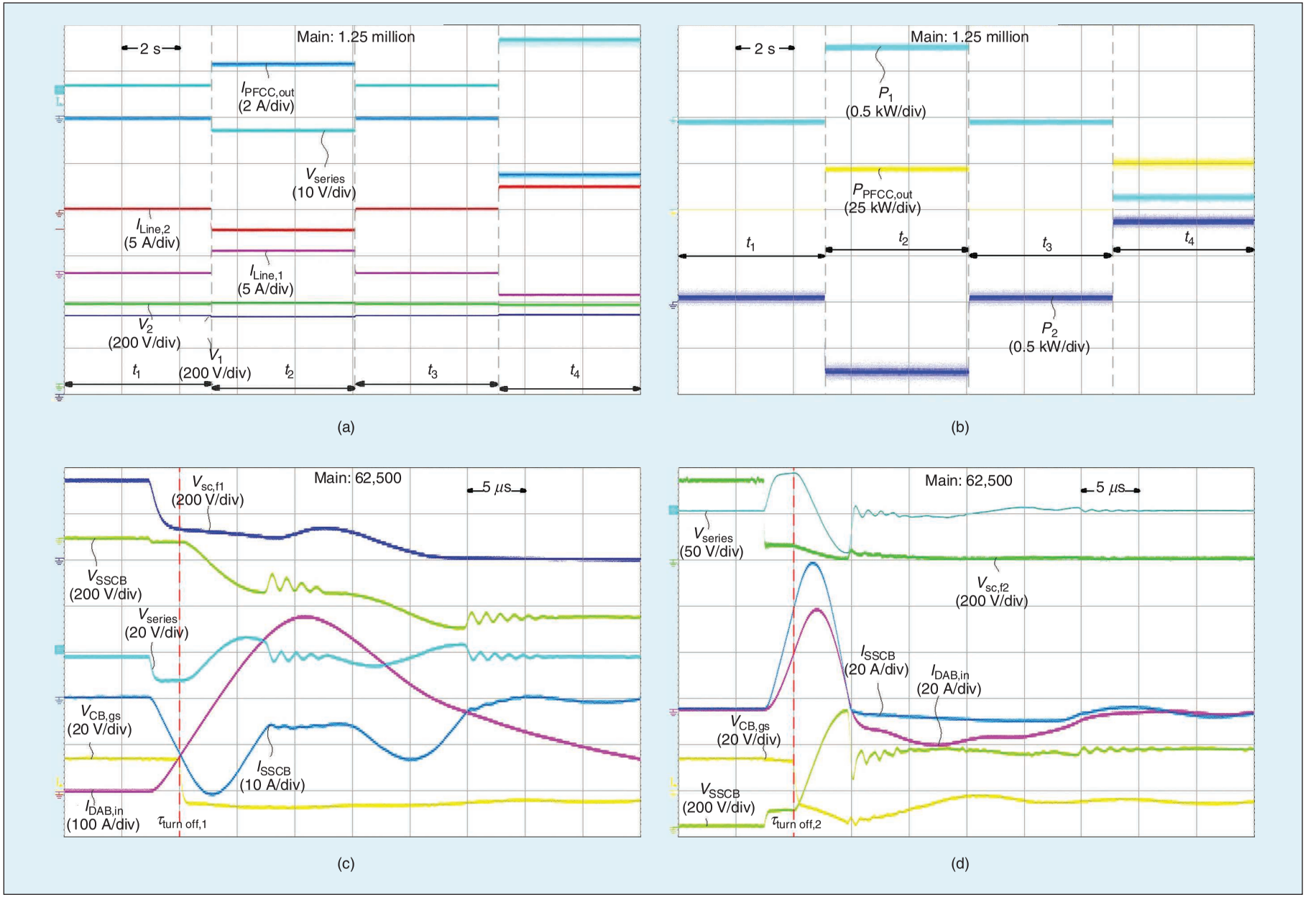

FIGURE 15 – The operational waveforms of the PFCC and SSCB: the (a) waveforms during PFC by the PFCC and (b) powers. Also shown are the variables during short circuit faults (c) 1 and (d) 2. div: division of the axis.

inductance L_{CB}. The peak current amplitude reached by the I_{SSCB} is around 60 A. However, a bulk of short circuit power is supplied from node n_2, but it does not flow through the building block.

During fault 2, the voltage V_{series} rises sharply to 50 V before the time $\tau_{turnoff,2}$, when MOSFETs $S_{CB,1}$ and $S_{CB,2}$ are turned off. This sharp rise is also visible on the voltage V_{SSCB}. After $\tau_{turnoff}$, the current I_{SSCB} continues to rise, as does the voltage V_{SSCB}. When the current I_{SSCB} reverses, so does the voltage V_{series}. It is notable, however, that the voltage V_{series} stabilizes after 30 μs, and the PFCC can return into stable operation.

Conclusion and Outlook

The technology discussed in this article pertains to a building block that is integrated with LVdc systems to give a scalable, compact, and derated solution for power and voltage regulation. A combination of a PFCC and fully rated SSCB is used for interesting dc applications, such as charge control for batteries, the voltage regulation of dc street-lighting systems, and current flow rerouting in meshed dc grids.

A simple steady-state equivalent model of a PFCC is used to demonstrate the role of the PFCC in three chosen applications, which are in various stages of technology readiness: street lighting, battery charging, and meshed LVdc grids. When used for battery charging, the PFCC acts as a charge controller and has to operate in a relatively large voltage range compared to other applications. However, even when the voltage swing is assumed to be 40% of the nominal grid voltage, the PFCC processes less than one third of the charging power.

The street-lighting system accumulates a voltage drop, which limits the segment length. The PFCC acts as a voltage compensator, which, in the presented scenario, extends the segment length by 50%. The prolonging of lines can bring potential economic benefits through material savings and easier installation.

Meshed grids in which the current follows along the path of least action can run into local congestions. The proposed building block enhances the power capacity of the grid by up to 40% while processing less than one tenth of the system power. The building block can thus prevent the local congestion by rerouting the current in meshed LVdc systems or interconnected LVdc grids. In all three applications, the PFCC processes only a fraction of the total system power. This is the key to the economic savings and efficiency gains.

The proposed building block enhances the power capacity of the grid by up to 40% while processing less than one tenth of the system power.

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