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A Continuous-Time Zoom ADC for Low-Power Audio Applications

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***Abstract*— This article presents a continuous-time zoom analog to digital converter (ADC) for audio applications. It employs a high-speed asynchronous SAR ADC that dynamically updates the references of a continuous-time delta–sigma modulator (CTDSM). Compared to previous switched-capacitor (SC) zoom ADCs, its input impedance is essentially resistive, which relaxes the power dissipation of its reference and input buffers. Fabricated in a 160-nm CMOS process, the ADC occupies 0.27 mm^2 and achieves 108.1-dB peak SNR, 106.4-dB peak signal to noise and distortion ratio (SNDR), and 108.5-dB dynamic range in a 20-kHz bandwidth while consuming 618 μW. This results in a Schreier figure of merit (FoM) of 183.6 dB.**

***Index Terms*— A/D conversion, asynchronous SAR analog to digital converter (ADC), audio ADC, continuous-time delta–sigma, delta–sigma ADC, dynamic zoom ADC, inverter-based operational transconductance amplifier (OTA), low-power circuits.**

I. Introduction

AUDIO analog to digital converters (ADCs) used in battery-powered devices are required to have high linearity and high dynamic range (DR) while also being energy efficient. These requirements can be met by the so-called zoom ADCs that are the hybrid combinations of SAR and delta–sigma ADCs [1], [2]. However, previous designs employed switched-capacitor (SC) front ends that required input and reference drivers capable of delivering large signal-dependent peak currents. For high linearity applications (>90 dB), the power dissipation of these drivers will be higher than that of the ADC itself, in some cases necessitating on-chip buffers, at the expense of chip area [3]. Previous zoom ADCs also required a first-order input filter to prevent aliasing and also to prevent them from overloading in the presence of large out-of-band signals [1], [2].

It is well known that ADCs based on the continuous-time delta–sigma modulators (CTDSMs) generally do not require anti-aliasing filters, while their resistive input impedance is easy to drive [3]. However, their design can be quite challenging. First, the linearity of the amplifiers used to realize their first integrators is quite critical [4]. Apart from directly introducing harmonic distortion, amplifier non-linearity degrades the SNR by folding out-of-band quantization noise into the signal band. However, achieving high linearity usually increases power consumption. To mitigate this, circuit-level techniques to assist the first integrator have been proposed [5], [6]. Although effective, these methods increase design complexity. Another way of mitigating the effect of amplifier nonlinearity is to reduce the first integrator's input swing. This can be done by using a multi-bit digital to analog converter (DAC) or by using a DAC that incorporates a finite impulse response (FIR-DAC) filter [7]. Furthermore, CT DACs suffer from inter-symbol interference (ISI), which manifests itself as distortion. Calibration [7], [8], dual return-to-zero (RTZ) switching [9], or digital ISI shaping techniques [10] have been proposed to mitigate ISI-induced distortion. These techniques considerably increase system complexity and degrade energy efficiency. Also, $1/f$ noise is a dominant noise source in audio CTDSMs. Chopping could be used to suppress $1/f$ noise, but this requires care due to chopping-related artifacts in CTDSMs [7], [11].

We propose a CT zoom ADC that achieves 108.1-dB peak SNR, 106.4-dB peak signal to noise and distortion ratio (SNDR), and 108.5-dB DR in a 20-kHz bandwidth while dissipating only 618 μW [12]. This performance is achieved by combining an asynchronous 5-bit SAR ADC with a third-order single-bit CTDSM. For improved energy efficiency and linearity, its first integrator is based on a capacitively coupled inverter-based operational transconductance amplifier (OTA) that is chopped to mitigate its $1/f$ noise. The DAC employs a novel ISI reduction technique based on a matched-pair layout.

This article is organized as follows. Section II provides a brief introduction to the CT zoom ADC architecture and describes the system design of the ADC along with the error sources and the system-level techniques used to mitigate them. Section III discusses the circuit implementation. The experimental results are presented in Section IV. Finally, this article ends with conclusions.

II. Continuous-Time Zoom ADC

The block diagram of the proposed CT zoom ADC is shown in Fig. 1. It consists of an N-bit coarse SAR ADC and a 1-bit fine CTDSM that operate concurrently. The digital output of the coarse ADC, k, satisfies $k \cdot V_{\mathrm{LSB},C} < V_{\mathrm{in}} < (k+1) \cdot V_{\mathrm{LSB},C}$, where V_{in} is the input signal and $V_{\mathrm{LSB},C}$ is the coarse quantization step or least significant bit (LSB). Via the multi-bit DAC shown in Fig. 1,

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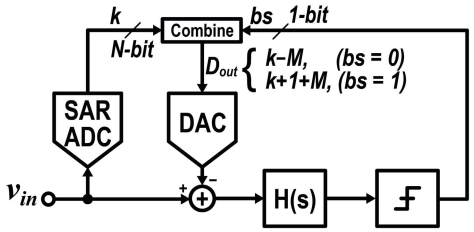

Fig. 1. Block diagram of the CT zoom ADC.

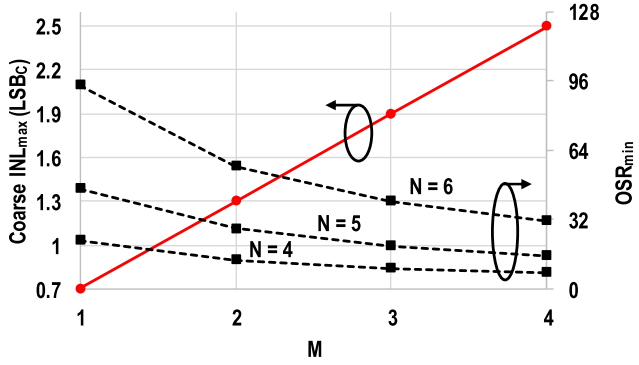

Fig. 2. Acceptable coarse ADC INL level and minimum OSR versus over-ranging factor (M).

the digital value k is used to dynamically adjust the references of the CTDSM such that

$$V_{\mathrm{REF,DSM}} = (k + 1 + M) \cdot V_{\mathrm{LSB},C} \quad (1)$$

$$V_{\mathrm{REF,DSM}} = (k - M) \cdot V_{\mathrm{LSB},C} \quad (2)$$

where M is an over-ranging factor. Driven by the modulator's bitstream (bs), the DAC then toggles between these references, effectively zooming in on V_{in}.

The use of over-ranging ensures that the input signal always lies in the modulator's stable input range even if the coarse ADC is not perfectly linear or if there is a mismatch between the coarse and fine quantization levels. For different values of M, the simulated integral nonlinearity (INL) of the coarse ADC that results in less than 10-dB signal to quantization noise ratio (SQNR) degradation is shown in Fig. 2. It can be seen that as M increases, the linearity requirement on the coarse ADC becomes increasingly relaxed.

If the slope of V_{in} becomes too large, the coarse ADC will not be able to update the fine ADC's references fast enough, leading to increased distortion [1], [2]. This is due to the delay between the sampling moment of the coarse ADC and the moment that its output is used by the DAC. In [2], this delay was minimized by using an asynchronous SAR ADC and by ensuring that its output was transferred to the DAC within half a sampling clock period.

In this article, the same approach is used. By using the analysis in [2] and assuming a full-scale input signal, the maximum input frequency ($F_{\mathrm{in,max}}$) that the zoom ADC can handle can then be expressed as

$$F_{\mathrm{in,max}} = \frac{\alpha(M + 0.5)2F_{\mathrm{BW}}\mathrm{OSR}}{\pi(2^N - 1)} \quad (3)$$

where α is a coefficient that defines the maximum stable input range, F_{BW} is the signal bandwidth, and OSR is the oversampling ratio ($= F_S/2F_{\mathrm{BW}}$). The minimum OSR, $\mathrm{OSR}_{\mathrm{min}}$, required to ensure that $F_{\mathrm{in,max}} \geq F_{\mathrm{BW}}$ for different values of M and N is shown in Fig. 2. It can be seen that for a given M, increasing N also increases $\mathrm{OSR}_{\mathrm{min}}$.

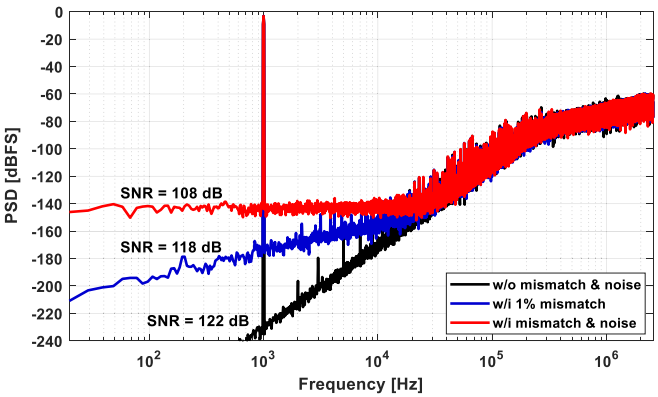

Fig. 3. Output spectra of the CT zoom ADC with different error sources.

A previous SC zoom ADC intended for audio applications achieved 103-dB SNDR with the help of a third-order loop filter, $N = 5$, $M = 2$, and OSR = 282 [1]. However, its coarse ADC required five clock cycles per conversion, so the use of a faster ADC should enable a significant reduction in OSR. This would reduce the power dissipated by the clock generator, the quantizer, and the digital logic, which is quite significant in the chosen 160-nm process. From Fig. 2, $\mathrm{OSR}_{\mathrm{min}}$ is found to be roughly 40 for $N = 5$ and $M = 1$, while simulations show that an OSR of ∼64 is commensurate with a target SNDR of 108 dB (the same as in [1]).

The use of data weighted averaging (DWA) to linearize the zoom ADC's multi-bit DAC puts a higher limit on OSR because it only provides 1st-order mismatch shaping while the CTDSM has a higher-order noise shaping. It also puts a lower limit on OSR due to the level of unit mismatch, below which the shaped mismatch error is too high for the targeted SNDR. Thus, in order to find the optimum OSR, first, an acceptable unit mismatch should be chosen depending on the technology and area restrictions. Assuming a third-order loop filter, $M = 1$, $N = 5$, and 1% unit mismatch, OSR = 128 is found to be the optimum where the contributions of shaped quantization noise and shaped mismatch error are equal at the signal band edge. This is shown in the output spectra obtained from the behavioral simulations shown in Fig. 3 for three different scenarios: no mismatch and thermal noise, 1% unit mismatch and no thermal noise, and both 1% mismatch and thermal noise. The resulting in-band SNR is 122, 118, and 108 dB, respectively. From Fig. 2, these parameters also ensure that the criterion $F_{\mathrm{in,max}} \geq F_{\mathrm{BW}}$ is satisfied with adequate margin.

III. Circuit Implementation

A simplified schematic of the implemented CT zoom ADC is shown in Fig. 4. It consists of a 5-bit asynchronous SAR ADC, a third-order feed-forward compensated loop filter, a 1-bit quantizer, and a 5-bit unary resistive DAC (R-DAC).

A. Loop Filter

As shown in Fig. 4, the CIFF loop filter used in the proposed CT zoom ADC is implemented with active-*RC* integrators.

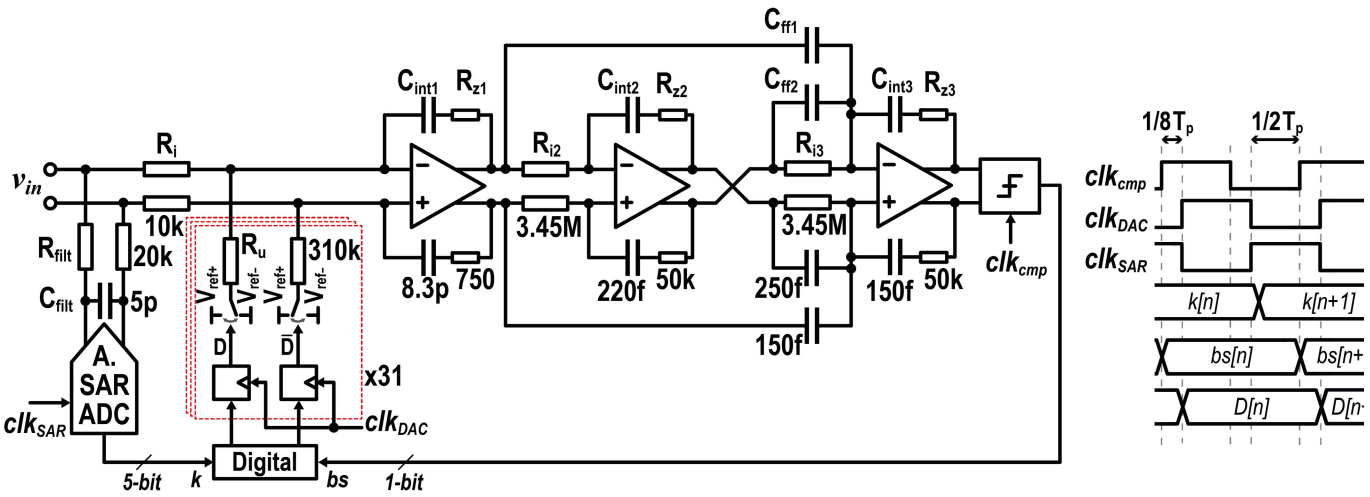

Fig. 4. Simplified schematic of the proposed CT zoom ADC. The units for the resistors are ohms, and the units for the capacitors are farads.

With a 1/8 sampling clock delay in the loop, the modulator is stable and its in-band quantization noise power is at least 10 dB lower than the thermal noise power, even in the case of $\pm 15\%$ *RC* spread. The input resistors ($R_i = 10$ kΩ) define the ADC's thermal noise and are sized to ensure that self-heating-induced distortion is below -120 dB. The integration capacitors are adjustable, making the modulator robust to $\pm 30\%$ *RC* spread.

Compared to other loop filter architectures, a CIFF loop filter has superior distortion and noise performance [13]. However, it requires a summing operation in the fast path around the quantizer. This can be implemented with a separate summing amplifier or with capacitive feed-forward paths to the third integrator. The former often degrades energy efficiency due to the need for an additional wide-bandwidth amplifier. For the latter, the speed of the third integrator's amplifier will limit the speed of the loop filter's fast path and thus compromise stability. Preventing this would require a faster amplifier, which would consume more power [14]. A more efficient approach is to insert resistors, R_{z1-3} in series with the integration capacitors $C_{\text{int}1-3}$, so as to improve their phase margin around F_s. The capacitors $C_{\text{ff}1-3}$ and $C_{\text{int}3}$ also need to be small to ensure that their parasitics do not impact the summing bandwidth. This is achieved by implementing the second and third integrators with large input resistances ($R_{i2-3} = 3.45$ MΩ), and small integration capacitors ($C_{\text{int}2} =$ 220 fF and $C_{\text{int}3} = 150$ fF) in order to reduce the loading of their respective amplifiers and, simultaneously, optimize area. The small value of $C_{\text{int}3}$ allows the use of small feed-forward capacitors ($C_{\text{ff}1} = 150$ fF and $C_{\text{ff}2} = 250$ fF), and hence further reduces the capacitive loading of their respective amplifiers. These techniques make it possible to reuse the third integrator as a summing block without compromising its power efficiency.

B. Capacitively Coupled Pseudo-Differential Amplifier

In contrast to SC integrators, in which charge is transferred in exponentially decaying pulses, and only the result at the end of the integration period matters, the charge transfer in a CT integrator is a continuous process. The linearity of this process depends on the linearity of the integrator's amplifier. In a CIFF loop filter, the first integrator's linearity is the most critical. This is often realized with a fully differential amplifier [see Fig. 5(a)] [3]–[5]. As discussed in [15], the linearity of a fully differential amplifier, however, is worse than that of its pseudo-differential counterpart [see Fig. 5(b)]. This is because the fixed tail current makes the amplifier's transconductance (g_m) compressive. However, removing the tail current source makes a pseudo-differential amplifier difficult to bias robustly. The dynamic biasing techniques proposed for SC designs [1], [15], [16] are not suitable for CT operation. Furthermore, pseudo-differential amplifiers usually suffer from poor power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) [1].

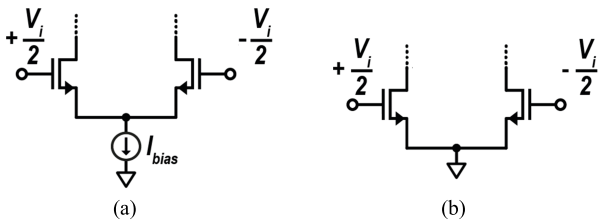

Fig. 5. (a) Fully differential and (b) pseudo-differential input amplifier.

Chopping is often employed to reduce $1/f$ noise in audio CTDSMs. In this article, we propose a capacitively coupled inverter-based pseudo-differential amplifier incorporating chopping. As shown in Fig. 6, it uses ac coupling capacitances (C_c) and large resistors ($R_b = 3$ MΩ) to bias its input transistors at the desired current levels and simultaneously block input common-mode variations. The biasing voltages (V_{bni}, V_{bpi}, V_{bnc}, and V_{bpc}) are generated by a constant-g_m biasing circuit, which is not shown for simplicity.

The combination of R_b andC_c behaves like a high-pass input filter. Setting its corner frequency below the audio band (<20 Hz) would require extremely large resistors and/or capacitors making this approach impossible to integrate. Instead, choppers are used to up-modulate audio signals to F_{chop} before this filter and then to demodulate them back

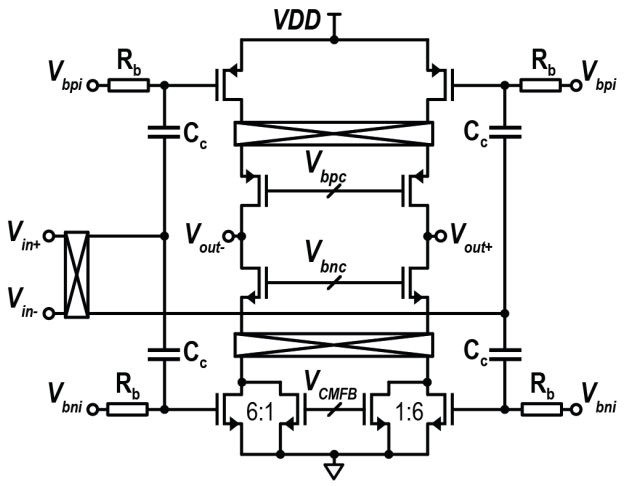

Fig. 6. Simplified schematic of the proposed amplifier.

into an output dc current. In this way, the high-pass filter's corner frequency only has to be lower than F_{chop}. To avoid down-converting the quantization noise present at the virtual ground node, the choppers are driven at the sampling frequency ($F_{\text{chop}} = F_S$) [7], [11]. Since the output choppers are placed in a high bandwidth node between the input devices and the cascodes, the dc gain reduction due to these is negligible.

For linearity, the coupling capacitors ($C_c = 2$ pF) are implemented as metal fringe capacitors and designed to be much larger than the gate capacitances of the input transistors to minimize signal attenuation. The polysilicon biasing resistors ($R_b = 3$ MΩ) are chosen to ensure that the high-pass corner frequency is much less than F_S. In the layout, R_b is placed under C_c to reduce the total area of the four R_b–C_c pairs to 0.01 mm^2.

The NMOS input transistors are split in a 6:1 ratio, with the smaller branch being used for common-mode feedback (CMFB). A CT CMFB circuit is used to sense and stabilize the amplifier's output common-mode voltage [17]. The input and output choppers also chop the offset and low-frequency noise contributed by the CMFB loop itself.

Simulations were made to compare the linearity of the proposed amplifier with that of its fully differential counterpart. Both the amplifiers are biased in weak inversion, have the same I_{bias} and device sizing, and thus have the same power consumption and g_m. In Fig. 7, the nonlinear components of their differential output currents are shown after being normalized to I_{bias}. It can be seen that the proposed capacitively coupled pseudo-differential amplifier is much more linear than its fully differential counterpart. In fact, it requires 2× less power for the same linearity. A detailed analysis of the linearity of both amplifiers is given in the Appendix.

The total power consumption of the amplifier is 205 μW, including the chopper drivers, biasing, and CMFB circuits. Its nominal and minimum dc gains are 60 and 55 dB, respectively, over process, voltage and temperature (PVT) (−55 °C–150 °C and 1.6–2 V), as shown in Fig. 8. The amplifier's simulated CMRR is greater than 70 dB up to 1 kHz. Its simulated PSRR is greater than 100 dB up to 1 kHz and greater than 50 dB for higher frequencies due to chopping.

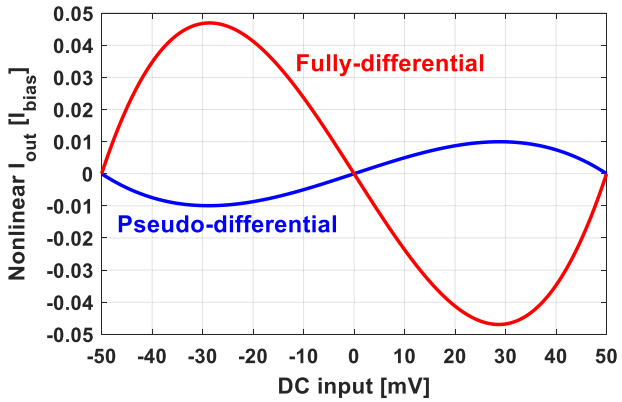

Fig. 7. Nonlinear components of I_{out} for a fully differential and pseudo-differential amplifiers.

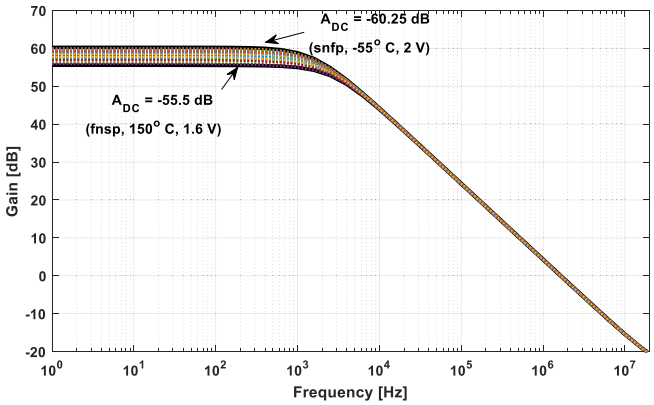

Fig. 8. OTA gain over PVT.

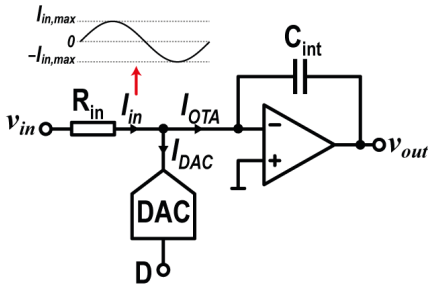

Fig. 9. I_{DAC} and I_{OTA} for NRZ and RZ DACs.

C. DAC

The DAC of the zoom ADC is one of its most critical blocks, as it directly impacts its total input-referred noise, total harmonic distortion (THD), and clock jitter sensitivity. An NRZ DAC is preferred for high energy efficiency and low jitter sensitivity. The input voltage is converted to a current (I_{in}) via R_{in}, as shown in Fig. 9. After subtracting the DAC current (I_{DAC}), their difference (I_{OTA}) is then integrated. The maximum value of I_{OTA} defines the output current requirements of the OTA and hence its power consumption. The maximum input current ($I_{\text{in,max}}$) for a sinusoidal input with amplitude $V_{\text{in,max}}$is

$$I_{\text{in,max}} = \frac{V_{\text{in,max}}}{R_{\text{in}}}. \tag{4}$$

Fig. 10 shows I_{OTA} and I_{DAC} for NRZ and RZ DACs for a zoom ADC based on a 3-bit coarse ADC. For an NRZ DAC,

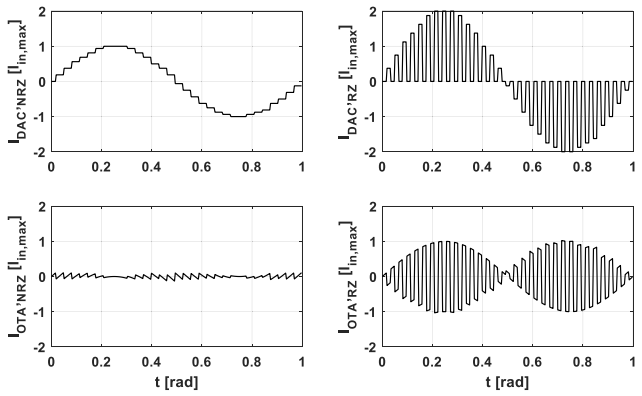

Fig. 10. I_{DAC} and I_{OTA} for NRZ and RZ DACs.

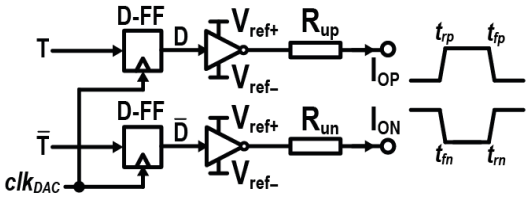

Fig. 11. Schematic of an R-DAC cell.

the difference between I_{in} and I_{DAC} is constant and decreases as the resolution of the coarse DAC is increased. For an RZ DAC, however, this difference is much larger, since I_{DAC} is sometimes zero, and so I_{OTA} should be as large as $I_{\mathrm{in,max}}$. Moreover, the jitter sensitivity of an NRZ DAC is considerably better than that of an RZ DAC.

There are two ways to implement a two-level NRZ DAC: as a current DAC (I-DAC) or as an R-DAC. However, an IDAC will generate extra distortion due to the interaction between the nonlinear output impedance of its current sources and the voltage swing at the virtual ground of the OTA. An R-DAC is not only more linear, but it also has lower thermal and $1/f$ noise [18]. Thus, an R-DAC is used in this article.

ISI refers to the signal-dependent errors that occur at code transitions due to the finite rise/fall times of the currents generated by the unit elements of the R-DAC. The use of DWA makes this problem even worse because it increases the number of unit element transitions in the DAC and introduces even-order distortion [10]. In this article, a novel ISI reduction technique is proposed to solve this problem.

In the output of the differential R-DAC unit element shown in Fig. 11, there are four different transition edges: t_{rp}, t_{rn}, t_{fp}, and t_{fn}. If the total amount of positive and negative DAC output currents within one period would match, there would be no nonlinear ISI error [10]. One approach to achieve this is to match a rising edge with its corresponding falling edge (match t_{rp} and t_{fn}, and match t_{rn} and t_{fp}) [7], [8]. However, this is hard to guarantee in practice since the speed of the rising edges is set by PMOS drivers, while the speed of the falling edges is set by NMOS drivers. Thus, background calibration is often necessary for this approach [7], [8].

Alternatively, we note that to avoid ISI, it is only necessary to match the rising and falling edges of the positive and the negative half DACs (match t_{rp} and t_{rn}, and match t_{fp} and t_{fn}). This is comparatively easy to achieve because the edges that need to be matched are generated by the same type of devices. However, the positive and the negative DAC unit resistors also need to match, as they also influence the resulting rise and fall times. Simulations indicated that the 1% matching needed for low DWA in-band noise (IBN) is also more than enough to achieve < -120-dB HD_2. The positive and negative half DACs should then be laid out next to each other. Noting that the ON resistances of the DAC switches are much smaller than R_{up} and R_{un}, the matching requirements on the driver inverters can be relaxed to 5%. The switch driving signal asymmetry, which is also a source of ISI error, is reduced by using two separate flip-flops to drive D and $\bar{D}$, as shown in Fig. 11.

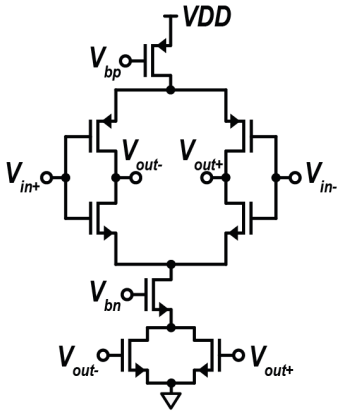

Fig. 12. Amplifiers used in the second and third integrators.

D. Amplifiers of the Second and Third Integrators

The noise and distortion specifications of the second and third integrators are relaxed by the gain preceding them. They are implemented with current-starved inverters as shown in Fig. 12, each consuming 15 μW while providing 45-dB dc gain.

E. Asynchronous SAR ADC and Alias Rejection

The asynchronous SAR ADC used in this article is similar to the one in [2], but with smaller DAC unit capacitors (1.8 fF) to reduce the peak currents drawn from the input, resulting in a total sampling capacitance of 55 fF.

Due to its input sampler, the asynchronous SAR ADC could alias the signals around F_S back to dc. This could be prevented by utilizing an all-pass filter [19]. However, the passive elements required to implement an all-pass filter for the chosen F_S would occupy a large area. In this article, we propose to use a simple first-order *RC* low-pass filter as shown in Fig. 4 to suppress the signal components around F_S instead. Simulations showed that $R_{\mathrm{filt}} = 20$ kΩ and $C_{\mathrm{filt}} = 5$ pF are enough to achieve better than 65-dB alias rejection around F_S.

IV. Measurement Results

As shown in Fig. 13, the prototype CT zoom ADC occupies 0.27 mm^2 in a 160-nm CMOS technology. The input resistors, R-DAC, loop filter, SAR ADC, and digital logic occupy 18%, 18%, 53%, 4%, and 7% of the total area, respectively.

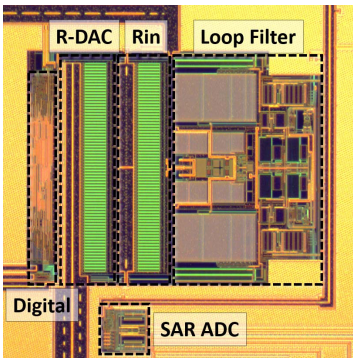

Fig. 13. Chip micrograph.

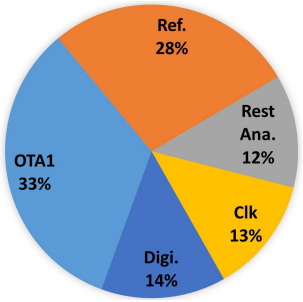

Fig. 14. Power breakdown.

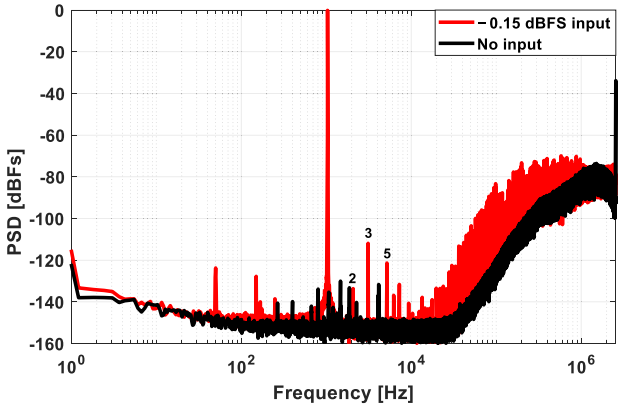

Fig. 15. Measured output spectrum (−0.15-dBFS input signal at 1 kHz, and no signal. 2^{23} points 8 average with Hanning window).

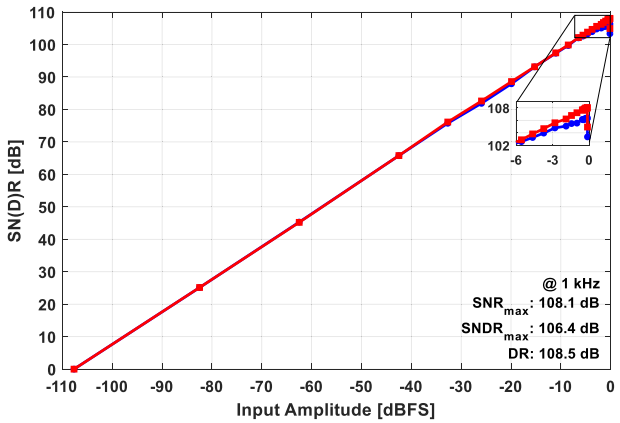

Fig. 16. Measured SNR and SNDR across input amplitude.

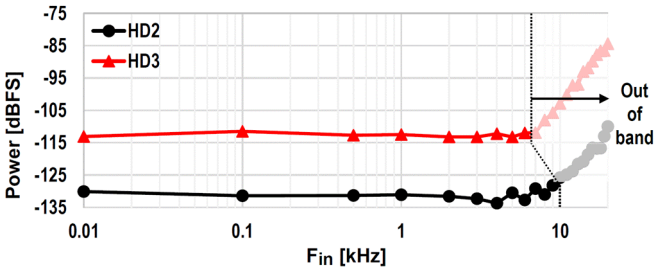

Fig. 17. HD_2 and HD_3 versus F_{in}.

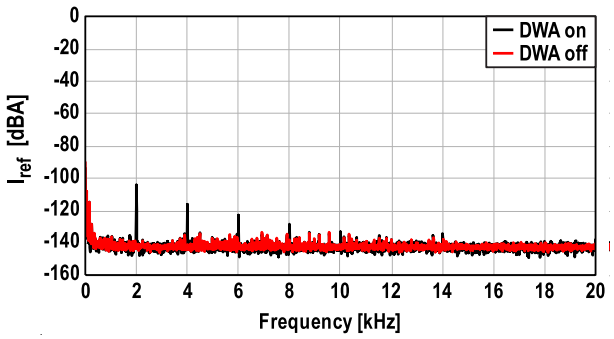

Fig. 18. Measured I_{ref} power spectrum for DWA ON and OFF.

The ADC consumes 618 μW from a 1.8-V supply. The analog, reference, clock, and digital circuitry consume 45%, 28%, 13%, and 14%, respectively, of this total power. As shown in Fig. 14, the first integrator dominates the analog power consumption. The voltage references are externally generated ($V_{ref+} = 1.8$ V and $V_{ref-} = 0$ V).

The measured output spectrum of the ADC is shown in Fig. 15. When no input signal applied ($V_{in} = 0$), the ADC effectively operates like a third-order 1-bit DSM. The in-band tones seen in this case are due to DWA. Peak SNDR is achieved with an input of −0.15 dBFS. HD_3 is the dominant distortion component at −113 dB, and all other harmonic components are below −120 dB. The tones at 50 and 150 Hz are due to the signal generator. The measured peak SNR, SNDR, and DR are 108.1, 106.5, and 108.5 dB, respectively (see Fig. 16).

Fig. 17 shows the HD_2 and HD_3 levels for −1-dBFS single-tone in-band input signals. HD_3 is lower than −113 dB and HD_2 is lower than −125 dB for all frequencies. Low HD_2 levels prove the efficacy of the proposed ISI mitigation technique. The apparent increase in HD_2 and HD_3 at higher frequencies is due to the increased quantization noise at these frequencies. The measured INL of the SAR ADC is 0.15 LSB_C.

The signal-dependent unit transitions caused by DWA make the current drawn from the reference signal-dependent [10]. To illustrate this, the current drawn from V_{ref+}, I_{ref}, is measured with an audio analyzer. The measured power spectrum of I_{ref} is shown in Fig. 18 for $F_{in} = 1$ kHz and for DWA "ON" and "OFF." It can be seen that DWA causes even-order tones

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK

	This work	JSSC'18 Jang [6]	JSSC'18 Karmakar [2]	JSSC'17 Gönen [1]	JSSC'17 Billa [7]	JSSC'16 Berti [21]	JSSC'16 Leow [22]	TCAS-I'16 Lee [16]
Architecture	**CT Zoom**	CT 1.5-Bit	SC Zoom	SC Zoom	CT FIRDAC	CT Multi-Bit	CT Multi-Bit	SC Single-Bit
Tech (nm)	**160**	65	160	160	180	160	65	180
Area (mm^2)	**0.27**	0.14	0.25	0.16	1	0.21	0.25	0.31
Supply (V)	**1.8**	1.2	1.8	1.8	1.8	1.6	1	1.8
Power (μW)	**618**	68	280	1120	280	390	800	300
F_S (MHz)	**5.12**	6.144	2	11.3	6.144	3	6.4	6.1
Bandwidth (kHz)	**20**	24	1	20	24	20	25	20
SNR (dB)	**108.1**	94.8	119.1	106	99.3	93.4	100.1	98.6
SNDR (dB)	**106.4**	94.1	118.1	103	98.5	91.3	95.2	97.7
DR (dB)	**108.5**	98.2	120.3	109	103.6	103.1	103	100.5
$FoM_{S,SNDR}$ [+] (dB)	**181.5**	179.5	183.6	175.5	177.8	170.5	170.1	175.9
$FoM_{S,DR}$ [++] (dB)	**183.6**	183.6	185.8	181.5	182.9	180.2	177.9	178.7

[+] $FoM_{S,SNDR}$ = SNDR + 10log(BW/Power) [++] $FoM_{S,DR}$ = DR + 10log(BW/Power)

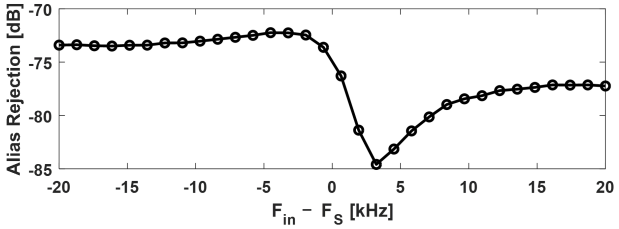

Fig. 19. Measured alias rejection properties of the CT zoom ADC.

in I_{ref}. The mixing of these even-order components with the input signal via the finite output impedance of the reference is thus the main reason for the odd-order harmonic components (HD_{3-9}) seen in Fig. 15.

The ADC's measured CMRR and PSRR at 50 Hz are greater than 70 and 100 dB, respectively, and its $1/f$ corner is lower than 20 Hz, demonstrating the performance benefits of the capacitively coupled chopped OTA. The measured alias rejection of the ADC is then higher than −72 dB for −6-dBFS input signals, as shown in Fig. 19.

Table I summarizes the performance of the proposed CT zoom ADC and compares it with that of other state-of-the-art audio ADCs. The proposed ADC outperforms all the others in terms of peak SNDR and Schreier figure of merit (FoM). Although the SC zoom ADC presented in [1] achieves a similar peak DR and SNR, it requires much stronger input drivers. The input impedance of the proposed CT zoom ADC is essentially resistive and so can be easily driven.

V. CONCLUSION

A CT zoom ADC to digitize audio signals with the state-of-the-art energy efficiency has been presented. The combination of a fast 5-bit asynchronous SAR ADC and a 5-bit NRZ DAC significantly reduced the input swing applied to a fine 1-bit CTDSM, thus significantly reducing its required linearity and power consumption. By implementing the first stage of the DSM with a highly linear capacitively coupled pseudo-differential amplifier, the ADC's energy efficiency is further improved. To reduce the potential ISI caused by its resistor DAC, a simple ISI-reducing layout technique is proposed and proven. Taken together, these techniques result in the state-of-the-art energy efficiency.

APPENDIX
LINEARITY ANALYSIS OF FULLY DIFFERENTIAL PSEUDO-DIFFERENTIAL INPUT PAIRS

In this appendix, an analysis of the input pairs shown in Fig. 5 is performed to compare their linearity. In order to not limit the analysis to only one operation region, i.e., weak, moderate, or strong inversion, the transconductance-to-current ratio (g_m/I_d)-based method in conjunction with the Enz, Krummenacher, Vittoz (EKV) model proposed in [20] is used. The drain current of a transistor in saturation

$$I_D = 2nV_{\text{T}}^2 \mu C_{\text{ox}} \frac{W}{L}(q^2 + q) \tag{5}$$

where q is the normalized mobile charge density at the source, n is the subthreshold slope, and V_T is the thermal voltage. The relationship between the gate drive voltage and q is given as

$$V_{\text{GS}} - V_{\text{TH}} = nV_T[2(q-1) + \log(q)] \tag{6}$$

where V_{TH} is the threshold voltage. g_m/I_D could be then found as [20]

$$\frac{g_m}{I_D} = \frac{1}{nV_T}\frac{1}{q+1}. \tag{7}$$

Due to the differential operation, even-order nonlinearity components will be zero. For this analysis, we will take only the third-order distortion into account. The output current then be written by using the power series expansion

$$i_d = g_{m1}v_{\text{gs}} + \frac{1}{6}g_{m3}v_{\text{gs}}^3 \tag{8}$$

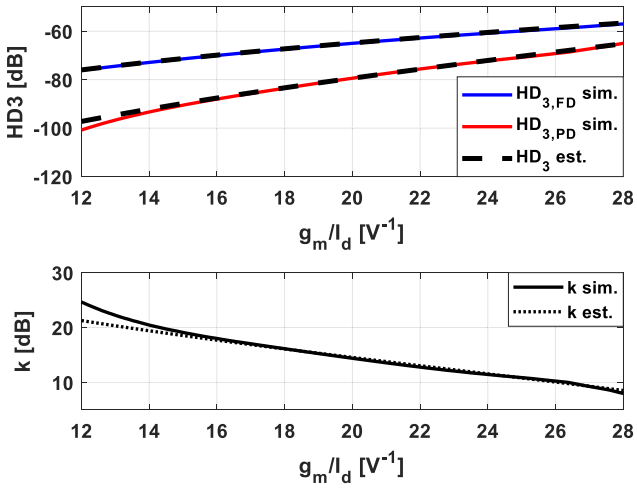

Fig. 20. HD_3 and k versus g_m/I_D for pseudo-differential and fully differential input pairs ($L = 0.7$ μm).

g_{m1} and g_{m3} are given in [20] for a common-source stage as

$$g_{m1} = I_s \left(\frac{1}{nV_T}\right) q$$
$$g_{m3} = I_s \left(\frac{1}{nV_T}\right)^3 \frac{q}{(2q+1)^3}. \quad (9)$$

HD_3 could be found for the pseudo-differential input pair shown in Fig. 19 by using (4)–(8) for a differential sinusoidal input signal with $v_{i,\text{pk}}$ amplitude

$$\text{HD}_{3,\text{PD}} \approx \frac{1}{16}\left|\frac{g_{m3}}{6g_{m1}}\right| v_{i,\text{pk}}^2 = \frac{1}{96}\left(\frac{1}{nV_T}\right)^2 \frac{1}{(1+2q)^3} v_{i,\text{pk}}^2. \quad (10)$$

The HD_3 of the fully differential input pair is found in [20]

$$\text{HD}_{3,\text{FD}} = \frac{1}{24}\left(\frac{1}{nV_T}\right)^2 \frac{(1+3q)}{2(1+2q)^3} v_{i,\text{pk}}^2. \quad (11)$$

The ratio of $HD_{3,\text{FD}}$ to $HD_{3,\text{PD}}$is then found as

$$k = \frac{\text{HD}_{3,\text{FD}}}{\text{HD}_{3,\text{PD}}} = 2 + 6q. \quad (12)$$

Using (4)–(6), we can find k in terms of g_m/I_D, n, and V_T

$$k = \frac{6}{\frac{g_m}{I_D} nV_T} - 4. \quad (13)$$

The only one process parameter required for this equation is n. g_m/I_D is a very useful design parameter that determines the achievable g_m for a given bias current I_D.

Fig. 20 shows the simulated HD_3 and k for the fully differential and pseudo-differential NMOS input pairs for different g_m/I_D values, both driven by a sinusoidal input with $v_{i,\text{pk}} = 10$ mV. The HD_3 and k values estimated by (10) and (11) after extracting $n = 1.25$ from the used 160-nm process are also shown in dashed lines. The simulated and estimated results are in good agreement, and they show that for all operation regions, the pseudo-differential pair is more linear than its fully differential counterpart. k is at least 8 dB for weak inversion (high g_m/I_D), and it increases to more than 20 dB for strong inversion (lower g_m/I_D). Note that the earlier analysis and simulations do not include the output impedance nonlinearity.

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