Design of an Active N-Path Filter for 5G mm-wave Receivers

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by

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Abstract

The fifth generation (5G) of mobile communications enables the use of millimeter-wave (mm-wave) frequencies, to allow a higher data rate and lower latency. Receivers with the ability to accurately detect a low-power desired signal, in the vicinity of large power blockers, require highly linear circuitry and a high dynamic range analog-to-digital converter (ADC). This increases the power consumption of the receiver, which is undesired, especially for mobile applications. Conventional solutions at mm-wave use a band-reject filter with a fixed center frequency, consuming a large chip area while providing no rejection to the other channels within the same frequency band. N-path filters (NPFs) have recently been used to reject interferers in adjacent channels, by using a tunable center frequency. The state-of-the-art NPFs at mm-wave only have a limited attenuation or use a large chip area.

In this thesis, a fourth-order NPF is designed for 26-30 GHz, to provide a large rejection in the adjacent channels, while requiring only a small area. Compared to higher-order NPFs at low frequencies, this filter uses a sine-wave local oscillator (LO) to eliminate the need of higher harmonics. An extensive analysis on the effect of using a sine wave, compared to a non-overlapping square wave, is performed. The implemented filter combines two frequency-shifted NPFs to create a flat in-band (IB) response and a steep roll-off, without the use of a large passive baseband filter.

The filter with 200 MHz bandwidth (BW) is designed in 40 nm CMOS. From circuit simulation, with the inductors and transformers included as electromagnetic (EM) models, a rejection of 14 dB in the center of the first adjacent channel is obtained. This increases up to 24 dB at far-out-of-band frequencies. The noise figure (NF) of 10-12 dB is the lowest of the state-of-the-art, due to the added low-noise amplifier (LNA) in front of the filter. Despite this LNA, the designed filter achieves a comparable power consumption (40 mW) and smaller area (0.2-0.3 µm) than the state-of-the-art. The IIP_3 is -4.5 dBm IB and -1.6 dBm at $\Delta f/BW_{RF}$ = 1. The IP_{1dB} is -20 dBm and the B_{1dB} is -19 dBm at $\Delta f/BW_{RF}$ = 1 and -16 dBm at $\Delta f/BW_{RF}$ = 2. The voltage gain of the filter is 10-14 dB over the designed frequency range for a supply voltage of 1.2 V.

The filter designed in this thesis is the first reported active N-path filter at mm-wave. The BW is among the smallest reported, while the estimated area is lower than the state-of-the-art. This filter achieves the lowest reported NF, combined with a large attenuation and gain. It is suggested to further reduce the NF of the filter, which allows the first stage LNA to have a smaller gain and possibly even remove its necessity. This will improve the power consumption, as well as the linearity of the filter. It is furthermore recommended to improve the attenuation in the adjacent channels by making the gain and phase of the two filter paths tunable. This increases the rejection of high power blockers, allowing for an even more power efficient receiver, which is critical for future 5G systems.

Acknowledgments

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Simon Verkleij
Delft, August 2022

Contents

1 Introduction

The fifth generation (5G) of wireless communication is approaching. Communication at millimeter-wave (mm-wave) frequencies allows for higher data rates and lower latency. 5G communication uses different frequency channels close to each other which can have large power interfering signals, while the desired signal at the main band can have a low power. A receiver that can handle these large blockers, while accurately receiving the desired low-power signal requires very linear devices and a high dynamic range analog-to-digital converter (ADC). This will consume a lot of power, making it infeasible to be implemented in mobile devices with their limited battery capacity. Power consumption can be significantly reduced by adding a filter to suppress interfering signals. In order to maintain the highest linearity, it is most beneficial to attenuate the interfering signals at an early stage in the receiver. This thesis describes the design of a mm-wave filter with a steep roll-off and tunable center frequency to attenuate interfering signals in nearby channels.

1.1. Background on mm-wave 5G

The operating bands for mm-wave 5G are defined by the 3rd Generation Partnership Project (3GPP) [1] and are visualized in Figure 1.1.

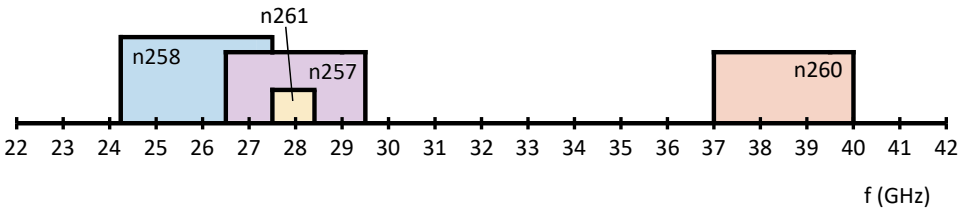


Figure 1.1: 5G mm-wave operating bands [1].

Each band is divided into channels with a BW of 50, 100, 200 or 400 MHz. It is decided to focus on the n257 band between 26 and 30 GHz, with a channel BW of 200 MHz, to demonstrate the filter. The center frequency of the filter needs to be tunable to cover this full band. The spacing between channels, the guard band, is commonly 10% of the BW. A 20 MHz guard-band is therefore used, which is larger than the minimum guard band of 4.93 MHz, as required by 3GPP [1].

According to the 5G standard, the receiver must be able to handle interfering signals with a power of 21.5 dBm above the main channel power [1]. These interfering signals are located at a distance of $F_{\text{loffset}} \geq 400.05$ MHz away from the main channel center frequency[1]. In addition to interference rejection, the standard also requires an adjacent channel selectivity (ACS) of at least 23 dB for adjacent channel powers up to -25 dBm. A desired signal must be received correctly with a blocker power which

[1] This number is calculated using the worst case subcarrier spacing (SCS) of 60 kHz in the equation $F_{\text{loffset}} = (\text{ceil}(400/\text{SCS}) + 0.5)\text{SCS}$.

is 23 dB larger. Since the ACS requirement is more strict (both in frequency offset and attenuation), the filter is designed for this specification. The filter does not need to provide the full 23 dB attenuation, since part of the rejection will be done at a later stage in the receiver (partially in the baseband and partially in the digital domain after the ADC). The amount of filtering is determined by the linearity specifications of the receiver.

The required attenuation of the filter is determined from a general mm-wave receiver, including a phase shifter used for multiple input, multiple output (MIMO) beamforming. Figure 1.2 shows the different stages of such a receiver with their expected gain and linearity [2]. The input power at 1 dB gain compression point (IP_{1dB}) is defined as the input power where the output power drops 1 dB below its expected value from the linear region. With a maximum input power of -25 dBm, the power at each stage must be lower than the IP_{1dB} of that stage. Figure 1.3 shows that the blocker power becomes larger than the IP_{1dB} at the input of the mixer. An attenuation of 10 dB before entering the mixer is required to suppress the blocker power below the IP_{1dB} level. Providing the filtering already at an earlier stage of the receiver allows for an improved linearity or a reduced power consumption of the successive stages, such as the phase shifter and low-noise amplifier (LNA).

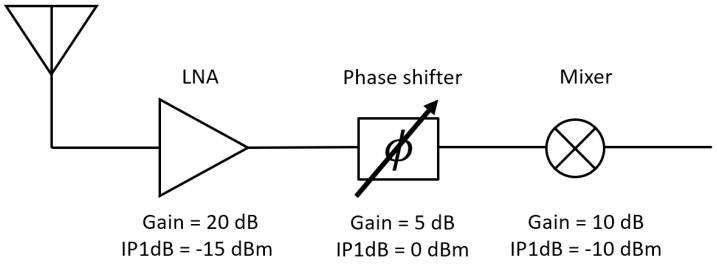


Figure 1.2: Block diagram of a general mm-wave receiver, with the expected gain and IP_{1dB} of each stage.

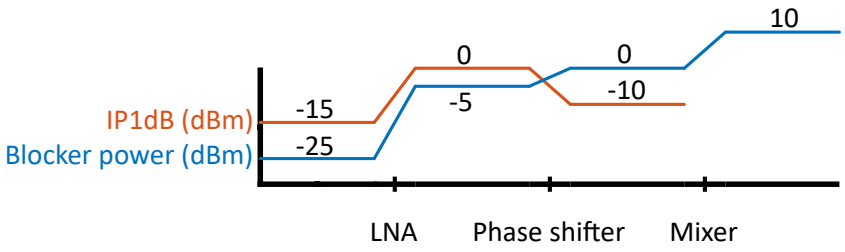


Figure 1.3: IP1dB and blocker power at each stage of the receiver.

The required filter is graphically shown in Figure 1.4. 10 dB attenuation is required at the center of the first adjacent channel, which is half a channel BW plus the 20 MHz guard band away from the main channel.

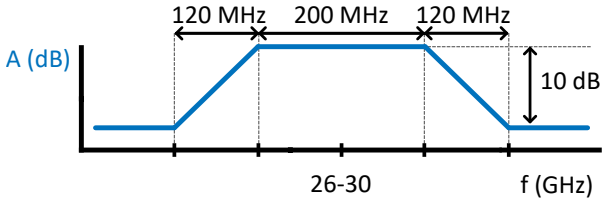


Figure 1.4: BW and attenuation requirements of the filter.

Implementing this as a passive band-pass filter around 28 GHz would require a filter order of 539, as calculated in eq. (1.1) - eq. (1.3). The derivation of these equations is included in Appendix A.1.

$$\text{Filter order LPF} = \left\lceil \frac{\Delta A_V}{20\log_{10}\left(\frac{f_{2,\text{Hz}}}{f_{1,\text{Hz}}}\right)} \right\rceil = \left\lceil \frac{10\text{ dB}}{20\log_{10}\left(\frac{28.22\text{ GHz}}{28.10\text{ GHz}}\right)} \right\rceil = 271 \tag{1.1}$$

$$\text{Filter order HPF} = \left\lceil \frac{\Delta A_V}{20\log_{10}\left(\frac{f_{2,\text{Hz}}}{f_{1,\text{Hz}}}\right)} \right\rceil = \left\lceil \frac{10\text{ dB}}{20\log_{10}\left(\frac{27.90\text{ GHz}}{27.78\text{ GHz}}\right)} \right\rceil = 268. \tag{1.2}$$

$$\text{Filter order BPF} = \text{Filter order LPF} + \text{Filter order HPF} = 539 \tag{1.3}$$

The required quality factor of the filter is

$$Q = \frac{f_c}{\text{BW}} = \frac{28\text{ GHz}}{200\text{ MHz}} = 140, \tag{1.4}$$

which cannot be implemented by a passive on-chip filter. Besides the large Q, the filter must be tunable between 26 and 30 GHz, to provide rejection in the adjacent channels. Without this tunability, a large amount of separate filters for each channel would be needed, resulting in a large area consumption, which is unpractical for mobile applications. A non-tunable filter can only be implemented as a band-select filter, rather than a channel-select filter, because of the smaller quality factor (Q = 7) and area consumption [3]. This, however, allows large blockers in adjacent channels to enter the receiver, increasing the power consumption to satisfy the linearity and dynamic range requirements. Because of the large filter order and Q, and the required tunability of the center frequency, an N-path filter (NPF) is often used in receiver architectures [4–12].

1.2. Research objective

In order to reduce the power consumption of a mm-wave 5G receiver, out-of-band (OOB) blockers should be filtered out at an early stage. The goal of this research is to design an N-path filter with a tunable center frequency (f_c) between 26 and 30 GHz, which suppresses blockers in the adjacent channels by at least 10 dB. An overview of the requirements is provided in Table 1.1.

Table 1.1: Requirements for the NPF.

Specification	Value
f_c	26-30 GHz
$\text{BW}_{\text{-3dB}}$	200 MHz
Attenuation	10 dB (at 120 MHz away from main band edge)
Noise figure	$\leq$ 8 dB
Power consumption	$\leq$ 50 mW
IIP_3	$\geq$ -10 dBm
IP_{1dB}	$\geq$ -25 dBm
S_{11}	$\leq$ -10 dB

1.3. System overview

A top-level diagram of the designed filter is shown in Figure 1.5. This consists of a filter in the second stage and an LNA in the first stage, which is needed to suppress the noise of the filter. The filter is implemented by two active NPFs with a frequency offset, which are combined to improve the attenuation. The design of each sub-circuit is described in a separate chapter.

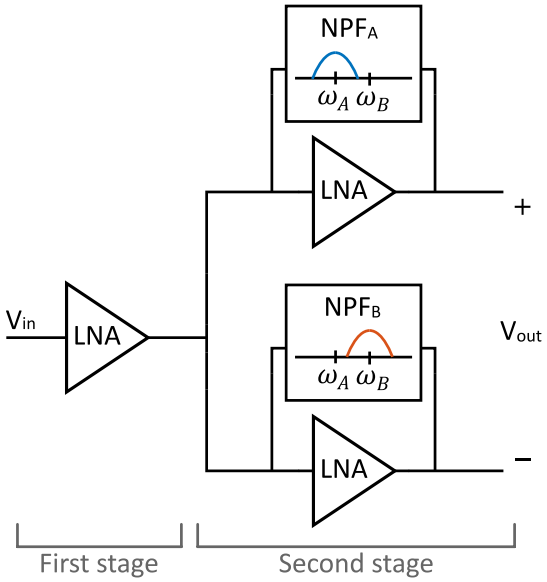


Figure 1.5: System overview of the designed filter.

1.4. Thesis outline

This thesis is structured as follows. Chapter 2 starts with an introduction on NPFs and derives their equivalent model. The challenges of operating an NPF at mm-wave are discussed, one of which is using a clock signal that does not require harmonic components at high frequencies. A standalone NPF shows limited attenuation, which is why an LNA is added to create a gain-boosted N-path filter (GB-NPF) in Chapter 3. The filter roll-off and ultimate rejection can be improved by combining two filters with a frequency offset, as discussed in Chapter 4. Chapter 5 presents the design of the first stage LNA, after which the layout of the individual components is designed in Chapter 6. The full circuit and its simulation results are included in Chapter 7. The project is concluded in Chapter 8, which also contains a discussion and provides recommendations for future work.

1.5. Original contributions

The following contributions are made to the research on NPFs.

- Analysis of using a sine wave local oscillator (LO) to operate an NPF at mm-wave without the need for higher harmonics (Chapter 2);
- Design of the first active NPF at mm-wave (Chapter 3);
- Design of the smallest reported higher order NPF at mm-wave (Chapter 4).

2

Mm-wave N-path filter

A band-pass filter (BPF) with a narrow BW is needed to suppress interfering signals close to the desired channel. Instead of implementing one filter per channel, which would consume a large amount of area, a filter with a tunable center frequency is used. An NPF can offer this tunability, in combination with a small BW, and is therefore commonly used in receiver architectures [4–12]. This chapter explains the operation and discusses the limitations of NPFs implemented at mm-wave. First, the operation of a general NPF is explained in Section 2.1, after which Section 2.2 presents the challenges at mm-wave frequencies and discusses how to design with these challenges.

2.1. Operation of an N-path filter

An NPF works by converting an impedance at baseband to radio frequency (RF), as shown in Figure 2.1.

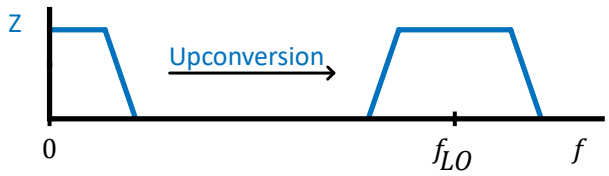


Figure 2.1: An NPF converts a baseband impedance to RF.

The shape of the baseband filter determines the shape of the filter at RF. This makes it possible to create a high-Q filter at RF by using only low-Q components at baseband. In order to generate a BPF at RF, the baseband filer must be a low-pass filter (LPF). This is often implemented by a shunt capacitor [4, 7, 8, 10, 13–18], as shown in Figure 2.2. Together with the on-resistance of the mixer switches, this capacitor forms an RC LPF.

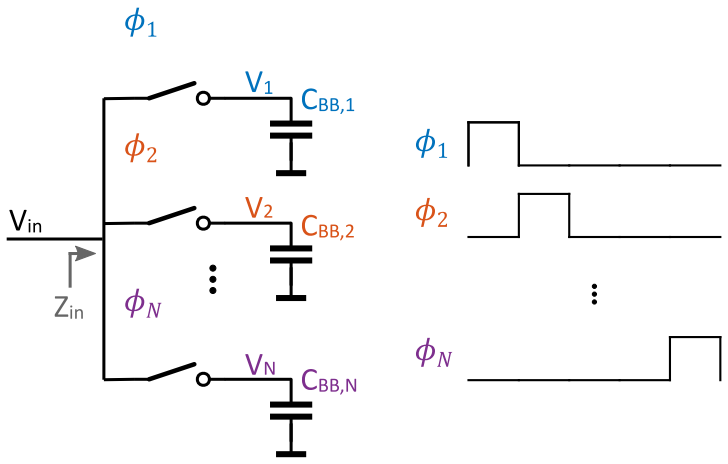


Figure 2.2: N-path filter with timing diagram.

Converting the baseband filter up to RF is realized by N mixing transistors, as shown in Figure 2.2. These switches are controlled by non-overlapping square-wave clock signals $\phi_1 - \phi_N$. The frequency of these clock signals, f_{LO}, determines the center frequency of the BPF at RF. Adjusting f_{LO} changes the center frequency, which makes the NPF tunable. The BW of the BPF is determined by the switch resistance R_{sw}, and the baseband capacitance C_{BB}. This can be approximated by eq. (2.1) [19]. A larger N reduces the time that each path is connected to the input node, thereby effectively increasing R_{sw} by a factor N.

$$BW_{-3dB} = \frac{1}{\pi N R_{sw} C_{BB}} \tag{2.1}$$

The operation of the NPF of Figure 2.2 can be explained with the transient voltages in Figure 2.3. Assume a sine-wave input voltage at $f_{RF} = f_{LO}$, as shown in Figure 2.3a. When switch 1 is closed ($\phi_1 = 1$), the input voltage charges $C_{BB,1}$, causing V_1 to increase, as shown in Figure 2.3b. This voltage stays constant for the rest of the clock period ($\phi_1 = 0$) and get charged again when switch 1 is closed. Since $f_{RF} = f_{LO}$, the same voltage of the input sine wave is sampled on $C_{BB,1}$ every clock cycle. After a number of cycles, V_1 is increased to V_{in} and the charge on $C_{BB,1}$ is kept constant.

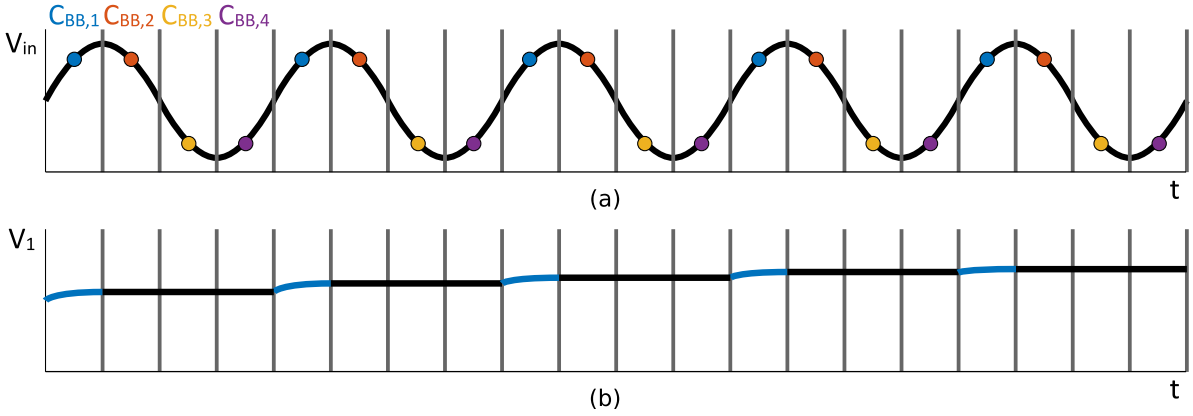


Figure 2.3: (a) Input voltage at $f_{RF} = f_{LO}$, with the sampling moments of each capacitor indicated by the colored dots. (b) The voltage on capacitor C_{BB1}, which increases when C_{BB1} is connected to the input and stays constant when the other capacitors are connected to the input.

When $f_{RF} \neq f_{LO}$, however, a different voltage gets sampled every clock cycle. This prevents a large voltage on the capacitor from building up, and only causes a small fluctuating baseband voltage. An example is shown in Figure 2.4, where $f_{RF} = f_{LO}/2$. The capacitor voltage increases in the first clock cycle, but decreases in the second. This pattern repeats, thereby allowing only a small voltage ripple

to exist on the capacitors. This causes the attenuation of the NPF for frequencies outside the main band.

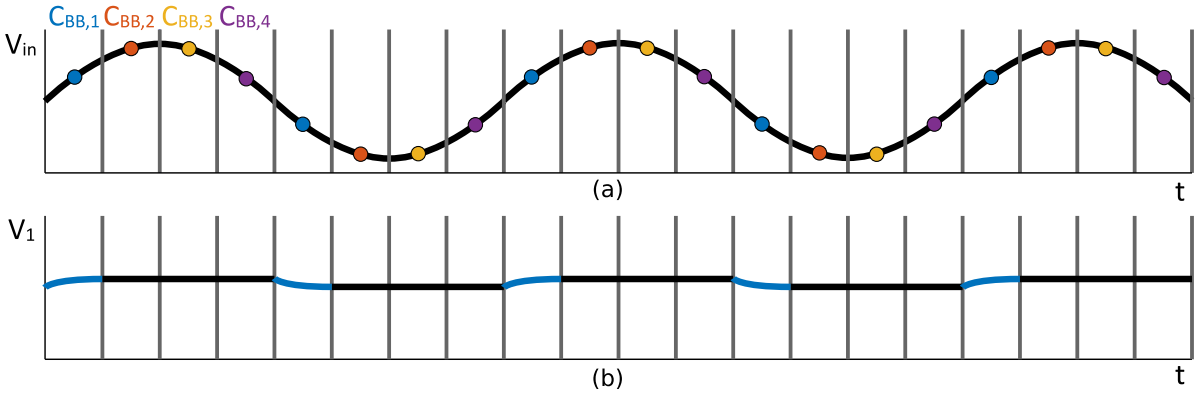


Figure 2.4: (a) Input voltage at $f_{RF} = f_{LO}/2$, with the sampling moments of each capacitor indicated by the colored dots. (b) The voltage on capacitor C_{BB1}, which increases and decreases depending on the sampled voltage.

2.1.1. Equivalent circuit

To better understand the operation and limitations of an NPF, an equivalent circuit is used. An NPF can be connected as a BPF or as a band-stop filter (BSF), as shown in Figure 2.5. The NPF has a large in-band (IB) and a small OOB impedance. Connecting the filter as a BPF provides a low-impedance path to ground at the undesired frequencies, thereby filtering out everything except the desired band [7, 8, 14, 15]. The BSF makes use of the large IB impedance of the NPF, by connecting it in series between the antenna en the receiver input [4, 8, 10–12, 16–18, 20]. This BSF is used inside a GB-NPF to again create a BPF, as will be discussed in Chapter 3. The corresponding equivalent circuits of the BPF and BSF are shown in Figure 2.5.

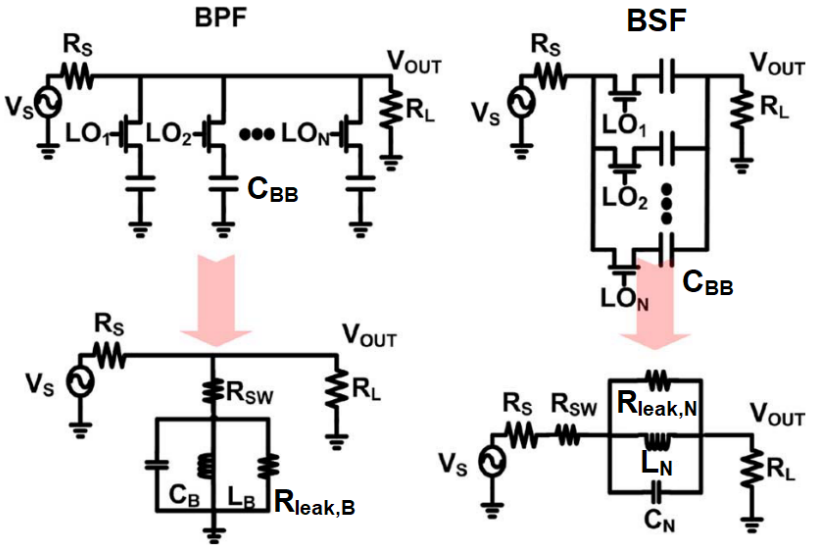


Figure 2.5: N-path BPF and BSF and equivalent RLC models [10].

The BPF is modeled around f_{LO} by a parallel RLC circuit in series with a switch resistance of the N-channel metal-oxide-semiconductor (NMOS), R_{sw}. Since only one NMOS will be turned on at the same time, the switch resistance of one NMOS is used for R_{sw}. The values of $R_{leak,B}$, C_B and L_B, for a duty cycle of $D = 1/N$, can be obtained as follows [10, 17, 21],

$$R_{leak,B} \approx \frac{2N\left(1-\cos\left(\frac{2\pi}{N}\right)\right)R_S + \frac{8\pi^2}{N}R_{sw}}{\frac{4\pi^2}{N} - 2N\left(1-\cos\left(\frac{2\pi}{N}\right)\right)}, \tag{2.2}$$

$$C_B = \frac{\pi^2}{MN \sin^2\left(\frac{\pi}{N}\right)} C_{\text{BB}}, \text{ and} \tag{2.3}$$

$$L_B = \frac{1}{(2\pi f_{\text{LO}})^2 C_B}, \tag{2.4}$$

where M is 2 for a single-ended circuit and 8 for a differential implementation. The equivalent circuit of the BSF is made with the same components, but the value of the resistor $R_{\text{leak,N}}$ is different from $R_{\text{leak,B}}$.

$$R_{\text{leak,N}} \approx \frac{\sin^2\left(\frac{\pi}{N}\right)}{\left(\frac{\pi}{N}\right)^2 - \sin^2\left(\frac{\pi}{N}\right)} \left(R_S + R_L + R_{\text{sw}}\right), \tag{2.5}$$

$$C_N = \frac{\pi^2}{MN \sin^2\left(\frac{\pi}{N}\right)} C_{\text{BB}}, \text{ and} \tag{2.6}$$

$$L_N = \frac{1}{(2\pi f_{\text{LO}})^2 C_N}. \tag{2.7}$$

At f_{LO}, the capacitor and inductor in both models resonate out and only R_{sw} and the leakage resistance R_{leak} ($R_{\text{leak,B}}$ or $R_{\text{leak,N}}$) remains. The IB impedance of the filter is thus $Z_{\text{IB}} = R_{\text{sw}} + R_{\text{leak}}$. Far OOB, the capacitor or inductor provides a short, resulting in a filter impedance of $Z_{\text{OOB}} = R_{\text{sw}}$, as shown in Figure 2.6.

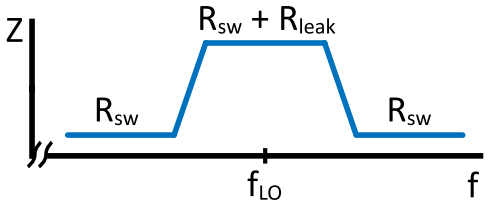


Figure 2.6: IB and OOB impedance of the NPF.

The attenuation of a BPF is caused by the difference in input impedance IB and OOB. Assuming $R_L \gg R_{\text{sw}} + R_{\text{leak}}$ (Figure 2.5), this attenuation is calculated from the voltage division between the source impedance Z_S and the input impedance of the receiver Z_{in}.

$$\text{Attenuation [dB]} = 20 \log_{10} \left[\frac{\left(\frac{|Z_{\text{in,IB}}|}{R_S + |Z_{\text{in,IB}}|}\right)}{\left(\frac{|Z_{\text{in,OOB}}|}{R_S + |Z_{\text{in,OOB}}|}\right)} \right] \tag{2.8}$$

Using the impedances from Figure 2.6, this is equal to

$$\text{Attenuation [dB]} = 20 \log_{10} \left(1 + \frac{R_S R_{\text{leak}}}{R_{\text{sw}} \left(R_S + R_{\text{sw}} + R_{\text{leak}}\right)}\right), \tag{2.9}$$

which, assuming the IB impedance is matched to the source impedance, can be rewritten as

$$\text{Attenuation [dB]} = 20 \log_{10} \left(1 + \frac{R_{\text{leak}}}{2R_{\text{sw}}}\right). \tag{2.10}$$

A small R_{sw} and a large R_{leak} are required to achieve a large attenuation. A small switch resistance can be obtained by increasing the size of the NMOS This however also decreases R_{leak}, as shown in eq. (2.2) and eq. (2.5). Larger NMOS transistors also result in a larger LO power consumption.

2.1.2. Number of paths

The number of paths in an NPF has an effect on the harmonic rejection, as well as the attenuation of the filter. Because of the harmonic components in the square-wave LO, a large NPF impedance is not only obtained at the desired frequency f_{LO}, but also at its harmonics, as shown in Figure 2.7. The components at the (N-1)th and (N+1)th harmonic fold back to f_{LO}. A large number of paths increases the frequency of these harmonics and thereby reduces the chance of high power signals folding back [7, 17, 22].

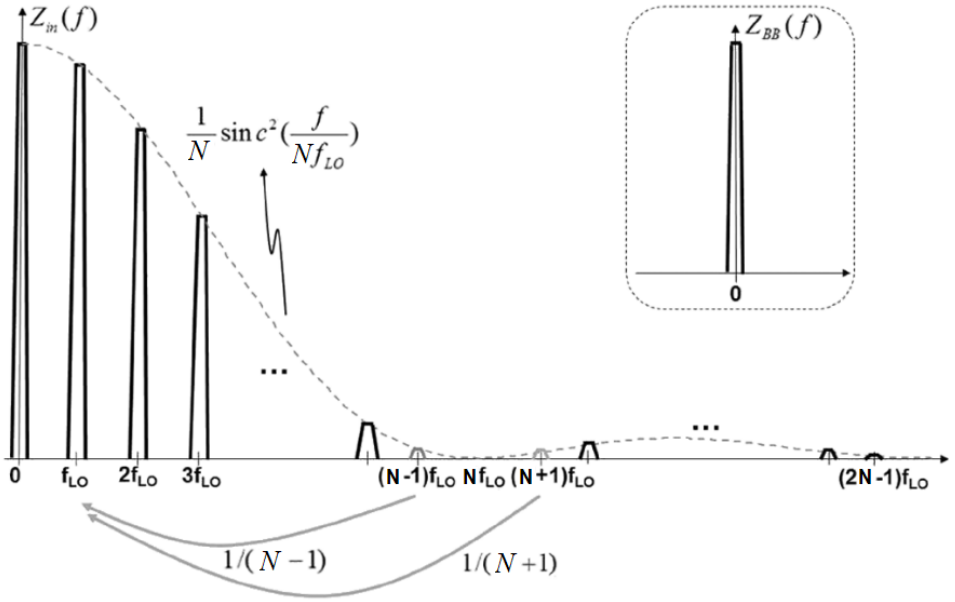


Figure 2.7: Input impedance of a band-pass NPF with N paths [22]. The components at the (N-1)th and (N+1)th harmonic fold back to f_{LO}.

Besides increasing the frequency that folds back onto the desired signal, a larger number of paths also improves the attenuation. For a larger number of paths, the calculated leakage resistance ($R_{leak,B}$ in the BPF and $R_{leak,N}$ in the BSF) increases, as shown in Figure 2.8. A larger leakage resistance for a constant R_{sw} results in a larger attenuation, according to eq. (2.10).

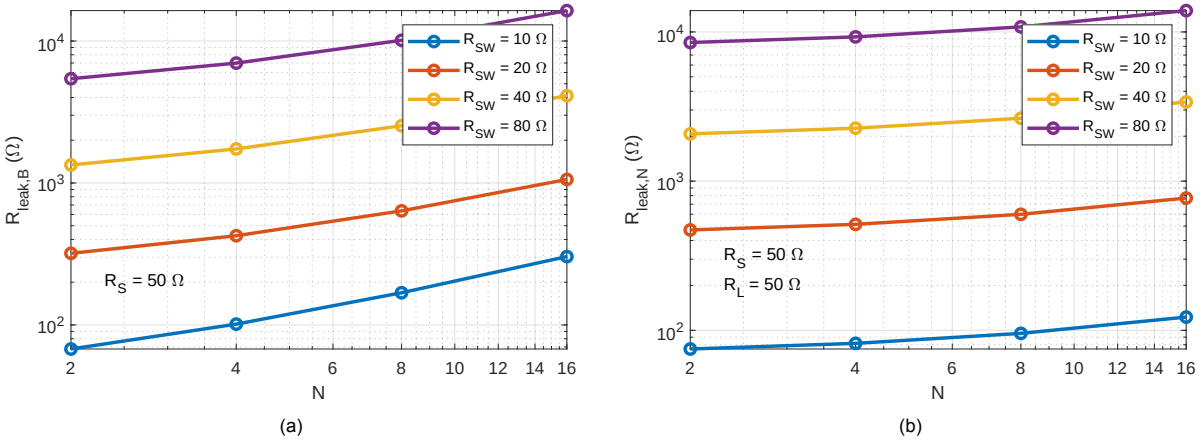


Figure 2.8: The calculated dependency of (a) $R_{leak,B}$ and (b) $R_{leak,N}$ on the number of paths N, for different R_{sw}.

Besides these advantages, a larger number of paths requires a smaller clock duty cycle, thereby increasing the complexity and power consumption of the clock generation circuitry. The extra switching transistors furthermore increase the total load connected to the clock circuitry, thereby increasing the power consumption even further.

2.2. Mm-wave challenges in N-path filters

An NPF at mm-wave cannot be operated by a 25% duty cycle square-wave LO, because of the required higher harmonics. Instead, a sine-wave LO can be used, since it only requires the fundamental frequency component [6, 13]. This section describes the challenges arising from using a sine wave and compares this LO with the traditional non-overlapping square wave.

2.2.1. Sine-wave LO

Compared to a 25% duty cycle square wave, using a sine wave as an LO signal poses two main challenges. First, the sine waves of the four paths are overlapping, as shown in Figure 2.9. This results in charge sharing between the baseband capacitors of different paths. Secondly, the LO voltage gets below its maximum during a part of the period, resulting in an increased R_{sw}.

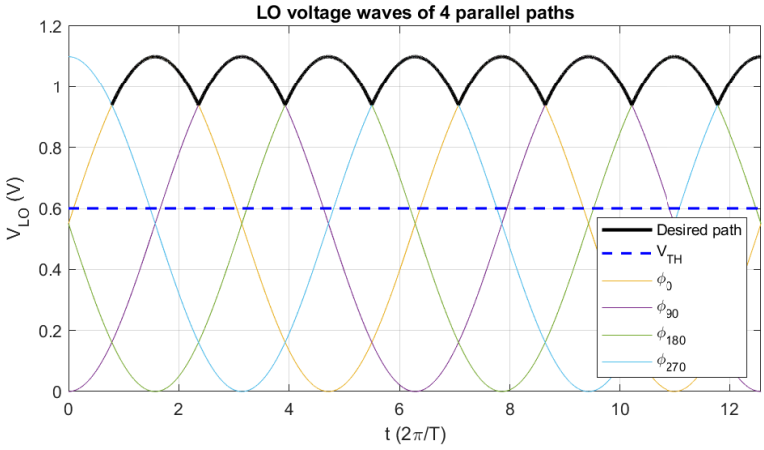


Figure 2.9: A quadrature sinusoidal LO signal results in overlap.

One method to reduce the overlap is by increasing the NMOS threshold voltage V_{TH}. This, however, increases R_{sw}, due to a decreased $V_{GS} - V_{TH}$ and thereby results in more noise and a worse linearity [23]. The LO overlap can also be reduced by connecting two 2-path filters in series, as shown in Figure 2.10 [13]. Each 2-path filter uses two 50% duty cycle LO signals, which due to the AND function of the two filters results in a similar operation as the 4-path filter with a 25% duty cycle. These 50% square-wave signals can be replaced by sine waves to operate at higher frequencies.

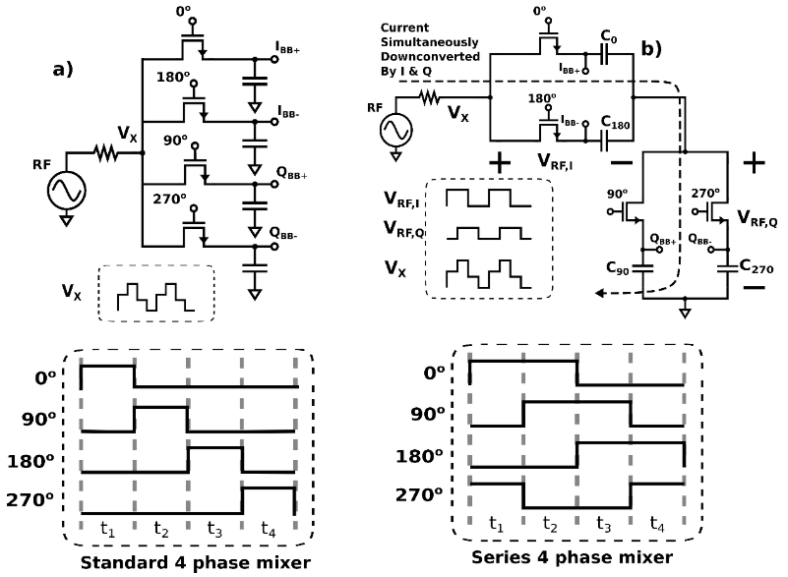


Figure 2.10: (a) 4-path filter operated by a 25% duty cycle LO. (b) The same V_X can be obtained with two stacked NPFs, controlled by 50% duty cycle LO signals [13].

While the two stacked NPFs (2x2-path NPF) can reduce the phase overlap for a square-wave LO, the inherent voltage variation of a sine wave already reduces the overlap between the phases. The mm-wave 4-path NPFs of [6] and [9] use four sine-wave LO signals. These sine waves overlap, but the on-resistance of the NMOS transistors is strongly dependent on the gate-to-source voltage (V_{GS}). At the peak of a sine wave, the desired path has a V_{GS} of 1.1 V. Two of the undesired paths at this point have a V_{GS} of 0.55 V and the last V_{GS} is 0 V.

The on-resistance versus V_{GS} of a 40-nm NMOS transistor with a width of 22 µm, simulated in Cadence, is shown in Figure 2.11a. From this simulation, the resistance of the desired path and the three parallel undesired paths is calculated and shown in Figure 2.11b. At the peak of the sine-wave LO, the desired path has a resistance of 66 Ω, while the parallel undesired paths have a total resistance of 570 Ω.

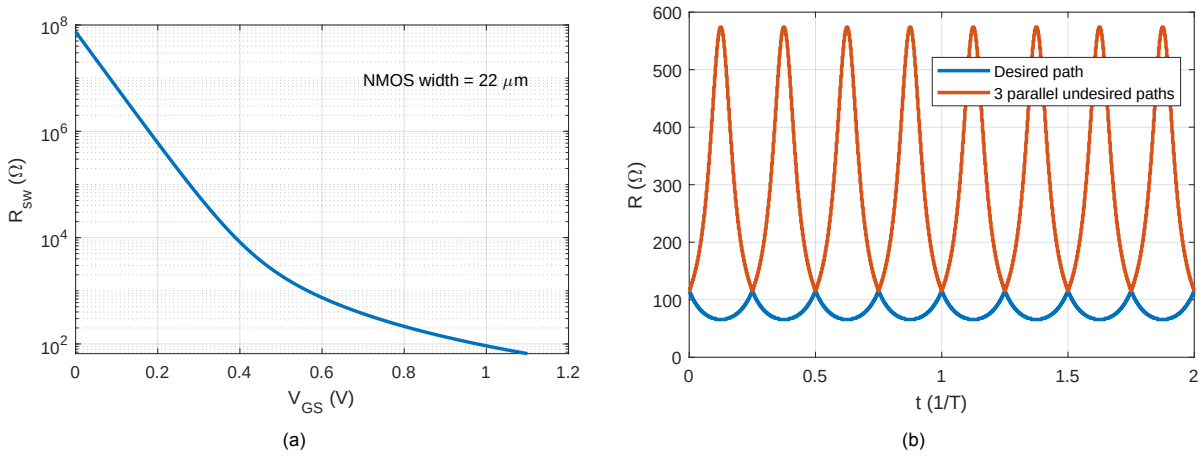


Figure 2.11: (a) Simulated on-resistance of a 40-nm NMOS transistor with a width of 22 µm, for different values of V_{GS}. (b) Calculated NMOS on-resistance of the desired path and the three parallel undesired paths for a 4-path NPF. The simulated resistance from (a) is used for this calculation.

Besides these two disadvantages, using an LO without higher harmonics has the advantage of eliminating the noise folding from these harmonics, which, for a square-wave LO, is shown in Figure 2.7.

2.2.2. Impedance comparison

The effect of a sine-wave LO is further investigated by comparing the impedance of different NPFs. The ratio between the IB and OOB impedance must be large to obtain a large attenuation. This ratio is compared for a 4-path filter with a square-wave LO, a 4-path filter with a sine-wave LO and a 2x2 path filter operated by a sine LO. Their impedance is measured by connecting the output to ground and simulating the input impedance, as shown in Figure 2.12.

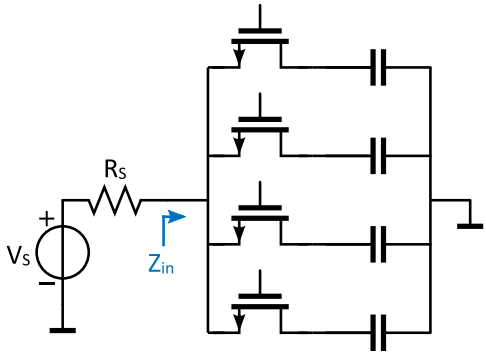


Figure 2.12: Circuit to simulate input impedance of the NPF.

The resulting impedance ratios for different input bias voltages are shown in Figure 2.13a. This impedance ratio can be approximated by

$$\frac{Z_{\text{IB}}}{Z_{\text{OOB}}} = \frac{R_{\text{sw}} + R_{\text{leak}}}{R_{\text{sw}}}. \tag{2.11}$$

The input impedance for the optimum input bias voltages is compared in Figure 2.13b.

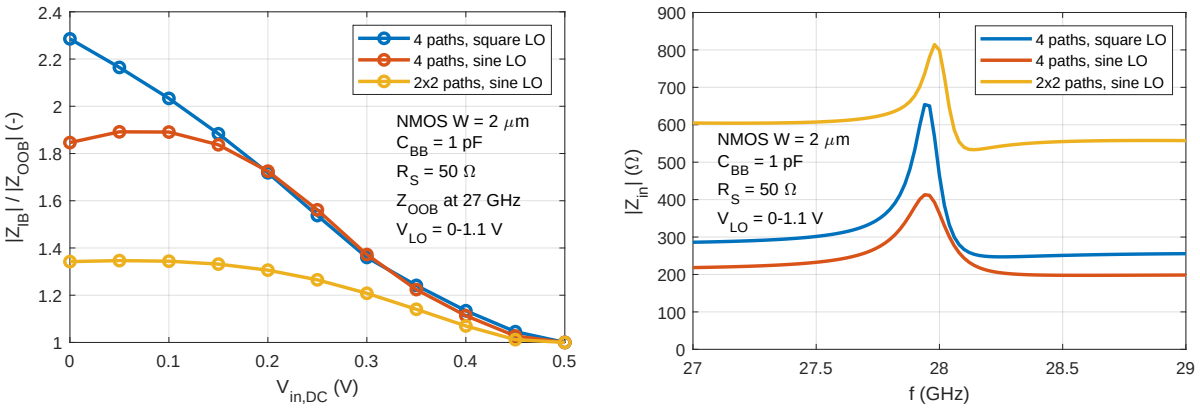


Figure 2.13: Comparison of NPF impedance of the 4-path filter with square-wave and sine-wave LO and the 2x2-path filter with sine-wave LO. (a) Simulated ratio between IB impedance (maximum impedance, around 28 GHz) and OOB impedance (at 27 GHz) for different input bias voltages. (b) Simulated impedance for an input bias voltage of 0 V for the square-wave LO and 50 mV for the two sine-wave LO filters.

From Figure 2.13a, it can first of all be seen that the largest ratio is achieved by the 4-path filter with square-wave LO. The impedance ratio decreases for a larger bias voltage, since this decreases V_{GS} and therefore increases R_{sw} while not changing R_{leak}. For the sine wave operated 4-path filter, however, the maximum impedance ratio is achieved for a bias voltage of 50 mV. Here, a large V_{GS} at the peak of the sine wave also decreases R_{sw}. There is however an optimum, since a large V_{GS} also results in multiple paths being turned on at the same moment, thereby decreasing R_{leak}. The 2x2-path filter has the smallest ratio between IB and OOB impedance and will therefore result in the smallest attenuation. This can be explained with the NPF model and calculated impedances in Figure 2.8a. A smaller number of paths reduces R_{leak} for a constant R_{sw}, thereby reducing the IB to OOB impedance ratio.

Figure 2.13b compares the input impedance of each filter for the optimum $V_{\text{in,DC}}$. The decrease in R_{leak} of the sine-wave LO filters compared to the square-wave LO filter, is clearly visible by the reduced difference between Z_{IB} and Z_{OOB}. The approximate doubling of R_{sw} in the 2x2-path filter can be seen by the increase in Z_{OOB}. The center frequency of all filters is shifted down compared to f_{LO} (28 GHz), due to the parasitic capacitances of the NMOS transistors [14]. This will however be compensated for by the frequency shifting mechanism as will be discussed in Chapter 4.

The effect of the switch width on the input impedance is also investigated. The width is increased by enlarging the number of fingers for a constant unit transistor width of 2 µm. Figure 2.14a shows the reduced IB and OOB impedance for an increased switch width of the 4-phase filter with sinusoidal LO.

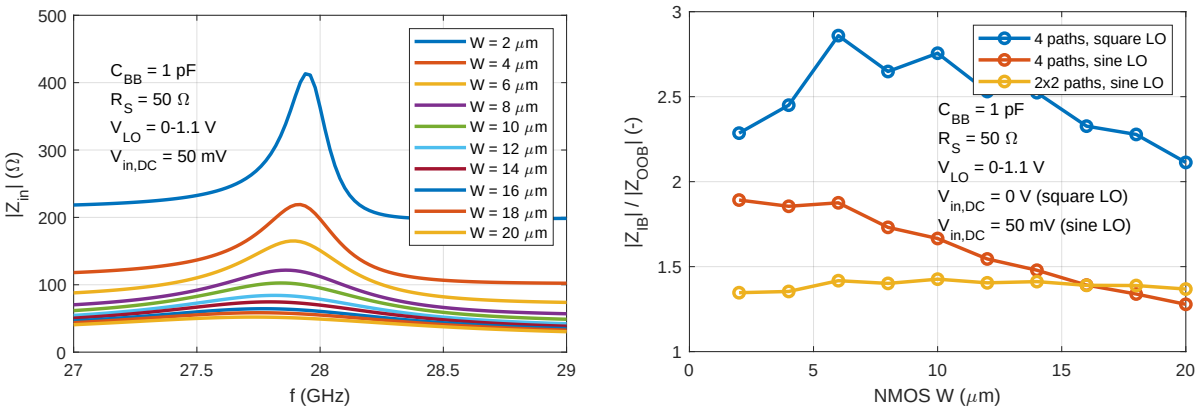


Figure 2.14: (a) Impedance of the 4-path sine LO filter for different switch widths. (b) Ratio between IB and OOB impedance of the three filters for different switch width.

The reduced R_{sw} increases the filter BW of eq. (2.1). This can be compensated by increasing the size of C_{BB}, which increases the chip area. A larger switch also adds more parasitic capacitance, shifting the center frequency further down. Figure 2.14b shows the IB/OOB impedance ratio for the three filters. For the 4-path sine LO filter, a low switch width results in the largest impedance ratio and thereby the largest attenuation.

2.2.3. Conclusion on mm-wave NPFs

From the above comparison of NPF impedance, it can be concluded that a sine-wave LO can be used to control the NPF at mm-wave, without losing much attenuation. The 4-path filter provides better results than the 2x2 path NPF and is considered suitable for mm-wave design. An optimum bias voltage can be found which compromises between a small R_{sw} of the used path (which needs a large V_{GS}) and a large on-resistance of the unused paths (which requires a small V_{GS}). A small switch width results in the largest difference between Z_{IB} and Z_{OOB}, while at the same time requiring a small C_{BB} and a low LO power consumption and resulting in a limited shift of center frequency.

The maximum achievable attenuation of a second order NPF[1] is limited by the difference between R_{sw} and R_{leak}. For the 4-path filter with a sine-wave LO, this resistance ratio is $R_{\text{leak}}/R_{\text{sw}}$ = 0.9 . With the NPF connected shunt at the input (as a BPF), the maximum attenuation for these resistance ratios is 3.2 dB, as calculated with eq. (2.10). Because of this limited attenuation, the NPF is not used as a standalone filter. The next chapter presents a technique to improve the attenuating by connecting the NPF in the feedback path of an LNA.

[1] A second order NPF has a first order LPF at baseband. Upconverted to RF results in a second order BPF.

3

Gain boosted N-path filter

The attenuation of a simple NPF is limited by the ratio between the switch resistance and leakage resistance (eq. (2.10)). For large frequencies, this ratio is small due to capacitive leakage of the NMOS, as well as the limited leakage resistance when using a sine wave LO. A GB-NPF provides a solution to increase the attenuation by connecting the NPF in the feedback path around an LNA. This chapter starts by explaining the operation of a GB-NPF using its equivalent circuit model in Section 3.1. Equations for the achievable attenuation and gain are derived and compared to a simple NPF. The GB-NPF with an ideal LNA is designed in Section 3.2, which also includes the simulation results. The chapter is concluded in Section 3.3.

3.1. Theory

A GB-NPF improves the attenuation by using current cancelation [4, 8, 10–12, 24, 25]. Figure 3.1 shows the GB-NPF with simplified IB and OOB current flows.

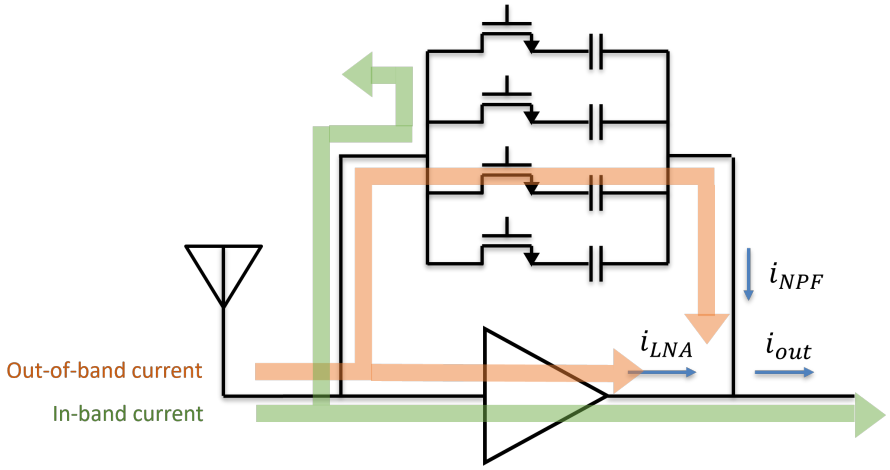


Figure 3.1: Gain-boosted N-path filter with in-band and out-of-band currents. Out-of-band currents pass through the NPF and cancel with the LNA current, which has a reversed phase. The in-band currents get blocked by the NPF, while passing through the LNA and therefore do not cancel at the output.

The NPF impedance is large IB and small OOB, thereby blocking the IB currents and passing the OOB currents through. The LNA reverses the phase of the signal, causing it to cancel out with the OOB current from the NPF. The IB current is not canceled and is therefore passed through the output. The condition for which the OOB current cancels at the output is derived using the equivalent model of this circuit, as shown in Figure 3.2.

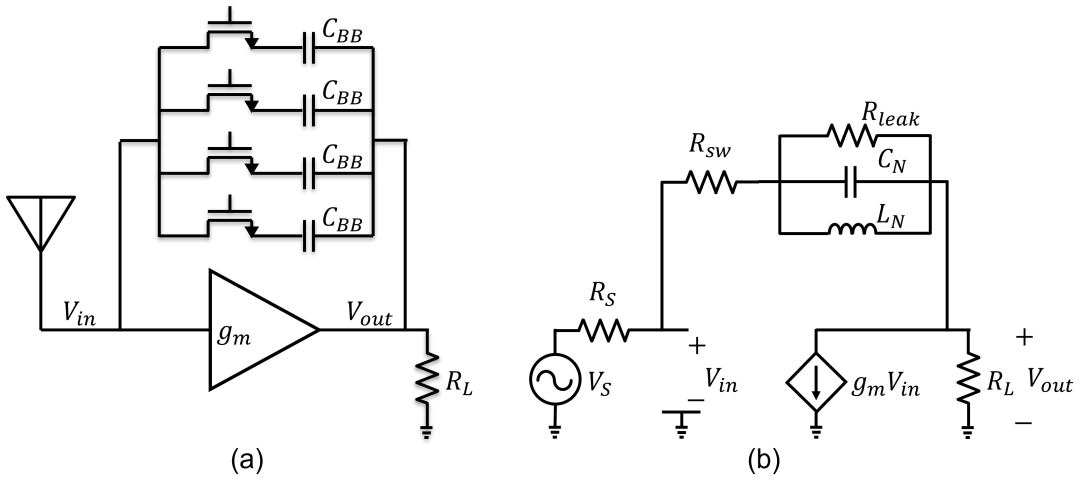


Figure 3.2: (a) Gain-boosted N-path filter and (b) its equivalent circuit model where R_{sw} is the on-resistance of the NMOS, R_{leak} represents the leakage of the NPF and R_L is the load resistance in parallel to the output resistance of the LNA.

3.1.1. Voltage gain

The voltage gain of the GB-NPF can be expressed as [10].

$$A_V = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_L(1 - g_m Z_{\text{NPF}})}{R_L + Z_{\text{NPF}}}. \tag{3.1}$$

The derivation of this equation is included in Appendix A.2.3. Perfect current cancelation reduces the gain to $A_V = 0$ when $g_m Z_{\text{NPF}} = 1$. This is desired to happen at OOB frequencies, to provide infinite blocker rejection. The required condition for zero gain at OOB frequencies, where $Z_{\text{NPF}} = R_{\text{sw}}$, is found to be

$$g_m R_{\text{sw}} = 1\angle 0. \tag{3.2}$$

A large IB voltage gain is however achieved when

$$g_m(R_{\text{sw}} + R_{\text{leak}}) \gg 1. \tag{3.3}$$

Because of the limited difference between R_{sw} and R_{leak} (Section 2.2.2), this poses a trade-off between a large IB gain and a large OOB rejection, which is visualized in Figure 3.3. The zero locations of the IB and OOB gain are close to each other, resulting in a difficult trade-off. A large IB gain at the same time results in a large OOB gain, leaving only a small attenuation. A large attenuation can only be achieved for a small IB gain.

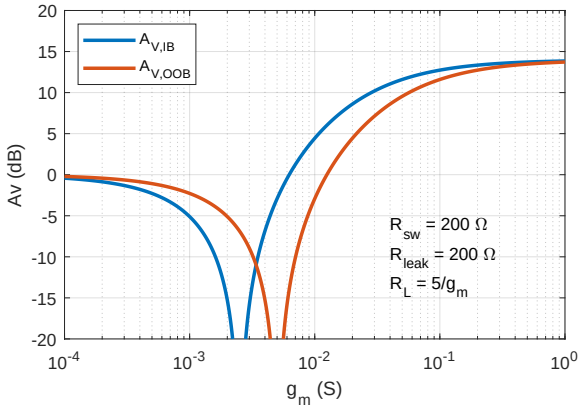


Figure 3.3: Calculated IB and OOB voltage gain for different values of g_m. The NPF impedances R_{sw} and R_{leak} are estimated from the simulation results in Figure 2.13b. The LNA gain is assumed to be $g_m R_L = 5$ (14 dB). The attenuation is found by looking at the difference of the IB and OOB gain in dB.

3.1.2. Input impedance

Besides attenuation in the voltage gain, the GB-NPF also provides filtering by the input impedance. This impedance, as derived in Appendix A.2.1 from the equivalent circuit in Figure 3.2, is

$$Z_{\text{in}} = \frac{R_L + Z_{\text{NPF}}}{1 + g_m R_L}. \tag{3.4}$$

Compared to a standalone NPF, the input impedance of the GB-NPF is approximately decreased by $1 + g_m R_L$, which is expected from the miller effect [20]. This effect causes the baseband capacitor C_{BB} to appear at the input with an increased size of $C_{\text{BB}}(1 + g_m R_L)$, thereby significantly reducing the required capacitor size.

The attenuation caused by the input impedance can be expressed using eq. (2.8), where the input impedance is assumed to be matched to the source impedance.

$$\begin{aligned} Att_{Z_{\text{in}}} &= 20 \log_{10} \left(\frac{|Z_{\text{in,IB}}| + |Z_{\text{in,OOB}}|}{2|Z_{\text{in,OOB}}|} \right) \\ &= 20 \log_{10} \left(\frac{R_L + R_{\text{sw}} + \frac{1}{2} R_{\text{leak}}}{R_L + R_{\text{sw}}} \right) \end{aligned} \tag{3.5}$$

A small R_L and R_{sw} and a large R_{leak} are required for a large attenuation. To control the input impedance without changing Z_{NPF}, an additional matching resistance R_f can be placed in the feedback around the LNA [4, 8, 10]. While this separates the input matching from the design of the filter attenuation, the resistor is connected in parallel to the NPF. This reduces the ratio between IB and OOB NPF impedance from $\alpha = (R_{\text{sw}} + R_{\text{leak}})/R_{\text{sw}}$ to

$$\alpha_f = \frac{Z_{\text{NPF,IB}} \| R_f}{Z_{\text{NPF,OOB}} \| R_f} = \frac{1 + \frac{R_f}{R_{\text{sw}}}}{1 + \frac{R_f}{\alpha R_{\text{sw}}}}. \tag{3.6}$$

This simplifies to $\alpha_f = \alpha$ if $R_f / R_{\text{sw}} \gg 1$, thus if $R_f \gg R_{\text{sw}}$. However, to have control over the input impedance, R_f cannot be much larger than R_{sw}. The matching resistor therefore reduces the already limited achievable attenuation and is not used in the design of the filter.

3.1.3. Noise figure

This section derives the IB noise of the GB-NPF. The considered noise sources of the GB-NPF are the thermal noise of the LNA and NPF. The LNA has a noise current $i_{n,gm}$ parallel to $g_m V_{\text{in}}$, and the NPF provides a parallel noise current of $i_{n,\text{NPF}}$, as shown in Figure 3.4.

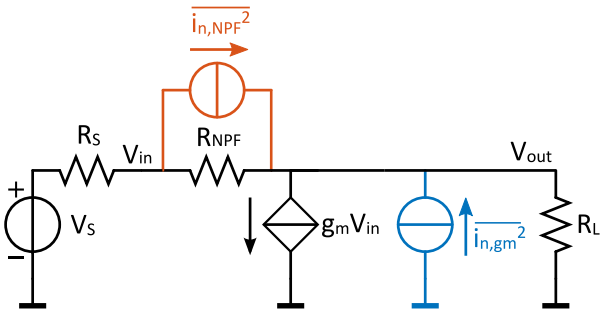


Figure 3.4: small-signal model of the GB-NPF, with noise sources of the LNA and NPF.

The noise of the LNA is brought to the input by multiplying the noise current with the output impedance and subsequently dividing it by the voltage gain. The resulting input noise voltage, as derived in Appendix A.2.4, is

$$\overline{V_{n,\text{in|gm}}^2} = \left(\frac{R_S + R_{\text{NPF}}}{1 - g_m R_{\text{NPF}}} \right)^2 \overline{i_{n,\text{gm}}^2}. \tag{3.7}$$

The g_m cell will be implemented by a common-source (CS) amplifier[1], which has a thermal noise current of $\overline{i_{n,\text{gm}}^2} = 4kT\gamma g_m$. Assuming $g_m R_{\text{NPF}} \gg 1$, eq. (3.7) can be simplified to eq. (3.8). A large g_m and R_{NPF} are needed to result in a low input noise voltage from the LNA.

$$\overline{V_{n,\text{in|gm}}^2} \approx \frac{4kT\gamma}{g_m}\left(\frac{R_S + R_{\text{NPF}}}{R_{\text{NPF}}}\right)^2. \tag{3.8}$$

The noise of the NPF is split in two current sources from each node to ground. The noise at the output node is converted to the input in the same way as the LNA noise. The noise current at the input node is multiplied by the input impedance in parallel with R_S to obtain the input-referred voltage noise. The total contribution of the NPF to the input noise voltage, as derived in Appendix A.2.4, is

$$\overline{V_{n,\text{in}|R_{NPF}}^2} = \left[\frac{R_S + R_{\text{NPF}}}{g_m R_{\text{NPF}} - 1} + \frac{R_L + R_{NPF}}{2(1 + g_m R_L)}\right]^2 \overline{i_{n,R_{NPF}}^2} \tag{3.9}$$

where $\overline{i_{n,R_{\text{NPF}}}^2} = 4kT/R_{\text{NPF}}$. The input noise voltage from the NPF (eq. (3.9)) can be simplified to

$$\overline{V_{n,\text{in}|R_{NPF}}^2} = \left[\frac{R_S + R_{\text{NPF}}}{g_m R_{\text{NPF}}} + \frac{R_L + R_{NPF}}{2 g_m R_L}\right]^2 \frac{4kT}{R_{\text{NPF}}} \tag{3.10}$$

For this noise to be small, a large g_m is required. An optimum value of R_{NPF} can be found for which the noise is minimum.

3.2. GBNPF design

3.2.1. Design methodology

As shown in Section 3.1, to simultaneously achieve high attenuation and high gain, the ratio between R_{leak} and R_{sw} must be maximized. While this ratio has been optimized for a BPF in Section 2.2.2, the GB-NPF connects the NPF as a BSF. Therefore, the optimal switch width will be determined for the NPF connected to a load resistance R_L. This will result in the optimal R_{sw} and R_{leak} values with the largest ratio between them. The next step is to equate the input impedance to 50 Ω with the assumption that the maximum LNA gain is $g_m R_L = 5$. From the input impedance equation, the required g_m of the LNA will be found. The design goals are as follows.

- Z_{in} = 50 Ω;
- A_V = 0 (to compare with standalone NPF)[2];
- Largest attenuation possible with above requirements.

3.2.2. Optimum switch width

The NPF switch width, resulting in the largest IB to OOB NPF impedance ratio, is found by simulating the circuit in Figure 3.5. The load impedance models the input impedance of the next stage (R_L') in parallel to the output impedance of the LNA (r_O). R_L' is assumed to have a maximum value of 200 Ω.

[1] This will be discussed in Chapter 4.

[2] For the final design, the GB-NPF is designed to achieve a larger gain, since the attenuation is mainly provided by the subtraction of the two filters (Chapter 4).

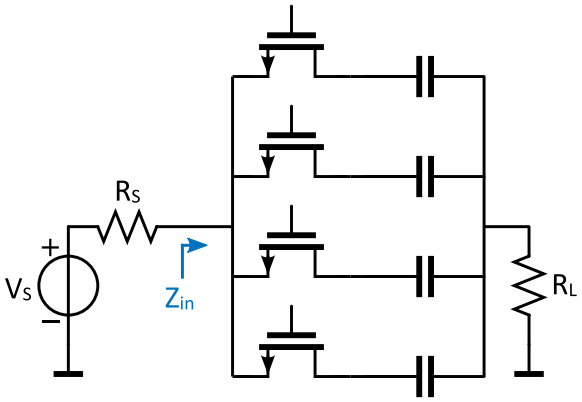


Figure 3.5: Circuit to simulate the IB and OOB NPF impedances when connected to a load resistance.

The simulated impedance ratio versus the input bias voltage and the switches' width are shown in Figure 3.6. Different values of R_L are used to show the effect of connecting the NPF to a load impedance. The only clear effect of R_L is a difference in the impedance ratio for a large NMOS width.

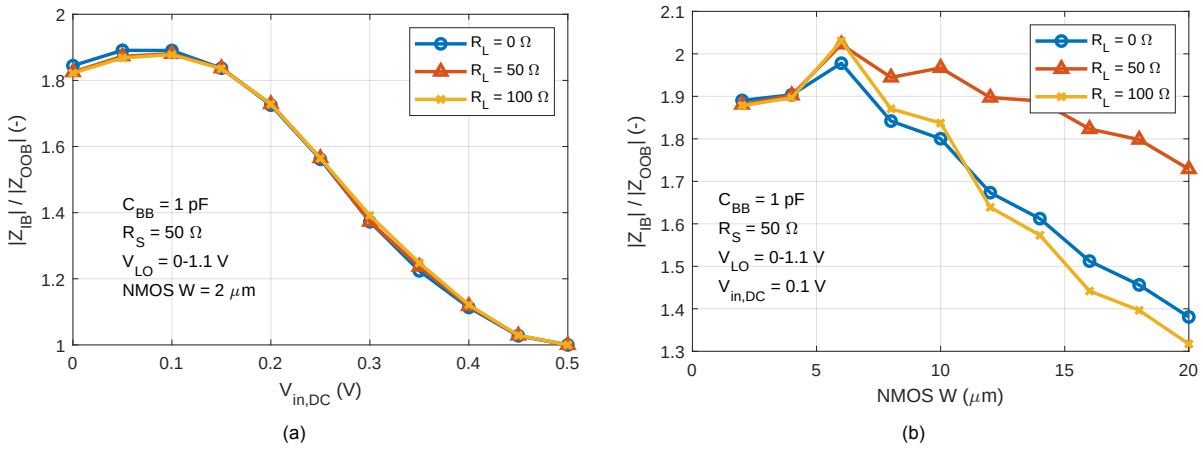


Figure 3.6: Simulated ratio between IB and OOB NPF impedance for different values of R_L versus (a) the input bias voltage, and (b) the NPF switch width.

The optimum input DC bias voltage is found to be $V_{\text{in,DC}}$ = 0.1 V and the optimum switch width is W = 6 µm. The resulting NPF impedance for different values of R_L is shown in Figure 3.7. A linear dependency between the IB NPF impedance to R_L is found to be

$$Z_{\text{NPF,IB}} = -0.414R_L + 197\ \Omega, \tag{3.11}$$

which is used for the next step in the design.

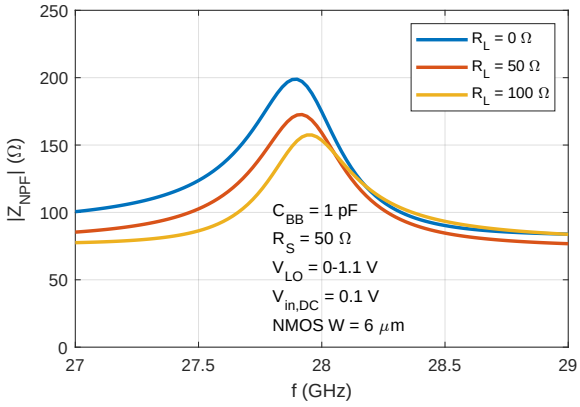


Figure 3.7: Simulated NPF impedance versus frequency for different values of the load resistor R_L.

3.2.3. Input impedance design

The IB input impedance is designed to be $Z_{\text{in,IB}}$ = 50 Ω. From eq. (3.4), it can be found that Z_{in} depends on the load impedance, the NPF impedance, and the LNA gain. The NPF impedance is chosen to provide the largest difference between the IB and OOB impedance, to maximize the blocker rejection. A large g_m is desired to achieve a large attenuation and a low noise figure (NF), so only the load impedance can be adjusted to achieve the desired $Z_{\text{in,IB}}$.

The effect of the load impedance (R_L) on $Z_{\text{in,IB}}$ is investigated. R_L is the output impedance of the LNA, r_O, in parallel to the input impedance of the next stage, R'_L. Since R_L also affects the NPF impedance, the obtained dependency between $Z_{\text{NPF,IB}}$ and R_L (eq. (3.11)) is substituted in eq. (3.4). The resulting required R_L can be achieved with different combinations of R'_L and r_O. The required r_O for a selected R'_L is found to be

$$r_O = \frac{R'_L\left(6Z_{\text{in,IB}} - b\right)}{R'_L(1+a) + b - Z_{\text{in,IB}}}. \tag{3.12}$$

Where a and b are the parameters from the relation between $Z_{\text{NPF,IB}}$ and R_L,

$$Z_{\text{NPF,IB}} = aR_L + b. \tag{3.13}$$

The full derivation of eq. (3.12) is included in Appendix A.2.5. For the optimum width of 6 µm, the possible combinations of r_O and R'_L, resulting in $Z_{\text{in,IB}}$ = 50 Ω, are shown in Figure 3.8a. A large R'_L,

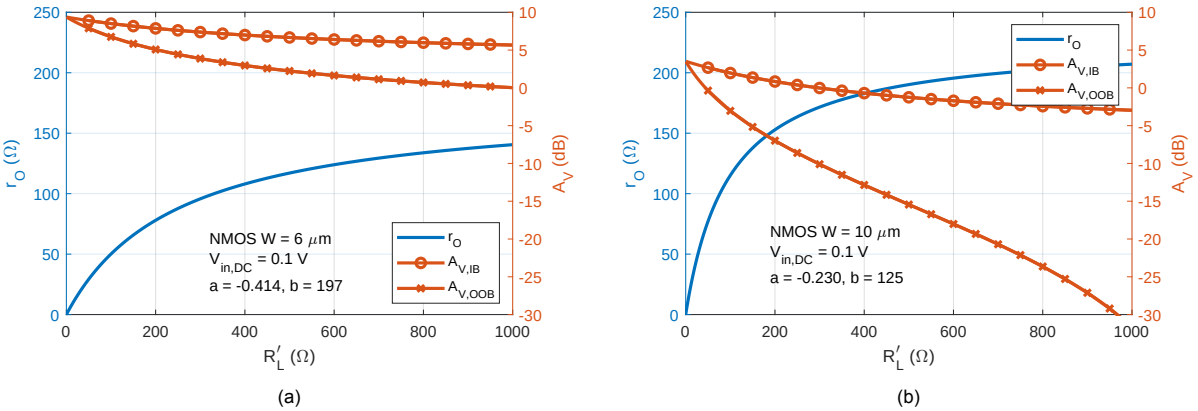


Figure 3.8: Calculated r_O using eq. (3.12) and voltage gain using eq. (3.1) for an NPF NMOS width of (a) 6 µm (a = -0.414, b = 197) and (b) 10 µm (a = -0.230, b = 125).

and thus a small is desired to obtain a large Since the input impedance of the next stage is expected to be limited to 200 Ω, the maximum achievable attenuation is only $A_{V,\text{IB|dB}} - A_{V,\text{OOB|dB}}$ = 2.9 dB. For this selected switch width and input impedance, the GB-NPF helps to provide gain, but does not improve the attenuation compared to the standalone NPF. The attenuation can be improved by selecting a larger

NMOS width, which results in a smaller Z_{NPF}. For a width of 10 µm, the simulated relation between $Z_{\text{NPF,IB}}$ and R_L is found to be $Z_{\text{NPF,IB}}$ = -0.230R_L + 125 Ω. The possible combinations of r_O and R'_L are shown in Figure 3.8b. The calculated attenuation is improved to 7.8 dB and the IB gain is close to 0 dB, as required for the comparison with the standalone NPF. From the design method described above, the following parameters are obtained.

- NMOS W = 10 µm;
- $V_{\text{in,DC}}$ = 100 mV;
- R'_L = 200 Ω;
- r_O = 153 Ω;
- g_m = 33 mS.

3.2.4. Resulting gain and attenuation

The resulting input impedance and voltage gain of the GB-NPF with ideal LNA are shown in Figure 3.9. The IB input impedance is closely matched to the designed 50 Ω. The voltage gain of 0.3 dB also corresponds to the designed gain of 0 dB. From Figure 3.9b, it can be seen that the GB-NPF, designed for 0 dB gain, can achieve a larger attenuation than a standalone NPF. The BW is decreased for the same value of C_{BB}, due to the miller effect as discussed in Section 3.1.

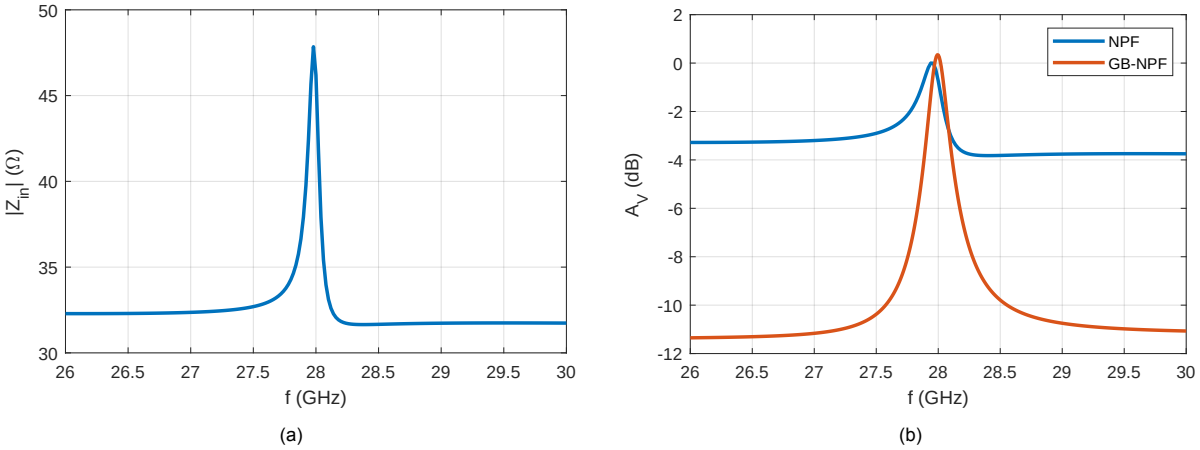


Figure 3.9: (a) Simulated input impedance of the designed GB-NPF with ideal LNA. (b) Simulated voltage gain of the designed GB-NPF, compared to the achievable voltage gain of the standalone NPF.

3.3. Conclusion

A GB-NPF can increase the attenuation of a standalone NPF by placing it in the feedback of an LNA. When the current through the NPF and LNA have the same magnitude and opposite phase, they cancel out, resulting in a large attenuation. The roll-off of the GB-NPF is limited to 20 dB per decade. With the attenuation at the edge of the main channel (f_{LO} + 100 MHz) set to 3 dB, the maximum achievable attenuation at the center of the adjacent channel is limited to 6.8 dB and cannot reach the required 10 dB. This can only be achieved by increasing the filter order, which is done in the next chapter.

4

Higher-order N-path filter

As shown in the previous chapter, a second-order NPF[1] cannot provide the required 10 dB attenuation at the first adjacent channel. Furthermore, the second-order GB-NPF showed to have an inverse dependency between the achievable gain and attenuation. When designed for a 0 dB IB gain, the far-OOB attenuation is limited to 11.5 dB. Designing for a larger attenuation reduces the IB gain even further. In order to simultaneously achieve a large gain and large attenuation, it is preferred to separate these parameters in the design.

A higher-order NPF is designed in this chapter, which improves both the attenuation at the center of the first adjacent channel and far-OOB. The chapter starts with a comparison of the state-of-the-art NPFs with an increased filter order in Section 4.1. The most promising technique is used as the basis for the design, which covers the rest of this chapter. The system overview of the designed higher-order filter is included in Section 4.2, after which the operation of this topology is explained in Section 4.3. The filter is designed in Section 4.4 and the simulation results are included in Section 4.5. Finally, Section 4.6 concludes the design of this filter.

4.1. State-of-the-art comparison

A first-order baseband filter cannot provide the required 10 dB attenuation at the center of the first adjacent channel, as shown in Figure 4.1. The roll-off of the filter can be improved by increasing the filter order. A second-order baseband filter provides 13 dB attenuation in the center of the first adjacent channel. Providing the required 10 dB filtering for the full adjacent channel would require a seventh-order baseband filter.
This section investigates the state of the art of higher-order NPFs. These can be categorized into three groups. First, a higher-order baseband impedance can replace the baseband capacitor. Secondly, zeros can be added to improve the attenuation in the adjacent channel. The last option is to combine the output of multiple NPFs with a frequency offset to create a flat IB response and a steep roll-off. The state of the art is discussed for these three categories after which a comparison allows us to select the most promising technique.

4.1.1. Higher-order baseband impedance

The filter order can be increased by adding a frequency-dependent gain to the baseband impedance [20, 26]. Park and Razavi [20] use a frequency-dependent amplifier in the baseband impedance of a GB-NPF, as shown in Figure 4.2. Due to the miller effect, the effective filter capacitance is

$$C_{\text{eff}} = (1 + A_0 A_1) C_M, \tag{4.1}$$

where A_0 is the gain of the main amplifier and A_1 the gain in the feedback path. The gain A_1 increases with frequency, thereby also increasing the effective capacitance with frequency. The filter BW is dependent on $1/C_{\text{eff}}$ and therefore decreases for larger frequencies, which results in a sharper roll-off. An

[1] A second-order NPF has a first-order LPF at baseband. Upconverted to RF results in a second-order BPF.

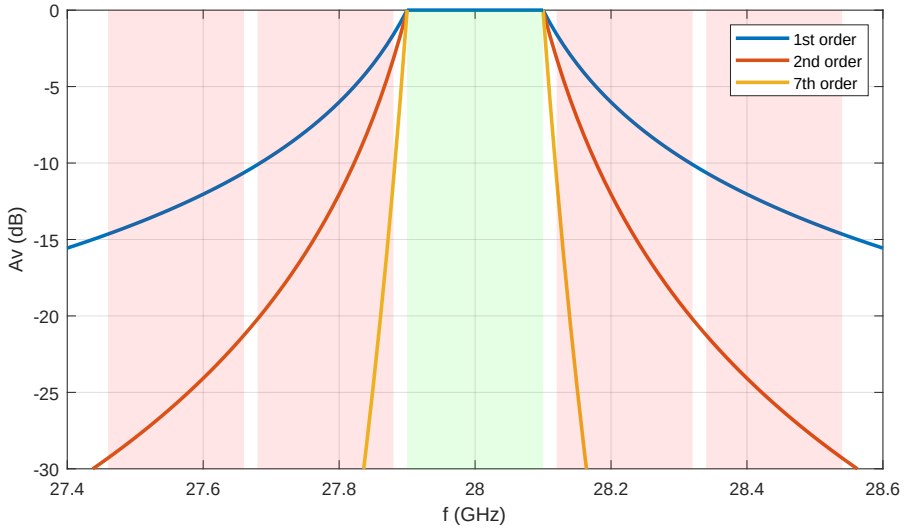


Figure 4.1: Ideal filter shapes for different order baseband filters. The green shaded area is the main band. The red shaded areas denote the first and second adjacent channels.

additional benefit of the baseband amplifier is the reduced size of the baseband capacitance C_M due to the increased loop gain and the Miller effect.

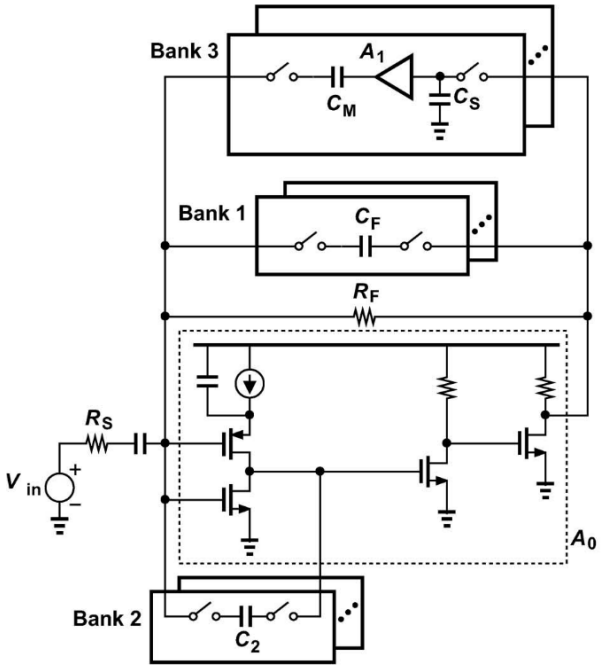


Figure 4.2: Active baseband impedance in GB-NPF [20].

This frequency dependent gain can also be used for an NPF without gain boosting [26]. This filter uses an active baseband impedance with a negative and positive feedback path, as shown in Figure 4.3a. The positive feedback path provides a second-order frequency dependency to the baseband impedance, thereby improving the filter roll-off.

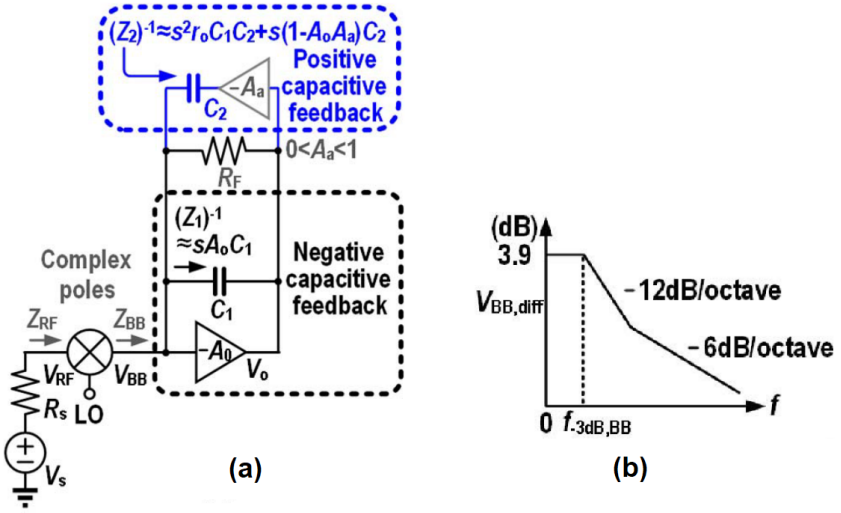


Figure 4.3: (a) Active baseband impedance with negative and positive feedback path. (b) Simplified plot for the baseband voltage which shows the filtering [26].

Using a frequency-dependent gain in the feedback path has two disadvantages. Firstly, the delay of the feedback path is increased. This increases the phase difference between the signals from the feedback path and the LNA, such that they do not completely cancel each other out. The OOB attenuation is thereby reduced, especially at mm-wave.

Secondly, the amplifier in the feedback path causes a zero in the transfer function, limiting the BW for which a large roll-off is achievable [26]. Figure 4.3b shows the baseband voltage V_{BB}. This has a second-order roll-off until the zero of the positive capacitive feedback brings it back to a first-order roll-off. This zero, caused by the resistor and output capacitor of additional gain A_a, is $s = (0.5R_aC_a)^{-1}$. The maximum BW is limited by this zero, since a larger BW would result in a limited frequency range with second-order roll-off before it reduces to first order. This circuit, as well as the filter in [20], are designed for 20 MHz BW and are thus less suitable to use for a BW of 200 MHz.

4.1.2. Increasing the filter slope with a zero

Besides increasing the baseband filter order, the attenuation close to the desired band can also be increased by adding a zero on either side. These can be added by two capacitors in the baseband filter, placed shunt to ground, as shown in Figure 4.4 [10].

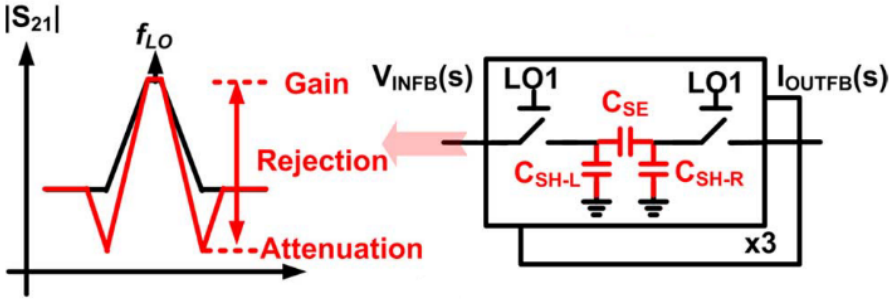


Figure 4.4: Two shunt capacitors at the baseband filter, used to create notches in the band-pass filter [10].

After upconversion to RF, each capacitor behaves as a parallel RLC resonator, as shown in Figure 4.5. The in-band and far-out-of-band signals of the GB-NPF are still following the same paths as in Figure 3.1, but the signals, which are slightly out-of-band now get attenuated due to the zeros.

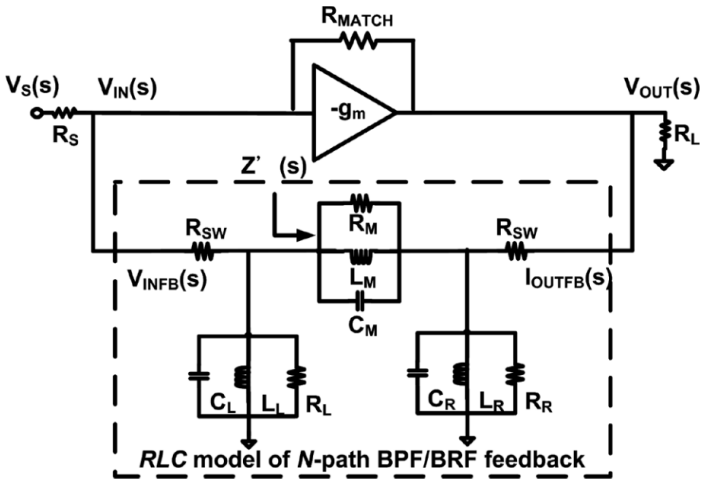


Figure 4.5: *RLC* model of the GB-NPF with two shunt capacitors in the baseband filter [10].

An inductor can be added between the left shunt capacitor and ground to move the notch closer to the desired band [11, 12]. Simulations performed by Qi et al. [12] show that the added inductor decreases the notch offset by 30% and 18% on the left and right sides of f_{LO}, respectively. The cost of adding an inductor to each baseband filter is a significant increase in the full chip area [12]. The resulting zeros are located at a 40 MHz offset from 850 MHz ($\Delta f/f_c = 5\%$). While this increases the attenuation in some of the nearby channels, the filtering at the first adjacent channel does not improve significantly. In the mm-wave filter, the center of the first adjacent channel is at 220 MHz offset from 28 GHz, thus $\Delta f/f_c = 0.8\%$.

Song and Hashemi [15] implemented these zeros with three separate NPFs, which are passively coupled, as shown in Figure 4.6. One NPF adds a zero to the low-frequency side of the desired band and one to the high-frequency side. While the zeros can be located close to the main channel, the coupling requires large inductors, thereby using a significant chip area.

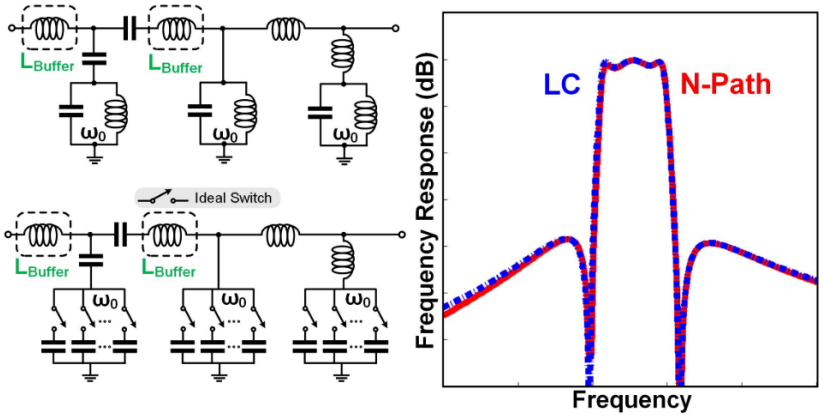


Figure 4.6: Passively coupled NPFs to create two zeros at the main-band edges [15].

Instead of adding zeros by two shunt RLC resonators, a series L and C can be used [8]. Figure 4.7 illustrates the band-stop filter with an extra C_s and L_s. These resonate with L_p and C_p respectively to create two nulls in the input impedance as well as the gain of the GB-NPF. An extra band-stop NPF is connected between the antenna to the output of the gyrator to improve the attenuation at frequencies further out-of-band than the nulls. The resulting attenuation is visible in the simulated input impedance and gain in Figure 4.7. The added zeros improve the attenuation close to the desired band, but requires more N-path transistors and two additional g_m cells, resulting in a larger power consumption.

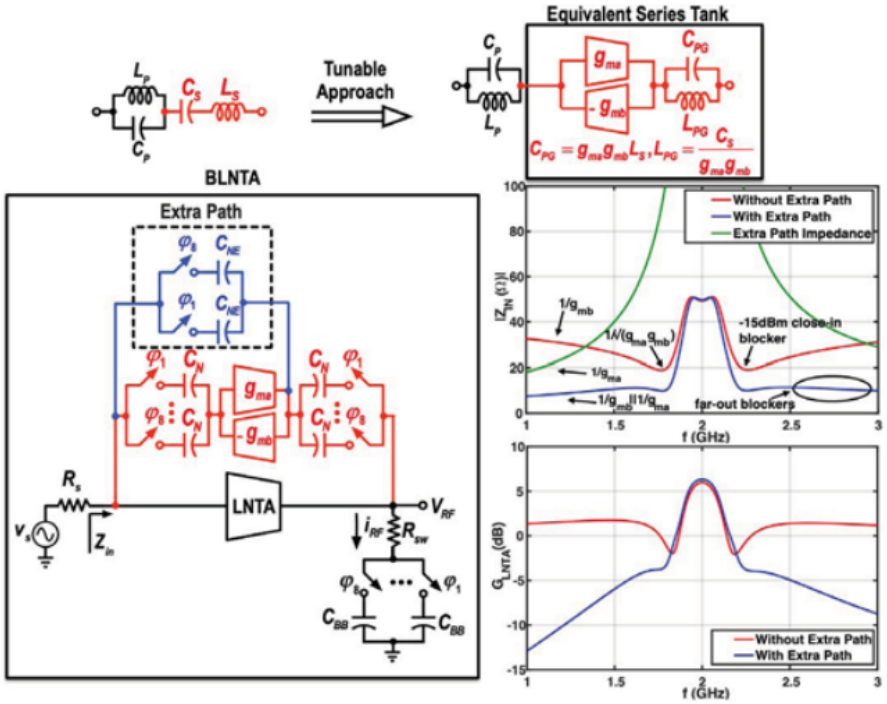


Figure 4.7: GB-NPF with two nulls created by the resonance of L_p and C_s and the resonance of C_p and L_s and its simulation results [8].

Another method used to obtain zeros in the transfer function is the use of a $C-LC-C$ baseband filter, as shown in Figure 4.8 [6]. This filter requires four large inductors in the order of 20 nH each for a BW of 800 MHz. Decreasing this BW to 200 MHz results in four 80 nH inductors, thereby using a significantly large area, especially when this inductance must be implemented at mm-wave. Implementing this filter as a GB-NPF would require the baseband filter to be a high-pass filter (HPF) instead of a LPF. This would need two inductors per path to implement an LCL-filter, thereby increasing the area even further.

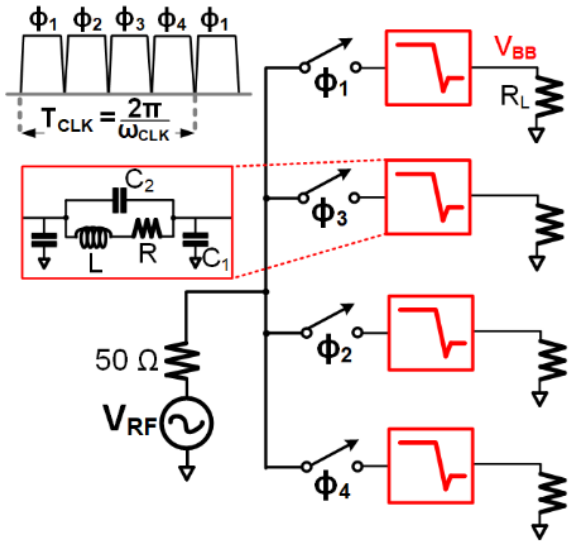


Figure 4.8: Third-order passive elliptic LPF implemented in a mixer-first receiver [6].

The last method for the creation of zeros in the transfer function is used in [21]. In this research, the outputs of a BPF and a BSF with equal center frequency are subtracted, as shown in Figure 4.9. This principle is illustrated with only passive filters, but is implemented by NPFs in the paper. The attenuation

in the first adjacent channel is almost completely determined by the BPF and thus does not benefit from the added zeros. These zeros can be brought closer to the main band by increasing the BSF gain. This however increases the difference between the BPF and BSF gains at far-OOB frequencies, resulting in a larger gain and thus a lower attenuation after the subtraction.

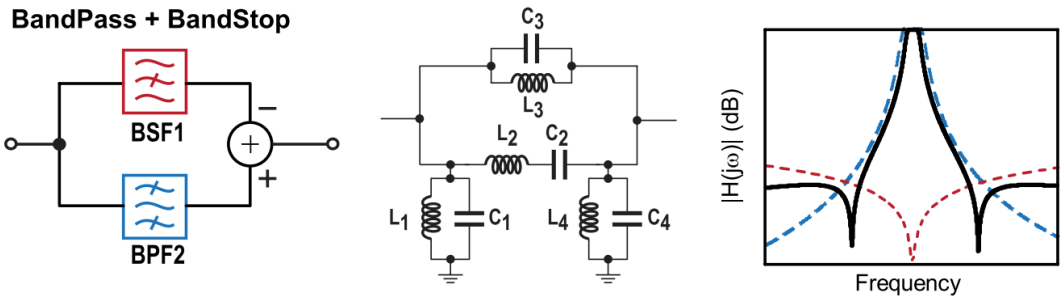


Figure 4.9: Subtraction of a BSF from a BPF to create two zeros [21].

4.1.3. Combination of N-path filters with a frequency offset

The third method to increase the attenuation is by using a combination of multiple NPFs with an offset in the center frequency. This comes with the added benefit of a more flat in-band response. The principle is illustrated by Amin et. al. [27] in Figure 4.10. This paper uses the subtraction of two BPFs with a frequency offset $\Delta\omega$. Although the filter is not implemented with NPFs, it still shows the principle of the subtraction.

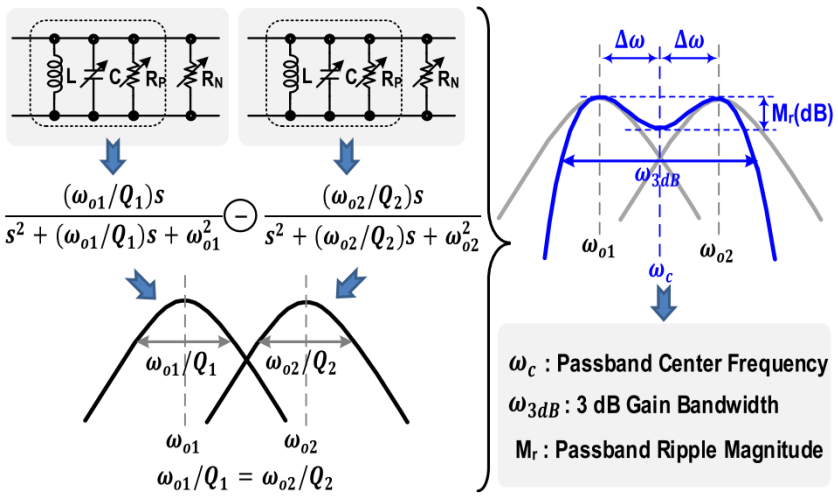


Figure 4.10: Summation of two BPFs with a frequency offset [27].

An NPF implementation of this technique is designed by Darvishi et. al. [16, 18]. The two filters shown in Figure 4.11 are controlled by the same LO signal, which frequency is the center frequency of the desired received channel. This LO can therefore also be used to control the mixer of the receiver. The frequency offset in the NPFs is obtained by differential g_m-cells.

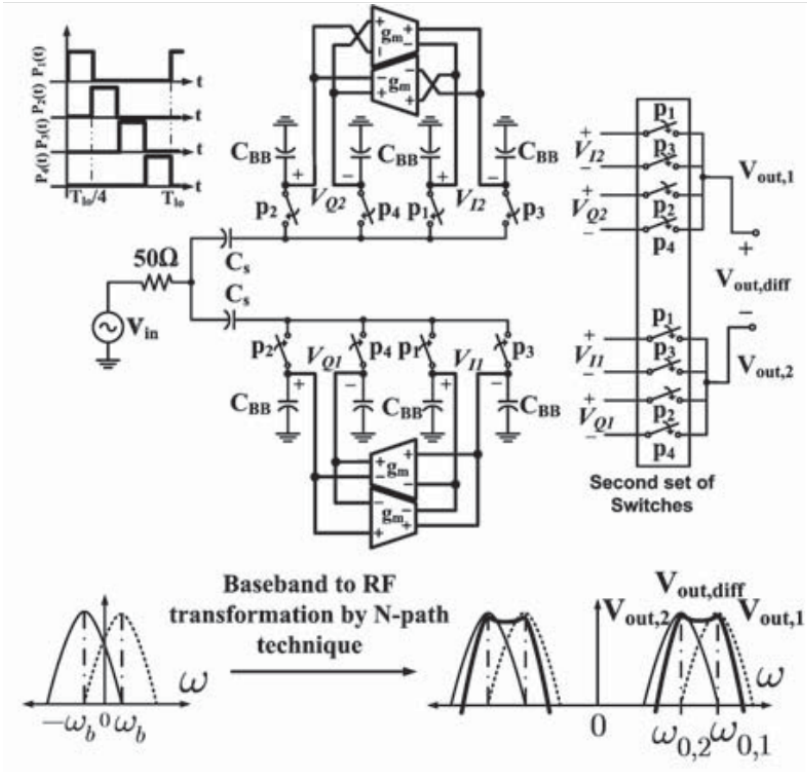


Figure 4.11: Subtraction of two NPFs with a frequency shifted caused by g_m cells [18]

4.1.4. Comparison of higher-order N-path filters

In order to conclude on the most promising filter architecture to use at mm-wave, the state-of-the-art NPFs are compared in three aspects. First, the achieved filter slope should be large to get a large attenuation close to the main channel. Besides that, the power consumption must be small. And lastly, the filter needs to be suited to operate in mm-wave, while using a small area.

The achieved filter slope of the state-of-the-art higher-order NPFs is compared. Since this slope is highly dependent on the filter BW, the filters are compared using their roll-off in dB per BW. This is defined in Figure 4.12. The slope is extrapolated to one BW away from the edge of the passband. The extrapolated attenuation at that frequency is the roll-off in dB/BW.

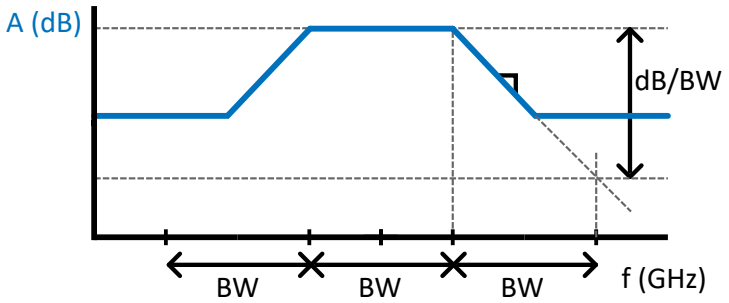


Figure 4.12: Definition of filter slope in dB per BW. This is the attenuation when the filter slope is extrapolated to one BW offset from the passband edge. This is not always equal to the attenuation at one BW offset, since the maximum attenuation can be smaller than the slope in dB/BW.

The roll-off of the state-of-the-art filters is compared in Figure 4.13. The largest roll-off can be found for the NPF with a frequency-dependent gain in the baseband impedance [20]. This architecture, as well as the filter presented in [26] are however less suitable for mm-wave, because of the increased delay and limited BW caused by the amplifier in the feedback path. The NPFs from [6, 15] require a number

of large inductors, resulting in a large chip area, making these filters less favorable architectures. The subtracted BPF and BSF from [21] also provides a large roll-off. This, however, requires a total of five NPFs, resulting in a power-hungry LO at mm-wave frequencies.

The most suitable architecture for the mm-wave NPF is the g_m cell-based NPF from [18]. This filter does not require large inductors and only uses two NPFs, limiting the area and LO power consumption respectively.

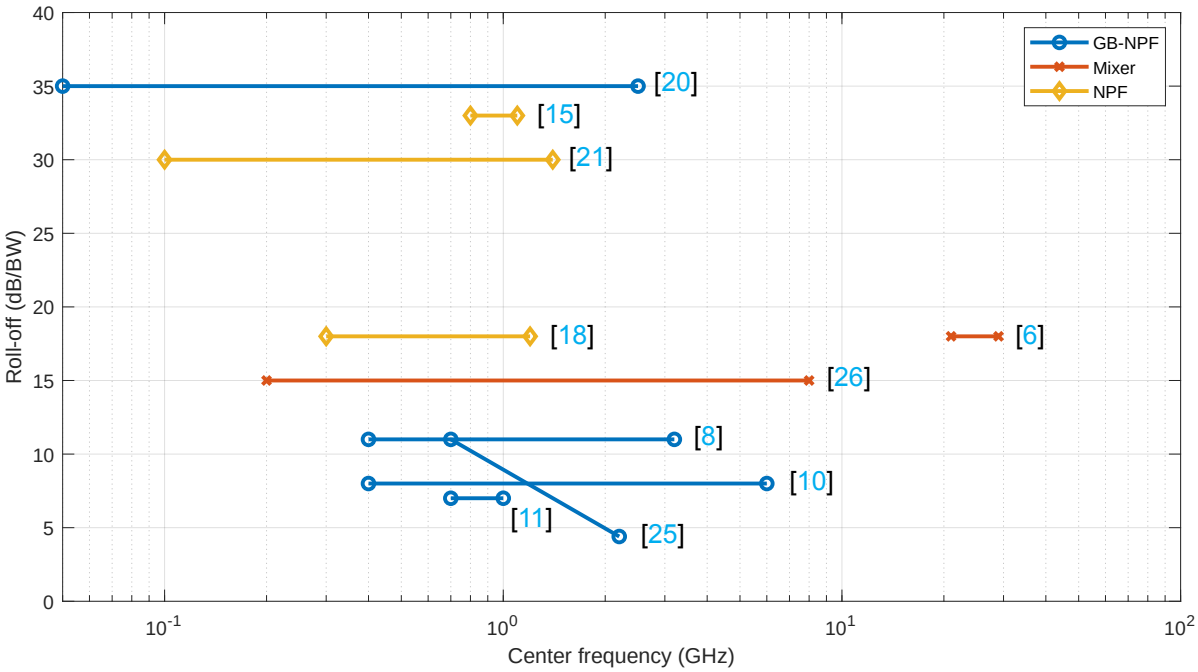


Figure 4.13: Comparison of the state-of-the-art higher-order NPFs. The filter slope is calculated in dB/BW.

4.2. Filter system overview

From the state-of-the-art overview, it can be found that two filters with a frequency offset can provide a large attenuation while maintaining a flat IB gain [18]. This topology has two additional benefits. First, the gain and attenuation can be designed separately. The filter in each path can be tuned to achieve the desired gain, since the attenuation is mainly caused by the subtraction of the output voltage of both paths. Secondly, the frequency of each path can be shifted by an arbitrary amount. This gives the possibility of compensating for the offset in center frequency found in the second-order NPFs. Shifting the frequency up and down by a different amount can create a filter centered around f_{LO}.

The top-level circuit of the implemented filter is shown in Figure 4.14. The NPFs in the frequency-shifted filter of [18] are implemented by GB-NPFs to improve the attenuation and increase the gain of the filter. The center frequency of the two NPFs is shifted to f_A and f_B, resulting in an output voltage $V_{\text{out+}}$, centered at f_A and $V_{\text{out-}}$, centered at f_B. The magnitude and phase of these voltages are shown in Figure 4.14. After subtraction, the remaining output voltage has a flat IB response and a sharp roll-off. A large IB phase difference between the paths, θ, results in a large output voltage after subtraction. At OOB frequencies, the magnitude and phase of the two paths are almost equal, thereby providing a small gain after subtraction, and thus a large OOB attenuation.

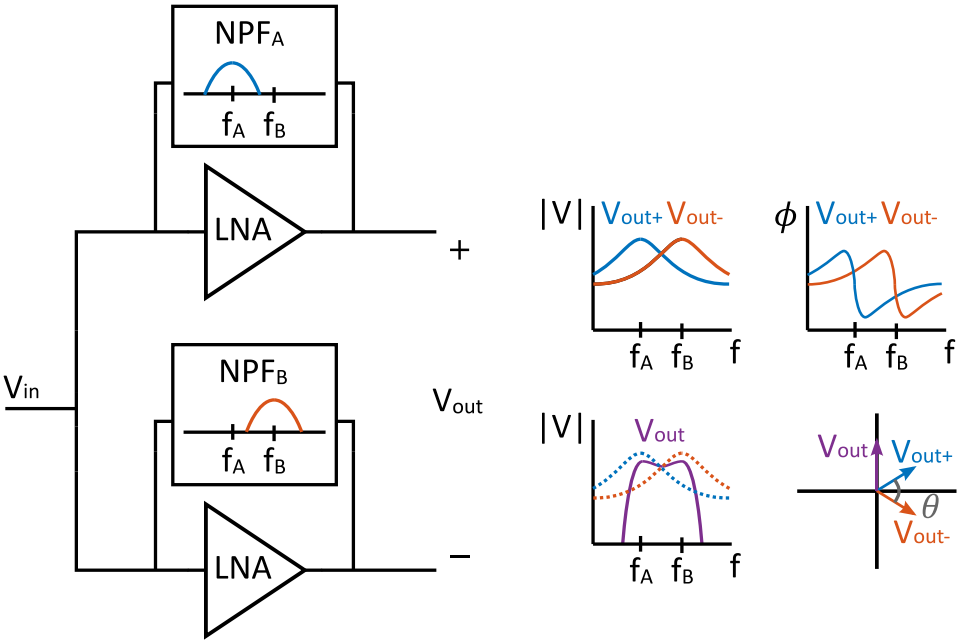


Figure 4.14: Top-level circuit of the frequency shifted GB-NPF.

The filter design is started with the frequency shifting technique. Different methods to provide an offset to the NPF center frequency are compared in Section 4.3. The design of the different parts of the filter is discussed in Section 4.4, after which Section 4.5 presents the simulation results. Section 4.6 subsequently concludes the higher-order NPF design.

4.3. Frequency shifting methods

The center frequency of an NPF is determined by the LO connected to the switches[2]. The LO frequency cannot be changed to accommodate for the frequency shift for two reasons. First of all, this clock signal will also be used for the mixer of the receiver, which must operate at the center frequency (f_{RF}). Secondly, two LOs would be needed to independently shift the center frequency of two paths, which will increase the chip area and cause interference problems [28]. The NPFs must be controlled by the LO at f_{RF}, while their center frequency must be at $f_{RF} - f_\Delta$ and $f_{RF} + f_\Delta$. This requires a frequency shifting mechanism without changing the LO. Three different realizations of a frequency shift in an NPF are used in literature and are discussed in this section.

4.3.1. NPF as baseband impedance

Two NPFs can be nested inside each other to create a filter at $f_{RF} + f_\Delta$ [29]. The first NPF will operate at f_{RF} and have a second NPF as baseband impedance. The second filter operates at f_Δ and has a LPF as baseband impedance. The second filter will thus upconvert the LPF to a BPF around f_Δ, which is moved to a BPF around $f_{RF} + f_\Delta$ by the first NPF. This principle is shown in Figure 4.15.

This filter requires two extra LO signals, of which one at $+f_\Delta$ and one at $-f_\Delta$[3]. While at a much lower frequency than f_{RF}, these still increase the chip area. The power consumption is also increased, due to the additional, nested, NPFs.

4.3.2. Rotation LO phases

An alternative method to obtain a frequency shift is by rotating the LO phases that are connected to each NPF switch [30]. The resulting clock phases that are connected to each NPF switch are visualized

[2] And by the offset caused by the parasitic capacitances of the switches, see Chapter 2.

[3] When each individual NPF is centered around f_{RF}, only one additional LO would be required. The center frequencies are however shifted down due to the parasitics of the switches. This results in two different required LOs for the up and down shift in frequency.

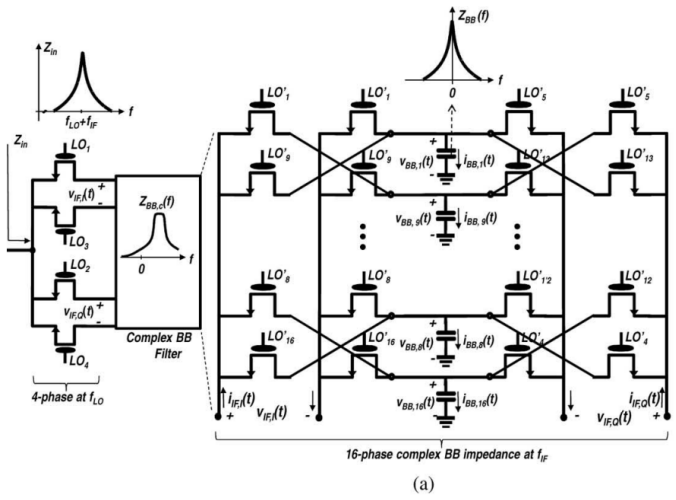


Figure 4.15: NPF at f_{RF}, with NPF at f_Δ as baseband impedance, to create a BPF around $f_{\text{RF}} + f_\Delta$ [29].

in Figure 4.16. This frequency shift can be implemented by either adding a delay to the quadrature LO

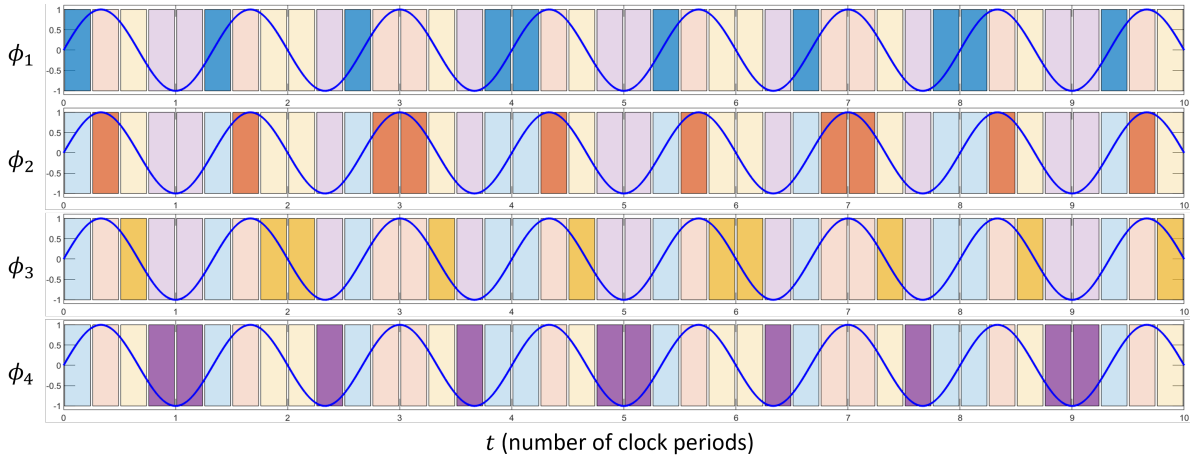


Figure 4.16: Clock phases connected to each NPF switch to obtain a frequency shift of $-f_{\text{RF}}/4$. The blue sine wave is an input signal at $f = \frac{3}{4} f_{\text{LO}}$.

signals or by physically rotating the clock signal that is connected to each switch. Adding a delay would require slowing down the LO signals with 1/4th of a period every time a double pulse is needed, as shown in Figure 4.16. This thus has to be a delay that increases every M periods, with $M = \frac{f_{\text{RF}}}{f_\Delta}$, which becomes unfeasible to implement.

The rotating clock signals could be implemented by connecting each clock phase to each NPF switch via an enable switch. This results in the problem that the enable switch must turn on and off fast enough to prevent overlap of multiple paths. Controlling the enable switches by a sine wave at 28 GHz results in multiple paths being (partially) turned on at the same time. This causes leakage between the paths and thereby a reduction in attenuation.

4.3.3. Charge shifting between the baseband nodes

The third frequency shift method is based on manipulating the charge on the baseband capacitors. Without any frequency shifting method, the voltage on the baseband capacitors will be a constant voltage when the input frequency equals the LO frequency. When this is not the case, the voltage will move up and down in small amounts but stays centered around 0 V. This is visualized in Figure 4.17a where an input voltage at $f_{\text{LO}} - f_\Delta$ is sampled on four capacitors at a rate of f_{LO}. Because of this

difference in frequency, a sine wave with small amplitude will exist on each capacitor. This sine wave is shown in Figure 4.17b. This amplitude is only small due to the frequency selectivity of the NPF. The

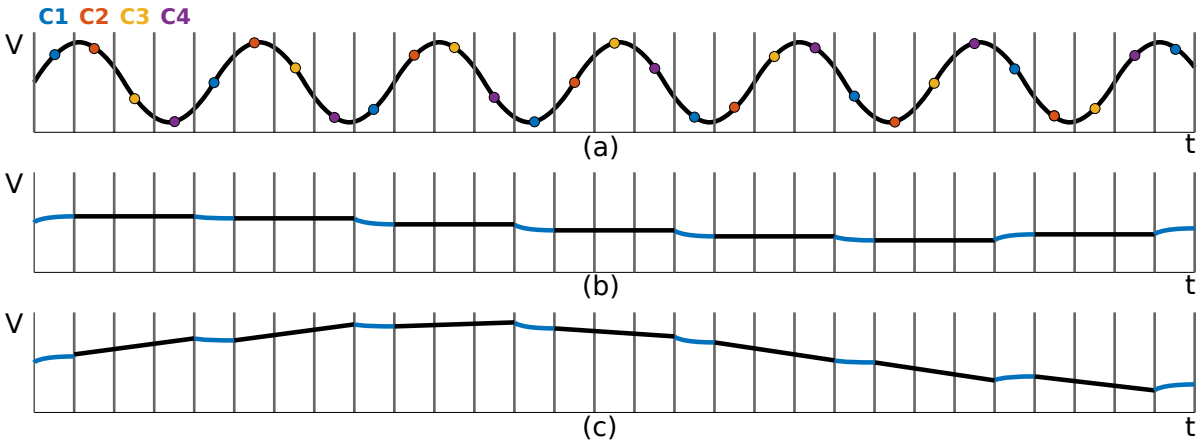


Figure 4.17: (a) Input voltage with $f_{RF} < f_{LO}$ and sampling moments of each capacitor highlighted with different colored dots. (b) Voltage on capacitor $C_{BB,1,B}$ without the g_m cells, which stays constant when $C_{BB,1,B}$ is not connected to the input. (c) Voltage on capacitor $C_{BB,1,B}$ with the gm cells. A positive voltage on in $C_{BB,2,B}$ causes an increase in the voltage on $C_{BB,1,B}$, thereby enlarging the existing sine wave at $|f_{RF} - f_{LO}|$.

filter would be shifted in center frequency when an input at $f_{LO} - f_\Delta$ results in a large amplitude sine wave at f_Δ on the baseband capacitors. When upconverted with f_{LO}, this results in a large amplitude sine wave at $f_{LO} - f_\Delta$. The baseband voltage is shown in Figure 4.17c. This behavior can be achieved by connecting a gm cell between each two consecutive NPF paths, as shown in Figure 4.18. When no gm cell is used, the capacitor voltages stay constant when not connected to the input. Adding the gm cells causes the capacitor voltages to change during the full period. A positive voltage $V_{2,B}$ causes charge to flow into $C_{BB,1,B}$, thereby increasing voltage $V_{1,B}$. A negative frequency offset can be obtained by using negative g_m cell gain, which can be implemented by reversely connecting the g_m cells in the NPF. The two paths of the filter are connected to a single ended input via two isolation impedances which are needed to reducing the sharing of charge between the capacitors of the two filters [18].

From the three compared methods to shift the NPF center frequency, the gm cell method is selected to be used, since it is the most feasible technique to implement at mm-wave.

4.4. Design

The filter will be used as the second stage in a 2-stage architecture. The input impedance of the filter (the second stage) partially determines the gain of the LNA (the first stage), which is defined by

$$A_{V,1} = g_{m,1}\left(r_{O,1} \| Z_{in,2}\right), \tag{4.2}$$

where $g_{m,1}$ and $r_{O,1}$ are the transconductance and output resistance of the first stage LNA and $Z_{in,2}$ is the input impedance of the filter. Since a large gain of the first stage reduces the noise of the second stage, it is important to design the filter for a large Z_{in}.

The design is started with a single GB-NPF, centered at f_{LO}. This is expanded with the g_m cells to shift the center frequency and the ideal LNA is replaced by a CS amplifier. The second part of the design discusses the problems arising when two frequency shifted GB-NPFs are added together. This includes the subtraction of the outputs and the isolation of the inputs. This part also includes a discussion on the noise figure of this filter.

4.4.1. Gain-boosted N-path filter at f_{LO}

Compared to the GB-NPF designed in Chapter 3, the design of this filter has two main differences. It must be designed to have a large input impedance and it can have a large gain at the cost of a lower attenuation, since the attenuation will mainly be provided by the output subtraction.

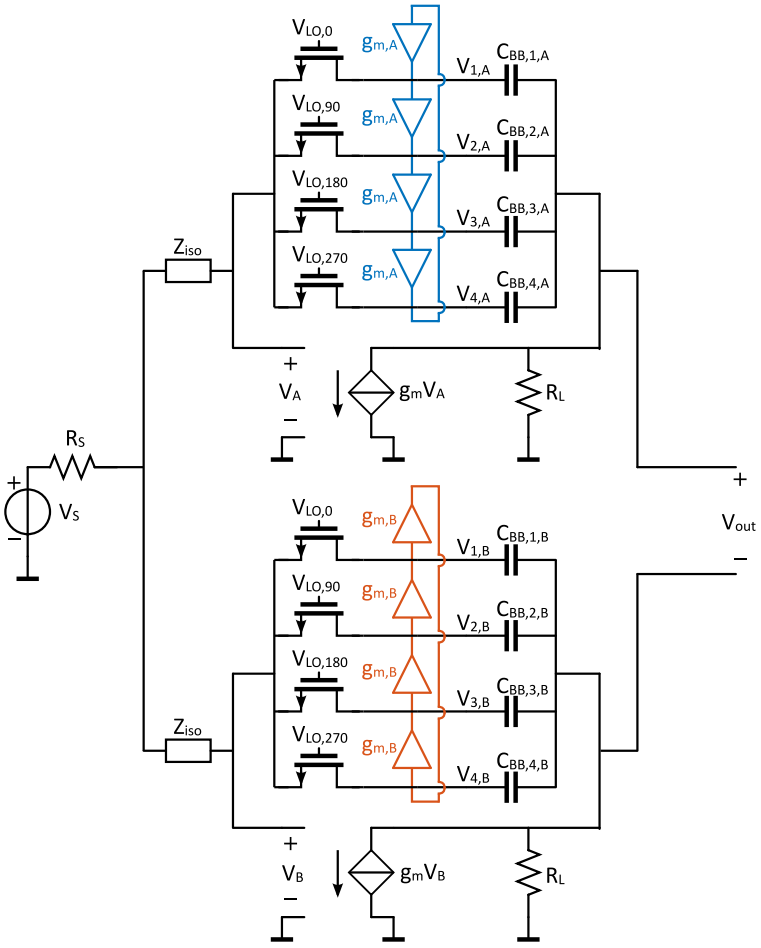


Figure 4.18: Circuit of the frequency shifted GB-NPF with g_m cells.

From eq. (3.4) it can be seen that a large Z_{in} requires a large Z_{NPF} and thus a small switch width. This also decreases the LO power consumption, but increases the noise from the NPF. A large NPF impedance ($Z_{\text{NPF}} \gg R_L$) simplifies the gain from eq. (3.1) to $|A_V| = g_m R_L$, with $R_L = r_O \| R'_L$. It is assumed that the LNA gain is limited to $g_m r_O$ = 5. As shown in Figure 4.19, a large g_m is required to achieve a large gain.

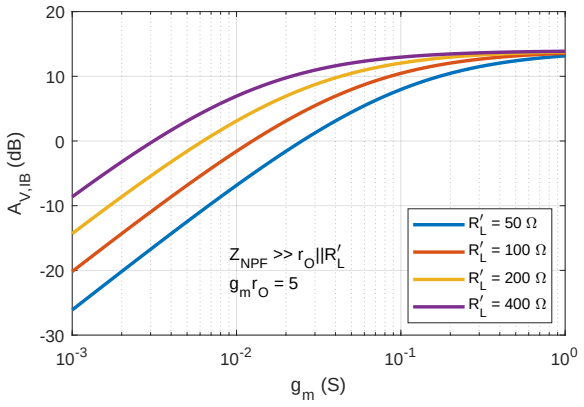


Figure 4.19: Calculated IB voltage gain for different values of g_m and R'_L.

For a large g_m, a gain of A_V = 5 (= 14 dB) can be achieved. This however has the disadvantage of a small Z_{in}, which can intuitively be understood from the Miller effect. The NPF impedance in the

feedback of the LNA can be seen as a shunt impedance at the input, reduced in value by $(1 + A_V)$. A larger gain therefore leads to a smaller Z_{in}. The LNA is designed to achieve a g_m of 30 mS and the NPF switch resistance is R_{sw} = 200 Ω. This is achieved by a switch width of 2 µm and length of 40 nm. The minimum length is used to minimize the parasitic capacitance of the switches and the LO power consumption. The IB NPF resistance (R_{sw} + R_{leak}) is 535 Ω.

With these parameters, the calculated gain of the single GB-NPF is 6.8 dB IB and 3.9 dB OOB (eq. (3.1)), resulting in 2.9 dB attenuation. The input impedance is calculated to be 170 Ω (eq. (3.4)).

Two switches per path

The non-ideal baseband capacitors will have a parasitic capacitance to ground on either side. The parasitic capacitance on the output node connects to the LNA and can reduce its gain [20]. A second set of switches is added to prevent this gain reduction by moving the parasitic capacitance to the baseband node instead of the RF node, thereby increasing its shunt impedance to ground at the signal frequency (100 MHz at the baseband node versus 28 GHz at the RF node). This however increases the LO power consumption by a factor 2 for the same switch size and by a factor 4 when the switch size doubles to keep the same R_{sw} of two switches in series. The width of the individual switches is doubled to 4 µm, to reduce the noise contribution of the NPF.

4.4.2. Gm cells

Ideal gm cells

To shift the two NPFs from their center frequency of $f_{\text{LO}} - f_{\text{offset}}$, g_m cells with a transconductance of roughly $g_{m,A}$ = 1.1 mS and $g_{m,B}$ = 900 µS are needed. With only one switch per path, the return current of the g_m cell could flow through the common node at the output of the NPF, which connects all baseband capacitors. With two switches per path, the output node is only connected to one path at the same time, while the return current should be able to flow continuously. Differential g_m cells are therefore used to replace the single-ended cells. These are connected, as shown in Figure 4.20.

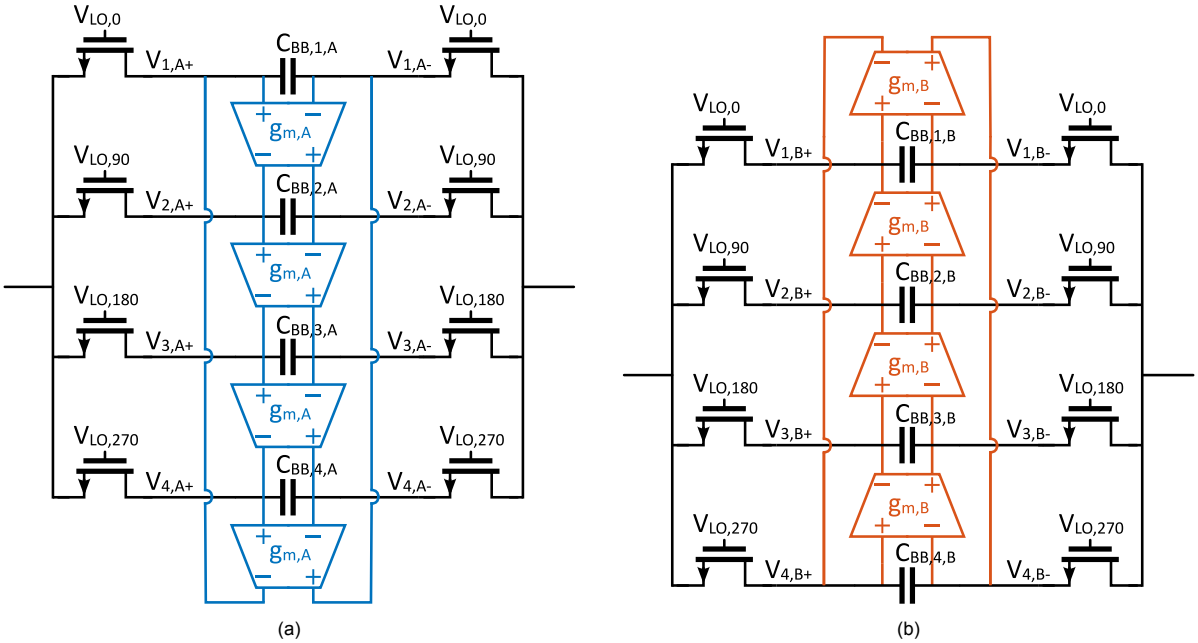


Figure 4.20: NPF with two switches per path and differential g_m cells to provide (a) a positive and (b) a negative center frequency shift.

Inverter-based implementation

The g_m cells are implemented by the differential transimpedance amplifier used in [26], because of its low NF and low power consumption. The circuit is shown in Figure 4.21. M_{cm1} and M_{cm2} implement a common-mode (CM) feedback, which works as follows. An increase in CM voltage at the output

reduces $|V_{GS}| - |V_{TH}|$ of $M_{cm1,2}$. This reduces the current in both paths of the inverter, thereby reducing the CM at the output voltage. A differential voltage will have no change on the total current through the CM transistors, since one current increases while the other decreases.

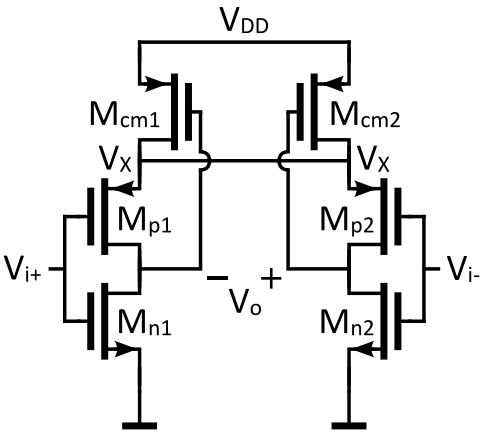


Figure 4.21: Circuit of the differential g_m cell, implemented as a transimpedance amplifier.

The parasitic capacitances and resistances of the g_m cell cause leakage between the paths of the NPF and to ground. The capacitances are minimized by using a small transistor length, while the output resistance of the inverter transistors is kept large by designing for a large g_m/I_D efficiency.

In order to keep all transistors saturated, the supply voltage must be raised to V_{DD} = 1.2 V.[4] The bias of the input nodes is arranged by a feedback resistor between the output and input node of each inverter as shown in Figure 4.22. The CM transistors are implemented as normal `pmos_rf` devices, while the other transistors are low threshold voltage devices implemented by `nmos_rf_lvt` and `pmos_rf_lvt`. Because of the voltage drop over $M_{cm1,2}$, the voltage on node X is smaller than V_{DD}. This reduces the V_{GS} of the inverter transistors. Using low V_{TH} devices ensures that $V_{GS} > V_{TH}$. The width of $M_{p1,2}$ is selected to provide the same g_m as $M_{n1,2}$. The width of the CM transistors is designed to make $|V_{DS}| - V_{Dsat}| > 0$. A smaller width increases the voltage drop over these transistors and decreases V_X. This results in a smaller V_{GS} of the inverter transistors. The width of $M_{cm1,2}$ is selected to result in the largest min $\left(|V_{DS,cm}| - V_{Dsat,cm}|, |V_{GS,p}| - |V_{TH,p}|, V_{GS,n} - V_{TH,n}\right)$. The resulting sizes of the g_m cell transistors for the two NPFs are shown in Figure 4.22.

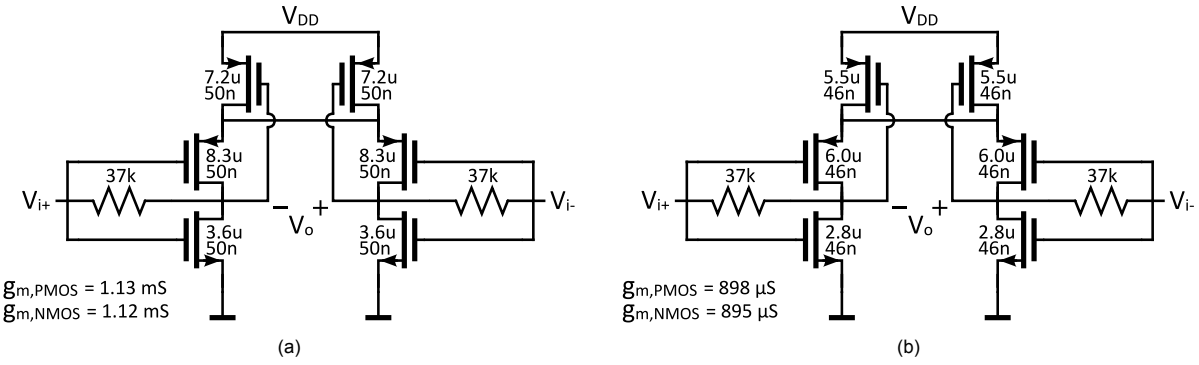


Figure 4.22: Differential g_m cell circuits with the used transistor width and length, to provide (a) a positive frequency shift to NPF A and (b) a negative frequency shift to NPF B.

Results

The obtained frequency shift is visible in the simulated NPF impedance in Figure 4.23. The filters from Figure 4.20 are simulated with one side connected to ground. The g_m cells shift the frequency as desired, but also reduce the impedance due to additional capacitive leakage to ground.

[4] The available voltage range for the amplifier will be smaller than 1.2 V, due to the (small) voltage drop over the bondwires. The amplifier is simulated with bondwires in the final circuit and all transistors are saturated.

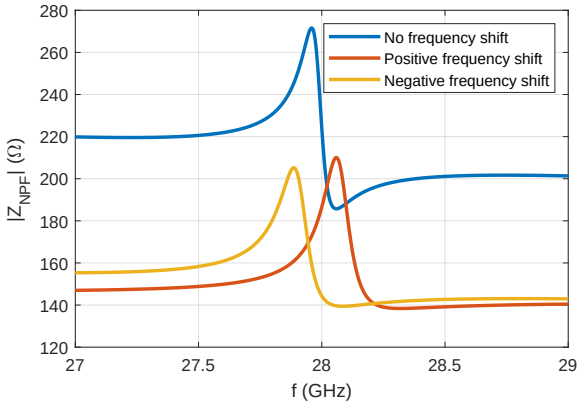


Figure 4.23: Simulated NPF impedance versus frequency for the filters in Figure 4.20, with and without the frequency shifting g_m cells. One side of the filter is grounded, while simulating Z_{11} with a port on the other side.

4.4.3. LNA of gain-boosted N-path filter

The main task of the LNA is to provide a sufficiently large g_m and r_O, to achieve a high gain of the GB-NPF. Since this LNA is connected to the filter input, the blockers are not yet fully suppressed[5], demanding a high linearity. Because of the required large input impedance of the GB-NPF, the LNA itself must also have a large Z_{in}. A CS topology is selected for its high linearity and large input impedance. The drain current of the LNA is provided through the load inductor L_D, as shown in Figure 4.24a. An inductor is used for two reasons. First of all, it has a lower voltage drop than a resistor for the same DC current. Secondly, it can resonate out the capacitance at the output node to provide gain at a high frequency [31]. The input bias voltage of the CS transistor is selected with the aid of the simulated g_m/I_D and g_m as shown in Figure 4.24b. A small width is desired to minimize the parasitic capacitances. The combination of a large g_m and a small width can be achieved by using a large V_{GS}, at the cost of a larger power consumption as shown by the g_m/I_D curve. From Figure 4.24b it can also be seen that a too large V_{GS} only results in a small increase in g_m, while the current keeps increasing at the same rate. An input bias voltage of 910 mV is selected to be used for the CS LNA. This voltage provides a large g_m, while not increasing the consumed current further than needed.

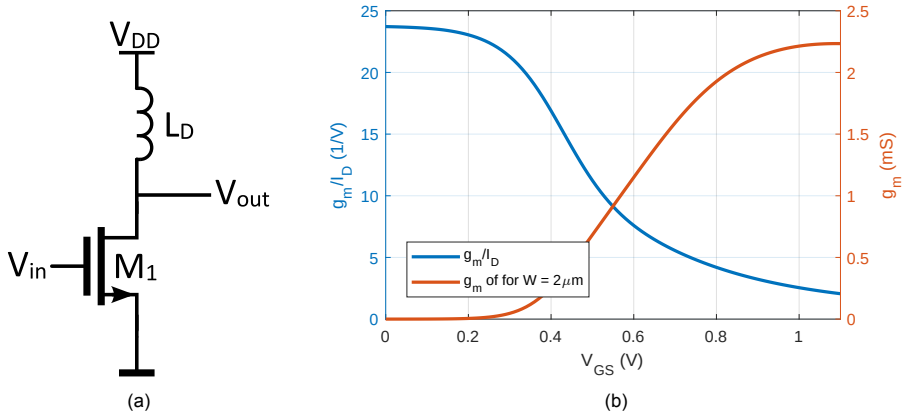


Figure 4.24: (a) CS amplifier with (b) g_m/I_D efficiency and transconductance for different gate voltages of a single CS stage.

This CS stage is compared to a cascode amplifier, as shown in Figure 4.25. A CS with a cascode transistor can provide an increased r_O for the same g_m. When implemented at mm-wave with a small supply voltage, however, the maximum input bias voltage is limited. This requires a larger width to obtain the same g_m, thereby increasing the parasitic capacitances which limit the reverse isolation and output impedance at RF. The cascode transistor M_2 is biased by voltage V_b which can be maximum V_{DD} = 1.1 V. To keep both transistors saturated, the input voltage must be $V_{\text{in}} \geq V_{\text{TH1}}$. The required

[5] There is some attenuation at the input due to the frequency-dependent input impedance of the GB-NPF. The majority of the attenuation is however achieved in the gain and therefore only visible after the filter.

voltage on node X is $V_X = V_{GS1} - V_{TH1} + V_{ov1}$, where V_{ov1} is the overdrive voltage of M_1. The cascode transistor is saturated when

$$V_b \geq V_X + V_{GS2} = V_{GT1} + V_{ov1} + V_{GT2} - V_{TH2}, \tag{4.3}$$

where $V_{GT} = V_{GS} - V_{TH}$. Assuming a threshold voltage of V_{TH} = 600 mV and an overdrive voltage of V_{ov} = 100 mV, the maximum V_{GT} can be calculated as

$$V_{GT1,2} \leq \frac{1}{2}(V_b - V_{ov1} - V_{TH2}) \tag{4.4}$$

which is 200 mV for the above mentioned assumptions. For a V_{TH} of 600 mV, the maximum input bias voltage is 800 mV. Compared to the 910 mV used for the CS stage, this reduces the g_m per unit width with 10%. A larger width is required to provide the same g_m, which increases the parasitics. The cascode architecture also increases the input-referred noise, because of the added noise of the common-gate (CG) transistor [32]. Because of these two reasons, the CS architecture is selected to be used in the GB-NPF.

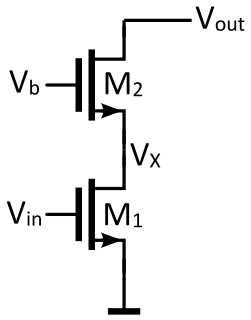


Figure 4.25: Cascode amplifier.

The input impedance of the amplifier must be large. This impedance can be increased by adding a source degeneration inductor to the CS transistor, as shown in Figure 4.26. This, however, reduces the gain, because the effective g_m decreases for a larger impedance connected to the source [33], according to eq. (4.5) and is therefore not used.

$$G_M = \frac{g_m}{1 + g_m s L_S} \tag{4.5}$$

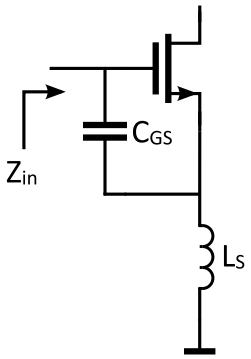


Figure 4.26: CS amplifier with inductive source degeneration.

In order to increase the input impedance of the filter, a relatively small NMOS width is used for the LNA, in combination with high-resistance NPF switches. The final GB-NPF circuit with the component sizes is shown in Figure 4.27. The bias voltages are shown in green. Because of the g_m cell bias voltages of 500 mV, the LO signals are increased to swing between 0.55 and 1.65 V. The bias of the LNA is separated from that of the NPF by two large capacitors. One at the input of the LNA and one at the output of the NPF.

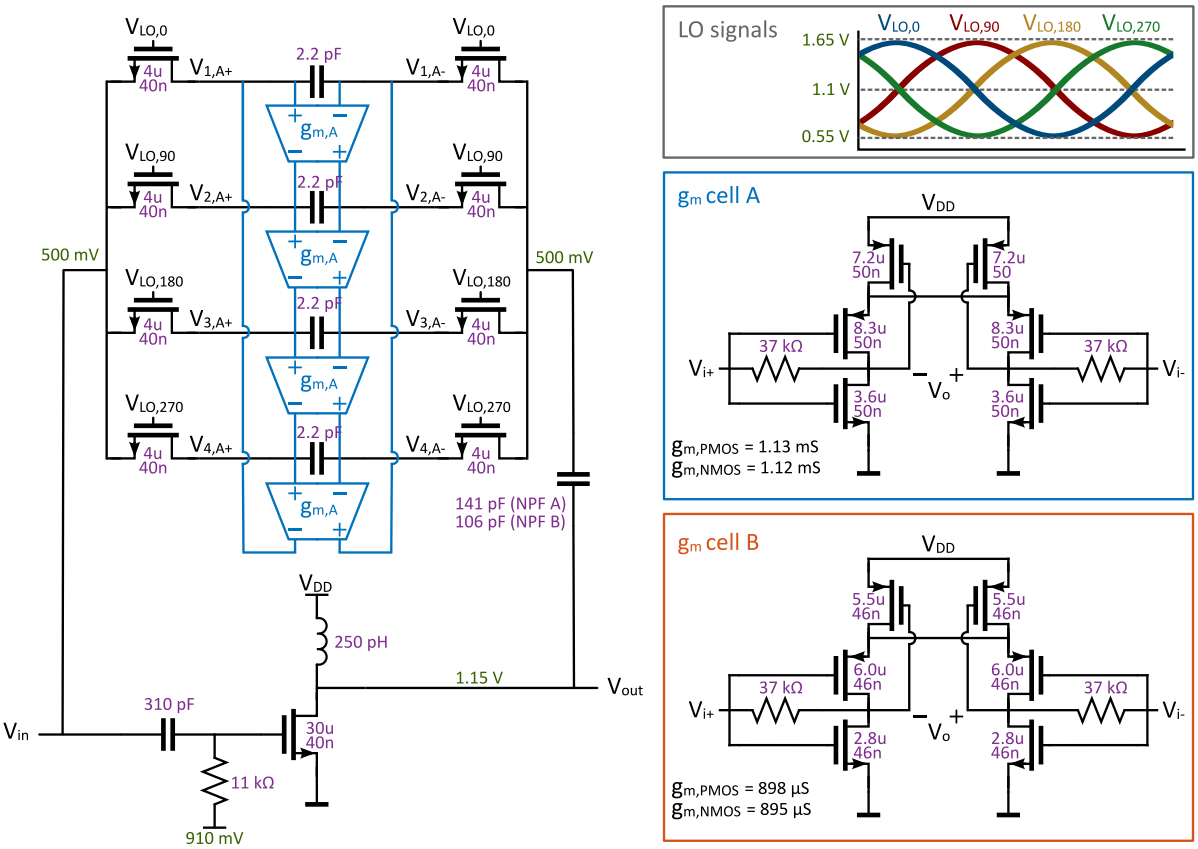


Figure 4.27: Schematic of the single frequency shifted GB-NPF with g_m cells. The component sizes are annotated in purple. The bias voltages are shown in green.

4.4.4. Output subtraction

A single GB-NPF only has a limited attenuation. The outputs two frequency-shifted filters are subtracted to provide a large OOB attenuation, while keeping a decent IB gain. Figure 4.28 shows the principle of the subtraction. In the left two plots, the output voltage and phase of both filters is shown. Because of the phase difference for IB signals, the subtraction of the two signals leads to a relatively large output voltage, as shown in the phasor diagrams. The OOB voltages, in contrary, are almost equal in magnitude and phase, resulting in a small output voltage and therefore a large OOB attenuation.

For an ideal IB phase difference of $\phi = 180°$, the subtraction effectively is an addition and the output voltage will be $|V_{out}| = |V_{out+}| + |V_{out-}|$. In reality, the phase difference is significantly smaller[6], resulting in $|V_{out}| \ll |V_{out+}| + |V_{out-}|$.

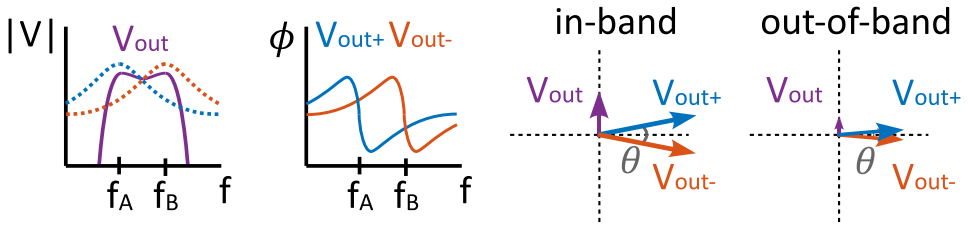


Figure 4.28: Output voltage and phase of both paths (V_{out+}, V_{out-}), which results in V_{out} after subtraction. The subtraction of the IB and OOB voltage can be explained using a phasor diagram.

The subtraction is implemented with a transformer, as shown in Figure 4.29. The primary inductance L_p also implements the two 250 pH drain inductors of the LNAs and is therefore connected to V_{DD} with

[6]The phase difference obtained by the designed filter is only $29°$.

its center tap. The maximum implementable inductance at 28 GHz is assumed to be 500 pH[7]. The achievable coupling coefficient k is assumed to be 0.6. Capacitors are added to tune the resonance to 28 GHz, without increasing the required inductance to more than 500 pH. These capacitors are partially embedded in the design of the transformer and partially added as separate components, as discussed in Chapter 6.

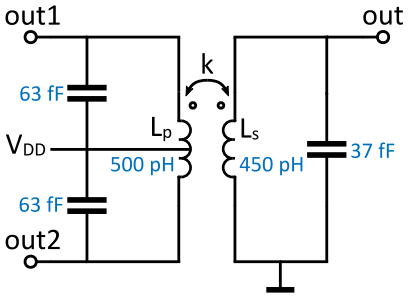


Figure 4.29: Model of output transformer, used for subtraction of the two paths, with required capacitances for matching.

The turn ratio, $n = \sqrt{L_s/L_p}$, determines the passive voltage gain of the transformer [34]. A larger n results in a larger output voltage as defined in eq. (4.6).

$$V_{\text{out}} = n(V_{\text{out},1} - V_{\text{out},2}) \tag{4.6}$$

A larger turn ratio, however, at the same time decreases the load impedance seen from the primary side, thereby reducing the voltage gain of each GB-NPF.

$$Z_{L,p} = \frac{Z_{L,s}}{n^2} \tag{4.7}$$

An optimum is found at $n = 1$, for which the filter gain is the largest. Implementing this with a real transformer requires two unequal inductances, which is why the secondary inductor is reduced to 450 pH.

4.4.5. Input isolation and matching

Two GB-NPFs are connected to the same input node. Inside these filters, the baseband capacitors are one by one connected to the input. While the charge sharing between these capacitors in each separate NPF is limited by selecting a large enough LO bias voltage, the capacitors of the two filters are still connected to each other. The baseband voltages of each filter are different due to the frequency offset. This results in unwanted charge sharing between the two filters, reducing their gain.

The input signal can be split by adding two amplifiers at the input, but this limits the linearity of the filter, or by splitting the clock signals to 8-phase T/8 duty cycle clocks which alternately turn on the first and second NPF switches [18]. This requires complex clock circuitry and when implemented with sine waves, the isolation between the paths reduces. The charge sharing is limited by adding an isolation impedance in series with the input of each path, as shown in Figure 4.18 [18]. This isolation impedance can be implemented by a resistor, capacitor or inductor, as long as the impedance at 28 GHz is large compared to the source impedance, $Z_{\text{iso}} \gg Z_S$. A resistor adds a large amount of noise, making it the least favorable option. The capacitor and inductor are compared in this section.

Comparison between capacitive and inductive isolation

The two filters are isolated by capacitors for the sake of simplicity in [18]. The disadvantage of using C_{iso} is the reduced gain and therefore the increased NF of the filter, due to capacitive voltage division between the isolation capacitor and the parasitic capacitance at the input node of the GB-NPF [35]. The capacitive isolation is compared with inductive isolation to find the best option for large gain and a low NF. The isolation impedance must be larger than the source impedance, which is the output impedance of the first stage ($R_{\text{out},1}$ = 141 Ω), see Chapter 5. A capacitor with $|Z_C|$ = 200 Ω is used. For a center

[7] Maximum expected inductance at 28 GHz which can have a self-resonance frequency (SRF) of at least 60 GHz and a Q of at least 12.

frequency of 28 GHz, the capacitor size is 30 fF. The inductive isolation must be done with L_{iso} = 1.1 nH to achieve an impedance of 200 Ω. This is however larger than the maximum expected implementable inductor at 28 GHz, which is 500 pH. The capacitive isolation is compared to the inductive isolation with 1.1 nH and with 500 pH. The matching network to provide a real input impedance of 155 Ω is shown in Figure 4.30.

Component	C_{iso}	L_{iso}	
Z_{iso}	30 fF	1.1 nH	500 pH
Z_s	35 fF	100 fF	63 fF
Z_{p1}	-	-	450 pH
Z_{p2}	500 pH	53 fF	-

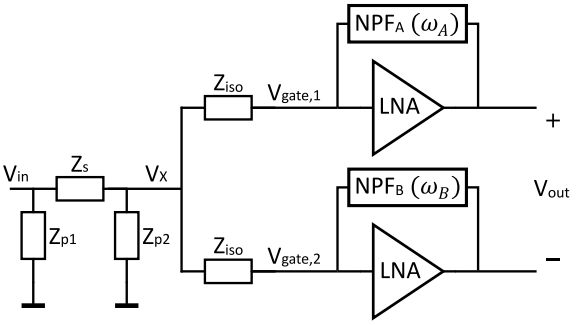


Figure 4.30: Input isolation and matching network of the frequency shifted GB-NPF with component values for capacitive and inductive isolation.

The circuit is simulated with the LNA, implemented by a CS transistor with a drain inductor, and the NPF, implemented by an ideal R-RLC model, as shown in Figure 2.5. The resulting voltage gain V_{out}/V_{in} for the capacitive isolation is -5.5 dB. For the inductive isolation with 1.1 nH, this is increased to -1.5 dB. For the inductor of 500 pH, the voltage gain is still -1.5 dB, which did not reduce because of the change in the matching network (Figure 4.30). The difference in gain is investigated by comparing the magnitude and phase of the gain of each GB-NPF, as shown in Figure 4.31. A large output gain (after subtraction of the two paths) is achieved for a large gain and phase difference. When using inductive isolation, at the center frequency of one path, the gain of the of the other path is almost at its minimum value as shown in Figure 4.31a. For capacitive isolation however, the difference in gain is much smaller, while the peak gain of each path is comparable. A larger C_{BB} to increase the roll-off of each path did not increase the total gain. When looking at the phase difference of both paths, a large difference is again obtained for inductive isolation (36.4°), while capacitive isolation results in a smaller phase difference (17.2°).

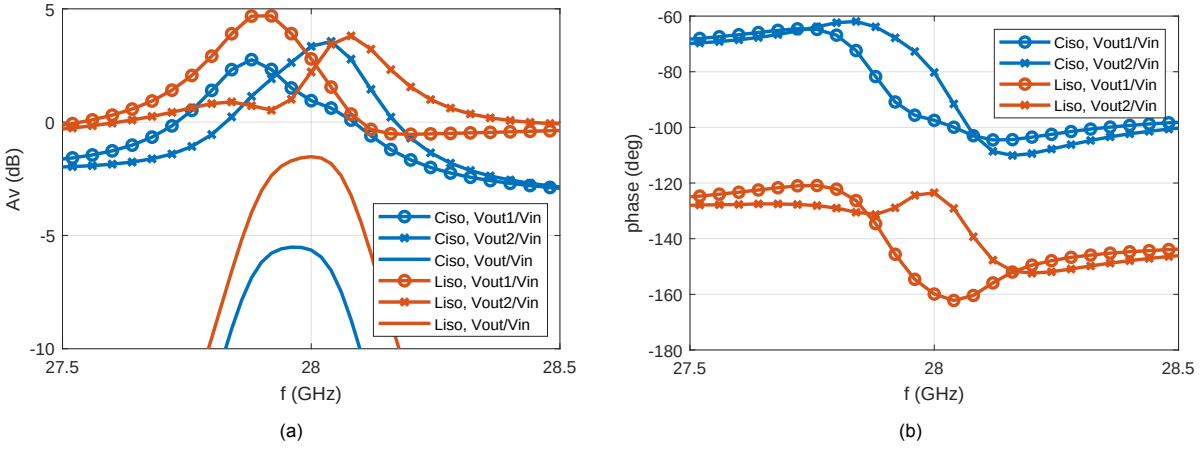


Figure 4.31: Simulated (a) magnitude and (b) phase of the gain from input to the output of both GB-NPFs and the output of the full filter. The inductive isolation is simulated with L_{iso} = 500 pH.

Besides the gain reduction, capacitive isolation also causes an increase in noise figure. Inductive isolation is used for its reduced NF and increased gain. The isolation inductors are 500 pH, since this is the expected maximum implementable inductor at 28 GHz.

4.4.6. Noise analysis

A large NF is inherent to the subtraction in this architecture [18]. Due to the subtraction of two signals with a non-ideal phase difference of $\phi < 180°$, the output voltage is smaller than that of each individual path (Section 4.4.4). The signal voltages of both paths thus reduce in magnitude, while their independent noise powers get added by the subtracting transformer. This increases the NF compared to two independent GB-NPFs. This section discusses the noise contributions of the different circuit elements, after which several methods are described to reduce the NF.

A large part of the noise comes from the g_m cells for the frequency shift, as expected from [18]. Because of the small required g_m, the width of the g_m cell transistors is made small, which results in a large noise contribution. The differential g_m cells provide a twice as large input referred noise voltage compared to single ended g_m cells, because of the doubled number of inverter transistors. The noise of the g_m cells is reduced by increasing the transistor width and thus the g_m value. The frequency shift is kept constant by also increasing C_{BB}. Increasing the transistor width and the size of C_{BB} both increases the parasitic capacitance at the baseband nodes, which reduces the gain of the filter [20]. A smaller gain increases the NF, so an optimum multiplication factor of 1.6 and 1.5 for the g_m cell width and C_{BB} respectively is found, which results in the lowest NF.

The noise of the NPF switches is reduced by 1.8 dB by increasing their width from 2 µm to 4 µm. A too large width reduces R_{NPF} too much to keep a large input impedance. From schematic simulations, the noise contribution of each component is found. These contributions are categorized in Table 4.1. The final component values are as mentioned in the previous sections.

Table 4.1: Simulated contributions to the input noise voltage in the frequency shifted GB-NPF at 27.96 GHz.

Component	Input noise voltage (V^2/Hz)
LNAs	5.26×10^{-18} (24.8%)
NPF switches	7.26×10^{-18} (34.2%)
frequency shifting g_m cells	5.02×10^{-18} (23.6%)

4.5. Results

The full NPF is simulated with ideal components[8]. The full circuit of the filter is shown in Figure 4.32.

Gain and attenuation

A voltage gain of -2.0 dB is achieved as shown in Figure 4.33a. The filter has a flat IB gain with a ripple of less than 0.1 dB. The attenuation at the center of the adjacent channel is 16.0 dB and 24.1 dB for the left and right channel respectively. The far OOB attenuation is 16.2 dB at 26 GHz and 14.4 dB at 30 GHz.

[8] Schematic components are used. Inductors have a quality factor of 12. Resistors and capacitors are ideal. Transistors are the RF schematic components from Taiwan Semiconductor Manufacturing Company (TSMC) (`nmos_rf` for the NPF switches and LNAs, `nmos_rf_lvt` and `pmos_rf_lvt` for the g_m cell inverter transistors, and `pmos_rf` for the g_m cell CM transistors).

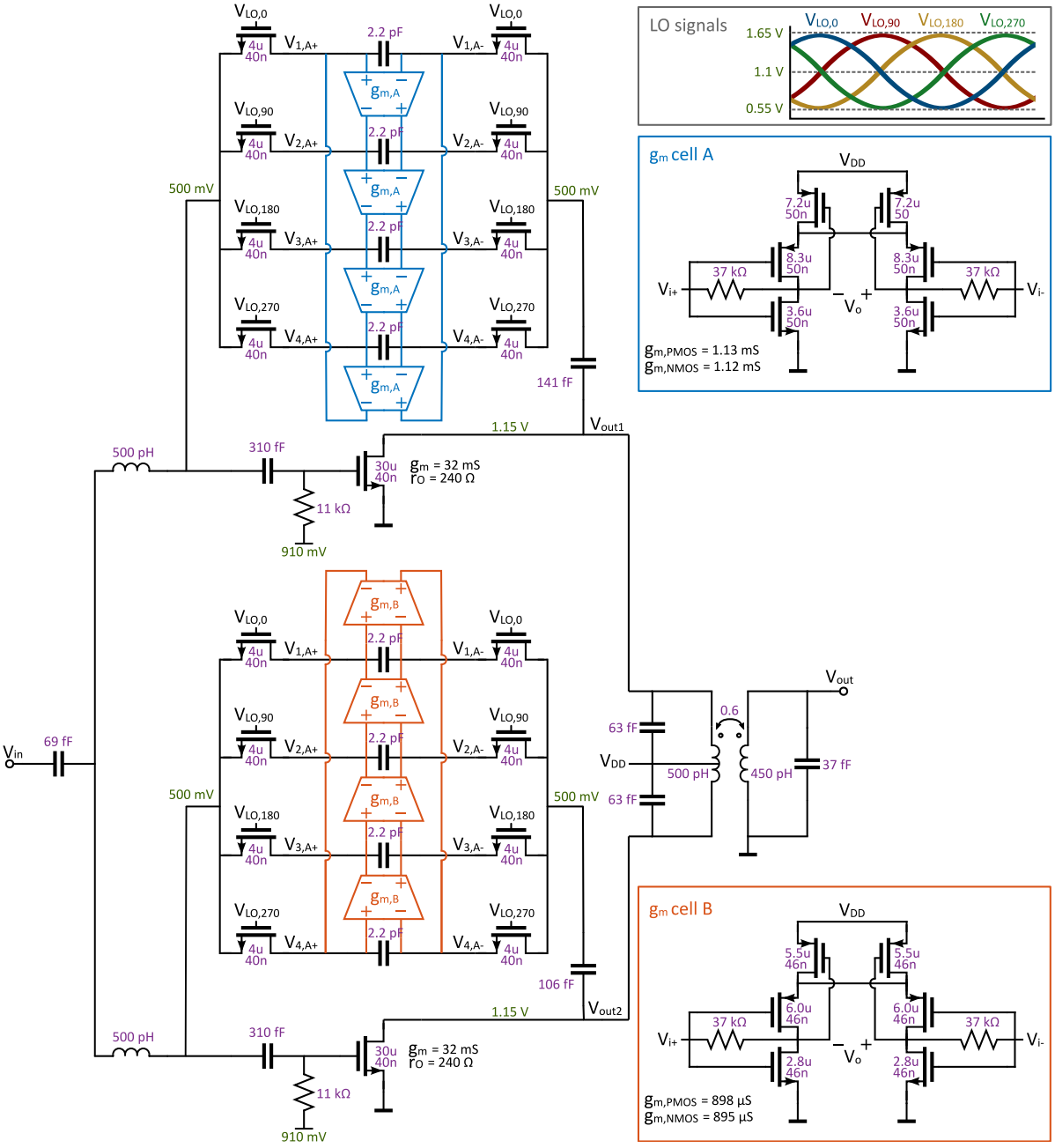


Figure 4.32: Schematic of the full filter consisting of two frequency shifted GB-NPFs, which are subtracted at the output. The component sizes are annotated in purple. The bias voltages are shown in green.

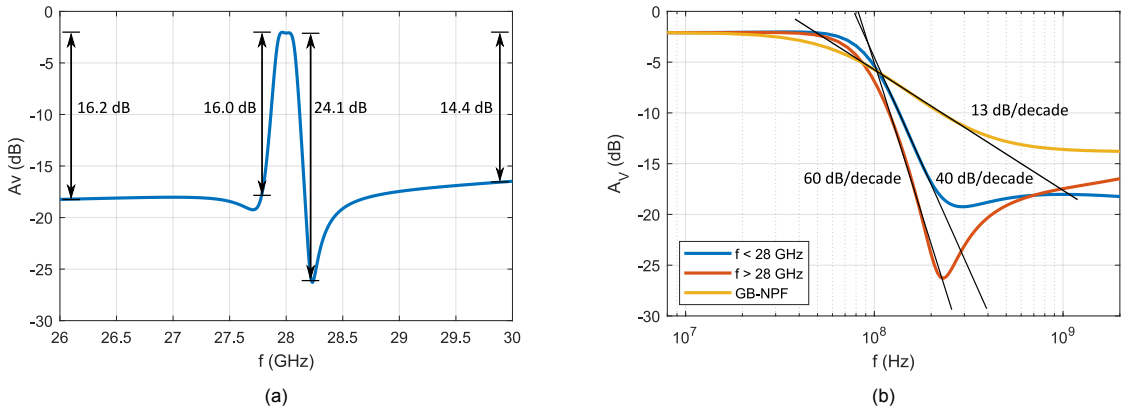


Figure 4.33: (a) Simulated voltage gain of the frequency shifted GB-NPF with ideal components. (b) Achieved roll-off of the simulated filter gain.

The achieved roll-off of the filter is shown in Figure 4.33b. For the lower side of f_{LO}, the roll-off is 40 dB/decade, as expected for the fourth-order BPF. The roll-off at the upper side of the band is 60 dB/decade, due to the low gain around 28.25 GHz. This low gain, after subtraction of the two filters, is caused by the equal gain and phase of these filters. Figure 4.34 shows the gain and phase of the two paths and indeed shows an equal gain and phase at approximately 28.25 GHz. This results in a zero in the transfer function of the complete filter. The limited far-OOB attenuation is caused by the gain and phase difference of the two paths at frequencies far away from the main band. The roll-off is compared to that of the single GB-NPF. Theoretically, this filter can achieve an attenuation of 20 dB per decade. However, due to the limited far-OOB attenuation, the roll-off only reaches a value of 12 dB per decade.

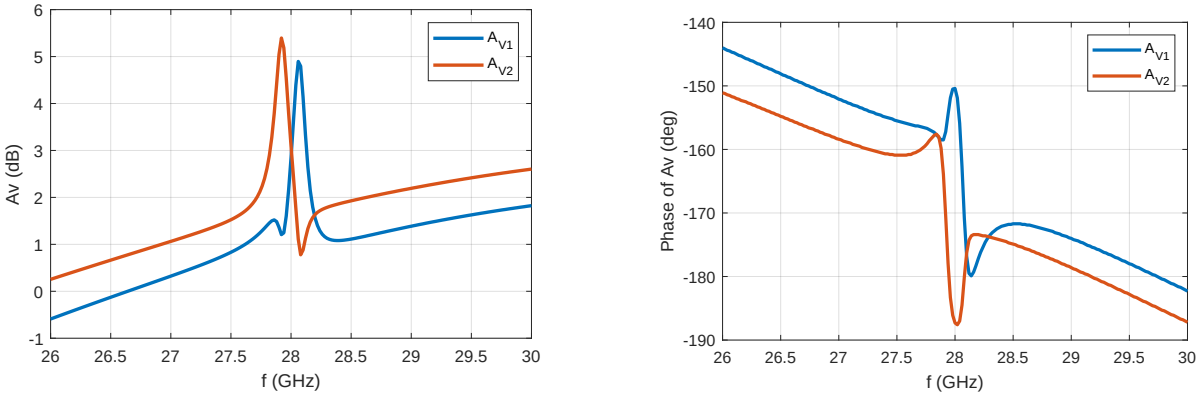


Figure 4.34: Simulated (a) voltage gain and (b) phase of the two frequency shifted GB-NPFs with ideal components. These signals are subtracted to obtain the voltage gain of Figure 4.33a.

The attenuation of this filter is compared to a simple NPF and GB-NPF in Figure 4.35. The -3 dB BW of the GB-NPF is designed to be 200 MHz, the same as the frequency shifted filter. The far OOB attenuation is improved by 4.0 dB compared to the GB-NPF, while the center of the adjacent channel experiences at least 8.2 dB more suppression. Besides the increased attenuation, the frequency shifted filter also results in a flat IB response compared to the GB-NPF.

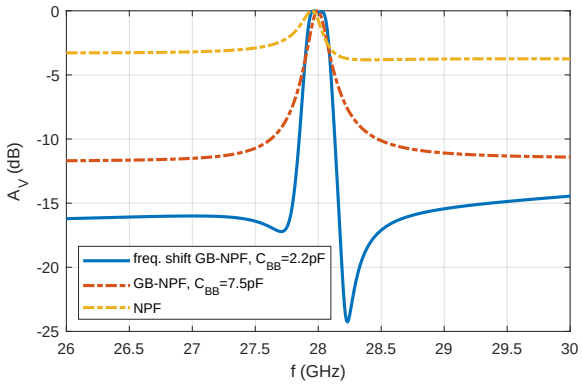
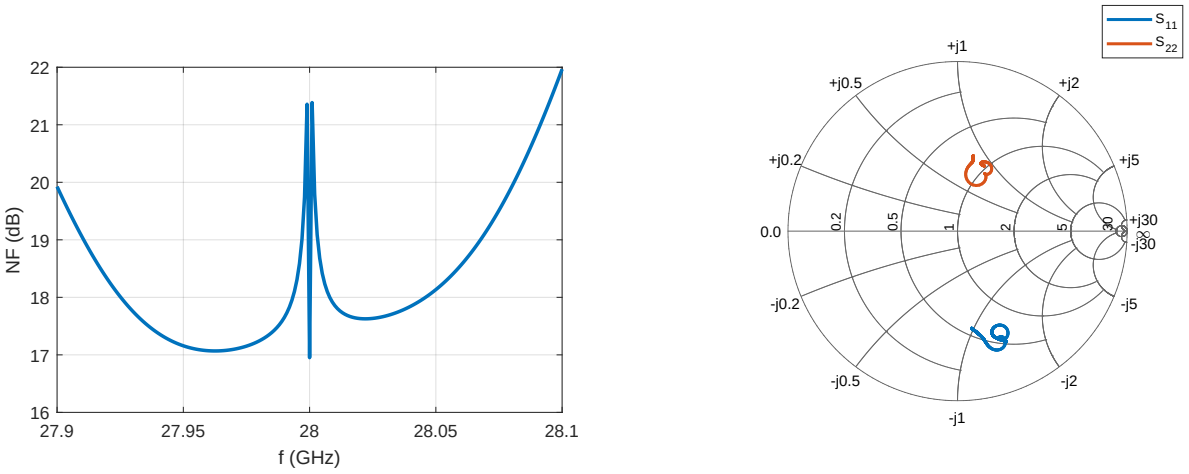


Figure 4.35: Normalized voltage gain of the frequency shifted GB-NPF compared to the standalone NPF and GB-NPF.

Noise figure and impedance matching

The simulated NF is included in Figure 4.36a. The large NF of 17.0 dB is partially inherent to this filter topology. The output subtraction reduces the signal power, while the noise powers from both paths are independent and therefore get added at the output, which increases the NF. The large noise around f_{LO} is the upconverted flicker noise of the NPF transistors.



(a) (b)

Figure 4.36: (a) Simulated noise figure of the frequency shifted GB-NPF with ideal components. The noise figure is large at f_{LO} due to the upconverted flicker noise. (b) Simulated input and output reflection coefficients from 26 to 30 GHz and. The input impedance is made real by the shunt inductor at the output of the first stage. The output impedance is made real by the shunt load capacitor. The noise figure is large at f_{LO} due to the upconverted flicker noise.

The input and output reflection coefficients are shown in Figure 4.36b. The imaginary part of the input and output impedances is resonated out by the shunt inductor at the output of the first stage and the load capacitor respectively.

4.5.1. Linearity

The input referred third-order intercept point (IIP_3) is simulated with two input signals at

$$\begin{aligned} f_1 &= f_{LO} + \Delta f \\ f_2 &= 2\,(f_{LO} + \Delta f) - f_{IM3} \end{aligned} \tag{4.8}$$

where f_{IM3} is the frequency of the third-order intermodulation distortion ($f_{IM3} = 2f_1 - f_2$). This frequency is set to 28.03 GHz. Δf is changed to see the effect of IB and OOB signals on the IIP_3. The IIP_3 is calculated by [31]

$$IIP_3|_{dBm} = \frac{\Delta P|_{dB}}{2} + P_{in}|_{dBm}, \tag{4.9}$$

Where $\Delta P|_{dB} = P_{in}|_{dBm} - P_{IM3,in}|_{dBm}$, with $P_{IM3,in}|_{dBm} = P_{IM3,out}|_{dB} + 10 - G_{IM3}|_{dB}$, resulting in

$$IIP_3|_{dBm} = \frac{P_{in}|_{dBm} - (P_{IM3}|_{dB} + 10 - G_{IM3}|_{dB})}{2} + P_{in}|_{dBm}. \tag{4.10}$$

The simulated IIP_3 is shown in Figure 4.37a for different values of Δf. Figure 4.37b shows the simulated blocker power at 1 dB IB gain compression point (B_{1dB}) for different blocker frequencies. This shows the effect of an OOB blocker on the gain compression point of a desired signal of -50 dBm at 28.05 GHz.

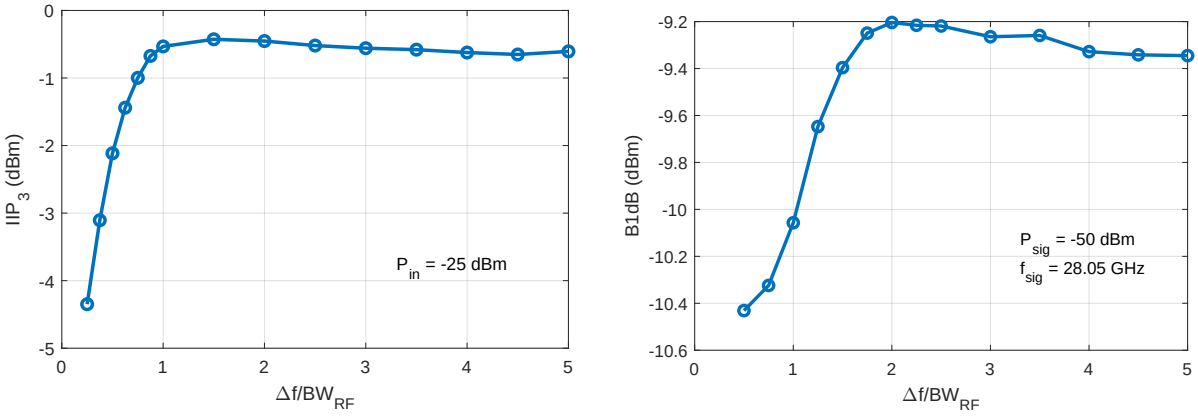


Figure 4.37: Simulated (a) IIP_3 and (b) B_{1dB} for different frequency offsets compared to f_{LO}. The frequency offset, Δf, is the offset of the first tone in the two tone IIP_3 test, and equals the blocker frequency in the B_{1dB} simulation. The plots show the frequency offset relative to the RF BW (200 MHz), to compare the results to the state-of-the-art.

The simulated IB IIP_3 is -4.5 dBm. The OOB IIP_3 is -0.5 dBm at $\Delta f/BW_{RF}$ = 1. The obtained B_{1dB} is -10.1 dBm at $\Delta f/BW_{RF}$ = 1 and -9.2 dBm at $\Delta f/BW_{RF}$ = 2. The IP_{1dB} is simulated with only one tone at 28.05 GHz and is found to be -7.3 dBm.

4.6. Conclusion

An NPF with a steep roll-off of 40 dB and a flat IB response is designed. This filter consists of two GB-NPFs with a frequency offset. The subtraction of these two filters results in a large attenuation, due to their comparable OOB gain. The frequency shift is implemented by moving charge between the baseband capacitors with differential g_m cells. A CS amplifier is used in the GB-NPF, of which the drain inductor is combined with the output transformer. Charge leakage between the two filters is prevented by adding isolation inductors at the input. The resulting filter has an IB gain of -2.0 dB and an attenuation in the center of the first adjacent channel of 16.0 dB. The far OOB attenuation is 14.4 dB. Compared to the simple GB-NPF, the attenuation in the adjacent channel is improved by 8.0 dB, while simultaneously providing a flat IB response with less than 0.1 dB IB ripple. The achieved noise figure is large with 17.0 dB, which is inherent to the output subtraction of this architecture. An LNA will be added in front of the filter to suppress the noise, which will be designed in Chapter 5.

5

Low-noise amplifier

A fundamental problem of two filters with a frequency offset is the increased noise due to the output subtraction. When the outputs of the two GB-NPFs are subtracted, the signal reduces in amplitude, while the noise powers get added. The resulting large noise figure of the circuit can be reduced with an additional gain stage connected in front of the filter, as shown in Figure 5.1.

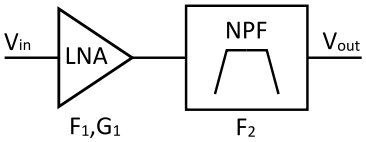


Figure 5.1: Toplevel view of two-stage circuit with LNA to reduce the noise figure.

The noise factor of the NPF, F_2, is attenuated by the gain of the first stage G_1. The total noise factor of the two-stage circuit is

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1}. \tag{5.1}$$

The noise factor of the additional LNA, F_1, should be small since it does not get attenuated by any gain. As a result of added gain, the signal and blocker powers are increased when arriving at the input of the NPF, increasing its linearity requirements. As shown in the results of Chapter 4, the lowest B_{1dB} is -10 dBm. For a maximum input power of -25 dBm, the voltage gain of the first stage can not be larger than 15 dB. The focus of the LNA design is to achieve a large gain to suppress the noise of the NPF. Besides that, a low noise figure and a flat gain between 26 and 30 GHz are also important.

The design is started with a comparison of the top-level topology of the two stages in Section 5.1. The effect of the first stage on the isolation between the two filters is investigated in Section 5.2, after which the topology of the LNA is selected in Section 5.3. Section 5.4 discusses the design of the LNA, of which the simulation results are presented in Section 5.5.

5.1. Top-level topology comparison

Two locations for the LNA are compared. One amplifier can be placed in front of the complete filter or each of the two frequency-shifted filters can have its own LNA. These two topologies are shown in Figure 5.2. Because of the reverse isolating properties of an LNA, the isolating inductors could be removed when using two LNAs. This section compares the gain and noise of the two topologies.

Gain comparison

The gain of each LNA can be defined as

$$A_V = g_m R_L, \tag{5.2}$$

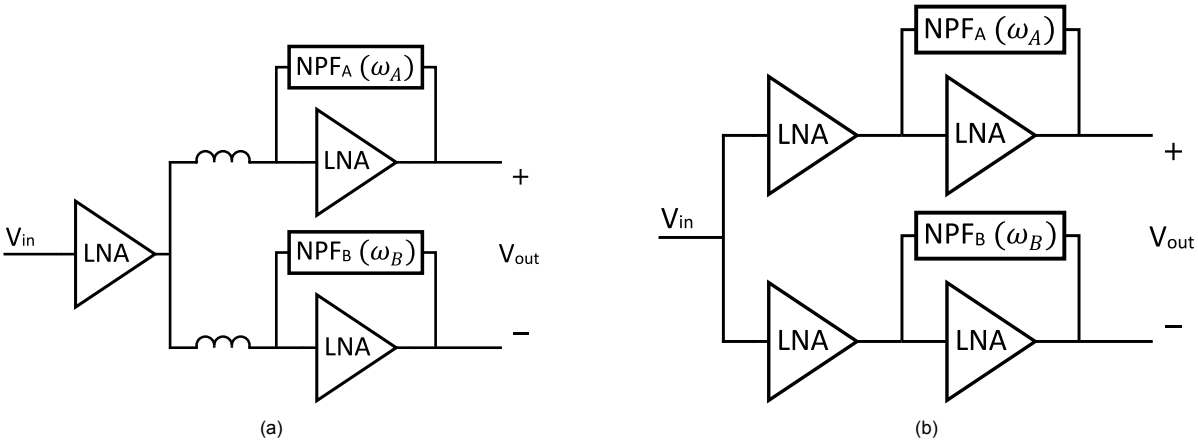


Figure 5.2: Two options of connecting an additional amplifier in front of the filter. (a) One LNA for the full filter. (b) One LNA per filter path.

with R_L the total resistance at the output node of the LNA. A large LNA output impedance and a large input impedance of the next stage are both needed to provide a large LNA gain. The achieved gain of the LNA in the two topologies can be calculated using the simplified small-signal models in Figure 5.3.

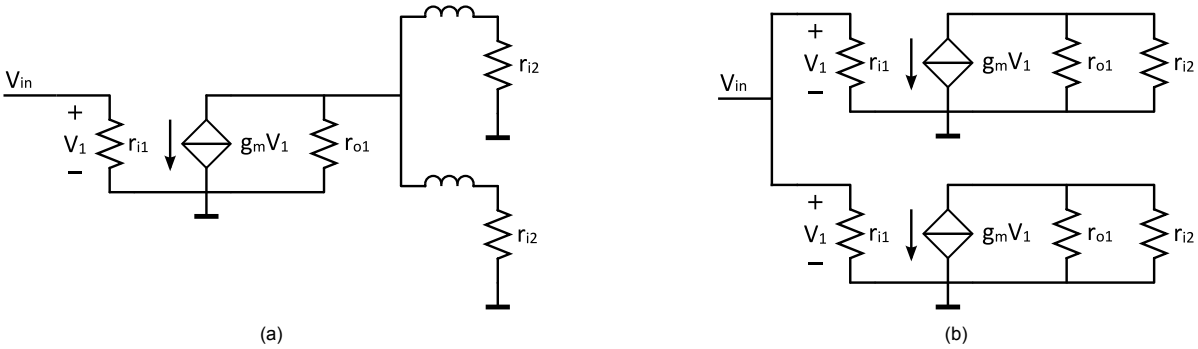


Figure 5.3: Simplified small-signal model to calculate the gain of the additional LNA(s). (a) One LNA for the full filter. (b) One LNA per path.

When using one LNA, the gain is

$$A_{V|1} = g_m \left(r_{o1} || \frac{r_{i2}}{2} \right). \tag{5.3}$$

The gain per LNA, when using two LNAs, is

$$A_{V|2} = g_m \left(r_{o1} || r_{i2} \right). \tag{5.4}$$

When designing both topologies for equal power consumption, the LNAs of the second topology must be decreases in size by a factor 2. This makes their gain equal to

$$A_{V|2} = \frac{g_m}{2} \left(2r_{o1} || r_{i2} \right) = g_m \left(r_{o1} || \frac{r_{i2}}{2} \right). \tag{5.5}$$

For an equal power consumption, the gain in both topologies is equal.

Noise comparison

The noise of the two circuits is, however, not equal. The contribution of the additional LNA(s) to the output noise voltage is calculated with the simplified circuit in Figure 5.4.

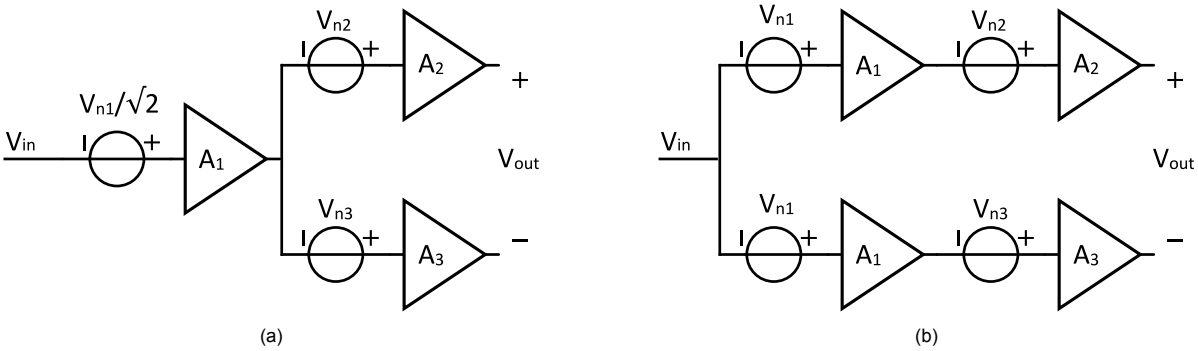


Figure 5.4: Simplified noise model to calculate the contribution of the additional LNA(s) to the output noise voltage. (a) One LNA for the full filter. (b) One LNA per filter path.

For the same power and gain, the size of the single LNA is double that of the two LNAs. This decreases its noise voltage by $1/\sqrt{2}$, as shown in Figure 5.4a. The output-referred noise voltage from the first-stage LNA in the first topology is

$$\overline{V_{n,\text{out}|1}^2} = \frac{\overline{V_{n1}^2}}{2} A_{V1}^2 \left(A_{V2} - A_{V3}\right)^2 . \tag{5.6}$$

The noise voltage of this LNA follows the same path as the signal through A_2 and A_3 and gets subtracted at the output. When using two separate LNAs with independent noise sources, their noise does not subtract, but adds, at the output. This results in a larger output noise voltage of

$$\overline{V_{n,\text{out}|2}^2} = \overline{V_{n1}^2} A_{V1}^2 \left(A_{V2}^2 + A_{V3}^2\right). \tag{5.7}$$

To conclude, both topologies can provide the same gain for equal power consumption. The single LNA topology, as shown in Figure 5.2a, gives the lowest noise contribution and is therefore selected to be used. This comes at the cost of increased chip area, since the isolation inductors are still required in this topology.

5.2. Effect of LNA on filter isolation

Without the first stage, the source impedance connected to the NPF is 50 Ω. This is replaced by the output impedance of the LNA which must be large to provide a large gain. The effect of this larger impedance on the isolation between the two filters is investigated. Depending on the baseband voltage of both filters, different leakage currents will flow. Three situations can be distinguished as shown in the simplified circuits in Figure 5.5.

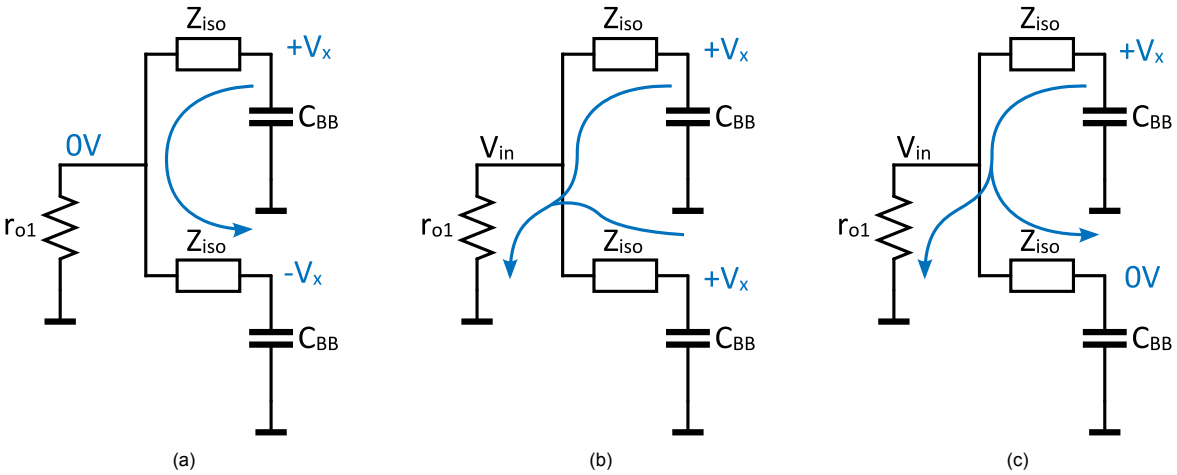


Figure 5.5: Leakage current from baseband capacitors for different baseband voltages.

When the baseband voltages are each other's inverse, the voltage at the input node will be 0 V and no current will leak through r_{o1}. This situation is shown in Figure 5.5a. The time constant of the leakage can be calculated as

$$\tau = 2Z_{\text{iso}}\frac{C_{\text{BB}}}{2} = Z_{\text{iso}}C_{\text{BB}} \tag{5.8}$$

and is independent on the size of r_{o1}. For equal baseband voltage, no current will flow between the two filters. All current leaks through the output resistance of the LNA, as shown in Figure 5.5b. Here, the size of r_{o1} partially determines the leakage time constant per path, which is

$$\tau = (Z_{\text{iso}} + 2r_{o1})\, C_{\text{BB}}. \tag{5.9}$$

An increased r_{o1} results in a larger time constant and thus a lower leakage current. In the third situation, the second baseband voltage is 0 V. The charge on the first baseband capacitor leaks both to ground and to the second baseband node. These two situations can be treated separately, as done in Figure 5.6. The time constant of situation 1 and 2 are

$$\tau = 2Z_{\text{iso}}\frac{C_{\text{BB}}}{2} = Z_{\text{iso}}C_{\text{BB}} \tag{5.10}$$

and

$$\tau = (Z_{\text{iso}} + r_{o1})\, C_{\text{BB}} \tag{5.11}$$

respectively. The second time constant is larger, thus the leakage current through r_{o1} to ground will be smaller than the leakage between the two filters. Increasing the output impedance of the LNA will again provide a larger time constant, resulting in a smaller leakage current. It can therefore be concluded that the addition of the first stage, with its large r_{o1} compared to the 50 Ω antenna impedance, improves the isolation between the two NPFs. It should, however, be noted that the isolation impedance Z_{iso} should remain large to maintain a good isolation.

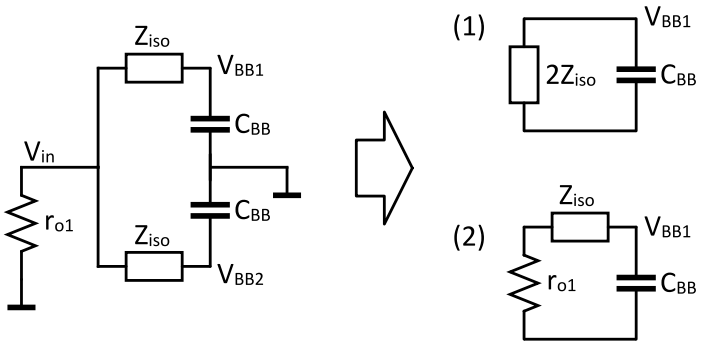


Figure 5.6: Equivalent circuit to analyze leakage time constant of the situation in Figure 5.5c. The leakage through the second isolation impedance (1) results in a different time constant than the leakage through the output impedance of the first stage (2).

5.3. LNA topology

The LNA should provide an input impedance of $50\ \Omega$ without the noise of a $50\ \Omega$ resistor. A CS stage can provide a lower NF than a CG amplifier, but it has a larger input impedance [31]. An inductor can be added in series with the source terminal to provide a real and frequency-independent part of the input impedance. The input impedance of the source degenerated CS stage in Figure 5.7 can be written as in eq. (5.12) [31].

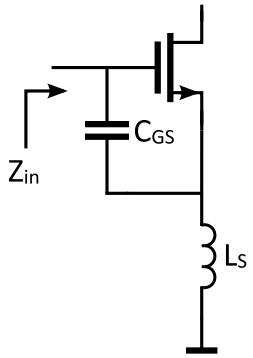


Figure 5.7: CS stage with source degeneration inductor L_S.

$$Z_{\text{in}} = \frac{1}{C_{\text{GS}}s} + L_S s + \frac{g_m L_S}{C_{\text{GS}}} \tag{5.12}$$

Although a cascode structure would increase the output impedance and the reverse isolation, it would not significantly improve the voltage gain which is limited by the input impedance of the second stage. Moreover, a cascode amplifier is often implemented with an additional inductor between the CS and CG transistors to increase f_T and reduce the NF [36, 37], resulting in a large chip area. A CS stage with inductive source degeneration is therefore used as the basis of the first stage LNA.

An inductor L_D is used as the load of the LNA, as shown in Figure 5.8. For the same DC current, an inductor has a smaller voltage drop than a resistor and can resonate out the parasitic capacitance on the output node [31].

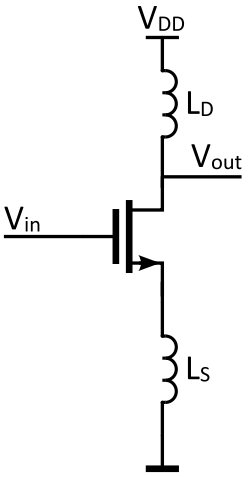


Figure 5.8: CS stage with source degeneration inductor L_S and load inductor L_D.

5.4. Minimum noise design

The LNA is designed to achieve low noise and high gain. First, the minimum noise factor, F_{min}, is optimized. Secondly, the input is matched to achieve the lowest noise factor, F_{LNA}, which is defined by

$$F_{\text{LNA}} = F_{\text{min}} + \frac{R_n}{G_S}\left[\left(G_S - G_{\text{opt}}\right)^2 - \left(B_S - B_{\text{opt}}\right)^2\right], \tag{5.13}$$

where F_{min} is the minimum achievable noise factor for the optimum noise match [38]. G_S and B_S are the real and imaginary part of the source admittance. G_{opt} and B_{opt} are the real and imaginary part of the optimum source admittance, for which $F_{\text{LNA}} = F_{\text{min}}$.

5.4.1. Minimum noise factor

The minimum noise factor, F_{min}, is optimized by finding the optimum drain current density, J_{drain}. From the plots in Figure 5.9, it can be found that the width per transistor finger and the transistor length should both be minimized to achieve the lowest noise. The optimum J_{drain} is found to be 164 µA/µm. This current density is obtained for a gate-source bias voltage of $V_{\text{GS}} = 750$ mV.

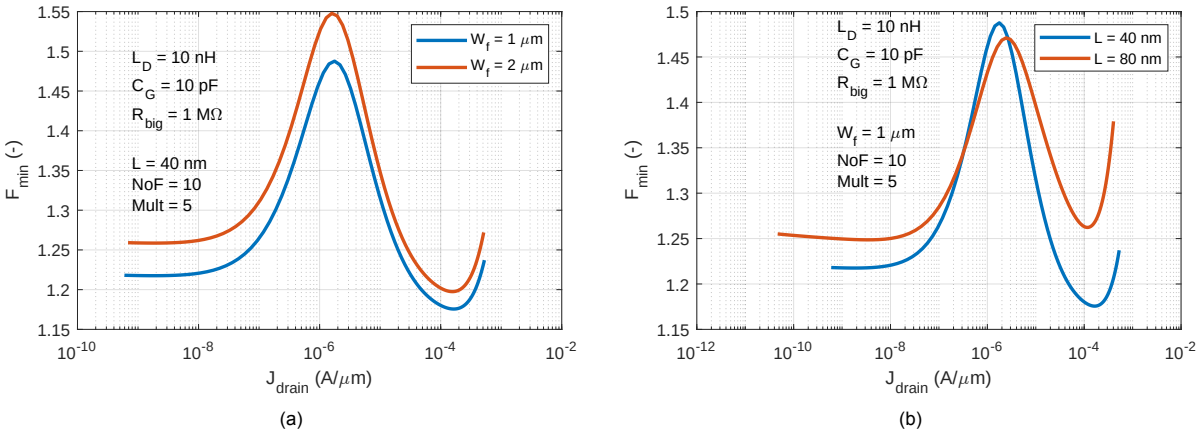


Figure 5.9: Minimum noise factor versus drain current density for (a) different transistor widths and (b) different transistor lengths.

The number of fingers and the transistor multiplier have no effect on the noise factor at the optimum J_{drain}, as shown in Figure 5.10.

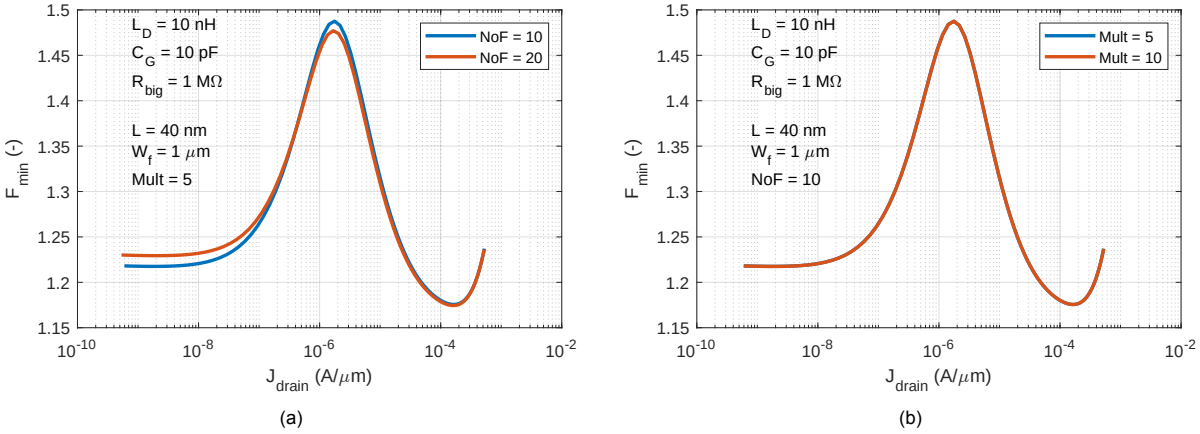


Figure 5.10: Minimum noise factor versus drain current density for (a) different number of fingers and (b) different transistor multipliers.

5.4.2. Input matching

After finding the drain current density for the lowest F_{min}, the total noise factor of the LNA can be minimized using the second part of eq. (5.13). This requires the noise impedance to be close to the source impedance, $Z_S \approx Z_{\text{opt}}$ [38], which can either be achieved by adjusting the optimum noise impedance or by changing the source impedance. Since the source impedance is determined by the $50\ \Omega$ antenna impedance, Z_{opt} has to be adjusted. Besides matching for the noise, the input impedance also needs to be matched to $50\ \Omega$, for maximum power transfer. The input matching is done in three steps, which are shown in Figure 5.11. First, the NMOS multiplier is increased to decrease R_{opt} to $50\ \Omega$. Secondly, the source degeneration inductor L_S is increased to increase R_{in} to $50\ \Omega$, according to eq. (5.12). As the last step, an inductor in series with the gate, L_G, is added to resonate out the imaginary parts, X_{opt} and X_{in}.

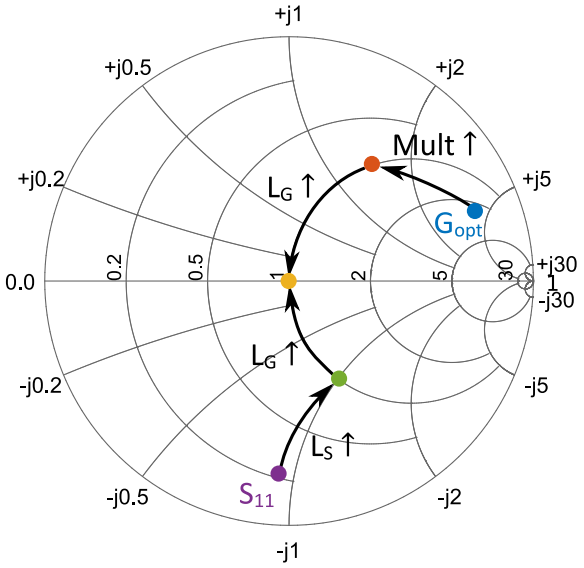


Figure 5.11: Procedure to achieve simultaneous noise and conjugate input matching.

Pad capacitance

A pad capacitance of roughly 50 fF is expected, which is connected between the input and ground. The effect of this capacitance on the gain and input impedance of the LNA can be understood from Figure 5.12.

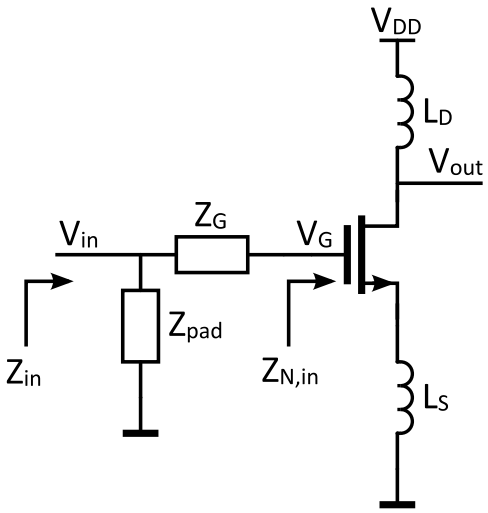


Figure 5.12: Circuit to analyze the effect of the pad capacitance on the input impedance and gain of the LNA.

The pad capacitance has an effect on the input impedance,

$$Z_{\text{in}} = Z_{\text{pad}} \| \left(Z_G + Z_{\text{N,in}} \right), \tag{5.14}$$

but not on the gain from V_{in} to V_G,

$$\frac{V_G}{V_{\text{in}}} = \frac{Z_{\text{N,in}}}{Z_G + Z_{\text{N,in}}}. \tag{5.15}$$

The pad capacitance changes the center frequency of the input impedance, while the center frequency of the voltage gain remains constant. This difference in center frequencies is shown in Figure 5.13.

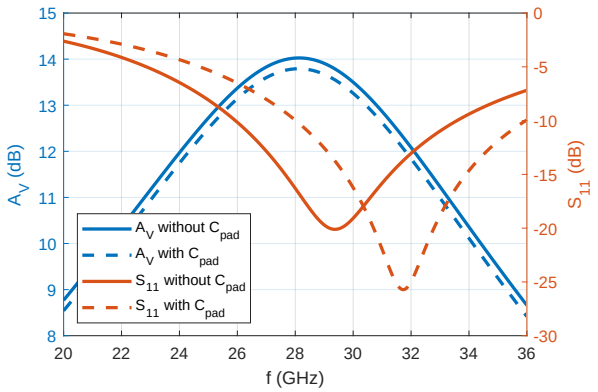


Figure 5.13: Simulated voltage gain (V_{out}/V_{in}) and input reflection coefficient of the LNA in Figure 5.12, with and without C_{pad} = 50 fF.

The effect of other circuit parameters on these center frequencies is investigated with the use of an equivalent model of the circuit. The input impedance of the NMOS transistor in Figure 5.12 can be written as [31]

$$Z_{N,in} = \frac{\left(Z_{load} + \frac{1}{C_{DS}s}\right)\left(L_S C_{GS} s^2 + g_m L_S s + 1\right)}{L_S C_{GS} s^2 + \left(Z_{load} C_{GS} + g_m L_S\right) s + g_m Z_{load} + \frac{C_{GS}}{C_{GD}} + 1}, \tag{5.16}$$

with

$$Z_{load} = \left\{\left[1 + g_m\left(r_O \| \frac{1}{C_{DS}s}\right)\right] L_S s + r_O \| \frac{1}{C_{DS}s}\right\} \| \, L_D s \, \| \, R_L. \tag{5.17}$$

The effect of different parameters on the center frequencies is calculated using these equations. From the results in Figure 5.14, it can be seen that only the pad capacitance can make the center frequencies equal. With a required C_{pad} of 50 fF, an inductor, L_{shunt}, is added in parallel with the pad capacitance, to reduce the center frequency of Γ_{in} [39, 40].

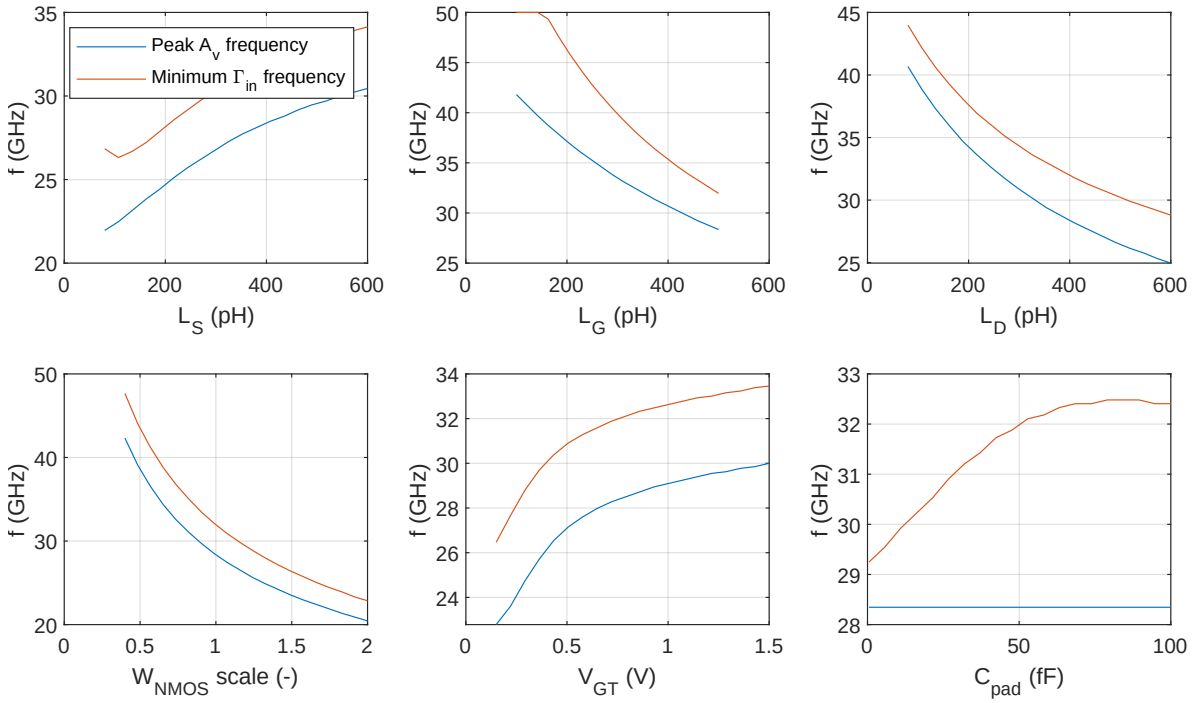


Figure 5.14: Calculated frequency of maximum voltage gain (V_G/V_{in}) and minimum input reflection coefficient of the circuit in Figure 5.12, for different swept parameters. Only C_{pad} can make the center frequencies equal.

5.4.3. Gm boosting

Adding L_{shunt} in parallel with C_{pad} adds a fourth inductor to the LNA. Realizing four separate inductors, while minimizing their mutual coupling requires a large chip area. L_{shunt} and L_S can be implemented as a transformer to reduce area and provide g_m boosting [40, 41]. The resulting LNA circuit is shown in Figure 5.15. An increase in input voltage causes the source voltage of the NMOS to decrease through the g_m boosting transformer. This increases V_{GS}, resulting in an increase in voltage gain.

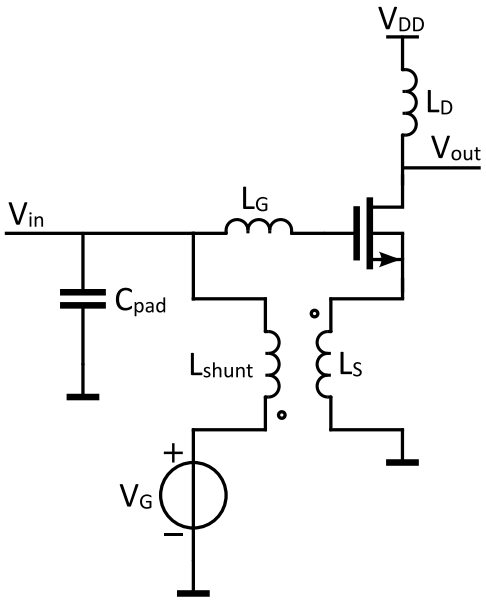


Figure 5.15: Schematic of the first stage LNA with pad capacitance and g_m boosting transformer.

The bulk of the NMOS is connected to the source terminal, to prevent an increase in threshold voltage through the body effect [28]. The bulk-source connection increases the g_m, resulting in a larger gain and lower noise, which are both important to reduce the two-stage NF.

5.4.4. Bondwires and decoupling capacitors

The V_{DD} and ground nodes are connected to the off-chip supply via bondwires, as shown in Figure 5.16. The on-chip supply voltage is kept constant with the use of a decoupling capacitor, C_{dec}. A decoupling capacitor with a low-quality factor is added to minimize the ringing of the supply voltage. This is modeled with $C_{\text{dec,lowQ}}$ and $R_{\text{dec,lowQ}}$ in the circuit of Figure 5.16. The component values are provided in Table 5.1. Three parallel bondwires of 1 nH to V_{DD} and 300 pH to V_{SS} are used to limit the gain reduction caused by these bondwires. The value of C_{dec} is chosen to provide an impedance of $1\ \Omega$ at 28 GHz. $C_{\text{dec,lowQ}}$ is increased until no overshoot is visible in the step response, which is at $C_{\text{dec,lowQ}} = 5C_{\text{dec}}$. The value of $R_{\text{dec,lowQ}}$ is selected to provide a critically damped step response.

Table 5.1: Component values of the bondwires and decoupling capacitors.

Component	$L_{\text{bondwire+}}$	$L_{\text{bondwire-}}$	C_{dec}	$C_{\text{dec,lowQ}}$	$R_{\text{dec,lowQ}}$
Value	333 pH, Q=60	100 pH, Q=60	5.7 pF	28.5 pF	12 Ω

5.4.5. ESD protection

The sensitive transistors on the chip must be protected from electrostatic discharge (ESD) through the input pin. Two different models are used to predict the voltage on the NMOS after an ESD event.

ESD models

These two models are the human-body model (HBM) and the machine model (MM). The HBM models a static discharge through a human contact, while the MM considers a metal contact such as a machine. The latter has a much smaller resistance than a human body and is therefore modeled differently. Both models use the same simulation setup, as shown in Figure 5.17, with different component values,

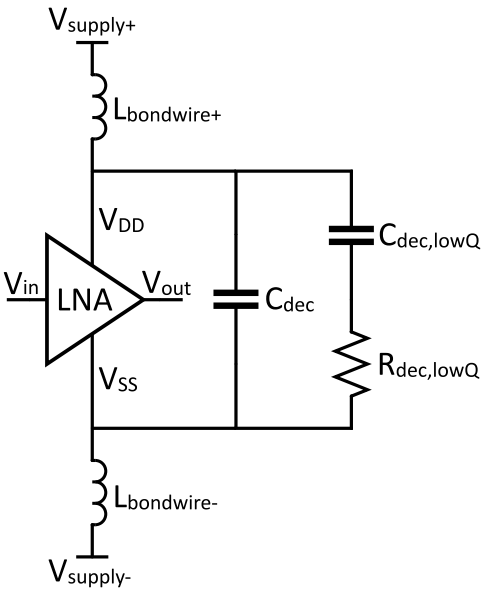


Figure 5.16: The bondwires of the supply connections are modeled with inductors. Decoupling capacitors are used to provide a stable supply voltage to the on-chip circuitry.

summarized in Table 5.2 [42]. The ESD capability of a chip is measured with different voltage levels for different standards, as defined by the electrical overstress (EOS)/ESD Association [43]. Commercial integrated circuits (ICs) typically require 2 kV for the HBM and 200 V for the MM [44]. Measuring an IC in a lab environment, however, reduces the requirements. For the circuit in this thesis, the maximum ESD voltages are found at which the voltage on the terminals of the NMOS ($|V_{GS}|$ and $|V_{GD}|$) remains below 2 V. The achieved ESD voltages for each model, and the corresponding class in the standard, are included in Table 5.2.

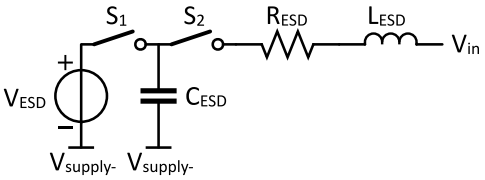


Figure 5.17: Circuit used for HBM and MM ESD testing. The ESD voltage is charged on C_{ESD}, after which S_1 is opened and S_2 is closed to discharge C_{ESD} through R_{ESD} and L_{ESD} into the circuit.

Table 5.2: Component values of the ESD model in Figure 5.17.

Model	C_{ESD}	R_{ESD}	L_{ESD}	V_{ESD}
HBM	100 pF	1.5 kΩ	750 nH	+2400/-1950 V (class 1C)
MM	200 pF	20 Ω	750 nH	+125/-100 V (class M2)

ESD diodes

The NMOS of the LNA must be protected for positive, as well as negative ESD voltages. Two diodes, one to V_{DD} and one to V_{SS}, are often used as ESD protection in mm-wave LNAs [45, 46]. Figure 5.18 shows the circuit of the LNA with the ESD protection diodes. Besides these diodes, L_{shunt} also aids in the protection, by providing a low-impedance path to ground for low-frequency signals.

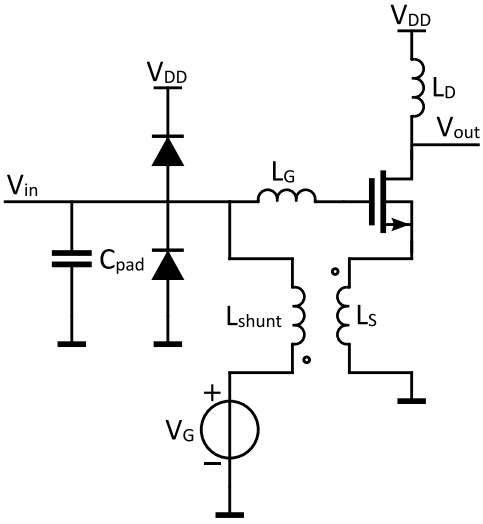


Figure 5.18: Schematic of the first stage LNA with ESD protection diodes.

A pn-junction diode with a unit size of 2x6 µm is used. The simulated total diode current versus input voltage is shown in Figure 5.19. Multiple diodes can be used in parallel to increase the discharge current and thereby decrease the input voltage and the voltage on the NMOS. The lower limit of the input voltage is determined by the threshold voltage of the diodes. For a positive input voltage, the diode connected to V_{DD} only starts conducting when the input voltage reaches $V_{\text{DD}} + V_{\text{TH}}$.

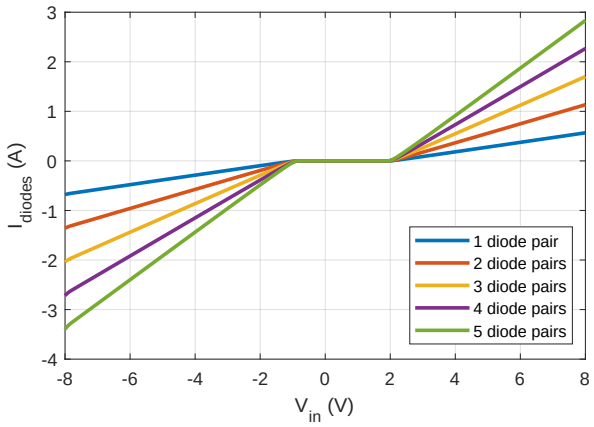


Figure 5.19: Total DC current through ESD diodes versus DC input voltage for a different number of parallel pairs of ESD diodes. Simulated with only the diodes, without the rest of the LNA.

Each pair of diodes adds a capacitance of 25 fF at 28 GHz, parallel to C_{pad}. Four parallel ESD diode pairs are used to limit the voltage on the nodes of the NMOS, while not adding too much capacitance at the input node.

Achieved ESD protection

The achieved ESD protection is simulated with the LNA with layout components, which will be designed in Chapter 6. The electromagnetic (EM) simulation models of the inductors and transformer are used to provide a more accurate result.

The maximum ESD voltage at which $|V_{\text{GS}}| < 2$ V and $|V_{\text{GD}}| < 2$ V is found for the two different ESD models. For the HBM, the maximum ESD voltage is +2400 V and -1950 V. The simulated transient voltages V_{GS} and V_{GD} are shown in Figure 5.20.

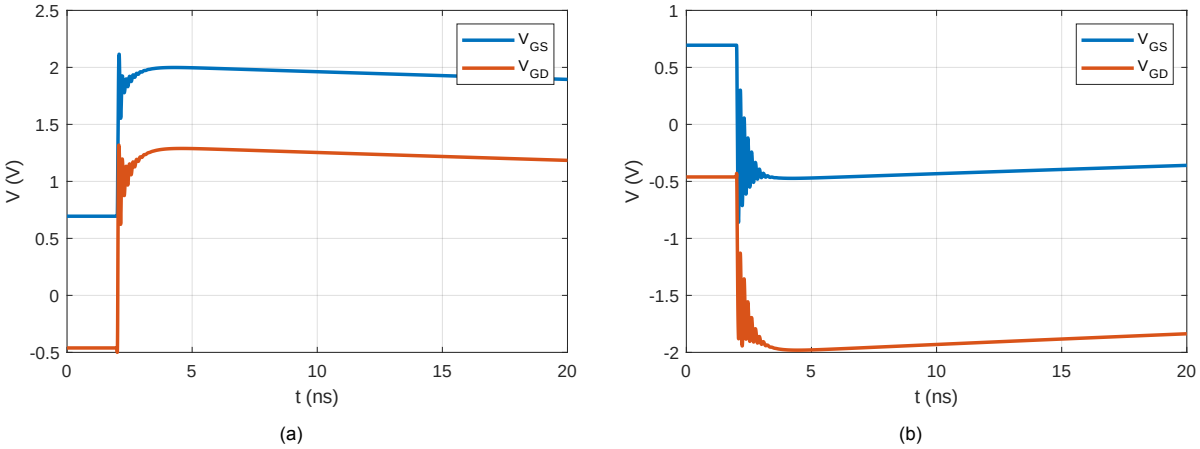


Figure 5.20: Transient voltages on the NMOS after applying a HBM ESD voltage of (a) +2400 V (b) -1950 V.

For the MM, the LNA can handle a maximum ESD voltage of +125 V and -100 V. The simulated transient voltages V_{GS} and V_{GD} are shown in Figure 5.21.

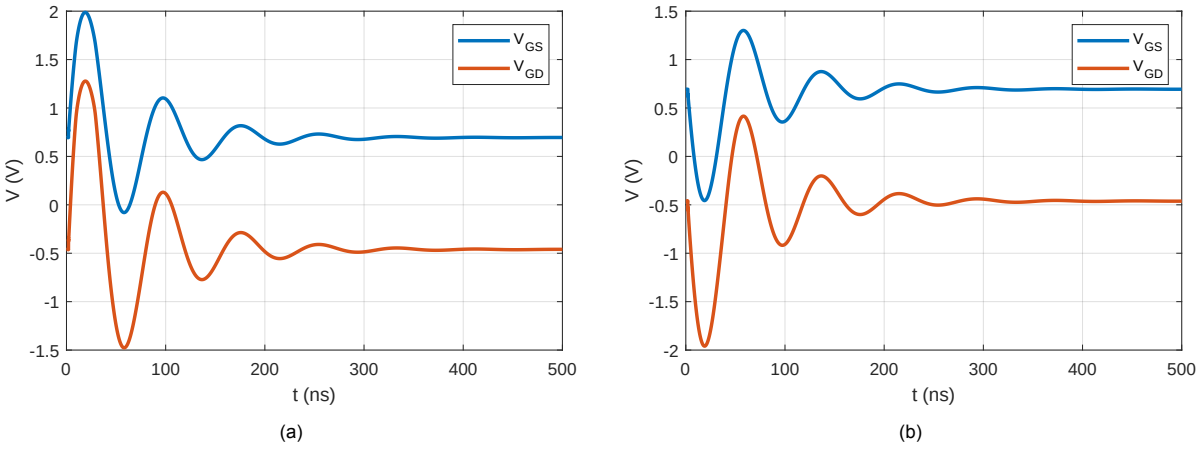


Figure 5.21: Transient voltages on the NMOS after applying a MM ESD voltage of (a) +125 V and (b) -100 V.

5.5. Simulation results

The LNA is simulated with ideal components[1], including the pad capacitance, ESD diodes, bondwires and decoupling capacitors. The input impedance of the second stage is modeled by a resistor of 119 Ω in parallel to a capacitor of 82 fF and used as the load impedance of the LNA.

The resulting voltage gain is 13.6 dB, with a ripple of 0.8 dB between 26 and 30 GHz, as shown in Figure 5.22a. The NF and NF_{min} of the LNA, as shown in Figure 5.22b, are 2.58 dB and 2.54 dB at 28 GHz respectively. Figure 5.23 shows the input reflection coefficient and the source impedance for minimum noise figure. The input is matched to 50 Ω with $S_{11} \leq$ -17.0 dB. The input impedance is also matched for optimum noise, with G_{opt} close to 50 Ω. The output impedance of the LNA is 23.4+j52.4 Ω at 28 GHz, which corresponds to a parallel RL circuit with R = 141 Ω and L = 357 pH. This inductor is used for the inter stage matching and resonates out with the parallel input capacitance of the second stage. The LNA consumes a DC power of 7.62 mW with the 1.2-V supply.

[1] Schematic components are used. Inductors have a quality factor of 12. Resistors and capacitors are ideal. Transistors are the schematic components from TSMC.

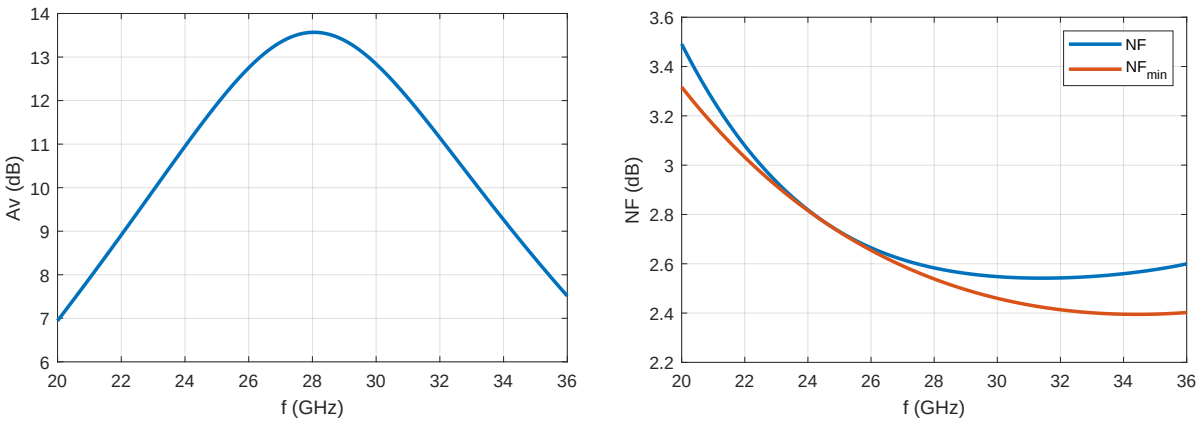


Figure 5.22: (a) Simulated voltage gain and (b) NF and NF_{min} of the LNA. Ideal components are used for these simulations.

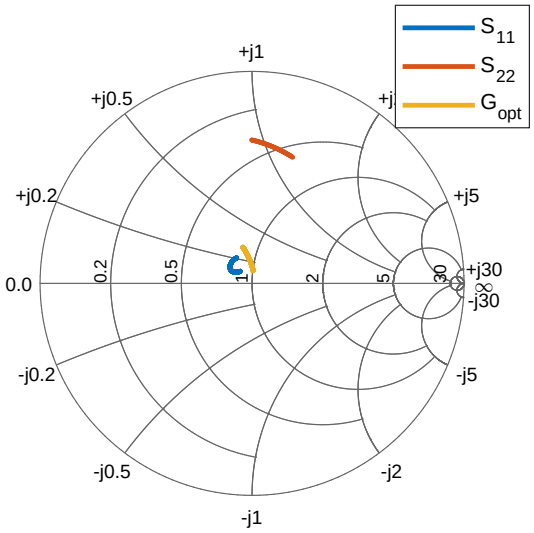


Figure 5.23: Simulated input and output reflection coefficient (S_{11} and S_{22}) and source impedance for minimum noise figure (G_{opt}) of the LNA. Ideal components are used for this simulation.

The IIP_3 is simulated by the method described in Section 4.5, and is shown in Figure 5.24a. Inside the 26-30 GHz BW, the IIP_3 ranges between 15.6 and 15.7 dBm. The simulated IP_{1dB} for different frequencies is shown in Figure 5.24b. This ranges between -2.1 and +3.7 dBm

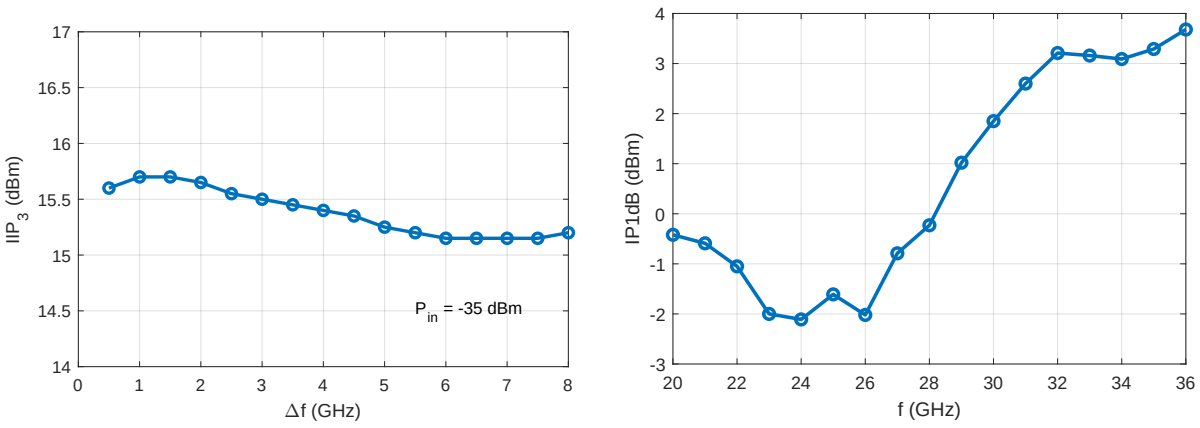


Figure 5.24: (a) Simulated IIP_3 of the first stage LNA for different frequency offsets compared to f_{LO}. Δf, is the offset from 28 GHz of the first tone in the two tone IIP_3 test, The IM3 frequency is 28.05 GHz. (b) Simulated 1 dB compression point for different frequencies.

5.5.1. Stability

The stability of the LNA is examined with the source and load stability factors μ and μ'. Figure 5.25 shows these stability factors, as well as the voltage gain. The stability factors are simulated with a 50 Ω port at the output instead of the expected input impedance of the second stage. For a voltage gain larger than 0 dB, $\mu \geq 1.33$ and $\mu \geq 1.19$. The LNA is therefore unconditionally stable.

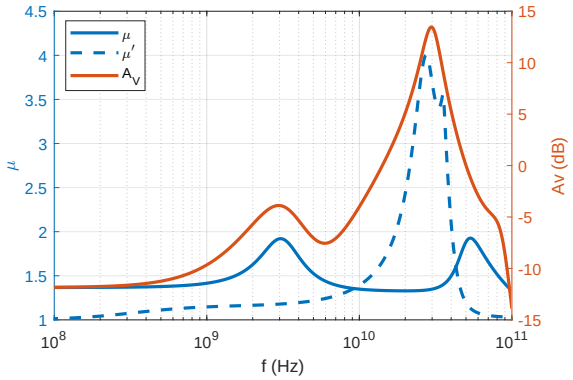


Figure 5.25: Simulated source and load stability factors μ and μ' of the LNA, as well as the voltage gain A_V. Ideal components are used for this simulation.

5.6. Conclusion

A CS LNA with g_m boosting has been designed as a first stage to reduce the noise of the NPF. The input matching network achieves a simultaneous noise and conjugate match, resulting in a voltage gain of 13.6 dB and a NF of 2.58 dB. The pad capacitance and ESD diodes are incorporated in the design of the matching network. Bondwires and decoupling capacitors are added, after which the circuit remains unconditionally stable.

6 Layout

The layout of all inductors and transformers, as well as the NMOS transistor of the LNA, is designed in this chapter. The simulation results of these layouts are used in the circuit simulation to provide more accurate results. The LNA has two inductors and one transformer for g_m boosting. The NPF uses two inductors for isolation and a transformer for the output subtraction. Metal 7 (M7) and M6 are used for the inductor and transformer designs. These provide the highest Q and lowest capacitance to the substrate. Section 6.1 starts with the theory on inductor layout design and discusses the designs of all inductors. The theory and design of the transformers is included in Section 6.2. The NMOS of the first stage LNA is designed in Section 6.3, after which Section 6.4 presents the full layout of all LNA inductors.

6.1. Inductor design

The layout of three different inductors has to be designed. The required and achieved inductance and quality factors of these inductors are summarized in Table 6.1. First, the theory on inductor design and general decisions are described in Section 6.1, after which the design of the three inductors is discussed in three separate sections.

Table 6.1: Overview of required and achieved specifications of the inductors used in the circuit, excluding the transformers.

Inductor	Location	Required L	Required Q	Achieved L	Achieved Q	Achieved SRF
L_{iso}	NPF isolation	$\geq$ 500 pH	$\geq$ 12	654 pH	12.2	61.4 GHz
L_G	LNA gate	450 pH	$\geq$ 12	450 pH	13.8	80.2 GHz
L_D	LNA load	262 pH	6	262 pH	15.5[i]	113 GHz

[i] Without $R_{parallel}$

6.1.1. Theory

An on-chip spiral inductor can be modeled as in Figure 6.1 [47].
The inductor in this model has a parallel capacitance. For low frequencies, the capacitor is an open circuit and the resulting impedance is determined only by the inductor. The inductor and capacitor resonate at the self-resonance frequency (SRF), after which the impedance turns from inductive to capacitive. In order to minimize the effect of the parallel capacitor, the SRF is designed to be at least two times the maximum used frequency. For an operating BW of 26-30 GHz, the SRF must be at least 60 GHz. At mm-wave, the SRF and Q are decreased by the capacitance to the substrate [48]. This capacitance is therefore minimized by using small metal trace widths, at the cost of a lower current capability.

A ground shield below the inductor adds a small resistance Z_{shield} to the equivalent circuit, connecting C_{ox1} to C_{ox2} without C_{Si_a} and C_{Si_b}. This increases the total capacitance between port 1 and 2 and thereby decreases the SRF [49]. A ground shield is therefore not used.

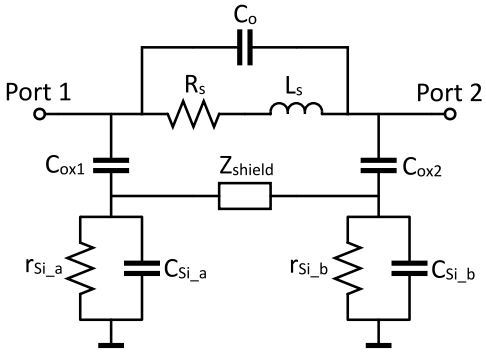


Figure 6.1: Lumped component model of a spiral inductor, with ground shield impedance Z_{shield} [47].

The maximum current of a 2 µm wide trace on metal 7 (M7), M6 and the via between M6 and M7 (VIA6) is calculated using the documentation from TSMC. The AC current is calculated for the recommended maximum temperature increase of 5 °C. The maximum AC and DC currents are shown in Table 6.2.

Table 6.2: Maximum current of a 2 µm wide trace, according to the TSMC documentation.

Layer	Maximum AC current	Maximum DC current
M6 (2 µm)	12.8 mA (RMS)	32.1 mA
M7 (2 µm)	24.6 mA (RMS)	61.5 mA
VIA6 (per via)	Not defined	6.15 mA

6.1.2. NPF isolation inductor L_{iso}

The isolation inductor reduces the charge leakage between the two frequency-shifted filters. The maximum achievable inductance with an SRF of 60 GHz is estimated to be 500 pH, but a larger inductance would give better isolation and therefore a larger gain. The isolation inductor is designed to achieve a maximum inductance for an SRF of 60 GHz.

Parallel traces

The skin effect decreases Q of the inductor at GHz frequencies [50]. Multiple conductors can be used in parallel to increase the quality factor. An inductor with one conductor of 6 µm wide is compared with the same inductor with three parallel conductors of 2 µm each, separated by a gap of 1 µm. These inductors are shown in Figure 6.2.

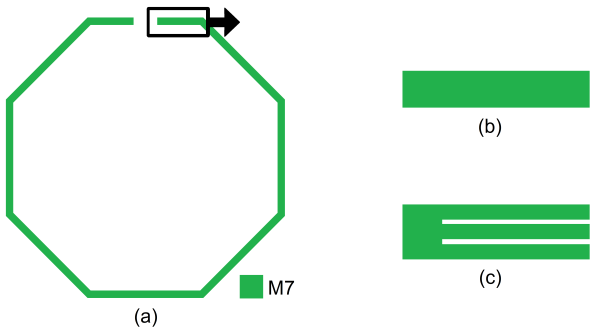


Figure 6.2: (a) Single turn octagonal inductor with (b) one conductor of 6 µm and (c) three parallel conductors of 2 µm each.

Designing these two inductors for the same SRF (56 GHz) results in a Q of 9.6 for the three parallel conductors, compared to 9.1 for the single conductor. The inductance is however decreased from 620 pH to 590 pH. The reduction in inductance decreases the isolation and the gain. The use of multiple parallel conductors is therefore not used in the inductor design.

Conductor width

A small width reduces the parasitic capacitance of the inductor, which increases the SRF. Three different widths of 2, 4 and 6 µm are compared. The outer diameter of the inductor is scaled to keep a constant SRF of 60 GHz. The results are summarized in Table 6.3.

Table 6.3: Comparison of different conductor widths of L_{iso} with one turn.

Width	Outer diameter	L	Q	SRF
2 µm	189 µm	651 pH	9.7	60 GHz
4 µm	191 µm	596 pH	10.1	60 GHz
6 µm	175 µm	550 pH	10.4	60 GHz

A small width results in a larger inductance for the same SRF, which results in a better isolation. For the other inductors, which need to be designed for a fixed inductance, the small width is beneficial for increasing the SRF and thereby improving the flatness of the inductance over the operating BW. The expected AC current through L_{iso} is estimated with the maximum input power of -25 dBm ($P_{\text{sig}} = 3.2$ µW). This corresponds to a root mean square (RMS) voltage of

$$V_{\text{RMS}} = \frac{1}{2\sqrt{2}}\sqrt{P_{\text{sig}} \cdot 8 \cdot 50\ \Omega} = 13\ \text{mV}. \tag{6.1}$$

The voltage gain of the first stage is 13.6 dB, resulting in an output voltage of 62 mV RMS. With an input impedance of the second stage of 191 Ω, the current is 326 µA. In the worst case, when only one NPF conducts current, this full current flows through one isolation inductor. The maximum expected current of 326 µA RMS is significantly less than the maximum allowable AC current on both M6 and M7, as shown in Table 6.2.

Two turns

Decreasing the trace width for a constant SRF also decreased Q. Using multiple turns can increase the quality factor, while reducing the area. The self inductance between the two loops increases L, while the trace resistance stays constant. This increases both Q and the SRF. The layout of the two turn L_{iso} is shown in Figure 6.3. A ground plane on M7 is added around the inductor to provide isolation to the other components in the layout.

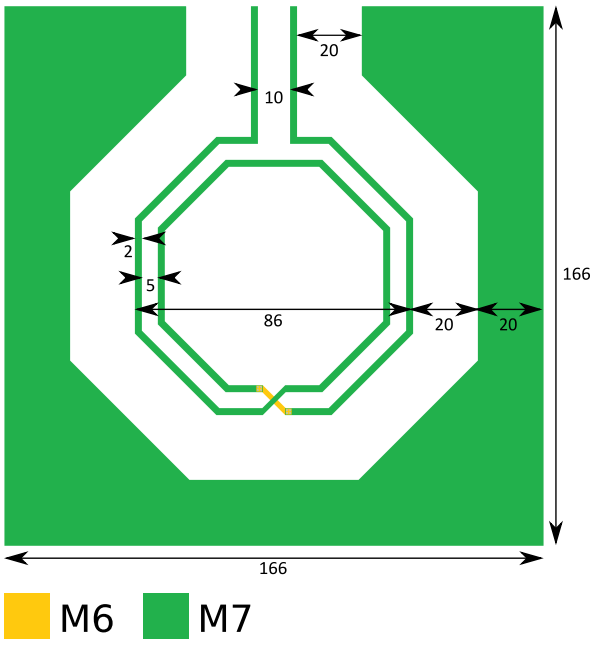


Figure 6.3: Layout of L_{iso} with two turns and a ground plane. The dimensions are in µm.

The isolation inductor achieves an inductance of 654 pH, with a Q of 12.2 and an SRF of 61.4 GHz. The quality factor and SRF meet the required values. The inductance is significantly higher than the required 500 pH, causing an improvement in the isolation and therefore a larger gain. The voltage gain of the NPF is increased by 1.5 dB.

6.1.3. LNA gate inductor L_G

The inductor in series with the gate of the LNA NMOS is required to be 450 pH with Q $\geq$ 12 and SRF $\geq$ 60 GHz. This inductor is designed for the maximum SRF, while fulfilling the L and Q requirements. This reduces the variance of L_G over the BW[1]. The resulting layout is shown in Figure 6.4. 1.75 turns

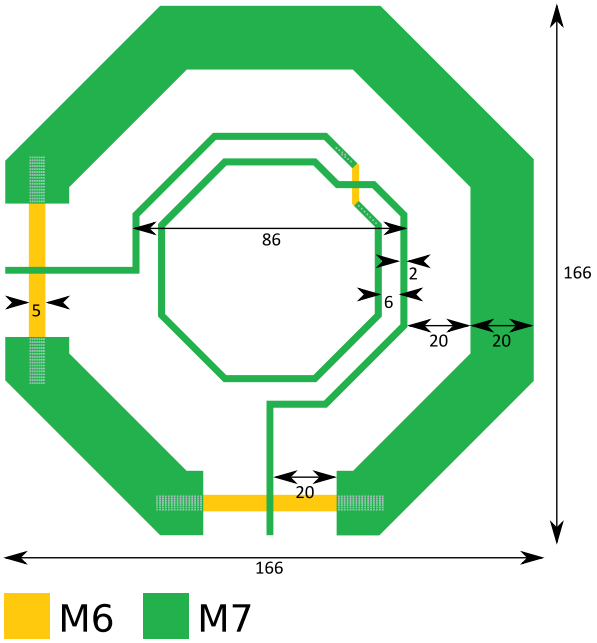


Figure 6.4: Layout of L_G with 1.75 turns and a ground plane. The dimensions are in µm.

are used to connect the inductor in the full layout of the LNA. This layout results in an inductance of 450 pH, with Q = 13.8 and an SRF of 80.2 GHz. Within the 26-30 GHz BW, the inductance varies from 443 to 458 pH. Q varies from 13.6 to 14.0.

6.1.4. LNA load inductor L_D

The load inductor has a value of 262 pH. This relatively low inductance makes it possible to achieve a large Q of 15.5 and a high SRF of 113 GHz. The resulting layout is shown in Figure 6.4. Compared to L_G, the spacing between the turns is increased to 7 µm. This increases the SRF at the cost of a smaller inductance, due to reduced self inductance. The large SRF limits the variance of the inductance between 26 and 30 GHz to 4 pF. By resonating out the capacitance at the drain, L_D determines the center frequency of the gain. The small variance results in a stable center frequency and thereby a lower ripple in the gain. The large SRF limits the variance of the inductance between 26 and 30 GHz to 4 pF. By resonating out the capacitance at the drain, L_D determines the center frequency of the gain. The small variance results in a stable center frequency and thereby a lower ripple in the gain. The BW of the LNA is increased by adding a resistor of 500 Ω in parallel with L_D. This reduces Q to 6 and reduces the ripple in the 26-30 GHz band to 1.0 dB.

Besides resonating out the capacitance at the drain, L_D also provides the DC current for the LNA. The expected DC current is 6.33 mA, which is a safe distance away from the maximum current of 32.1 mA and 61.5 mA on M6 and M7 respectively, for a conductor with of 2 µm. 10 vias are used per contact between M6 and M7. This makes their maximum DC current equal to that of the traces on M7.

[1]The effective inductance, calculated by Im$Z/j\omega$, changes over the BW due to the parallel capacitor as shown in Figure 6.1.

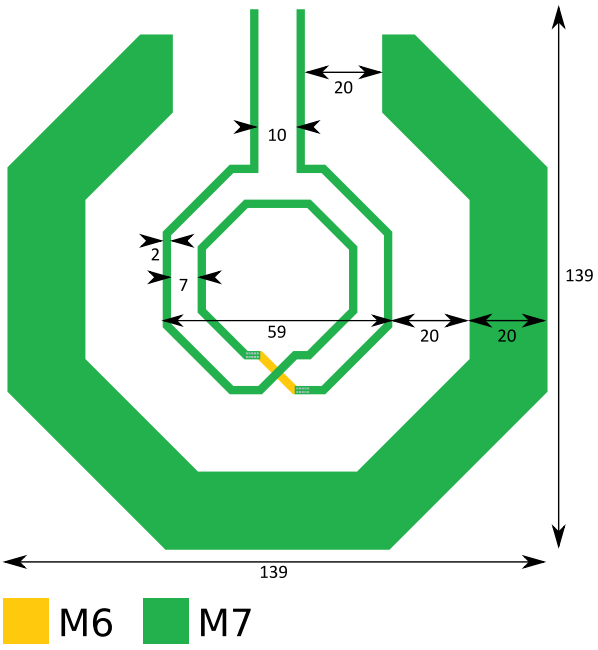


Figure 6.5: Layout of L_D including ground plane. The dimensions are in µm.

6.2. Transformer design

Two transformers are designed. Table 6.4 shows an overview of their required parameters. It is assumed that the primary inductance (L_p) cannot have the same value as the secondary inductance (L_s) and that these two values are limited to 500 pH.

Table 6.4: Overiew of transformers used in the circuit, with their required parameters.

Transformer	L_p	L_s	SRF	k	Q
NPF output subtraction	500 pH	450 pH	≥ 60 GHz	≥ 0.6	12
LNA g_m boosting	250 pH	230 pH	≥ 60 GHz	0.4	12

6.2.1. NPF output transformer

The output transformer is used to subtract the output signals of both NPFs. As shown by the model in Figure 6.6, capacitors are used to match the circuit. These capacitors can partially be implemented inside the transformer, which reduces the SRF.

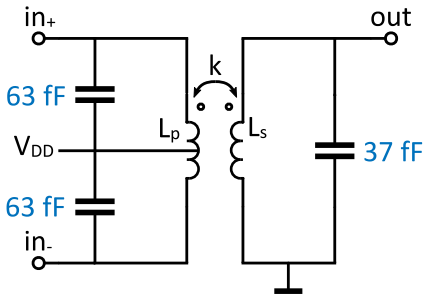


Figure 6.6: Model of output inductor with required capacitances for matching.

A transformer can be implemented by two stacked inductors on two different metal layers or by two inductors on the same layer (planar transformer). Stacking the inductors gives a better coupling factor, because of the reduced distance between the windings [51]. Implementing a large inductance with a high SRF requires a small capacitance to the substrate and thus a small trace width, causing a reduced Q due to the increased resistivity of any layers other than M7. The planar transformer is

not affected by the low resistivity, since both inductors are implemented on M7. The transformers are therefore implemented according to the planar topology. From the inductor design it is found that a width of 2 µm minimizes the capacitance to the substrate, while keeping a relatively large Q. The spacing between the two inductors is designed to be 5 µm, thereby providing a larger coupling factor, k, while not reducing the SRF more than needed. The layout of the output transformer is shown in Figure 6.7.

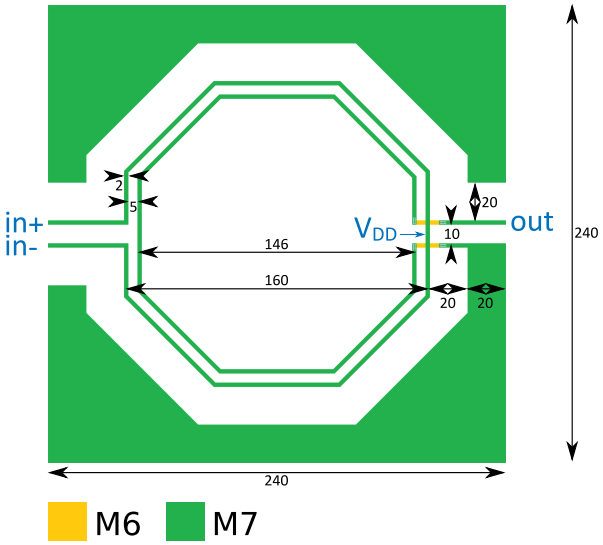


Figure 6.7: Layout of the output transformer including ground plane. The dimensions are in µm.

The resulting inductances are L_p = 478 pH and L_s = 575 pH. The grounded side of the secondary inductor increases its inductance, since it removes the parasitic capacitance to ground on one side. The increased The quality factors are Q_p = 15.1 and Q_s = 10.1. The coupling factor is k = 0.63 and the SRF is 49 GHz. Even for this relatively low SRF, the resulting gain of the NPF only varies 0.5 dB between 26 and 30 GHz.

6.2.2. LNA g_m boosting transformer

This transformer is used to provide g_m boosting at the first stage LNA. L_{shunt} and L_S are designed to be coupled with k = 0.4. These inductances are relatively small, allowing for a compact design. The SRF of a small inductor is larger, allowing for more inter-winding capacitance and therefore more loops. The resulting layout can be seen in Figure 6.8. The spacing between the turns is reduced to 2 µm to achieve a large coupling factor. Tuning is done by increasing the width of the connection wires of L_{shunt} and by reducing diameter of the inner turn of this inductor. Both reduces the inductance of L_{shunt} to the desired value.

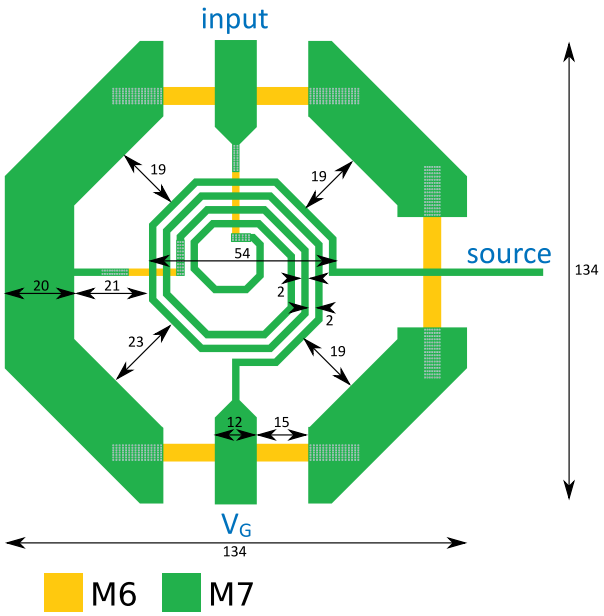


Figure 6.8: Layout of the g_m boosting transformer including ground plane. The dimensions are in µm.

The resulting inductances are L_{shunt} = 256 pH and L_s = 228 pH. Both quality factors are as required, Q_{shunt} = 13.0 and Q_s = 13.1. The SRF is 73 and 102 GHz for L_{shunt} and L_s respectively and the coupling factor is k = 0.42. All inductors and transformers of the first stage LNA are combined in Section 6.4.

6.3. NMOS design

This section presents the design of the NMOS of the first stage LNA. The required width of 54 µm is split over two unit cells with 27 fingers of 1 µm width.

6.3.1. Unit cell

The unit cell is designed first, with the focus on a low gate resistance, r_g, and small parasitic capacitances. The gate resistance limits the f_{max} of the NMOS and can be reduced by connecting the gates from two sides. This reduces r_g with a factor 4 compared to connecting the gates from only one side [52]. The gate-drain capacitance C_{GD} has more effect on the f_{max} and stability of the LNA than the gate-source capacitance C_{GS} [52]. Both capacitances are designed to be small, but when needed, C_{GD} is prioritized. The gate and drain connection wires exit the transistor on opposite side to minimize this capacitance. The resulting unit cell layout is shown in Figure 6.9 and Figure 6.10. Thick connections are used to minimize their resistance. The bulk of the NMOS is connected to source, as discussed in Chapter 5.

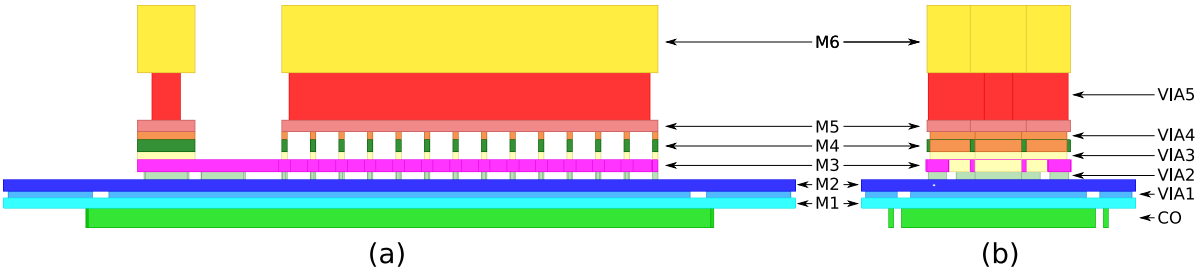


Figure 6.9: Layout of the NMOS unit cell seen from (a) the side and (b) the front.

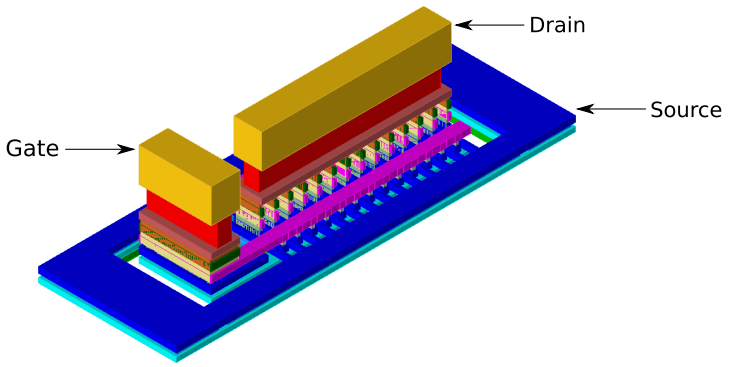


Figure 6.10: Layout of the NMOS unit cell in 3D view.

6.3.2. Full NMOS

The two unit cells are combined and connected on M6 (gate and drain) and M1-M2 (source), as shown in Figure 6.11 and Figure 6.12. Because of the higher sheet resistance of the lower metal layers, the sources are connected by a wide trace. A slot has been added to comply with the design rules. All three terminals connect to an inductor on the top metal and are therefore routed out of the NMOS on M7.

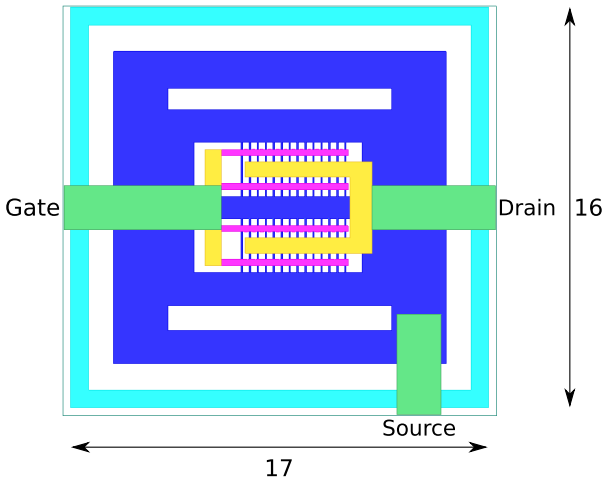


Figure 6.11: Top view of the full NMOS layout.

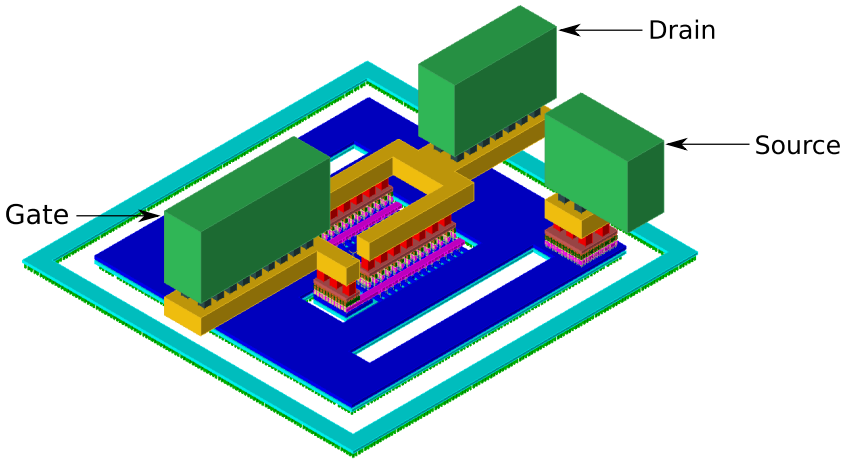


Figure 6.12: 3D view of the full NMOS layout.

The cross section of the NMOS transistor is shown in Figure 6.13. Three P+ and one NT_N guard rings are used to improve the isolation to other parts of the circuit. The NT_N layer is not shown in Figure 6.11 and Figure 6.12, but extends by 20 µm on each side.

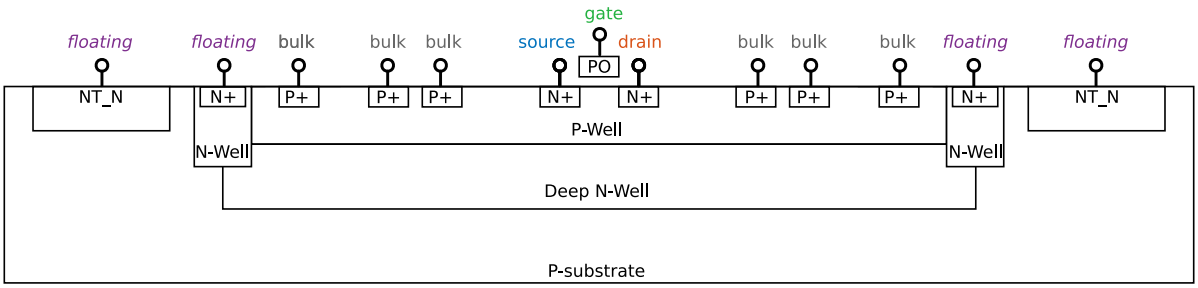


Figure 6.13: Cross section view of the NMOS. The dimensions are not on scale.

6.4. Layout of all inductors in LNA

All inductors of the LNA are combined in one layout as shown in Figure 6.14. This full layout, except the NMOS transistor, is simulated to create one EM model for the LNA inductors. The other inductors (L_{iso}) and the output transformer are simulated in individual EM models. All EM models are included as component in the schematic simulation to obtain the final results as presented in Chapter 7.

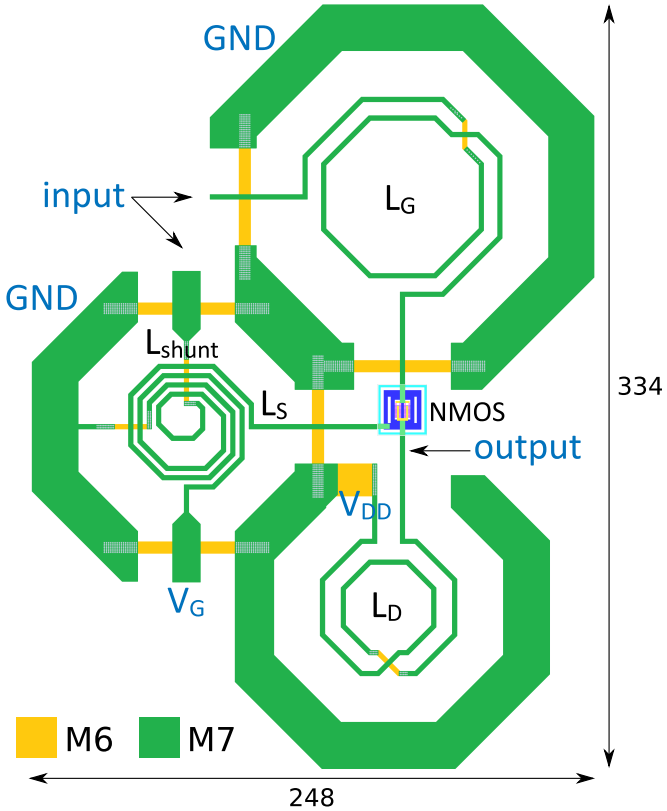


Figure 6.14: Layout of all inductors and NMOS of first stage LNA. Dimensions are in µm.

6.5. Simulation results

The LNA is simulated with the EM model of the inductor and transformer layouts and Calibre simulation of the NMOS transistor. These results are compared to the LNA with ideal components in Figure 6.15 and Figure 6.16. The voltage gain is increased by 2 dB to 15.6 dB, which is partially caused by a larger coupling factor of the g_m boosting transformer. The NF is kept constant at 2.58 dB. Figure 6.16 shows

that the input impedance and G_{opt}, which are slightly unmatched. The input reflection coefficient is increased from $S_{11} \leq$ -17 dB to $S_{11} \leq$ -10 dB. This can be improved with a larger source degeneration inductor, at the cost of a decreased gain and an increased NF.

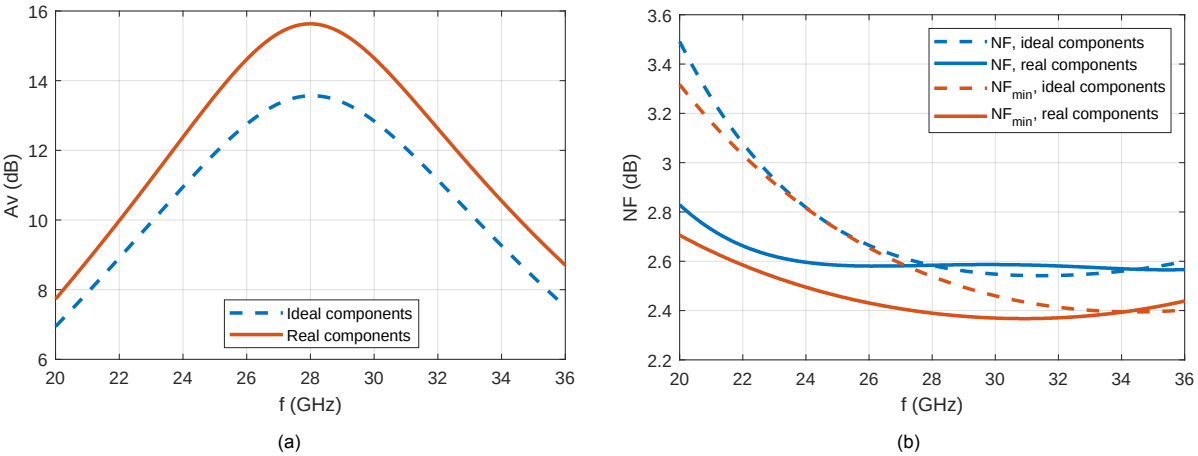


Figure 6.15: (a) Simulated voltage gain and (b) NF and NF_{min} of the LNA, with EM model of the inductors and Calibre simulation of the NMOS transistor.

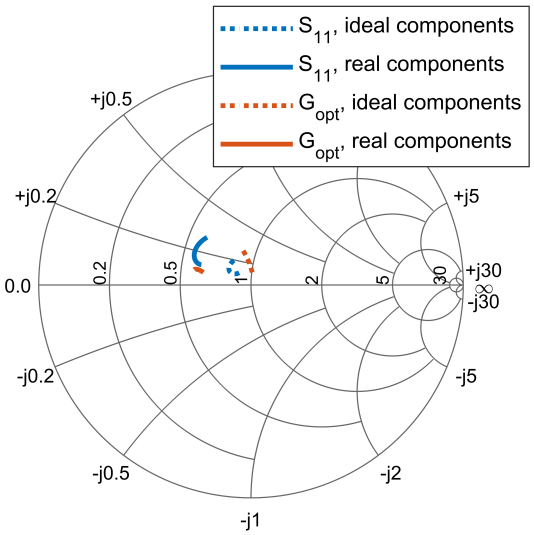


Figure 6.16: Simulated input reflection coefficient (S_{11}) and source impedance for minimum noise figure (G_{opt}) of the LNA, with EM model of the inductors and Calibre simulation of the NMOS transistor.

The IIP_3 is simulated by the method described in Section 4.5. Figure 6.17a shows the simulated IIP_3, which is 19.7 dBm IB and decreases to 14.3 dBm at a frequency offset of 8 GHz. The simulated IP_{1dB} of the LNA with ideal components varies between -0.6 and +3.6 dBm within the 26-30 GHz band.

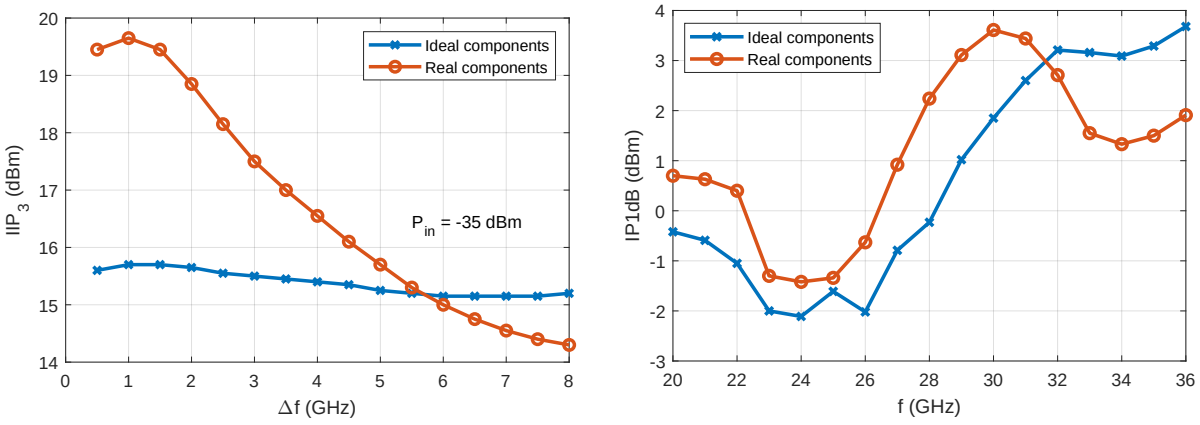


Figure 6.17: (a) Simulated IIP_3 of the first stage LNA with real components, for different frequency offsets compared to f_{LO}. Δf, is the offset from 28 GHz of the first tone in the two tone IIP_3 test, The IM3 frequency is 28.05 GHz. (b) Simulated 1 dB compression point for different frequencies.

7 Results

This chapter presents the simulation results of the mm-wave filter, including first stage LNA. The complete circuit is shown in Section 7.1, after which the simulation results are included in Section 7.2. The obtained performance is compared with the state-of-the-art in Section 7.3.

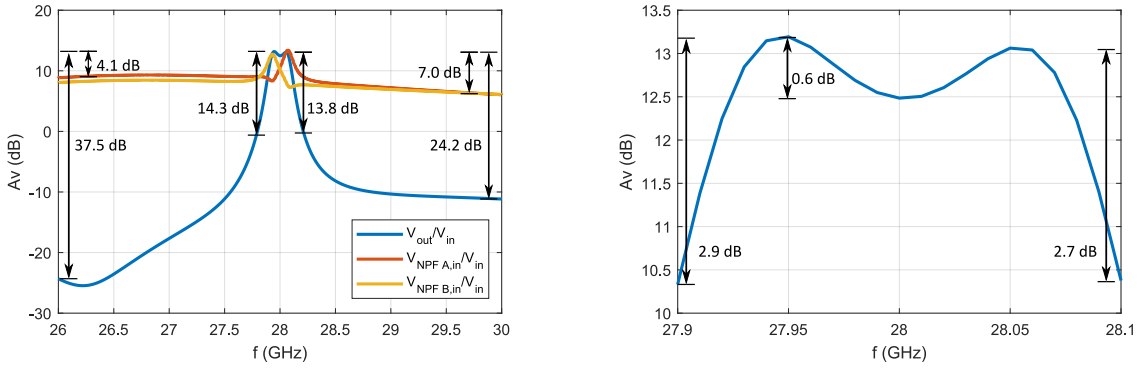
7.1. Full circuit

The full circuit of the filter is shown in Figure 7.1. The results are obtained from schematic simulation in Cadence (pss+pac for voltage gain, pss+psp for reflection coefficient, pss+pnoise for noise figure). The inductors and transformers are included in the circuit by using their EM simulated S-parameters. The NMOS of the first stage is included as a Calibre simulation result, extracted from Cadence layout simulation. The other components in the schematic are real components from the TSMC library[1].

7.2. Simulation results

7.2.1. Gain and noise

The achieved gain and attenuation of the filter are shown in Figure 7.2. An IB gain of 13.2 dB is obtained with an IB ripple of 0.6 dB. The attenuation at the center of the first adjacent channel is 14.3 and 13.8 dB for the left and right channel, respectively. Allowing a larger IB ripple would increase this attenuation, because it allows a smaller BW of the individual filters. A far-OOB, attenuation of 37.5 and 24.2 dB is achieved for the left and right side, respectively.



(a) (b)

Figure 7.2: Simulated voltage gain of the two-stage circuit with real components. (a) Voltage gain of the full circuit (V_{out}/V_{in}), with annotated attenuation at the center of the first adjacent channel and far OOB, and gain from the input of the first stage to the input of each NPF ($V_{NPF,in}/V_{in}$). (b) IB voltage gain of the full circuit (V_{out}/V_{in}).

[1] `nmos_rf` for the switches and LNAs of the NPF, `pmos_rf` for the g_m cell CM transistors, `nmos_rf_lvt` and `pmos_rf_lvt` for the g_m cell inverter transistors, `rppolywo` for the resistors, and `crtmom_wo_rf` for the capacitors.

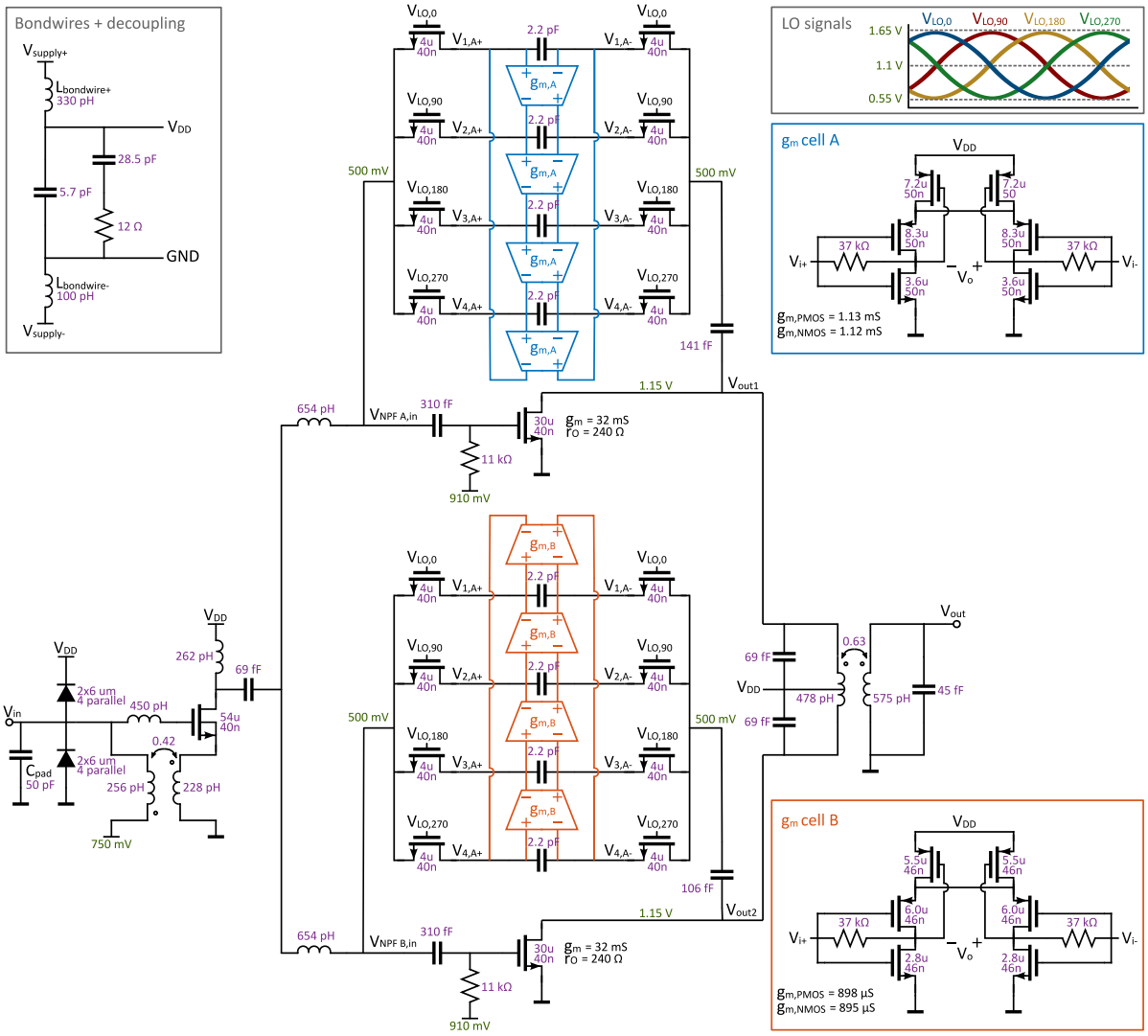


Figure 7.1: Schematic of the full circuit consisting of the LNA and the two frequency-shifted GB-NPFs. The component sizes are annotated in purple. The bias voltages are shown in green.

Besides attenuation in the gain, the NPF also provides attenuation in its input impedance. This is shown by the voltage gain from the input of the first stage to the input of each NPF ($V_{\text{NPF,in}}/V_{\text{in}}$) in Figure 7.2a. An attenuation of 4.1 dB and 7.0 dB is achieved for lower and higher far-OOB frequencies, respectively.

The wide-band filter is achieved by subtracting the output voltages of the two individual filters. The gain and phase of these two filters are shown in Figure 7.3. It can be seen that both the gain and phase match closely for low frequencies. This causes the large attenuation in Figure 7.2a. The increased difference in magnitude of both gains at frequencies larger than f_{LO} results in a smaller attenuation. Since the IB phase difference of the two filters is limited to 29°, instead of the ideal 180°, the subtraction of the paths results in a reduced gain. The 20 dB gain of the individual paths is reduced to 13 dB after subtraction. The attenuation, however, is improved from 5 dB for the individual paths to more than 24 dB for the full filter.

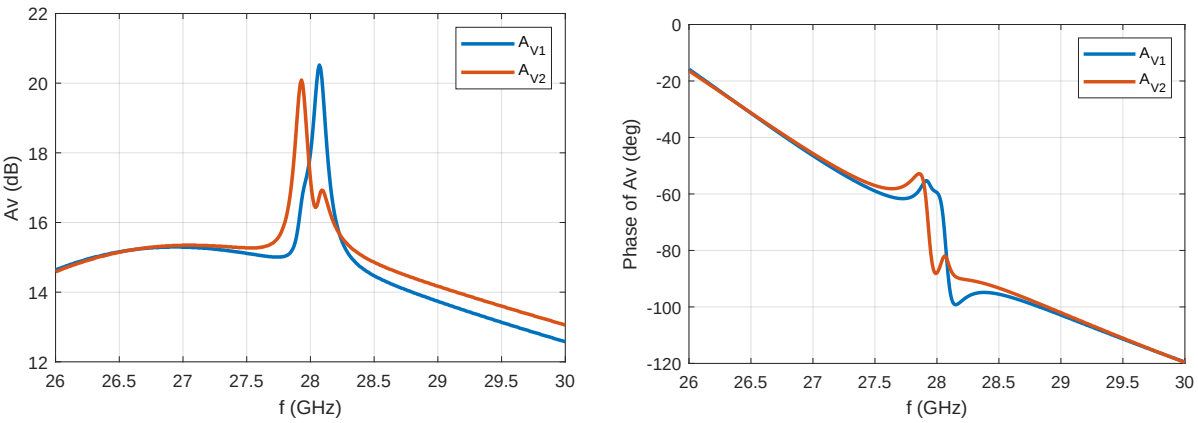


Figure 7.3: Simulated (a) voltage gain and (b) phase of both filter paths of the two-stage circuit with real components. These two gains are subtracted by the output transformer to obtain the total voltage gain.

The achieved roll-off of the voltage gain is shown in Figure 7.4a. Compared to the ideal higher-order NPF, this is decreased from 40 dB per decade to 34 dB per decade. This reduction can be explained by the fact that no zeros close to the main band are visible in the gain in Figure 7.2a. The zeros appear at the frequency where the gain and phase of both paths are equal. As shown in Figure 7.3, only one zero occurs around 26.5 GHz, where the gain and phase of both paths cross. Close to the main band, the difference in phase limits the attenuation. Reducing the phase of the second filter can result in an equal phase of both paths close to the main band. At the same time, this unfortunately increases the phase difference and thereby reduces the attenuation at far-OOB frequencies. A trade-off between the attenuation close to the main band and far OOB is found, which can be optimized by tuning the gain and phase of the individual filters, depending on the application.

Figure 7.4b shows the noise figure of the two-stage circuit. This is reduced from 20 dB for only the second stage to 10.2 dB for the filter, including the first stage LNA. The flicker noise of the baseband filter increases the noise around 28 GHz, but is ignored by the simulator at the exact LO frequency. The increment around f_{LO} is not visible when the noise contribution of the g_m cells is disabled.

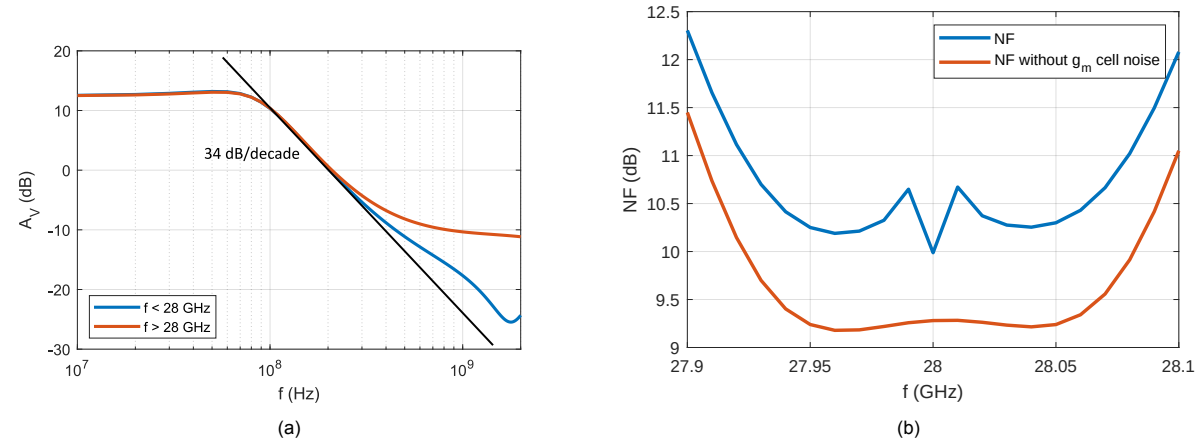


Figure 7.4: Simulated (a) roll-off and (b) noise figure of the two-stage circuit with real components.

7.2.2. Results over the full BW

The center frequency of the filter is swept from 26.02 to 29.98 GHz in steps of 220 MHz (by changing f_{LO}) to see the performance over the full BW. The input reflection coefficient is shown in Figure 7.5a. It can be seen that the input impedance is small (25-35 Ω), resulting in an $S_{11} < -9.0$ for the full BW of 26 to 30 GHz. A larger input impedance could have been achieved by increasing the source degeneration inductor of the first stage LNA. This, however, decreases the gain and increases the NF.

Figure 7.5b shows the IB NF for the different LO frequencies between 26 and 30 GHz. The minimum NF in each channel varies between 9.8 and 11.0 dB.

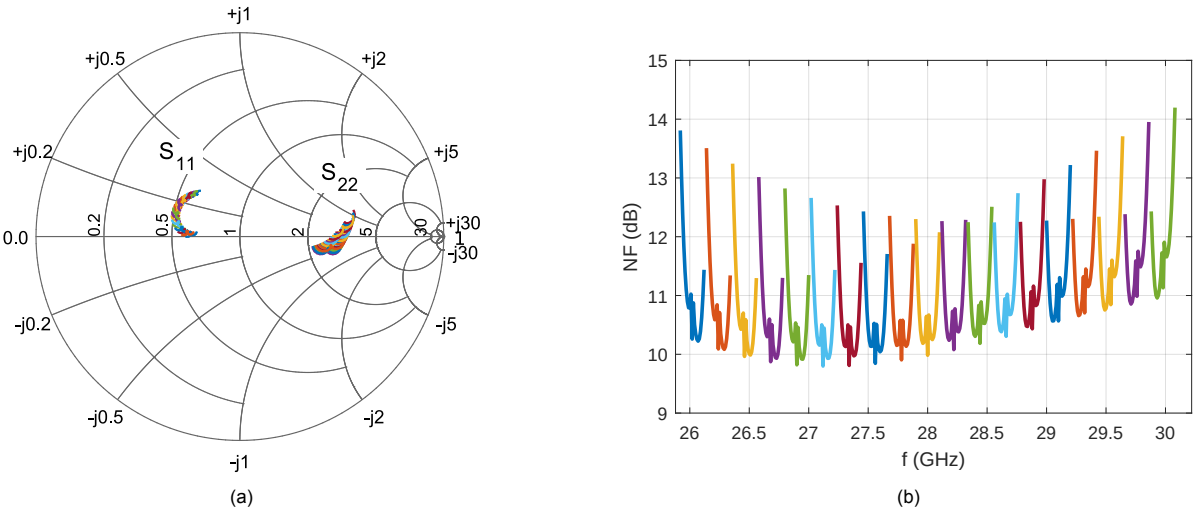


Figure 7.5: Simulated (a) IB input and output reflection coefficients and (b) IB NF for different values of f_{LO} between 26 and 30 GHz of the two-stage circuit with real components.

The voltage gain of the filter for different center frequencies is shown in Figure 7.6. The maximum center gain (gain at f_{LO}) is found to be 13.09 dB at f_{LO} = 27.12 GHz. The minimum gain is 9.32 dB at f_{LO} = 29.98 GHz. A difference of 3.8 dB in IB gain is thus obtained over the full 4 GHz f_{LO} variation.

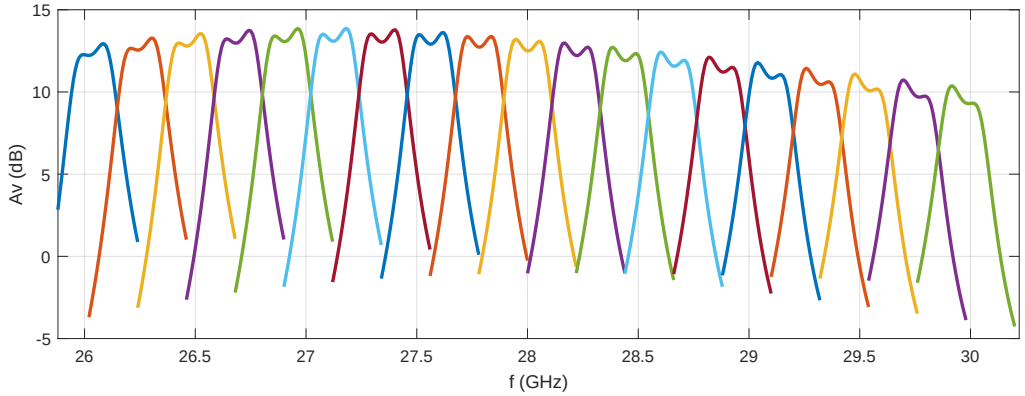


Figure 7.6: Simulated voltage gain for different values of f_{LO} between 26 and 30 GHz of the two-stage circuit with real components.

7.2.3. Linearity

The IIP_3 is simulated with two input signals at

$$\begin{aligned} f_1 &= f_{LO} + \Delta f \\ f_2 &= 2\,(f_{LO} + \Delta f) - f_{IM3} \end{aligned} \tag{7.1}$$

where f_{IM3} = 28.03 GHz. The IIP_3 is calculated using eq. (4.10) and shown in Figure 7.7a for different values of Δf. Figure 7.7b shows the simulated B_{1dB} for different blocker frequencies. This shows the effect of an OOB blocker on the gain compression point of a desired signal of -50 dBm at 28.05 GHz.

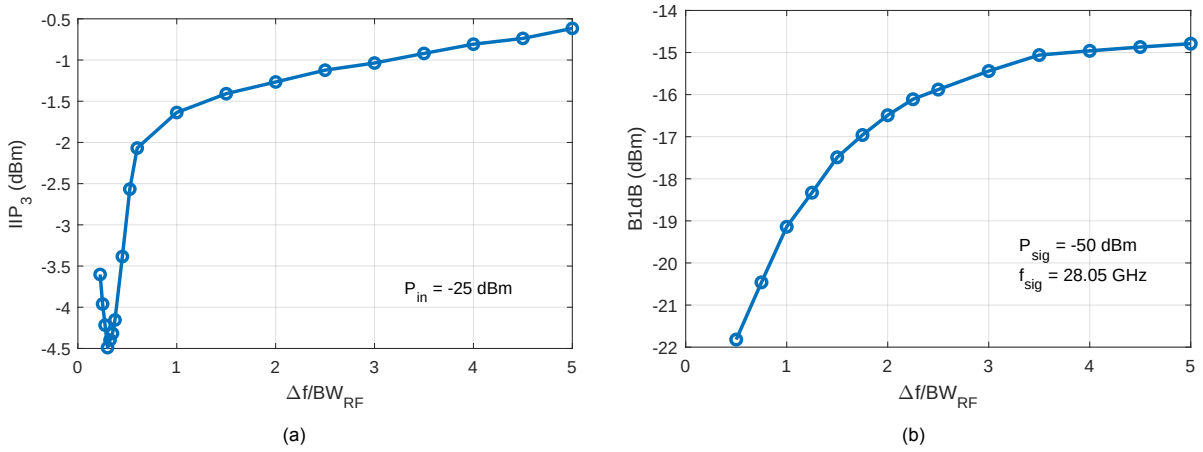


Figure 7.7: Simulated (a) IIP_3 and (b) B_{1dB} for different frequency offsets compared to f_{LO}. The frequency offset, Δf, is the offset of the first tone in the two-tone IIP_3 test, and equals the blocker frequency in the B_{1dB} simulation. The plots show the frequency offset relative to the RF BW (200 MHz), to compare the results to the state-of-the-art.

The simulated IB IIP_3 is -4.5 dBm. The OOB IIP_3 is -1.6 dBm at $\Delta f/BW_{RF}$ = 1 and -1.3 dBm at $\Delta f/BW_{RF}$ = 2. The obtained B_{1dB} is -19 dBm at $\Delta f/BW_{RF}$ = 1 and -16 dBm at $\Delta f/BW_{RF}$ = 2. The IP_{1dB} is simulated with only one tone at 28.05 GHz and is found to be -20 dBm.

7.2.4. Power consumption

The power consumption of the full circuit is 40.3 mW. This can be split into the consumption of the first stage LNA, the NPF LNAs, the g_m cells and the LO generation, as visualized in Figure 7.8. The simulated power consumption of the first stage LNA is 7.60 mW. The two LNAs inside the GB-NPF together consume 24.00 mW. The eight g_m cells use a combined power of 1.64 mW. The power consumption to generate the four-phase sinusoidal LO signals is estimated. The input impedance at the gate of each of the 16 NPF switches is simulated to be 10.9 kΩ, in parallel with 5.00 fF. The capacitance will be resonated out by the inductance of the clock generation circuit. The remaining resistance of 10.9 kΩ results in a power per switch of $(1.1\ V)^2/10.9\ k\Omega$ = 0.11 mW. For 16 switches, this power becomes 1.77 mW. Generating the sine waves with a class-A amplifier with a 25% power efficiency results in a consumed power of 7.10 mW.

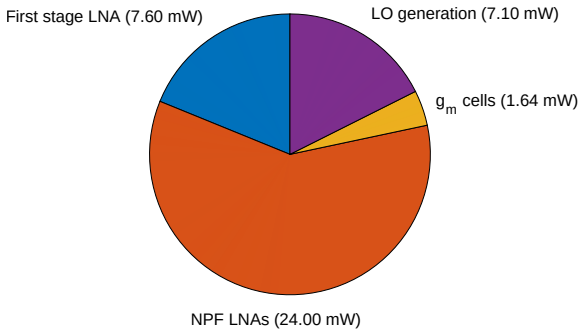


Figure 7.8: Power consumption of the different parts of the two-stage circuit with real components.

7.3. Comparison with state-of-the-art

The achieved performance of the designed NPF is compared with state-of-the-art NPFs at mm-wave in Table 7.1. The designed filter simultaneously achieves a large attenuation and a small BW. A larger attenuation is achieved by [6], which uses large inductors in the baseband filter. Decreasing the BW from 1000 MHz to 200 MHz increases the inductor size and its corresponding chip area. The noise figure is lower than the state-of-the-art, because of the added first stage LNA. The gain is equal to that of the receiver in [9], while consuming less power and achieving a larger attenuation. The linearity is however worse than the state-of-the-art, but still high enough to handle the blocker power levels of the

5G specification.

Table 7.1: Performance summary and comparison with state-of-the-art mm-wave NPFs.

		This work	JSSC2021 [6][a]	JSSC2021 [9]	RFIC2021 [53]
Architecture		LNA + active filter	Mixer first + BB amplifier + 3rd-order BB filter	Mixer first + BB amplifier	NPF shunt at input + BB amplifier with adjustable BW
Technology		40nm CMOS	65nm CMOS	28nm CMOS	45nm SOI CMOS
Supply voltage (V)		1.2	1.2	1.2	1.8
Frequency range (GHz)		26-30	21-29	10-35	6-31
-3 dB RF BW (MHz)		**200**	1000	400	180[b]
Filter order		4	6	2	4
Rejection center 1st adj.ch. (dB)		13.8	48[b]	7.8[b]	16[b]
Ultimate rejection (dB)		**24.2**	49	NR	17[b]
Voltage gain (dB)		**10-14**	3-6	11-15	-4.5 to -6.6
IIP3 (IB) (dBm)		-4.5	NR	10-14	1.6-6.3
IIP3 (OOB) (dBm)	$\Delta f/\mathrm{BW_{RF}} = 1$	-1.6	NR	NR	14
IP1dB (dBm)		-20	3	-2.5-0	-7.4 to -2
OOB B1dB (dBm)	$\Delta f/\mathrm{BW_{RF}} = 1$	-19	NR	NR	4.4
	$\Delta f/\mathrm{BW_{RF}} = 2$	-16	3.4	NR	NR
NF (26-30 GHz) (dB)		**10-12**	12-15	15-16	17-19
Power consumption (mW)		40	23	42-60	150-380
Active area (mm^2)		**0.2-0.3**[c]	0.63	NR	1.1[b]

[a] Baseband amplifier on. [b] Estimated from figure. [c] Estimated, excluding LO generation. [d] NR = not reported.

8

Conclusion and discussion

8.1. Outcome of the thesis

This thesis presented the theory, design and simulation results of a mm-wave NPF for 5G applications. This NPF uses a sine-wave LO to eliminate the need for higher harmonics. The effect of the sine wave on the NPF impedance is analyzed, after which the optimum bias voltage is chosen to provide the largest out-of-band attenuation. A gain-boosted architecture is used to provide gain and improve the out-of-band attenuation, which is otherwise limited by the difference between the switch and leakage resistance of the NPF. The GB-NPF with a first-order baseband filter cannot provide the required attenuation in the center of the first adjacent channel. The roll-off is improved by using two GB-NPFs with a frequency offset, which simultaneously provide a flat IB response. g_m cells shift charge between the baseband capacitors, to create a shift in the filter center frequency. The output of these filters is subtracted to create a large OOB attenuation at frequencies where the two filters achieve the same gain and opposite phase. The inputs are isolated to prevent charge leakage between the two NPFs. This isolation is done with inductors, instead of capacitors, to not decrease the gain and increase the NF by capacitive voltage division at the filter input.

Because of the limited phase difference between the two filter paths, the output subtraction causes a high NF. This is reduced by the addition of an LNA in front of the filter. This LNA is designed to have low noise, while providing a large gain to suppress the filter noise. The required area of the inductors, which provide optimum noise and impedance matching, is reduced by combining two as a transformer. This, at the same time, implements g_m boosting, which increases the LNA gain. The input matching design includes the pad capacitance and ESD diodes. The achieved ESD protection is +2400/-1950 V for the HBM and +125/-100 V for the MM.

The layout of the inductors, transformer, and NMOS of the first stage LNA is designed and used to obtain the simulation results in Cadence. The other components are schematic components from the TSMC library. After replacing the real components with the EM simulated version, the input reflection coefficient increased from $S_{11} \leq$ -17 dB to $S_{11} \leq$ -10 dB at 28 GHz. For the full frequency range of 26-30 GHz, the input matching is $S_{11} \leq$ -9.0 dB, which does not fulfill the required -10 dB. The NPF, with an RF BW of 200 MHz, achieves an IB gain of 13 dB, with a ripple of 0.6 dB. Even though the NPF is operated by a sine-wave LO, resulting in a smaller difference between R_{sw} and R_{leak}, a large attenuation is achieved. The attenuation at the center of the first adjacent channel is 14 dB, which increases to 24 dB at far-OOB frequencies ($\Delta f/BW_{RF}$ = 10). A slope of 34 dB per decade is achieved, which can be improved by tuning the gain and phase offset of the two filters, thereby adjusting the locations of the zeros. The total NF (including first stage LNA) is 10 dB at 28 GHz. While this does not fulfill the required 8 dB, the achieved NF is smaller than the state-of-the-art mm-wave NPFs. An IB IIP_3 of -4.5 dBm is obtained. The OOB IIP_3 is -1.6 dBm at $\Delta f/BW_{RF}$ = 1. The IP_{1dB} is -20 dBm IB and -19 dBm at $\Delta f/BW_{RF}$ = 1. The circuit consumes 40 mW of power, including the estimated power consumption of the LO. Other than the NF and S_{11}, all requirements of Table 1.1 are fulfilled.

To conclude, the filter designed in this thesis is the first active NPF at mm-wave, resulting in a large gain and attenuation. The BW is among the smallest reported, with a power consumption comparable to the state of the art. The designed filter is the smallest reported NPF at mm-wave.

8.2. Discussion

8.2.1. Achieved noise figure

With the addition of the first stage LNA, the achieved NF is lower than the state-of-the-art. The undesired effect of this LNA, besides its area and power consumption, is the reduced linearity of the circuit. Since the filtering happens only after the first stage, the interfering signals are amplified before arriving at the filter itself. For an LNA gain of 16 dB, the IP_{1dB} and B_{1dB} are reduced by roughly 16 dB.

In order to eliminate the need for a first stage amplifier, or at least reduce its required gain, the NF of the filter must be reduced. The large NF is partially inherent to the filter architecture. The subtraction of both filter paths reduces the signal power, while adding the uncorrelated noise powers of both filters [18]. The 1/f noise of the g_m cells operating at baseband is also a significant addition to the NF [54, 55].

Reducing the NF of the filter, first of all, requires a critical review of the subtraction architecture from [18], with the knowledge obtained in this thesis. Secondly, the LNA in the GB-NPF can be designed to have an optimum current density and input matching to achieve the lowest possible NF. This design method is already used for the first stage LNA, but can be expanded to the design of the GB-NPF LNAs as well. To reduce the noise of the NPF switches, their sizing can be reconsidered. This is reliant on the LNA design, since the input impedance and IB and OOB gain depend on both the NPF impedance and the g_m and r_O of the amplifier.

Lastly, the noise of the g_m cells can be reduced by increasing their transistor size. A larger width reduces the thermal noise and a larger $W \cdot L$ results in less flicker noise. Enlarging the g_m value also increases the frequency shift. Compensation can be done with larger baseband capacitors, which require smaller switch resistances to maintain a constant filter BW. The larger NPF switches and g_m cell transistors both result in a larger power consumption, which has to be sacrificed for a reduced NF. The increase in chip area is negligibly small, due to the small switches and capacitors in comparison with the large inductors and transformer. Increasing the transistor size, however, brings an increased parasitic capacitance to the baseband nodes. This reduces the gain of the circuit, which is not beneficial for the NF [20]. An optimum g_m cell size, for which the lowest NF is achieved, has been found in this thesis. Nonetheless, it is recommended to gain a better insight into the noise behavior of the g_m cells, which can potentially result in a reduced NF.

8.2.2. Achieved roll-off

The achieved roll-off of the fourth-order NPF is limited to 34 dB per decade. A theoretical 40 dB per decade is expected and for the NPF with ideal components, a simulated roll-off of up to 60 dB per decade is achieved. A large far-OOB attenuation is achieved when the gain and phase of both filters are (almost) equal at far-OOB frequencies. Having an equal gain and phase at frequencies close to the main band improves the attenuation at the adjacent channels and also the roll-off of the filter.

In this design, the gain of both filters is adjusted to provide a flat IB gain. This is done by using different values of the DC blocking capacitor at the output of each NPF. Besides adjusting the IB gain, this tuning also affected the OOB gain and phase. The difference in OOB gains at frequencies larger than f_{LO} causes the attenuation to be limited to 24 dB, while the attenuation at frequencies lower than f_{LO} gets as large as 38 dB. The gain of both paths can be adjusted to result in equal attenuation at the low and high frequencies, but cannot improve the attenuation in the adjacent channel.

The blocker rejection in the adjacent channel is limited by the relatively large phase difference between the two paths (Figure 7.3b). Increasing the phase of the first path can equalize the two paths' phases at a frequency close to the desired band. This adds a zero in the first or second adjacent channel, thereby significantly increasing the attenuation close to the desired band, and thereby also the roll-off. However, adjusting the phase to create a zero close to the main band leaves the far-OOB

frequencies with a large phase difference. There is a trade-off between the ultimate rejection at far-OOB frequencies, and the attenuation in the first adjacent channel.

Besides the gain and phase of the two paths, the roll-off of the filter can also be increased by using a smaller BW of each separate GB-NPF. The two filters then need a larger frequency offset to create the same BW after subtraction of 200 MHz. The steeper roll-off will not only be visible at the edge of the band, but also inside the band. The gain at f_{LO} will decrease, which causes a larger IB ripple. The maximum allowable ripple should be found by analyzing the effect of the ripple on the error vector magnitude (EVM), and depends on the used modulation scheme.

8.2.3. Reciprocal mixing of the phase noise

A downside of NPFs, compared to mixer-free BPFs, is the increased NF due to reciprocal mixing. The LO will have phase noise, which is modeled by a noise voltage at frequencies around f_{LO}. When mixing with a high power OOB blocker, this noise ends up in the main band. For a low-power desired signal, the noise from the reciprocal mixing can become problematic.
To better understand the effect of the phase noise, the NPF can be modeled as in Figure 8.1. The N mixing switches are replaced by a mixer, which performs both downconversion and upconversion. These two conversions can be split and modeled by two separate mixers, operated by the same LO [56].

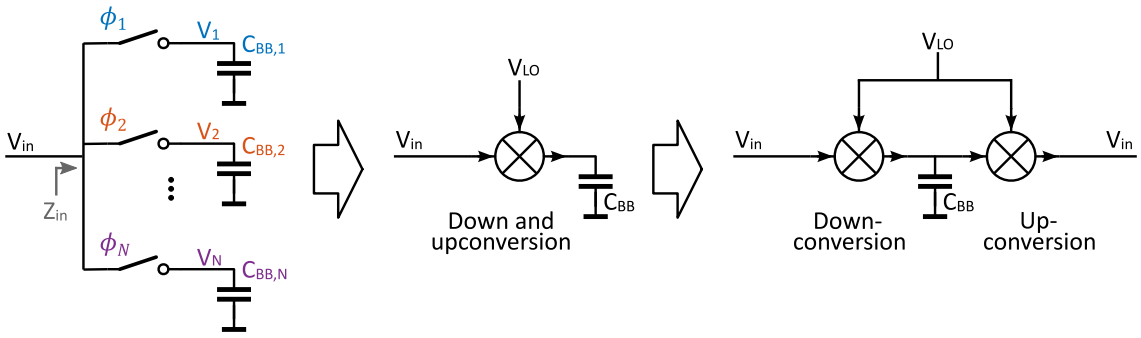


Figure 8.1: Model of the NPF to analyze the effect of LO phase noise.

The reciprocal mixing of the phase noise is explained with the use of Figure 8.2, where two different scenarios are analyzed. The first one, shown in Figure 8.2a, models the effect of an OOB blocker (1), which gets downconverted by the LO with phase noise (2). The phase noise is mixed with the blocker and arrives at low (IB) frequencies (3). After filtering with the baseband filter, the blocker is suppressed (4). Upconversion happens with the same noisy LO (2), but this time, the blocker power is suppressed, such that it does not mix again with the phase noise. The result is the upconverted baseband spectrum with a large phase noise around f_{LO} (5).

The second scenario, in Figure 8.2b, shows the effect of a large IB signal on the reciprocal mixing of the phase noise. The IB signal (1) mixes with the LO with phase noise (2), causing the phase noise to appear in the baseband spectrum (3). The filtering of the baseband LPF suppresses the noise at higher frequencies, but does not suppress the large power signal in the desired band (4). For the upconversion, the IB signal has the same amplitude as for the downconversion. Therefore, the phase noise of the LO is again mixed with this signal (5). Since the down and upconversion are down by the same LO, with the same phase noise, the noise arising in the upconversion is correlated with that of the downconversion. Because of the 180° phase difference, these noises are subtracted, resulting in a low phase noise inside the main band (6).

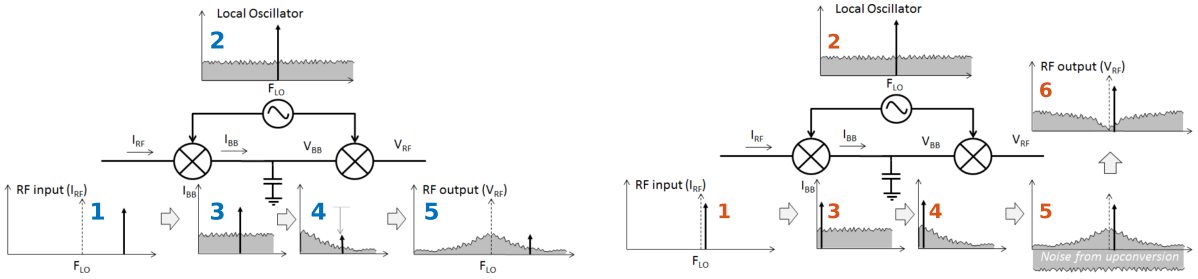


Figure 8.2: Reciprocal mixing of LO phase noise with blocker signal in a standalone NPF [56]. (a) An OOB blocker results in a large phase noise around f_{LO}, but a small phase noise at OOB frequencies. (b) For an IB signal, however, the phase noise is small around f_{LO} and large at OOB frequencies.

In the filter designed in this thesis, the reciprocal mixing with the LO phase noise is reduced by the attenuation in the input impedance. The NPFs do not only provide attenuation in the gain, but also in the input impedance. This attenuation is 4-7 dB, as shown in Figure 7.2a. OOB blockers get attenuated before mixing with the LO, resulting in a lower phase in the downconverted spectrum. Besides the attenuation in input impedance, the first stage LNA also causes attenuation of the signals outside the operating BW of 26-30 GHz. This reduces the power of the far-OOB blockers, minimizing their impact on noise folding.

The reciprocal mixing of the phase noise can intuitively be explained by a time shift in the LO phases. Mirzaei and Darabi [57] analyze this by splitting the noisy LO signal in an ideal clock and an error signal, as shown in Figure 8.3a. The LO phase noise effectively changes the clock phases, which can cause multiple paths to be turned on simultaneously or all paths to be turned off. The effect of phase noise is different for a sine LO, since the NPF switches are not instantaneously turned on and off. The sine wave clock only gradually opens and closes the switches, making it less sensitive to phase noise, as shown by the smaller error pulses in Figure 8.3b. Charge sharing is one of the effects of phase noise, which occurs when multiple switches are turned on at the same time. Reducing the conduction angle by decreasing V_{GS} of the NPF switches can reduce the charge leakage caused by the LO phase noise.

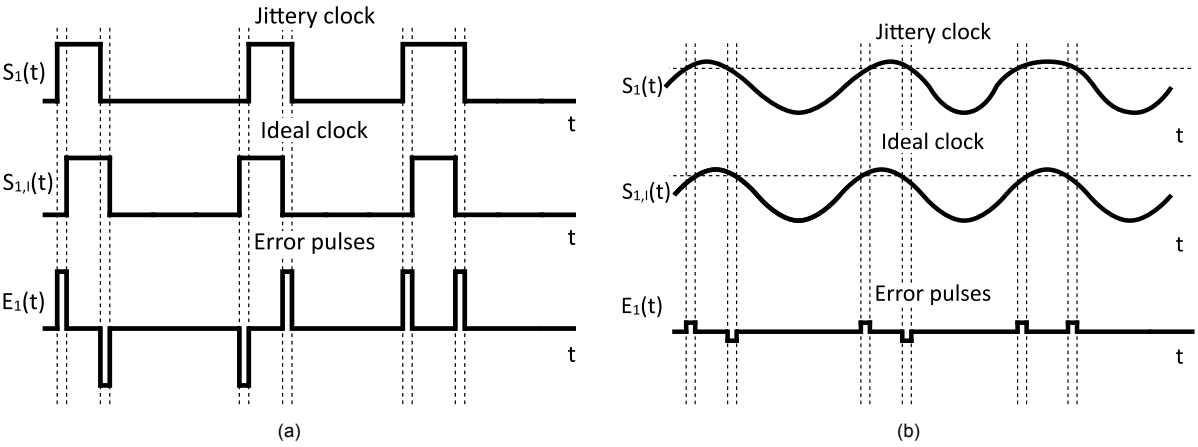


Figure 8.3: Modeling the effect of phase noise with an error signal. $S_1(t)$ is the clock signal of switch 1 including phase noise. The ideal clock is shown by $S_{1,I}(t)$ and $E_1(t)$ models the error signal. (a) A noisy square wave LO results in large error pulses [57]. (b) A noise sine wave LO results in smaller error pulses.

In conclusion, the mixing switches of the NPF cause an increase in IB NF due to reciprocal mixing of the phase noise. The filtering in the input impedance, and the reduced error pulses due to the sine LO, reduce the reciprocal mixing. It is, however, recommended for future work to develop a more detailed model of the reciprocal mixing of the phase noise, in order to understand and minimize its effect on the NF.

8.3. Recommendations for future research

- **Reduced noise figure** - As discussed in Section 8.2.1, the first stage LNA can be removed when the NF of the filter is decreased. It is recommended to carefully review the selection of the higher-order filter architecture, using the obtained insights of this thesis. Within this architecture, the noise can be reduced by designing the LNAs for optimum current density and noise matching, as described for the first stage LNA design. The LNA should be designed together with the NPF, to find the best NF while fulfilling the gain, attenuation and input impedance requirements. It is furthermore recommended to better understand the trade-off between noise and parasitic capacitance of the frequency shifting g_m cells, in order to further reduce their contribution to the NF.

- **Tunable zero location** - The attenuation in the first adjacent channel can be improved by having zeros close to the desired band. The subtraction of the two filters causes a zero when the gain and phase are equal. It is suggested to make the gain and phase of the two paths adjustable, to obtain a tunable zero location. A delay line can be added for the phase adjustment and the DC blocking capacitors in the current design can be made tunable to control the gain of each path.

- **Reduced power of NPF LNAs** - The LNAs of the GB-NPFs have the largest power consumption in the complete circuit. Redesigning these amplifiers for a higher g_m/I_D efficiency can reduce the power consumption. It is also recommended to design different amplifier topologies, for instance a cascode and inverter, such that they can be compared in the simulation instead of only theoretically.

- **g_m cell for 1.1 V supply** - The currently designed g_m cells require a supply power of 1.2 V in order to keep all transistors saturated. First of all, it is suggested to use separate bondwires and on-chip supply lines for these g_m cells to keep their V_{DD} and GND voltages constant and independent of the current consumption of the rest of the circuit. Secondly, it is recommended to research topologies that can work with a smaller supply voltage of 1.1 V or even lower.

- **Effect of phase noise** - Reciprocal mixing of the LO phase noise with OOB blockers results in an increased IB NF. The effect of the phase noise has not been modeled in this work, since a noise-free LO is used in the simulations. It is suggested to include phase noise in the design considerations of the NPF and to model the effect on the NF by using the method described in [57].

- **Alternative isolation method** - The inductors used for isolation of the two NPFs use a significant amount of area, due to their large sizes. Besides the use of lumped components (R,L,C), it can be investigated to use a different isolation method which uses less area.

- **Implementation on chip** - While the simulation results of the designed filter look promising, it is recommended to tape-out and measure the designed chip. The measurement results can, especially at mm-wave, differ significantly from the simulation results.

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Acronyms

3GPP 3rd Generation Partnership Project. 1

5G fifth generation. 1, 3, 75, 76

ACS adjacent channel selectivity. 1, 2

ADC analog-to-digital converter. 1, 2

B_{1dB} blocker power at 1 dB IB gain compression point. 43–45, 73, 74, 77

BPF band-pass filter. 5–9, 13, 17, 21, 25, 26, 28–30, 42, 78, 88

BSF band-stop filter. 7–9, 17, 25, 26, 28

BW bandwidth. i, 1, 2, 5, 6, 13, 20, 21, 23, 25, 27, 42, 44, 57, 59, 61, 62, 70, 72, 74–79, 88

CG common-gate. 36, 48, 49

CM common-mode. 33, 34, 40, 70

CS common-source. 17, 31, 35, 36, 39, 44, 48, 49, 58, 89

EEMCS Electrical Engineering, Mathematics and Computer Science. ii

ELCA Electronic Circuits and Architectures. ii

EM electromagnetic. 55, 67, 68, 70, 76

EOS electrical overstress. 54

ESD electrostatic discharge. 53–56, 58, 76

EVM error vector magnitude. 78

GB-NPF gain-boosted N-path filter. 4, 7, 14–17, 19–25, 28, 29, 31–33, 35–45, 71, 74, 76–78, 80, 89, 91

HBM human-body model. 53–56, 76

HPF high-pass filter. 25, 88, 89

IB in-band. 7, 8, 12–21, 28, 32, 33, 37, 40, 42–44, 68, 70, 71, 73, 74, 76–80

IC integrated circuit. 54

IIP_3 input referred third-order intercept point. 43, 44, 57, 58, 68, 69, 73, 74, 76

IP_{1dB} input power at 1 dB gain compression point. 2, 3, 44, 57, 68, 74, 76, 77

LNA low-noise amplifier. 2–4, 13–17, 19, 20, 23, 31–33, 35–37, 39, 40, 44–59, 62–65, 67–72, 74, 76, 77, 79, 80, 91, 93

LO local oscillator. 4, 8–14, 26, 28–30, 32, 33, 36, 38, 72–74, 76, 78–80

LPF low-pass filter. 5, 13, 21, 25, 29, 78, 88, 89

MIMO multiple input, multiple output. 2

MM machine model. 53, 54, 56, 76

mm-wave millimeter-wave. 1–5, 10, 11, 13, 23, 25, 27, 28, 31, 35, 54, 59, 70, 74–77, 80

NF noise figure. 19, 33, 38–40, 42, 48, 49, 53, 56–58, 67, 68, 72, 73, 76–80

NMOS N-channel metal-oxide-semiconductor. 7, 8, 10, 11, 13–15, 18–20, 36, 50, 52–56, 59, 62, 65–68, 70, 76, 91

NPF N-path filter. 3–22, 24–36, 38–40, 42, 44, 45, 47, 48, 58, 59, 61–64, 70–72, 74–80, 87, 91, 92

OOB out-of-band. 3, 7, 8, 12–19, 21, 23, 26, 28, 33, 37, 40, 42–44, 70–74, 76–80

RF radio frequency. 5, 6, 13, 21, 23, 33, 44, 74, 76, 87

RMS root mean square. 61

SCS subcarrier spacing. 1

SRF self-resonance frequency. 59–65

TSMC Taiwan Semiconductor Manufacturing Company. 40, 56, 60, 70, 76

TU Delft Delft University of Technology. ii

Symbols

$C_{\mathbf{BB}}$ baseband capacitor. 6–8, 13, 20, 40

D duty cycle. 7

L_p primary inductance. 63

L_s secondary inductance. 63

N number of paths. 6, 7, 9, 87

$R_{\mathbf{leak}}$ leakage resistance of NPF. 8, 12, 13, 15–17, 33, 76

$R_{\mathbf{sw}}$ switch resistance of NPF. 6–10, 12, 13, 15–17, 33, 76

R_L load resistor. 8, 16

$V_{\mathbf{GS}}$ gate-to-source voltage. 11–13

$V_{\mathbf{TH}}$ threshold voltage. 10

$Z_{\mathbf{NPF}}$ NPF impedance. 16

ϕ_1 phase of clock signal 1. 6

ϕ_N phase of clock signal N. 6

$\mathbf{BW_{-3dB}}$ -3 dB bandwidth. 3, 6

$f_{\mathbf{LO}}$ local oscillator frequency. 6–9, 13, 24, 42–44, 58, 69, 71–74, 77–79

$f_{\mathbf{RF}}$ RF frequency, received signal frequency. 6, 7, 29, 30

$f_{\mathbf{max}}$ maximum frequency of oscillation (unity power gain). 65

f_T transit frequency (unity current gain). 49

f_c center frequency. 3

$\mathbf{NF_{min}}$ minimum noise figure. 56, 57, 68

A

Derivation of equations

A.1. Passive filter order calculation

Implementing the required filter as a passive filter around 28 GHz requires a large filter order. The required order is calculated in this appendix. The filter is shown in Figure A.1.

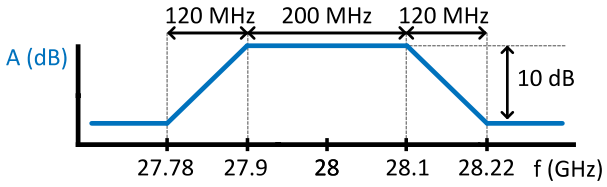

Figure A.1: BW and attenuation requirements of the filter centered at 28 GHz.

The order of this filter is found by splitting the BPF in a LPF and HPF, as shown in Figure A.2.

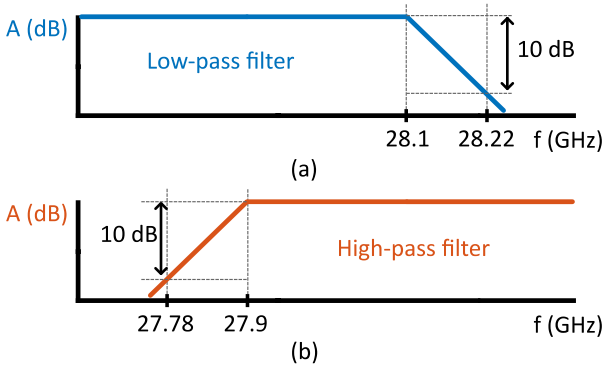

Figure A.2: BW and attenuation requirements of the LPF and HPF, which together form the BPF.

First, the required roll-off of the LPF is found in dB per decade. The filter has a cut-off frequency of 28.1 GHz and requires 10 dB attenuation at 28.22 GHz. The difference between these two frequencies is converted from Hz to the number of decades with eq. (A.1).

$$\Delta f_{\text{decade}} = \log_{10}\left(\frac{f_{2,\text{Hz}}}{f_{1,\text{Hz}}}\right) = \log_{10}\left(\frac{28.22\ \text{GHz}}{28.10\ \text{GHz}}\right) = 1.85 \times 10^{-3} \tag{A.1}$$

The required roll-off in dB per decade is

$$\frac{\Delta A_V}{\Delta f_{\text{decade}}} = \frac{\Delta A_V}{\log_{10}\left(\frac{f_{2,\text{Hz}}}{f_{1,\text{Hz}}}\right)} = \frac{10\ \text{dB}}{1.85 \times 10^{-3}} = 5403\ \text{dB/decade}. \tag{A.2}$$

A first-order filter achieves a roll-off of 20 dB per decade, thus the required filter order for the LPF is

$$\text{Filter order LPF} = \left\lceil \frac{\frac{\Delta A_V}{\Delta f_{\text{decade}}}}{20} \right\rceil = \left\lceil \frac{\Delta A_V}{20 \log_{10}\left(\frac{f_{2,\text{Hz}}}{f_{1,\text{Hz}}}\right)} \right\rceil = \left\lceil \frac{5403}{20} \right\rceil = 271. \tag{A.3}$$

The same calculation is done for the HPF in Figure A.2, resulting in a required filter order of

$$\text{Filter order HPF} = \left\lceil \frac{\Delta A_V}{20 \log_{10}\left(\frac{f_{2,\text{Hz}}}{f_{1,\text{Hz}}}\right)} \right\rceil = \left\lceil \frac{10 \text{ dB}}{20 \log_{10}\left(\frac{27.90 \text{ GHz}}{27.78 \text{ GHz}}\right)} \right\rceil = 268. \tag{A.4}$$

Together, this results in a filter order of

$$\text{Filter order BPF} = \text{Filter order LPF} + \text{Filter order HPF} = 539. \tag{A.5}$$

A.2. Gain boosted N-path filter equations

This section derives the equations for the input and output impedance, the voltage gain and the input noise voltage for the GB-NPF shown in Figure A.3.

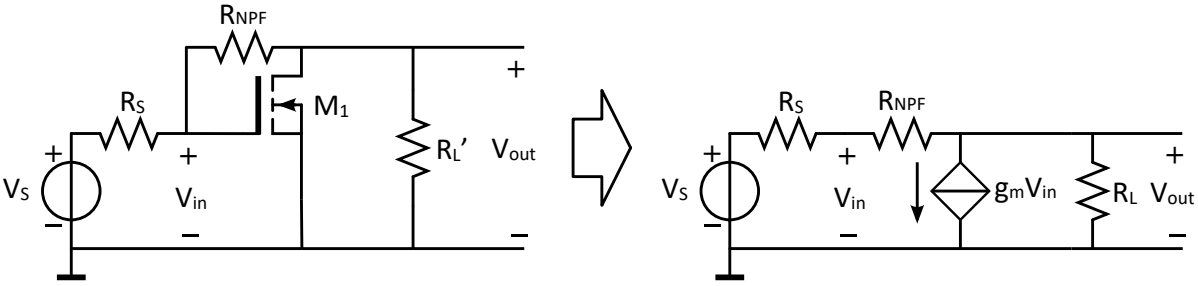

Figure A.3: small-signal model of CS amplifier with feedback impedance.

A.2.1. Input impedance

The current through R_{NPF} is

$$I_{NPF} = \frac{V_{in} - V_{out}}{R_{NPF}} = g_m V_{in} + \frac{V_{out}}{R_L} \tag{A.6}$$

$$V_{in}\left(\frac{1}{R_{NPF}} - g_m\right) = V_{out}\left(\frac{1}{R_L} + \frac{1}{R_{NPF}}\right) \tag{A.7}$$

$$V_{out} = V_{in}\frac{\frac{1}{R_{NPF}} - g_m}{\frac{1}{R_L} + \frac{1}{R_{NPF}}} = V_{in}\frac{R_L(1 - g_m R_{NPF})}{R_L + R_{NPF}} \tag{A.8}$$

$$\frac{I_{in}}{V_{in}} = \frac{1}{R_{NPF}}\left(1 - \frac{R_L(1 - g_m R_{NPF})}{R_L + R_{NPF}}\right) = \frac{1 + g_m R_L}{R_L + R_{NPF}} \tag{A.9}$$

The input resistance is

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{R_L + R_{NPF}}{1 + g_m R_L} \tag{A.10}$$

When $R_L \gg R_{NPF}$, this simplifies to $R_{in} = \frac{1}{g_m}$.

A.2.2. Output impedance

Voltage source at input is shorted. There will be a voltage V_{in} due to voltage division from the test voltage applied at the output. This will cause a current $g_m V_{in}$.

$$R_{out} = Z_L || (Z_F + Z_S) || \left(1 + \frac{Z_F}{Z_S}\right)\frac{1}{g_m} \tag{A.11}$$

A.2.3. Voltage gain

The voltage gain from input to output is calculated before. Here we calculate the voltage gain from source to output.

Current moving through R_S from the source to the output node is I_S.

$$V_{in} = V_S - I_S R_S \tag{A.12}$$

Node current equation at output node gives

$$I_S = g_m V_{in} + \frac{V_{out}}{R_L} \tag{A.13}$$

These two equations give

$$V_{in} = V_S - g_m R_S V_{in} - \frac{R_S}{R_L} V_{out} \tag{A.14}$$

$$V_{in}\,(1 + g_m R_S) = V_S - \frac{R_S}{R_L} V_{out} \tag{A.15}$$

$$V_{in} = \frac{V_S - \frac{R_S}{R_L} V_{out}}{1 + g_m R_S} \tag{A.16}$$

The current through R_{NPF} from input to output is

$$I_S = \frac{V_{in} - V_{out}}{R_{NPF}} \tag{A.17}$$

Combining eq. (A.12) and eq. (A.17) gives

$$V_{in} = V_S - \frac{R_S}{R_{NPF}} V_{in} + \frac{R_S}{R_{NPF}} V_{out} = \frac{V_S + \frac{R_S}{R_{NPF}} V_{out}}{1 + \frac{R_S}{R_{NPF}}} \tag{A.18}$$

$$V_{in} = \frac{R_{NPF} V_S + R_S V_{out}}{R_{NPF} + R_S} \tag{A.19}$$

Equating eq. (A.16) and eq. (A.19) gives

$$\left(V_S - \frac{R_S}{R_L} V_{out}\right)(R_{NPF} + R_S) = (R_{NPF} V_S + R_S V_{out})\,(1 + g_m R_S) \tag{A.20}$$

$$V_S\,[R_S + R_{NPF} - R_{NPF}(1 + g_m R_S)] = V_{out}\left[R_S(1 + g_m R_S) + \frac{R_S}{R_L}(R_S + R_{NPF})\right] \tag{A.21}$$

$$A_v = \frac{V_{out}}{V_S} = \frac{R_L(1 - g_m R_{NPF})}{R_L(1 + g_m R_S) + R_S + R_{NPF}} \tag{A.22}$$

For a matched input impedance, with $R_{in} = \frac{R_L + R_{NPF}}{1 + g_m R_L}$, the gain simplifies to

$$\begin{aligned} A_v = \frac{V_{out}}{V_S} &= \frac{R_L(1 - g_m R_{NPF})}{R_L\left(1 + g_m\left(\frac{R_L + R_{NPF}}{1 + g_m R_L}\right)\right) + \frac{R_L + R_{NPF}}{1 + g_m R_L} + R_{NPF}} \\ &= \frac{R_L(1 - g_m R_{NPF})(1 + g_m R_L)}{R_L(1 + g_m R_L + g_m\,(R_L + R_{NPF})) + R_L + R_{NPF} + R_{NPF}(1 + g_m R_L)} \\ &= \frac{R_L(1 - g_m R_{NPF})(1 + g_m R_L)}{2(R_L + R_{NPF})(1 + g_m R_L)} \\ &= \frac{R_L(1 - g_m R_{NPF})}{2(R_L + R_{NPF})} \end{aligned} \tag{A.23}$$

A.2.4. Noise figure

The input noise voltage of the GB-NPF is calculated, considering the noise sources in Figure A.4. First, the input noise originating from the NMOS transistor of the LNA is calculated, after which the contribution of the NPF is calculated.

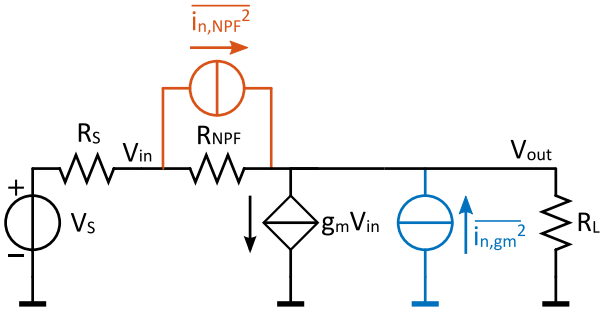

Figure A.4: small-signal model of the GB-NPF, with noise sources of the LNA and NPF.

Noise from NMOS

The LNA noise current is

$$\overline{i_{n,gm}^2} = 4kT\gamma g_m \tag{A.24}$$

Its contribution to the output noise voltage can be calculated using the nodal equations (KCL) on the input and output node. KCL on the input node gives

$$\frac{V_{in}}{R_S} = \frac{V_{n,out|\text{gm}} - V_{in}}{R_{\text{NPF}}} \tag{A.25}$$

$$V_{in} = \frac{R_S}{R_S + R_{\text{NPF}}} V_{n,out|\text{gm}} \tag{A.26}$$

KCL on the output node gives

$$\overline{i_{n,\text{gm}}} = \frac{V_{in}}{R_S} + g_m V_g + \frac{V_{n,out|\text{gm}}}{R_L} \tag{A.27}$$

With

$$V_g = V_{n,out|\text{gm}} \frac{R_S}{R_{\text{NPF}} + R_S}, \tag{A.28}$$

and eq. (A.26) this gives

$$\overline{i_{n,\text{gm}}} = \frac{R_S}{R_S + R_{\text{NPF}}} V_{n,out|\text{gm}} \frac{1}{R_S} + g_m V_{n,out|\text{gm}} \frac{R_S}{R_{\text{NPF}} + R_S} + \frac{V_{n,out|\text{gm}}}{R_L} \tag{A.29}$$

$$\overline{i_{n,\text{gm}}} = V_{n,out|\text{gm}} \left[\frac{1}{R_S + R_{\text{NPF}}} + g_m \frac{R_S}{R_{\text{NPF}} + R_S} + \frac{1}{R_L} \right] \tag{A.30}$$

$$\begin{aligned} \frac{V_{n,out|\text{gm}}}{\overline{i_{n,\text{gm}}}} &= \frac{1}{\frac{1}{R_S + R_{\text{NPF}}} + g_m \frac{R_S}{R_{\text{NPF}} + R_S} + \frac{1}{R_L}} \\ &= \frac{R_S + R_{\text{NPF}}}{1 + g_m (R_S) + \frac{R_S + R_{\text{NPF}}}{R_L}} \\ &= \frac{R_L (R_S + R_{\text{NPF}})}{g_m R_L (R_S) + R_S + R_{\text{NPF}} + R_L} \end{aligned} \tag{A.31}$$

This is equal to the calculated output impedance of the circuit (concluded based on equation derivation).

$$\frac{V_{n,out|\text{gm}}}{\overline{i_{n,\text{gm}}}} = R_{out} = R_L || (R_{\text{NPF}} + R_S) || \left(1 + \frac{R_{\text{NPF}}}{R_S} \right) \frac{1}{g_m} \tag{A.32}$$

The input referred noise voltage is calculated by dividing the output noise voltage over the voltage gain from source to output. This gain is obtained the same way as in appendix A.2.3.

$$A_{v,S\to out} = \frac{V_{out}}{V_S} = \frac{R_L(1-g_m R_{\text{NPF}})}{R_L(1+g_m(R_S))+R_S+R_{\text{NPF}}} \tag{A.33}$$

The input referred noise voltage due to the thermal noise of the NMOS is

$$\overline{V^2_{n,\text{in}|\text{gm}}} = \frac{V^2_{n,out|\text{gm}}}{A^2_{v,S\to out}} = \frac{R^2_{out}}{A^2_{v,S\to out}}\overline{i_{n,\text{gm}}} \tag{A.34}$$

$$\begin{aligned}\overline{V^2_{n,\text{in}|\text{gm}}} &= \frac{\left(\frac{R_L(R_S+R_{\text{NPF}})}{g_m R_L(R_S)+R_S+R_{\text{NPF}}+R_L}\right)^2}{\left(\frac{R_L(1-g_m R_{\text{NPF}})}{R_L(1+g_m(R_S))+R_S+R_{\text{NPF}}}\right)^2}\overline{i^2_{n,\text{gm}}} \\ &= \frac{\left(\frac{R_L(R_S+R_{\text{NPF}})}{g_m R_L(R_S)+R_S+R_{\text{NPF}}+R_L}\right)^2}{\left(\frac{R_L(1-g_m R_{\text{NPF}})}{g_m R_L(R_S)+R_S+R_{\text{NPF}}+R_L}\right)^2}\overline{i^2_{n,\text{gm}}} \\ &= \left(\frac{R_S+R_{\text{NPF}}}{1-g_m R_{\text{NPF}}}\right)^2\overline{i^2_{n,\text{gm}}}\end{aligned} \tag{A.35}$$

Noise from NPF

The noise contribution of R_{NPF} can be calculated using the small-signal model in Figure A.4, where the noise is modeled as a current source in parallel to R_{NPF}.

$$\overline{i^2_{n,NPF}} = \frac{4kT}{R_{\text{NPF}}} \tag{A.36}$$

The noise splitting theorem is used to replace the current noise source by two separate sources from each node to ground [58].

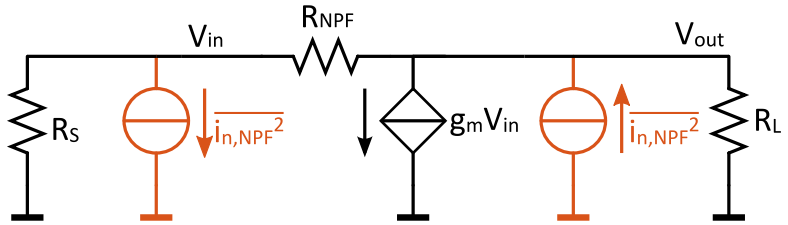

Figure A.5: Current noise source of R_{NPF} can be split in two noise currents connected to ground.

The noise current at output node causes an input noise voltage the same way as the NMOS noise current:

$$\overline{V_{n,\text{in}|NPF,1}} = \frac{R_S+R_{\text{NPF}}}{1-g_m R_{\text{NPF}}}\overline{i_{n,NPF}} \tag{A.37}$$

The noise current at the input must be multiplied by the impedance connected to the input node, $R_S||R_{in}$. When the input impedance is matched to the source impedance, this simplifies to $R_{in}/2$.

$$\overline{V_{n,\text{in}|R_{NPF},2}} = -\frac{R_{in}}{2}\overline{i_{n,R_{NPF}}} = -\frac{R_L+R_{NPF}}{2(1+g_m R_L)}\overline{i_{n,R_{NPF}}} \tag{A.38}$$

Since these two noise source are originating from the same source, they are fully correlated. The total input referred noise voltage from the NPF is therefore simply the addition of these two noise voltages.

$$\overline{V^2_{n,\text{in}|R_{NPF}}} = \left[\frac{R_S+R_{\text{NPF}}}{g_m R_{\text{NPF}}-1}+\frac{R_L+R_{NPF}}{2(1+g_m R_L)}\right]^2\overline{i^2_{n,R_{NPF}}} \tag{A.39}$$

A.2.5. Relation between r_O and R'_L for a required $Z_{\text{in,IB}}$

Starting with

$$Z_{\text{in,IB}} = \frac{R_L + Z_{\text{NPF,IB}}}{1 + g_m R_L}, \tag{A.40}$$

R_L is replaced with $R'_L \| r_O$ and $Z_{\text{NPF,IB}} = aR_L + b$.

$$\begin{aligned} Z_{\text{in,IB}} &= \frac{R'_L \| r_O + aR_L + b}{1 + g_m \left(R'_L \| r_O\right)} \\ &= \frac{R'_L \| r_O (1 + a) + b}{1 + g_m \left(R'_L \| r_O\right)} \end{aligned} \tag{A.41}$$

The LNA gain is estimated to be $g_m r_O = 5$, thus $g_m = 5/r_O$.

$$\begin{aligned} Z_{\text{in,IB}} &= \frac{\frac{R'_L r_O}{R'_L + r_O}(1 + a) + b}{1 + 5\frac{R'_L}{R'_L + r_O}} \\ &= \frac{R'_L r_O (1 + a) + b(R'_L + r_O)}{6R'_L + r_O} \end{aligned} \tag{A.42}$$

$$R'_L r_O (1 + a) + b(R'_L + r_O) = (6R'_L + r_O) Z_{\text{in,IB}} \tag{A.43}$$

$$r_O \left[R'_L (1 + a) + b - Z_{\text{in,IB}}\right] = R'_L \left[6Z_{\text{in,IB}} - b\right] \tag{A.44}$$

Thus,

$$r_O = \frac{R'_L \left(6Z_{\text{in,IB}} - b\right)}{R'_L (1 + a) + b - Z_{\text{in,IB}}}. \tag{A.45}$$