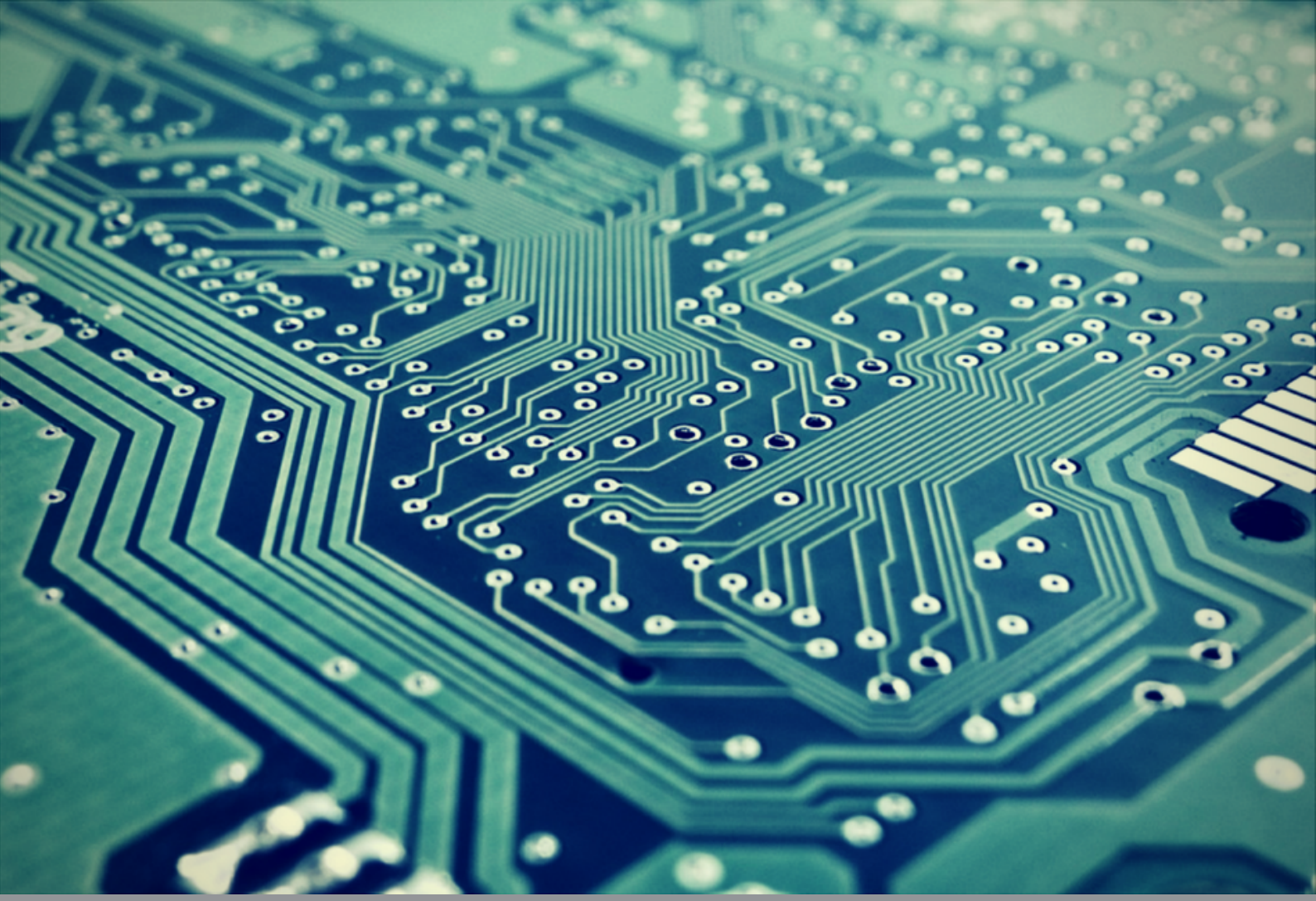

Technische Universiteit Delft

Fast Fault Detection and Protection

in low voltage direct current (LVDC) networks

MSc Thesis

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TU Delft

Fast Fault Detection and Protection

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Samad
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Abstract

Low voltage direct current (LVDC) networks used as electricity distribution systems for a community have the potential of operating at higher efficiencies and can integrate various distributed renewable energy sources and storage elements. However, their emergence is being hindered due to the lack of reliable fault protection techniques. DC faults exhibit extremely fast current rise rates as compared to faults in AC grids. Therefore, this research focuses on developing a fast fault detection and isolation technique applicable especially in LVDC networks. Fault isolation was achieved via solid state circuit breakers (SSCB) due to their fast functioning capability and high controllability levels. For quick fault detection two distinct techniques were selected. The first measured the distribution line's rate of change of current while the second technique determined the current magnitude by measuring the on-state voltage across the SSCB's semiconductor device. The complete design of the fault detection circuits leading to isolation has been presented in this research work. The performance of both the designed detection circuits and fault isolation via the SSCB have been validated through practical experiments. The results demonstrated that isolation of the fault subsequent to its occurrence is achievable in just a few microseconds. Hence, this implies that the fast rising DC fault currents can be detected and interrupted in adequate time prior to resulting in any hazardous consequences.

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1 Introduction

The first chapter is an introduction to the thesis topic. First, it provides some information to familiarize the reader with some important background knowledge. This is followed by the problem definition and the motivation behind the thesis. The potential contribution of this research is stated in the form of the thesis aim. Next, the major research questions that will need to be answered to fulfill the aim are presented. Finally, a layout of the further contents in the report is given.

1.1. Thesis Background

The advancements in the technological fields of power electronics and smart grids are enabling future electricity distribution systems to become more efficient and cost-effective. These fields will help in meeting the ever increasing demand of electricity in the future. As today's power distribution systems are slowly incorporating modern energy sources to satisfy demands, the overall system also needs to be optimized in order to develop an electricity distribution network capable of benefiting from the technological advancements.

It is common knowledge that the traditional electricity distribution networks are alternating current (AC) based. In the late 1800's, during the 'war of the currents' AC based networks prevailed over direct current (DC) based. This was because of the availability of transformers that could easily step up or down the AC voltage making transmission of electricity over long distances much more efficient. At that time, there was no mature technology enabling DC voltage levels to be changed easily and hence, DC power was not considered for electricity transmission.

However, with technological advancements especially in power electronics, DC systems now possess the capability of being used in various applications [7]. In fact many electronic devices, household loads and electric vehicles require DC power. Various renewable energy sources (RES) also produce a DC output. As a result, DC distribution systems are seriously being considered. This is because DC can potentially operate more efficiently than low voltage AC networks. The main reasons for this are that the number of AC-DC conversion steps will be significantly reduced, decreasing the amount of system losses. Moreover, DC systems are not liable to the 'skin effect' and the effective value of voltage or current always equals the peak value (for AC, the effective value is lower by a factor of 1.41). This enables DC networks to transfer larger amounts of power for the same cable sizes. There is also no need to transfer reactive power over the distribution lines, again increasing the potential of delivering greater power. Additionally, multiple RES can be directly incorporated in a DC network without the trouble of frequency and phase synchronization. These advantages make the implementation of DC networks an attractive option.

Already DC networks are functional in some areas of the world. These are at high voltages and are known as HVDC grids. These grids are mainly used to transfer power across long distances economically. Along with easy control, HVDC grids realize all the advantages of DC transmission [8]. HVDC technology is also being preferred to HVAC technology to integrate RES like offshore wind power plants [9].

The possibility of using DC power systems at low voltages, known as low voltage direct current (LVDC) networks is still not widely used. The main applications to date are in data centers, electric

traction systems and telecommunication systems. However, due to enhancements in technology, LVDC systems as 'last mile' electricity distribution networks have the potential of fulfilling the challenges of future smart grids [10]. They can directly power up various types of DC loads without the need of an AC stage. Furthermore, small scale RES and energy storage devices can be easily connected to an LVDC network, key items of a future smart grid [10]. Therefore, LVDC networks have the potential of replacing traditional local distribution systems.

However, the implementation of LVDC networks on a large scale is being obstructed by the challenges faced by DC grids. One particular obstacle is the lack of standardization of LVDC distribution systems. For an AC system, there are clear standards about transmission and distribution voltage levels, frequency and system architecture. This makes it easier to design and test new products. However, there is not a widely accepted standard for LVDC networks. The IEC 60038 standard only defines the maximum range of low voltage DC as 1500V [11]. Within this range, there are several applications operating at different voltage levels. Some examples are of data centers at 380V, electric vehicles at 400V and public transport traction systems between 750 - 1500V [11]. As an LVDC distribution network can be used for several applications (simultaneously) a clear operating voltage standard is missing. This can create a feeling of unreliability between different research work and make it difficult for results to be compared. As a result, standardization for an LVDC distribution network is desperately required to ensure research compatibility and an increase in the knowledge pool.

Another major reason hindering the wide scale use of LVDC networks is the lack of reliable protection schemes in the event of a fault. Fault refers to an abnormal condition in the grid. This can be a severe short-circuit, temporary ground connection or a lightning surge. A fault can have damaging effects on the DC network and its auxiliary equipment. Moreover, DC faults have different characteristics than AC faults and can be more hazardous. DC distribution lines usually have less inductance and as a result, large currents can flow in very short times. In addition, the traditional AC circuit breakers are not fit for use in DC networks because they rely on the natural zero crossings of the current, a phenomenon not inherently observed in DC current [12].

Currently there is a real lack of commercially available technology regarding DC fault protection. This is hindering the emergence of LVDC networks. From a safety perspective, it is essential to develop reliable protection systems. In order for this to be achieved, DC faults and their characteristics will first have to be understood. Only then can the advantages of LVDC distribution netwroks as part of a future smart grid setup be realized.

1.2. Thesis Motivation

The protection of the DC grids in operation today (mostly HVDC) is implemented on the AC side. If a fault occurs in the DC distribution lines, AC circuit breakers located after the DC terminals are opened to cut off the current [13], [14]. The major disadvantage of this method is that AC circuit breakers inherently take a relatively long time (40-50 milliseconds) to interrupt the fault. This can be dangerous for the semiconductor components of the power electronic converters used to interface the AC and DC lines as they are unable to conduct large currents beyond their nominal ratings. Hence, the converters are over designed in order to survive the huge currents, at the expense of extreme increase in costs. Moreover, in this configuration in case of a fault the entire DC grid has to be usually shut down to isolate the fault. This causes inconveniences and disruption of power in areas that are not even in the vicinity of the fault.

Recently, DC circuit breaker technology has developed significantly. Y. Li et. al. in [13] report that ABB has developed a hybrid DC circuit breaker for HVDC grids capable of interrupting fault currents within 2 milliseconds. A hybrid circuit breaker uses a combination of a solid state circuit breaker (SSCB) and a mechanical switch to quickly isolate the faulted section. A pure SSCB based DC circuit breaker has also been researched. As they have no moving parts they can interrupt fault currents even faster (in microseconds) [15]. An SSCB used for HVDC applications consists of several transistors in series. The reason is to be able to block the high grid voltages when the SSCB is opened to interrupt the current flow. This causes the overall turn-on voltage to be significantly large if the SSCB comprises of IGBTs (if MOSFETs, the drain resistance) during normal operation. Hence, the SSCB tends to have higher power conduction losses and also becomes expensive [8], [13].

However, there are still no commercially available fault protection solutions especially for LVDC networks relying only on DC circuit breakers. Direct translation of fault protection measures from HVDC

to LVDC might not be a feasible option due to differences in operating distances, voltage and power levels. As a result, there is a desperate need for the development of protection schemes particularly for LVDC networks. Hence, the main motivation for this research work is to contribute to the development of reliable and fast protection systems for LVDC networks. This is absolutely necessary in order for them to be used safely, a factor which cannot be compromised at all. To achieve this, it is imperative to understand the different steps involved in the protection of LVDC networks.

Fault protection can be broadly divided into four categories. These are detection, classification, location and isolation [16]. Fault detection refers to identifying when an abnormal condition occurs in the DC network. An abnormal condition is mostly an increase of current in the distribution lines beyond the nominal rated value. Due to low line impedances, the rate of current rise can be quite fast. Therefore, this demands that fault detection should also be fast. For this purpose, fault detection circuits need to be implemented in the DC distribution lines. These detection circuits should work by measuring and processing signals directly from the DC distribution lines.

Moreover, the signals measured by the detection circuit can also be used in the classification and location of the fault. This information can be useful in determining the necessary action to be taken to remedy the fault. Some faults can be classified as temporary and non-threatening while others can be extremely dangerous and should be isolated immediately. Thus, the protection system can be designed to operate based on the type and position of the fault.

In addition, fault isolation indicates the protective measures taken by the circuit breakers based on the information processed by the detection circuits. These circuit breakers operate in a 'normally on' operation. After fault detection, appropriate signals are sent to the breakers to isolate the faulted distribution line. In an LVDC distribution network, isolation can be done using hybrid DC circuit breakers or SSCBs. Due to the lower voltage and power levels the use of SSCBs is realizable and possibly more advantageous [14].

1.3. Thesis Aim

From the details provided for DC fault protection in the previous section, fault detection is the most crucial part. Fault isolation via DC circuit breakers and subsequently, the protection of the network is entirely dependent on detecting the fault in adequate time. This imposes a challenge to design fast detection circuits. Hence, to fulfill the design challenge these circuits will have to act based on the transients observed after fault occurrence [17].

Moreover, the resulting signals from the detection circuits should be processed quickly and in the event of a fault being detected, protection action should be initiated immediately. This can be a change in the gate driver's output (from high to low) for fault isolation via a SSCB.

Hence, the main objective of the thesis revolves around these factors and is stated below:

"The aim is to develop a fault detection method for LVDC networks. The method should be fast in operation in order to design an overall quick acting protection system for LVDC networks"

1.4. Research Questions

To achieve the bold aim mentioned above, the major research questions that will need to be answered along the way are:

- **What can be the admissible methods for detecting a fault in DC transmission lines?**

  This question can be answered by conducting a literature review to gain insight about the methods used for detecting faults in DC distribution lines. Next, the methods that can be used particularly for LVDC networks will be analyzed.

- **What factors are important in selecting a suitable fast fault detection method?**

  Identify the pertinent features for detecting a fault in DC distribution lines. On the basis of these highlighted features, choose an appropriate method that is fast and accurate in determining the occurrence of a fault.

- **How to design the circuitry of the appropriate fault detection method?**

  Understand the design requirements of the chosen detection method. Then design the circuit such that it can accurately measure the relevant signals required in detecting a fault. The circuit design should also be realized practically.

- **What are the key aspects in assessing the performance of the selected detection method and the protection system?**

  Develop a protection system for isolation of faults occurring in the DC distribution lines. Define parameters on which the performance of the designed fault detection method will be judged. Perform practical experiments to validate the working of the detection method and assess its performance.

1.5. Report Outline

The chapter provided a brief introduction to the thesis topic. This was followed by the aim of the thesis and the major research questions to be answered in the thesis work.

Furthermore, the report includes five more chapters. Chapter 2 is a literature review about the various fault detection methods applicable in LVDC networks. It helps to answer the first and second major research questions stated in the previous section. In the third chapter, the most suitable fault detection methods are selected. The major focus of this chapter is towards the circuit design of these selected methods. Therefore, the third chapter also partly answers the second and the third major research question completely.

Next, after the detection of a fault, the fault has to be isolated via the solid state circuit breaker. Hence, chapter 4 discusses fault isolation after a fault has been detected by the designed circuits. This will help in answering the fourth and final major research question of the thesis. Chapter 5 contains the hardware implementation of the entire thesis work. It aims to practically validate the theory and the circuit designs proposed in the previous sections. Finally, a summary of the thesis in the form of a conclusion and some future recommendations are included in the final chapter.

2

Detection Methods

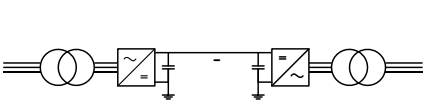
This chapter outlines the literature study of the thesis and the major insights gained from the reviewed literature. The first section highlights the characteristics of DC faults to help understand the requirements of fast fault detection. The next two sections present various applicable fault detection methods in LVDC networks. Furthermore, the following section talks about the important challenges still remaining before fast fault detection and protection can be implemented. The applicable fault detection methods for LVDC networks are briefly summarized in the final section of this chapter.

2.1. Characteristics of DC Faults

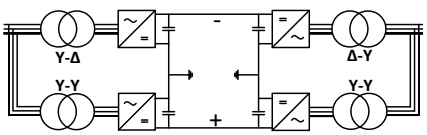
In order to design reliable DC fault detection methods, the characteristics of DC faults first need to be understood. These characteristics refer to the changes observed in the grid (mainly in the voltages and currents) after a fault has occurred. DC fault characteristics have both a transient phase and a steady state. The duration of the transient phase is dependent on various parameters. Therefore, appropriate detection methods can be selected that can operate quickly based on the fault characteristics shown.

DC fault properties are dependent on various factors. Some of these factors are the DC distribution system's architecture, the type of fault and grounding of the DC lines. These features of DC grids need to be discussed in detail to fully understand the characteristics of DC faults.

DC system architecture can be classified into 3 categories; monopolar, bipolar and homopolar DC links. The simplest of these is the monopolar DC link. It uses a single conductor to transfer power and earth ground as the return path. The conductor has negative polarity to reduce corona effects [18]. Sometimes a metallic return conductor is also used as a neutral line. Meanwhile, a bipolar system architecture consists of 2 conductors, one at a positive voltage potential and the other at the same negative voltage potential. A third conductor serving as a neutral line is usually also included. Bipolar architectures are capable of delivering double the power of monopolar architectures however, they normally require double the number of voltage source converters (VSC) and are more expensive [18]. Homopolar DC system architectures are similar to bipolar, except that both the conductors have the same polarity. Figure 2.1 shows a visualization of 2 different system architectures.



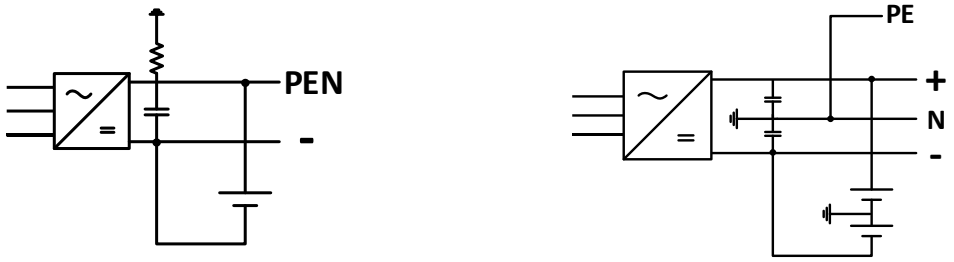
(a) Monopolar DC Grid



(b) Bipolar DC Grid

Figure 2.1: DC System Architectures

Furthermore, DC faults can show different characteristics based on the grounding structure of the DC grid. Grounding of LVDC grids can be done in several methods, high resistance grounded, low



(a) IT DC system

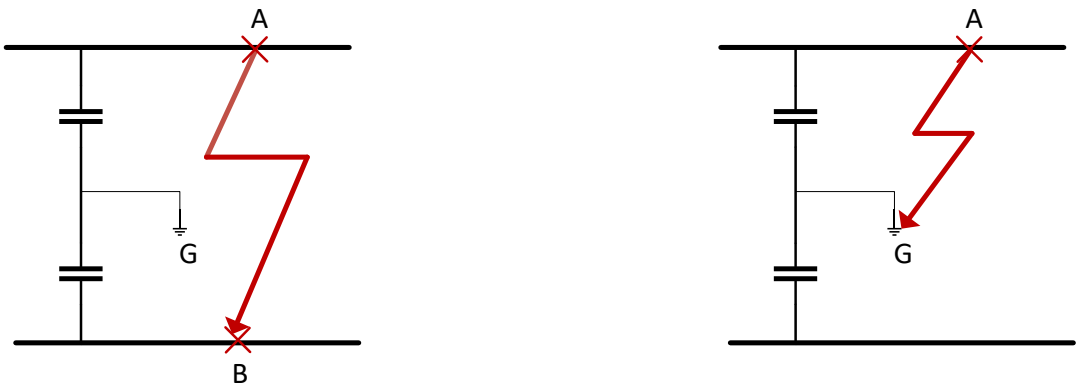
(b) TN-S DC system

Figure 2.2: LVDC grounding

resistance grounded or even left ungrounded. Two alternate grounding systems for LVDC grids are shown in figure 2.

Figures 2.2a and 2.2b show a VSC used to interface a 3 phase AC grid with two different DC system architectures (monopolar and bipolar). They also show the preferred grounding systems of the architectures. In an IT DC ground system, one conductor is connected to ground through an impedance. In most cases the grounded conductor is the neutral line. Hence, it forms a protective earth neutral (PEN) line. This system is most suited to a monopolar DC architecture that includes a return conductor. A monopolar system without a return conductor would naturally be left ungrounded. Conversely, a TN-S ground system directly grounds the neutral line without any impedance. It also uses different conductors for protective earth (PE) and neutral (N) to have no interference during normal operation of the system [19].

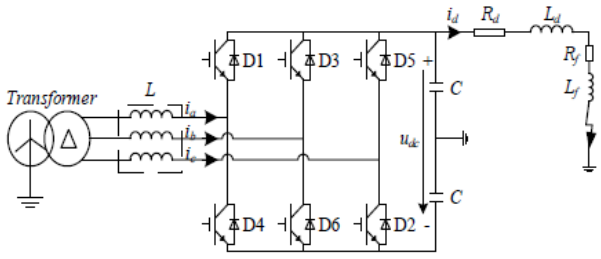
Additionally, there are 2 fault categories in DC grids, a line to line fault or a line to ground fault. In a grid, line refers to a current carrying conductor. A line to line fault results in a conduction path being formed between two conducting lines. This type of fault is observed in bipolar DC systems. The fault usually results in a short-circuit and extremely large currents can flow from the lines into the fault. A line to ground fault occurs when a path is created between a conductor and ground. The consequences of a line to ground fault are dependent on the fault's impedance and can also be severe. Figure 2.3 shows a visualization of both types of faults in a bipolar or homopolar DC grid. Figure 2.3a depicts a line to line fault between points A and B while 2.3b shows a line to ground fault at point A.



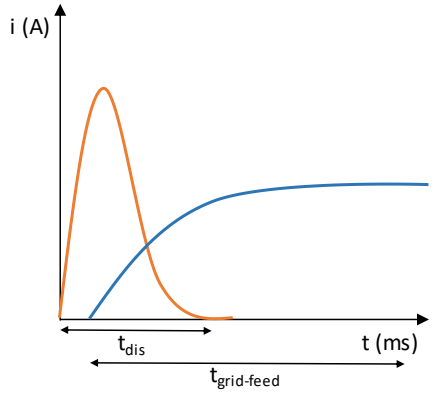
(a) Line to line fault

(b) Line to ground fault

Figure 2.3: Fault types in DC grids



(a) Equivalent circuit after fault occurrence [20]



(b) DC line's current rise after fault occurrence

Figure 2.4: Diagram of a positive line to ground fault

With knowledge about some important factors affecting DC grid fault behaviour, DC fault characteristics of each fault type can be elaborated. Figure 2.4a shows the equivalent circuit of a bipolar DC transmission line with a positive line to ground fault. The insulated gate bipolar transistors (IGBT) represent the VSC, U_{dc} the line to line voltage, i_d the line current, R_d and L_d the line parameters and R_f and L_f the fault impedance.

If the fault has a low impedance, an immediate voltage transient is observed (due to a large rate of change of current) and the faulted line capacitor starts discharging rapidly [19]-[21]. The magnitude of the voltage transient is also dependent on the line impedance (R_d, L_d) and the fault location. The faulted line's capacitor discharges into the fault and the DC line voltage drops constantly. The capacitor discharge current is shown in figure 2.4b as the orange waveform. Capacitor discharge is extremely rapid as represented by the time t_{dis}. The process continues until the DC line voltage becomes smaller than the instantaneous AC voltage. Next, the system enters the grid side current feeding stage (represented as the blue waveform and by the time $t_{grid\text{-}feed}$ in figure 2.4b) [20]. In this stage, the anti-parallel diodes of the VSC are forward biased due to the higher AC side voltage. As a result, current starts flowing into the fault from the AC grid via the freewheeling diodes. The AC side current also starts charging the non-faulted DC line capacitor. The stage finishes when the voltage of the non-faulted line's capacitor increases beyond the AC voltage and the circuit attains a new steady state.

High impedance line to ground faults result in a smaller voltage transient due to a slower rate of increase of current [19]. The DC line voltage can still tend to be relatively high and limited current flows from the AC side. Nevertheless, these types of faults also pose dangers to the DC network. In an IT DC ground system high impedance faults can be difficult to detect due to the already present impedance used in grounding. The changes in current magnitude can be quite small making it extremely challenging to measure and detect a fault.

Moreover, line to line faults mainly result in a low impedance conduction path being formed between the two conductors [22]. The characteristics observed are similar to a low impedance line to ground fault. However, they can be even more fatal because a new steady state might not be achieved due to the inability of the faulted DC line capacitors being recharged via the AC grid.

Due to the low impedance of DC transmission lines, at fault occurrence a high rate of current rise is expected [23]. As a result, the line current can increase to extremely dangerous values very rapidly. This poses threats to the power electronic circuits used in the DC grid especially the semiconductor switches of the VSC. The switches are not capable of sustaining currents larger than their nominal rated values, generally beyond several microseconds [15]. As LVDC grids are expected to be used as 'last mile' distribution networks in a community, the potential dangers subsequent to fault occurrence are unacceptable. Hence, there is a need of detecting faults quickly in order to protect the DC grid, its equipment from damage and for LVDC grids to be a viable option for a community distribution network. The detection methods should preferably be able to act during the capacitor discharge time to prevent

the fault current flowing through the VSC switches [2]. Thus, action should be taken based on the transients observed after fault occurrence [17].

The DC fault characteristics discussed should form the basis of the fault detection methods. The following sections explore various applicable methods of fault detection in LVDC grids.

2.2. Unit Based Detection Methods

Fault protection of presently operating point to point HVDC systems has been implemented on the AC side [12], [24]. This type of protection usually detects faults in the order of tens of milliseconds [25]. As mentioned in the earlier section, this amount of time required by a system for fault protection is too long to be used with multi terminal LVDC networks. Alternatives such as time-inverse over current relays do offer faster fault detection and protection times however, due to the smaller anticipated operating distances of LVDC networks their co-ordination can prove to be a difficult task in a meshed DC network [2].

Compared to these conventional methods, unit based fault detection can prove to be fast acting without the need to implement complex algorithms and face system co-ordination issues. Unit based detection refers to detecting faults within a predefined specific area. In terms of a network, an area can be composed of various loads, distribution lines and feeders. Of course, it can also be defined to contain lesser number of elements. These methods can be applied in various subsections throughout the network to achieve complete fault detection capability. Unit based methods work by measuring and comparing quantities at the boundaries of the specified area that they protect [1]. To detect faults, the quantity compared is usually either the current magnitude, current flow direction or the rate of change of current. This will be explained in detail later.

The processing of the measured quantities relies heavily on communication between the sensors used in the specific unit protected area. Hence, for unit based detection communication links need to be established throughout the network, in particular between sensors located in a specified area. This could hinder the implementation of unit based fault detection, due to the additional costs related to establishing communication links, installing sensors and the potential increase in the overall size of the system [25], [1]. However, the development of smart grid concepts already have a prerequisite for including sensors and communication infrastructure. The communication system has to cover the entire smart grid network and is used mainly for control purposes to achieve better monitoring, power quality and grid operation efficiency [26]. Therefore, due to the pre-existing infrastructure, unit based fault detection methods can be implemented in smart grid applications that include LVDC distribution without incurring a significant increase in costs [25].

2.2.1. Differential Current Protection

A particular unit based detection method is known as the differential current protection. This detection method works by measuring and comparing the current magnitudes at the boundaries of the specified protection zone. The difference of the two measured current quantities is computed continuously and compared to a predefined threshold value. For a single DC transmission line, during normal operation the calculated difference will be zero or close to zero (because of current ripples due to line capacitances) as the same current flows through the line. However, if a fault occurs in the specified unit protected area then the differential current will be greater than zero. If this calculated differential current exceeds the predefined threshold, then a fault is detected by the differential current scheme.

Figure 2.5 can be used to illustrate the operation of the differential current fault detection scheme. The semiconductor switches represent the VSC and interface an LVDC grid with an AC power source. A simple LVDC line is shown which is terminated in a passive load. R and L represent the various resistances and inductance along the DC cable and C_F is the line filter capacitor.

The differential current protection measures the boundary currents labeled i_a, i_b in figure 2.5 and monitors faults by computing the differential sum of i_a, i_b [1]. The differential current sum ($\Delta i(t)$) is then simply defined as

$$\Delta i(t) = i_a(t) - i_b(t). \tag{2.1}$$

When a fault occurs, i_a is redirected via the fault path. With the DC line terminated in only a passive load, i_b is momentarily supported by the stored energy in the line inductance which de-energize quickly.

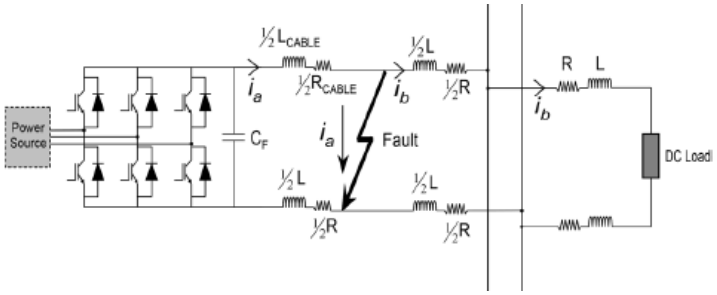


Figure 2.5: Differential current scheme with passive load connected [1]

As a result, a large $\Delta i(t)$ is measured. If the measured $\Delta i(t)$ is larger than the set threshold current (i_{TH}) such that

$$\Delta i(t) > i_{\text{TH}}, \tag{2.2}$$

then a fault is detected in the DC line by the current differential method.

For this purpose, a central processing unit is required. This processing unit works by receiving the measured current signals from the current sensors located at the boundaries of the unit protected zones. It then performs the above mentioned calculations to determine if a fault occurred and if necessary, generate and transmit fault trip signals to the relevant circuit breakers [1]. This implies that communication links between the sensors, central processor and the circuit breakers have a huge contribution to the working of the differential current protection method. Therefore, for effective operation of this fault detection method, communication must be fast, accurate and synchronized.

The principles of operation of the differential current protection method make it less vulnerable to the effects of varying fault impedance [25]. This is because regardless of the fault impedance, a particular sensor will measure a greater current than the other sensor located in the same defined unit protection zone. Hence, by adjusting the corresponding threshold value at which the differential current protection acts, susceptibility to false fault detection due to varying fault impedance can be reduced.

Moreover, this fault detection method has the potential to improve the selectivity of the DC grid. Selectivity refers to the ability of the protection system to isolate only the faulted part of the grid and let the rest of the grid operate normally. A differential current scheme can be designed to achieve high levels of selectivity. It should detect and initiate protection action only for faults occurring in the predefined unit area and be resistant to faults outside the area (external faults). For external faults, the currents measured via the sensors will normally be similar (apart from transients due to line capacitance). Therefore, $\Delta i(t)$ will be small implying an internal fault did not occur. As a result, the DC grid's selectivity improves by not tripping the circuit breakers in the unit defined protection zone. Henceforth, the differential current protection method stays true to its unit based detection principles as well.

Differential current protection can also be extended to detect faults in multi terminal DC grids. They have a similar working methodology. An example of the implementation of differential current protection in multi terminal DC grids for medium voltages is explained in [2]. The multi terminal grid is divided into several zones, with each zone described as a sub-microgrid (SMG). The boundaries of each SMG are defined by the VSCs used as connection points for various distributed energy sources and loads.

In [2], a two level differential current protection is implemented. The first level is an implementation of the method in a more familiar manner, where the differential current sum is computed of each distribution line. The second level implements the differential current protection on a multi terminal level. It first calculates the current sum at the terminal boundaries of the SMG and then computes the differential current sum. Equation (3) below illustrates the calculation of the differential current sum of an SMG

$$\Delta i(t) = I_{\text{SMG}}(t) - \sum_{i=1}^{n-1} I_i(t). \tag{2.3}$$

The SMG current is represented by I_{SMG}, n depicts the number of boundaries of the SMG and I_{i} the current at each boundary. The two level differential current protection can help in strengthening the

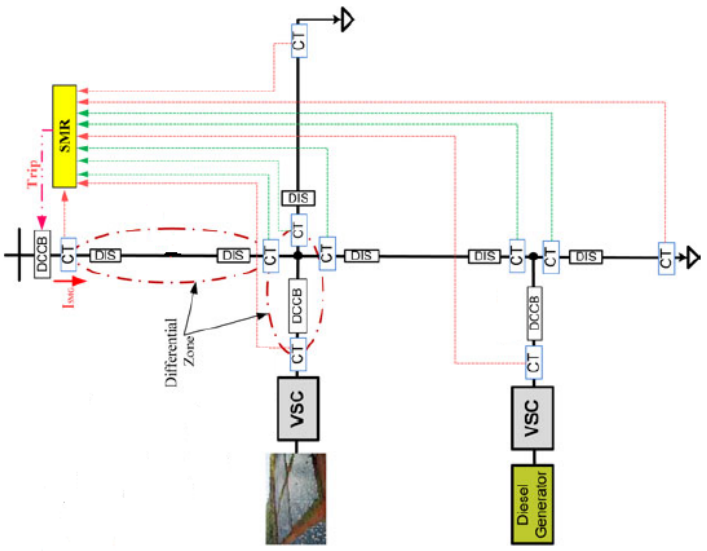


Figure 2.6: Implementation of two level differential current protection [2]

overall ability to detect faults. An example of this method is shown in figure 2.6. The current sensors (CT) transmit their measurements to the central processor represented by the SMR block. The SMR controls the operation of the various circuit breakers (DCCB) and the DC line isolators (DIS).

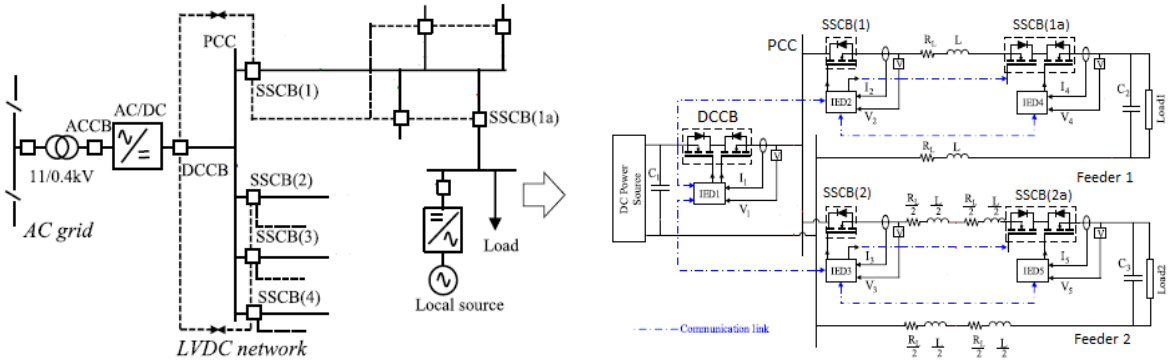
In figure 2.6, the green arrows represent the communication links used by the CTs for each differential zone's fault detection (first level protection) while the red arrow communication links administer the multi terminal differential current protection (second level). Therefore, in the event of fault detection, a trip signal can be generated by either level of the implemented differential current protection [2]. Although, in this way a higher number of sensors, protective devices and communication links are required, the overall fault detection capability of the differential current protection method is improved substantially.

Furthermore, there is always a possibility of sensor and communication failure. This has repercussions on the conventional differential current protection resulting in the entire mechanism being disabled. A solution proposed by Tzelepis et al. in [27], is to use several current sensors along the distribution line. Then several differential current sums are calculated according to the measurements of two consecutive sensors. Hence, even if a sensor or its communication link malfunctions, the system can still operate with a reduced number of sensors.

Additionally, the conventional differential current protection is vulnerable to false fault detections particularly due to large current transients as a result of inrush current or cable capacitance discharge due to an external fault. According to [27], the vulnerability can be decreased by also measuring the rate of change of current based on the sensor's readings. If $\Delta i(t)$ surpasses the initial threshold, it proposes to calculate the rate of change of current $(\frac{di_S}{dt}, \frac{di_{(S+1)}}{dt})$ of the two consecutive sensors that surpassed the initial threshold. If these derivatives also exceed a threshold then it can be concluded with confidence that indeed a fault has been detected. Generally, the reliability and stability of differential current protection can be improved with more sensing technology albeit at the expense of increased data processing and capital costs.

2.2.2. DC Current Direction Flow Method

Another unit based fault detection method is to sense the DC current direction flow in several zones of the LVDC distribution grid. An LVDC grid is expected to easily integrate distributed energy sources [12]. However, if a fault occurs, the fault will be supplied by both the main AC grid and the distributed sources. To feed the fault, there is a possibility that the current direction of the distributed sources is reversed. Hence, detecting changes in the current direction flow in the grid lines forms the basis of this fault detection method. The operation relies on local measurements and exchange of the measured data between sensors in different zones via communication channels. Due to an alternate working principle, this method also provides the possibility of precisely determining the fault location in addition



(a) Line diagram (b) Circuit schematic

Figure 2.7: LVDC distribution grid model [3]

to detection.

The working methodology stems from measuring the DC line's voltage, current magnitude and the current direction [10]. The signals are measured by electronic devices installed in the DC distribution lines. In [10], these devices are termed intelligent electronic devices (IED) and form the basis of the entire fault detection and protection mechanism. An IED consists of sensors, communication functionality, has the ability of data processing and generating output signals. Fault detection occurs by various IEDs communicating amongst each other and exchanging the measured signals [10]. Subsequently, each IED runs a protection algorithm that determines both fault detection and location. Next, if a fault is detected the IED itself initiates the protection action by opening the relevant circuit breakers. For quick fault protection times, the use of SSCBs is ideal.

IEDs continuously monitor the current and voltage magnitudes at the installed locations. The first step in detecting DC grid faults is to sense changes in these magnitudes. Transient changes in the voltage and current magnitudes are usually due to a fault or large changes in the load. Therefore, if changes detected by the IEDs in the voltage, current magnitudes surpass predetermined thresholds, then the current direction flow algorithm is initiated [3]. This algorithm determines if the threshold was exceeded due to fault occurrence and if applicable, confirms the detection of a fault.

Figure 2.7 can be used to explain the working of the current direction flow algorithm. Figure 2.7a shows a line diagram of a last mile distribution LVDC grid. Last mile distribution refers to power distribution to the end users (mostly households) in a small community. The square figures represent the SSCBs. The IEDs are also installed at these locations in order to measure local signals near the SSCB and initiate quick protection action. The LVDC network is represented by the solid lines while the dashed lines show the communication links between the IEDs. The line diagram shows several DC feeders with a main circuit breaker ($SSCB_1$, $SSCB_2$...) and distribution branches with their own circuit breakers ($SSCB_{1a}$) located 'downstream'. Figure 2.7b shows a detailed grid schematic with the the working of the IEDs and the SSCBs realized with MOSFETs. Moreover, the DC feeder's IED communicates only with the downstream IEDs and the 'upstream' DCCB. Hence, data exchange is done in a coordinated manner.

The algorithm assumes that currents flowing downstream are 'positive' and upstream are 'negative' [10]. The IED represents these directions as '1' and '0' respectively. First, the current direction of the upstream IEDs is checked. If the main DCCB reports a '1' and the main feeder IEDs report a '0', then the fault is immediately detected to be on the point of common coupling (PCC). The IEDs instruct the appropriate SSCBs to initiate protection. However, if the main IEDs also report a '1', then a fault is detected downstream on a DC line feeder. Now, the main IED of the DC feeder communicates with the downstream IEDs. If all the downstream IEDs feedback a '0', then a fault is detected on the main DC line feeder [3]. Similarly if the downstream IEDs feedback a '1', then the fault is detected to be at the end user's side at which the initial current, voltage magnitude thresholds were surpassed. As a result, the IED at the extreme end will be responsible to clear the fault. Accordingly, it is deemed that indeed a fault was detected along with a reasonable estimate on the location of occurrence.

The nature of operation ensures that high resistance faults can also be detected. Therefore, the capability of this method to detect faults is high. Furthermore, this method relies on excessive commu-

nication between the IEDs for fault detection confirmation. This increases the possibility of communication delays and errors. To mitigate this, it is suggested that the IEDs utilize the communication links only when the measured voltage magnitudes exceed the initial threshold [10]. Moreover, unlike the differential current protection method a central processor is not required. The various IEDs themselves execute the current direction flow algorithm and protection. This promises to further reduce communication delays. Due to the high selectivity offered, the unit based detection principles are also preserved by this method. This is demonstrated by the fact that only the relevant circuit breakers act to isolate a fault detected in the unit defined zone.

Although unit based fault detection can provide good selectivity, their reliance on communication can be problematic in fault detection in DC grids. As mentioned previously, the low impedance of DC grids usually causes high transients to be experienced after fault occurrence. For the safety of the DC grid and its auxiliary equipment, fault protection must be based on detecting these rapid transients [17]. For this to be achieved in a DC grid network the communication system faces extreme challenges and is susceptible to errors.

A significant challenge in using communication is to ensure that the various sensor measurements are synchronized in time [25]. As the sensors are physically situated at a distance from each other, there measurements can have a signal propagation time delay between them. This will cause the sensor measurements to be unsynchronized in real time. In the event of a fault, due to the extremely high expected $\frac{di}{dt}$ values the unsynchronized measurements will adversely affect the execution of optimum fault protection. Moreover, the high discharge rate of line capacitances also contributes to synchronization errors [28]. Their discharge current cannot be controlled and adds more uncertainty to the fault protection execution.

However, the most stringent requirement in LVDC fault protection is the fault detection time. Unfortunately, the time delays associated with communication and further additional processing of data in unit based detection methods make it difficult to fulfill this requirement [24]. Tzelepis et. al. report that using differential current protection, for a fault distance of 1km the detection and protection initiation time is 1.3ms [27]. Most of this time is used in communication between the sensors and the central processing unit. This amount of time is acceptable for HVDC applications but not necessarily for LVDC networks. Additionally, Fletcher et. al. use the differential current protection method, to experimentally report impressive protection initiation times of up to 41μs. However, the experiment was a scaled down version conducted at 20V with the fault simulated at a distance of only 20m. In a practical setting of an LVDC distribution network, the operating distances will be much higher. As a result, the communication delay times will become longer and the chances of disturbances in communication will also increase. This will make it difficult to isolate high current faults within a safe operating time range.

The main application of LVDC grids is to be used as a distribution network in communities to provide power to end users. This setup helps in potentially realizing the advantages of DC technology. Due to the size of the application, cost becomes an important factor. Installing communication links for a small scale distribution network will significantly ramp up the initial costs of the system [25]. As a result, from an economic point of view the use of unit based methods with extensive communication does not seem as a viable alternative for fault detection [29].

2.3. Non-unit Based Detection Methods

Non-unit based methods provide another alternative for detecting faults. Similar to unit based methods, they also protect specific sections of the distribution network from faults. However, contrary to unit based methods, non-unit based fault detection methods do not have defined boundaries of the areas in which they operate. This essentially means that there can be an overlap in the areas of operation between several non-unit based detection systems installed in different sections of the network.

The methods rely only on local measurements to detect faults [24]. The circuit breakers initiate protection action purely based on the locally measured signals. Hence, there is no need for communication between sensors located in different areas. As a result, non-unit based detection methods operate independent of any sort of communication. This makes them free of the limitations associated with communication links as highlighted in the previous section. As no communication delays are expected, they have the potential to offer faster protection against faults occurring in a distribution network [8]. Hence, implementing non-unit based fault detection methods becomes an attractive option for LVDC distribution networks.

As these methods do not function within fixed boundaries, there is a concern of false fault detections in a different section of the network. This can cause multiple circuit breakers to act resulting in the isolation of a larger than necessary part of the grid. The various non-unit based detection methods discussed in detail ahead will show how to minimize spurious fault detections in the other parts of the network.

As explained earlier in the report, fault currents can increase extremely rapidly in DC grids. Some factors that affect the rate of rise are the operating voltage level, line impedance, fault impedance and location. To put this in perspective, fault current rise of up to 10kA/ms is possible in HVDC grids working at 800kV [29]. Even though LVDC networks will operate at much smaller voltage levels, their line impedance are expected to be significantly lower than HVDC grids due to smaller operating distances. Therefore, high fault current gradients will also be experienced in LVDC networks. In fact, Emhemed and Buurt in [10], report that LVDC fault currents can have an increasing rate of 4-5kA/ms. As circuit breakers have ratings of maximum current and operating times, the consequences are that non-unit based detection technology cannot react to such high current rise rates in adequate time [8]. As a result, it is necessary to limit the current rise after fault occurrence to ensure detection circuits and protection (via circuit breakers) can function appropriately.

2.3.1. Fault Detection Using Fully Controllable Converters

A particular approach for this is to use fully controllable power converters to interface the AC grid and the DC network. These converters possess the capability to control the amount of current flowing through them. Hence, in the event of a fault on a DC line, the converter can actively restrict the current flow (and rate of increase) in to the fault and allow the circuit breakers on the DC line to isolate the fault . However, the current is restricted to values that are only slightly larger than the nominal rated values [30]. The limited rise of current minimizes the transients observed. This makes fault detection via non-unit based methods extremely challenging.

Nevertheless, a fault detection method in medium voltage DC grids using fully controllable converters has been explained in [30]. It relies on mechanical contactors instead of circuit breakers. The method is based on calculating the equivalent resistance at the converter output terminals by monitoring the voltage and line current. When a fault occurs, the line current increases causing the instantaneous resistance to decrease. If the resistance decreases beyond a threshold value, a fault is detected. Consequently, the converter's control system initiates action to limit the current at a specified value. Due to this, the calculated equivalent resistance starts to increase. There is a time delay until the resistance increases beyond a certain threshold. Moreover, in order to isolate the fault safely using mechanical contactors, the current has to fall below a specified value. Hence, the system must wait longer before the fault can be isolated. This method mentions fault isolation times of at least 20ms [30]. Even though the current is limited after fault occurrence, this time is regarded as too slow considering the fact that SSCBs possess the capability of operating in the range of several microseconds.

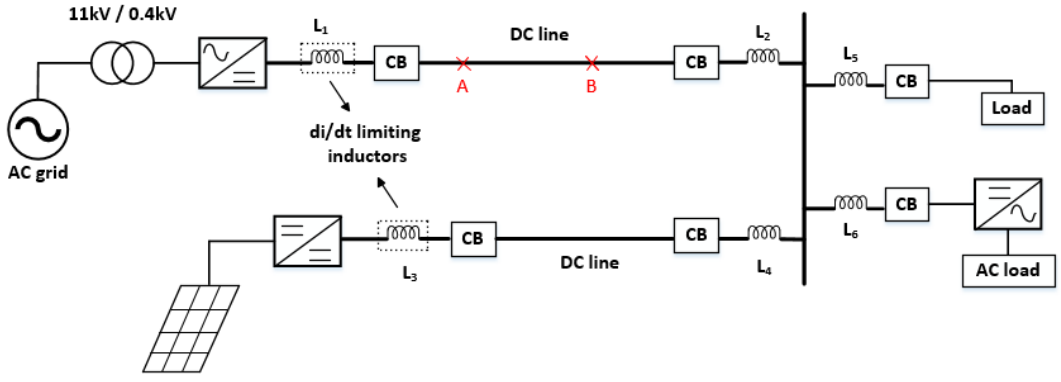


Figure 2.8: Single line diagram of a LVDC grid with $\frac{di}{dt}$ limiting inductors

2.3.2. Detection Methods Using $\frac{di}{dt}$ Limiting Inductors

An alternate method to limit the rate of increase of the line current is to add DC reactors at the endpoints of the DC grid lines [31]. Externally added inductors in the grid lines are mostly used as the DC reactors. Therefore, the inherent property of inductors to restrict sudden changes in current is utilized. Larger inductors limit the current increase more and hence, provide circuit breakers more time to properly protect the grid from faults. Moreover, in the event of a fault, transient voltages appear across the inductors. As a result, measurements across the externally added inductors can also be used as a means of non-unit based fault detection [31], [32]. The following discussion elaborates on various methods of fault detection via the current rise rate limiting inductors.

Figure 2.8 shows a schematic of a LVDC grid with added current limiting inductors. The loads are supplied power by the AC grid and a local distributed energy source (example a solar farm). Power electronic converters (AC-DC, DC-DC) that interface these sources to the DC network are also shown in the figure. The DC lines transmit power from these sources to the loads. If a fault occurs on a DC line, detection is achieved via the inductors which results in the action of the appropriate circuit breakers (represented by CB). Solid state circuit breakers will be used for fast interruption of the fault, subsequent to detection. Various inductors and circuit breakers are added to ensure that faults can be detected and isolated in the entire DC network.

In addition, when a fault occurs on a DC line the entire line segment should be isolated. Otherwise the fault current will be supplied by the other sources in the network. To accomplish this without adding communication links in the DC network, the fault must be detected at each end of the particular line [33]. This is done by adding another $\frac{di}{dt}$ limiting inductor and a circuit breaker at the other end of the line. However, in the network of figure 2.8 this is not necessary for the lines directly connected to the loads because of the assumed absence of energy sources at the locations. In this way, the entire network does not need to be de-energized and the loads can still be powered by the alternate source.

A particular fault detection method predicated on the $\frac{di}{dt}$ limiting inductors is known as the 'rate of change of voltage (ROCOV)' method [8]. This method relies on measuring the line side voltage of the associated $\frac{di}{dt}$ limiting inductor and computing its derivative as a function of time. When a fault occurs, a rapid decrease in the line voltage is observed at the fault location. Hence, the derivative of the line voltage has a steep rise from almost zero to a large value. The ROCOV method measures this change for the purpose of quick fault detection. In fact, this method can identify a fault condition within microseconds [8], [24].

As the fault location distance from the inductor increases, the measured voltage derivative steadily decreases. This is due to the larger impedance between the fault location and the measurement point. As a result, the ROCOV calculation has a smaller magnitude. In figure 2.8, a fault at location A will result in a higher ROCOV magnitude than a fault at B (assuming similar fault impedance) when measured at L_1. To ensure fault detection along a specific DC line, an appropriate threshold has to be established. The threshold can be determined via trial and error. The threshold of a specific DC line is set such that it is lower than the minimum observed ROCOV magnitude for a fault on the line and higher than the maximum ROCOV magnitude for an external fault. Therefore, by setting a suitable threshold the selectivity of this method is also improved.

Although this method provides a fast technique of detecting faults, it relies on an assumption that the converter side voltage remains constant after fault occurrence. Unfortunately, this is inaccurate and becomes invalid due to the rapid discharge of the line capacitors into the fault. This can result in false fault detections leading to unnecessary tripping of circuit breakers in the unaffected parts of the network. Furthermore, this method has been proposed to be used for multiterminal HVDC grids operating at 320kV using inductors of 100-200mH [8]. Substantially large inductor values are necessary in HVDC grids to provide impedance to sufficiently limit the fault current rise. These inductors store huge amounts of energy that is dissipated in surge arresters after the circuit breaker is opened [34]. However, these inductor values cannot be used at all in LVDC applications. This is because the proposed solid state circuit breakers protection via common snubber circuits would be unable to dissipate the extremely large amount of stored energy. Hence, there is a need to significantly scale down the $\frac{di}{dt}$ limiting inductor values for this fault detection method to be applicable in a LVDC network.

Another technique of utilizing the $\frac{di}{dt}$ limiting inductors for fault detection is to directly measure the voltage across the inductor. During normal operation, the voltage across the inductor is near zero due

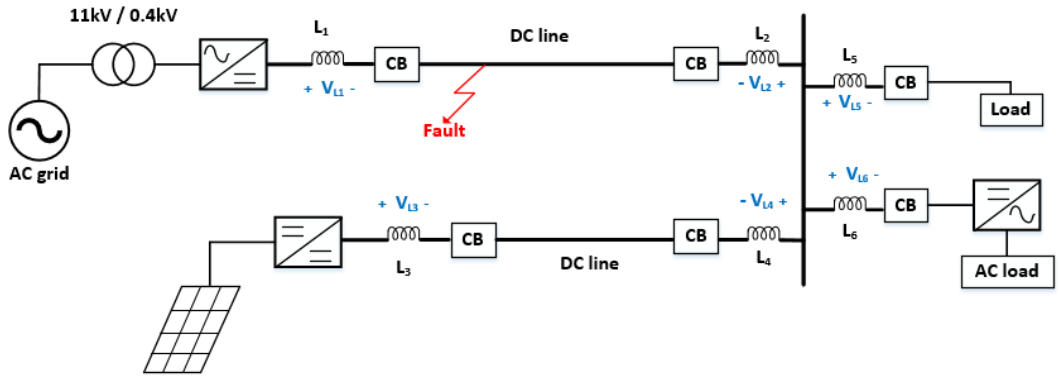


Figure 2.9: Fault detection V_L measurement across the $\frac{di}{dt}$ limiting inductors

to mostly DC current flowing in the transmission lines [28]. After fault occurrence, a significant dip in the line voltage is immediately observed at the fault location [35]. This imposes a brief transient voltage across the $\frac{di}{dt}$ limiting inductor. This immediate transient is expected to be much higher across an inductor situated on the faulted line than across an inductor located on a healthy line in the DC network [32].

Figure 2.9 is a redrawn version of figure 2.8 exhibiting a fault and the voltage measurements (V_L) across the inductors (in blue) that form the basis of this fault detection method. In this case, V_{L1} would have the largest transient magnitude (due to close vicinity) followed by V_{L2} and the other V_L measurements. As opposed to the ROCOV method, the voltage is measured across the inductor instead of on just the line side. Hence, there is no need to assume that the converter side voltage will remain constant after fault occurrence. Additionally, as this method measures only the change of voltage across the inductor (instead of the rate), it promises to detect faults even faster than the ROCOV method explained earlier.

The voltage across an inductor (V_L) is given by the simple equation below

$$V_L = L\frac{di}{dt} \tag{2.4}$$

Therefore, measuring V_L is essentially equivalent to the measurement of the rate of change of current ($\frac{di}{dt}$) in the DC line. As faults in DC lines usually have high $\frac{di}{dt}$ rates, measuring V_L gives an early indication of the occurrence of a fault without the current increasing to dangerously large values.

Fault detection based on the inductor voltage is a promising method for use in LVDC grids particularly due to its speed of operation [32]. When a fault occurs, the time constant (τ) of the induced transient voltage is

$$\tau = \frac{L}{R} \tag{2.5}$$

where L and R are the inductance and the resistance of a particular DC grid line. Due to the recommendation of using smaller inductors in LVDC applications with SSCBs, at fault instance, the voltage induced across the inductor exists for a short duration. Hence, this creates a challenge of detecting this ephemeral voltage. As a result, for this method to be adopted for fault detection purposes, fast detection circuits capable of measuring the ephemeral voltages will have to be designed.

Furthermore, Li et al. in [35] report an alternative fault detection method based on the $\frac{di}{dt}$ limiting inductor voltage. This method detects faults by monitoring the change rate in the inductor voltage. The previously mentioned method detects faults by only measuring the inductor voltage. This method goes a step beyond by calculating the rate of change in the inductor voltage as well. Moreover, it is different from the ROCOV detection technique because it computes the rate of voltage change directly across the inductor instead of just the DC line side voltage.

To calculate the change rate of the inductor voltage, two voltage thresholds are defined; the initial threshold ($V_{LT\text{-}t1}$) and the protection threshold ($V_{LT\text{-}t2}$) [35]. These thresholds correspond to the inductor voltage. As explained earlier, when a fault occurs the voltage across the inductor rises rapidly. This

method detects faults by calculating the time taken for the inductor voltage to increase from $V_{LT\text{-}t1}$ to $V_{LT\text{-}t2}$. The working methodology can be explained using figure 2.9. After fault occurrence, the inductor voltages (V_L) rise. If a certain V_L in the DC network increases beyond $V_{LT\text{-}t1}$, a time measurement is initiated. If V_L also increases beyond the next threshold, $V_{LT\text{-}t2}$, the time measurement is stopped. The recorded time (Δt) is compared with a predefined threshold. If Δt is smaller, then a fault has been detected as a result of the rapid rise of the voltage across the inductor.

Hence, the time taken for the inductor voltage to change from $V_{LT\text{-}t1}$ to $V_{LT\text{-}t2}$ is measured. It is equivalent to measuring the second derivative of the DC line current. This is shown in the equation below

$$\frac{V_{\text{LT-t2}} - V_{\text{LT-t1}}}{\Delta t} = \frac{\Delta V_{\text{L}}}{\Delta t} = \frac{dV_{\text{L}}}{dt} = L\frac{d^2 i}{dt^2} \tag{2.6}$$

Moreover, a condition is applied on Δt. This condition states that Δt has to be larger than a minimum defined time for a disturbance in the network to be identified as a fault. This helps in distinguishing actual faults from transient disturbances such as large fluctuations in the load. Consequently, the robustness of the fault detection procedure increases by decreasing possible false triggers and spurious fault detections.

Some results of the detection procedure are available for an HVDC multiterminal grid operating at 480kV in [35]. In this particular example, the initital and protection thresholds are set at 5kV and 10kV respectively. After fault occurrence, $V_{LT\text{-}t1}$ is surpassed at 510μs and $V_{LT\text{-}t2}$ at 560μs [35]. Hence, Δt is 50μs. The time threshold is set at 180μs, ensuring fault detection. This shows that the fault detection procedure is quite fast. Furthermore, there is a possibility of using this method in LVDC networks by scaling down the inductor voltage and time thresholds. Accordingly, Δt will also be reduced. However, the problem is that this detection technique has some idle time, in terms of waiting for V_L to surpass the first initial threshold ($V_{LT\text{-}t1}$) after a fault has occurred. In the example above, the idle time is 510μs. In an LVDC network with SSCBs, it is desirable to implement fault protection as quickly as possible. Although this method is more robust, due to its nature of operation it will take longer to detect a fault than the technique of simply measuring the change in the inductor voltage. It also requires a processor to operate at a high sampling frequency at each location of the local $\frac{di}{dt}$ limiting inductor to quickly calculate the change rate of the inductor voltage [32].

In addition, another technique explained by Liu et al. in [28], utilizes the impedance of the $\frac{di}{dt}$ limiting inductors for fault detection purposes in a multiterminal HVDC network. The inductor can be considered as an electrical boundary, exhibiting a high impedance path for higher frequency components. The fast transient observed after fault occurrence consists of several frequencies. As a result, the inductor will attenuate the magnitude of higher transient frequency signals by a much larger extent than of the lower frequency signals. Hence, measuring the voltage magnitudes at the ends of a $\frac{di}{dt}$ limiting inductor forms the basis of this fault detection method.

This technique first defines a frequency range within which to measure the observed transient signals. Next, the magnitude of the voltage signals of the observed transient (after fault occurrence) corresponding to this frequency range are measured. The voltage measurements are done at both sides of the $\frac{di}{dt}$ limiting inductor; the line side and the converter side. Using this information, a transient voltage ratio is computed between the line side voltage and the converter side voltage [28]. The transient voltage ratio (K) is used as a marker to determine if a fault occurred in the DC network and can be simply defined as

$$K = \frac{V_{\text{TL}}(f)}{V_{\text{TC}}(f)} \tag{2.7}$$

where V_{TL}(f) and V_{TC}(f) represent the measured line side and the converter side voltage magnitudes within the specified frequency range. In figure 2.9, when a fault occurs at the specified location, the line side voltage magnitude of V_{L1} and V_{L2} will be smaller than the magnitudes measured at the opposite ends of the respective inductor. However, for the other inductors located on unfaulted transmission lines in the network, the line side and converter magnitudes will be relatively equal. This is because of a smaller transient across these inductors. As a result, the calculated ratio will be close to unity for unfaulted lines and less than unity on the faulted line. Hence, in this manner a fault can be identified in the network via this technique.

A precondition for this fault detection technique is to have high impedances at the boundaries of the transmission lines. In a DC system, this can be achieved with large inductors. However, their use is not feasible in an LVDC network. Moreover, the possibility of using smaller inductors specifically for LVDC applications could lead to inadequate performances. This is because the low inductances might not provide enough impedance between the line side and the converter side. A possible solution can be to shift the frequency range in which the transient signals are measured to a higher spectrum. However, this would require a processor to operate at an even higher sampling frequency and be extremely accurate. This could be expensive to implement in various local locations throughout the LVDC network. Large load fluctuation transients could also increase the number of false detections due to the higher frequency range spectrum.

2.3.3. Fault Detection via Measurements Across the Solid State Circuit Breaker

This report proposes to use SSCBs as the circuit breakers for fault isolation in LVDC networks. This is essentially due to their capability of fast operation, typically within several microseconds [10]. SSCBs are comprised of semiconductor switches, usually MOSFETs or IGBTs. Therefore, an additional fault detection technique is achievable based on the semiconductor components (MOSFET or IGBT) of the SSCB. This method functions via the online measurement of relevant signals across the SSCB components. Online measurement refers to simultaneously conduct measurements across a device while it is in operation. These measurements are mostly used in condition monitoring of the semiconductor devices used in power electronic applications [36]. Condition monitoring is useful in tracking the ageing of the devices as a result of systematic use. This helps in reducing failures by scheduling system maintenance ahead of time. For this purpose, either the junction temperature (T_{junc}), drain to source resistance (R_{DS}) of a MOSFET or the on-state voltage (V_{CE}) of an IGBT are monitored [36], [37]. Hence, the basis of the condition monitoring technique can be adopted for fault detection purposes in the LVDC transmission lines using SSCBs [38].

This detection method works by directly measuring the voltage across the SSCB device. When a MOSFET/IGBT is conducting, the voltage across it is directly proportional to the current flowing through the device's channel. This is because in their on-states a MOSFET can be considered as a resistor while an IGBT can be modelled as a constant voltage drop in series with an on-state resistance [38]. The equations (2.8) and (2.9) below illustrate this for a MOSFET and an IGBT respectively.

$$V_{DS} = I_{DS} R_{DS}, \tag{2.8}$$

$$V_{CE} = V_J + I_C R_{on}, \tag{2.9}$$

where V_{DS} is the MOSFET's drain to source voltage, V_J is the junction on-state voltage of an IGBT, R_{on} is the IGBT's on-state resistance, I_{DS} and I_C are the channel currents of the MOSFET and IGBT respectively. Hence, voltage measurement across the SSCB device can provide a direct indication about the magnitude of the current flowing in the line. Moreover, as SSCBs already have (albeit low) on-state power losses, this method can acquire information about the line current without the need of adding extra current sensors in the distribution lines. As a result, there are no additional power losses in the LVDC network due to the measurement equipment.

This type of solution already exists and is known as desaturation protection. However, there are some challenges associated with its implementation for fault detection purposes in LVDC networks. For its operation, the desaturation protection requires a relatively large voltage to build up across the SSCB device, typically 6-7 V [39]. As modern semiconductor switches have low channel resistances (R_{DS} and R_{on}), this will require extremely large currents to flow for the device voltage to reach the desaturation protection threshold. Due to the low current withstanding capability, the SSCB devices are at a risk of being destroyed even before the threshold can be achieved.

The online measurement of the device voltage (V_{DS} or V_{CE}) will exhibit variations in real time. According to (2.8) or (2.9), the measured voltage can be processed to accurately represent the current. An increase in the voltage will indicate a larger current flowing through the SSCB and thus, the particular transmission line. Therefore, appropriate thresholds can be set to determine fault occurrence in the particular line based on the line current calculations via the measured SSCB device voltages.

2.4. Existing Challenges in Fast Fault Detection for LVDC Networks

The admissible methods of DC fault detection discussed earlier also highlighted some limitations particularly for LVDC networks. These limitations can hinder the fast detection and isolation of faults in the LVDC network. As a result, the limitations can be considered as current existing challenges that require solutions in order to implement fast fault detection. The major challenges in fast fault detection in LVDC networks are elaborated ahead.

In the above literature, the fault detection schemes proposed specifically for LVDC systems (differential protection, current direction monitoring) relied on communication links for their operation. Although these methods exhibited their ability to detect the faulted lines in the grid, they are just too time consuming because of the added communication delays. Fault detection and protection times of between 1-2 ms have been reported for LVDC systems relying on communication [10], [3]. In fact, the bulk of this time is due to the associated communication delays between the sensors and the processing unit [27]. In hindsight, this is still quite fast compared to the traditional protection systems used in AC distribution networks. However, for LVDC networks that incorporate power electronic converters with sensitive semiconductor components, fault detection within microseconds is necessary. By employing detection methods that can operate without communication, the possibility of fault detection within the required time frame is achievable.

Moreover, some alternate solutions to avoid the use of communication for fault detection purposes were based on including $\frac{di}{dt}$ rise limiting inductors in the distribution lines. These detection techniques were mostly reported for HVDC applications. As a result, they incorporate larger inductor values (100-200 mH) to sufficiently limit the current rise after fault occurrence. Unfortunately, these values are not feasible for use in LVDC systems with SSCBs. Larger inductors can store considerable amounts of energy that must be dissipated across the circuit breakers when a faulted distribution line is isolated. As the SSCB snubber circuits can dissipate only limited amounts of energy, large inductors can potentially cause the SSCB to malfunction or even be destroyed. Therefore, it is necessary to scale down the size of the $\frac{di}{dt}$ limiting inductors to utilize the detection techniques in LVDC networks. However, extremely small inductors might not be capable of sufficiently limiting the $\frac{di}{dt}$ rise rates because of their low impedance. This can lead to the possibility of delayed (or even no) fault detections, which can cause fatal damages in the LVDC network, as a repercussion of the huge fault line currents. Hence, a challenge exists in selecting an appropriate range of permissible values for the $\frac{di}{dt}$ limiting inductors to be utilized in a fault detection technique for an LVDC network.

To reap the benefits of fast fault detection, a fault in the network should also be isolated as quickly as possible. For this purpose, the use of SSCBs as the circuit breakers in the LVDC network has been selected in this research work. At present, there is limited published knowledge regarding fault isolation and system protection particularly for LVDC networks using SSCBs. Therefore, an exciting opportunity is at hand to implement fast isolation via SSCBs subsequent to fault detection. Unlike AC circuit breakers, SSCB products are not available off the shelf. Therefore, designing an SSCB prototype integrated with fast fault detection forms another compelling challenge.

2.5. Summary

This chapter presented a literature review of the admissible fault detection methods for LVDC networks. The methods were categorized as unit based or non-unit based. Unit based methods were dependent on communication while non-unit methods detected faults without using communication. Techniques capable of working without communication proved to detect faults much faster. These mainly relied on adding $\frac{di}{dt}$ limiting inductors in the DC distribution lines. Figure 2.10 below shows a detection tree summarizing the various fault detection methods. Moreover, some obstacles hindering the fast detection were also highlighted and their potential solutions discussed.

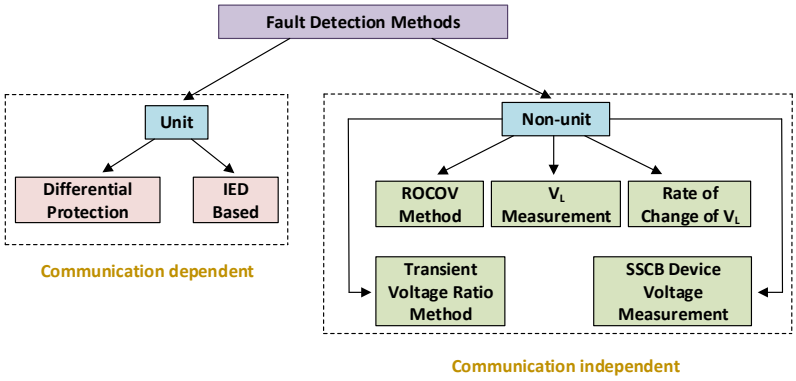


Figure 2.10: Tree showing the applicable fault detection methods in LVDC networks

3

Design of the Fault Detection Circuits

"Engineering is the art of compromise."

- Paul Horowitz, Winfield Hill, *The Art of Electronics*

This chapter provides details about the design of the fault detection circuits. In the first section, the most appropriate fault detection methods for LVDC networks are first identified. This is followed by the circuit design of the selected fault detection methods in the subsequent sections.

3.1. Suitable Fault Detection Methods

The primary requirements of the fault detection procedure are its accuracy and speed of operation. As mentioned in the previous chapter, the detection speed is vital due to the extremely fast rise of currents expected in the faulted distribution lines. Therefore, the most fitting solution for implementing a fault detection technique is the one that can operate the quickest while minimizing false detections.

As a result, the non-unit based method reliant on the voltage (V_L) across the externally added $\frac{di}{dt}$ limiting inductors is selected. As shown in equation (2.4), this particular detection method is fast in operation because the measured quantity (V_L) is directly proportional to the rate of change of current ($\frac{di}{dt}$) observed in the distribution lines. Additionally, this method does not require complex computations unlike the other fault detection techniques dependent on the $\frac{di}{dt}$ limiting inductors. Hence, the implementation is also straightforward. In terms of accuracy of this method, higher V_L magnitudes are expected to be observed across the faulted distribution line's inductors than across the unfaulted distribution lines [32]. Accordingly, appropriate thresholds can be set that enable the faulted distribution lines to be discriminated easily.

Although fault identification via measuring V_L promises to be a rapid method, there are still possibilities of a fault in the distribution lines remaining undetected. This mostly occurs if a high resistance fault occurs such that the line current magnitude only slightly exceeds beyond the nominal rated value. Moreover, a fault can also remain undetected if its location is farther away from the $\frac{di}{dt}$ limiting inductor, specifically near the middle of a longer DC distribution line. This is because the parasitic line inductance can be significantly larger than the $\frac{di}{dt}$ limiting inductor. These scenarios result in a smaller observed magnitude of the V_L transient across the $\frac{di}{dt}$ limiting inductor. Consequently, this causes detection of the fault to become uncertain.

Therefore to prevent uncertainty and maximize the capability of detecting faults in the network, this research work proposes to also use the voltage measurement across the SSCB devices for the purpose of fault detection. This method will work simultaneously with the detection technique based on the V_L measurement. It can prove to be an effective detection method since the voltage across the SSCB semiconductor devices (either MOSFET or IGBT) is directly proportional to their channel current. Hence, the faults that seem to be difficult to detect via the V_L measurement across the $\frac{di}{dt}$ limiting inductors can be identified using the SSCB device voltage. In this way, fault detection is triggered essentially due to the faulted distribution line's current increasing beyond nominal values.

The outputs of the detection circuits of both the techniques used will be interfaced together. The tripping signal of the SSCB is controlled via the detection circuit outputs. For fast fault isolation and network protection, whichever technique detects a fault first should activate the trip signal to the SSCB. Therefore, each detection method individually possess the capability to trip the SSCB in the event of a fault being identified on the relevant distribution lines.

Ideally, the V_L detection technique should be used for extremely fast fault detection and protection. This typically refers to low resistance faults or faults occurring in close vicinity of the $\frac{di}{dt}$ limiting inductor. Relatively high resistance faults, if undetected by the V_L detection technique can be identified by the SSCB device voltage measurement. A drawback of the SSCB voltage measurement method is that to detect a fault, it has to wait for the line current flowing through the SSCB devices to increase beyond the nominal rated value [40]. This can particularly be dangerous for the SSCB's semiconductor components because the amount of stress that they have to tolerate increases [35]. However, it is expected that for higher resistive faults the current levels will not become larger than twice the rated value (2 p.u.) of the distribution lines [19], [32]. The semiconductor devices of the SSCB are able to withstand currents larger than the nominal rated values for a few tens of microseconds [15]. As a result, fault detection based on after the line current has increased beyond the nominal rated value of the SSCB devices should not be problematic. This is due to the capability of the SSCBs to trip remarkably fast, within a few microseconds or even less [15].

3.2. Circuit Design of the V_L Detection Method

Due to the low impedances of the DC distribution lines, a fault incident can be expected to result in high $\frac{di}{dt}$ rates and subsequently a significant V_L magnitude across the externally added inductor should be observed. In order to design an appropriate detection circuit, the complete characteristics of the voltage V_L observed after fault occurrence need to be understood.

Is the rate of change of current in a specific distribution line the only factor affecting the observed magnitude of V_L? Are there other factors that also determine the magnitude? Moreover, what is the expected waveform and duration of the V_L transient voltage. These are critical details that need to be considered before a circuit capable of measuring V_L can be designed. The following section provides answers to these important questions by theoretically analyzing the events after a fault has occurred.

3.2.1. Theoretical Evaluation

During normal operation, the LVDC network operates in a steady state and mostly DC current flows through the lines. Hence, the V_L magnitude is zero. However, immediately after a fault the steady state operation is disturbed leading to transients occurring in the distribution lines of the network. To determine the characteristics of V_L immediately after fault occurrence, the initial effects of the line capacitance can be neglected. This results in a simplified first order equivalent model of the faulted

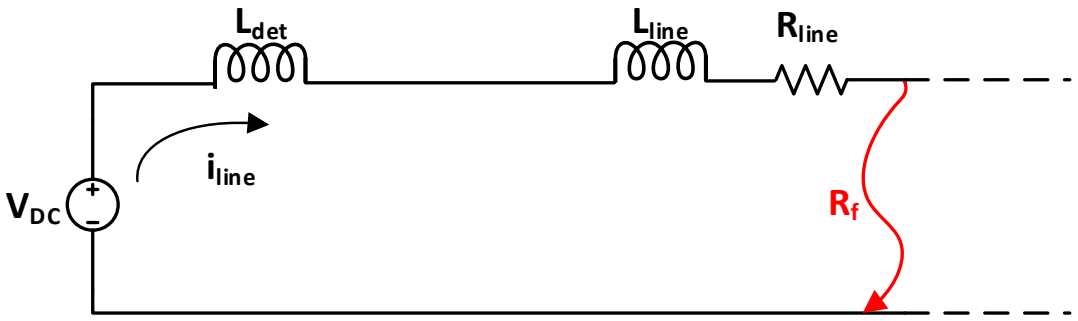


Figure 3.1: Line diagram of a DC distribution line immediately after a fault

distribution line as depicted in figure 3.1. V_{DC} can represent the output voltage of a VSC or a distributed energy source. L_{det} is the externally added $\frac{di}{dt}$ limiting inductor also used for fault detection purposes, R_f is the fault resistance, L_{line} and R_{line} are the line inductance and resistance. The equivalent circuit can be used to understand how the line current (i_{line}) changes immediately after a fault has occurred in a distribution line. Consequently, the characteristics of the voltage transient (V_L) across L_{det} can also be interpreted.

According to Kirchoff's voltage law, the loop equation in the above figure is

$$V_{DC} = (L_{det} + L_{line})\frac{di_{line}(t)}{dt} + (R_{line} + R_f)\, i_{line}(t). \tag{3.1}$$

This can be rearranged to form a differential equation of the line current

$$\frac{di_{line}(t)}{dt} + \left(\frac{R_{line} + R_f}{L_{det} + L_{line}}\right) i_{line}(t) = \frac{V_{DC}}{L_{det} + L_{line}}. \tag{3.2}$$

This equation can be solved using an integrating factor. The solution is stated in (3.3). Complete details of the differential equation's solution are included in appendix A.

$$\mathbf{i_{line}(t) = \frac{V_{DC}}{R_{line} + R_f} + \left(i(0) - \frac{V_{DC}}{R_{line} + R_f}\right) e^{-\left(\frac{R_{line}+R_f}{L_{det}+L_{line}}\right)t}}. \tag{3.3}$$

In (3.3), i(0) is the magnitude of the current flowing in the line just before the fault occurs. Using equation (2.4), the transient voltage V_L produced across L_{det} after fault occurrence can be calculated. The equation is repeated below for convenience

$$V_L = L_{det}\left(\frac{di_{line}(t)}{dt}\right). \tag{3.4}$$

Substituting (3.3) in (3.4) leads to equation (3.5)

$$V_L = L_{det}\left[\frac{d}{dt}\left(\frac{V_{DC}}{R_{line} + R_f} + \left(i(0) - \frac{V_{DC}}{R_{line} + R_f}\right) e^{-\left(\frac{R_{line}+R_f}{L_{det}+L_{line}}\right)t}\right)\right], \tag{3.5}$$

and then simplifying (3.5) gives the expression below

$$\mathbf{V_L = [V_{DC} - i(0)(R_{line} + R_f)]\left(\frac{L_{det}}{L_{det} + L_{line}}\right) e^{-\left(\frac{R_{line}+R_f}{L_{det}+L_{line}}\right)t}}. \tag{3.6}$$

Equation (3.6) depicts that the magnitude of V_L is dependent on two major factors. The first is the difference between the output source voltage (V_{DC}) and the voltage drop across the resistive elements of the distribution line. Line resistance and inductance of 0.164Ω/km and 0.24mH/km have been reported specifically for LVDC distribution lines [21]. Due to the low DC distribution line resistance, the voltage drop is usually small. Hence, V_{DC} has a more significant contribution to the observed V_L magnitude. Moreover, the second major factor is the ratio of L_{det} to the total inductance in the DC distribution line. If L_{line} is small compared to L_{det}, then the majority of the transient voltage magnitude will be across L_{det}. This can be the case if the fault location is in close vicinity to L_{det}. Albeit, if L_{line} is large, then the share of the transient voltage across L_{det} will be much smaller. This type of scenario can occur on an extremely long distribution line with the fault location at a considerable distance from L_{det}. Unfortunately, a larger L_{det} cannot be added in LVDC network lines because of a limit on the amount of energy that can be dissipated in the SSCB's snubber circuit after fault isolation. Thus, the inductance ratio also has a notable contribution to the transient voltage magnitude. These factors together determine the observed V_L magnitude subsequent to fault occurrence. Depending on the fault location and V_{DC}, the magnitude of V_L can be quite large, up to several hundreds of volts.

Additionally, it can be inferred from (3.6) that the V_L transient voltage has an exponential waveform. Due to the negative sign, it is a decaying exponential time function. As a result, the highest magnitude

across L_{det} is observed immediately after a fault happens. The speed of decay of the transient is determined by the exponential waveform's time constant (τ). The time constant of a faulted DC distribution line is

$$\tau = \left(\frac{L_{\text{det}} + L_{\text{line}}}{R_{\text{line}} + R_{\text{f}}} \right). \tag{3.7}$$

The relatively small L_{line} and L_{det} ensure that τ is also short. This implies that subsequent to a fault, the transient voltage across L_{det} exists only for a brief duration.

3.2.2. Circuit Design Requirements

The theoretical evaluation after a fault occurs has exhibited some important characteristics of the transient V_L voltage. In order to measure V_L, these characteristics directly determine the design of the detection circuit. Therefore, the design requirements of the circuit for the V_L based fault detection method can be deduced. The circuit has to be designed according to the necessary design requirements to ensure that a fault is detectable.

The design requirements are listed and elaborated below:

- **Measure the differential voltage across the L_{det} inductor**
  The selected fault detection method relies on the potential difference across the externally added inductor. Processing single-ended voltage measurements can add computation delays. Hence, to not compromise on the speed of fault detection the circuit has to be capable of measuring the voltage difference across the inductor.

- **The circuit should be fast in its operation**
  As depicted in equations (3.6) and (3.7) in the previous section, the V_L transient voltage has a decaying exponential waveform with a short time constant. Therefore, after fault occurrence the transient exists only momentarily. To ensure fault detection, the circuit should be able to measure the momentary transient voltage before it evanesces. Consequently, the design needs to consider the operation speed of the detection circuit.

- **Measure a range of V_L magnitude across the L_{det} inductor**
  Equation (3.6) also illustrates that the magnitude of V_L is dependent on the fault impedance and location. As a result, a large range of the V_L transient magnitude can be expected. The detection circuit should be able to accurately measure a wide span of the expected V_L's magnitude range. This can result in a tremendous number of faults in the LVDC network being detected and isolated as quickly as possible via the V_L detection method.

- **No effect on the normal performance of the LVDC network**
  The detection circuit should function only when a fault has occurred in the distribution lines. Apart from this it should not have any contribution and seem as if it is invisible in the network. This will allow the normal operation of the LVDC network and also guarantee the safety of the designed detection circuit itself.

3.2.3. Detection Circuit Design

The preceding design specifications provide a basis for the selection of an appropriate voltage measurement device. The sharp V_L transient voltage experienced in the event of a fault consists of various frequency components. Therefore, the measurement device should have a high operation bandwidth to be capable of measuring the rapid voltage changes across L_{det}. Moreover, the device should have a minimal time delay between its input signals and the corresponding output results. This will improve the speed of the circuit in detecting possible faults. Using analog based measurement devices can fulfill the design requirements.

Operational amplifiers (Op-Amp) completely fit the above description. They are analog devices offering a wide range of versatile characteristics that are easily controllable through additional external components. Op-Amps have two inputs which can be configured to measure a differential voltage. This enables V_L across L_{det} to be measured by connecting the Op-Amp inputs across the inductor. The differential voltage has to be measured in the presence of a common voltage across the inductor's terminals. Op-Amps can suppress most of the common mode voltage at their input terminals and amplify only the differential voltage. This particular property is known as common mode rejection (CMR)

and is expressed as a ratio (CMRR) [41]. In general, greater the value of the CMRR, the better is the performance of the Op-Amp. Various Op-Amps are available with a high CMRR.

Furthermore, several Op-Amps have large bandwidths and high slew rates. Slew rate is defined as the change of voltage per unit time and is measured in V/μs. A high slew rate indicates that the Op-Amp's output can respond faster to changes at the inputs. Along with large operating bandwidths this property of Op-Amps makes them suitable to measure the sharp and ephemeral V_L transient. Additionally, Op-Amps have a fixed range for the output voltage swing. The range is usually limited by the amplifier's supply voltage. This can make it difficult to measure extremely large V_L magnitudes across L_{det}. However, the closed loop differential voltage gain of Op-Amps can be easily set using external resistors. By properly designing the external resistor values, the amplifier can be able to translate a large range of V_L magnitudes such that the output remains within the allowed voltage swing.

These diverse properties make Op-Amps the ideal devices for measurement of the V_L magnitude. Therefore, the Op-Amp and its supplementary circuit form an integral part of the V_L based fault detection method. Hence, designing the Op-Amp circuit is equivalent to the design of the fault detection circuit. There are several types of amplifiers capable of measuring the V_L voltage. The following subsections evaluate these options.

Fully-Differential Amplifier

A logical choice to measure the differential voltage across L_{det} for fault detection purposes is to use a fully-differential amplifier. The amplifier is aptly named because its output is also in the form of a differential voltage. Figure 3.2 below shows the schematic of a fully-differential amplifier. The resistors (R_F and R_G) are used to set the closed loop differential voltage gain. V_s and -V_s represent the amplifier's positive and negative supply voltages.

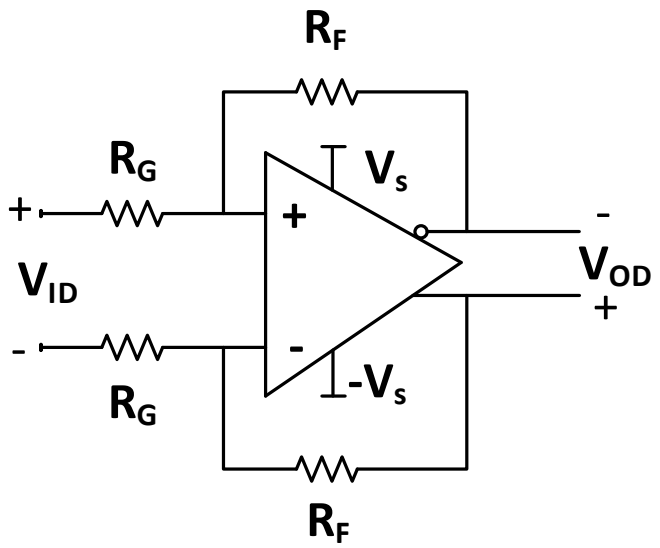


Figure 3.2: Schematic of a Fully-Differential Amplifier

The fully-differential amplifier uses its two inputs to measure a differential input voltage (V_{ID}). V_{ID} is scaled by the voltage gain to produce two output voltages. The outputs have a phase difference of 180° between them. Hence, each output is the inverted version of the other. The voltage difference between the two outputs is the amplifier's differential output voltage (V_{OD}) and can be calculated using the equation below

$$V_{\text{OD}} = \left(\frac{R_F}{R_G}\right) V_{\text{ID}}, \tag{3.8}$$

where $\left(\frac{R_F}{R_G}\right)$ represents the amplifier's voltage gain.

Fully-differential amplifiers can attain high slew rates and operating bandwidths. In fact, the THS4520 fully-differential amplifier can operate at a slew rate of 570V/μs and has a bandwidth of up to 620MHz [42]. This can enable the detection circuit to track the quick changes in the V_L voltage. Moreover, as the output voltage is a differential measurement, the noise that is common on the voltage supply and output terminals is cancelled. This results in an increased noise immunity of the amplifier and possibly better performance [43]. The two opposite output voltages of a fully-differential amplifier result in double the output voltage swing compared to that of a normal Op-Amp. This feature can allow a larger range of the high expected V_L magnitudes to be measured accurately via the fully-differential amplifier.

To determine fault occurrence, the V_L voltage measured by the detection circuit will be compared to a predefined threshold value. The subsequent outcome has direct control over the state of the SSCB (either conducting or open). A digital controller will be used to control the SSCB. They incorporate microcontrollers which are easy to use and capable of high performance levels. Furthermore, the digital controller will also be used to read and process the V_L signal measured via the detection circuit.

A drawback of a fully-differential amplifier is that its output is not single-ended but a differential voltage signal. This essentially signifies that a fully-differential amplifier cannot be directly interfaced with a digital controller. Although an extra Op-Amp stage can be added to convert the differential output to a single-ended signal, this would add unnecessary time delay and possibly undermine the speed of the V_L fault detection method. Therefore, even though with all its suitable properties a fully-differential amplifier is not the best option to use in the detection circuit.

Regular Op-Amp Configured as a Differential Amplifier

A regular Op-Amp's property of measuring a differential voltage can be utilized to measure the V_L transient voltage. The major difference compared to a fully-differential amplifier is that the output of the amplifier is a single-ended signal. The configuration of a differential amplifier via a regular Op-Amp is shown below in figure 3.3. It has only one feedback connection between the output and the inverting input terminals. R_G is connected between the non-inverting terminal and the ground potential. The two input voltage signals (V_{IN1} and V_{IN2}) are connected to the Op-Amp's input terminals through R_1 and R_2.

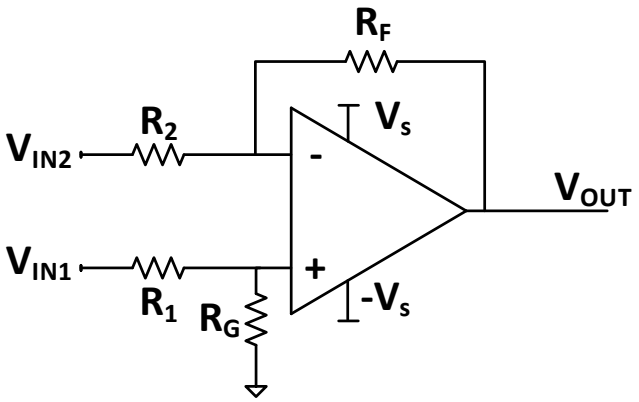


Figure 3.3: Schematic of a Differential Amplifier via a Regular Operational Amplifier

The two input voltage signals can also have a common mode voltage component. However, the amplifier should operate only on the differential voltage component measured between V_{IN1} and V_{IN2} to produce the output signal V_{OUT}. Similar to the fully-differential amplifier, the resistors (R_1, R_2, R_F and R_G) are used to set the closed loop differential voltage gain. An equation for V_{OUT} equivalent to

(3.8) can be realized if the resistors are selected such that R_1=R_2 and R_F=R_G. This results in

$$V_{OUT} = \left(\frac{R_F}{R_2}\right)(V_{IN1} - V_{IN2}), \tag{3.9}$$

for the differential amplifier.

Regular Op-Amps having large bandwidths are readily available. Thereby, enabling the sharp V_L transient to be measured. Moreover, as V_{OUT} is a single-ended signal it can be readily interfaced with a microcontroller after being digitized. This will help in preserving the speed of the V_L fault detection method.

During normal operation, the voltage V_L across L_{det} is expected to be zero. This implies that the voltage on both the terminals of L_{det} will be equal to V_{DC} as seen in figure 3.1. As the differential amplifier is expected to be directly connected across the terminals of L_{det}, V_{DC} will also be present at the amplifier's inputs (V_{IN1} and V_{IN2}). Therefore, a large common mode voltage will be applied at the inputs of the differential amplifier. This requires the amplifier to have an extremely large CMRR to mitigate the effect of the common mode voltage at the output [44]. However, for regular Op-Amps the CMRR is specified only until the supply voltage (V_s, $-V_s$) limit [45], [46]. These are within tens of volts, usually up to a maximum of 30 V for most amplifiers [47]. If the limits are surpassed, the CMRR deteriorates extremely quickly.

LVDC networks are expected to operate at voltage levels of 350-380 V [10], [11]. Hence, referencing figure 3.1, the network's nominal voltage will become the average common mode input voltage of the differential amplifier. The nominal voltage value is tremendously higher than the safe operating input voltage limits of regular Op-Amps. The input voltage's range of operation is usually recommended up till the supply voltage. Moreover, at such large input voltage values, an Op-Amp's CMR ratios are also not specified. This can result in the differential amplifier's output to be inaccurate, noisy and to eventually malfunction [45].

Isolation Amplifier

An alternative method of measuring the differential voltage V_L in the presence of a large common mode voltage is via an isolation amplifier. Isolation amplifier is a type of a differential amplifier. It provides galvanic isolation between its input and output terminals. As a result, the input and output terminal circuits of the amplifier become physically separated from each other. This allows the amplifier to function properly in the presence of a large common mode input voltage. The isolation barrier also protects voltage sensitive components within the amplifier from damage.

Figure 3.4 below shows the schematic of an isolation amplifier. It requires two power supplies (V_s, $-V_s$ and V_{DD}, $-V_{DD}$) for its operation, one on either side of the isolation barrier. Isolation between the two power supplies is also necessary.

There are three methods of providing isolation between the input and output terminals. The first is a transformer-based isolation, incorporating the transformer within the IC package. The second is optical

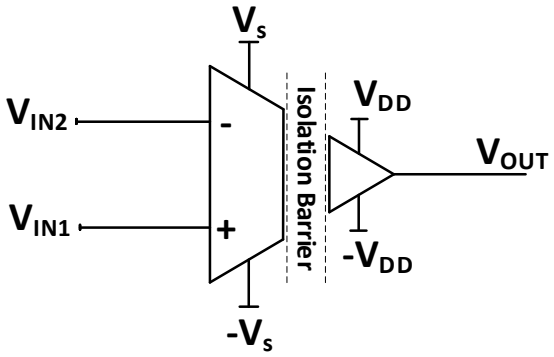


Figure 3.4: Schematic of an Isolation Amplifier

based, using LED optocouplers and the last method is via small capacitors. The optical based isolation barrier can withstand voltages up to 900 V while the capacitor based isolation up to 5 kV [48], [49]. Therefore, in an LVDC network setup, isolation amplifiers are a good choice to sense the differential voltage V_L across the L_{det} inductor. The reason is because the nominal LVDC network voltage (350-380 V) is within the common mode voltage range of various isolation amplifiers. Consequently, compared to other types of Op-Amps, isolation Op-Amps also tend to have higher CMRRs [44].

Nevertheless, a major limitation of isolation amplifiers is the expected time delay in the output voltage responding to a change at the input terminals. The time delays are mainly observed due to the physical coupling of signals across the isolation barrier. These delays are reported to be in the range of several microseconds [50]. The shortest time delay for an isolation amplifier is for the ISO224 device produced by Texas Instruments. They report 2μs for the output voltage to rise in response to a change at the inputs [49]. As mentioned earlier, the anticipated $\frac{di}{dt}$ rise as a consequence of a fault is extremely high in DC networks (about 10 kA/ms) [29]. Even though the ISO224 isolation amplifier's 2μs response time is impressive, it can prove to be unsatisfactory for the V_L based fault detection method. This is because the V_L fault detection method is meant to detect and isolate faults that cause extremely high $\frac{di}{dt}$ rise rates in the network. For this to be feasible, the detection circuit's processing time delay has to be as short as possible. Unfortunately, this is a tall order for an isolation amplifier.

Furthermore, due to the isolation barrier between the output and input terminals, conventional negative feedback cannot be applied. This means that the differential voltage gain cannot be controlled externally through resistors. All isolation amplifiers either have a fixed or a predefined small range for the gain. This implies that the entire anticipated magnitude range of the V_L transient cannot be accurately measured by an isolation amplifier. As there is no control over the differential gain, the result can be saturation of the Op Amp's output terminal. This will lead to inaccurate measurements and possible false fault detections. Therefore, the reasons explained above show that measuring the fast V_L transient voltage via an isolation amplifier faces some technical limitations.

Final Detection Circuit Design

Thus far, several types of Op-Amps have been proposed to be used as part of the design of the fault detection circuit. Each type of Op-Amp has some merits and demerits. Regular differential amplifiers are fast in their operation and have a single ended output signal. However, their input common mode voltage levels are quite low. On the other hand, isolation amplifiers can operate in the presence of high common mode voltages but they have inherent time delays that are deemed unacceptable for the purpose of fault detection.

Nevertheless, an Op-Amp's design as a constituent of the fault detection circuit has been finalized. The final adopted design aims to combine the benefits of various types of amplifiers discussed while also reducing the demerits as much as possible. The design uses a regular amplifier configured as a differential amplifier. Moreover, a technique known as 'poor man's isolation is utilized'. This technique enables the differential amplifier to operate in the presence of large common mode voltages [51]. Instead of providing physical galvanic isolation, the poor man's isolation technique uses large impedances to 'isolate' the differential amplifier from the common mode voltage. This method cannot be considered as proper isolation but it is effective in protecting and allowing the differential amplifier to function in an environment of high common mode voltage. Additionally, this technique also doesn't add the time delays associated with galvanic isolation barriers observed particularly in isolation amplifiers. Hence, this design alteration should allow faults in the LVDC network to be detected extremely rapidly via the V_L based detection method while also protecting the Op-Amp measurement circuit.

Figure 3.5 shows the differential amplifier and the poor man's isolation impedances connected together. To protect the differential amplifier, an isolation impedance is required before each input. This also helps in balancing the amplifier's inputs. The isolation impedances are represented by R_{ISO1}, R_{ISO2} and usually have large values. As seen in figure 3.5, V_{IN1}, V_{IN2} are applied before R_{ISO1} and R_{ISO2}. The difference between V_{IN1} and V_{IN2} represents the voltage magnitude V_L, across the L_{det} inductor in a DC distribution line. R_{ISO1} and R_{ISO2} 'isolate' the differential amplifier from the high common mode voltage present across the inductor terminals (V_{IN1}, V_{IN2}). In this manner, when a fault occurs the transient voltage V_L produced across L_{det} can be measured accurately by the differential amplifier.

Due to the addition of the isolation impedances (R_{ISO1}, R_{ISO2}) in the overall detection circuit, the

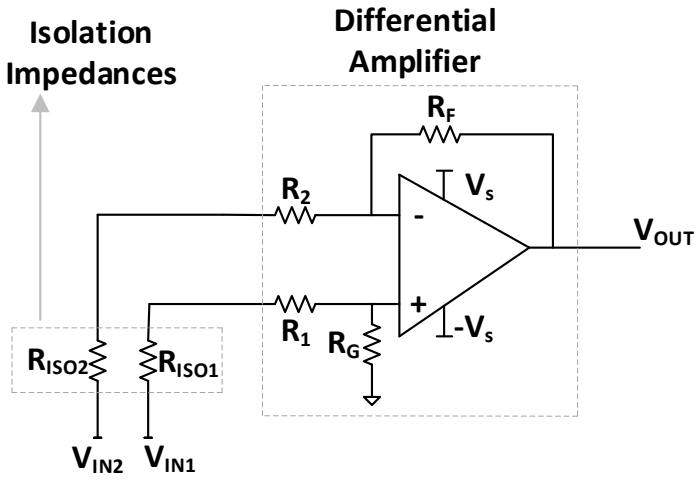


Figure 3.5: Differential Amplifier With Poor Man's Isolation

differential voltage gain of the Op-Amp changes. It is given by the equation below

$$V_{\text{OUT}} = \left(\frac{R_{\text{F}}}{R_{\text{ISO2}} + R_2}\right)(V_{\text{IN1}} - V_{\text{IN2}})\,. \tag{3.10}$$

3.2.4. Simulation Results

To investigate the validity of the finalized design of the detection circuit, some simulations were conducted. The performance of the fault detection circuit can be judged from the simulation results. Moreover, other important characteristics of the detection circuit, the SSCB or in general the LVDC network (that could have been previously overlooked) can be highlighted with the help of simulations.

First, a simulation model of a DC distribution line in a LVDC network needs to be developed. The model should incorporate the SSCB and the L_{det} inductor used for both, limiting the $\frac{di}{dt}$ rise and fault detection. Next, a controllable fault condition will be added in order to judge the performance of the designed detection circuit.

The DC distribution line's model used for simulation purposes is shown below in figure 3.6. The model portrays a 'last mile' LVDC distribution network. Power is being delivered from an energy source to an end user (a house) represented by the load. V_{DC} denotes the output voltage of a VSC used to

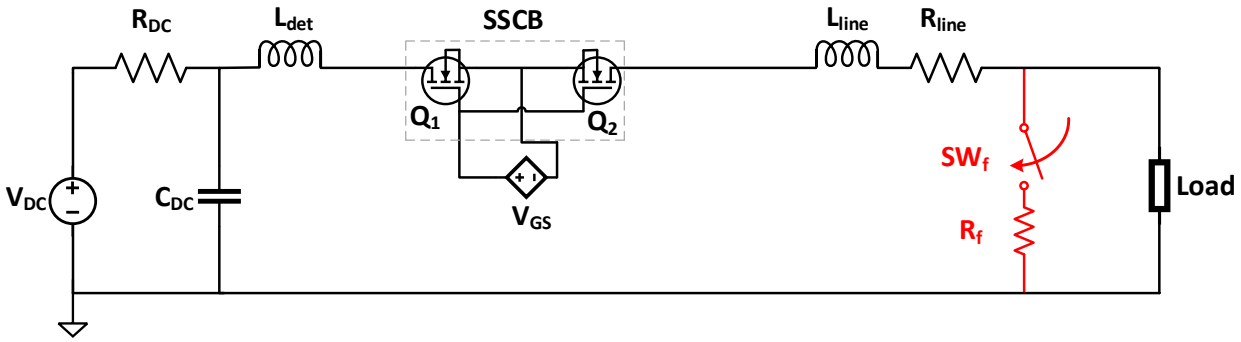


Figure 3.6: Model of a DC Distribution Line

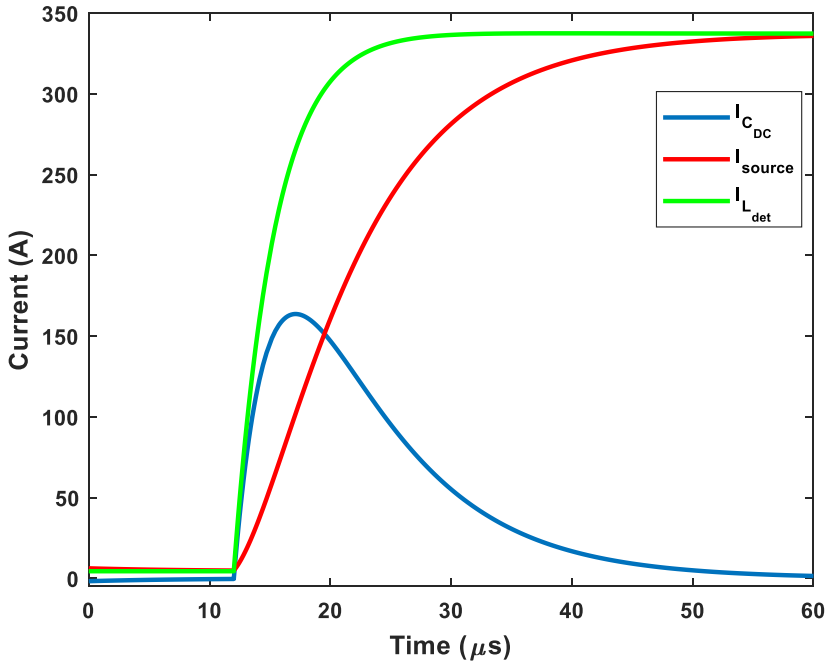


Figure 3.7: Current Flow In a DC distribution Line After Fault Occurrence

connect the energy source to the LVDC network. R_{DC} and C_{DC} represent the VSC's output impedance and the capacitor used to smooth the V_{DC} voltage. Moreover, Q_1 and Q_2 are MOSFETs connected in an anti-series configuration to form the SSCB while V_{GS} is the SSCB's gate drive signal. The controllable fault is shown in red in figure 3.6. SW_f is a simple controllable switch. Its state determines whether a fault condition exists in the DC distribution line. Closing SW_f simulates a fault with resistance R_f.

Distribution Line Model's Simulation Results

Next, a fault was simulated to observe the flow of currents in the DC distribution line. The corresponding results are shown in figure 3.7. The simulations are performed in LTspice® XVII and the results are plotted using MATLAB®. The figure shows currents flowing from the energy source (red), the capacitor (blue) and in the distribution line (green). A fault condition was generated at 12μs by closing SW_f. As seen in the figure, before fault occurrence, the load is supplied current from the source and the capacitor's contribution is negligible. Immediately after the fault a huge spike is seen in the capacitor current and consequently, the line current. As expected, the capacitor's current spike cannot be sustained and the current tapers off. However, the line current still increases. This is because the source now begins to supply the majority of the current into the fault. From figure 3.7 it can also be inferred that after the fault, the line current rises to 10 times its normal value in approximately 2μs and to 30 times in just 10μs. Hence, this again highlights the extreme dangers associated with DC faults and the need for fast detection and isolation.

Moreover, figure 3.8 below shows the V_L magnitude across L_{det} along with the current flowing through the inductor (same as the line current). The figure exhibits the transient nature of the V_L magnitude. Before fault occurrence, V_L is zero due to DC current flowing across the inductor. However, after the fault due to the extremely quick current rise, a large immediate transient magnitude is observed across L_{det}. As the $\frac{di}{dt}$ rise rate decreases, the voltage V_L also sharply diminishes. The line current quickly attains a new steady state, consequently causing V_L to again fall to zero. Figure 3.8 also illustrates that the V_L transient voltage has a prominent value for only a few microseconds. Hence, this elucidates the reason why the designed V_L detection circuit needs to be extremely fast in its measurement.

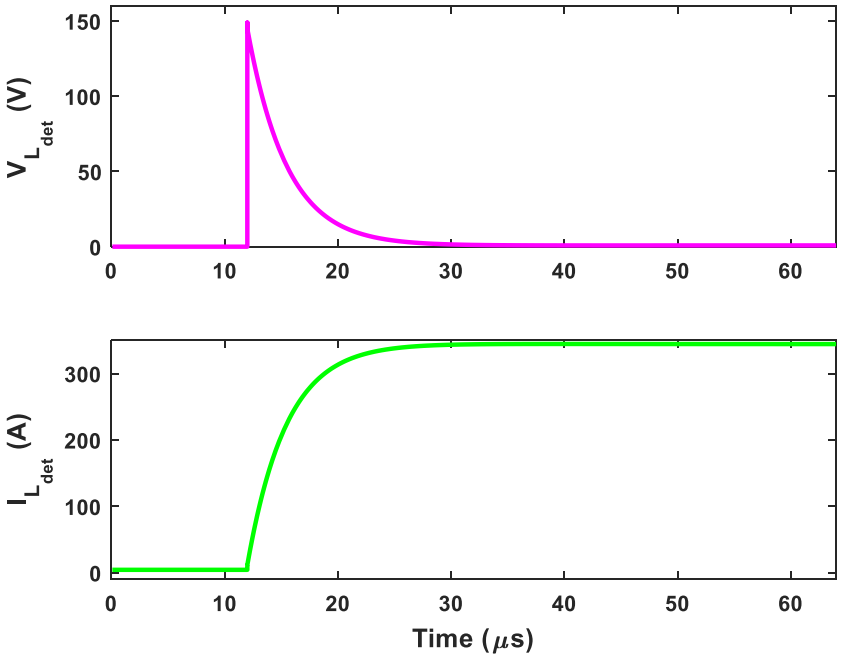


Figure 3.8: Current and Voltage Waveforms Across the L_{det} Inductor

The circuit parameters of the distribution line and the additional components used for the results are expressed in the table below. V_{DC}'s value is similar to the value recommended for LVDC distribution networks while C_{DC} is a typical value of a VSC's output filter capacitor. L_{line} is comparable to L_{det}, indicating that the fault was in close vicinity to L_{det}. Additionally, Silicon Carbide (SiC) MOSFETs are used for the SSCB as they typically have lower on-state resistances (R_{DS}). Their recommended gate to source (V_{GS}) voltage is slightly higher than that used for Silicon MOSFETs.

V_{DC} (V)	C_{DC} (μF)	L_{det} (μH)	L_{line} (μH)	R_{line} (mΩ)	R_{Load} (Ω)	R_f (Ω)	V_{GS} (V)	Q_1,Q_2
350	750	1.5	2.4	1.6	80	1	15	C3M0030090K

Table 3.1: Circuit Parameters for the Simulation Results Shown In Figures 3.7 and 3.8.

Figure 3.9 demonstrates various V_L magnitudes across L_{det} as a function of increasing fault location distance from L_{det}. Consequently, this also signifies the periodic increase in L_{line} and R_{line}. For the results of figure 3.9, the circuit parameters are identical to those of table 3.1 apart from L_{line} and R_{line}. With increasing L_{line}, the V_L magnitude decreases. This is as predicted in equation (3.6) in section 3.2.1. Furthermore, figure 3.9 also shows that for greater L_{line} values the V_L magnitude has a prominent value (close to the peak) for a longer period of time. This is due to a longer time period (τ).

A trade-off exists between the measurement of the V_L voltage and the fault location. A fault occurring in close vicinity produces a large transient magnitude but lasts for an extremely short period of time. Where as, a fault farther away exists for longer but can have a relatively small transient magnitude. Hence, this shows that the designed V_L detection circuit should be capable of measuring a sufficient range of the voltage transient's magnitude across L_{det}.

Simulation Results of the Designed Detection Circuit

Till now, the V_L voltage waveforms shown were measured directly across the L_{det} inductor. Henceforth, the finalized design of the V_L detection circuit shown in figure 3.5 is connected across L_{det}. This subsection presents the details of the detection circuit and its corresponding simulation results.

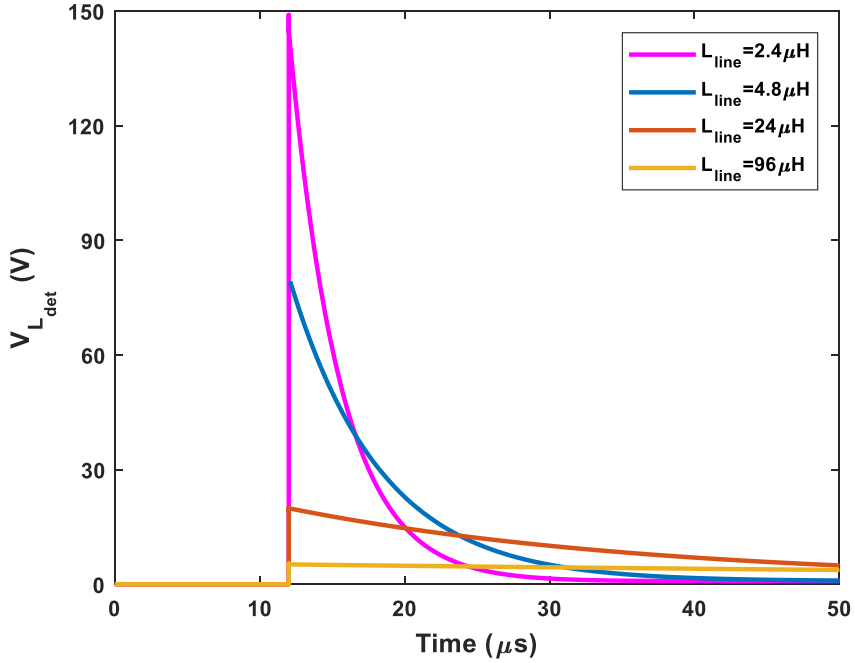


Figure 3.9: Voltage Across L_{det} With Increasing Fault Distance

The differential Op-Amp responsible for measuring the V_L magnitude is connected across L_{det} via the isolation impedances (R_{ISO1}, R_{ISO2}). As mentioned previously, the isolation impedances protect the differential Op-Amp's inputs from the high common mode voltage present at the terminals of L_{det}. The Op-Amp chosen to be configured as the differential amplifier is LM7321 manufactured by Texas Instruments. Its particular simulation model was imported in LTspice XVII and used to obtain the simulation results. LM7321 has adequate bandwidth and slew rate values. It has a sufficient CMR ratio and a wide supply voltage (V_s to -V_s) of up to 30 V [52]. Moreover, the LM7321 has the ability to drive capacitive load outputs. This property will be useful in the practical implementation of the fault detection setup. The reason is that the Op-Amp's output will be the input to a microcontroller for processing the detection circuit's output.

Consequently, this sets a restriction on the output voltage (V_{OUT}) of the differential amplifier such that it should not exceed 3.3 V. As microcontrollers operate at a 3.3 V logic, the restriction is placed to ensure their safety. Therefore, the resistor values of the differential amplifier are selected according to equation (3.10) while keeping the maximum allowed V_{OUT} in mind. These values are listed in table 3.2.

R_{ISO1} (kΩ)	R_{ISO2} (kΩ)	R_1 (kΩ)	R_2 (kΩ)	R_G (kΩ)	R_F (kΩ)	C_F (pF)
300	300	0.1	0.1	3	3	33

Table 3.2: Component Values of the Designed V_L Fault Detection Circuit

Naturally, R_{ISO1} and R_{ISO2} have large values to provide high impedance. These high impedances mimic the 'isolation' and allow the differential amplifier to measure the V_L transient voltage in the presence of the high common mode voltage [51]. The resistor values were selected considering that the nominal voltage (V_{DC}) in the simulation model is 350 V and that there is always some L_{line} present in the distribution line. This causes the V_L voltage across L_{det} to remain smaller than 350 V (also seen in figure 3.9). Hence, these values should ensure that the differential amplifier's V_{OUT} remains within the safe limit. In table 3.2, a value for C_F is also mentioned. C_F represents a capacitor to be connected in parallel to R_F in figure 3.5. Together both of these components form a low pass filter to limit the

band of frequencies in V_{OUT}. This should help V_{OUT} to have a smooth response at the moment of fault occurrence.

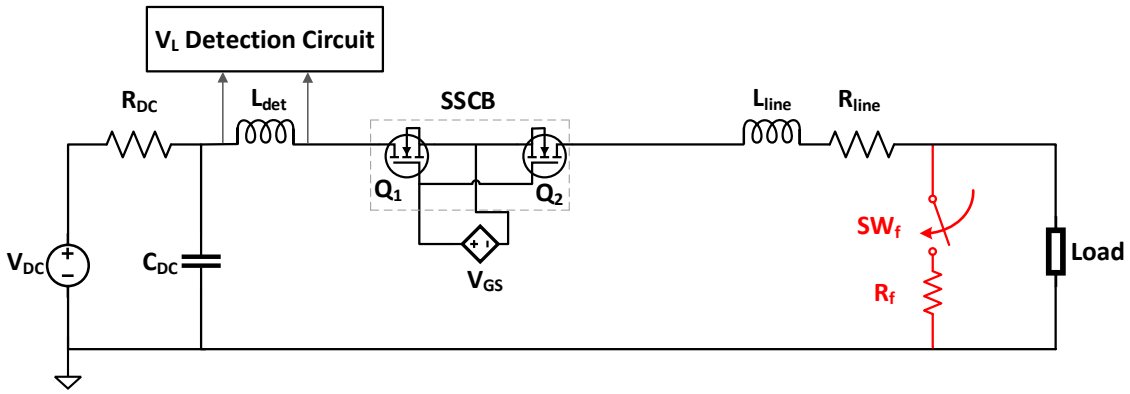


Figure 3.10: DC Distribution Line and the V_L Detection Circuit

Figure 3.10 depicts the DC distribution line's model and the connecting points of the designed V_L detection circuit. The detection circuit is shown as a block for simplicity in figure 3.10 and represents the circuit of figure 3.5. Additionally, figure 3.11 shows V_{OUT} (in blue) of the designed detection circuit when a fault is simulated in the distribution line at 12μs. The figure can be considered as a zoomed version of figure 3.8. The circuit parameters of table 3.1 are used again for the results. Figure 3.11 shows that V_{OUT} is able to track the V_L transient voltage across L_{det}. After fault occurence, the V_L voltage shoots up immediately, where as an initial rise time of approximately 400ns is observed in V_{OUT}'s waveform. However, this amount of time is acceptable. After the rise, V_{OUT} tracks V_L extremely well. Moreover, the magnitude of V_{OUT} also remains within the set extreme limit. Hence, these results indicate that the design of the V_L detection circuit is adequate.

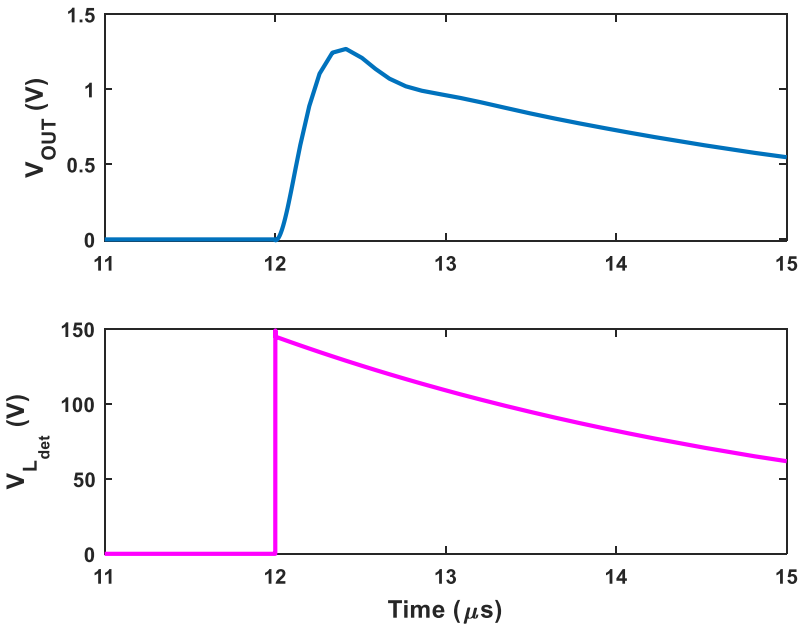
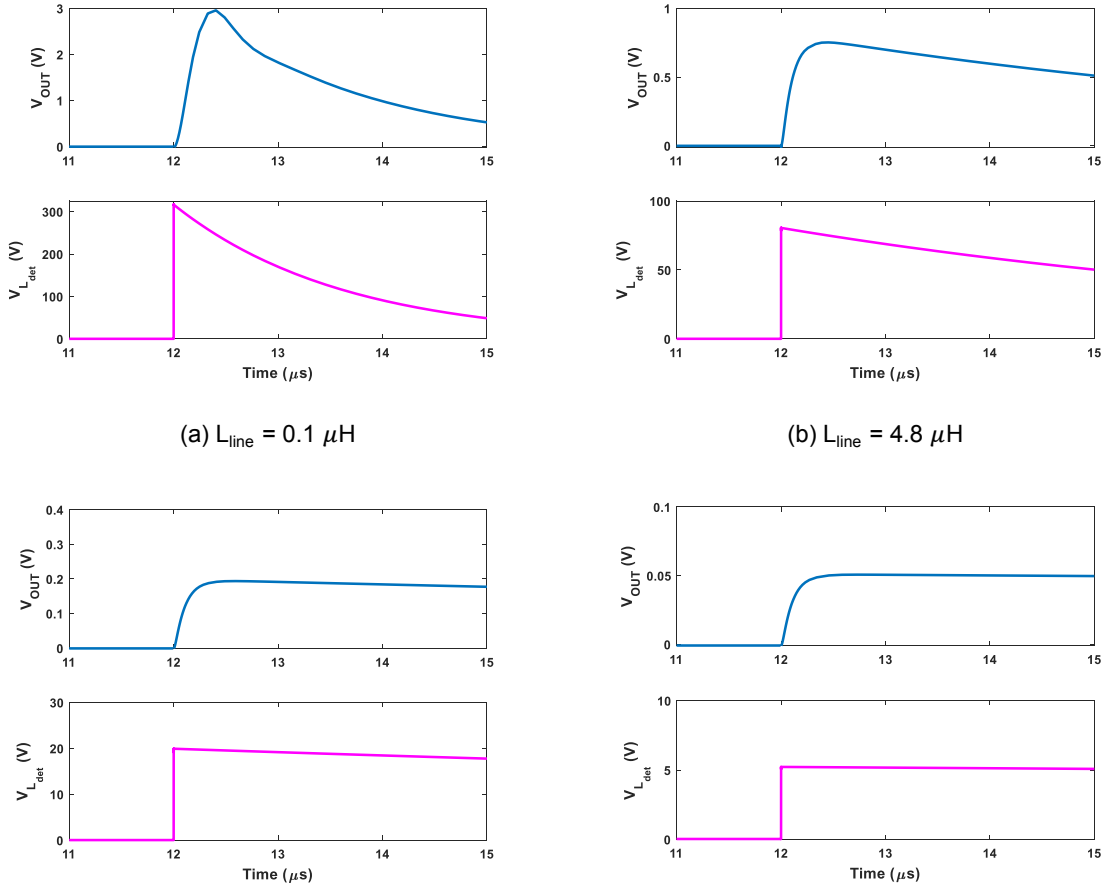


Figure 3.11: V_L Across L_{det} and the Corresponding Measurement of the Detection Circuit (V_{OUT})



(a) L_{line} = 0.1 μH

(b) L_{line} = 4.8 μH

(c) L_{line} = 24 μH

(d) L_{line} = 96 μH

Figure 3.12: V_L and the Measured V_{OUT} by the Designed Detection Circuit as a Function of L_{line}

Moreover, figure 3.12 shows several V_{OUT} waveforms of the designed detection circuit measured from their corresponding V_L voltage. The measurements are a function of increasing L_{line} thus, also indicating an increase in the fault distance from the L_{det} inductor. Figure 3.12a displays results with L_{line} of 0.1 μH. Such a low L_{line} value indicates that the fault occurred extremely close to the terminals of L_{det}. Therefore, as predicted by equation (3.6) and observed in the figure the peak value of V_L is comparable to V_{DC}. Accordingly, V_{OUT} is also large and close to the maximum allowed value. As V_{OUT}'s voltage does not exceed the 3.3V limit, the detection circuit's design is proved to be valid even for the most extreme fault condition. The rise time of the V_{OUT} voltage is also quick, signifying that fast fault detection is possible via the designed circuit.

In addition, the detection circuit's response with higher L_{line} is also adequate. As seen in figure 3.12b, V_{OUT} demonstrates a quick response to the immediate V_L voltage transient across L_{det} due to a fault in the distribution line. The magnitude of V_{OUT} also has a sufficient value for a longer time as compared to figure 3.12a. However, when L_{line} is exceedingly large as in figures 3.12c and 3.12d, after fault occurrence the V_{OUT} magnitude is severely low. The observed peak values are only 0.2 V in figure 3.12c and 0.05 V in figure 3.12d respectively. This is principally because of the smaller voltage drops across the L_{det} inductor. Although, the V_{OUT} magnitudes correspond with equation (3.10), the differential voltage gain cannot be increased significantly. The major reason is that the isolation impedances (R_{ISO1}, R_{ISO2}) must have large values for the differential amplifier to function properly. Moreover, the values of R_F and R_G in figure 3.5 cannot be increased due to fear of the microcontroller malfunctioning if the voltage exceeds its limits.

As a result, due to the low expected V_{OUT} magnitudes when L_{line} is sufficiently high (the fault distance

is large) the fault detection threshold will have to be set at an extremely small value. In a practical set up, due to noise or sudden load steps the threshold can be exceeded by the V_{OUT} signal. These false fault detections will cause problems of unnecessary tripping of the SSCB and interruptions in the LVDC network. Therefore, a low threshold voltage for the V_L detection circuit is unfeasible. Hence, this highlights the need for the V_{DS} based fault detection. It can operate on distant faults and thus, significantly reduce unnecessary tripping and interruptions in the network.

3.3. Circuit Design of the V_{DS} Detection Method

Although the V_L based detection method has proven to be fast in identifying faults in the LVDC network, it is still not capable of detecting each and every type of fault. This susceptibility was highlighted in the previous section as L_{line} increased (greater fault distance) compared to L_{det}'s inductance. Moreover, a high impedance fault can have the same effect on the V_L detection circuit as a large L_{line} does. Hence, the outcome being that the high impedance fault could also remain undetected in the network via the V_L detection circuit.

To prevent these types of faults from remaining undetected in the LVDC network, another fault detection method relying on measuring the voltage across the SSCB device (MOSFET or IGBT) was proposed. This method will work simultaneously with the V_L based detection method to maximize the fault detection capability in the distribution lines of the network. Although an SSCB can be implemented with either MOSFETs or IGBTs (choice dependent on the application), for simplicity this method will be called the V_{DS} based fault detection method.

The underlying principle behind this fault detection method is that during its on-state a MOSFET's channel can be modelled as a resistor (an IGBT as a constant voltage and a resistor). Therefore, measuring the V_{DS} voltage across an SSCB's device will be proportional to its channel current I_{DS}. As the entire distribution line's current flows through the SSCB (figure 3.6), I_{DS} is equivalent to the line current. Hence, monitoring the V_{DS} voltage can provide direct information about the current magnitude in the distribution line. A fault in the network resulting in an 'overcurrent' condition can be detected via the V_{DS} voltage measurement. Owing to the expected quick rise in the distribution line currents, V_{DS} will also increase rapidly. Thus, enabling fault detection via measurement of the V_{DS} voltage to be fast as well.

3.3.1. Circuit Design Requirements

Normally, a MOSFET/IGBT's on-state voltage are measured to estimate the degradation and ageing of the device used in a particular application. This measurement is done in an 'offline' method by stopping the application and disconnecting the semiconductor device module. The reason is to achieve a higher measurement degree accuracy [4]. However, for fault detection purposes disconnecting the device is not an option. The V_{DS} voltage measurements across the SSCB's semiconductor devices have to be carried out simultaneously with the LVDC network's operation. Only then can a fault in a distribution line be detected via this method.

Therefore, this sets some design requirements for the V_{DS} measurement circuit. These requirements are listed and briefly discussed below:

- **Measure the channel voltage of a SSCB device**
  The SSCB device's channel voltage is directly proportional to the current flowing through the channel. The V_{DS} voltage is in fact, the differential voltage measured across the channel. As a result, a design requirement of the detection circuit is to measure a differential voltage.

- **Be precise in its voltage measurements**
  Depending on the device's on-state resistance and nominal current rating, the V_{DS} voltage can range from several millivolts (mV) to a few volts. To minimize false fault detections and unnecessary tripping of the SSCB, V_{DS} should be measured accurately. This imposes the detection circuit to be able to precisely measure the channel voltage.

- **The detection circuit should be fast in its operation**
  As explained previously and shown in figure 3.7, the line current increases extremely rapidly after a fault has occurred. Consequently, V_{DS} will also increase at the same speed. To be able to quickly identify faults, the detection circuit should be able to measure the rapid changes in the

V_{DS} signal. Hence, the detection circuit needs to have minimum measurement and processing delays.

- **No effect on the normal performance of the SSCB and the LVDC network**
  The detection circuit is meant to be constantly measuring the V_{DS} voltage in anticipation of a fault. Meanwhile, the circuit should allow the distribution line to function normally and hence, also the LVDC network. However, it should be capable of interrupting the flow of current in a particular distribution line when a fault is detected via the measured V_{DS} voltage across its own SSCB.
- **Ensure the protection of its own circuit components**
  The V_{DS} measurement circuit will be directly connected across the SSCB's devices in the DC distribution line. As a result, the detection circuit is vulnerable to large currents and voltages. Therefore, in addition to the above mentioned requirements the circuit's design must cater to the safety of its own components.

Most of the circuit design requirements are similar to those in section 3.2.2 for the V_L based fault detection method. The major reasons are that both detection circuits are required to measure a differential voltage and have as little processing delays as possible. The latter requirement is important in ensuring the quick detection of faults.

3.3.2. Detection Circuit Design

The circuit design requirements specified in the previous subsection require a voltage measuring device similar to the one used for the V_L voltage signal. Again these requirements are easily fulfilled by Op-Amps. Therefore, to also measure the V_{DS} voltage, a regular Op-Amp configured as a differential amplifier can be used. Its schematic was shown in figure 3.3. The differential amplifier's suitable characteristics have already been highlighted in section 3.2.3. Moreover, several MOSFET devices (that can be utilized to form an SSCB) are available with extremely low on-state resistances (R_{DS}), in the order of only a few tens of milliohms (mΩ). Hence, the V_{DS} voltage across them is expected to rise to a few volts. This magnitude of differential voltage can be easily measured via a differential amplifier.

However, for the Op-Amp to measure the V_{DS} voltage, it will have to be connected directly across the SSCB's device. This connection can create problems in the network and the detection circuit itself. The reason is that the voltage on the SSCB's terminals is equivalent to the distribution line's nominal voltage. Therefore, this voltage will become the common mode input voltage of the differential amplifier. As explained earlier, regular Op-Amps have specified CMR values only till their supply voltages ($-V_s$, V_s). If the input common mode voltage exceeds beyond $-V_s$ or V_s, the Op-Amp's CMR performance degrades substantially. As the LVDC network's nominal voltage is several times higher than the maximum allowed magnitude of V_s, the direct connection of the differential amplifier across an SSCB device will produce extreme measurement errors. In fact, the large voltage at the inputs will endanger the safety of the entire detection circuit.

A similar problem was experienced in the V_L detection circuit's design. The solution adopted in that scenario was to use large impedances before the differential amplifier's inputs. The impedances imitated an isolation barrier between the differential amplifier and the input terminals. As a result, the Op-Amp was able to measure the differential voltage in the presence of the large common mode voltage. This type of an amplifier was dubbed the 'poor man's isolation amplifier' and its schematic represented in figure 3.5.

Although the circumstances for the V_{DS} detection circuit are similar, unfortunately the poor man's isolation technique cannot be used. This is because some current will flow in to the isolation resistors via the distribution line. This current will cause some measurement inaccuracies in the differential amplifier. As the V_{DS} voltage across the SSCB will be just a few volts, significant differences between the measured and the actual value can occur. In order to know the magnitude of the distribution line current, the V_{DS} voltage must be measured precisely at all times. The poor man's isolation technique cannot guarantee extreme measurement precision in the order of millivolts (mV). As accuracy is a necessary requirement of the V_{DS} detection circuit, a different approach must be adopted for its design.

An Adopted Circuit Design Method

The V_{DS} detection circuit's design should be able to fulfill all the requirements stated earlier. Therefore, this necessitates the design to be capable of measuring fast and accurate differential voltages.

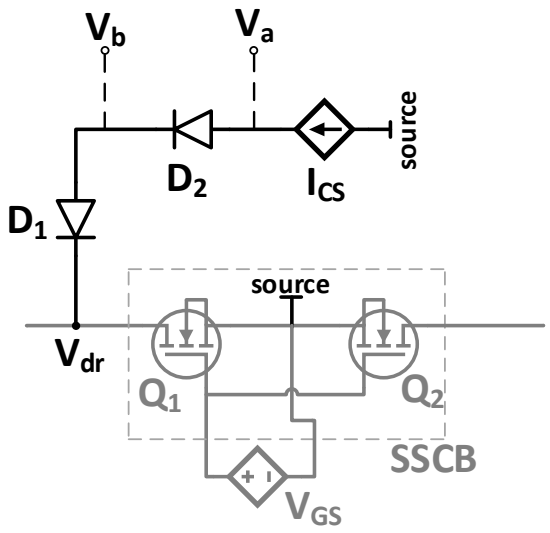


Figure 3.13: The V_{DS} Detection Circuit's Design Reported in [4]

Moreover, it should also be able to simultaneously protect the components from large common mode voltages and the likely voltage spikes across the SSCB device.

For this purpose, a circuit proposed by S. Beczkowski et. al. in [4], designed to measure the on-state voltage of a semiconductor device is adopted. This circuit design is capable of satisfying the requirements of accurate measurements and providing protection to the circuit components. The adopted design uses two diodes and a current source. The diodes are used for both, protecting the detection circuit's components and also in the precise measurement of the V_{DS} voltage. Nevertheless, a differential amplifier is still required for measuring the differential voltage. These components together form the basis of the adopted V_{DS} detection circuit's design.

The extra added components and their configuration is shown in figure 3.13. These components are highlighted in the figure and are connected across a particular device of the SSCB (in figure 3.13 across MOSFET Q_1). The two diodes (D_1 and D_2) are connected in series and a current source (I_{CS}) is connected behind them. I_{CS} is used to forward bias D_1, D_2 during the normal operation of the SSCB and the network. I_{CS}'s voltage reference is the common source terminal of the two SSCB MOSFETs. As a result, this enables the drain voltage (V_{dr}) of the MOSFET Q_1 to be measured with reference to the source voltage. Hence, the circuit becomes capable of measuring the V_{DS} voltage across Q_1. Furthermore, when the SSCB turns off in response to fault detection, D_1 protects the detection circuit's components by blocking the voltage across Q_1 [4].

During the normal operation of the distribution line, I_{CS} injects a small current through D_1 and D_2. Consequently, the diodes have forward voltage drops of V_{D1} and V_{D2} respectively. Assuming the two forward voltage drops are equal (V_{D1} = V_{D2}), the V_{dr} voltage can be measured with reference to the two SSCB MOSFETs common source voltage. The two voltage nodes V_a, V_b labelled in figure 3.13 are measured with reference to the common source voltage. They are related via the simple equation below

$$V_{\mathrm{a}} = V_{\mathrm{b}} + V_{\mathrm{D2}}. \tag{3.11}$$

Moreover, V_b is associated with V_{dr} in a similar way,

$$V_{\mathrm{b}} = V_{\mathrm{dr}} + V_{\mathrm{D1}}. \tag{3.12}$$

Considering the above assumption to be valid, equation (3.11) can be substituted in (3.12) to evaluate an expression for V_{dr} in terms of V_a and V_b. This is

$$\mathbf{V_{dr} = 2V_b - V_a}. \tag{3.13}$$

As the V_a, V_b voltages and I_{CS} have the SSCB's common source terminal as their reference, the V_{dr} voltage measured is equivalent to Q_1's V_{DS} voltage. In order for this method to make precise measurements, it is essential that the assumption of the forward voltage drops of D_1 and D_2 always remains valid. This can be made certain by using two identical diodes and that the current flowing through them via I_{CS} is the same. Moreover, the selected diodes should have similar forward voltage temperature coefficients and thermal junction characteristics [4]. This will ensure that the variations in the characteristics of D_1 and D_2 due to external conditions are identical.

In figure 3.13, D_1 is necessary to block the high voltages. By adding D_2 in series and ensuring that $V_{D1} = V_{D2}$, V_{DS} across Q_1 is measured via the voltages across D_2. Therefore, this design does not require a direct connection of a differential amplifier to the high common mode voltage terminals of the SSCB.

In addition, the equation in (3.13) can be realized using Op-Amps. These Op-Amps are to be connected directly at the V_a, V_b voltage terminals. This configuration is shown in figure 3.14. The first Op-Amp is configured as a non-inverting amplifier. Its purpose is to double the magnitude of the V_b voltage signal. Hence, following the conventional differential gain formula of a non-inverting amplifier (equation 3.14), R_5=R_6

$$V_{\mathrm{b}}{}' = \left(1 + \frac{R_5}{R_6}\right) V_{\mathrm{b}}, \tag{3.14}$$

where V_b' is the non-inverting amplifier's output signal. The second Op-Amp is configured as the differential amplifier that performs the arithmetic subtraction on its two input signals, as required in equation (3.13). The resultant output signal V_{dr}' is simply given by

$$V_{\mathrm{dr}}{}' = \left(\frac{R_4}{R_2}\right)(V_{\mathrm{b}}{}' - V_{\mathrm{a}}) = \left(\frac{R_4}{R_2}\right) V_{\mathrm{dr}}. \tag{3.15}$$

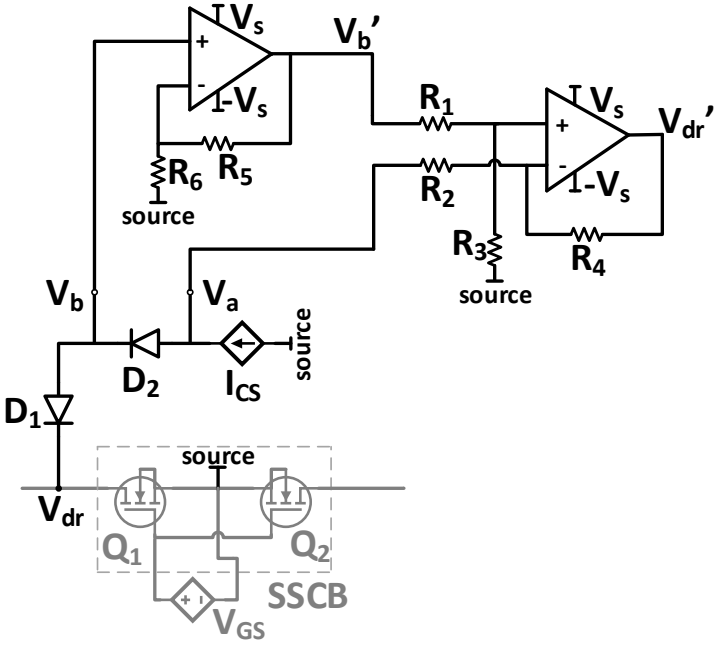


Figure 3.14: Configuration of Operational Amplifiers for the V_{DS} Measurement

Therefore, V_{dr}' is the representation of the V_{dr} signal measured by the designed detection circuit. As the detection circuit's components and the corresponding signals use the common source voltage as the reference, V_{dr}' is analogous to the V_{DS} voltage signal. The resistor ratio between R_4 and R_2 in equation (3.15) can also be utilized to provide a differential gain.

Apart from D_1 and D_2 having similar characteristics, the Op-Amps should also have excellent measurement accuracy to ensure precise V_{DS} measurements. For this purpose, an Op-Amp with extremely low noise and distortion characteristics is required. A suitable candidate is the OP275 Op-Amp produced by Analog Devices [53]. It can attain low noise performance levels. In addition, its other characteristics such as slew rate, bandwidth and CMRR also have sufficient values.

Similar to the designed V_L detection circuit's output voltage signal in the previous section, the measured V_{DS} signal (V_{dr}') also has to be input to a microcontroller. The reason is to process the measured signal to determine if a fault is detected and then if necessary, to initiate appropriate protective action. However, the V_{dr}' signal in figure 3.14 cannot be directly connected to a microcontroller. This is because the V_{dr}' signal and all the detection circuit components use the SSCB's common source voltage as the reference. Meanwhile, the microcontroller will be connected to the voltage ground of the distribution network. As a result, a direct connection will lead to inaccurate readings and can even have disastrous consequences for the microcontoller or the V_{DS} detection circuit. Therefore, the V_{dr}' must be galvanically isolated. The galvanic isolation can ensure the safe operation of the designed detection circuit and the microcontroller.

Final Detection Circuit Design

This subsection presents the complete design of the V_{DS} detection circuit. The galvanic isolation required to interface the measured V_{dr}' signal to a microcontroller can be provided via an optocoupler. This is shown in figure 3.15. The V_{dr}' is input to the optocoupler via a resistor R_{opto}. The galvanically isolated output (V_{OUT}) is measured across the resistor R_{OUT}. Now, V_{OUT} can be safely connected to a microcontroller after being digitized. V_{DD} represents an isolated power supply with the network ground as its reference. R_{opto} is required to limit the current flowing into the optocoupler while the value of R_{OUT} determines the V_{OUT} magnitude. Hence, R_{OUT} can be selected such that V_{OUT} remains within the 3.3V safe limit of a microcontroller.

In order to not undermine the detection speed of the designed circuit a high speed optocoupler is necessary. The optocoupler should have extremely short rise and fall times. The 6N136 optocoupler manufactured by Vishay Intertechnology is a good alternative. Its output has a typical rise time of 0.2μs [54]. This extra time delay can be deemed satisfactory and within limits.

Moreover, the input photodiode of the optocoupler becomes forward biased only when the voltage across it is larger than its forward voltage drop (V_F). For the 6N136 optocoupler, V_F is 1.3V [54]. Therefore, for fault detection to be completed via the designed circuit, V_{dr}' must be larger than V_F. This can be ensured by setting a maximum value of the current flowing in the distribution line for which the SSCB should not trip. The corresponding V_{dr}' value should be slightly lower than V_F.

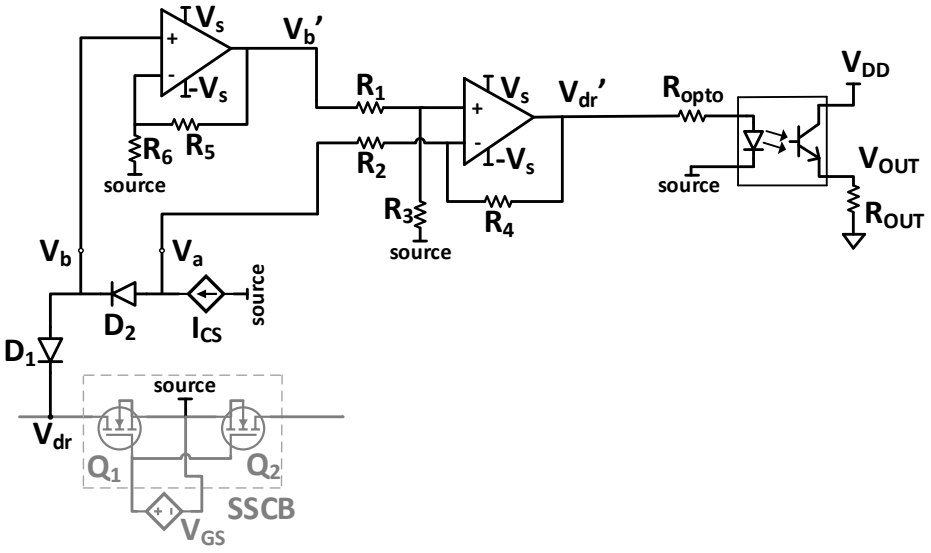


Figure 3.15: Complete Design of the V_{DS} Detection Circuit

This will make certain that V_{OUT} is zero and a fault condition is not detected by the microcontroller. However, if the distribution line's current increases beyond the maximum allowed magnitude, insinuating the occurrence of a fault, the measured V_{dr}' signal will increase beyond V_F. As a result, the optocoupler will be activated and V_{OUT} will rise. Consequently, this will enable the microcontroller to execute the required protection action.

Hence, the rise of the V_{OUT} signal becomes the detection circuit's indication of a fault being detected. The rise is triggered when the V_{dr}' signal forward biases the optocoupler's input photodiode. As shown in equation (3.15), the differential amplifier's gain $\left(\frac{R_4}{R_2}\right)$ can be utilized if necessary, to amplify the measured V_{dr}' signal such that it is capable of activating the optocoupler.

3.3.3. Simulation Results

This subsection presents some simulation results of the final designed V_{DS} detection circuit. These results provide the basis to evaluate the performance of the detection circuit. For this purpose, the DC distribution line's model within an LVDC network developed in section 3.2.4 is used. This model is repeated again in figure 3.16 along with the designed V_{DS} detection circuit. The box in figure 3.16 represents the complete detection circuit of figure 3.15. Meanwhile, the arrows depict the connections of the protective diode D_1 and of the SSCB's common source terminal to form the reference voltage for the detection circuit.

Next, a fault was simulated by closing SW_f in figure 3.16. However, in this case R_f has a larger value as compared to the fault condition in section 3.2.4. This was done to restrict the current from rising to extremely large values. The important circuit parameters of the simulation are listed in table 3.3.

V_{DC} (V)	C_{DC} (μF)	V_{GS} (V)	Q_1,Q_2	R_{DS} (mΩ)	R_{Load} (Ω)	R_f (Ω)
350	750	15	C3M0030090K	28 [5]	80	15

Table 3.3: Circuit Parameters for the Simulation Results Shown in Figure 3.7

Due to the higher fault resistance, it is uncertain if the fault will be detected via the V_L detection circuit. Nonetheless, the designed V_{DS} detection circuit should be capable of detecting these types of faults.

Figure 3.17 shows the line current and the corresponding V_{DS} voltage across MOSFET Q_1. The simulated fault occurs at 12μs. As expected, the line current increases rapidly after the fault. The faulted distribution line's current settles quickly however, at a lower magnitude as compared to the line current in figure 3.7. Moreover, figure 3.17 shows a sudden dip in the V_{DS} voltage immediately after the fault is simulated. The voltage dip can be explained due to the sudden change in the potential difference between the common source voltage of the SSCB MOSFETs and the fault location. Due to the immediate fault, the common source voltage momentarily becomes larger than the voltage at the fault location. However, the potential difference quickly decreases and soon V_{DS} increases as a result

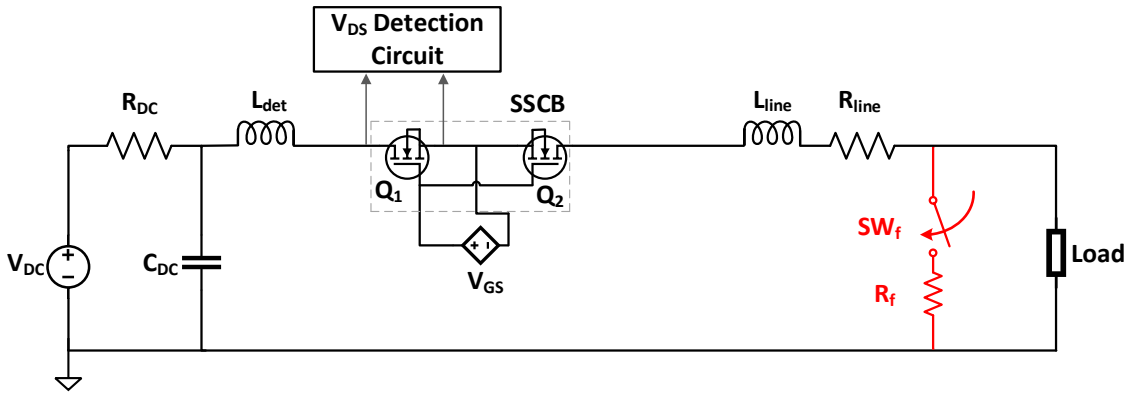


Figure 3.16: DC Distribution Line Model and the V_{DS} Detection Circuit

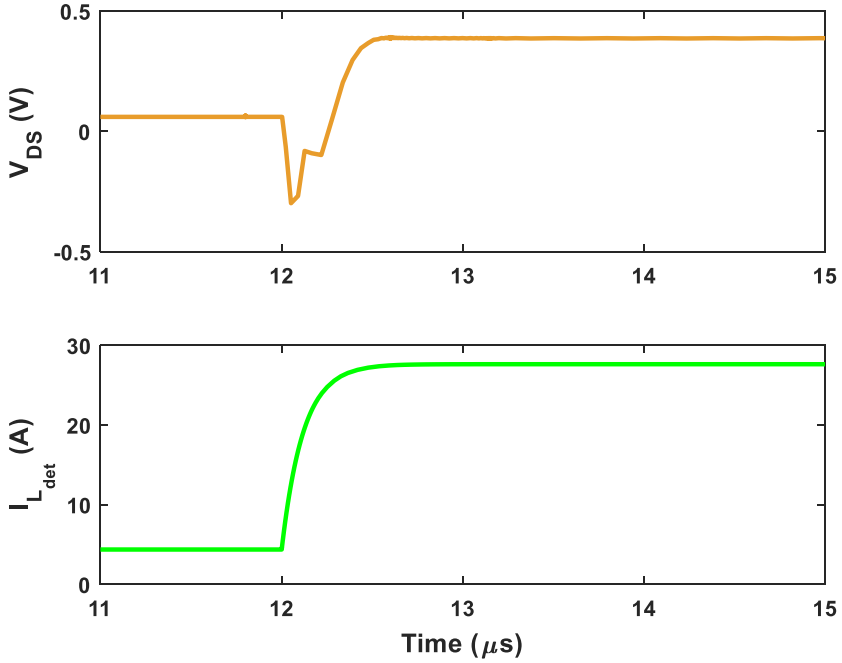


Figure 3.17: Distribution Line's Current and the Corresponding V_{DS} Voltage Across SSCB MOSFET Q_1

of the larger fault current flowing in the distribution line. In addition, two MOSFETS in parallel were used to represent both Q_1 and Q_2 (total of 4 in the SSCB) for the results of figure 3.17. Hence, in the DC transmission line's model Q_1, Q_2 have an equivalent R_{DS} of 14 mΩ each. Therefore, according to equation (2.8), the values of the V_{DS} voltage in figure 3.17 are appropriate.

Figure 3.18 below shows the measured voltage signals V_{dr}' (light blue) and V_{OUT} (purple) of the designed detection circuit corresponding to the V_{DS} voltage across Q_1. The measured V_{dr}' signal via the detection circuit follows the V_{DS} waveform extremely well. The Op-Amps used exhibit a quick response to changes in the V_{DS} signal after fault occurrence. Hence, the detection circuit does not introduce any extra time delays and is capable of fast fault detection. Moreover, the Op-Amps are also able to reject some of the noise observed in the V_{DS} waveform after fault occurrence to a great extent. This demonstrates the excellent low noise and distortion performance of the selected OP275 Op-Amps. As a result, a smooth and fast rise in the V_{dr}' signal is observed. From figure 3.18 it is evident that the differential amplifier of the detection circuit (figure 3.15) also provides a gain to the measured V_{DS} signal. As mentioned previously, the gain is used to produce a sufficient input voltage across the optocoupler's photodiode so that it becomes forward biased in the event of a fault occurring in the distribution line. The gain approximately equals 5 to ensure the photodiode's forward voltage of 1.3V is fulfilled [54]. A large gain was designed due to the low R_{DS} of the SSCB MOSFETs, consequently resulting in the low observed V_{DS} voltage.

Furthermore, the optocoupler's output (V_{OUT}) is zero before the fault is simulated in the distribution line. This verifies that the optocoupler's photodiode is off as V_{dr}' is lower than its forward biasing voltage. After V_{dr}' increases beyond the forward voltage, V_{OUT} measured across R_{OUT} begins to increase. Figure 3.18 also verifies the 6N136 optocoupler's rise time. It is approximately 0.3μs which is judged to be good enough. Next, V_{OUT} settles at a value that is within the safe limits for a microcontroller. Therefore, now a microcontroller can be safely connected without issues concerning grounding or the input voltage being too large. Thereby, allowing fault detection to be confirmed and the required protection action to be executed.

The detection circuit's component values to obtain the results of figure 3.18 are provided in table 3.4. From these values, the differential amplifier's gain can be precisely determined. Resistors R_5 and

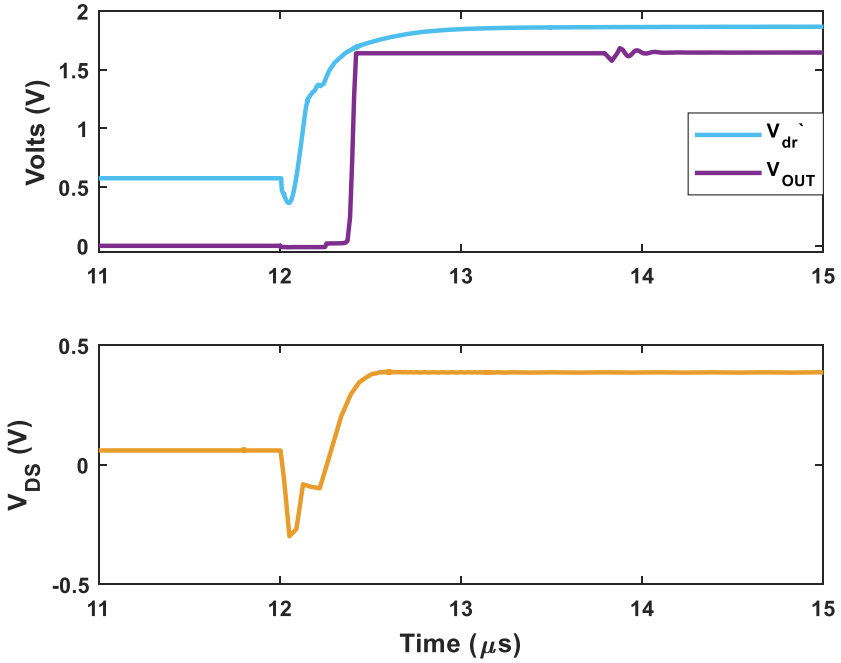


Figure 3.18: MOSFET Q_1's V_{DS} Voltage and the Corresponding Measured Signals of the V_{DS} Detection Circuit

R_6 of figure 3.15 have equal values to double the V_b voltage signal as required in equations (3.13) and (3.14). R_{opto} is used to limit the input current of the optocoupler's photodiode in order to prevent it from malfunctioning.

R_5 (kΩ)	R_6 (kΩ)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	R_4 (kΩ)	R_{opto} (kΩ)	R_{OUT} (kΩ)
2	2	1.5	1.5	7.6	7.6	0.01	0.25

Table 3.4: Component Values of the V_{DS} Detection Circuit for the Results of Figure 3.18

The results of figure 3.18 confirm that the design of the V_{DS} fault detection circuit is capable of accurate measurements and fast fault detection.

3.4. Design of the Junction Temperature Adjustment Circuit

The semiconductor devices (MOSFET/IGBT) of the SSCB operate in the normally-on configuration. Their on resistance was utilized in the previous section for fault detection by designing a V_{DS} measurement circuit. The designed circuit's output is directly dependent on the actual V_{DS} voltage across a particular SSCB MOSFET. Effectively, V_{DS} is dependent on the product of the on-resistance (R_{DS}) and the current flowing in the DC distribution line. Ideally, R_{DS} should have a constant value. However, this is not true. The value is a function of various external factors; the most dominant are the gate to source voltage (V_{GS}) and the junction temperature (T_j). The variation of R_{DS} as a function of V_{GS} can be minimized by ensuring that V_{GS} is kept constant at an adequate value. However, it is extremely difficult to control the T_j of the semiconductor device while in operation. As a result, variations in T_j can occur, consequently causing variations in the R_{DS} value.

Figure 3.19 shows the variation in R_{DS} as a function of T_j for two types of MOSFET technologies, Silicon Carbide (SiC) and Silicon (Si). The SiC MOSFET (C3M0030090K) has less variation in its R_{DS} as compared to the Si MOSFET (IPW65R019C7). The Si MOSFET's R_{DS} almost doubles when T_j increases from its nominal value of 25°C to 100°C. The SiC MOSFET's R_{DS} at the nominal T_j of 25°C is higher than the Si MOSFET. However, the increase in the SiC MOSFET's R_{DS} in the optimum T_j

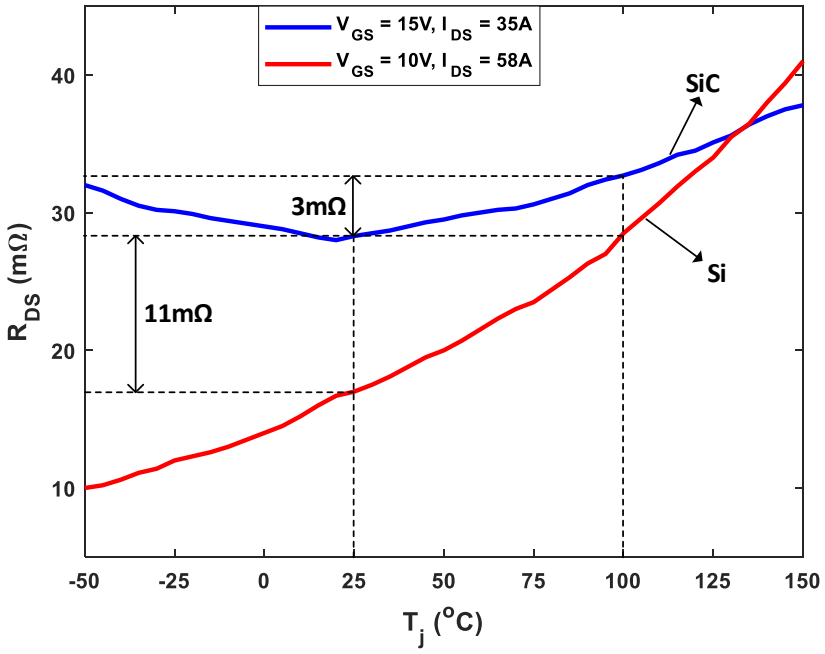


Figure 3.19: R_{DS} as a Function of T_j for SiC MOSFET C3M0030090K and Si MOSFET IPW65R019C7 [5], [6]

operating range (25-100°C) is less. Beyond the boundaries of this range, R_{DS} shows a higher variation.

The increase in T_j can lead to unfavourable circumstances for the V_{DS} based fault detection circuit. A large load demand in the LVDC network will cause higher currents flowing in the DC distribution lines. Higher currents will lead to greater power dissipation in the SSCB MOSFETs. This will further increase T_j and thus also the R_{DS} value. As a result, the V_{DS} voltage will increase for the same amount of current flowing in the distribution line. Consequently, the measured V_{DS} voltage via the designed detection circuit (V_{dr}') will also increase. The increased V_{dr}' can lead to a false fault detection and hence, the unnecessary interruption in the power flow of the LVDC network. Therefore, the increase in T_j of the SSCB's devices can lead to spurious fault detections even when the line currents are within the nominal ratings and there is no fault in the distribution lines. In addition, an LVDC network operating in higher ambient temperatures can also result in unnecessary tripping.

Therefore, for the V_{DS} based fault detection method to operate reliably under all load conditions and ambient temperatures, the adverse effect of increase in V_{DS} due to R_{DS} needs to be countered. However, little can be done about the increasing T_j and the corresponding increase in the measured V_{dr}' signal. Hence, a solution is required that measures the amount of increase in R_{DS} and can subsequently shift the V_{dr}' signal to a lower level by an amount that corresponds to the increase in R_{DS}. This solution can be realized in the form of a supplemental circuit to the original designed V_{DS} detection circuit of figure 3.15.

3.4.1. Design of the Supplemental Level Shifting Circuit

The major requirement of the supplemental circuit is to be able to measure the amount of change in R_{DS} as a function of T_j. This is possible by using a temperature measurement device to monitor the case temperature (T_{case}) of the SSCB MOSFETs. A negative temperature coefficient (NTC) thermistor is a suitable option. The resistance of a thermistor varies as a function of the ambient temperature. Therefore, a thermistor can be fixed on the case or on the heatsink of an SSCB MOSFET to measure the temperature. The B57703M thermistor manufactured by TDK is a good choice due to its high accuracy and a ring like structure that allows easy mounting on a semiconuctor device [55]. Although the thermistor will measure T_{case}, T_j can be estimated via this measurement. Different estimation

techniques for T_j have been described in [36], [37].

As T_{case} varies, the thermistor's resistance will also change. Due to the NTC nature of the B57703M thermistor, the resistance decreases with increasing temperature. This property can be utilized to produce an output voltage that varies linearly with the temperature. Hence, the supplemental circuit needs to be designed such that its output voltage varies as a function of the thermistor resistance and thus consequently, the case temperature. As T_{case} is directly dependent on R_{DS} and T_j, the output voltage is effectively controlled by any variation in these two MOSFET parameters. This output voltage can be interfaced with the measured V_{dr}' signal enabling its magnitude to be shifted, if necessary.

The supplemental circuit can be realized via an Op-Amp and a thermistor. Its design is shown in figure 3.20. The NTC thermistor (R_{NTC}) is connected in series with a simple resistor R_{ref} to form a voltage divider. Resistors R_{th1} and R_{th2} also form another voltage divider while R_f and R_g are used to provide a voltage gain. The circuit uses the Op-Amp in an inverting configuration with a non-inverting voltage reference. This voltage reference on the non-inverting pin is simply set according to the ratio between R_{th1}, R_{th2} and is expressed below

$$V_+ = V_s\left(\frac{R_{th2}}{R_{th1} + R_{th2}}\right), \tag{3.16}$$

where V_+ is the voltage on the non-inverting pin. By appropriately selecting the values of the circuit's auxiliary resistors it can be ensured that the output voltage (V_{sh}) of the supplemental level shifting circuit is always negative. A negative output is required in order to compensate for the increase in the V_{dr}' signal due to the increased R_{DS}. V_{sh} can be calculated via the Op-Amp's equation below

$$V_{sh} = V_s\left[\left(1 + \frac{R_f}{R_g}\right)\left(\frac{R_{th2}}{R_{th1} + R_{th2}}\right) - \left(\frac{R_f}{R_g}\right)\left(\frac{R_{ref}}{R_{NTC} + R_{ref}}\right)\right]. \tag{3.17}$$

Moreover, the position of the thermistor R_{NTC} in the circuit's design in figure 3.20 is a strategic one. When the SSCB MOSFET's T_{case} increases (indicating an increase in the R_{DS}), R_{NTC} subsequently decreases. As a result, the voltage across R_{ref} increases. According to equation (3.17), V_{sh} will decrease and become more negative.

At nominal values of R_{DS}, V_{sh} will be designed to have a small negative value. In addition, the V_{dr}' signal accurately represents the V_{DS} voltage according to the nominal R_{DS} value. However, as R_{DS} increases, V_{dr}' will increase and V_{sh} will become more and more negative. By adding the two voltage signals together, the original V_{dr}' signal's level can be appropriately shifted to a lower value to minimize the adverse effect of the increase in R_{DS}. In this way, the LVDC network will be able to operate under high load conditions and consequently, high SSCB module temperatures without the fear of unnecessary tripping occurring via the V_{DS} based fault detection circuit.

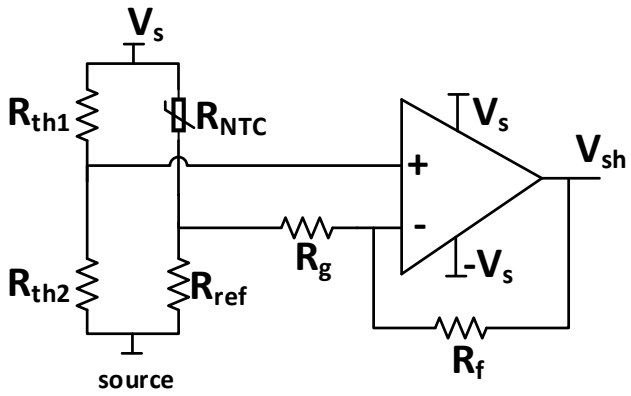


Figure 3.20: Regular Operational Amplifier Used To Design the Supplemental Level Shifting Circuit

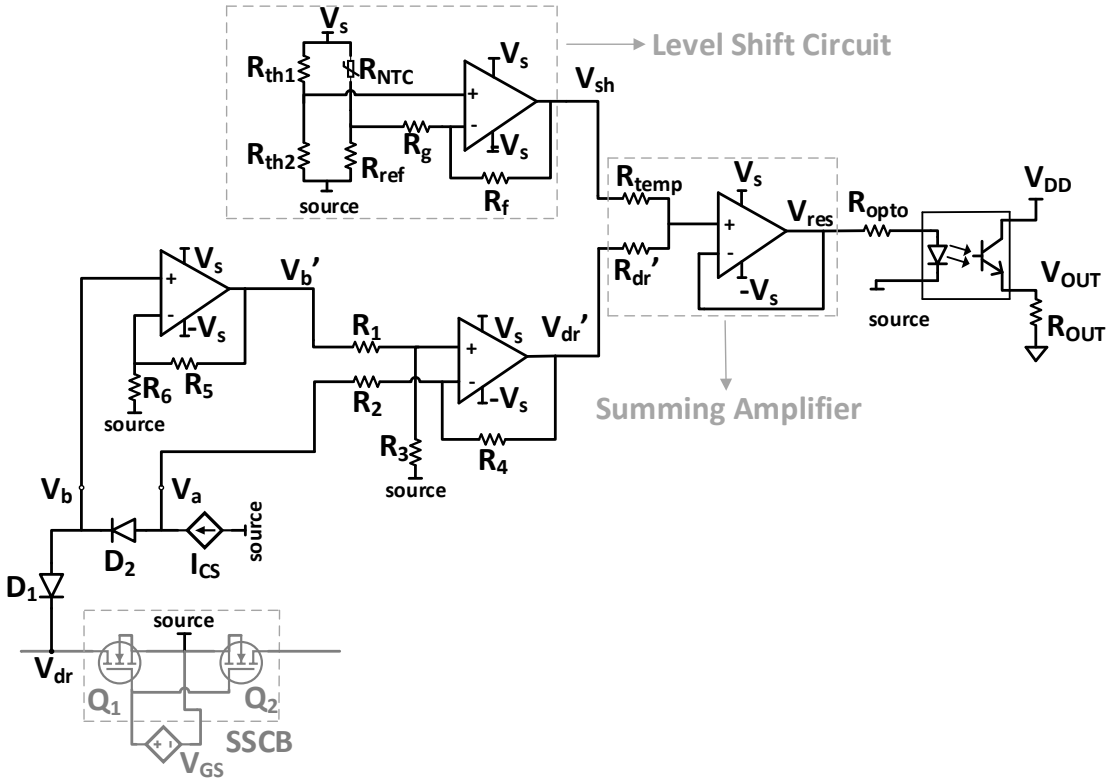


Figure 3.21: V_{DS} Detection Circuit With the Supplemental Level Shift Circuit and the Summing Amplifier

The output voltage V_{sh} of the supplemental circuit needs to be arithmetically summed with the V_{dr}' signal. The resultant signal will become the input to the optocoupler. The summation can be done via an Op-Amp configured as a summing amplifier. The complete V_{DS} detection circuit along with the level shifting circuit and the summing amplifier is shown in figure 3.21. V_{dr}' and V_{sh} are the inputs on the non-inverting terminal of the summing amplifier. As the summing amplifier's only purpose is to add the two input voltage signals together, it is configured as a voltage follower. A voltage follower has unity gain, thus its output equals the input voltage. According to the summing amplifier's equation V_{res} is given by

$$V_{\text{res}} = \left[\left(\frac{R_{\text{temp}}}{R_{\text{temp}} + R_{\text{dr}}'}\right)V_{\text{dr}}' + \left(\frac{R_{\text{dr}}'}{R_{\text{temp}} + R_{\text{dr}}'}\right)V_{\text{temp}}\right]. \tag{3.18}$$

The above equation illustrates that the resistors (R_{temp}, R_{dr}) determine the contribution of each signal (V_{dr}', V_{sh}) towards V_{res}. Therefore, R_{dr}' R_{temp} can be considered as weights of the two input signals being added. A particular signal can have a greater contribution in V_{res}'s value by appropriately choosing the resistor values. Moreover, figure 3.21 shows that V_{res} is the input voltage of the optocoupler. With the supplemental level shift circuit included in the design, the magnitude of V_{res} now determines the activation of the optocoupler, rather than V_{dr}' in figure 3.15.

3.4.2. Simulation Results

This subsection shows some results of the level shift circuit working in tandem with the V_{DS} detection circuit. The DC distribution line model of figure 3.6 is used again. Moreover, a nominal current of 20A for the DC distribution line is assumed. This implies that current magnitudes larger than this value should be identified as a fault via the designed V_L or V_{DS} detection circuits. Otherwise, the detection circuits should not interrupt the operation of the DC distribution line.

To demonstrate the working of the level shift circuit, a load step was simulated in the DC distribution line's model. The step is an increase in the load, thus a higher current is demanded. Figure 3.22

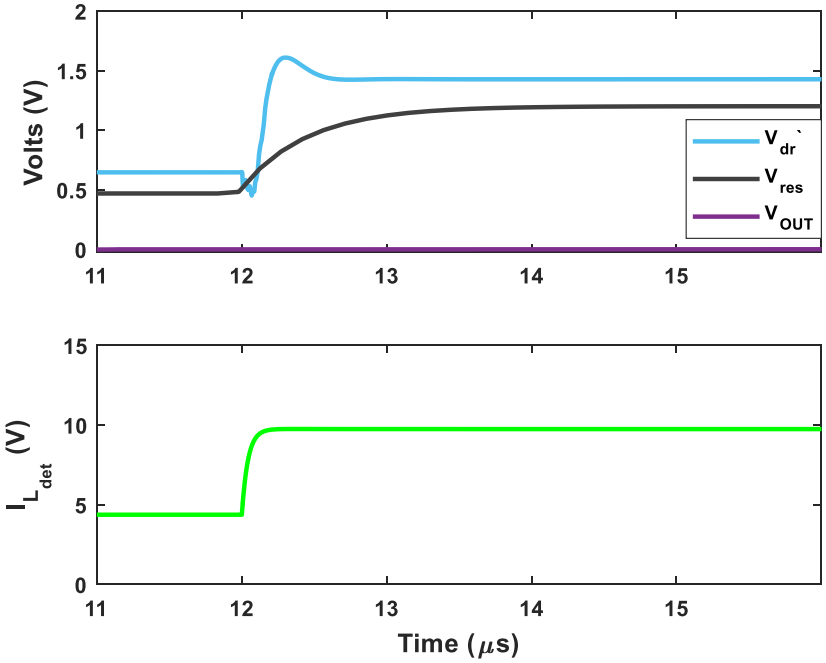


Figure 3.22: DC Distribution Line's Current After a Load Step and the Corresponding Detection Circuit Signals

shows the distribution line's current and some corresponding signals of the V_{DS} detection circuit. The distribution line's SSCB is assumed to be operating under high T_j conditions. As seen in the figure, after the load step (at 12μs) the distribution line's current magnitude has doubled. The corresponding V_{dr}' signal (light blue) rises to a steady state value of around 1.4V. This voltage is greater than the forward biasing voltage of the optocoupler's photodiode (1.3V) [54]. Consequently, the higher resultant R_{DS} due to a high T_j would have activated the optocoupler in figure 3.15. This would have caused an interruption of the power flow in the distribution line even when the current magnitude is lower than the nominal rated value.

The results of figure 3.22 correspond to the complete detection circuit shown in figure 3.21. Therefore, the effect of the supplementary level shifting circuit is also illustrated. V_{res} (gray) shows that its magnitude has been adjusted for the effect of the increase in R_{DS}. After the load step its magnitude remains smaller than the optocoupler's forward biasing voltage. Hence, V_{OUT} (purple) stays at zero because the optocoupler does not get activated. Therefore, due to adjustment via the level shift circuit the distribution line can operate without tripping in the LVDC network even when the junction temperatures of the SSCB MOSFETs are fairly high.

Moreover, figure 3.23 shows the operation of the V_{DS} detection and the level shifting circuits when a fault occurs in a particular DC distribution line. After the fault, the V_{dr}' increases rapidly. Consequently, V_{res} also rises. As expected, the magnitude of V_{dr}' is larger than it was in figure 3.22. As the steady state value of V_{res} is higher than 1.3 V, the optocoupler becomes forward biased. This confirms the detection of the fault. In figure 3.23, it can be seen that after fault occurrence the instant when the V_{OUT} signal begins to rise is slightly delayed as compared to that in figure 3.18. This is because the optocoupler is now activated via the V_{res} signal instead of the V_{dr}' signal. Hence, V_{OUT} begins to rise only when V_{res} has surpassed the photodiode's forward biasing voltage.

The amount of shift in figure 3.23 between the V_{dr}' and V_{res} signals is slightly larger than in figure 3.22. This is due to the larger line current in the latter figure. Hence, there was a larger increase in the actual V_{DS} waveform. Generally, the amount of shift should be equivalent to the increase in the V_{dr}' signal caused by the increase in the R_{DS} value. However, the increase in the V_{dr}' signal is dependent on several factors. The most notable of these are the distribution line current, instantaneous T_j, nominal

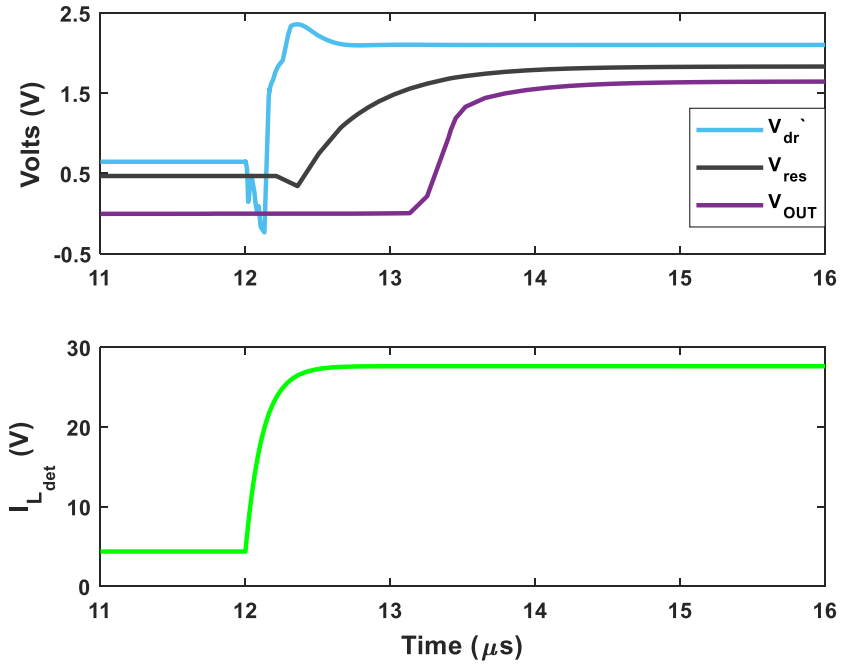


Figure 3.23: DC Distribution Line's Current After a Fault and the Corresponding Detection Circuit Signals

R_{DS} value and the type of MOSFET technology. Numerous varying factors can make it difficult to always shift the signal by the appropriate amount. Therefore, a close estimation of the amount of shift required compared to the actual change in the V_{dr}' signal due to the change in R_{DS} is good enough.

3.5. Summary

In this chapter the most suitable fault detection methods in an LVDC network were identified. The choice was made based on the speed of operation. As a result, the V_L based fault detection method was selected. However, in certain scenarios such as a high impedance fault or a distant fault, the V_L based method can prove to be uncertain. Therefore, to maximize the fault detection capability another detection method reliant on the voltage measured across the distribution line SSCB's semiconductor device is also selected. This method was named the V_{DS} based fault detection method.

Furthermore, the circuit design of these fault detection circuits is then introduced. The major requirements of each fault detection method are considered in the circuit design. Next, the finalized circuit designs of both methods are developed and their performance evaluated via simulations. The simulation results are also used to interpret the implications of a fault on the designed detection circuits.

The effect of an increase in the junction temperature of the SSCB devices on the V_{DS} based fault detection method is examined. Higher junction temperatures tend to increase the on-state resistance of the SSCB's semiconductor devices. This in turn causes the measured V_{DS} voltage to be higher as well resulting in unnecessary interruptions in the power flow of the LVDC network. Hence, a solution to counter the adverse effects of the junction temperature on the V_{DS} detection circuit is provided in the form of a supplemental circuit called the level shifting circuit.

4

Fault Isolation

This chapter talks about isolation of the fault in the DC distribution line after it has been detected. Some simulation results of the detection circuit signals that lead to fault isolation are included. The results of the relevant current and voltage waveforms of the DC distribution line are also shown, followed by their interpretation and some key insights that can be drawn.

4.1. Fault Isolation Subsequent to Detection

The previous chapter focused on the circuit design of the two selected fault detection methods. The design of the detection circuits enabled the fast measurement of the relevant signals used by each method in determining the occurrence of a fault. The measurement speed was critical due to the extremely fast anticipated rise in the line currents of a DC network.

After fault detection, the faulted distribution line(s) must be isolated from the rest of the LVDC network. This has to be done via the particular SSCB of the distribution line. The SSCB's semiconductor devices are controlled via a gate driver circuit. The gate driver's input signal is provided by the specific microcontroller used for processing the output signals of the two designed fault detection circuits. The connections between the detection circuits, microcontroller, gate driver and the SSCB are illustrated in figure 4.1 in the form of a flow chart on top of the DC distribution line's model. Moreover, for a fault to be isolated subsequent to detection, the microcontroller should invert the logic of the gate driver's input signal. This will result in the gate driver actively switching off the SSCB's devices. In order to not undermine the quick identification of faults via the detection circuits, fault isolation should also be executed quickly. As SSCBs can operate within a few microseconds, the signal processing speeds of the microcontroller and gate driver will largely determine the speed of fault isolation.

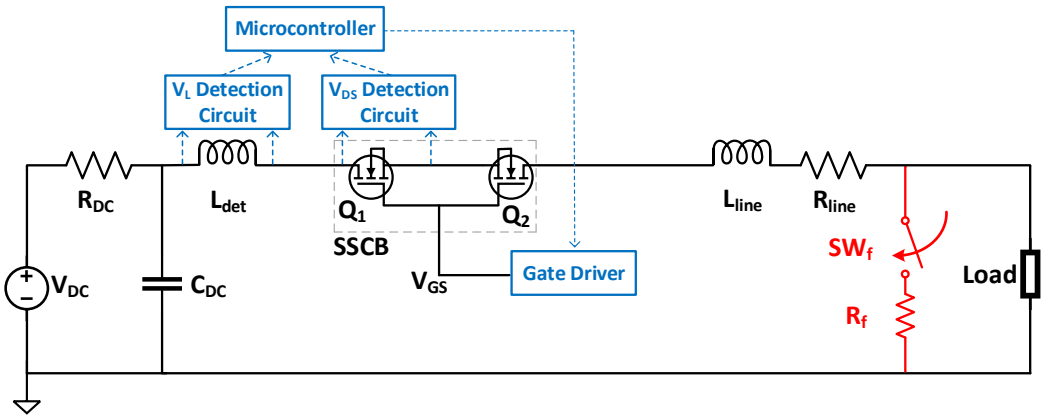


Figure 4.1: Microcontroller and Gate Driver Interfaced with the Detection Circuits and the SSCB

Several microcontrollers are capable of extremely fast processing speeds. In fact, the TMS320F28379D microcontroller manufactured by Texas Instruments has a signal processing speed of up to 200 MHz and an ADC conversion time of about 300 ns [56]. In addition, gate drivers with low propagation and switching delays for the output voltage are also commercially available. The UCC21540 and ADuM4135 gate driver products have mentioned output voltage switching delays of between 40-55 ns [57], [58]. As a result, these products can guarantee the fast isolation of a fault after its detection.

4.1.1. Simulation Results

This subsection shows some simulation results of the complete fault detection and protection system. The model shown in figure 4.1 is used. Similar to previous models, the switch SW_f simulates a fault with resistance R_f. However, as the detection circuit outputs are now interfaced to the SSCB's gate driver, they are capable of interrupting the power flow in the DC distribution line.

For simplicity of the simulation, the microcontroller block is replaced by an analog comparator. Its purpose in the simulation is to confirm fault detection by comparing the detection circuit outputs to a threshold value. Moreover, the supplementary level shift circuit discussed in the previous section is also not considered to obtain the results.

Table 4.1 lists the circuit parameters of the DC distribution line model. They are similar to the ones in table 3.1 and are repeated below for convenience.

V_{DC} (V)	C_{DC} (μF)	L_{det} (μH)	L_{line} (μH)	R_{line} (mΩ)	R_{Load} (Ω)	R_f (Ω)	Q_1,Q_2
350	750	1.5	2.4	1.6	80	1	C3M0030090K

Table 4.1: Circuit Parameters for the Simulation Results Shown In Figures 4.2 and 4.3

Figure 4.2 shows the signal waveforms of the simulated fault. SW_f is closed at 12 μs. The V_L detection circuit's output signal (V_{OUT-L}), the corresponding fault identification threshold voltage (V_{th}) and V_{GS} waveforms are illustrated.

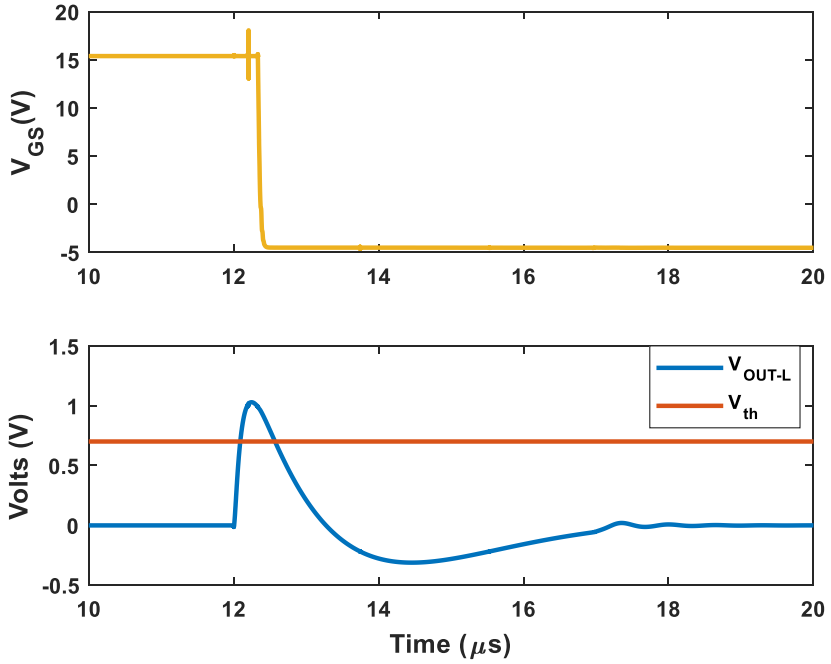


Figure 4.2: V_L Detection Circuit's Output Voltage and the V_{GS} Waveform of the SSCB Illustrating Fault Isolation

Before the fault, V_{OUT-L} is zero and lower than V_{th}. Therefore, V_{GS} is high and the SSCB permits the standard operation of the distribution line in the LVDC network. However, immediately after the

fault $V_{OUT\text{-}L}$'s magnitude increases rapidly. Due to the low impedance of the fault and being in close vicinity of L_{det} (a low L_{line} value in table 4.1), $V_{OUT\text{-}L}$ rises beyond the set V_{th}. This triggers the analog comparator (used in simulation instead of a microcontroller) to confirm fault detection. Consequently, the comparator sends a trip signal to the SSCB's gate driver resulting in the V_{GS} signal being pulled low. The signal is pulled down to a value of approximately -5 V. This is to ensure that any type of unwanted ringing or noise on the SSCB device's gate terminal does not cause the V_{GS} signal to accidentally increase beyond the device's gate threshold voltage. Moreover, from figure 4.2 the propagation delay and transition speed of the V_{GS} signal is also evident. This shows that the gate driver is capable of quickly turning off the SSCB devices after fault detection has been confirmed.

Figure 4.3 illustrates the V_{DS} waveform across an SSCB's MOSFET, its channel current (I_{DS}), the distribution line current (I_L) and also the V_{GS} waveform. I_{DS} is measured at the drain of the MOSFET Q_1 in figure 4.1. As expected, before fault occurrence I_{DS} is equivalent to I_L. Even after the fault, the two current waveforms rise at the same rate and are identical. When the V_{GS} signal is pulled low (subsequent to fault detection), the I_{DS} waveform rapidly falls to zero as a consequence. This exhibits that the SSCB MOSFETs have been turned off and stopped conducting. However, I_L still increases for a short duration, has a peak and then begins to fall to zero. This is because the line current has commutated from the SSCB to the snubber circuit connected across the MOSFET (although not shown in figure 4.1). The current charges the snubber circuit's capacitor and transfers the energy that was stored in the L_{det} inductor. Furthermore, after the SSCB MOSFETs have stopped conducting the V_{DS} voltage across Q_1 begins to rise. Q_1 now blocks the forward voltage which eventually rises up to V_{DC}. The energy stored in the snubber circuit's capacitor is dissipated in order to prevent a large V_{DS} voltage spike.

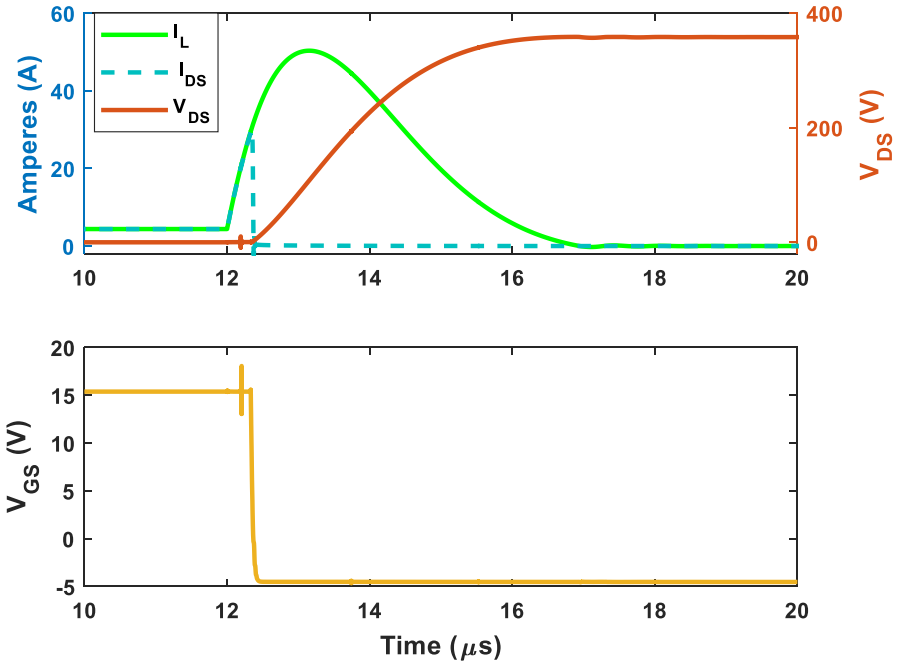


Figure 4.3: The SSCB's V_{GS}, V_{DS}, I_{DS} Waveforms and I_L Illustrating Fault Isolation

In figure 4.2, after fault isolation the $V_{OUT\text{-}L}$ waveform falls rapidly and goes below zero. The negative voltage coincides with the time when I_L begins to fall to zero after its peak in figure 4.3. The decreasing I_L results in a negative $\frac{di}{dt}$, causing V_L across L_{det} to also be negative and consequently, $V_{OUT\text{-}L}$. Moreover, figures 4.2 and 4.3 indicate that fault detection and isolation is indeed fast. The simulation results show that when the fault is identified via the V_L detection circuit, it is isolated within 500 ns. I_L also does not increase to extremely large values and falls to zero within 5 μs after fault occurrence.

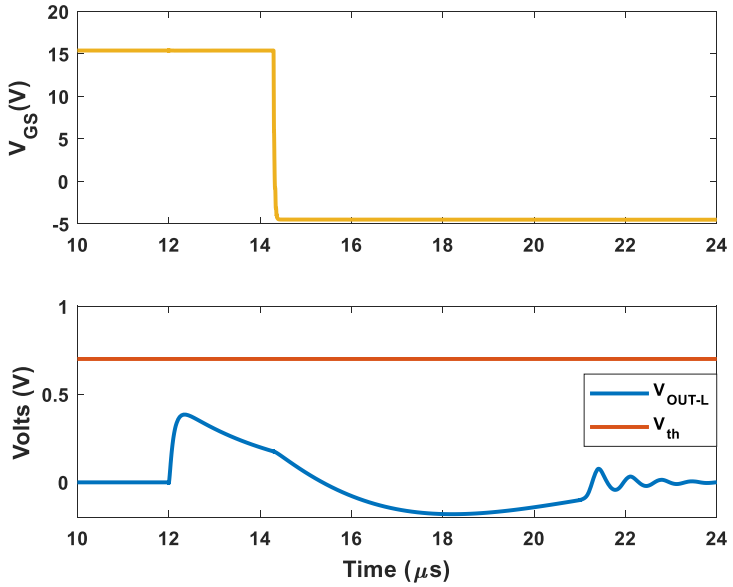


Figure 4.4: V_L Detection Circuit's Output Voltage and the V_{GS} Waveform of the SSCB With a Larger Line Inductance

V_{DC} (V)	C_{DC} (μF)	L_{det} (μH)	L_{line} (μH)	R_{line} (mΩ)	R_{Load} (Ω)	R_f (Ω)	Q_1,Q_2
350	750	1.5	10	6.67	80	1	C3M0030090K

Table 4.2: Circuit Parameters for the Simulation Results Shown In Figures 4.4, 4.5 and 4.6

Furthermore, figure 4.4 shows the corresponding V_L detection circuit's signal waveforms for a fault that occurred at a greater distance from the L_{det} inductor. The circuit parameters are also shown in table 4.2. They are similar to those in table 4.1 except for L_{line} and R_{line}. The larger L_{line} and R_{line} values indicate that the fault location is farther away compared to the previous scenario. As seen in figure 4.4, the magnitude of V_{OUT-L} does not exceed the threshold voltage set for the confirmation of fault detection. Therefore, due to the larger L_{line} the fault cannot be identified via the V_L detection circuit. However, around 14 μs the V_{GS} waveform is pulled low, indicating that the SSCB has been opened and the fault isolated.

This implies that the fault must have been detected via the V_{DS} detection circuit. As the waveform of V_{OUT-L} remains below V_{th}, the fault is detected when the distribution line's current increases beyond a value that causes the V_{DS} detection circuit's optocoupler (figure 3.15) to be activated. This is shown via the specific waveforms in figure 4.5 below.

After the fault occurs at 12 μs, the V_{dr}' signal begins to rise due to the greater I_L flowing through the faulted distribution line. Due to the large L_{line}, the current rise is relatively slower and hence, also the rise of the V_{dr}' signal. Eventually, the V_{dr}' signal's magnitude increases beyond the optocoupler's forward voltage. Consequently, causing the optocoupler's output voltage (V_{OUT-DS}) to also rise. As the rise of the V_{OUT-DS} waveform already confirms fault detection, the comparator's threshold (used only in the simulation model) is set at a fairly low voltage value. Therefore, the rise of the V_{OUT-DS} signal immediately triggers the gate driver to pull down the V_{GS} signal of the SSCB. This results in the isolation of the fault via the V_{DS} based detection circuit.

After the V_{GS} signal is pulled low, the V_{DS} waveform across Q_1 begins to rise. Subsequently, the V_{DS} detection circuit's diode (D_1 in figure 3.15) used to protect the designed circuit from high voltages becomes reverse biased. Hence, the V_{dr}' signal begins to fall rapidly and settles at a negative value. This results in the optocoupler turning off and the fall of the V_{OUT-DS} waveform.

Figure 4.6 shows the V_{DS}, I_L, I_{DS} and also the V_{GS} waveforms for the simulated fault with the parameters of table 4.2. The waveforms are mostly similar to those in figure 4.3. However, the rate of

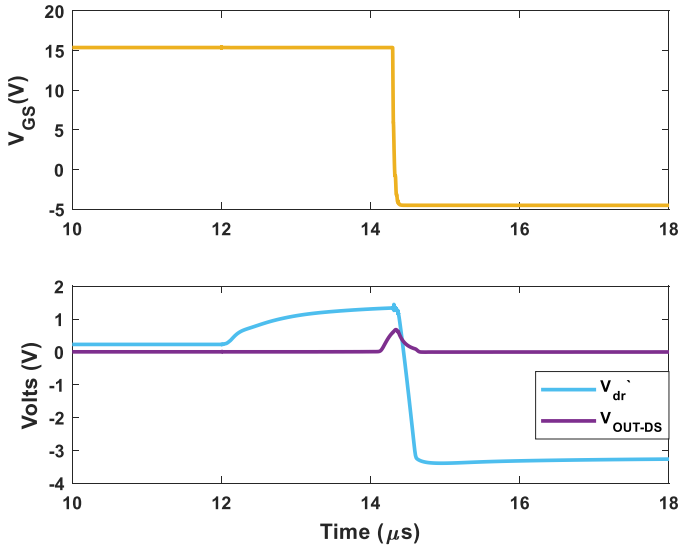


Figure 4.5: V_{DS} Detection Circuit's Output Voltage Signals and the V_{GS} Waveform of the SSCB Illustrating Fault Isolation

increase of I_L in figure 4.6 is slower than in figure 4.3. This is because of the larger value of L_{line} used in the simulation model. Consequently, after fault isolation I_L's decrease rate and the V_{DS} waveform's increase rate are also slower.

Figures 4.5 and 4.6 depict that fault identification and isolation via the V_{DS} detection circuit are achievable within 2.5 μs. Although the magnitude of the relevant signals (V_{dr}', V_{GS}) can change rapidly, the majority of this time is dependent on the speed of rise of the fault current in the distribution line. This in turn, depends on the location of the fault and thus the amount of L_{line} from the fault location to the SSCB.

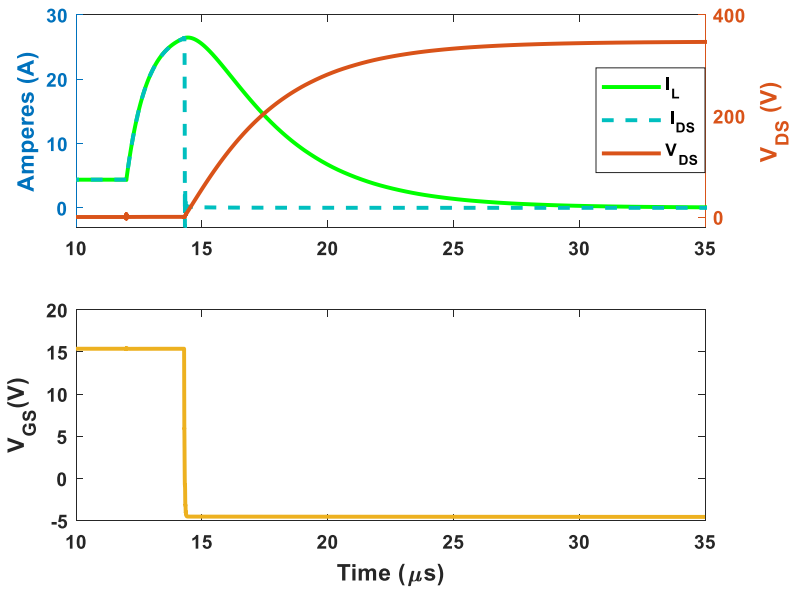


Figure 4.6: The SSCB's V_{GS}, V_{DS}, I_{DS} Waveforms and I_L Illustrating Fault Isolation With a Larger Line Inductance

4.1.2. Inferences From the Results

The simulation results in the previous subsection demonstrated that the amount of inductance of the distribution line from the fault location to the detection circuits has a major impact on the identification of a fault. As was seen, a fault with a larger L_{line} remained undetected via the V_L detection circuit.

The major reason is due to the low value of the L_{det} inductor compared to L_{line}. According to equation (3.6), the major share of the transient voltage after fault occurrence will be observed across L_{line} rather than L_{det}. Consequently, the V_{OUT-L} signal had a magnitude lower than V_{th}. A simple solution is to increase the value of the L_{det} inductor. This will ensure a higher transient voltage across L_{det} and subsequently, V_{OUT-L} can surpass the set V_{th} voltage even when L_{line} is high. However, a larger L_{det} inductor will store a greater amount of energy. Hence, after fault isolation more energy will have to be dissipated across the SSCB's snubber circuits. If the snubber circuit is not redesigned to dissipate the extra energy, it can have dangerous consequences for the SSCB. Large voltage spikes could be produced across the SSCB's device which could cause them to be permanently damaged. Therefore, increasing the value of the L_{det} inductor is not so straightforward. Hence, to be able to detect faults via the V_L based method in high L_{line} conditions, there exists a trade-off. This is between the selected value of L_{det} and the amount of energy allowed in the design to be dissipated by the SSCB's snubber circuit.

Furthermore, the total time required to isolate the fault after its occurrence can be used to assess the performance of the complete fault protection system. For the two distinct experimental results shown, these were about 0.5 μs and 2.5 μs. Even though the rate of increase of $\frac{di}{dt}$ in the distribution line is high after the fault, the current does not reach extremely large magnitudes. As a result, the safety of the LVDC network and its components can be assured. Hence, based on the reported fault isolation times and the current magnitudes, the overall performance of the protection system can be deemed to be fast and adequate.

The two experimental results assumed the same low fault impedance (R_f) but different L_{line} values (tables 4.1 and 4.2). The fault with the larger L_{line} value was detected via the V_{DS} detection circuit and required more time to be isolated from the rest of the LVDC network. Moreover, a high impedance fault occurring in a distribution line will also be identified via the V_{DS} detection circuit. However, it is not necessary that the high impedance fault's isolation will also require approximately 2.5 μs or even longer. This time is mostly dependent on the amount of L_{line} observed between the fault location and the SSCB. A high impedance fault occurring closer to the SSCB (a low L_{line}) will cause the V_{DS} detection circuit's output signals (V_{dr}', V_{OUT-DS}) to rise quicker, thereby enabling faster fault isolation.

4.2. Summary

In this chapter, the simulation results of fault isolation after detection were presented. The isolation of the fault and the corresponding waveforms when detected via each method, the V_L or V_{DS} were also shown. Next, some important conclusions were drawn from the results and used to judge the performance of the overall fault protection system.

5

Hardware Evaluation

This chapter presents the practical results of the operation of the designed fault detection circuits. First, the experimental setup and an SSCB prototype used in attaining the results are explained. This is followed by the relevant experimental waveforms. Based on the results achieved, the performance of the complete fault protection system is assessed.

5.1. The Experimental Setup

In order to validate the design of the fault detection circuits, a suitable practical setup was assembled. The setup is composed of various building blocks. In addition to the detection circuits, these are an SSCB prototype, gate driver and microcontroller circuits, DC power supply and appropriate measurement equipment. Printed circuit boards (PCB) were designed for the SSCB prototype, gate driver circuit and of course, for the designed V_L, V_{DS} fault detection circuits.

5.1.1. The SSCB Prototype and the Designed Detection Circuits PCB

The SSCB prototype was built with SiC MOSFETs (C3M0030090K). The design consists of a total of 8 MOSFETs. Therefore, the SSCB is made up of two columns (containing 4 parallel MOSFETs each) connected in an anti-series configuration. A larger number of MOSFETs in parallel are utilized to decrease the SSCB's on-state resistance and also increase the current carrying capability hence, the power rating. The prototype also includes the L_{det} inductor on the same PCB.

An image of the SSCB prototype and the additional required circuits is shown in figure 5.1. The additional circuits are mounted on top of the prototype. In the figure, the MOSFETs and the snubber circuits are not visible as they are placed on the bottom side of the prototype's PCB. A large heatsink (required for the MOSFETs) and the L_{det} inductors are visible. Moreover, in figure 5.1 the two round silver connections (close to the L_{det} inductors) on the PCB represent the terminals of the SSCB. These terminals are directly connected to the common drain points of the parallel MOSFETs. The dimensions are also included to provide an indication of the size of the entire SSCB prototype and the additional circuits.

Figure 5.1 suggests that the prototype's PCB is symmetrical. This is indeed true. The reason for this is to allow the bidirectional flow of current through the SSCB. Bidirectional power flows are expected to be integrated in future DC networks [26]. In an SSCB, this is possible due to the anti-series connection of the MOSFETs. The current flows through the drain to source channels of a parallel branch of MOSFETs and via the body diodes of the other branch and vice versa for the current flow in the other direction. As a result, two L_{det} inductors are also needed for bidirectional fault detection capability via the V_L measurement method. For this purpose, the physical layout of the SSCB prototype's PCB is important.

Furthermore, the paramount task of this research work, the PCB containing the various detection circuit components is mounted on top of the SSCB prototype. A separate PCB was designed especially for the fault detection circuits. This is done to have two different operating voltage levels on each PCB. The SSCB prototype's PCB operates at the nominal V_{DC} value while the detection circuit's components require a low signal voltage (up to 15V) for their operation. Hence, this type of a design can reduce

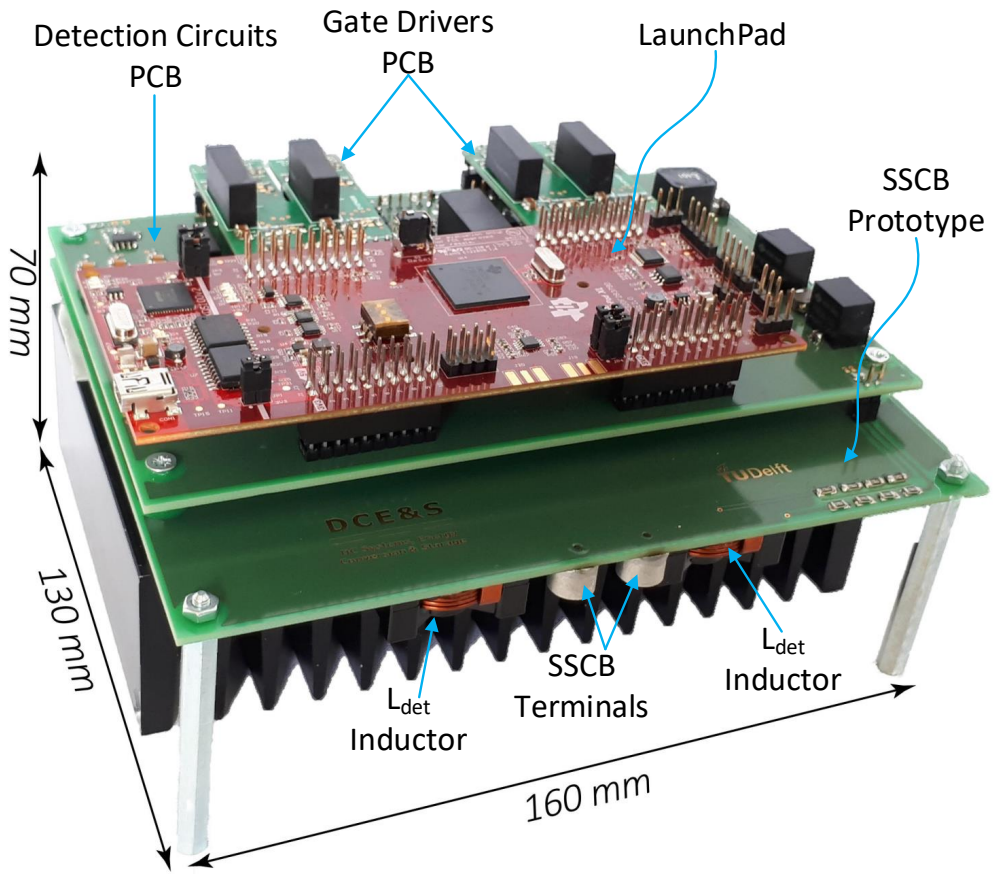


Figure 5.1: The SSCB Prototype

the conducted electromagnetic interference (EMI) noise between the components operating at different voltage levels. For the V_L detection circuit, only the isolation resistors are located on the SSCB prototype (seen in the bottom right in figure 5.1). Similarly, for the V_{DS} detection circuit, only the diode responsible to block the high voltage (across the SSCB MOSFETs) is on the prototype's PCB. The rest of the circuit components are placed on the detection circuits PCB.

Moreover, as the SSCB prototype is capable of operating bidirectionally, the detection circuits PCB contains two sets of the designed V_L and V_{DS} measurement circuits. One set of the V_{DS} detection circuit is connected across each parallel branch of the SSCB MOSFETs. Hence, depending on the current direction, one V_{DS} measurement set will always be able to detect a positive voltage and thus be capable of detecting a fault. Meanwhile, the inputs of the two differential amplifiers of the V_L detection sets are interchanged. Thus, in the event of a fault occurrence, the voltage after the isolation resistors will be positive across the input terminals of one of the two differential amplifiers. This is again determined by the direction of the current. Therefore, the detection circuits PCB is able to detect bidirectional faults.

Figure 5.1 also illustrates the gate driver PCBs. The output signals of these PCBs are connected to the MOSFETs on the prototype PCB. Each gate driver PCB controls a parallel branch of the SSCB MOSFETs. The gate driver used is ADuM4135 manufactured by Analog Devices. Although, it's primarily meant to drive IGBTs, its performance in driving MOSFETs is also adequate. The ADuM4135 has an integrated desaturation protection. However, it's disabled as it's not required. The gate driver's input logic signal is provided by the LaunchPad.

The LaunchPad is a development board for the proposed TMS320F28379D microcontroller to be used [59]. As seen in figure 5.1 it's mounted on top of the detection circuits PCB. An advantage of using the LaunchPad is that it contains analog comparators. These analog comparators have a digital output, either high or low. Hence, the output signals of the detection circuits (V_{OUT-L}, V_{OUT-DS}) are connected

to the inputs of the analog comparators. As the comparator outputs are digital, they become input to the TMS320F28379D microcontroller for the purpose of confirming fault detection.

In addition, the output logic signal of the Launchpad (that is input to the gate drivers) is dependent on the state of the analog comparators. If the state is low, the output signal is high and the SSCB operates normally. The moment an analog comparator's state goes high (indicating the detection of a fault), the Launchpad's output goes low causing the gate drive signal to decrease and consequently, turn the SSCB MOSFETs off.

5.1.2. The Complete Experimental Setup

For the hardware evaluation of the designed fault detection circuits, the SSCB prototype of figure 5.1 is connected to a DC power supply and a load. An experimental representation of the DC distribution line model shown in figure 4.1 is constructed. This representation is shown in figure 5.2.

Several items are highlighted in the experimental setup. In the center, the SSCB prototype is placed. Behind the prototype, a low voltage power supply is connected to the detection circuits and gate driver PCBs. This power supply provides a 15V supply to power up the various components on these PCBs. The external inductor highlighted in figure 5.2 is used to model the expected line inductance of a DC distribution line.

Moreover, the big power supplies are used as the voltage source of the modeled DC distribution line. Initially only one of the power supply is used. It is set at a voltage of 350V and delivers the power demanded by the connected load. The mechanical switch is used to create a fault in the DC distribution line. Due to this created fault, the designed detection circuits should react and isolate the distribution line. This is dependent on the increase in the line current supplied by the power supply after the mechanical switch is closed. However, the power supply has internal short circuit protection. Therefore, when the fault is created the power supply immediately stops its current. As a result, it does not give the opportunity for the detection circuits to operate. However, as the purpose of the experiment is to judge the performance of the designed fault detection circuits, a capacitor is added in parallel to the power supply. This capacitor is labelled as 'external capacitor' in figure 5.2. Hence, now when the mechanical switch is closed the fault current is provided by the external capacitor instead of the power supply.

The Pearson and Rogowski coils are used for current measurement purposes. The Pearson coil measures the distribution line current. It is placed around a wire that connects the power supply and the external capacitor node to the SSCB prototype. Hence, it is able to measure the current provided by the external capacitor when a fault is created in the distribution line model. In addition, the Rogowski coil measures the drain current of a particular SSCB MOSFET. The coil is wrapped around the leg of the MOSFET on the bottom side of the SSCB prototype (difficult to see in figure 5.2). Both these coils cannot measure steady state currents but only AC current. Nonetheless, this is adequate as the current after fault occurrence will be changing with time and thus will be measurable.

5.2. Experimental Results

This section shows the experimental results of the designed fault detection circuits. The important circuit waveforms after fault isolation via the gate drivers and the launchpad are also included. To obtain the experimental results, the V_L and V_{DS} detection circuits were active simultaneously. Hence, both of the circuits possessed the capability of detecting the fault when created by closing the mechanical switch. On most occasions, it was detected via the V_L measurement circuit. This was due to its quicker operating speed (also observed in the previous chapter via the simulation results).

In order to evaluate the V_{DS} measurement circuit's performance as well, a new set of experiments were conducted with a small alteration. The alteration was made to the threshold voltages of the Launchpad's analog comparators used for the V_L measurement circuit outputs. The threshold was increased to the maximum possible value such that the V_L circuit's output wont be able to exceed it. Hence, now when the fault was created in the line, it was detected via the V_{DS} measurement circuit. A nominal line current magnitude of 16A and a tripping current of 32A were used for the V_{DS} measurement circuit. The major test circuit parameters are listed in table 5.1.

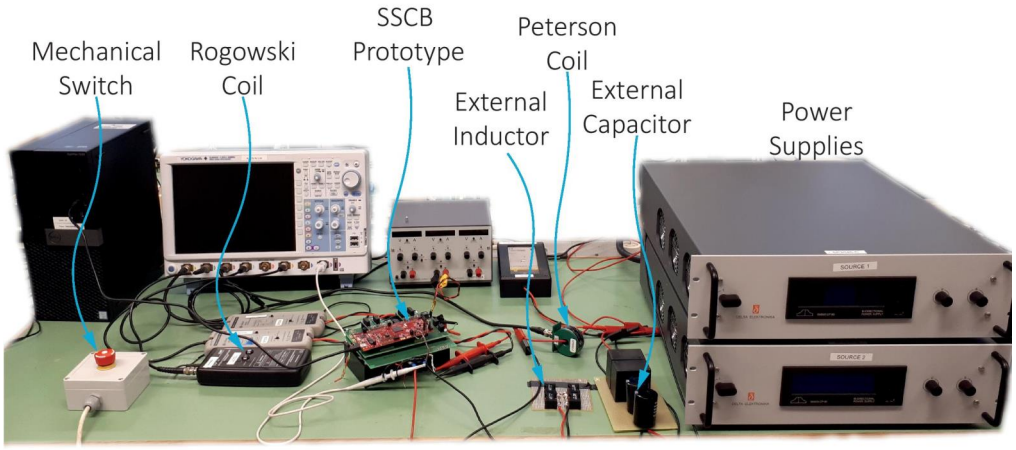


Figure 5.2: The Complete Experimental Setup

V_{DC} (V)	L_{det} (μH)	SSCB $R_{DS\text{-}on}$ (mΩ)	I_{nom} (A)	I_{trip} (A)	R_f (Ω)	C_{sn} (μF)	R_{sn} (Ω)
350	1.5	30	16	32	1	0.33	39

Table 5.1: Circuit Parameters of the Experimental Tests

Figure 5.3 demonstrates the results of the second set of experiments. In the figure the V_{DS} detection circuit outputs (V_{dr}', $V_{OUT\text{-}DS}$), the V_{GS} voltage and a MOSFET's I_{DS} measured via the Rogowski coil are shown. During normal operation (before a fault is created), the I_{DS} curve depicts that its value is zero. As explained in the previous subsection, this is because the Rogowski coil cannot measure the steady state current. For these experimental results, only 4 MOSFETs were connected on the SSCB prototype instead of 8.

When a fault is created, I_{DS} rises rapidly. Accordingly, V_{dr}' also begins to rise. Although some noise is observed at this instant in the V_{dr}' signal, the general increasing trend can still be seen. The noise also causes a false rise in $V_{OUT\text{-}DS}$'s waveform. Fortunately, it quickly falls and does not cause the Launchpad's comparator to confirm the premature fault detection. Next, the line current increases beyond the tripping value consequently causing V_{dr}' to increase to a value that activates the optocoupler. Due to this, the true rise of the $V_{OUT\text{-}DS}$ waveform begins. When the magnitude of $V_{OUT\text{-}DS}$ has risen beyond the set threshold value of the analog comparator, the LaunchPad confirms fault detection and stops the gate drive logic signal. As a result, the V_{GS} signal is pulled low. This turns off the SSCB MOSFETs and hence, the sudden fall in the I_{DS} waveform is observed. Now the fault in the distribution line has been isolated.

Even after fault isolation, the $V_{OUT\text{-}DS}$ waveform rises for a brief duration. This is because the V_{dr}' signal's magnitude remains large enough to keep the optocoupler activated. The V_{dr}' signal quickly falls to a negative value when the V_{DS} detection circuit's high voltage protection diode becomes reverse biased. Consequently, $V_{OUT\text{-}DS}$ then steadily begins to fall to zero. Although this is insignificant as the fault has already been detected and isolated via these signals.

Moreover, figure 5.4 shows the V_{DS}, $V_{C\text{-}DC}$, I_L and the I_{DS} waveforms corresponding to the fault detection via the V_{DS} circuit. $V_{C\text{-}DC}$ is the voltage measured across the external capacitor (seen in figure 5.2). From figure 5.4, a small dip is immediately observed in the $V_{C\text{-}DC}$ waveform when the fault occurs. This is in fact the capacitor discharging into the fault and hence the rise of the I_L waveform. During the current rise, I_L's magnitude is equivalent to twice of I_{DS}. This is because I_{DS} represents the drain current of only one of the two parallel MOSFETs while I_L is the total line current. By observing figures 5.3 and 5.4 together, V_{dr}' reaches the optocoupler's forward voltage approximately when I_L equals the tripping current magnitude of 32A. The small difference is due to the flowing DC current not observed in the I_L waveform. Hence, the fault is promptly detected via the V_{DS} circuit when the actual

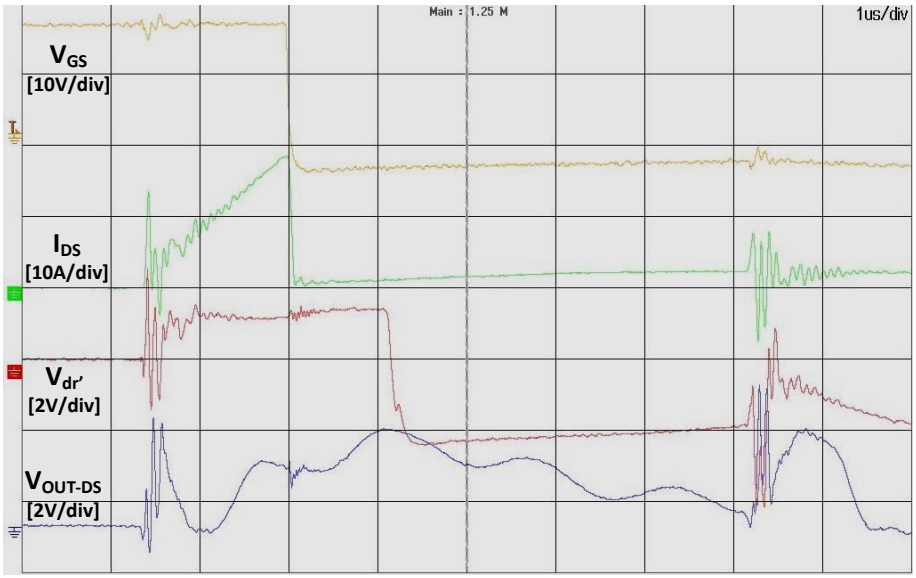


Figure 5.3: Signal Level Waveforms of the V_{DS} Detection Circuit Illustrating Fault Detection and Isolation

I_L has increased beyond the tripping value.

After the SSCB is turned off and the fault is successfully isolated, I_L still increases. As explained earlier, this is due to the snubber circuit's capacitor being charged. Subsequent to isolation, the V_{DS} waveform's rise and its peak are also observed in figure 5.4. After the V_{DS} peak, I_L becomes momentarily negative. This is due to the snubber capacitor's discharge and the dissipation of its stored energy.

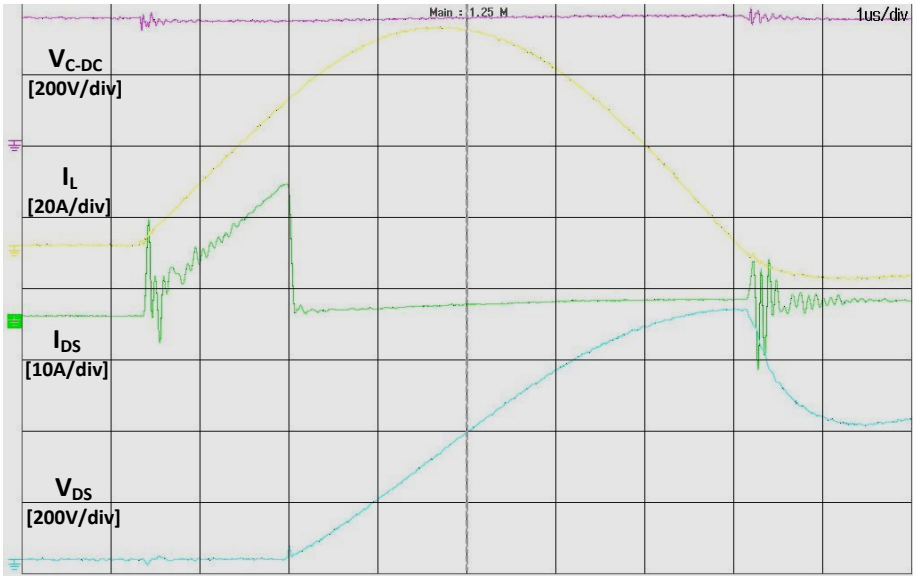


Figure 5.4: Power Level Waveforms Associated with the SSCB Prototype Showing Fault Isolation via the V_{DS} Detection Circuit

The total isolation time (after fault inception) when detected via the V_{DS} circuit is approximately 1.6 μs. This shows that the design of the detection circuit indeed makes it capable of operating quickly. Overall, the practical performance of the experimental set-up is comparable to the simulation results demonstrated in the previous chapter. This depicts that the practical design of the V_{DS} detection circuit is adequate.

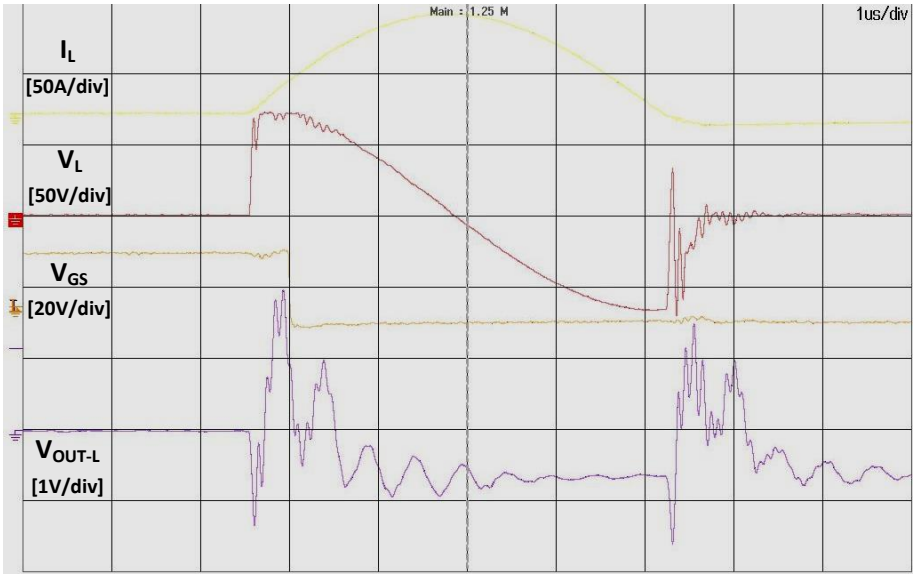


Figure 5.5: Signal Level Waveforms of the V_{DS} Detection Circuit Illustrating Fault Detection and Isolation

Furthermore, the threshold value for the V_L analog comparators was reset to their original value. Hence, for the next set of experiments, the fault was detected via the V_L measurement circuit. Figure 5.5 illustrates V_L, the corresponding V_{OUT-L}, V_{GS} and I_L waveforms. When the fault occurs, the rapid rise in I_L from a steady state value is again observed. Due to the high $\frac{di}{dt}$, the magnitude of V_L suddenly increases to a large value. Consequently, the V_{OUT-L} waveform also has a sharp rise. As seen in the figure, the rise of the V_{OUT-L} signal is a bit noisy. First, its magnitude becomes negative and then increases rapidly to track the rise of the V_L signal. Nevertheless, the noisy V_L signal's peak reaches a sufficient magnitude to exceed the threshold value of the analog comparator and change its output state from low to high. As a result, fault detection is confirmed and the gate driver subsequently pulls down the V_{GS} signal of the SSCB MOSFETs. Therefore, the fault has been isolated extremely rapidly even before the V_L transient voltage's magnitude begins to decrease.

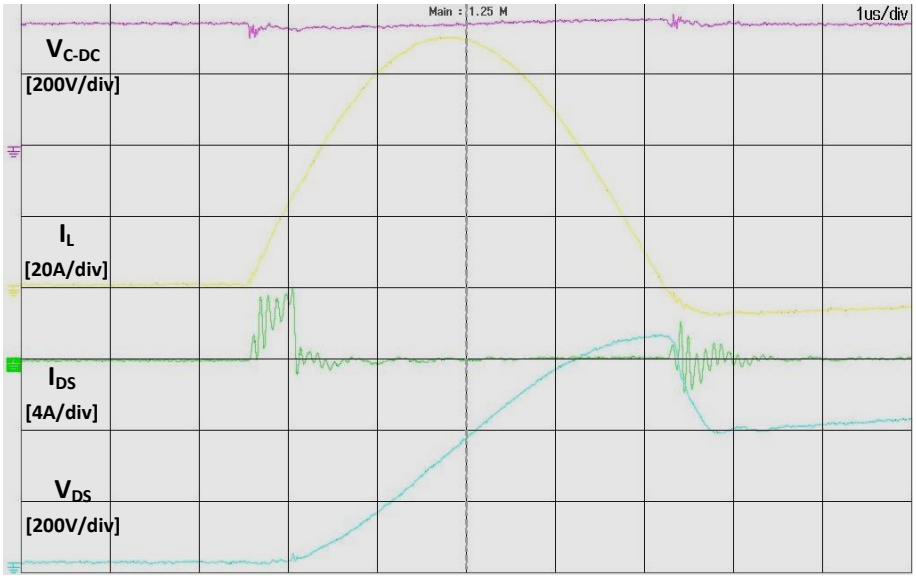


Figure 5.6: Power Level Waveforms Associated with the SSCB Prototype Illustrating Fault Isolation via the V_L Detection Circuit

In figure 5.6, the $V_{C\text{-}DC}$, V_{DS}, I_L and I_{DS} waveforms are shown. The waveforms have similar shapes to those in figure 5.4. The quicker fault detection and isolation speed can also be deduced from the I_{DS} waveform. The SSCB turned off before I_{DS}'s magnitude could increase to large values. The initial noise observed in the I_{DS} waveform in figure 5.4 is also seen in figure 5.6. Moreover, from I_L's waveform in figure 5.6, it can be inferred that the fault was indeed detected by the V_L measurement circuit. The reason is that when the SSCB MOSFETs turn off, the magnitude of I_L is lower than the tripping value set for the V_{DS} detection circuit (32A).

For the fault detected via the V_L circuit, the total isolation time (after fault inception) is around 0.5μs. This shows that the V_L designed detection circuit is also quick in its operation. Hence, faults occurring in close vicinity to the SSCB on the distribution line or low resistance faults can be quickly identified via the V_L detection circuit. Generally, the practical performance of the V_L detection circuit is mostly analogous to the simulation model's results discussed in the previous chapter. The difference is in the actual $V_{OUT\text{-}L}$ signal in figure 5.5. Although, it's able to track the changes in V_L, its waveform still contains some noise.

Moreover, the performance of the V_L and V_{DS} detection circuits was evaluated in response to an increase in the power demanded by the load. This was done by connecting another load in series with the mechanical switch of figure 5.2. Hence, now when the mechanical switch was closed, a load step was generated instead of a fault. The notable waveforms of this experimental test are shown in figure 5.7.

Due to the sudden increase in the load demand, I_L increases to fulfill the extra power required. Consequently, as seen in the figure the V_{dr}' waveform also increases. As the new steady state current is within the nominal rated value, the V_{dr}' signal's magnitude remains lower than the optocoupler's forward biasing voltage. Therefore, the optocoupler is not activated and the V_{DS} detection circuit does not recognize the load step as a fault in the distribution line. Moreover, in figure 5.7 a rise in the $V_{OUT\text{-}L}$'s waveform is not observed at the moment the load step is created. This is due to the relatively lower measured $\frac{di}{dt}$ for a load step than for a fault in the distribution line. As a result, the V_L detection circuit also does not identify the increase in the load as a fault. Hence, the V_{GS} signal remains unchanged and a higher current seamlessly flows through the distribution line.

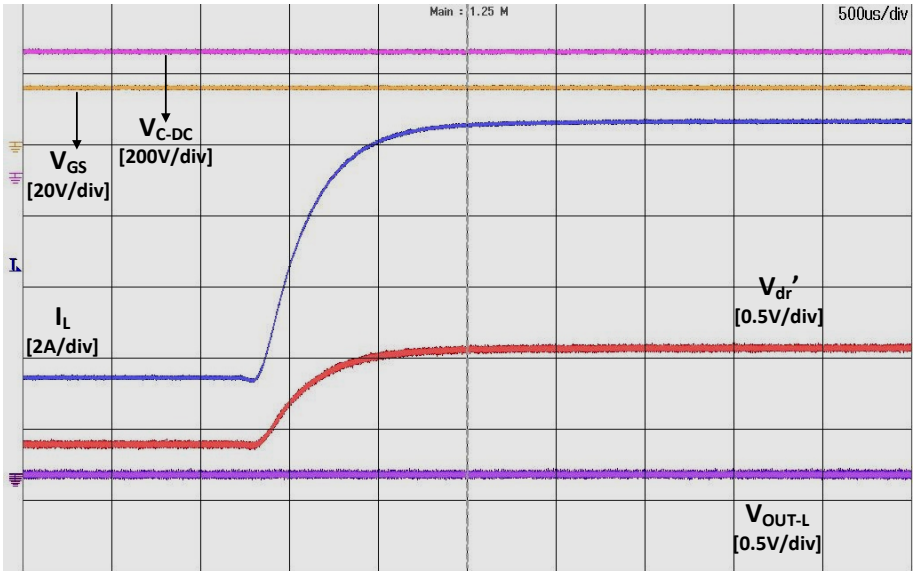


Figure 5.7: Experimental Waveforms Depicting a Load Increase in the Distribution Line

5.3. Inferences from the Experimental Results

The waveform of V_{dr}' in figure 5.3 demonstrates that the adopted design of the V_{DS} detection circuit is extremely accurate in tracking the distribution line's current. The circuit has also shown that it possesses the capability of measuring the quick changes in the current flowing through the SSCBs. The

original source for the design of this circuit claims a measurement accuracy within millivolts [4]. However, for this claim to be justified the measurement circuit needs to fulfill some specifications. These specifications are related to the two diodes used for protection and measurement (seen in figure 3.15) and have been explained earlier in section 3.3.2. As the results in figure 5.3 also exhibit millivolts accuracy, it can be evaluated that the practical implementation of the adopted V_{DS} measurement circuit design is also successfull in meeting the set specifications in [4].

Furthermore, in figure 5.5 the signal level waveforms of fault identification via the V_L detection circuit were shown. Although the designed circuit's output voltage waveform (V_{OUT-L}) was able to detect the fault, it contained some noise and oscillations in it. V_{OUT-L} was able to track the initial fast rise of the V_L signal but then experienced oscillations due to the noise present in the signal. The oscillations in the V_{OUT-L} waveform can make fault detection via the V_L measurement based method unreliable. This is because their unpredictable nature can lead to false fault detections or even the fault remaining undetected.

The major reason for the high frequency noisy oscillations appearing in the V_{OUT-L} signal is due to the degraded CMR ratio of the differential amplifier of the V_L measurement circuit. Although the CMR ratio of the amplifier used is normally high, it is defined for differential voltage magnitudes up to the amplifier's supply voltage ($-V_s$, V_s). In the practical experiments, the LM7321 Op-Amp was used as the differential amplifier. Its maximum $-V_s$, V_s range is up to ±15V. However, for the results shown in figure 5.5, $-V_s$, V_s of only ±5V were used. As the V_L differential voltage magnitude observed in figure 5.5 is reasonably larger than V_s, the amplifier's specified CMR ratio deteriorates and some common mode voltage creeps into the V_{OUT-L} waveform as noise.

A simple improvement to reduce the noisy oscillations is to increase the Op-Amp's supply voltage ($-V_s$, V_s) to the maximum limit of ±15V. This will help in maintaining a relatively higher CMR ratio. However, the power supply used on the detection circuits PCB (figure 5.1) to supply the Op-Amp's $-V_s$, V_s voltages was also used to provide power to the LaunchPad. As the LaunchPad has a maximum logic input voltage limit of 5V, the Op-Amp's $-V_s$, V_s voltages couldn't be increased to ±15V. This practical technical limitation did not permit the reduction of the oscillations observed in the V_{OUT-L} signal.

Nevertheless, to demonstrate that the oscillations observed in V_{OUT-L}'s waveform in figure 5.5 are indeed due to the degraded CMR ratio, the experiment was repeated at a lower input voltage (V_{DC}). A low V_{DC} value will produce a smaller V_L transient magnitude and thus maintain the CMR ratio of the Op-Amp. With V_{DC} = 100V, a fault was again created in the distribution line. The subsequent detection and isolation results are shown in figure 5.8.

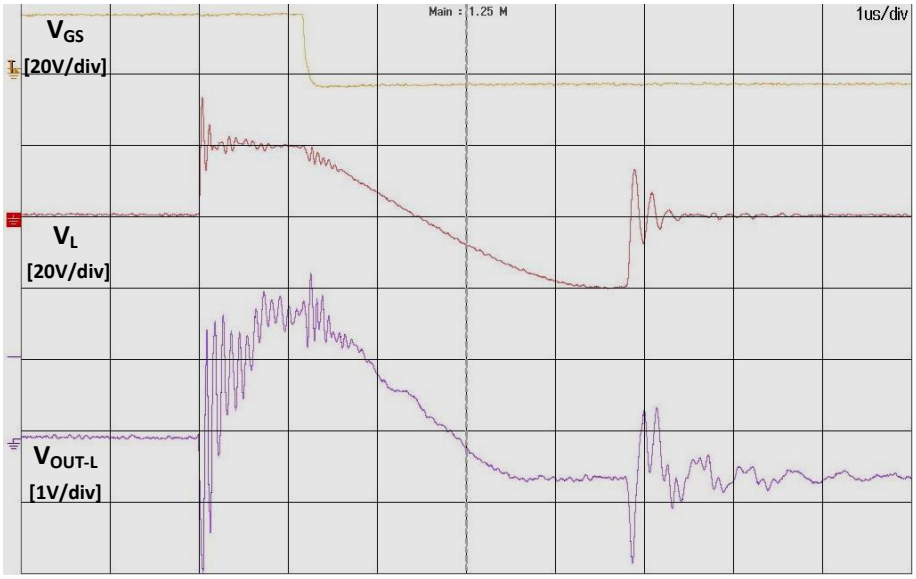


Figure 5.8: Experimental Waveforms of Fault Detection and Isolation via the V_L Detection Circuit when V_{DC}=100V

In figure 5.8 due to the low V_{DC}, the V_L magnitude rises up to only 20V. As a result, the Op-Amp's

CMR ratio remains high and the V_{OUT-L} waveform perfectly tracks the V_L signal. The rise time of the V_{OUT-L} signal is also adequate, albeit a bit noisy. However, no oscillations are observed after the signal's rise. The signal's magnitude also rises to a sufficiently high value such that the LaunchPad's analog comparator can confirm fault detection. Consequently, the V_{GS} signal is pulled low, completing fault isolation.

5.4. Summary

The hardware evaluation of the designed fault detection circuits was discussed in this chapter. First, the designed SSCB prototype and the detection circuits PCB were explained. This was followed by the description of the experimental setup used to validate the performance of the designed circuits. Next, the experimental results were presented. Judging by the results, the performance of both the designed V_L and V_{DS} detection circuits were deemed to be satisfactory.

6

Conclusions and Recommendations

The final chapter of this report elaborates on the major conclusions drawn from the research work. Comprehensive answers are provided for the research questions stated in the introduction chapter. Finally, some recommendations for further work are given related to fault detection and protection of LVDC networks.

6.1. Conclusions

The major aim of the research work was to develop a fault detection method, especially for LVDC networks that is quick in identifying a fault condition. For this purpose, not one but two distinct detection methods were selected to operate together simultaneously.

The first method was based on measuring the differential voltage across an inductor added in the DC distribution line. The inductor's voltage provided a direct indication of the rate of change of current in the DC distribution line. A large magnitude of the inductor voltage specified a high rate of increase of current and thus, was used to signify an abnormal condition in the distribution line. As a fault condition usually results in a high rate of current rise, it was detectable by measuring the inductor voltage. This method was called the V_L based fault detection method.

The second method was named the V_{DS} based fault detection method. This method measured the on state voltage of the SSCB's semiconductor device and determined the magnitude of the current flowing in the distribution line. For SSCBs comprised of MOSFETs, this was easily possible as the MOSFETs can be modelled as a resistance when conducting current. The V_{DS} method was selected in addition to the first method to avoid any uncertainties in fault detection via the V_L measurement based method. Uncertainties could occur due to variations in fault impedance and location. Moreover, the V_{DS} measurement method detects a fault only when the distribution line current's magnitude exceeds the nominal rated value. Hence, this method's operation is similar to that of an overcurrent protection scheme.

The two methods were selected after conducting a literature review of the admissible fault detection methods for LVDC networks. This review can be found in the second chapter of the report. The literature review categorized the detection methods into two broad categories; unit based and non-unit based. Unit based methods detect faults within a predefined zone and rely heavily on communication between various sensors in the network. Where as, non-unit based methods also detect faults in a roughly specified zone but have no fixed boundaries. Moreover, they can operate independent of communication. The two selected methods, V_L and V_{DS} are classified as non-unit based fault detection techniques. Non-unit methods were preferred in LVDC networks because they have the potential of detecting faults in less amount of time as compared to unit based methods. The reason is because they do not experience communication delays.

The third chapter's focus was towards the circuit design of the V_L and V_{DS} based fault detection techniques. First, the important requirements to detect a fault were listed for each method. Subsequently, the detection circuits were designed such that the respective requirements were entirely fulfilled. The V_L detection circuit's requirement of measuring the rapidly changing differential voltage across the inductor was satisfied by using a differential amplifier with a high slew rate. The detection circuit's protection

from the LVDC network's high common mode voltage was ensured by adding isolation impedances in the input paths of the differential amplifier. These impedances were also used to set the amplifier's differential gain in order to be capable of measuring a wide range of voltages. Similarly, a differential amplifier also fulfilled the V_{DS} detection circuit's requirement of fast and precise measurements. In this case, the protection of the circuit was guaranteed by using a diode to block the network's high common mode voltage. To prevent this diode from affecting the circuit's regular performance, another diode and a current source were required for accurate V_{DS} measurements. This measurement technique was adopted from the research work published in [4].

Moreover, the performances of the designed circuits in identifying a fault condition were assessed via simulations. The included simulation results demonstrated that the circuit performances were exceptional. Therefore, the design of the detection circuits were deemed to be adequate. Furthermore, the third chapter also provided a remedy against the possible false fault detections via the designed V_{DS} circuit due to increase in the junction temperature of the SSCB MOSFETs. This solution was in the form of a supplementary circuit to the adopted V_{DS} detection circuit design. The supplementary circuit is known as the level shifting circuit. It decreases the V_{DS} circuit's output by an appropriate amount in order to cancel out the effect observed due to the increase in the junction temperature.

In the fourth chapter, the simulation results of fault isolation subsequent to detection were presented. Isolation was controlled by changing the SSCB gate driver's output logic signal. From the results, it was concluded that the design of the complete fault detection and protection system can indeed fulfill the requirements of speed and accuracy. Next, the practical evaluation of the two selected fault detection methods was done. For this purpose, special PCBs were designed for the SSCB, the detection circuits and the gate driver. A microcontroller was also used to process the detection circuit outputs and control the state of the gate driver. Several experiments were conducted to test the performance of the designed detection circuits. The experimental test results were similar to the simulation results illustrated in chapter four. Hence, via their practical performance, the design of the detection circuits was validated.

The key parameter to assess the performance of the detection circuits and the complete protection system was the total amount of time required to interrupt the flow of current in the distribution line after the fault had occurred. This amount of time is crucial as the current can reach dangerous magnitudes extremely quickly. From the experimental results, this was around 0.5μs for detection via the V_L circuit and 1.5μs via the V_{DS} circuit. These times illustrate that fault isolation is achievable before the distribution line's current increases to dangerous magnitudes. As a result, the designed detection circuits satisfy the key performance criteria.

In addition, another important parameter to judge the performance was the ability of the detection circuits to prevent false fault detections. This is vital in order to avoid unnecessary power flow interruptions in the LVDC network. The performance parameter was judged by conducting an experiment in which a sudden load step was created, resulting in a higher current flowing. Subsequently, the detection circuits did not register the current rise as a fault and allowed the distribution line to operate normally under a larger load. Thus, the ability of the detection circuits to differentiate between faults and changes in the load was also deemed to be adequate.

The satisfaction of the above performance parameters signifies that the detection circuits and the overall protection system have been designed appropriately.

6.2. Further Work and Utilization

This research work was focused on detecting faults in the distribution lines of an LVDC network. For this purpose, specific fault detection methods were selected and their circuits were designed. The design and execution of the detection circuits was the fundamental step towards implementing fault protection in an LVDC network.

As LVDC networks are likely to form a meshed grid structure, there should be a high level of selectivity regarding fault isolation in the distribution lines. Selectivity refers to isolation of only the faulted distribution lines from the network and thus enabling the other distribution lines to operate normally. As the two fault detection methods are non-unit based, they cannot always ensure high selectivity levels in a meshed grid setup. Hence, there are chances that when a fault is isolated, power interruptions occur in a larger than necessary part of the network. As a result, additional research can be carried out to investigate methods to improve the selectivity in fault isolation via the two detection techniques. The

major objective of the additional work should be to precisely determine the location of the fault in the LVDC network. This will enable the particular SSCB of the faulted distribution line to be opened. Accordingly, the neighbouring distribution line SSCBs can remain unaffected thereby allowing the normal operation in other areas of the network with the faulted distribution line isolated.

The results of this research work demonstrated fault isolation and protection in a LVDC network model especially using SSCBs. There is barely any published research work available that exhibits the practical performance of SSCBs for the protection of DC networks. Therefore, this work can add to the scientific knowledge related to the protection of DC networks. Researchers interested in assessing the performance of SSCBs for fault isolation purposes can use this work as a reference.

Furthermore, the significance of this research work is in assessing the effectiveness of using non-unit based fault detection techniques in LVDC networks. Most of the research published in the area of fault detection specifically for LVDC networks utilize unit based and communication dependent techniques [1], [3]. However, for this research non-unit based detection methods were preferred due to their potential of operating faster than unit based methods. The results of this research work assist the potential use of non-unit based fault detection methods for future LVDC networks. In addition to shorter protection times, they can certainly help reduce the initial implementation and installation costs of the LVDC network. This is because there will not be a need to install communication links and extra sensors throughout the network. As a result, this research can be utilized to help strengthen the idea of implementing fault protection in LVDC networks via non-unit based techniques.

A

Theoretical Evaluation After Fault Occurrence

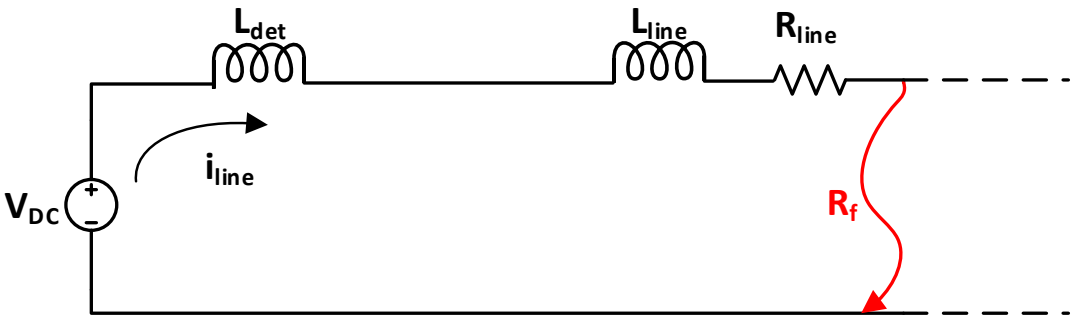


Figure A.1: Line diagram of a DC distribution line immediately after a fault

This appendix derives the solution of the line current's differential equation in a faulted DC distribution line. The starting point is from the voltage loop equation of the equivalent circuit in figure A.1. This is

$$V_{\text{DC}} = (L_{\text{det}} + L_{\text{line}}) \frac{di_{\text{line}}(t)}{dt} + (R_{\text{line}} + R_{\text{f}})\, i_{\text{line}}(t). \tag{A.1}$$

The equation can be rearranged and written as an ordinary first order differential equation as a function of time.

$$\frac{di_{\text{line}}(t)}{dt} + \left(\frac{R_{\text{line}} + R_{\text{f}}}{L_{\text{det}} + L_{\text{line}}}\right) i_{\text{line}}(t) = \frac{V_{\text{DC}}}{L_{\text{det}} + L_{\text{line}}}. \tag{A.2}$$

This equation can be solved using the technique of an integrating factor. An integrating factor can be used to solve differential equations that have a similar form below,

$$\frac{dy}{dx} + Py = Q. \tag{A.3}$$

The integrating factor (I) is defined as

$$I = e^{\int P dx}, \tag{A.4}$$

and the solution can be obtained by multiplying I on both sides of the original differential equation, such that

$$Iy = \int IQdx. \tag{A.5}$$

In (A.2), $P = \left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)$ and $Q = \left(\frac{V_{\text{DC}}}{L_{\text{det}}+L_{\text{line}}}\right)$. Hence,

$$I = e^{\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)t}, \tag{A.6}$$

and now (A.5) can be used to find a solution for the differential equation.

$$e^{\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)t} i_{\text{line}}(t) = \int e^{\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)t} \left(\frac{V_{\text{DC}}}{L_{\text{det}}+L_{\text{line}}}\right) dt, \tag{A.7}$$

$$e^{\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)t} i_{\text{line}}(t) = \left(\frac{V_{\text{DC}}}{L_{\text{det}}+L_{\text{line}}}\right)\left(\frac{L_{\text{det}}+L_{\text{line}}}{R_{\text{line}}+R_{\text{f}}}\right) e^{\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)t} + c, \tag{A.8}$$

$$i_{\text{line}}(t) = \frac{V_{\text{DC}}}{R_{\text{line}}+R_{\text{f}}} + ce^{-\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)t}. \tag{A.9}$$

The integration constant (c) can be calculated via an initial condition. Assuming the fault occurs at time $t = 0$, the line current can be assumed to be $i(0)$. Therefore,

$$c = i(0) - \frac{V_{\text{DC}}}{R_{\text{line}}+R_{\text{f}}}, \tag{A.10}$$

and (A.9) can be written as

$$\mathbf{i_{line}(t)} = \frac{\mathbf{V_{DC}}}{\mathbf{R_{line}+R_f}} + \left(\mathbf{i(0)} - \frac{\mathbf{V_{DC}}}{\mathbf{R_{line}+R_f}}\right)\mathbf{e}^{-\left(\frac{\mathbf{R_{line}+R_f}}{\mathbf{L_{det}+L_{line}}}\right)\mathbf{t}}, \tag{A.11}$$

to present the solution of the differential equation. Next, the voltage produced across L_{det} immediately after a fault occurs can be determined via the equation below

$$V_{\text{L}} = L_{\text{det}}\frac{di_{\text{line}}(t)}{dt}. \tag{A.12}$$

Substituting (A.11) in (A.12) will give the required result.

$$V_{\text{L}} = L_{\text{det}}\left[\frac{d}{dt}\left(\frac{V_{\mathbf{DC}}}{R_{\mathbf{line}}+R_{\mathbf{f}}} + \left(i(0) - \frac{V_{\mathbf{DC}}}{R_{\mathbf{line}}+R_{\mathbf{f}}}\right)e^{-\left(\frac{R_{\mathbf{line}}+R_{\mathbf{f}}}{L_{\mathbf{det}}+L_{\mathbf{line}}}\right)t}\right)\right], \tag{A.13}$$

$$V_{\text{L}} = -L_{\text{det}}\left(i(0) - \frac{V_{\text{DC}}}{R_{\text{line}}+R_{\text{f}}}\right)\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right) e^{-\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)t}, \tag{A.14}$$

$$V_{\text{L}} = L_{\text{det}}\left(\frac{V_{\text{DC}} - i(0)\,(R_{\text{line}}+R_{\text{f}})}{L_{\text{det}}+L_{\text{line}}}\right) e^{-\left(\frac{R_{\text{line}}+R_{\text{f}}}{L_{\text{det}}+L_{\text{line}}}\right)t}, \tag{A.15}$$

$$\mathbf{V_L} = [\mathbf{V_{DC}} - \mathbf{i(0)}(\mathbf{R_{line}}+\mathbf{R_f})]\left(\frac{\mathbf{L_{det}}}{\mathbf{L_{det}}+\mathbf{L_{line}}}\right)\mathbf{e}^{-\left(\frac{\mathbf{R_{line}}+\mathbf{R_f}}{\mathbf{L_{det}}+\mathbf{L_{line}}}\right)\mathbf{t}}. \tag{A.16}$$

Therefore, (A.16) is the expression of the transient voltage observed across the externally added $\frac{di}{dt}$ limiting inductor (L_{det}) after a fault occurs in a DC distribution line.

B

Bidirectional Fault Detection Capability Across the SSCB Prototype

This appendix demonstrates the experimental results of bidirectional fault detection and isolation across the SSCB via the designed detection circuits PCB.
Due to the anti-series configuration of the SSCB's semiconductor devices, it is equivalent to a four quadrant switch. Therefore, the SSCB is capable of interrupting the bidirectional flow of currents. The detection circuits PCB was also designed to be able to detect bidirectional faults. This was done by using two sets of the designed V_L and V_{DS} measurement circuits. The two V_{DS} detection circuit sets were connected across each parallel MOSFET branch of the SSCB. Meanwhile, for the two V_L circuit sets the differential amplifier inputs via the L_{det} inductor were interchanged.

The bidirectional fault detection capability was evaluated by simply swapping the two input terminals of the SSCB. Now, the current flows in the opposite direction through the SSCB MOSFETs. Hence, when a fault is created it should be identified by the other set of the detection circuits. This idea can be visualized via the circuit schematic shown in figure B.1. The schematic is similar to that in figure 4.1 except that the current flows into MOSFET Q_2 of the SSCB and leaves from Q_1. Moreover, the practical results shown in chapter 5 correspond to a particular direction of current flow. In the following figures, the experimental results of fault detection and isolation via the second set of the V_L and V_{DS} circuits are shown. Figure B.2 shows the practical waveforms when the fault is detected via the V_{DS} detection circuit and figure B.3 the waveforms for detection via the V_L circuit.

The various signal and power level waveforms in figure B.2 demonstrating fault detection and isolation are similar to the ones seen in figures 5.3 and 5.4. Even the noise at fault inception is also observed in the waveforms. Thus, the false rise of the $V_{OUT\text{-}DS}$ waveform also occurs. It also decreases rapidly,

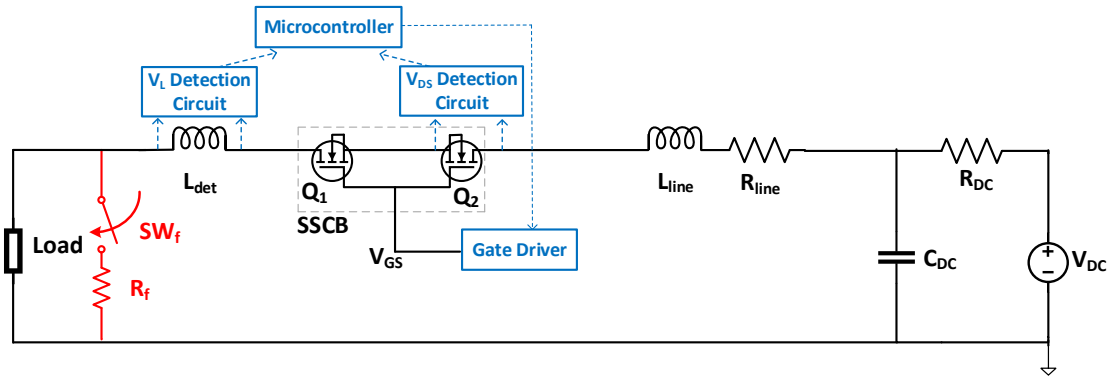
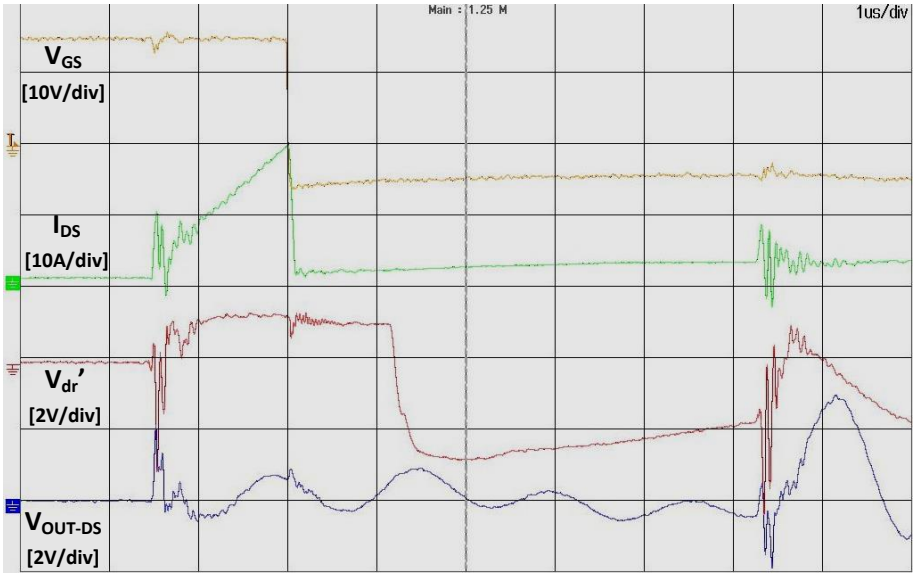


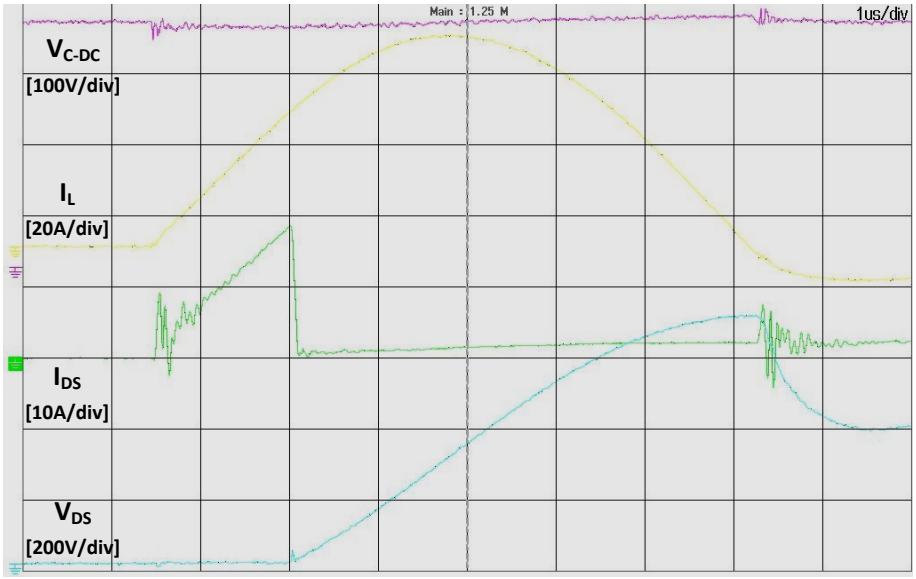
Figure B.1: Caption

even faster than in figure 5.3. Moreover, the true rise of V_{OUT-DS} is also observed after V_{dr}' has increased beyond the optocopuler's forward voltage. However, after fault isolation greater amount of oscillations are observed in V_{OUT-DS}'s waveform as compared to that in figure 5.3.

Overall, the total fault detection and isolation time of the second V_{DS} detection circuit set is comparable to the experimental results of figures 5.3 and 5.4. From figure B.2b it can be inferred that after I_L has increased beyond the tripping current value of 32A, the fault confirmation and isolation time is less than half a microsecond. The time from fault inception till its isolation is also less than 2μs.



(a) Detection Circuit's Signal Level Waveforms

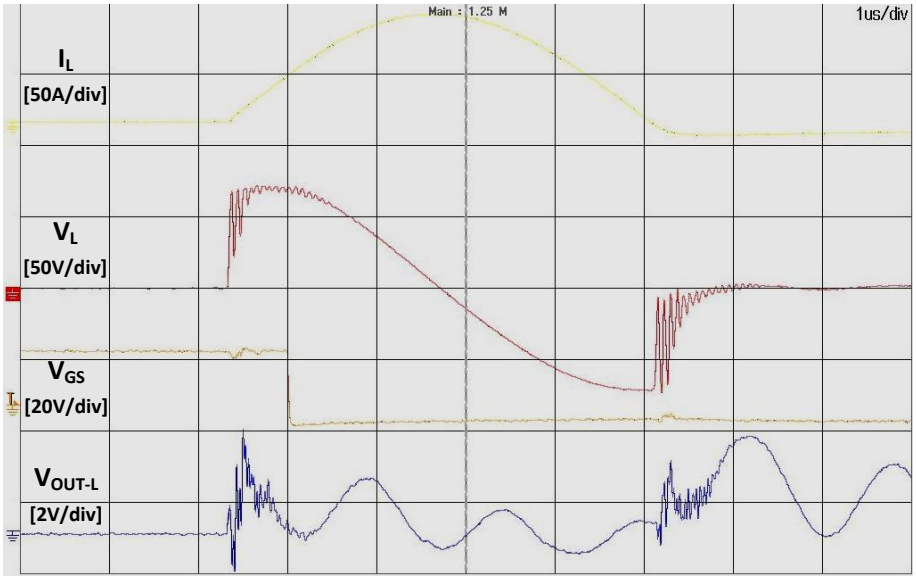


(b) SSCB Power Level Waveforms

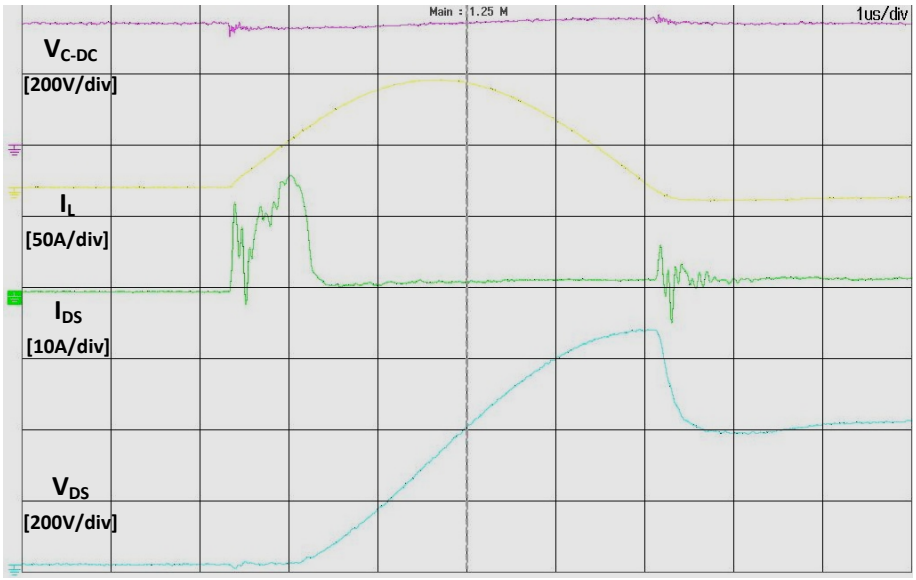
Figure B.2: Fault Identification via the Second V_{DS} Detection Circuit Set

The waveforms shown below correspond to the measurements done via the second V_L detection circuit set. Due to the design of the SSCB prototype, both the V_L circuits measure the differential voltage across the same inductor. Consequently, the results of both the circuits should be equivalent. This is confirmed via the waveforms seen in figure B.3. They are extremely similar to the ones in

figures 5.5 and 5.6. The noise and oscillations observed in the V_{OUT-L} waveform are also comparable to those seen in figure 5.5. Again this is due to the reduced CMR ratio of the differential amplifier as it is operating at a low supply voltage of ±5V. Methods to improve the CMR ratio and thus reduce the noise and oscillations have been explained in section 5.3. Overall, fault detection and isolation via the second V_L detection circuit also takes less than 1μs. Albeit it is slightly slower than the results of figure 5.5, the extra delay was due to a relatively higher threshold value used for the LaunchPad's comparator block.



(a) Detection Circuit's Signal Level Waveforms



(b) SSCB Power Level Waveforms

Figure B.3: Fault Identification via the Second V_L Detection Circuit Set

The similarity in the waveforms and the fault detection times between the results shown above and those in section 5.2 confirm that bidirectional faults can be identified across the SSCB prototype.

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