Multi-level forming-free HfO_2-based ReRAM for energy-efficient computing

Hua, Erbing; Abunahla, Heba; Gaydadjiev, Georgi; Hamdioui, Said; Ishihara, Ryoichi

DOI
10.1109/DRC61706.2024.10605282

Publication date
2024

Document Version
Final published version

Published in
DRC 2024 - 82nd Device Research Conference

Multi-level forming-free HfO_2-based ReRAM for energy-efficient computing

Erbing Hua, Heba Abunahla, Georgi Gaydadjiev, Said Hamdioui, and Ryoichi Ishihara
Qutantum and Computer Engineering, Delft University of Technology, Mekelweg 4, 2628CD, Delft, The Netherlands
Email: e.hua, h.n.abunahla, g.n.gaydadjiev, s.hamdioui, r.ishihara@tudelft.nl / Phone: +310644461674

2024 Device Research Conference (DRC) | 979-8-3503-7373-8/24/$31.00 ©2024 IEEE | DOI: 10.1109/DRC61706.2024.10605282

Introduction

Memristor technology has shown great promise for energy-efficient computing [1], though it is still facing many challenges [1, 2]. For instance, the required additional costly electroforming to establish conductive pathways is seen as a significant drawback as it contributes to power and area overheads, and limited device endurance. In this work, we propose a novel *forming-free* HfO_2-based ReRAM device with *low operating voltages*, *multi-level capability*, and less sensitivity to device-to-device (D2D) and cycle-to-cycle (C2C) variations. The device is fabricated using *CMOS-compatible* processes, excluding *the undesirable complex steps* mandatory to manufacture the state-of-the-art forming-free devices [3, 4, 5]. This is accomplished by utilizing the desirable formation energy of Pd-O bonds [6, 7], which creates conducting paths at room temperature while maintaining the analog switching ability of the devices. The proposed ReRAM device holds a great value for dense memories and energy-efficient compute architectures.

Results and discussion

A simplified fabrication method for the novel ReRAM devices is shown in Fig. 1a. It avoids specific treatments, including element doping, X-ray irradiation, and thermal annealing. The successful realization of the layout design (Fig. 1b) is verified by scanning electron microscopy (SEM), as shown in Fig. 1c. To clarify the node structure explicitly, the different layers are schematically demonstrated in Fig. 1d. Exploration of the electrical characteristics of the fabricated devices unveils three promising attributes for energy-efficient bio-inspired computing: forming-free functionality, low operating voltages, and multi-level switching capabilities. Fig. 2a exhibits the I-V characteristics of the conventional Pt/Ti/HfO_2/Pt structure [8], for which a forming cycle is required to achieve stable switching behaviour. In contrast, this cycle is eliminated for the novel Pd/Ti/HfO_2/Pd stack, as shown in Fig. 2c, though both structures are fabricated simultaneously using the method in Fig. 1a. To further highlight the superiority of the proposed ReRAM device, D2D and C2C variations of 20 devices are studied for the Pt- and Pd-based structures, as illustrated in Fig. 2b and 2d, respectively. Statistical analysis in the inset table of Fig. 2d reveals coefficients of variation that demonstrate mitigated variations and reduced V_{SET} for the Pd-based structure compared to the Pt-based devices and the state-of-the-art report [4]. The multi-state capability of the fabricated Pd/Ti/HfO_2/Pd device is investigated using Linear Sweep Voltammetry (LSV) operation described in Fig. 3a. Figure 3b depicts that the resistance can be tuned gradually by changing the RESET stop voltage to control the level of rupture in conductive filaments (CF). To verify the stability of the different resistance states, the READ-number-dependent resistance stability test is conducted (Fig. 3d) through the READ operation described in Fig. 3c. This reflects an analog switching functionality of the device, which offers the potential to store tunable multi-bit weights within a single memory cell. To better understand the conduction mechanism occurring in the devices, I-V curve fitting is performed for the Pd- and Pt-based structures, as shown in Fig. 4b and d, respectively. The Space-Charge-Limit-Current (SCLC) conduction model is in line with the fitting results for our novel Pd-based devices reported here. The slope (k) with the coefficient of determination (r^2) evolves from around 1.0 (ohmic conduction) to approximately 2.0 (SCLC) for both high resistance states (HRS) and low resistance states (LRS) (Fig. 4 b), which is different from the evolution in Fig. 4d (ohmic conduction). This can be explained through the existence of Pd/HfO_2 and a derived interface of PdO_x/HfO_{2-x} where it generates innumerable oxygen defects on the interface at room temperature[6] and crystalizes the amorphous HfO_{2-x}, creating a conductive path and trapping charges at near-V_{SET} regions.

Conclusion

This work has demonstrated, for the first time, a novel ReRAM device using Pd/Ti/HfO_2/Pd stack with optimized thicknesses; allows to avoid the costly electro-forming step without any special process steps to create the CF. The proposed device outperformed state-of-the-art forming-free ReRAM devices through multi-level capacity and low switching votalges. As a result, the ReRAM device reported here will open new insights for reduced manufacturing costs and energy-efficient computation, especially for computation-in-memory and bio-inspired computing.

References

[1] D. Kim et al., Nat. Rev. Electr. Eng., vol. 1, p. 10-23, (2024)
[2] A.James, Nat. Rev. Electr. Eng., vol. 1, p. 6-7 (2024).
[3] Y.B. Wang et al., TED, vol. 69, p. 6705-6709, (2022).
[4] X. Ding et al., TED, vol. 70, p. 1671-1675, (2023).
[5] Y.S. Chen et al., EDL, vol. 31, p. 1473–1475, (2010).
[6] H.B. Do et al., AIP Advances, vol. 7, p. 085208, (2017).
[7] MK Bruska et al., PCCP, vol. 13, p. 15947–15954, (2011).
[8] A. Hardtdegen et al., ECS Trans., vol.75, p.177, (2016).

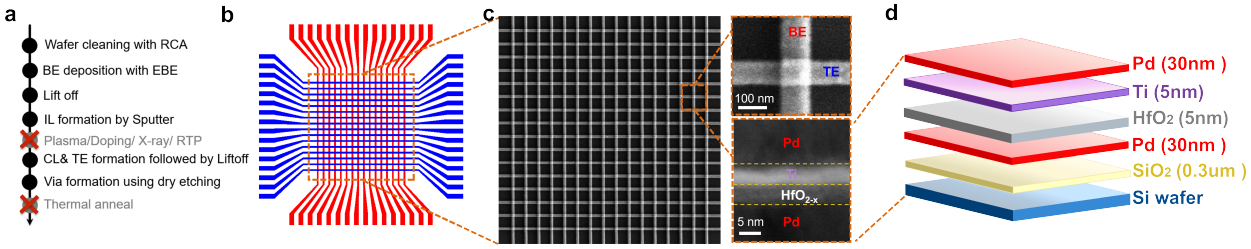

Fig. 1: a) Device fabrication flowchart. RCA: standard wafer cleaning process; BE: bottom electrodes; EBE: electron beam evaporator; IL: insulating layer; RTP: rapid thermal processing; CL: capping layer; TE: top electrodes. b) 16×16 crossbar layout of design. c) Scanning electron microscope (SEM) images of the 16 × 16 crossbar. The upper right SEM image is one of the nodes, and the lower right one is the image of the node cross section (scanning transmission electron microscopy). d) Schematic illustration of the stack.

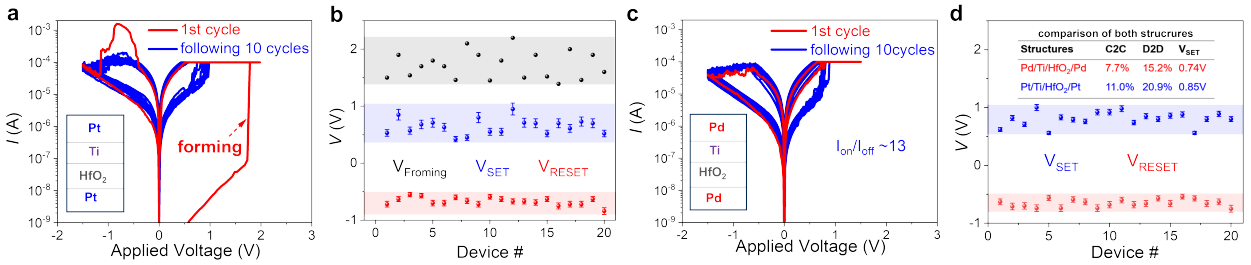

Fig. 2: a) I-V curves of traditional ReRAM devices with an electroforming process. b) Device-to-device (D2D) variation of 20 devices from the same structure as the one in a). c) I-V curves of Pd-based ReRAM devices without an electro-forming process. d) D2D variation of 20 devices from the same structure as the one in c). The inset table is a comparison in cycle-to-cycle (C2C) variation, D2D and V_{SET} for both structures.

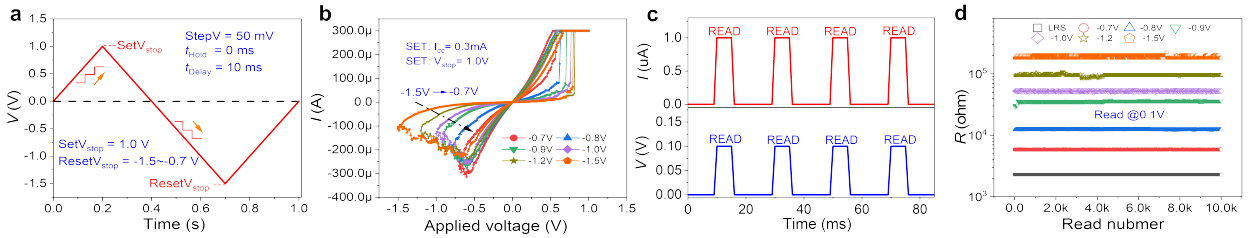

Fig. 3: a) Linear Sweep Voltammetry (LSV) operation for I-V measurement. b) I-V curves obtained by the method in a), where compliance current is 300 uA and RESET stopping voltages vary from -1.5 to -0.7V. c) READ operations for specific resistance states. d) Seven of the Read-number-dependent resistance states obtained by the method in c)

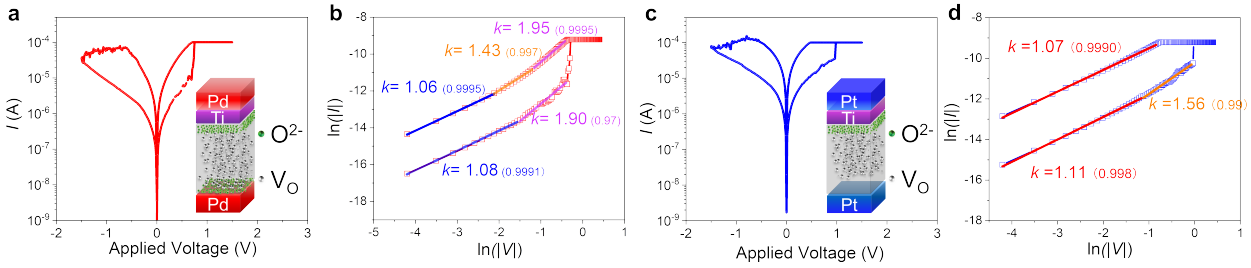

Fig. 4: a) The I-V curve of Pd/HfO_2/ Ti/Pd to be fitted. b) Double-logarithm fitted plot from positive bias of a). c) The I-V curve of Pt/HfO_2/Ti/Pt to be fitted. d) Double-logarithm fitted plot from positive bias of c). The inset diagrams in a) and c) show schematics of corresponding strucrures, where they emphasize the interface of PdO_x/HfO_{2-x}.