Performance Enhancement with a Capacitor-Scaling Design for SSHC Piezoelectric Energy Harvesting Interfaces

Zou, Yiwei; Du, Sijun

DOI
10.1109/ISCAS48785.2022.9937764

Publication date
2022

Document Version
Final published version

Published in
Proceedings of the 2022 IEEE International Symposium on Circuits and Systems (ISCAS)

Performance Enhancement with a Capacitor-Scaling Design for SSHC Piezoelectric Energy Harvesting Interfaces

Yiwei Zou and Sijun Du
Department of Microelectronics, Delft University of Technology, Delft, The Netherlands
Email: sijun.du@tudelft.nl

2022 IEEE International Symposium on Circuits and Systems (ISCAS) | 978-1-6654-8485-5/22/$31.00 ©2022 IEEE | DOI: 10.1109/ISCAS48785.2022.9937764

***Abstract*—Piezoelectric energy harvesting (PEH) has attracted much attention as an approach to exploit ambient vibrational energy to power self-sustained devices. Among the proposed interface circuits for PEH, Synchronized Switch Harvesting on Capacitor (SSHC) rectifier distinguishes itself since it achieves high power efficiency while requires no inductor. The power SSHC can extract is a function of the voltage flip efficiency. In previous studies the flip efficiency is given only under particular condition, which limits the analysis and design of SSHC circuits. This paper presents the derivation of a generic flip efficiency expression. From the result, a novel capacitor-scaling design is proposed which can reduce the total switched capacitance by up to 50% while achieving the same performance (or to enhance performance while maintaining the total capacitance). This is particularly preferred for a fully integrated design and can significantly decrease the on-chip capacitor area. The results are validated by simulations implemented in a $0.18\,\mu\text{m}$ CMOS BCD technology.**

I. Introduction

With the accelerating development of Internet-of-Things (IoT), the need for portable and lightweight power source is increasing. In many applications such as wireless sensors [1], wearable electronics [2] and implantable biomedical devices [3], where the batteries are difficult to be recharged or replaced, energy harvesting has been introduced as an effective way to serve as a power source, since it can collect ambient energy and turn them into electrical power.

Piezoelectric energy harvesting is a promising approach to scavenge ambient vibrational energy to power self-sustained systems because of its high power density and compatibility with microelectronics process [4]. As the piezoelectric transducer (PT) outputs an AC voltage, it cannot be directly used as power supply until it is rectified. Full-bridge rectifier (FBR), as shown in Fig. 1 (a), is widely used to transform the AC-type output into a rectified DC voltage. However it suffers from poor power efficiency because a large amount of energy is wasted during the transition between two voltage thresholds $V_S + 2V_D$ and $-(V_S + 2V_D)$, where V_S is the output of the interface circuit and V_D is the diode voltage drop.

Many kinds of active interface circuits have been proposed to maximize the extracted power [5]- [7], among which the

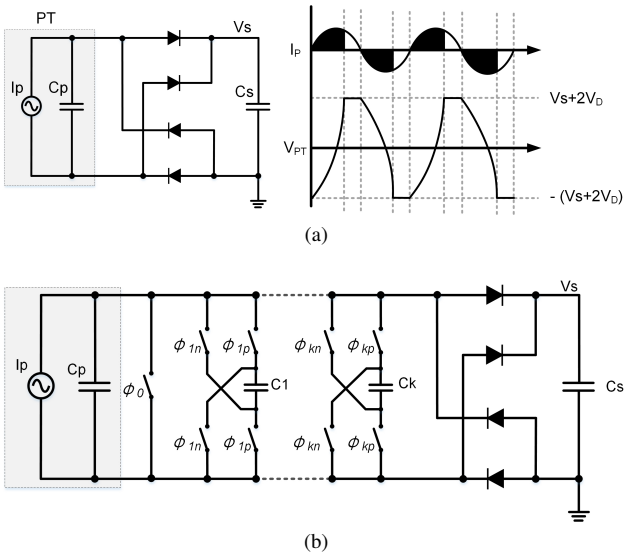


Fig. 1. (a) Full-bridge rectifier (FBR) and its transient waveform. (b) Synchronized Switch Harvesting on Capacitor (SSHC) rectifier.

Synchronized Switch Harvesting on Capacitor (SSHC) interface, as shown in Fig. 1 (b), distinguishes itself because of its high power extraction ability while removing the requirement of an off-chip inductor [7]. This characteristic has made SSHC a promising candidate for full on-chip integration. The output power of SSHC is related to voltage flip efficiency, η_f, which represents the effectiveness of synchronous voltage flipping. In [7], the η_f is given when every switched capacitor C_K has the same value as the PT's inherent capacitor C_P. In [8] the curve of η_F varying with C_K/C_P is simulated. However they both have not provided a generic expression of η_F, which is greatly needed to analyze and ameliorate the design of SSHC rectifiers.

In this paper, the flip efficiency values for one- and two-stage SSHC are manually calculated. Through the results, a generic flip efficiency expression of SSHC is derived and verified. From the expression we propose a novel design to reduce the total capacitance by up to 50% while maintain the same energy extraction performance by increasing the stage number N. From another perspective, the output power perfor-

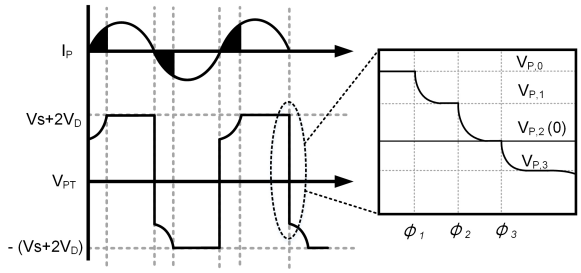


Fig. 2. The associate waveform of one-stage SSHC during flipping.

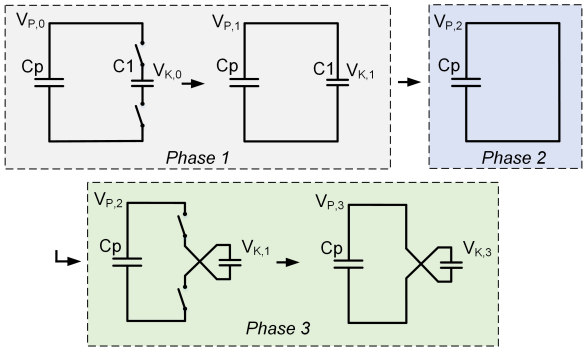


Fig. 3. The simplified flipping process of a one-stage SSHC.

mance can be improved with the same total capacitance also by increasing N. This design makes the full on-chip integration of SSHC much easier with the capacitance reduction.

II. SSHC Interface Circuit

A. Rectified output power

Fig. 2 shows the transient waveform of SSHC. To reduce the wasted charge when the voltage across the transducer V_{PT} flips from $\pm(V_S + 2V_D)$ to $\mp(V_S + 2V_D)$, the SSHC circuits first collect the charge on a series of capacitors and then reverse the top and bottom plates to flip the voltage. The flip efficiency η_F, which is defined by the absolute voltage ratio after and before flipping, i.e, $|V_{P,3}/V_{P,0}|$, determines how much charge is lost during the process, hence can lead to the output power of the interface circuit.

In a manner similar to the derivation in [9], the relation between output power and flip efficiency for SSHC is given by

$$P_{SSHC} = 2f_P C_P V_S(2V_{OC} - (1-\eta_F)(V_S + 2V_D)) \quad (1)$$

where f_P is the excitation frequency, C_P is the inherent capacitor of the PT and V_{OC} is the open circuit amplitude (zero-to-peak) of the PT. The maximum power is obtained when $V_S = \frac{V_{OC}}{1-\eta_F} - V_D$:

$$P_{SSHC,max} = 2f_P C_P(1-\eta_F)(\frac{V_{OC}}{1-\eta_F} - V_D)^2 \quad (2)$$

From (2) we notice that for a given PT excited at a given excitation level, the maximum output power only depends on η_F. Therefore, achieving a high η_F becomes the key factor affecting the rectifier's performance.

B. Theoretical derivation of flip efficiency

The flip efficiency η_F is not at its optimal value when the SSHC circuits begins to operate from its cold state, because there is no charge in each switched capacitor initially. However as the number of flip cycles increases, the voltage in all capacitors accumulates and the system will gradually enter its steady state, i.e, the absolute value of charge in each capacitor remains unchanged after each flipping operation. Since the SSHC rectifier can typically enter its steady state in only tens of vibration periods, the expression of η_F to be derived in this section is the η_F in the steady state.

TABLE I
Flip efficiency for different stage number and switched capacitance calculated from eq.(9)

Number of stage(s)	Flip efficiency		
	$C_K = 0.1C_P$	$C_K = C_P$	$C_K = 10C_P$
1	0.083	0.333	0.476
2	0.154	0.500	0.645
3	0.214	0.600	0.732
4	0.267	0.667	0.784
5	0.313	0.714	0.820
6	0.353	0.750	0.845

As a first step, the η_F of one-stage SSHC is calculated. Fig. 3 shows the simplified flipping process in steady state of a one-stage SSHC. We assume that the voltage across $C1$ and C_P before flipping are $V_{k,0}$ and $V_{p,0}$, the voltage across $C1$ and C_P after phase 1 are $V_{k,1}$ and $V_{p,1}$, and so on. The equations of the three phases are listed below:

$$\begin{cases} V_{P,0}C_P + V_{K,0}C1 = V_{P,1}C_P + V_{K,1}C_1 \\ V_{P,1} = V_{K,1} \end{cases} \quad (3)$$

$$V_{P,2} = 0 \quad (4)$$

$$\begin{cases} V_{P,2}C_P - V_{K,0}C1 = V_{P,3}C_P + V_{K,3}C_1 \\ V_{P,3} = V_{K,3} \end{cases} \quad (5)$$

Noted that from the steady-state condition, another equation can be obtained:

$$V_{K,0} = -\ V_{K,3} \quad (6)$$

Combining (2)-(5), the flip efficiency of a one-stage SSHC is derived:

$$\eta_{F,1} = \left|\frac{V_{K,3}}{V_{P,0}}\right| = \frac{C_1}{C_P + 2C_1} \quad (7)$$

As we can see from (7), $\eta_{F,1}$ only depends on the ratio of PT capacitor C_P and switched capacitor C_1.

With respect to a 2-stage SSHC, the flip efficiency can be derived in a similar way by setting up the equations of each phase. To get a better insight of the pattern of flip efficiency, all switched capacitors are assumed identical, whose capacitance

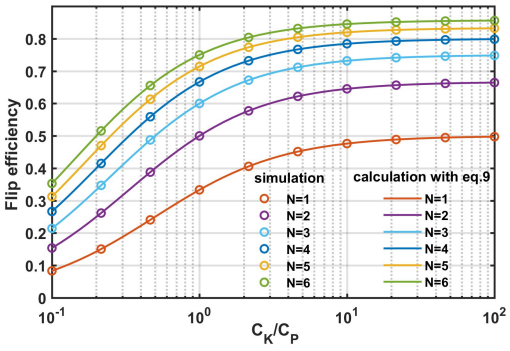


Fig. 4. Calculated and Matlab simulated flip efficiency with C_K/C_P varing from 0.1 to 100.

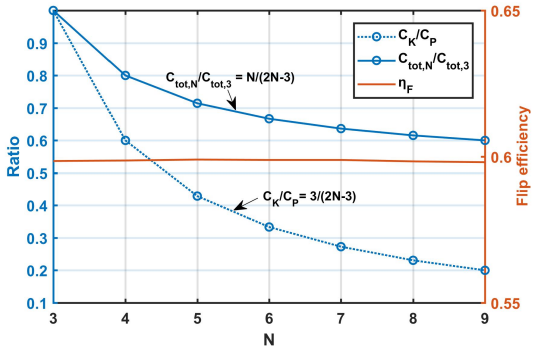


Fig. 5. The capacitance ratio and flip efficiency simulation results with different stage number.

equals to C_K. Through calculation, the flip efficiency of a 2-stage SSHC is given by

$$\eta_{F,2} = \frac{2C_K}{C_P + 3C_K} \tag{8}$$

From (7) and (8), a pattern of flip efficiency can be found. We postulate that $\eta_{F,N}$ obeys the following equation:

$$\eta_{F,N} = \frac{NC_K}{C_P + (N+1)C_K} \tag{9}$$

where N is the stage number. The expression of $\eta_{F,N}$ shows that we can increase N or C_K to make η_F higher. Table I summarizes the calculated η_F for different stage number and switched capacitance. To further verify this hypothesis, simulation results based on SSHC rectifier models are given in section III. The results exhibit a perfect fit with (9).

C. Capacitor scaling

From equation (9) we can arrive at an interesting deduction. For a N-stage SSHC with $C_K = C_P$, while the total capacitance is NC_P, if we increase the stage number to M while remain the same η_F, the ratio of total capacitance of M- and N-stage SSHC can be calculated as (11).

$$C'_K = \frac{N}{2M - N} C_P \tag{10}$$

$$\frac{C_{tot,M}}{C_{tot,N}} = \frac{MC'_K}{NC_K} = \frac{M}{2M - N} \tag{11}$$

It can be noted from (11) that by increasing the stage number M, this ratio approaches 1/2, which means that we can reduce the total switched capacitance by up to 50% while maintaining the same power extraction performance, by simply adding more switching stages. While infinite M is not practical, the total capacitance can still be saved by 33% and 40% when the number of stages is doubled and tripled, respectively. From another aspect, it also means that by increasing M, we can improve the power extraction with the same amount of capacitance.

Despite the rise in phases, the total flipping time stays the same when stage number increases. The total flipping time is proportional to the accumulation of RC time constants of each phase. Thus the ratio of flipping time of M-stage SSHC (C_K is chosen according to (10)) with respect to N-stage SSHC ($C_K = C_P$) can be written as

$$\frac{\tau_M}{\tau_N} = \frac{NC_P R/2M}{C_P R/2} = \frac{N}{M} \tag{12}$$

$$\frac{T_{flip,M}}{T_{flip,N}} = \frac{2M\tau_M + \tau_0}{2N\tau_N + \tau_0} = 1 \tag{13}$$

where τ_M and τ_N are the RC constant of each switched capacitor path in M- and N-stage SSHC and τ_0 is the RC constant of ϕ_0.

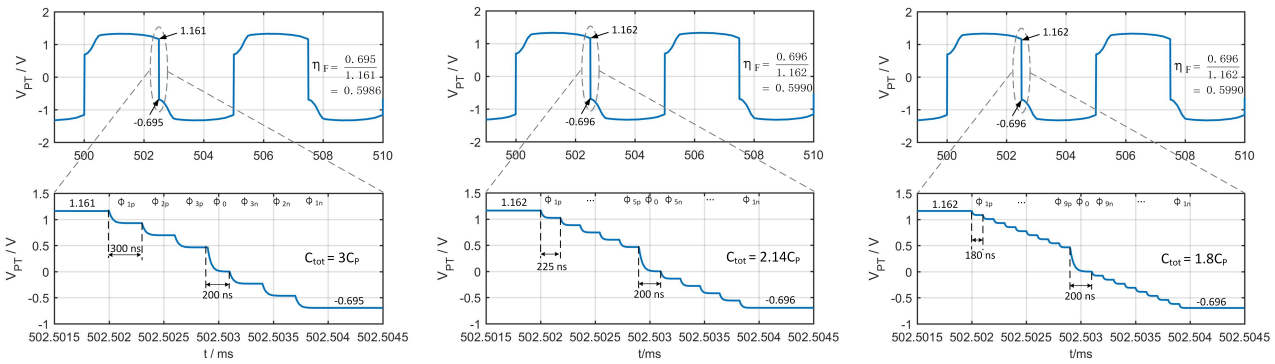
The capacitance reduction comes at a cost of circuit complexity and power consumption. Since the control circuits are composed of identical delay blocks and gate drivers, increasing stage number would not lead to much difficulties. The power consumption of the additional blocks would not be significant either compared with the harvested power level.

III. Simulation Results

In order to verify the expression of SSHC's flip efficiency in equation (9) as well as the capacitor scaling theory, Matlab mathematical analysis has been performed. In addition, an SSHC rectifier model has been built and simulated in Cadence in a $0.18\,\mu\text{m}$ CMOS BCD technology.

Fig. 4 shows the comparison between the simulated flip efficiency and calculated ones from (9) for 1- to 6-stage SSHC when C_K/C_P varies from 0.1 to 100. To make sure that the system enters the steady state with large C_K/C_P and N values, and obtains an accurate η_F, each simulation result is recorded after 2,000 flipping cycles. As shown in the results, the simulated points fit very well with (9); hence the correctness of the flip efficiency's expression in (9) can be well verified.

To verify the proposed capacitor scaling scheme, a series of simulations based on SSHC circuit model has been conducted in Cadence. The results are shown in Fig. 5. In the initial 3-stage SSHC model, all the three switched capacitors equal to C_P ($C_{tot,3} = 3\,C_P$), and hence its theoretical flip efficiency is 60%. As shown in Fig. 5, when the stage number is



(a) (b) (c)

Fig. 6. The transient waveforms of (a) 3-, (b) 5- and (c) 9-stage SSHCs. The switched capacitor's value C_K in 3-stage SSHC equals to C_P while in other circuits C_K is scaled according to (10).

gradually increased from 3 to 9 with each switched capacitor C_K designed according to (10), the flip efficiency is almost a constant value (around 59.8%), while the total capacitance $C_{tot,M}$ is reduced. Compared with the 3-stage SSHC, the total capacitance is reduced by 33% and 40% when the stage-number is doubled and tripled, respectively. These results have validated the proposed capacitor scaling scheme and further verified the η_F expression in (9).

The transient waveforms of 3-, 4-, 5- and 9-stage SSHC rectifiers in the aforementioned simulations are shown in Fig. 6. The PT inherent capacitor C_P is 30 nF. As it can be seen from the results, although the SSHCs have different stages and flipping phases, they all have the same flip efficiency, which is near 59.8%. The total switched capacitance for 4-, 5- and 9-stage SSHC are $2.4\,C_P$, $2.14\,C_P$ and $1.8\,C_P$, respectively. This implies that the total capacitance for these three rectifiers are reduced by 20%, 28.7% and 40%, respectively, compared with 3-stage SSHC with 3 switched capacitors equal to C_P (total capacitance is $3\,C_P$). If the stage number keeps increasing, the total capacitance would be reduced further. This result indicates that we can minify the capacitors while maintaining the same power extraction performance, which is a function of η_F, by adding more stages. While more flipping phases are introduced, it is important to analyze the total time required for voltage flipping. In order to achieve the optimal η_F with minimal flipping time, the time interval of each phase in 3-, 4-, 5- and 9-stage SSHC is set to 300, 225, 180 and 100 ns according to (12), while ϕ_0 for all rectifiers equals to 200 ns, as shorter phase interval would degrade the flip efficiency. It can be noted that all of the SSHC rectifiers have the same total flipping time (2 μs) despite the increase in phases.

Fig. 7 shows the output power of SSHC varying with output voltage V_S when the stage number of SSHC is increased from 3 to 5 and 9 while their total capacitance all equal to $3\,C_P$. The PT's parameters and diode's voltage drop are given in the figure. The result shows that the 5- and 9-stage SSHC have raised the peak extracted power by 18.2% and 36.2%, respectively, compared with the 3-stage SSHC. The η_F

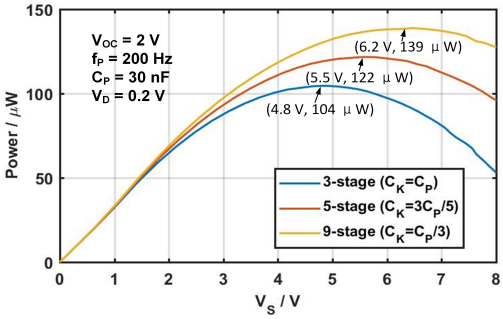


Fig. 7. Simulated output power of 3-, 5- and 9-stage SSHC with equal total capacitance ($C_{total} = 3\,Cp$) but different phase schedules.

obtained from the simulations are 59.7%, 64.9% and 68.7% for 3-, 5- and 9-stage SSHC, respectively, which also fit well with (9). Therefore the power extraction performance can be enhanced while maintaining the total capacitance by adding more stages.

IV. Conclusion

In this paper the generic expression of flip efficiency η_F (9) in SSHC rectifiers is derived and verified. The expression of η_F, which is a function of capacitor's ratio C_K/C_P and stage number N, inspires a novel capacitor scaling design which can reduce the total switched capacitance by up to 50% while remaining the same power extraction performance by adding more stages and lessening each switched capacitor. The proposed theory has been modeled and simulated with 3- to 9-stage SSHC circuits. The results show that while the total capacitance of the 4- to 9-stage SSHC rectifiers are saved by 20% to 40%, respectively, they all have the same flip efficiency (59.8%) with respect to the original 3-stage SSHC. These results demonstrate that, at the cost of slightly higher design complexity and power consumption, the system can significantly reduce the on-chip capacitor's area without sacrificing the system's performance, which provides a prospect of a fully integrated SSHC PEH system.

REFERENCES

[1] J. A. Paradiso and T. Starner, "Energy scavenging for mobile and wireless electronics," in IEEE Pervasive Computing, vol. 4, no. 1, pp. 18-27, Jan.-March 2005.

[2] X. Teng, Y. Zhang, C. C. Y. Poon and P. Bonato, "Wearable Medical Systems for p-Health," in IEEE Reviews in Biomedical Engineering, vol. 1, pp. 62-74, 2008.

[3] J. Olivo, S. Carrara and G. De Micheli, "Energy Harvesting and Remote Powering for Implantable Biosensors," in IEEE Sensors Journal, vol. 11, no. 7, pp. 1573-1586, July 2011.

[4] A. Khaligh, P. Zeng and C. Zheng, "Kinetic Energy Harvesting Using Piezoelectric and Electromagnetic Technologies—State of the Art," in IEEE Transactions on Industrial Electronics, vol. 57, no. 3, pp. 850-860, March 2010.

[5] Y. K. Ramadass and A. P. Chandrakasan, "An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," in IEEE Journal of Solid-State Circuits, vol. 45, no. 1, pp. 189-204, Jan. 2010.

[6] E. Lefeuvre, A. Badel, C. Richard, and D. Guyomar, "Piezoelectric energy harvesting device optimization by synchronous electric charge extraction," J. Intell. Mater. Syst. Struct., vol. 16, no. 10, pp. 865–876, 2005.

[7] S. Du and A. A. Seshia, "An Inductorless Bias-Flip Rectifier for Piezoelectric Energy Harvesting," in IEEE Journal of Solid-State Circuits, vol. 52, no. 10, pp. 2746-2757, Oct. 2017.

[8] X. Yue and S. Du, "Voltage Flip Efficiency Optimization of SSHC Rectifiers for Piezoelectric Energy Harvesting," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), 2021, pp. 1-5.

[9] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga and A. A. Seshia, "A Nail-Size Piezoelectric Energy Harvesting System Integrating a MEMS Transducer and a CMOS SSHI Circuit," in IEEE Sensors Journal, vol. 20, no. 1, pp. 277-285, 1 Jan.1, 2020.