

A Dynamic Zoom ADC with 109-dB DR for Audio Applications

Gönen, Burak; Sebastiano, Fabio; Quan, Rui; van Veldhoven, Robert; Makinwa, Kofi A.A.

DOI

[10.1109/JSSC.2017.2669022](https://doi.org/10.1109/JSSC.2017.2669022)

Publication date

2017

Document Version

Accepted author manuscript

Published in

IEEE Journal of Solid State Circuits

Citation (APA)

Gönen, B., Sebastiano, F., Quan, R., van Veldhoven, R., & Makinwa, K. A. A. (2017). A Dynamic Zoom ADC with 109-dB DR for Audio Applications. *IEEE Journal of Solid State Circuits*, 52(6), 1542-1550. Article 7887686. <https://doi.org/10.1109/JSSC.2017.2669022>

Important note

To cite this publication, please use the final published version (if applicable). Please check the document version above.

Copyright

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights. We will remove access to the work immediately and investigate your claim.

A Dynamic Zoom ADC with 109-dB DR for Audio Applications

Burak Gönen, Fabio Sebastiano, Rui Quan, Robert van Veldhoven, Kofi A. A. Makinwa

Abstract

This paper presents a dynamic zoom ADC. Intended for audio applications, it achieves 109 dB DR, 106 dB SNR, and 103 dB SNDR in a 20kHz bandwidth, while dissipating only 1.12mW. This translates into state-of-the-art energy efficiency as expressed by a Schreier FoM of 181.5 dB. It also achieves state-of-the-art area efficiency, occupying only 0.16mm² in 0.16- μ m CMOS. These advances are enabled by the use of concurrent fine and coarse conversions, dynamic error-correction techniques and a dynamically biased inverter-based OTA.

Keywords: Zoom ADC, dynamic, audio, DR, discrete-time, delta sigma, hybrid ADC, precision, compact ADC

I. INTRODUCTION

To achieve effective acoustic noise and echo cancellation, audio codecs for automotive applications often require up to eight input channels [1,2]. In order to detect the expected low-level disturbances, i.e. acoustic noise and echoes, in the presence of the wanted acoustic signals, i.e. voice or music, energy efficient audio ADCs with high dynamic range (DR > 100 dB) are needed. Moreover, they must occupy a minimal die area to enable the low-cost realization of multi-channel audio codecs. $\Delta\Sigma$ ADCs have become the most popular choice for audio applications since they provide high resolution at a high energy efficiency [3-20]. ADCs based on single-bit $\Delta\Sigma$ modulators ($\Delta\Sigma$ Ms) are preferred for their inherent linearity, but achieving high resolution usually requires a high-order loop-filter and a high oversampling ratio

(OSR). Furthermore, their high level of out-of-band quantization noise tightens the requirements on their decimation filters, consequently increasing its complexity and compromising energy efficiency. As an alternative, multi-bit $\Delta\Sigma$ Ms facilitate the use of lower order loop-filters and lower OSR, while also ensuring low out-of-band quantization noise. However, they require fast multi-bit quantizers to avoid introducing excessive loop delay and, hence, loop instability. These are often implemented as flash ADCs at the expense of exponentially increasing circuit complexity, area, and power consumption.

Recently, zoom ADCs have been shown to be well suited for high resolution and high linearity applications; simultaneously achieving high energy efficiency and small die area [21-23]. A zoom ADC employs a two-step architecture: the result of a coarse ADC is used to adapt the references of a fine ADC, allowing it to “zoom in” on the signal level. The accuracy of the conversion thus depends exclusively on the accuracy of the fine ADC and its references [22, 24]. Consequently, the accuracy and resolution of the coarse ADC can be low, facilitating its implementation as an ultra-low-power low-area SAR converter. Furthermore, zooming relaxes the dynamic range of the fine converter, facilitating its implementation as a compact and energy-efficient single-bit $\Delta\Sigma$ M. In prior implementations of the zoom ADCs, however, the coarse and fine converters were operated sequentially, with a coarse SAR conversion followed by a much slower fine $\Delta\Sigma$ conversion, thus limiting their application to the conversion of quasi-static signals, such as temperature or capacitance [21-23].

In order to extend the use of zoom ADCs to audio applications, this paper presents the first *dynamic* zoom ADC, in which the coarse and fine ADCs are operated concurrently, i.e. in parallel [25]. It achieves 109 dB DR, 106 dB SNR and 103 dB SNDR in a 20-kHz bandwidth while dissipating 1.12 mW and occupying 0.16 mm². In

terms of bandwidth, this represents a 1000-fold improvement on previous zoom ADCs [21-23], while maintaining their state-of-the-art energy efficiency.

The paper is organized as follows. Section II describes the architecture of the dynamic zoom ADC. In Section III, the system level design is presented. Section IV focuses the circuit level implementation. Measurement results are given in Section V and conclusions are drawn in Section VI.

II. Dynamic Zoom ADC

The block diagram of the proposed dynamic zoom ADC is depicted in Fig. 1. It consists of a coarse SAR ADC and a fine $\Delta\Sigma$ M working *concurrently*. A schematic representation of the SAR ADC's quantization levels and their relation to the zoomed-in references of the $\Delta\Sigma$ M's DAC is shown in Fig. 2(a). The SAR ADC's output (k) is found such that $k \cdot V_{LSB,C} < V_{in} < (k+1) \cdot V_{LSB,C}$ where $V_{LSB,C}$ is its quantization step, or least-significant bit (LSB). The digital value k is then processed to dynamically adjust the references of the fine DAC such that $V_{REF-} = k \cdot V_{LSB,C}$ and $V_{REF+} = (k+1) \cdot V_{LSB,C}$. In the example given in Fig. 2(a), the SAR ADC's output k corresponds to the quantization level d so that $V_{REF-} = d \cdot V_{LSB,C}$ and $V_{REF+} = (d+1) \cdot V_{LSB,C}$. These reference voltages straddle the input signal V_{in} , thus ensuring that it lies in the input range of the fine $\Delta\Sigma$ M. Thanks to zooming, the signal (V_x in Fig. 1) processed by the loop filter is much smaller than V_{in} , i.e. $|V_x| \leq LSB_C \ll V_{in}$, and so the $\Delta\Sigma$ M's quantization step can be considerably reduced. In the example shown in Fig.2(a), however, V_{in} might be very close to one of the chosen references, i.e. $V_{in} \approx V_{REF+}$ or $V_{in} \approx V_{REF-}$, resulting in modulator overload (especially in the case of higher-order modulators). Moreover, mismatch between the quantization levels of the coarse and fine DACs, as shown in Fig. 2(b), could also cause V_{in} to fall outside the $\Delta\Sigma$ M's input range.

To address this issue, the $\Delta\Sigma$'s input range can be widened by using *over-ranging*, i.e. by choosing its DAC references as $V_{REF+} = (k+1+M/2) \cdot LSB_C$ and $V_{REF-} = (k-M/2) \cdot LSB_C$ where M is the over-ranging factor. Fig. 2(c) gives an example of over-ranging with $M = 2$ in the presence of the same mismatch as in Fig. 2(b). The chosen references $V_{REF+} = (k+2) \cdot LSB_C$ and $V_{REF-} = (k-1) \cdot LSB_C$ now correctly straddle V_{in} even in the presence of a coarse conversion error. In other words, over-ranging leaves more room for coarse errors, and thus dramatically relaxing the accuracy requirements of the SAR ADC while ensuring that the $\Delta\Sigma$ is always stable. Moreover, over-ranging can be easily accommodated in the digital backend by just adding and subtracting an integer value, i.e. $\pm M/2$, while adjusting the fine ADC's references.

Since over-ranging increases the $\Delta\Sigma$'s input range, it also increases its quantization noise, resulting in a trade-off between resolution, linearity and the offset requirements of the SAR ADC. Because the input signal V_{in} is directly fed to the fine $\Delta\Sigma$, the linearity of the overall zoom ADC is only determined by the fine DAC and the loop filter, as long as the SAR ADC's INL error is small enough to keep the $\Delta\Sigma$ stable. Achieving the required loop filter linearity is greatly eased by zooming, since it ensures a low swing at the input of the loop filter ($|V_x| \leq M \cdot LSB_C \ll V_{in}$). At the same time, DEM can be used to meet the high linearity requirements in the fine DAC. In this way, zooming enables an energy-efficient two-step conversion without stringent linearity requirements on the coarse ADC, which can then be simply realized as an ultra-low-power low-area converter.

The final output of the zoom ADC is simply acquired by combining the coarse and fine digital outputs as they are used in the fine DAC, i.e. $(k+1+M/2)$ for $bs = 1$, and $(k-M/2)$ for $bs = 0$.

III. System Level Design

A. SAR resolution, BW, and over-ranging

As explained in the previous section, it is desirable to increase the resolution of the coarse ADC to reduce the $\Delta\Sigma$'s input range and hence its resolution. However, due to the limited conversion speed of the coarse ADC, the update of the $\Delta\Sigma$'s references is subject to a delay, during which the input signal can move out of the $\Delta\Sigma$'s stable input range. This issue is more pronounced for faster input signals and for smaller $\Delta\Sigma$ input ranges, i.e. for higher resolution of the coarse ADC. As shown in Fig. 3(a), when the input signal changes slowly enough to always allow the dynamically adjusted references straddle the signal, the conversion is always valid. However, the $\Delta\Sigma$ can overload when the input signal is changing too fast to be tracked by the coarse SAR ADC, as shown in Fig. 3(b).

The stable input range of $\Delta\Sigma$ can be expressed as:

$$V_{\Delta\Sigma,max} = \alpha \cdot (V_{REF,+} - V_{REF,-}) = \alpha \cdot (M + 1) \cdot \frac{V_{REF,FS}}{2^N} \quad (1)$$

where $V_{REF,FS}$ is the full-scale of the zoom ADC, $\alpha \leq 1$ defines the topology-dependent stable input range of the $\Delta\Sigma$, and N is the coarse ADC resolution. If the conversion rate of the coarse ADC is $f_{S,coarse}$, the delay in reference update is $1/f_{S,coarse}$ and no overload occurs if the signal variation (ΔV_{in}) does not exceed the stable input range of the $\Delta\Sigma$ during this interval, i.e.

$$\Delta V_{in} \leq \alpha \cdot \frac{V_{REF,FS} \cdot (M+1)}{2^N} \quad (2)$$

The largest signal variation occurs for a full-scale input sinusoid at maximum frequency $f_{in,max}$ at its zero-crossings, for which

$$\begin{aligned} \Delta V_{in} &\cong \frac{1}{f_{S,coarse}} \cdot \frac{dV_{in}}{dt} = \frac{1}{f_{S,coarse}} \cdot \frac{d}{dt} V_{REF,FS} \cdot \sin(2\pi \cdot f_{in,max} \cdot t) \Big|_{t=0} \\ &= V_{REF,FS} \cdot 2\pi \cdot \frac{1}{f_{S,coarse}} f_{in,max} \end{aligned} \quad (3)$$

combining (2) with (3) results in

$$f_{in,max} < \frac{\alpha \cdot (M+1) \cdot f_{S,coarse}}{\pi \cdot 2^{N+1}} \quad (4)$$

Assuming that the SAR ADC and the $\Delta\Sigma$ are clocked at the same frequency f_S and that the SAR ADC requires N clock periods to complete its N -bit conversion, i.e. $f_{S,coarse} = f_S/N$, the maximum input signal frequency of the zoom ADC is:

$$f_{in,max} < \frac{\alpha \cdot (M+1) \cdot f_S}{\pi \cdot N \cdot 2^{N+1}} \quad (5)$$

It is clear that the signal bandwidth of the zoom ADC is limited by the coarse ADC's resolution, but that it can be improved by increasing f_S or M . Since the energy efficiency of a $\Delta\Sigma$ is, to first-order, independent of its sampling frequency, a higher f_S is preferred over a higher M . Moreover, as will be shown in Section IV, increasing f_S decreases the area of the $\Delta\Sigma$. In the chosen technology, i.e. 0.16- μ m CMOS, $f_S = 11.29$ MHz is chosen, as a compromise between bandwidth optimization and consumption in the digital circuits (DEM controller, SAR controller, decimation filter). Fig. 4 shows $f_{in,max}$ as a function of the over-ranging M for $f_S = 11.29$ MHz, $\alpha = 0.5$ and for different SAR ADC resolutions. Both a 4-bit SAR ADC with $M = 2$, and a 5-bit SAR ADC and $M = 4$ are suitable. The latter is chosen since its quantization error will be lower, resulting in more accurate predictions of the fine ADC's input range.

B. Loop Filter and Quantizer

The Signal-to-Quantization-Noise-Ratio (SQNR) of the zoom ADC depends on the $\Delta\Sigma$'s SQNR, the SAR ADC's resolution, and the over-ranging factor M . In order to have a thermal-noise-limited Signal-to-Noise-Ratio (SNR), the quantization noise should be much less than the thermal noise, i.e. SQNR = 130 dB for SNR = 110 dB. The $\Delta\Sigma$'s SQNR is determined by the loop-filter order, the quantizer resolution and the OSR. Since out-of-band quantization noise is already low enough thanks to the zoom-induced reduction in $\Delta\Sigma$ input range, multi-bit quantization is not required.

The theoretical $SQNR_{max}$ for a zoom ADC with 1-bit quantizer, 5-bit SAR ADC and $M = 4$ for different loop-filter orders is shown in Fig. 5 [26]. This simplified model indicates that, for the chosen $OSR = 11.29 \text{ MHz} / 40 \text{ kHz} = 282$, a 2nd-order loop-filter would be sufficient. However, a real 2nd-order loop filter will not have enough margin. For a robust design, the 3rd-order $\Delta\Sigma$ shown in Fig. 6 is chosen, taking into account an expected 15% (simulated) power penalty for the loop-filter's 3rd stage. A switched-capacitor (SC) loop-filter is chosen for its robustness to clock jitter. It is implemented as a cascade of integrators with feed-forward (CIFF) compensation for its superior linearity and energy efficiency.

System level simulations revealed that the required SQNR performance is met for a DC gain of 65 dB in the 1st integrator, and a 40-dB DC gain for both the 2nd and the 3rd integrators. The first integrator's gain coefficient a_1 in conventional $\Delta\Sigma$ s is usually less than one to realize a large stable input range. However, since zooming allows for an input range much smaller than the zoom ADC's full-scale input, $a_1 = 1.5$ is chosen. This corresponds to a 1st-integrator output swing of up to 27% of the full-scale. The area of a SC $\Delta\Sigma$ is mostly dominated by the sampling and the integration capacitors of the first integrator due to the noise requirements. Thanks to the increased a_1 , the integration capacitor of the first integrator can be much smaller.

C. The Fine DAC

Since linearity is a critical specification for audio applications, the Total Harmonic Distortion (THD) of the zoom ADC should be less than -100 dB. As linearity is mainly limited by the fine DAC, even after the application of DEM, its unit elements should be designed for low mismatch. In the chosen process, thermometric capacitive DACs using lateral metal-metal capacitors have been shown to achieve 0.025% mismatch [22], and so a 5-bit version of this DAC is used. A data weighted averaging (DWA)

scheme is used to further enhance the DAC linearity. The worst case residual error after DWA can be estimated as:

$$E < \frac{1}{OSR} \cdot \sqrt{2^N - 1} \cdot \delta_{max} \quad (6)$$

where δ_{max} is the worst case mismatch [22, 27]. For the assumed $\delta_{max} = 0.025\%$ with $N = 5$, and $OSR = 282$, the expected worst-case THD is -106 dB, as was also verified by system level simulations.

IV. Circuit Design

A. $\Delta\Sigma$ Modulator

A simplified circuit schematic of the proposed dynamic zoom ADC is depicted in Fig. 7. The fine DAC is implemented by using 160 fF metal fringe-capacitor units $C_{DACp,n[1..31]}$ resulting in a total 5 pF sampling capacitor that meets the thermal-noise requirements. The reduced swing of the $\Delta\Sigma$ M enables the use of low-gain amplifiers for the realization of the integrators, such as simple energy-efficient CMOS inverters [22]. However, pseudo-differential inverter-based amplifiers exhibit poor Common-Mode Rejection Ratio (CMRR) [13]. This is improved by an input sampling circuit that utilizes switches S_{1-3} to reject input common mode signals. At the end of the sampling phase Φ_1 , switch S_1 opens and the differential input signal V_{in} is sampled on all 31 fine DAC capacitors $C_{DACp,n[1..31]}$, while the input common-mode is cancelled. The CMRR is limited by the matching of the two sampling capacitors, and is simulated to be higher than 60 dB. Because they see rail-to-rail signals, the input switches $S_{i[1..31]}$ are bootstrapped to improve their linearity [9]. In the integration phase Φ_2 , m DAC elements ($m = k-2$ or $m = k+3$) are connected to $V_{ref,p}$ in the positive branch (to $V_{ref,n}$ in the negative branch), while the others are connected to $V_{ref,n}$ ($V_{ref,p}$). Thus, a differential charge equal to $31 \cdot C_{DACp} \cdot V_{in} - C_{DACp} \cdot m \cdot (V_{ref,p} - V_{ref,n})$ is transferred to the integration capacitors $C_{int1p-n}$, effectively performing reference zooming in charge domain. Since

the units used in each period are scrambled by the DWA algorithm, a high-accuracy reference zooming is achieved. The quantizer is implemented as a dynamic latch proceeded by a single stage preamplifier.

B. Loop-Filter Integrators

Inverter-based integrators have been used in $\Delta\Sigma$ modulators for their excellent energy efficiency [13, 21, 22, 28, 29]. However, a simple CMOS inverter's quiescent current is strongly dependent on its input voltage, and is prone to process, supply voltage and temperature (PVT) variations. An energy-efficient pseudo-differential inverter-based Operational Transconductance Amplifier (OTA), shown in Fig. 8(a), employing a dynamic biasing scheme addressing PVT sensitivity is proposed in [22]. The proposed topology, however, is not suitable for high sampling frequencies, as explained in the following. During the sampling phase Φ_1 , the input is sampled on C_s and the input transistors M_1 and M_2 are diode connected and biased by a floating current source via cascode transistors M_{3b} and M_{4b} while M_{3a} and M_{4a} are in off state. The bias voltages V_{OP} and V_{ON} are sampled on the auto-zeroing capacitors C_{az} while simultaneously sampling the offset and $1/f$ noise of the OTA to implement auto-zeroing. Since the floating current source needs to be removed from the circuit in the following integration phase Φ_2 , M_{3b} and M_{4b} are driven off and M_{3a} and M_{4a} are turned on by biasing their gates with $V_{b,n1}$ and $V_{b,p1}$, respectively. Because of the large current flowing in the OTA, the switching gates of cascode transistors $M_{3a,b}$ and $M_{4a,b}$ are large enough to significantly load the biasing circuit generating $V_{b,n1}$ and $V_{b,p1}$. For $f_s = 11.29\text{MHz}$, settling to the correct biasing voltages within each period, would require the biasing circuit to consume about the same amount of power as the OTA itself, which would significantly degrade energy efficiency.

A dynamic biasing scheme for inverter-based OTAs is proposed in this work and shown in Fig. 8(b). Instead of switching the floating current source by means of cascode transistors, switches S_{b1-3} are introduced. During the sampling phase Φ_1 , diode connections are established around the input transistors (M_{1-2}) via S_{b1} and S_{b3} , and the floating current source (M_{5-6}) forces the same bias current (125 μA) through the input and cascode (M_{3-4}) transistors. At the same time, the bias voltages as well as the offset and the $1/f$ noise are sampled on the auto-zeroing capacitors C_{az} (2 pF each). In the integration phase Φ_2 , diode connections are broken by opening the switches S_{b1} and S_{b3} and the floating current source consisting of M_5 and M_6 is simply bypassed by S_{b2} . Since there is no switching capacitive load to the biasing circuit, its power consumption can be minimized. Furthermore, the proposed biasing scheme results a much more compact design by eliminating two large cascode transistors. A simple switched-capacitor common mode feedback (CMFB) circuit as in [28] is adequate to avoid output common-mode drift in the pseudo-differential implementation.

Integration capacitors $C_{int} = 3.3$ pF are realized by using metal fringe capacitors. The parasitic capacitance across S_{b4} (C_{par}) may limit the integrator's DC gain if particular care is not taken. During the integration phase Φ_2 , the sampled charge is transferred to the integration capacitor C_{int} . In the following sampling phase Φ_1 , S_{b4} is off and C_{par} is in series with C_{int} . Thus, some of the integrated charge leaks into C_{par} , and is discharged in the following Φ_2 phase, thus limiting the integrator DC gain. Hence, the ratio between C_{int} and C_{par} should be much higher than the intended DC gain of 65 dB, meaning less than $C_{par} < 1$ fF for the $C_{int} = 3.3$ pF, which is achieved by an optimized switch layout and proper shielding.

Due to their more relaxed requirements, fully differential current-starved inverter-based OTAs with SC CMFB are used to implement OTA_2 and OTA_3 , as depicted in Fig. 9. Because of the relaxed noise and linearity requirements due to the 1st-integrator gain, they were biased at 5x lower current levels compared to the first OTA (50 μ A each) and their capacitors were also scaled accordingly.

C. SAR ADC

The simplified schematic of the SAR ADC with its timings is shown in Fig. 10. The 11 fF unit capacitors are sized to ensure that coarse conversion errors due to noise and mismatch are less than 1 LSB_C. As shown in Fig. 10, the SAR ADC samples the input once every 5 clock cycles. At the end of each 5-cycle conversion, the result k is given to the fine DAC. The same quantizer as in the $\Delta\Sigma$ M is used.

V. Experimental Results

The dynamic zoom ADC has been realized in a 0.16- μ m CMOS technology. The prototype ADC¹ occupies an area of 0.16 mm², as shown in Fig. 11. It draws 0.62 mA from a 1.8 V supply, with the digital circuitry consuming 29% of the power (DWA, SAR logic, and the non-overlapping clock generator). The first integrator with its 56% share dominates the analog power consumption. In contrast, the SAR ADC's analog section draws only 7 μ W (measured).

The test chip's digital outputs are the $\Delta\Sigma$ M bit-stream, the SAR ADC's comparator output, and a clock at f_s synchronized to the data. Initially, PCB-coupled interference from these outputs to the ADC's references limited the measured SNDR to 98.3dB, in a 20 kHz bandwidth, and with a 1 kHz, 1.25 V(rms) input signal [25]. Lowering the supply of the digital output drivers from 1.8 V to 0.9 V, resulting in a much cleaner

¹ The ADC presented in this paper is an improved version of the one presented in [25].

spectrum (Fig. 12). The ADC's peak SNR, SNDR and DR were then measured to be 106 dB, 103 dB and 109 dB, respectively, with DWA on (Fig. 13). With DWA off, $\Sigma\Delta$ DAC mismatch limits the peak SNDR to 72 dB. The ADC's measured CMRR is greater than 62 dB from DC up to 1 MHz for full-scale common mode inputs, demonstrating the effectiveness of the common-mode cancellation scheme. Also its $1/f$ corner is below 20 Hz, which demonstrates the effectiveness of the auto-zeroing scheme used in the 1st integrator.

As discussed before, full-scale out-of-band signals may overload the $\Delta\Sigma$. This will typically degrade its in-band DR and noise floor. To test this, Fig. 14 shows the measured DR in 20 kHz bandwidth in the presence of full-scale in- and out-of-band differential signals. A full-scale sine wave is applied to the prototype ADC's input and its frequency is swept from 10 Hz to 100 kHz. In-band noise is measured to predict the achievable DR. The ADC's DR starts to degrade with full-scale inputs above 27kHz, which is in line with the results of system-level simulations. Inserting a 1st-order RC low-pass filter (LPF) with a 30 kHz corner frequency in series with the ADC, ensures that its DR remains constant for full-scale inputs up to at least 100 kHz (the maximum output frequency of our low-noise signal generator).

Table 1 presents a summary of the ADC's performance in comparison with state-of-the-art ADCs with similar resolution (> 100 dB DR) and bandwidth. A key observation is that it is significantly more area efficient than previous designs in similar technology nodes. A large part of the ADC's area consists of capacitors, which, in turn, is defined by the kT/C noise required to obtain a given DR. Fig. 15 compares the DR and active area of state-of-the-art audio ADCs (> 90 dB DR). It can be seen that the proposed zoom ADC occupies the least area, Independent of the technology node used.

VI. Conclusion

This paper describes a dynamic zoom ADC which can digitize audio signals with state-of-the-art energy and area efficiency. Its coarse ADC consists of an efficient 5-bit SAR ADC, while its fine ADC consists of a $\Delta\Sigma$ modulator that employs DWA to achieve high linearity. The ADC's overall energy efficiency is improved by reducing the swing of the loop filter, thus relaxing its non-thermal noise limited power consumption and allowing the use of simple inverter-based amplifiers. The $1/f$ noise of the ADC is suppressed by the inherent auto-zeroing scheme of the proposed inverter-based amplifiers. A test chip implemented in a 0.16 μm CMOS process achieves a 109 dB DR, 106 dB SNR, and 103 dB SNDR while having a very competitive Schreier FoM of 181.5 dB with a state-of-the-art area efficiency.

References

- [1] S. M. Kuo and D. R. Morgan, "Active noise control: a tutorial review," in *Proceedings of the IEEE*, vol. 87, no. 6, pp. 943-973, Jun 1999.
- [2] S. J. Elliott, A. R. D. Curtis, A. J. Bullmore, and P. A. Nelson, "The active minimization of harmonic enclosed sound fields, Part III: Experimental verification," *J. Sound Vibration*, vol. 117, no. 1, pp. 35–58, 1987.
- [3] C. De Berti, P. Malcovati, L. Crespi and A. Baschiroto, "A 106 dB A-Weighted DR Low-Power Continuous-Time $\Delta\Sigma$ Modulator for MEMS Microphones," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 7, pp. 1607-1618, July 2016.
- [4] S. Billa, A. Sukumaran and S. Pavan, "A280- μ W 24-kHz-BW 98.5dB-SNDR chopped single-bit CT $\Delta\Sigma$ achieving <10-Hz 1/f noise corner without chopping artifacts," *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2016, pp. 276-277.
- [5] A. Sukumaran and S. Pavan, "Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2515-2525, Nov. 2014.
- [6] T. C. Wang, Y. H. Lin and C. C. Liu, "A 0.022mm² 98.5dB SNDR hybrid audio delta-sigma modulator with digital ELD compensation in 28nm CMOS," *2014 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, KaoHsiung, 2014, pp. 317-320.
- [7] T. Wang, W. Li, H. Yoshizawa, M. Aslan and G. C. Temes, "A 101 dB DR 1.1 mW audio delta-sigma modulator with direct-charge-transfer adder and noise shaping enhancement," *2012 IEEE Asian Solid State Circuits Conference (A-SSCC)*, Kobe, 2012, pp. 249-252.
- [8] T. Y. Lo, "A 102dB dynamic range audio sigma-delta modulator in 40nm CMOS," *2011 IEEE Asian Solid State Circuits Conference (A-SSCC)*, Jeju, 2011, pp. 257-260.
- [9] H. Park, K. Nam, D.K. Su, K. Vleugels and B.A. Wooley, "A 0.7-V 870- μ W Digital-Audio CMOS Sigma-Delta Modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1078-1087, Apr. 2009.
- [10] Y. Yang, T. Sculley and J. Abraham, "A Single-Die 124 dB Stereo Audio Delta-Sigma ADC with 111 dB THD," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1657-1665, Jul. 2008.

- [11] K. Nguyen, R. Adams, K. Sweetland and H. Chen, "A 106-dB SNR hybrid oversampling analog-to-digital converter for digital audio," *IEEE Journal of Solid-State Circuits*, vol.40, no.12, pp.2408-2415, Dec. 2005.
- [12] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson and D. Hester, "A 114-dB 68-mW Chopper-stabilized stereo multibit audio ADC in 5.62 mm²," in *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2061-2068, Dec. 2003.
- [13] T. Christen, "A 15-bit 140- μ W scalable-bandwidth inverter-based $\Delta\Sigma$ modulator for a MEMS microphone with digital output" *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1605-1614, Jul. 2013.
- [14] S. Pavan and P. Sankar, "Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 7, pp. 1365-1379, July 2010.
- [15] S. Pavan, N. Krishnapura, R. Pandarinathan and P. Sankar, "A Power Optimized Continuous-Time $\Delta\Sigma$ ADC for Audio Applications," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 351-360, Feb. 2008.
- [16] L. Dorrer *et al.*, "A Continuous Time $\Delta\Sigma$ ADC for Voice Coding with 92dB DR in 45nm CMOS," *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, San Francisco, CA, 2008, pp. 502-631.
- [17] P. Morrow *et al.*, "A 0.18 μ m 102dB-SNR mixed CT SC audio-band $\Delta\Sigma$ ADC," *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, San Francisco, CA, 2005, pp. 178-592 Vol. 1.
- [18] A. L. Coban and P. E. Allen, "A 1.5 V 1.0 mW audio $\Delta\Sigma$ modulator with 98 dB dynamic range," *1999 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 1999, pp. 50-51.
- [19] E. J. van der Zwan, "A 2.3 mW CMOS $\Sigma\Delta$ modulator for audio applications," *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International*, San Francisco, CA, USA, 1997, pp. 220-221.
- [20] Y. H. Leow; H. Tang; Z. C. Sun; L. Siek, "A 1 V 103 dB 3rd-Order Audio Continuous-Time $\Delta\Sigma$ ADC With Enhanced Noise Shaping in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2625-2638, Nov. 2016.
- [21] K. Souri and K. A. A. Makinwa, "A 0.12 mm² 7.4 μ W micropower temperature sensor with an inaccuracy of 0.2°C from 30°C to 125°C," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1693–1700, Jul. 2011
- [22] Y. Chae, K. Souri and K.A.A. Makinwa, "A 6.3 μ W 20 bit Incremental Zoom ADC with 6 ppm INL and 1 μ V Offset," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3019-3027, Aug. 2013.
- [23] S. Oh, W. Jung, K. Yang, D. Blaauw and D. Sylvester, "15.4b incremental sigma-delta capacitance-to-digital converter with zoom-in 9b asynchronous SAR," *IEEE Symp. VLSI Circuits Dig.*, pp.1-2, Jun. 2014.

- [24] H. W. Chen, I. C. Chen, H. C. Tseng and H. S. Chen, "A 1-GS/s 6-Bit Two-Channel Two-Step ADC in 0.13- μ m CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3051-3059, Nov. 2009.
- [25] B. Gönen, F. Sebastiano, R. van Veldhoven and K. A. A. Makinwa, "A 1.65mW 0.16mm² dynamic zoom ADC with 107.5dB DR in 20kHz BW," *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2016, pp. 282-283.
- [26] R. Schreier, and G. Temes, *Understanding Delta-Sigma Data Converters*, Piscataway, NJ, USA: IEEE Press/Wiley, 2005.
- [27] I. Galton, "Why dynamic-element-matching DACs work," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 57, no. 2, pp. 69–74, Feb. 2010.
- [28] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.
- [29] R. H. M. van Veldhoven, R. Rutten and L. J. Breems, "An Inverter-Based Hybrid $\Delta\Sigma$ Modulator," *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, San Francisco, CA, 2008, pp. 492-630.
- [30] A. Jain and S. Pavan, "Improved characterization of high speed continuous-time $\Delta\Sigma$ modulators using a duobinary test interface," *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, Beijing, 2013, pp. 1252-1255.

Table I. Performance summary and comparison with previous work.

	Unit	This work	[3]	[4]	[20]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]
Year	-	2016	2016	2016	2016	2014	2014	2012	2011	2009	2008	2005	2003
Technology	nm	160	160	180	65	180	28	180	40	180	350	350	350
Die Area	mm ²	0.16	0.21	1.33	0.256	1.25	0.022	0.38	0.05	2.16	7.2	0.82	5.62
Power consumption	mW	1.12	0.39	0.28	0.8	0.28	1.13	1.1	0.5	0.87	165	18	68
Sampling frequency	MHz	11.29	3	6.144	6.4	6.144	24	2.56	6.5	5	6.144	5.12	6.144
Signal bandwidth	kHz	20	20	24	25	24	24	20	24	25	20	20	20
Peak SNR	dB	106	93.4	99.3	100.1	98.9	100.6	99.5	-	100	-	106 [†]	-
Peak SNDR	dB	103	91.3	98.5	95.2	98.2	98.5	99.3	90	95	111	99	105 [†]
DR	dB	109	103.1	103.6	103	103	100.6	101.3	102	100	124 [†]	106 [†]	114 [†]
FOMs ^{††}	dB	181.5	180.2	182.9	177.9	182.3	173.8	173.9	179	174.6	174.8 [†]	166 [†]	168.7 [†]

[†] A-weighted

^{††} FOMs=DR+10log(Signal bandwidth/Power)

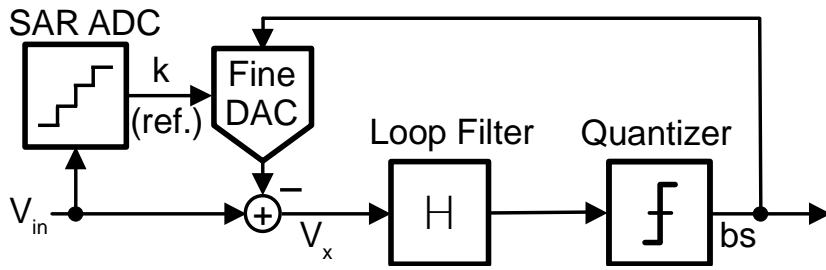


Fig. 1. Block diagram of the dynamic zoom-ADC

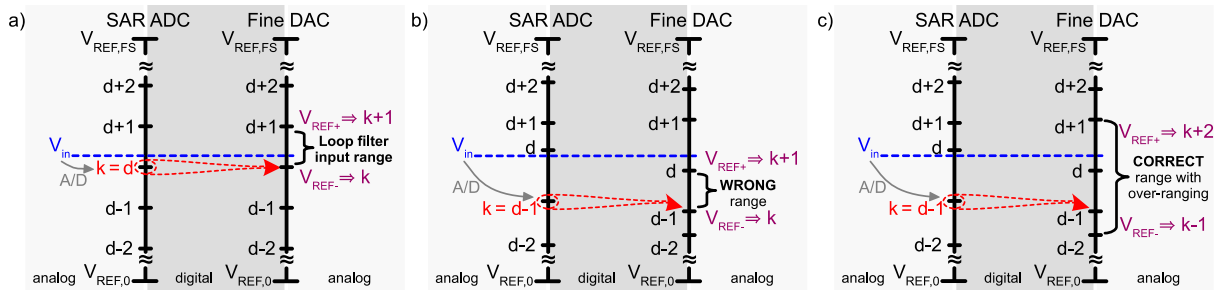


Fig. 2. (a) The SAR ADC's quantization levels and references chosen by the fine DAC for an example input (b) Same as (a), but with mismatch on both the SAR and fine DAC levels yielding an error in the chosen references. (c) Same as (b) with over-ranging ($M = 2$) resulting the input value to be within range of the chosen references.

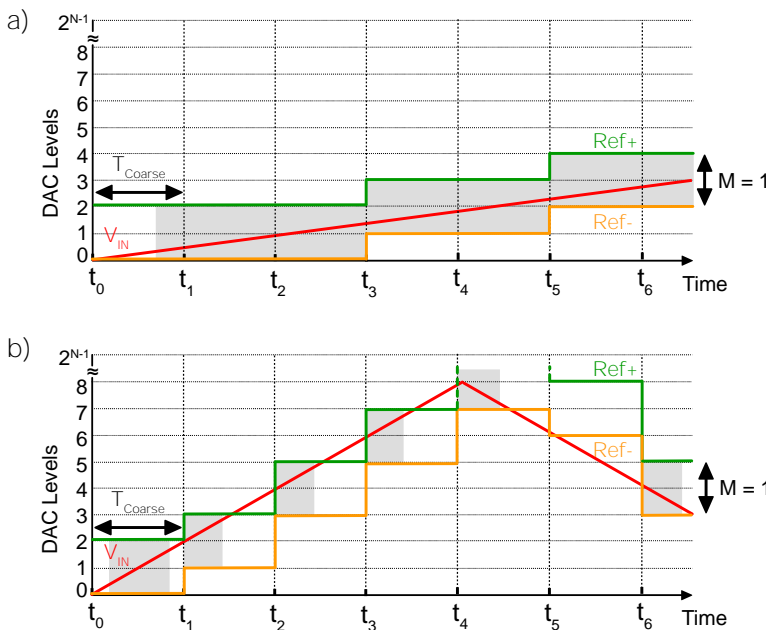


Fig. 3. Time domain operation of zooming for a slow changing input (a), and a fast changing input (b) for $M=1$.

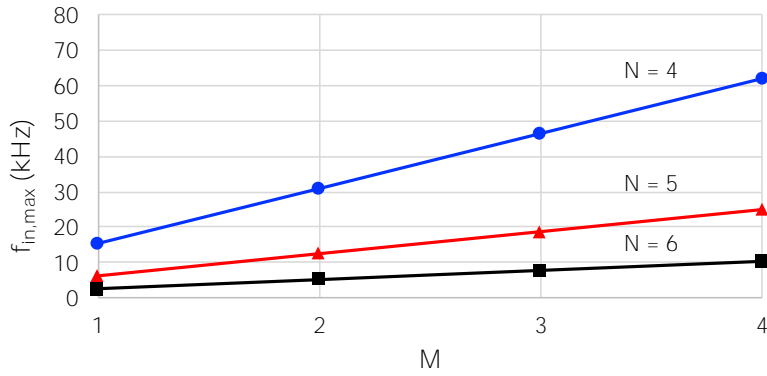


Fig. 4. $f_{in,max}$ vs M for 4 - 6 bit SAR ADCs clocked at 11.29MHz f_s .

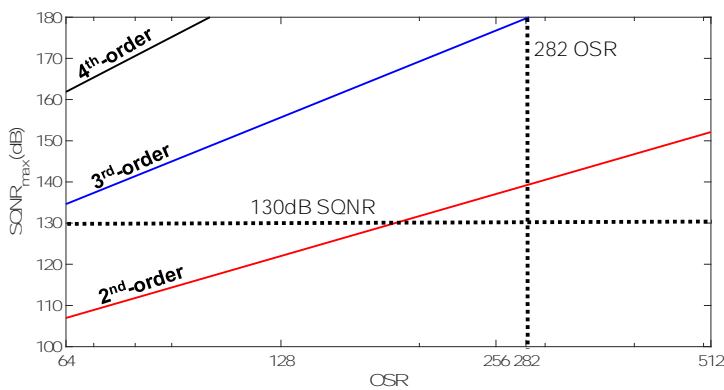


Fig. 5. SQNR_{max} of a Zoom-ADC with 5-bit SAR ADCs, and a 1st, 2nd and 3rd order 1-bit $\Delta\Sigma$ vs OSR.

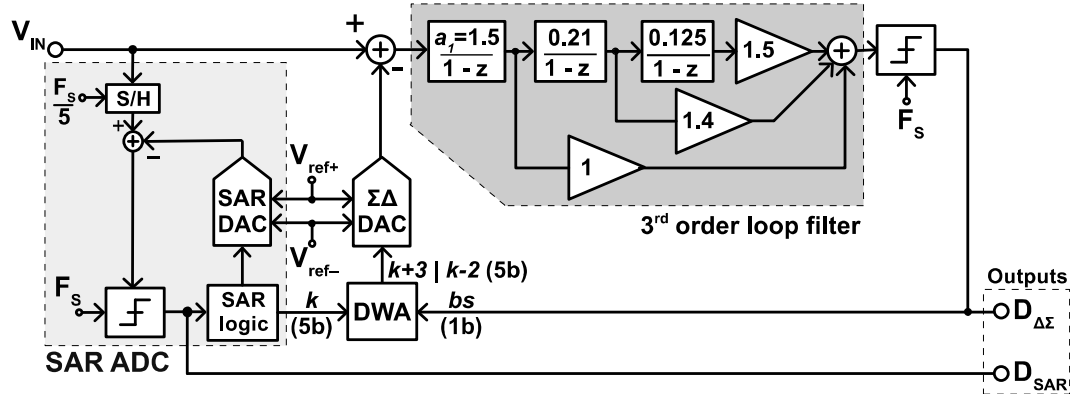


Fig. 6. System level block diagram of the implemented dynamic zoom-ADC.

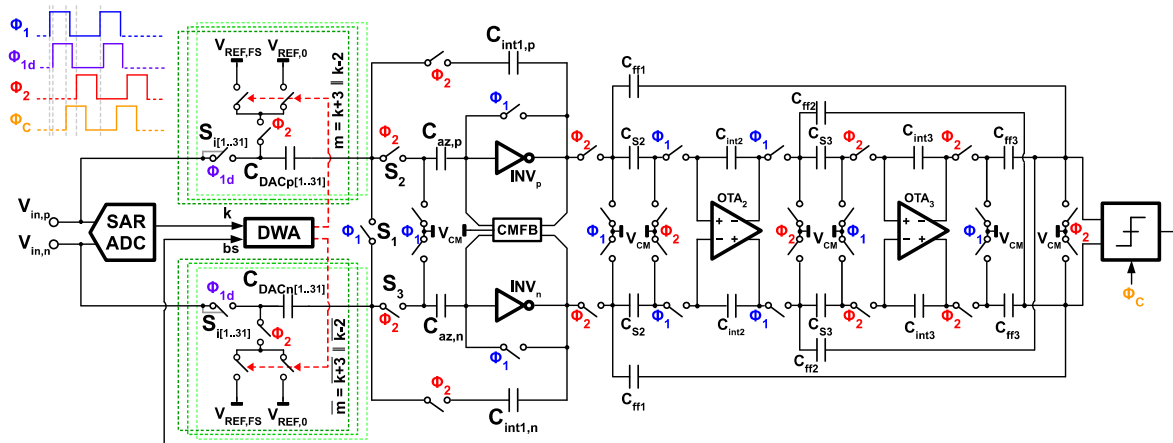


Fig. 7. Simplified schematic of the implemented dynamic zoom-ADC

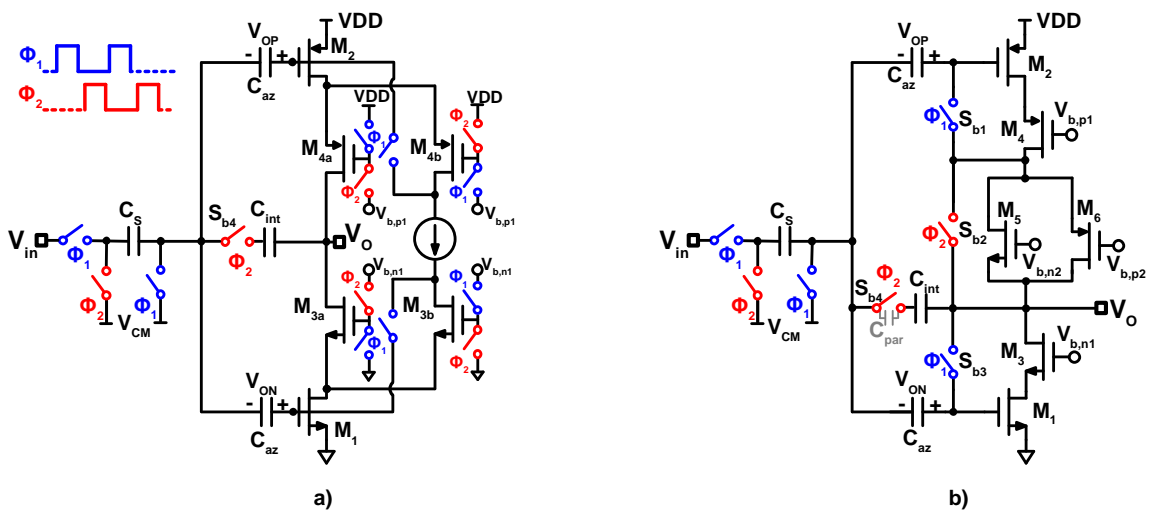


Fig. 8. (a) The inverter-based integrator used in [22]. (b) The inverter-based integrator proposed in this work.

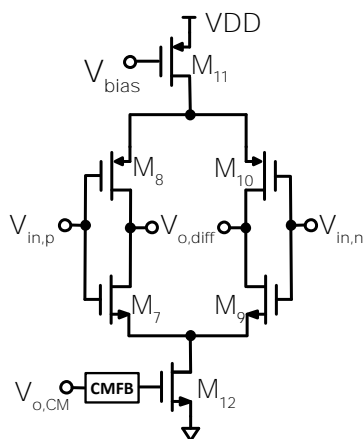


Fig. 9. Simplified schematic of OTA₂ and OTA₃.

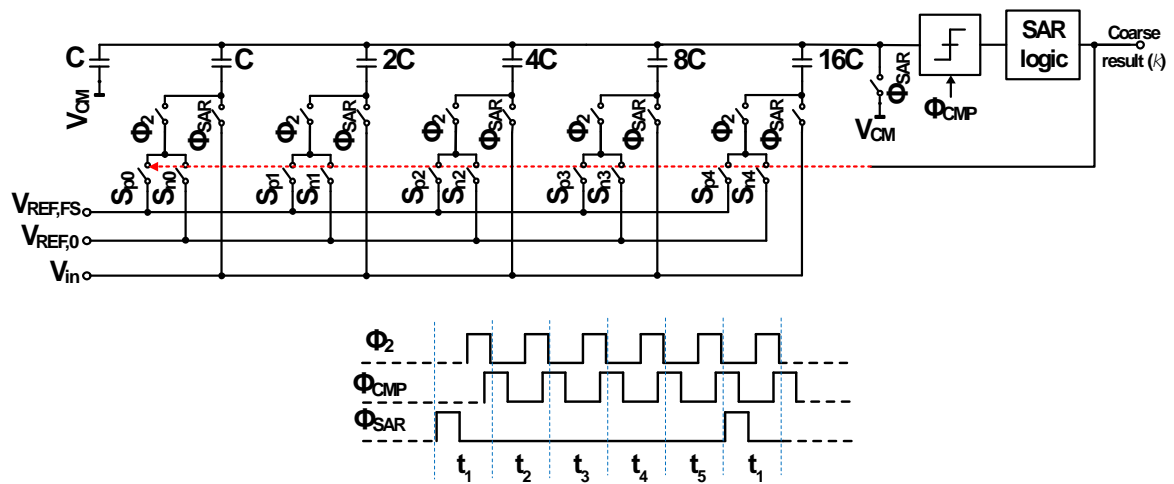


Fig. 10. Simplified schematic of the SAR ADC.

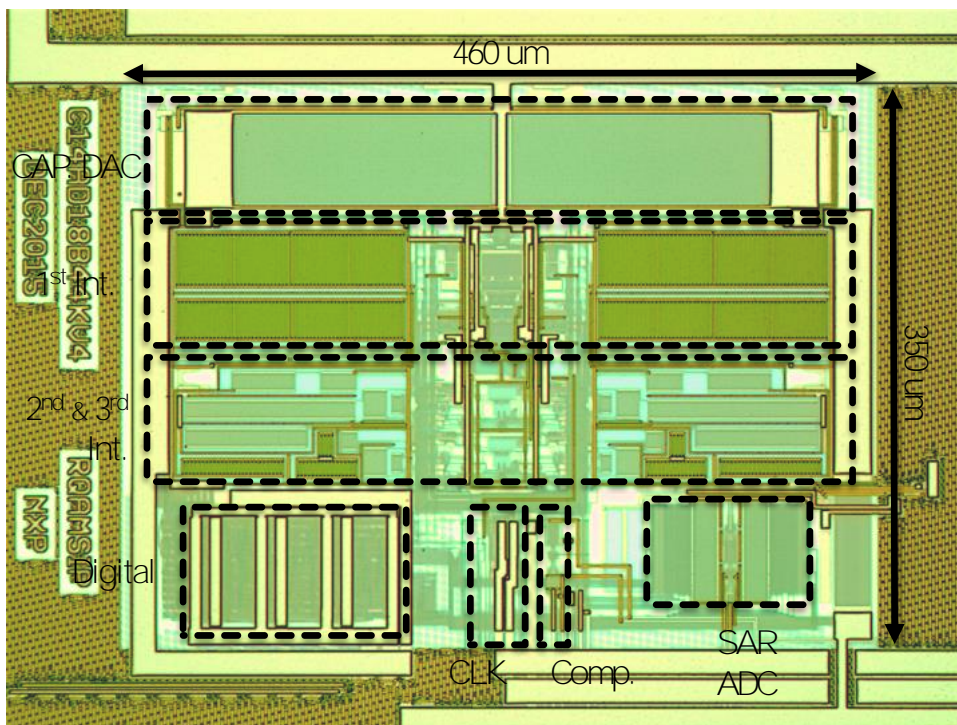


Fig. 11. Chip micrograph.

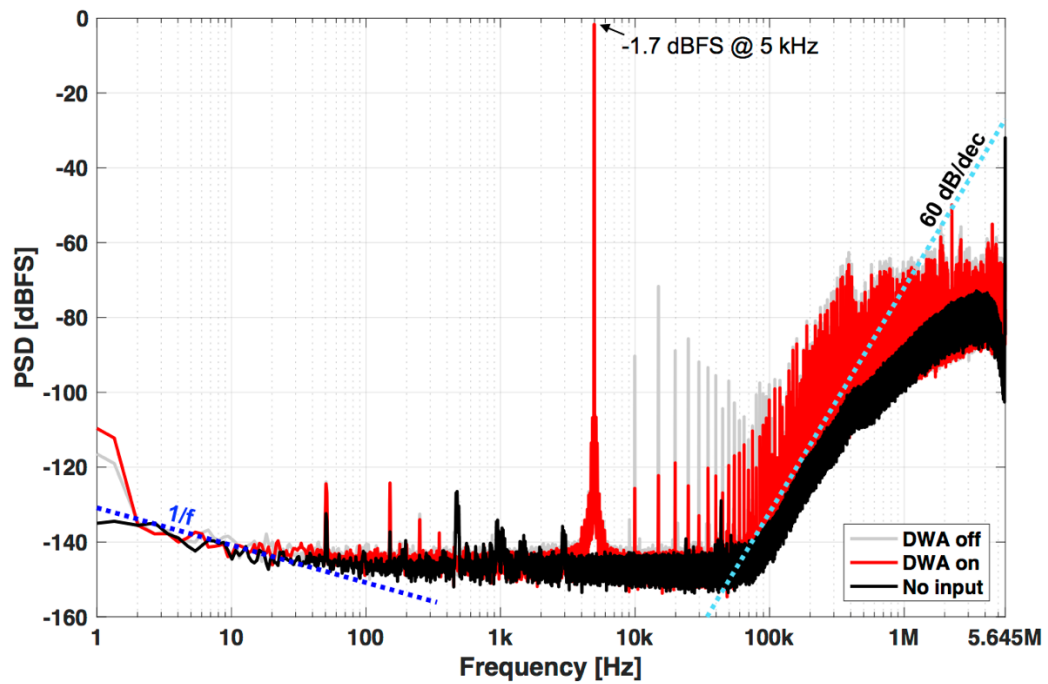


Fig. 12. Measured output spectra for DWA off, DWA on, and no input. Inputs are connected to V_{CM} for no input case, with DWA on.

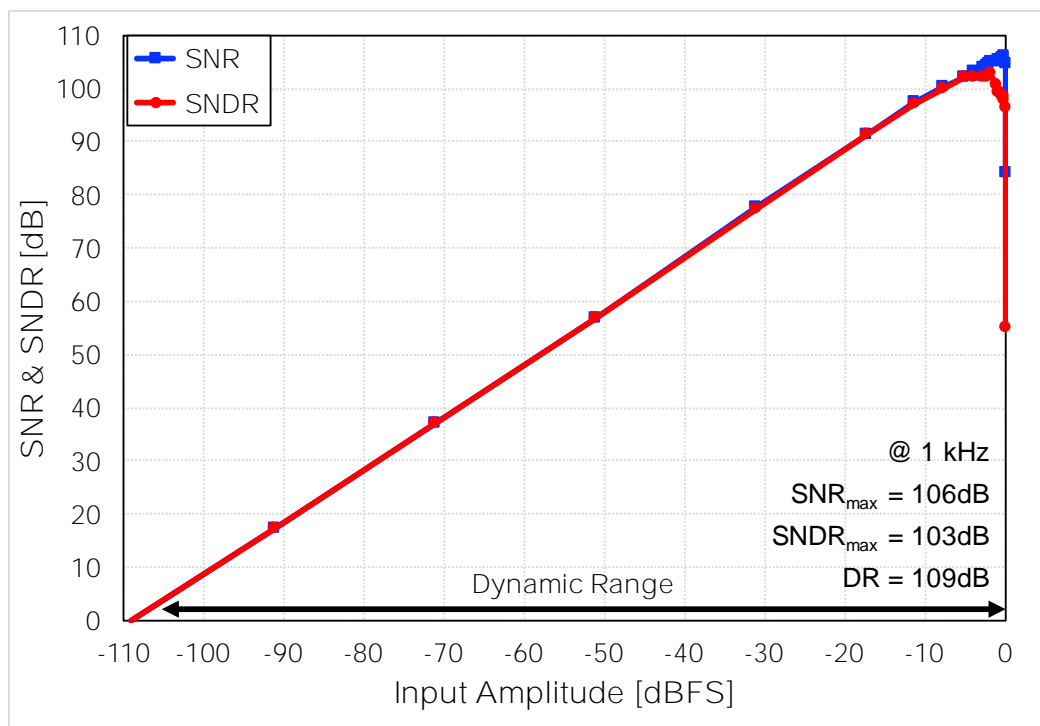


Fig. 13. Measured SNR/SNDR vs input amplitude (DWA on)

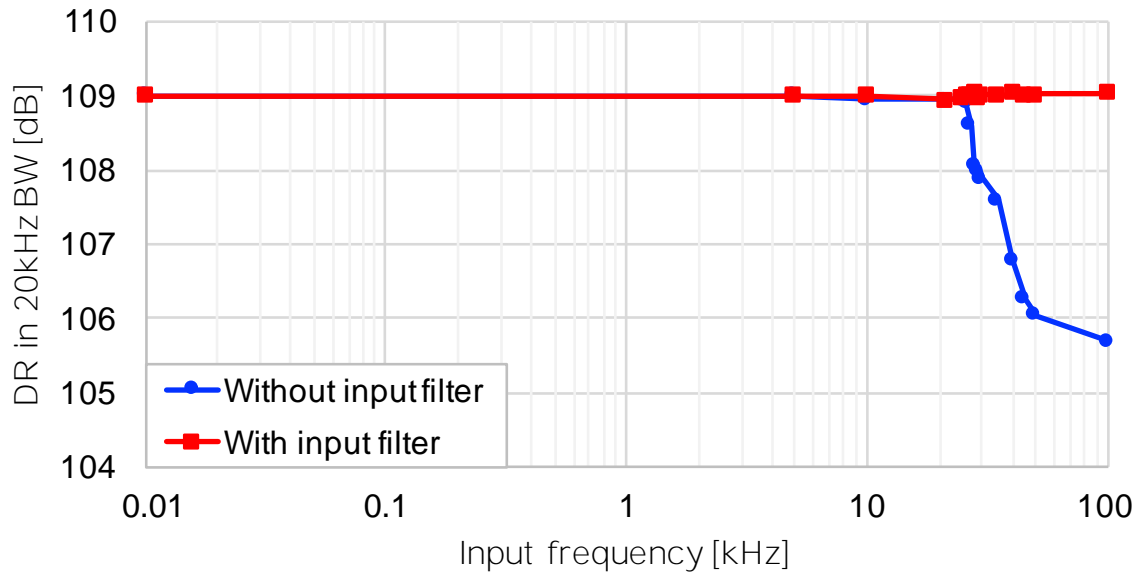


Fig. 14. DR in 20kHz BW in the presence of in and out-of-band full-scale inputs with and without an LPF at the input with 30 kHz corner frequency (DWA on).

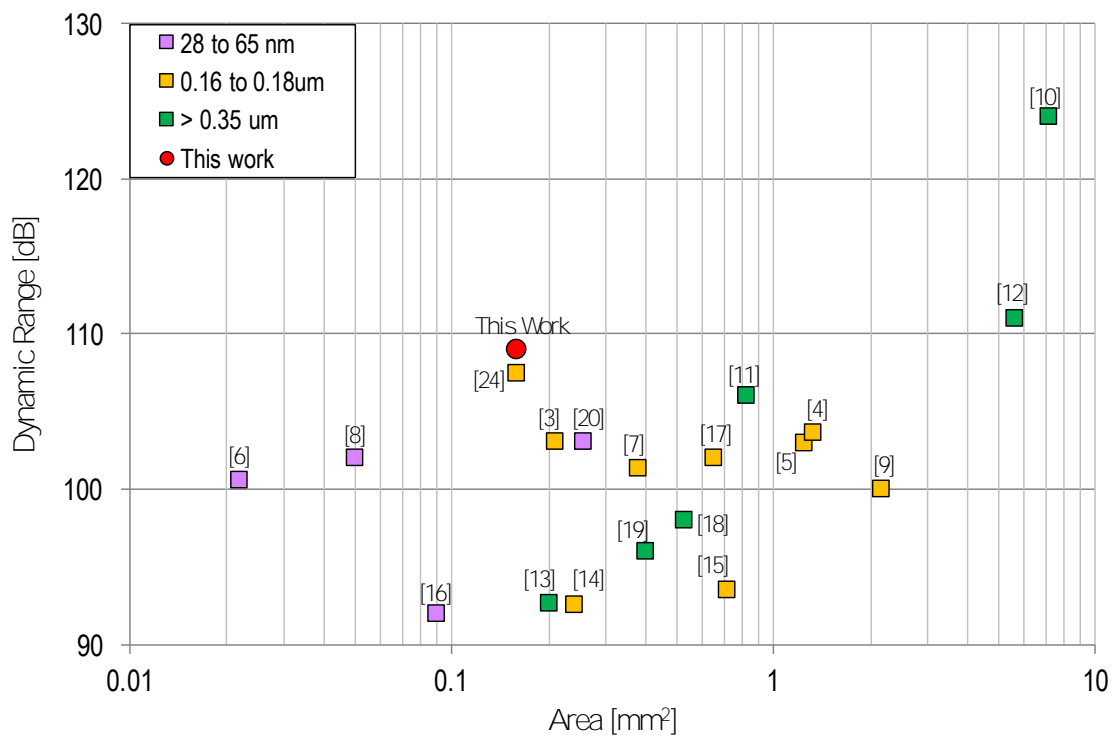


Fig. 15. DR versus silicon area comparison of the state-of-the-art audio ADCs (20 - 24kHz BW) with higher than 90dB DR.