A BJT-Based CMOS Temperature Sensor with Duty-Cycle-Modulated Output and ±0.5°C (3σ) Inaccuracy from -40 °c to 125 °c

Huang, Zhenyan; Tang, Zhong; Yu, Xiao Peng; Shi, Zheng; Lin, Ling; Tan, Nick Nianxiong

DOI
10.1109/TCSII.2021.3068283

Publication date
2021

Document Version
Accepted author manuscript

Published in
IEEE Transactions on Circuits and Systems II: Express Briefs

A BJT-based CMOS Temperature Sensor with Duty-cycle-modulated Output and ±0.54 °C (3σ) Inaccuracy from -40 °C to 125 °C

Zhenyan Huang, *Student Member, IEEE,* Zhong Tang, *Member, IEEE,* Xiao-Peng Yu, *Member, IEEE,* Zheng Shi, Ling Lin, and Nick Nianxiong Tan, *Senior Member, IEEE,*

***Abstract*—This brief presents a 0.65% relative inaccuracy CMOS temperature sensor with a duty-cycle-modulated (DCM) output. It uses a BJT-based front-end to generate a proportional to absolute temperature voltage (V_{PTAT}) and a complementary to absolute temperature voltage (V_{CTAT}), which are then modulated to a digital-friendly duty-cycle output. Dynamic element matching with Kelvin connection (KC-DEM) is applied to improve the accuracy of V_{PTAT}. To enhance the robustness of the sensor, a continuous-time dynamic single-threshold hysteresis comparator with high energy efficiency is proposed. Implemented in a standard 0.13-μm CMOS process, the sensor has an active area of 0.086 mm^2 and achieves an inaccuracy of ±0.54 °C (3σ) from -40 °C to 125 °C.**

***Index Terms*—CMOS temperature sensor, duty-cycle, BJT, low relative inaccuracy, KC-DEM.**

I. Introduction

CMOS temperature sensors are widely used in diverse fields, including environmental monitoring [1], Internet of things (IoT) [2], SoC thermal management [3], etc. Conventionally, smart CMOS temperature sensors comprise sensing elements and readout interfaces. Many devices can be used as sensing elements in CMOS technologies, like bipolar junction transistors (BJTs), MOSFETs, resistors, etc [4]. BJTs stand out for their long-term stability and their high accuracy after one-point calibration [5], [6]. The signals from sensing elements can be digitized in many ways, e.g. by using traditional analog-to-digital converters (ADC) [3], time-to-digital converters (TDC) [7], and frequency-to-digital converters (FDC) [8], etc. In industrial applications, modulating the temperature information into a duty-cycle-modulated (DCM) output is also attractive due to its simple interface. This can be easily and robustly connected to digital systems, such as microcontrollers, as well as to analog systems, like thermostats [5].

Recently, some new works based on DCM scheme have been reported. Wang et al. [5] combined a BJT-based current-mode front-end with DCM output to achieve high accuracy of ±0.3 °C from -45 °C to 130 °C. However, a relatively high power consumption of 198 μW and a large area of 2.21 mm^2 are required in a 0.7-μm CMOS technology. In [9], a low power NPN-based DCM temperature sensor was proposed at the expense of a poor accuracy of ±0.85 °C from -30 °C to 120 °C. Tang et al. [10] proposed a capacitor-reused DCM CMOS temperature sensor with a compact area of 0.073 mm^2 and a high accuracy of ±0.38 °C, but its temperature range is limited between -10 °C to 100 °C, which greatly limits its applications. Hence, compared to BJT-based temperature sensors with traditional ADC interfaces, existing DCM schemes still have challenges to achieve balances among accuracy, power consumption, die area, and temperature range.

In this brief, we present a BJT-based CMOS temperature sensor with DCM output that can achieve a good balance among the features stated above. This temperature sensor consists of a BJT-based front-end which can generate the proportional to absolute temperature (PTAT) voltage V_{PTAT} and the complementary to absolute temperature (CTAT) voltage V_{CTAT}, these temperature dependent voltages are then proceeded by a voltage-to-duty-cycle converter. In the BJT front-end circuit, dynamic element matching with Kelvin connection (KC-DEM) is applied to reduce the inaccuracy caused by BJT mismatches and avoid the impact of the DEM switch on-resistance. As an extra benefit, the applied KC-DEM technique can also reduce the spread of resistance ratio in the V_{PTAT} generation circuit. A continuous-time dynamic single-threshold hysteresis comparator is proposed to improve the robustness of the voltage-to-duty-cycle conversion with high energy efficiency. The proposed sensor has a relative inaccuracy of 0.65% (from -40°C to 125 °C) while maintaining a small chip area of 0.086 mm^2 in a standard 0.13-μm CMOS process.

II. Architecture of Proposed Temperature Sensor

A. Basic Operating Principle

The basic operating principles are shown in Fig. 1. The circuit works in two alternate phases. The capacitor voltage V_C is reset to the ground at the beginning of each phase, and then the capacitor is charged by current I_C. In phase Φ_1, SW_1 and SW_3 are on while SW_2 and SW_4 are off; V_{CTAT} and V_C are connected to node A and node B respectively; When $V_C < V_{CTAT}$, the output of the comparator remains logic high; Once $V_C > V_{CTAT}$, the circuit comes into phase Φ_2 following the output of the comparator flips to logic low. In phase Φ_2,

This work was supported by NSFC-Zhejiang Joint Fund for the Integration of Industrialization and Informatization under grant number U1709221.

Zhenyan Huang, Xiao-Peng Yu, Zheng Shi, and Nick Nianxiong Tan are with the Institute of VLSI Design, Zhejiang Univ., Hangzhou 310027, China.

Zhong Tang was with the Institute of VLSI Design, Zhejiang Univ., Hangzhou 310027, China, He is now with the Electronic Instrumentation Lab, TU/Delft, 2628 CD Delft, The Netherlands(e-mail: tangz@zju.edu.cn).

Ling Lin is with the Department of Analog IC Design, Vango Technologies Inc., Hangzhou 310053, China.

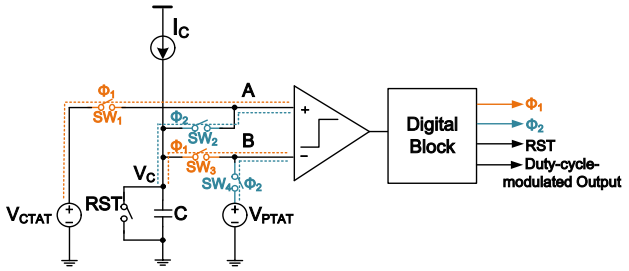

Fig. 1. Simplified diagram of the proposed design

SW_1 and SW_3 are off while SW_2 and SW_4 are on; V_{PTAT} is connected to node B while V_C to node A, thus the output of the comparator remains logic low when $V_C < V_{PTAT}$; When $V_C > V_{PTAT}$, the output turns to logic high again, and the circuit goes into a new DCM period. After being converted to the time domain, V_{CTAT} and V_{PTAT} can be expressed as

$$V_{PTAT} = \frac{I_C \cdot (t_l - t_{rst})}{C}, \tag{1}$$

$$V_{CTAT} = \frac{I_C \cdot (t_h - t_{rst})}{C}, \tag{2}$$

where I_C is the charging current, t_h and t_l are the logic-high time and logic-low time respectively. t_{rst} is the time duration for the capacitor to reset, which can be compensated conveniently in the digital domain [11].

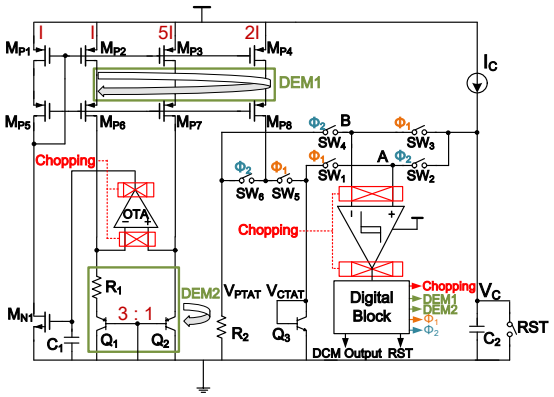

Fig. 2. Circuit diagram of the proposed design

Fig. 2 shows how V_{PTAT} and V_{CTAT} are generated, where $V_{PTAT} = 2 \cdot R_2 \cdot \Delta V_{BE}/R_1 = n \cdot \Delta V_{BE}$ and $V_{CTAT} = V_{BE}$. Assume $Y = V_{BE}/(n \cdot \Delta V_{BE})$, then

$$\mu = \frac{k \cdot n \cdot \Delta V_{BE}}{k \cdot n \cdot \Delta V_{BE} + V_{BE}} = \frac{k}{k + Y}, \tag{3}$$

where μ is a linear function of temperature, k is the curvature compensation coefficient in the digital domain [10]. Therefore, the temperature can be calculated as

$$T = A \cdot \mu + B, \tag{4}$$

where A and B are the temperature calculation coefficients and T is the temperature in Celsius.

Let $t_1 = t_h - t_{rst}$, $t_2 = t_l - t_{rst}$, combining equation (5)-(4), μ can be re-written as

$$\mu = \frac{k}{k + \frac{t_1}{t_2}} \tag{5}$$

and the temperature can be easily calculated by measuring the values of t_h and t_l from the DCM output.

B. Kelvin Connection for DEM of BJT

When generating ΔV_{BE}, DEM is a common technique to reduce the inaccuracy caused by elements mismatches [12]. In [10], DEM is applied to the BJTs to reduce the mismatch. However, the voltages that drop across the DEM switches will introduce errors when sensing ΔV_{BE}. From simulations, the temperature sensitivity of ΔV_{BE} is ~230 μV/°C, the on-resistance of single switch in this design is ~400 Ω; With a bias current of 400 nA, a 10% variation of on-resistance will induce a temperature error of ~0.3 °C. Increasing the size of the switches or decreasing the bias current may reduce the error, but these may degrade the accuracy due to the leakage current at high temperatures. Thus, KC-DEM is applied to solve this problem [13].

In Fig. 2, DEM2 is the place where KC-DEM is applied. Fig. 3 illustrates the details of KC-DEM and its simplified equivalent circuit, together with the timing diagram of self-controlled switch signals $ph\langle 3{:}0\rangle$ and their inverse ones $ph'\langle 3{:}0\rangle$. These signals are all derived from the DCM output. In KC-DEM, the input nodes of the OTA are directly connected to the BJT and resistors respectively through switches and there are no switch connections between the resistor and BJTs. Seen from the node X and Y, the OTA's inputs are high impedance nodes, thus the voltage-drops across the switches SW3 and SW4 are almost negligible.

In each phase of DEM, three branches of resistors are equivalently shunt and one branch is shorted in turn. Although such connection will increase the area of resistors, applying DEM to resistors can also reduce the spread of resistance ratio $n_0 = R_2/R_1$ in Fig. 2 given the effect of spread and mismatch in fabrication. The resistance of different branches can be described as $R_1 = (1+\delta_{1j}) \cdot \overline{R_1}$, $R_2 = (1+\delta_{2j}) \cdot \overline{R_2}$, where $\overline{R_1}$ and $\overline{R_2}$ are the average resistance of R_1, R_2 respectively, and δ_{1j}, δ_{2j} are the normalized deviations of $\overline{R_1}$, $\overline{R_2}$ respectively. Assume that the ideal resistance ratio is $n_0 = \overline{R_2}/\overline{R_1}$, the real ratio is $n_0{}' = R_2/R_1 \simeq (1 + \delta_{2j} - \delta_{1j}) \cdot n_0$ when no DEM is applied. The relative error between n_0 and $n_0{}'$ is

$$\frac{\Delta n_0}{n_0} = \frac{n_0{}' - n_0}{n_0} = \delta_{2j} - \delta_{1j}. \tag{6}$$

When m-phase DEM is applied, the resistance ratio is

$$n_0{}'' = n_0 \cdot (1 + \delta_{2j} - \frac{1}{m} \cdot \sum_{j=1}^{m} \delta_{1j}). \tag{7}$$

The relative error between n_0 and $n_0{}''$ is

$$\frac{\Delta n_0{}'}{n_0} = \frac{n_0{}'' - n_0}{n_0} = \delta_{2j} - \frac{1}{m} \cdot \sum_{j=1}^{m} \delta_{1j}. \tag{8}$$

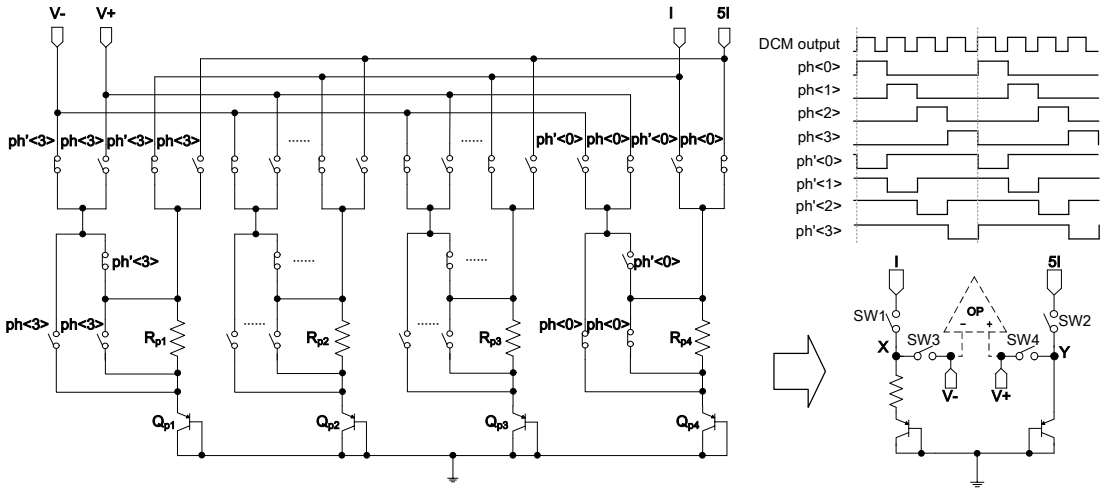

Fig. 3. Kelvin connection for the BJTs and simplified equivalent circuit

The standard deviation of $\Delta n_0/n_0$ and $\Delta n_0'/n_0$ are

$$\sigma(\frac{\Delta n_0}{n_0}) = \sqrt{\sigma^2(\delta_{1j}) + \sigma^2(\delta_{2j})}, \tag{9}$$

$$\sigma(\frac{\Delta n_0'}{n_0}) = \sqrt{\frac{\sigma^2(\delta_{1j})}{m} + \sigma^2(\delta_{2j})}, \tag{10}$$

where $\sigma(\delta_{1j})$ and $\sigma(\delta_{2j})$ are the standard deviation of δ_{1j} and δ_{2j} respectively. Equation (9) - (10) suggest that the deviation of resistance ratio can be reduced after m-phase DEM. Fig. 4 shows the simulation results, where m is 4 in the proposed design. From the 200-point Monte Carlo simulation results, the ideal resistance ratio n_0 in this design is 4.29. When R_1 is implemented with three shunt resistors, the equivalent resistance is the same as the original one, but the 3σ deviation of n_0 is reduced from 0.56% to 0.31%, suggesting a 46% improvement is achieved. Combining four-phase DEM, the 3σ deviation of n_0 is further reduced to 0.27%, which achieves a 52% improvement.

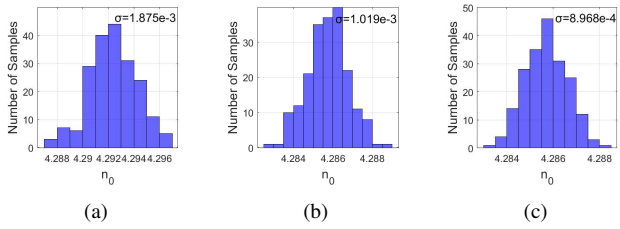

Fig. 4. 200-point Monte-Carlo simulation in circuit level when R_1 is implemented with (a) a single resistor; (b) three shunt resistors; (c) four-phase DEM

C. Robustness Enhancement

In [10], dynamic comparator is used and triggered by a tens of MHz clock. During one clock cycle, the charging capacitor needs to be reset, and the comparator's inputs have to be reconfigured and settled, resulting in a tight timing requirement. To relax these requirements, a continuous-time comparator is employed. With a similar digital logic circuit in [14], the comparator's output can be latched for a few system clock cycles for each flip, which releases the settling requirement of the front-end circuit, thereby higher energy efficiency can be achieved. Meanwhile, noise in the circuit may introduce chatter to the output of the comparator when V_C is close to V_{PTAT} or V_{CTAT}. Employing hysteresis can be useful to stabilize the output, but the traditional hysteresis comparator will induce comparing errors since the hysteresis also changes the desired switching point (V_{PTAT} or V_{CTAT} in this design). Thus, a continuous-time dynamic single-threshold hysteresis comparator is proposed to solve these problems, as shown in Fig. 5. In phase Φ_1, the comparator has no hysteresis when the output turns from logic high to logic low but it has a positive threshold voltage V_{TP} when the output reverses, i.e. flips from logic low to logic high. On the contrary, in phase Φ_2, the comparator has no hysteresis when output changes from logic low to logic high but has a negative threshold voltage V_{TN} when output reverses. Therefore, the proposed dynamic single-threshold hysteresis scheme does not change the switching point of the comparator and make the comparison more robust at the same time. According to the simulations, the comparator consumes about 9.2 μW.

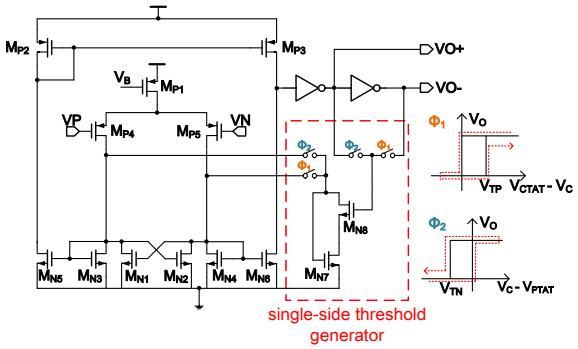

Fig. 5. Diagram of the continuous-time dynamic single-threshold hysteresis comparator

D. Techniques for Low Power and High Accuracy

In Fig. 2, Q_1 and Q_2 have an area ratio of 3:1 and the ratio of bias current through device M_{P2} and M_{P3} is 1:5, thus the temperature sensitivity of ΔV_{BE} will be higher and smaller resistance of R_2 is required. Besides BJTs, DEM is also applied in the current mirrors to generate accurate V_{PTAT} and V_{CTAT}. Instead of applying two branches of PNP transistors to compensate for the limited current gain β of 2 in the used 0.13-μm process [10], a NPN transistor is employed to generate V_{BE}, which can provide higher β of 9.8 and achieve higher accuracy than two branches of PNP transistors at the same bias current. The bias current I is about 360 nA at 27 °C to attain a similar β for Q_1 and Q_2. The OTA is a pMOS-input telescopic structure, which can easily obtain a high gain with less current compared to the folded-cascode one. Chopping is applied to both the OTA and the comparator to reduce the temperature errors caused by offset and 1/f noise. DEM and chopping signals are self-controlled by DCM output and are generated after the output of the comparator flips. Thus, the circuit has enough time to settle before next flip. The frequencies of chopping, DEM1, and DEM2 are f_{DCM}/2, f_{DCM}/8, f_{DCM}/4 respectively, where f_{DCM} is the frequency of DCM output.

When DEM and chopping are employed, switching ripples will introduce errors to the PTAT bias current. Therefore, in order to avoid the voltage errors on capacitor voltage V_C when charging the capacitor, the charging current is generated from an independent bias current circuit instead of the PTAT bias circuit in Fig.2. Using independent bias current to charge the capacitor can also relax the bandwidth requirement of the amplifier because the OTA is now only required to settle before V_C is approaches the V_{PTAT} or V_{CTAT}. The output frequency is about 5 kHz at room temperature, indicating that a bandwidth of 100 kHz is enough for the OTA. Meanwhile, the proposed design connects the output of OTA to a common source amplifier, which uses a diode-connected load and makes the gate of M_{P2} in Fig. 2 a low-impedance node. Thus lower bias current of OTA is needed to meet the load requirements [15] and the OTA finally draws 2 μA.

III. Measurement Results

The proposed temperature sensor is fabricated using a standard 0.13-μm CMOS process. Fig. 6 shows the die photograph of the prototype design. The sensor occupies a core area of 0.086 mm^2, including the core circuit, bias circuit, and control logic circuit. Sixteen sample chips are packaged and tested. The outputs of the chips are measured over a temperature range from -40 °C to 125 °C at an interval of 15 °C. A Pt-100 resistor, whose temperature inaccuracy is less than 30 mK, is placed next to the chips on the test board as the reference. A 20-MHz input clock is adopted in the logic control block to generate the capacitor-reset signal. The frequency of the DCM output of the proposed design varies from 4 kHz to 9 kHz over the temperature range of -40 °C to 125 °C. The output waveform is sampled by a logic analyzer and processed off-chip to get the ratio of logic-high time and logic-low time. In order to cancel all first-order mismatch errors caused by the component mismatch and offset [5], the results are averaged over eight successive periods of DCM output, corresponding to a conversion time of 1.3 ms. The temperature is then calculated through the equations (4) and (5). With 1000 successive readings, the proposed design shows a resolution of 60 mK (rms) at room temperature.

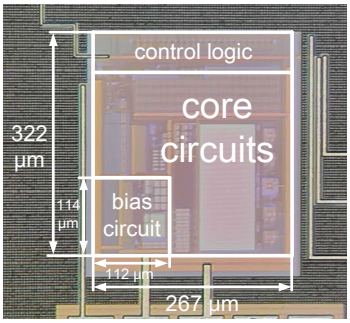

Fig. 6. Die photo of proposed design

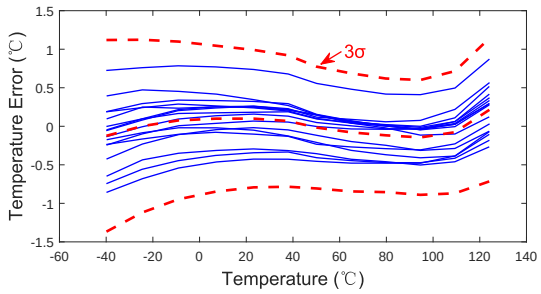

Fig. 7. Temperature error before calibration

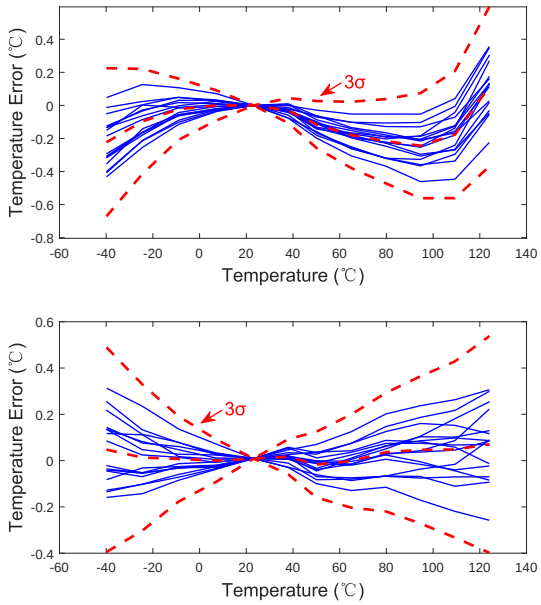

Fig. 8. (a) shows the temperature error after one-point calibration. (b) shows the temperature error after both one-point calibration and systematic error removal

Fig. 7 and Fig. 8 are the measurement results before and after calibration respectively. The 3σ temperature inaccuracy is

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameters	**This work**	[5]	[9]	[10]
Tech.(nm)	**130**	700	180	130
Type	**PNP&NPN**	PNP	NPN	PNP
ADC	**Duty-cycle**	Duty-cycle	Duty-cycle	Duty-cycle
Area (mm^2)	**0.086**	2.21	0.1	0.073
Temperature Range (°C)	**-40 to 125**	-45 to 130	-30 to 120	-10 to 100
Supply (V)	**1.2/3.3**	2.7-5.5	1.6-2	1.8-3.5
Power (μW)	**39.7**[*]	198[*]	0.9[*]	30.6[*]
Inaccuracy (°C)	**±0.54 (3σ)**	±0.3	±0.85 (3σ)	±0.38 (3σ)
Relative Inaccuracy (%)	**0.65**	0.34	1.13	0.69
Resolution (°C)	**0.06**	0.003	0.039	0.032
Conv. Time (ms)	**1.3**	1.8	8.1	2.4
Energy/ Conv. (nJ)	**51.6**	360	7	73
Acc. FoM (nJ%^{2})	**21.8**	41.62	8.94	34.76

[*] Excluding the off-chip counter. Simulation results show the counter consumes ∼10.6 μW when f_s=20 MHz in the target 0.13-μm CMOS process. Acc. FoM = Energy/Conversion × (Relative Inaccuracy)^2

-1.4 °C/1.2 °C without calibration. After one-point calibration, the 3σ temperature inaccuracy is -0.67 °C/0.6 °C, and the curves present the high order nonlinearity. The systematic non-linearity might be caused by the voltage sensitivity of the MOS capacitor which is used as the charging capacitor. Therefore, a fixed-coefficient fifth-order polynomial fitting is applied to remove the systematic error. The residual inaccuracy is then reduced to ±0.54 °C (3σ) from -40 °C to 125 °C, corresponding to a relative inaccuracy is 0.65%.

The proposed temperature sensor consumes 39.7 μW with 1.2 V/3.3 V (digital/analog) power supplies and attains an accuracy FoM of 21.8 nJ%^{2} [12]. At 25 °C, the sensor operates from a 2.1 V to 3.5V analog supply with a supply sensitivity of 0.21 V/°C. Table I summaries the performance of this work and compares it with state-of-the-art BJT-based DCM temperature sensors in CMOS technologies. The proposed design achieves a wider temperature range and a better relative inaccuracy than [9] and [10]. Compared to [5], it also attains a 1.9× improvement in accuracy FoM. This work achieves a good balance among accuracy, temperature range, and power consumption.

IV. CONCLUSION

A BJT-based CMOS temperature sensor with DCM output is designed and verified in a standard 0.13-μm CMOS process. KC-DEM is applied and a continuous-time dynamic single-threshold hysteresis comparator is proposed to improve the accuracy and enhance the robustness, leading to a ±0.54 °C (3σ) inaccuracy from -40 °C to 125 °C. It has an active area of 0.086 mm^2 and achieves a resolution of 60 mK with a conversion time of 1.3 ms, while consuming 39.7 μW.

REFERENCES

[1] S. Jeong, Z. Foo, Y. Lee, J. Y. Sim, D. Blaauw, and D. Sylvester, "A fully-integrated 71 nW CMOS temperature sensor for low power wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, 2014.

[2] R. Zhang, S. Fan, and L. Geng, "A near-zero-power temperature sensor with ±0.24 °C inaccuracy using only standard CMOS transistors for IoT applications," in *2018 IEEE ISCAS*, 2018, pp. 1–4.

[3] M. Eberlein and H. Pretl, "A no-trim, scaling-friendly thermal sensor in 16nm finfet using bulk diodes as sensing elements," in *ESSCIRC 2019 - IEEE 45th Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2019.

[4] K. Makinwa, "Smart temperature sensor survey," http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls, accessed: Apr. 2020.

[5] G. Wang, A. Heidari, K. A. A. Makinwa, and G. C. M. Meijer, "An accurate BJT-based CMOS temperature sensor with duty-cycle-modulated output," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1572–1580, 2017.

[6] B. Yousefzadeh and K. A. A. Makinwa, "9.3 A BJT-based temperature sensor with a packaging-robust inaccuracy of ±0.3 °C (3σ) from −55 °C to +125 °C after heater-assisted voltage calibration," in *2017 IEEE ISSCC*, 2017, pp. 162–163.

[7] B. Wang, M. Law, A. Bermak, and H. C. Luong, "A passive RFID tag embedded temperature sensor with improved process spreads immunity for a −30°C to 60°C sensing range," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 337–346, 2014.

[8] D. S. Lin and H. P. Hong, "A 0.5 V BJT-based CMOS thermal sensor in 10-nm FinFET technology," in *2017 IEEE A-SSCC*, 2017, pp. 41–44.

[9] B. Wang, M. Law, C. Tsui, and A. Bermak, "A 10.6 pJ · K^2 resolution FoM temperature sensor using astable multivibrator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 7, pp. 869–873, 2018.

[10] Z. Tang, Y. Fang, X. Yu, Z. Shi, and N. Tan, "Capacitor-reused CMOS temperature sensor with duty-cycle-modulated output and 0.38 °C (3σ) inaccuracy," *Electron. Lett.*, vol. 54, no. 9, pp. 568–570, 2018.

[11] Z. Tang, Y. Fang, X. Yu, Z. Shi, L. Lin, and N. N. Tan, "A dynamic-biased resistor-based CMOS temperature sensor with a duty-cycle-modulated output," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 9, pp. 1504–1508, 2020.

[12] K. Souri, Y. Chae, and K. A. A. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of ± 0.15°C (3σ) from −55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, 2013.

[13] M. Pertijs, K. Makinwa, and J. Huijsing, "A CMOS temperature sensor with a 3σ inaccuracy of ±0.1°C from -55°C to 125°C," in *2005 IEEE ISSCC*, 2005, pp. 238–596 Vol. 1.

[14] D. Zhu, J. Wang, L. Siek, C. L. Kok, L. Qiu, and Y. Zheng, "High accuracy time-mode duty-cycle-modulation-based temperature sensor for energy efficient system applications," in *2014 ISIC*, 2014, pp. 400–403.

[15] K. Souri and K. A. A. Makinwa, "A 0.12 mm^2 7.4 μW micropower temperature sensor with an inaccuracy of ±0.2 °C (3σ) from −30 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1693–1700, 2011.