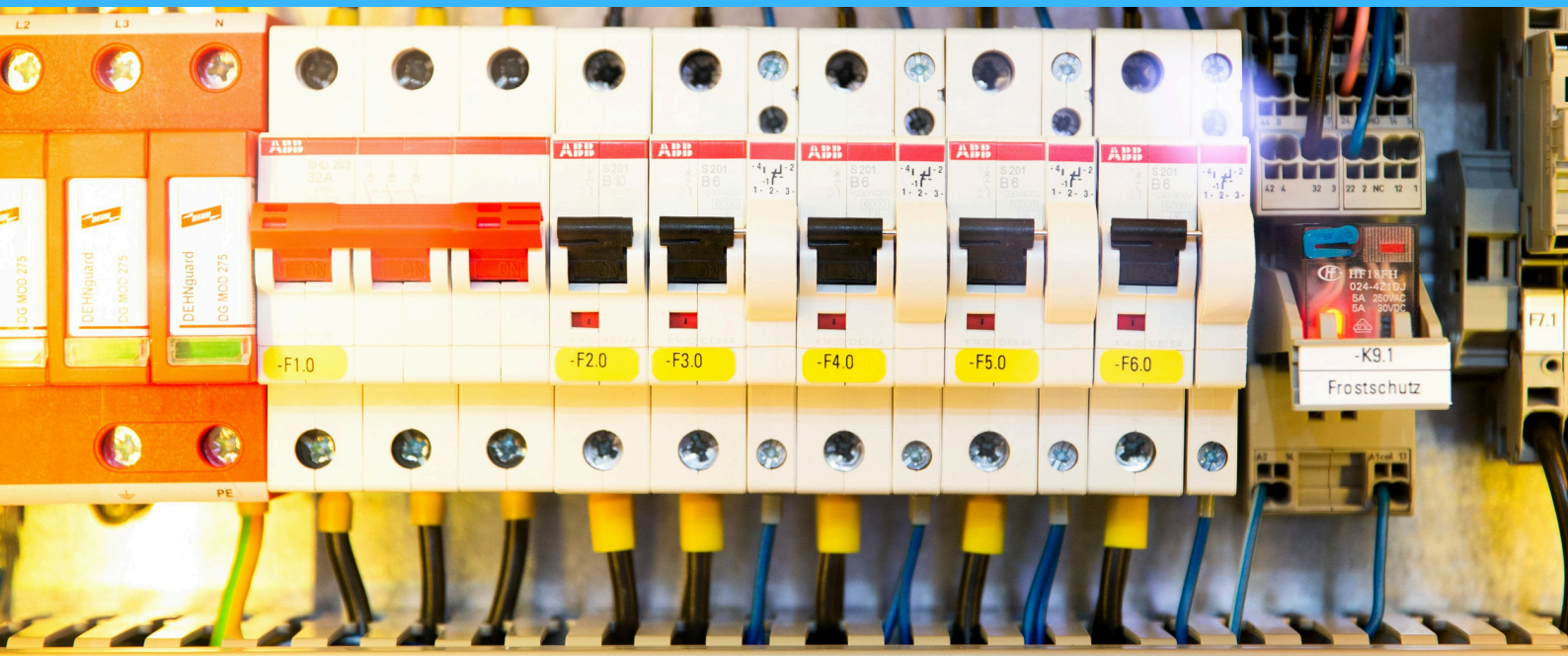
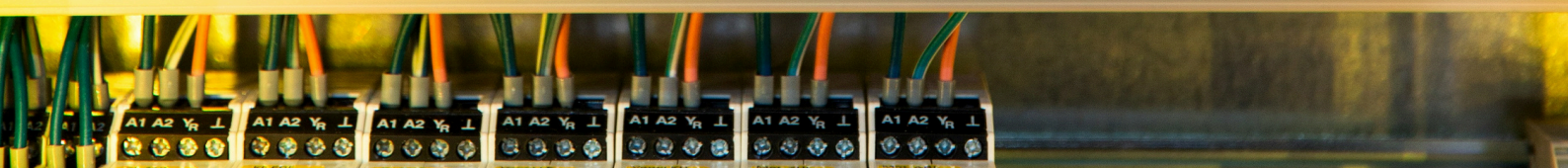


MASTER THESIS ON SHORT CIRCUIT ASSESSMENT



Kalpesh Jaikumar (5751721)



Short Circuit Assessment of Industrial Mains Distribution System: A Case Study of ASML

Kalpesh Jaikumar

in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering,
at the Delft University of Technology,
Faculty of Electrical Engineering, Mathematics and Computer Science,
to be defended publicly on Friday, August 30, 2024, at 10:00

Student Number:	5751721	
Project Duration:	October 2023 - August 2024	
Thesis committee:	Dr. Zian Qin	TU Delft
	Dr. Aditya Shekhar	TU Delft
	Dr. Qinwen Fan	TU Delft
	Mr. Miad Ahmadi	TU Delft
	Mr. Aleksandar Tankosic	ASML
	Mr. Arian de Bakker	ASML

An electronic version of this dissertation is available at
<http://repository.tudelft.nl/>.

ABSTRACT

With the increasing requirements of the semiconductor industry, ASML lithographic machines, essential for chip manufacturing, are becoming more complex. Consequently, the mains distribution system, a crucial part of these machines, is increasingly vulnerable to short circuit (SC) faults due to the growing number of system components. SC assessment of this system in compliance with international standards is vital as they are utilized by companies worldwide.

This thesis provides a standardized assessment method for industrial mains distribution system that complies with international standards. The assessment method includes the determination of available SC current and overall short circuit current rating (SCCR) and is implemented as a Matlab tool. Additionally, this thesis explores ways to increase the SCCR of the system by improving protection and limiting current considering current limiting alternating current circuit breakers and various direct current circuit breaker (DCCB) technologies, including fault current limiters. Finally, the assessment results are validated through the physical testing results of a branch circuit within the ASML mains distribution system.

ACKNOWLEDGEMENT

I would like to express my sincere gratitude to ASML for giving me this opportunity and trusting me with this project. The skills I acquired while working on this project are invaluable and will benefit me throughout my career.

I am incredibly appreciative of Aleksandar Tankosic, my supervisor at ASML, for his constant support and direction. I am so grateful to him for his invaluable assistance that words cannot truly express. I also want to thank Arian de Bakker, my manager at ASML, for all of his help and guidance with any problems I encountered upon.

I would want to thank all of the instructors at TU Delft who have taught me different courses throughout the course of my two years here. I am especially grateful to Dr. Aditya Shekhar, my supervisor at TU Delft, for helping me identify and address my weaknesses, which has allowed me to greatly improve my work. My sincere gratitude also goes out to Miad Ahmadi, my daily supervisor, whose advice and support have been invaluable throughout my thesis journey. His guidance will never be forgotten. Finally, I would like to thank Dr. Zian Qin and Dr. Qinwen Fan for accepting to be members of my thesis committee.

I owe a great debt of gratitude to my parents, who are a constant source of inspiration. I am eternally grateful for their support. I also wish to thank my classmates and friends for their encouragement and assistance during my challenging times at TU Delft.

*Kalpesh Jaikumar
Delft, August 2024*

CONTENTS

1	Introduction	1
1.1	About ASML	1
1.1.1	History of ASML	1
1.2	Motivation	2
1.3	Thesis Objective and Research Questions	2
1.4	Research Outcomes	5
1.5	Thesis Outline	5
2	International Standards For SC	7
2.1	NFPA 79	8
2.1.1	UL 508A	9
2.2	IEC 60204-1	9
2.2.1	IEC 61439-1	9
2.2.2	IEC 60909-0	10
2.2.3	IEC 60865-1	10
2.3	Semi S22	10
2.4	Conclusion	10
3	AC SC Study	12
3.1	Introduction	12
3.2	AC SC Current Calculation	13
3.2.1	AC SC Faults	13
3.2.2	Symmetrical Components	14
3.2.3	Superposition Principle Method	15
3.2.4	Proposed Calculation Method	16
3.2.5	Verification	22
3.3	Determination of SCCR	23
3.4	Conclusion	23
4	AC SC Protection	24
4.1	AC Mechanical CBs	24

4.1.1	Arc Voltage	25
4.1.2	TRV	26
4.2	Current Limiting AC CBs	28
4.2.1	Need for Limitation	28
4.2.2	Conditions for Current Limitation	29
4.2.3	Cascading	30
4.3	Comparison	30
4.3.1	SCCR	31
4.3.2	Mechanical Stress	31
4.3.3	Effect on TRV	31
4.3.4	Peak Current and Interruption Time	32
4.3.5	Cost	32
4.4	Conclusion	32
5	DC SC Study	33
5.1	Fault Current from DC Voltage Source	33
5.2	Fault Current from AC Voltage Source	34
5.2.1	Two-level VSC	35
5.2.2	Current Calculation	37
5.2.3	Verification	40
5.3	Conclusion	41
6	DC SC Protection	42
6.1	DC Mechanical CB	43
6.2	SSCB	45
6.2.1	Power Semiconductor Technology	46
6.2.2	Voltage Clamping Circuit	47
6.3	Hybrid CBs	47
6.4	DC FCL	49
6.4.1	Resistive Type FCL	49
6.4.2	Inductive Type FCL	50
6.5	Comparison	51
6.5.1	Complexity	52
6.5.2	Number of Components (N)	52
6.5.3	Fault Interruption Time (t)	52
6.5.4	Cost	52
6.5.5	Conduction Power Loss (P_L)	52
6.6	Conclusion	52
7	Design of SC Assessment Tool	54
7.1	Introduction	54
7.2	Software Architecture	54
7.2.1	User Interface (UI) layer	55
7.2.2	Simulation Engine Layer	57
7.2.3	Data Handling Layer	58
7.3	Conclusion	59

8 Case Study ASML	60
8.1 The System	60
8.2 Comparison of Results	61
8.3 Conclusion	63
9 Conclusion	64
A Current Limiting CB	66
B Park Transformation	68
C Tool Results	69

LIST OF TABLES

3.1	Types of three phase SC faults	14
3.2	voltage factor c	18
3.3	Three phase fault results	22
4.1	Cost analysis	32
5.1	DC fault results	40
6.1	Comparison of Si, SiC and GaN [49]	46
7.1	Summary of the tool panels	57
7.2	Summary of component modeling	59
8.1	Components in the circuit	60
8.2	Comparison of results	62

LIST OF FIGURES

1.1	ASML system[2]	2
1.2	System assessment	3
1.3	Thesis outline	6
2.1	Standards around the world	7
2.2	Overview and connection between the standards	11
3.1	Series RL circuit connected to an AC voltage source	12
3.2	Peak SC current variations	13
3.3	Symmetrical components	15
3.4	Superposition method	16
3.5	Calculation steps	17
3.6	Equivalent circuit using IEC 60909 method	17
3.7	AC SC current [3]	20
3.8	Verification of calculation and simulation	22
3.9	Sensitivity analysis to find $\frac{X}{R}$	22
4.1	Arc voltage	25
4.2	TRV	26
4.3	Equivalent single phase circuit	27
4.4	Variation of peak TRV with system voltage	27
4.5	AC short circuit current limitation	28
4.6	Single phase representation of a system	28
4.7	Limited short circuit current [28]	29
4.8	Effect of cascading	30
4.9	Comparison overview of parameters, where n is the number of CBs in series	31
4.10	Variation of peak TRV with breaker resistance	32
5.1	Boost converter	34
5.2	DC fault current from a DC voltage source	34
5.3	Two level VSC	35
5.4	Controller in dq frame	36

5.5	PLL controller	36
5.6	Inner controller	37
5.7	Outer controllers	37
5.8	DC fault analysis	38
5.9	Capacitor discharge stage	38
5.10	Diode freewheel Stage	39
5.11	Grid feeding stage	40
5.12	Verification of calculation and simulation	40
6.1	DC fault interruption	42
6.2	LC path	43
6.3	LC oscillation response	43
6.4	DC mechanical CB	44
6.5	Comparison of current in DC mechanical CBs with and without SSCB.	44
6.6	Components of SSCB [10]	45
6.7	Comparison of current in DC SSCBs with and without SSCB.	46
6.8	Basic hybrid CB	48
6.9	Types of hybrid DC CB commutation	49
6.10	Effect of resistive FCL	50
6.11	Effect of inductive FCL	50
6.12	Solid state FCL	51
6.13	Overview of the comparison of DC protection technologies	52
7.1	Layer based architecture	55
7.2	Tool UI	55
7.3	SC current panel	56
8.1	Branch circuit of ASML mains distribution system	61
8.2	SC current without CB	62
8.3	SC current with current limiting CB	62
A.1	Peak let-through current of Eaton NZMN series from datasheet	66
A.2	Peak let through energy of Eaton NZMN series from datasheet	67
C.1	Result 1	69
C.2	Result 2	70
C.3	Result 3	70
C.4	Result 4	71
C.5	Result 5	71

INTRODUCTION

ELECTRONIC devices such as personal computers (PCs), smartphones, and gaming consoles are experiencing significant advancements in processing power, largely attributed to the microchips embedded within them. These microchips are increasingly equipped with more components, notably transistors, enhancing their computational capabilities while maintaining a compact form factor. Moore's Law, initially postulated by Gordon Moore, a co-founder of Intel, in 1965, accurately projected the ongoing escalation in the transistor count within individual microchips, a principle that remains relevant in contemporary times. Present-day microchips have the capacity to accommodate tens or even hundreds of transistors [1]. The year 2021 witnessed a remarkable milestone in the semiconductor industry, as unit sales reached an unprecedented 1.15 trillion shipments [2]. Photo lithographic technology stands as the predominant method employed in microchip fabrication, involving six fundamental stages: deposition, application of photoresist, lithography, etching, ionization, and packaging.

1.1 About ASML

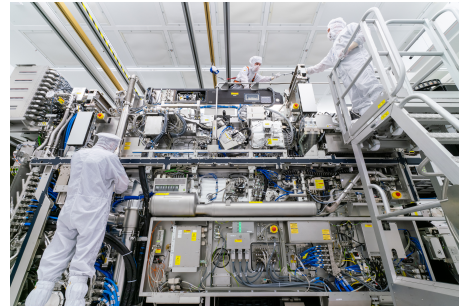
ASML is the leading manufacturer of photolithography machines. The technology used in these machines is complex and requires many steps to manufacture a chip. The machine consists of multiple cabins or panels to perform various functions, and the power system in each panel is becoming more complex due to increasingly advanced and powerful chip requirements. One of ASML's machines, the NXE 3400, is shown in Figure 1.1a and the complex power system of the machine is depicted in Figure 1.1b.

1.1.1 History of ASML

In 1984, Philips and chip-machine manufacturer Advanced Semiconductor Materials International (ASMI) established ASM Lithography, a company aimed at developing lithography systems for the expanding semiconductor market. In 1990, they launched the PAS 5500, a breakthrough platform that remains in use today. In the 2010s, they introduced EUV lithography technology. Now, they continue to advance and improve technologies



(a) NXE 3400



(b) Power system

Figure 1.1: ASML system[2]

to meet the ever-growing demands of the semiconductor industry.

1.2 Motivation

The mains distribution system in the ASML machine consists of a mains panel connected to the grid, which in turn connects to various panels performing different functions within the machine. This distribution system is becoming increasingly complex due to rising industry demands and enhanced functionalities, leading to a surge in the number of components. Consequently, the probability of short circuit (SC) faults within the system is increasing.

The increase in SC faults has detrimental effects, such as destroying components sensitive to high currents, system breakdowns, and fire hazards, potentially leading to significant financial losses for ASML, amounting to thousands of euros. SC faults can occur on both the alternating current (AC) and direct current (DC) sides, resulting in different transients. Moreover, as the machines are deployed globally, they must comply with various international standards, each with distinct requirements.

Currently at ASML, there is no standardized approach for assessment¹ of the system for SC faults during the design stage. This can lead to confusion about which method to use to check compliance with international standards. The results from the assessment are important as they are used during the physical testing of the system. Therefore, this thesis aims to standardize the methods for assessment and improve the protection of the mains distribution system. However, most theories and results can be applied to various low-voltage systems.

1.3 Thesis Objective and Research Questions

The main objective of this thesis is

¹Assessment involves determining the SC current at the location of the fault, short circuit current rating (SCCR) of the system and checking if the system can withstand the SC fault.

To standardize methods for SC assessment and increase the SCCR of industrial mains distribution systems.

The assessment is based on compliance with various international standards for SCs, such as IEC and NFPA. The steps involved in the system assessment are shown in Figure 1.2.

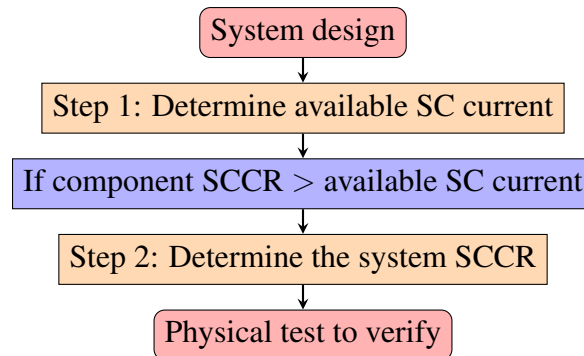


Figure 1.2: System assessment

The main focus of this thesis is to standardize methods for the determination of SC current and SCCR of the system complying with the international standards and to study different protection mechanisms that can improve the protection and limit the current thereby increasing the SCCR of the system².

To achieve this main objective, the research will address several key sub-objectives, each of which can be derived into research questions as follows:

Sub-objective 1: Study of international standards

- **Research question 1:** *What are the differences and similarities among the international standards for SC?*

Different international standards have to be complied by industrial machinery such as IEC and NFPA. Semi S22 is also a standard focused only on semiconductor machinery.

There is no literature explaining the connection and difference between different standards for SC analysis. Therefore, a comprehensive analysis of IEC, NFPA and Semi S22 standards is presented in Chapter 2. This analysis helps in obtaining a standardized method for system assessment.

Sub-objective 2: Determination of standardized methods

- **Research question 2:** *How should AC SC current be calculated?*

To improve the protection of the distribution system, it is necessary to calculate the available SC current accurately so that sufficiently rated protection devices can be used. Different components need to be modeled to calculate the SC current.

²Increase in system SCCR is an advantage as high currents can be applied without affecting the system and can be used for a wider range of applications

The superposition theorem can be used to calculate the SC current. However, there are many disadvantages to using this method, which are explained in Chapter 3. The IEC [3] standard provides a comprehensive method to calculate the SC current, but the current from the feeder network must be known, which is not always the case in physical systems, including those at ASML. The main challenge lies in finding a calculation method that complies with both international standards, as their requirements differ. Therefore, a calculation method to determine the SC current that complies with both standards is presented in Chapter 3.

- **Research question 3:** *How should DC SC current be calculated?*

In the literature, most research explains DC SC faults based on numerical simulations. However, the authors in [4] provide a theoretical calculation method for the DC side SC current for a two-level converter for a high voltage system. Based on this, a theoretical SC current calculation method for low voltage systems is presented in Chapter 5, which aligns with the numerical simulation results.

- **Research question 4:** *How should the SCCR of the system be determined?*

To determine the SCCR, both [5] and [6] are considered and a standardized method is presented in Chapter 3.

Sub-objective 3: Evaluation and improvement of system protection

- **Research question 5:** *How can AC SC protection be improved?*

With AC mechanical circuit breaker (CB), the breaker opening time consists of relaying and interruption time. Using fast relays makes it possible to achieve fault clearance in three cycles of 50 Hz, which is 0.06 seconds [7]. However, due to the increasing number of conductors and elements in the system, more components are affected by the thermal and mechanical stress caused by SC faults. This can lead to serious consequences if not interrupted quickly.

Current-limiting AC mechanical CBs can replace traditional CBs. They limit the overall peak SC current and have a quicker fault-clearing time. Therefore, the use of current-limiting AC mechanical CBs and their advantages comparing various parameters are presented in Chapter 4.

- **Research question 6:** *How can DC SC protection be improved?*

The problem with DC fault interruption is that there is no zero crossing of the SC current. When a DC fault occurs, there is a sudden current increase and a voltage drop across the DC bus. This leads to high currents on the freewheeling body diodes in the VSC converter, affecting them, and the high-frequency transients affect the system's stability. Therefore, it is important to have a quick fault response.

In the literature, AC-side CBs can be used [8], but the problem is that the AC breaker is slow, and the DC would have already reached its peak. A DC mechanical CB with a parallel LC network to create artificial zero currents is explained in [9]. Authors in [10],[11], and [12] have explained the use of solid-state circuit breakers (SSCB), hybrid CBs, and fault current limiters and [12] have explained the use of

solid-state circuit breakers (SSCB), hybrid CBs and fault current limiters(FCL) respectively. A comparison between mechanical, hybrid, and SSCBs for high-voltage systems is discussed in [13]. However, there is limited literature on the comparison between DC mechanical, hybrid, solid-state, and DC FCL for low-voltage systems. Chapter 6 aims to compare different protection measures.

Sub-objective 4: Validation of results

- **Research question 7:** *How can the results be validated?*

An SC scenario in a branch circuit of the ASML mains distribution system is considered to validate the methods. The physical test results are compared with the numerical simulation results.

ASML has no standardized tool to assess the systems for SC faults during the design phase. Therefore, a Matlab tool has been developed specifically for this purpose. While tools such as the Eaton Bussmann FC app and the Rockwell Automation SCCR tool [14] are available on the internet, they do not use standardized calculation methods. Chapter 7 explains the development of the Matlab tool for testing the system, and Chapter 8 focuses on validating the results.

1.4 Research Outcomes

The outcomes of this master thesis are summarized below

- **Chapter 2:** Comprehensive analysis of IEC, NFPA and Semi S22 standards for SC.
- **Chapter 3:** Standardized methods to determine AC SC currents and SCCR to assess the system.
- **Chapter 4:** Comparison of standard and current limiting AC CBs.
- **Chapter 5:** Theoretical equations for DC SC current calculation that match numerical simulation values.
- **Chapter 6:** Comparison of different DC protection methods for low voltage systems.
- **Chapter 7:** Tool to assess the design of industrial mains distribution system.

1.5 Thesis Outline

The outline of this thesis and the relation between the chapters are shown in Figure 1.3.

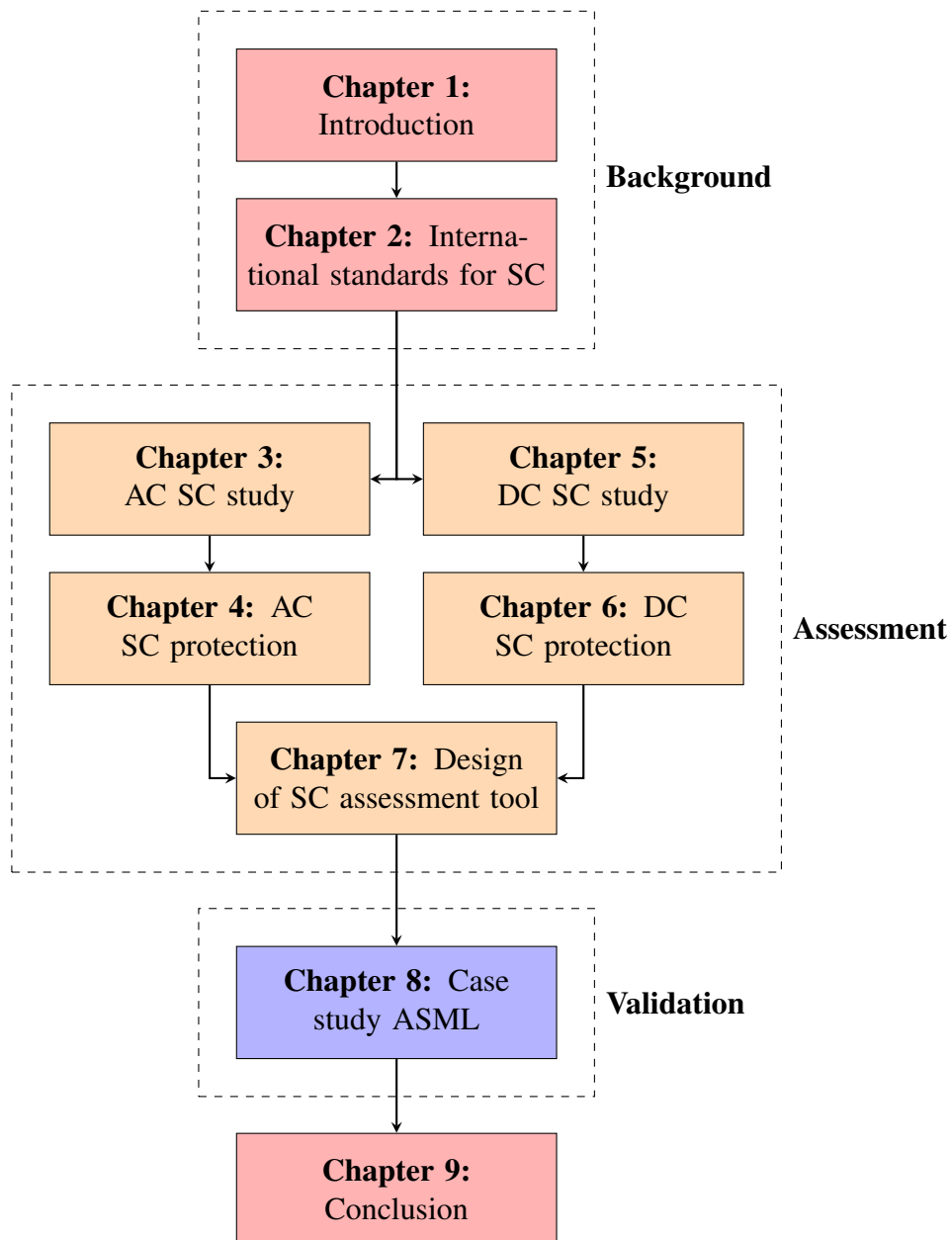


Figure 1.3: Thesis outline

INTERNATIONAL STANDARDS FOR SC

ASML Lithographic machines are being produced and widely used by several customers worldwide and they must comply with different international standards adopted by the region where the customer is located. Standards to be followed in different parts of the world are shown in 2.1.

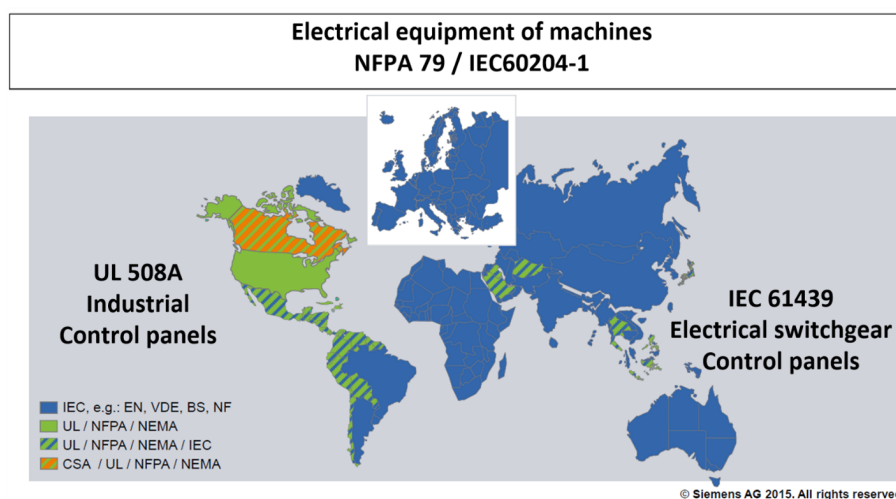


Figure 2.1: Standards around the world

From the figure, it can be seen that for industrial machinery **IEC60204-1** standard is adopted in most of the world except the North American region where **NFPA 79** is the standard that should be followed. Each standard has its own safety and SC requirements and given the global distribution of ASML machines, compliance with both IEC and NFPA standards is important to ensure consistency and meet regulatory obligations across diverse markets.

Apart from the above-mentioned standards, ASML as a semiconductor equipment manufacturer shall comply with industry-specific standards. **Semi S22** is a standard specific to the semiconductor industry and will be investigated for SC requirements. The comparison between the standards is shown in Figure 2.2. As seen from Figure 2.2, the main high-level standards NFPA 79, IEC 60204-1 and Semi S22 are interlinked and point to

different standards with different scopes regarding system requirements.

The summary of standards is as follows:

- **SC current calculation:**
 - **IEC 60909-0** SC currents in three-phase AC systems - Part 0: Calculation of currents
 - * **IEC 60909-1** SC currents in three-phase Part 1: Factors for the calculation of SC currents according to IEC 60909-0 a.c. systems
 - * **IEC 60909-4** SC currents in three-phase AC systems – Part 4: Examples for the calculation of SC currents
 - **UL 508A** Industrial Control Panels.
 - **Semi S22** Safety Guideline for the Electrical Design of Semiconductor Manufacturing Equipment
- **Calculation of effects of SC:**
 - **IEC 60865-1** SC currents - Calculation of effects - Part 1: Definitions and calculation method
- **SCCR of the design**
 - **UL508A** Industrial Control Panels.
 - **UL 67** Panelboards
 - **IEC 61439-1** Low-voltage switchgear and control gear assemblies - Part 1: General rules
 - **Semi S22** Safety Guideline for the Electrical Design of Semiconductor Manufacturing Equipment

The overview and comparison between different standards are shown in Figure 2.2. A thorough study of all the standards is done, and the parts that are relevant to the scope are explained in the subsequent sections.

2.1 NFPA 79

This standard provides requirements for the application of electrical/electronic equipment or systems supplied as part of industrial machines that will promote the safety of life and property. According to this standard, The SCCR of a system can be determined using the method given in UL 508A [15], which is explained in the next section.

2.1.1 UL 508A

UL508A is a standard for the safety of industrial control panels. This standard gives a method to determine the SCCR of the system to assess the design.

According to this standard, the SCCR of the control panel can be determined in three steps which are briefly given below and are explained further in Chapter 3:

1. Establishing the SCCR of individual power circuit components.
2. Modifying the available SC current within a portion of a circuit in the panel due to the presence of current-limiting components.
3. Determining the overall panel SCCR.

According to NFPA 79, for semiconductor manufacturing equipment industry assessment done by certified external laboratory by IEC or Semi S22 standards can be accepted. The IEC and Semi S22 standards are explained in the next section.

2.2 IEC 60204-1

IEC 60204-1 is a standard dealing with the safety of machinery.

This standard points to standard IEC 60909-0 [3] that provides a method to determine the available SC current and to IEC 61439-1 [16], that does not give any method to determine the SCCR of the system, but it does explain how to test the system. Although this standard does not explain a method to determine the SCCR of the system, it points to standard UL 508A [15] where a method is explained.

2.2.1 IEC 61439-1

This standard is applicable for low-voltage switchgear and control gear assemblies.

This standard does not specify any method to determine the SCCR of the system. Instead, it provides verification methods that can be used to verify the SC withstand strength. This verification step is the next step after the assessment step to validate the assessment.

According to this standard, the verification can be done by three ways:

- Verification by comparison with a reference design – Using a checklist.
- Verification by comparison with a reference design(s) – Using calculation.
- Verification by test.

2.2.2 IEC 60909-0

IEC 60909-0 is a standard for SC currents in three-phase AC systems. This standard gives a calculation method to determine SC currents in a three phase AC system. This calculation method is used as the base for the standardized method, which explained in Chapter 3.

Standard IEC 60909-1 acts as a supplement to this standard, explaining about the factors and assumptions used.

2.2.3 IEC 60865-1

IEC 60865-1 is a standard that is concerned with the effects of SC faults. This standard gives methods to calculate the thermal and mechanical stress in the system due to SC faults. These methods are explained in Chapter 4.

2.3 Semi S22

Semi S22 is the standard to provide safety guidelines for the electrical design of semiconductor manufacturing equipment. This standard provides a point-to-point method for calculating the SC current and SCCR. However, IEC and NFPA standards are preferred at ASML due to the limited scope of this standard and limited availability of testing laboratory certified by this standard. Therefore they are not further considered in this thesis.

2.4 Conclusion

In this chapter, a comprehensive analysis of international standards for SC was conducted. The similarities and differences between the IEC, NFPA, and Semi S22 standards were examined and are shown in Figure 2.2. This analysis directly addresses research question 1 by providing a detailed comparison of the standards. It also serves as a foundation for determining standardized assessment methods, which will be elaborated upon in the subsequent chapters.

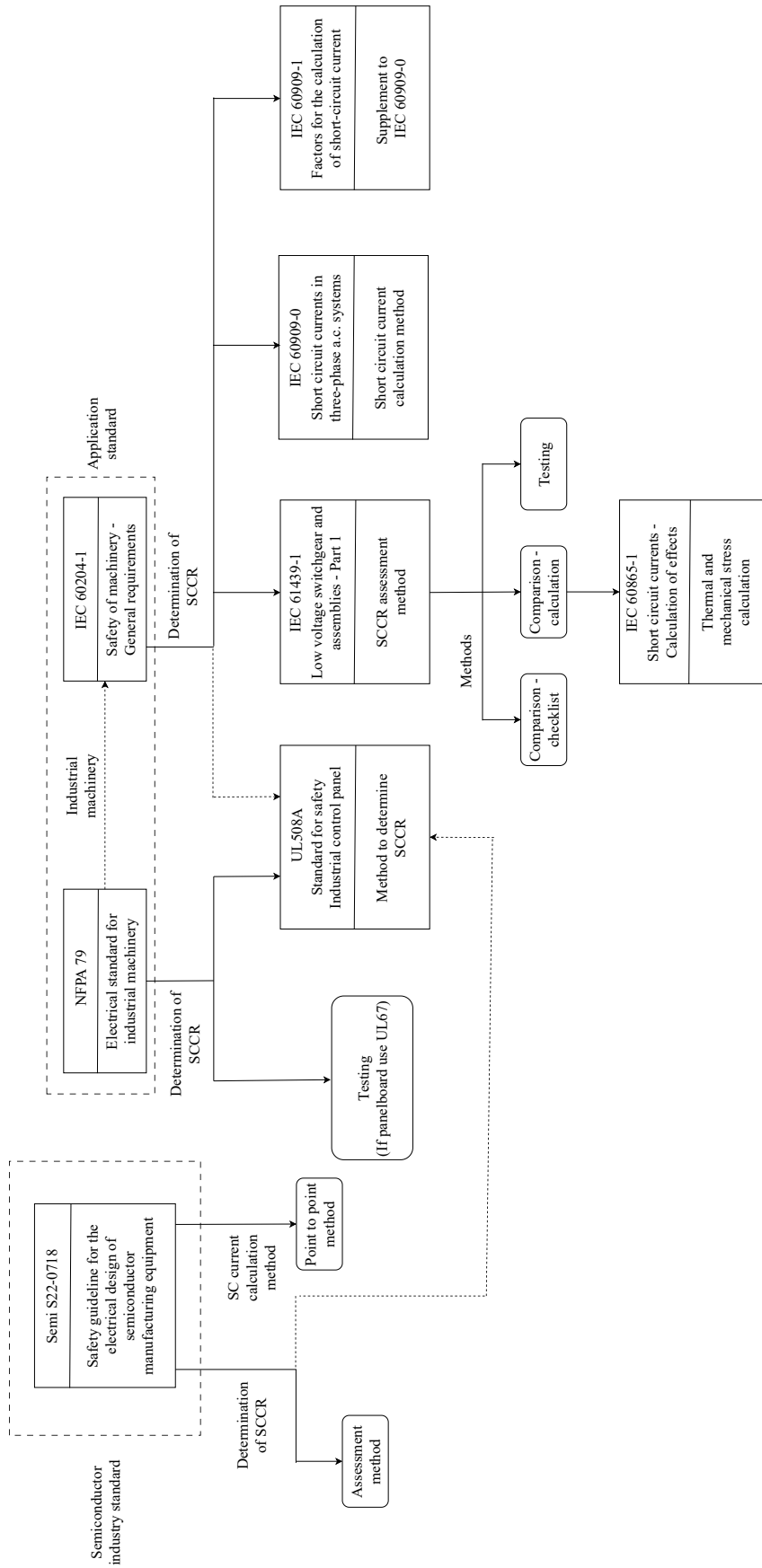


Figure 2.2: Overview and connection between the standards

AC SC STUDY

THE steps involved in assessing AC systems are determining available SC currents and system SCCR. This chapter reviews the literature on the AC SC current and SCCR determination methods and presents a standardized method.

3.1 Introduction

An equivalent circuit is shown in Figure 3.1 to understand the behavior of an AC SC in a power system. This circuit representation includes an inductance L , which is realistic since SCs are mostly inductive due to the energy stored in the magnetic field of the components [17]. The losses in the system can be represented by the resistance R . By applying Kirchhoff's Voltage Law (KVL) to the circuit, Equation 3.1 is obtained:

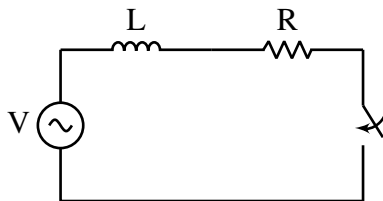


Figure 3.1: Series RL circuit connected to an AC voltage source

$$Ri(t) + L\frac{di(t)}{dt} = V_m \sin(\omega t + \alpha) \quad (3.1)$$

Where α is the difference between the voltage angle when the fault occurred and the voltage zero crossing.

Solving the above equation according to [18] leads to the equation

$$i(t) = \frac{V_m}{|Z|} (\sin(\omega t + \alpha - \theta) - \sin(\alpha - \theta)e^{-\frac{Rt}{L}}) \quad (3.2)$$

where, $\theta = \tan^{-1}(\frac{\omega L}{R})$ is the power factor angle. Z is the impedance and is given by $|Z| = \sqrt{R^2 + (\omega L)^2}$

The current $i(t)$ has an AC component $i_{AC}(t)$ which is symmetrical and a DC component $i_{DC}(t)$ characterized by $e^{-\frac{Rt}{L}}$ that decays with time. The two currents can be represented as

$$i(t) = i_{AC}(t) + i_{DC}(t) \quad (3.3)$$

Usually, in a power system, as the reactance of the system is high compared to the resistance, the power factor angle θ can be approximated to $\pi/2$. For the DC component to be zero, there are two cases as per equation 3.2:

- $\sin(\alpha - \theta)$ is zero - In this case, since θ is equal to $\pm\pi/2$, α should also be equal to $\pm\pi/2$. This shows that if the fault occurs at an instant when the voltage is maximum, the DC component does not exist, and the current is symmetrical.
- $e^{-\frac{Rt}{L}}$ can never be equal to zero; however, as the time t or the ratio of $\frac{R}{L}$ increases, it decays faster and goes very close to zero, making the current symmetrical.

The DC component is maximum when the term $\sin(\alpha - \theta)$ is one, this means as θ is equal to $\pm\pi/2$, α should be equal to 0 or $\pm\pi$. This shows the DC component is maximum, and the current becomes asymmetrical with maximum instantaneous peak value. The instantaneous peak current decreases as the fault angle concerning the voltage waveform changes between 0 and $\pi/2$. This is represented in the Figure 3.2.

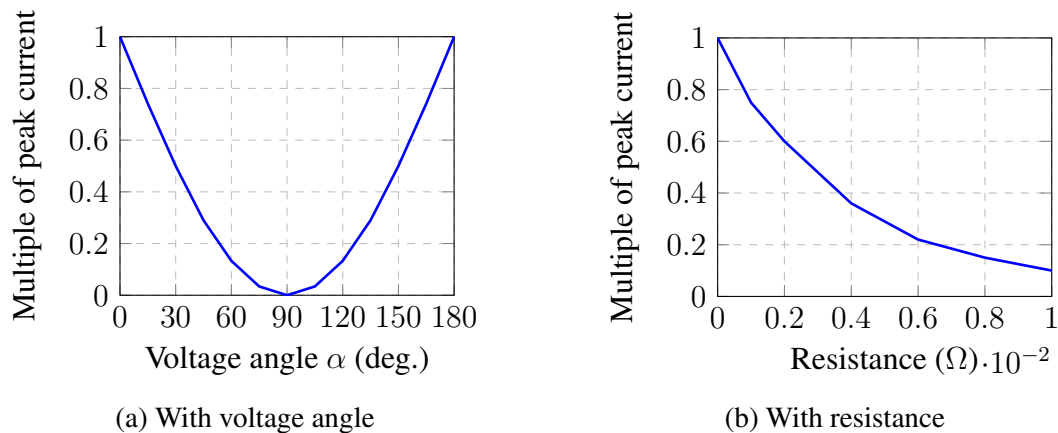


Figure 3.2: Peak SC current variations

3.2 AC SC Current Calculation

This section deals with different faults that can occur in a three-phase AC system and the calculation method to find the available SC current during each fault.

3.2.1 AC SC Faults

The faults in a three-phase system are classified as symmetrical and unsymmetrical faults [19]. These faults are shown in Figure 3.1. The three-phase-to-ground fault is a type of symmetrical fault where an SC fault occurs in all three phases. This is a balanced fault

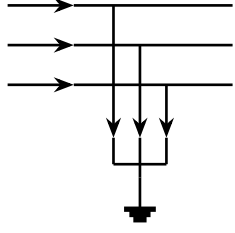
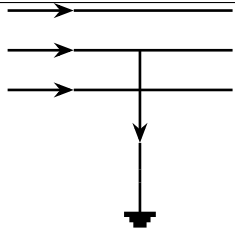
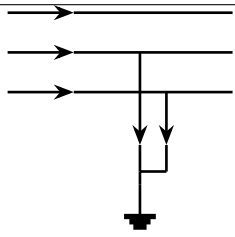
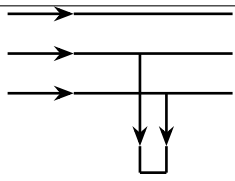
Three-phase-to-ground	
Line-to-ground	
Double line-to-ground	
Line-to-line	

Table 3.1: Types of three phase SC faults

where equal current flows in all three phases and only the phase differs. Each phase can be solved separately. However, this is the most severe type of fault in a power system [19].

The line-to-line, the double line-to-ground, and the line-to-ground SC faults are unsymmetrical faults as the current is different in the three phases. These unbalanced faults can be solved by representing them as a set of three symmetrical components, as explained in the next section. Single phase to ground is the most frequent fault in a power system.

3.2.2 Symmetrical Components

There are many methods in the Literature, such as the compensation method [20] and the rigid approach [21] for solving unbalanced systems. However, the symmetrical components method, introduced by Dr. C. L. Fortescue at the American Institute of Electrical Engineers meeting in 1914 [22], is the most used. Fortescue's work proves that an unbalanced system of n phasors can be transformed into n systems of balanced phasors called symmetrical components [23]. These phasors are equal in length, and the angle between them is the same. According to this theorem, an unbalanced three-phase system can be represented by three balanced components:

- **Positive Sequence Component**

The positive component shown in figure 3.3a, have balanced and symmetrical ar-

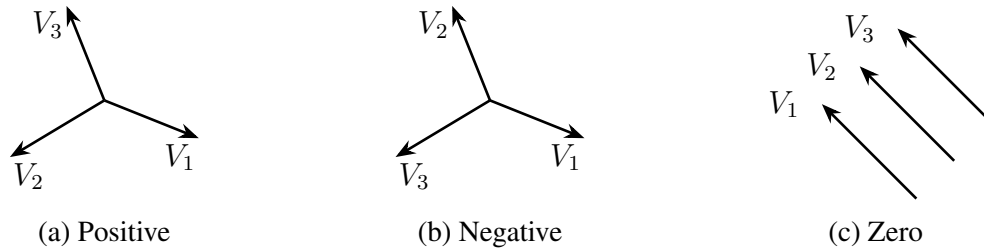


Figure 3.3: Symmetrical components

rearrangement of vectors and an observer at rest will see the vector in the order $\vec{V}_1, \vec{V}_2, \vec{V}_3$, which is in the same sequence as original system.

- **Negative Sequence Component**

The negative component shown in figure 3.3b has a balanced and symmetrical arrangement of vectors, and an observer at rest will see the vector in the order $\vec{V}_1, \vec{V}_3, \vec{V}_2$, which is in the opposite sequence as the original system.

- **Zero Sequence Component**

The zero sequence component shown in figure 3.3c, have vectors with same amplitude and co-linear and an observer will see the vectors passing simultaneously.

Consider a set of three voltage phasors, which can be represented as the sum of their components as,

$$V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V_{a,0} \\ V_{b,0} \\ V_{c,0} \end{bmatrix} + \begin{bmatrix} V_{a,+} \\ V_{b,+} \\ V_{c,+} \end{bmatrix} + \begin{bmatrix} V_{a,-} \\ V_{b,-} \\ V_{c,-} \end{bmatrix} \quad (3.4)$$

Considering V_a as the origin and using the operator 'a', where $a = e^{j\frac{2\pi}{3}}$, the following expression is obtained

$$V_{abc} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} V_0 \\ V_+ \\ V_- \end{bmatrix} = \mathbf{V}I_{0+-} \quad (3.5)$$

Where \mathbf{A} is the transformation matrix.

Faults can be represented by their sequence circuits as explained in [19] and [23].

3.2.3 Superposition Principle Method

The superposition method as explained in [24][25] is a method for calculating SC currents. It consists of three steps as follows and is also shown in Figure 3.4:

- The equivalent circuit is considered, and the pre-fault voltage across the fault location is calculated
- Since the voltage across a fault is close to zero, it is assumed that the fault acts as a voltage source with the same magnitude as the pre-fault voltage with opposite polarity. The equivalent circuit consists of the pre-fault voltage with all other voltages short-circuited. Then, steady-state currents and voltages are calculated.

- Both circuits are superposed so that the equivalent voltage at the fault location is zero. The voltages and currents are represented as the sum of the two circuits. This gives the overall SC current due to the fault.

The pre-fault voltage across the fault is the most important factor determining the SC current. However, the variations during operation in a three-phase AC system are very large. In a given system, there are as many different SC current magnitudes as possible and different load-flow conditions for every location. Normally, extreme load-flow cases are not known [24]. Moreover, the steady-state condition must be specified. The entire network's data are often difficult to determine [26].

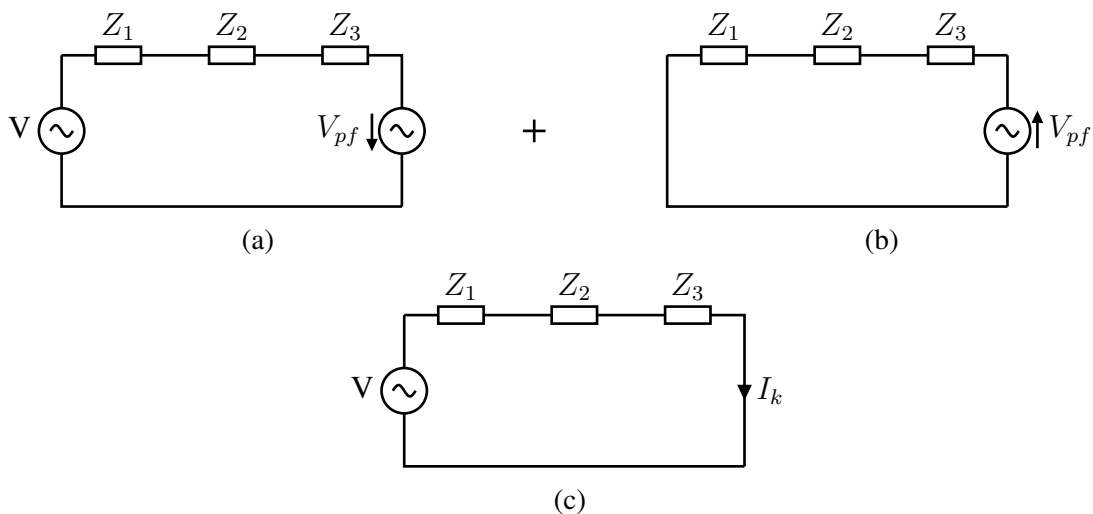


Figure 3.4: Superposition method

3.2.4 Proposed Calculation Method

The proposed AC SC current calculation method is based on IEC 60909-0 and UL 508A. The IEC 60909-0 method is derived from the superposition method and provides a procedure for calculating SC currents without calculating the pre-fault current and voltages. This is valid because the currents due to SCs are very high compared to pre-fault currents. According to this method, an equivalent voltage source with the nominal system voltage along with a factor c is introduced at the fault location, and that is the only active voltage source in the system, the remaining sources being short-circuited, and the components in the system are replaced by their internal impedances [3]. An example of the IEC 60909-0 representation is shown in Figure 3.6.

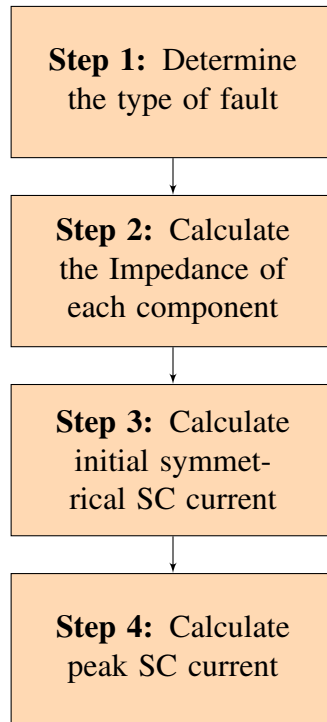


Figure 3.5: Calculation steps

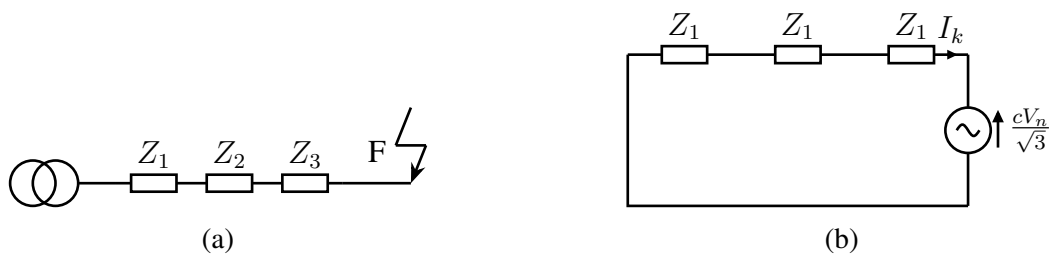


Figure 3.6: Equivalent circuit using IEC 60909 method

According to [24], during the planning stage of the system as the future load-flow conditions are unknown, the aim of the voltage factor c is finding an SC current as close as possible to the real value. The voltage factor c for different voltage levels is shown in the table as per [3].

The next step is the modeling of components to find their equivalent impedance as follows:

3.2.4.1 Network Feeders

When a SC fault occurs at a feeder connection point Q , the equivalent impedance of the network is determined by

$$Z_Q = \frac{c \cdot U_{nQ}}{\sqrt{3} \cdot I''_{kQ}} \cdot \frac{1}{t_r^2} \quad (3.6)$$

Nominal voltage V_n	Voltage factor c for the calculation of	
	maximum SC currents c_{max}	minimum SC current C_{min}
Low voltage (100V to 1000V)	1.05	0.95
High voltage (>1KV to 230KV)	1.10	1.00
High Voltage (>230 KV)	1.10	1.00

Table 3.2: voltage factor c

In the above equation, the term U_{nQ} represents the nominal voltage of the system, I''_{kQ} is the maximum SC current the feeder can supply. The t_r^2 term represents the transformer turns ratio and is included only if a transformer is present and transformation to the secondary Low voltage side must be done.

If either R_Q or X_Q is known equation 3.7 is used

$$X_Q = \frac{Z_Q}{\sqrt{1 + \left(\frac{R_Q}{X_Q}\right)^2}} \quad (3.7)$$

From the Equation 3.6, it is important to know the current that the feeder can supply. However, the data is not available in physical and ASML systems. Due to this, the method used in UL 508A [15] is incorporated, and it states that the SC current available from the feeder is infinite and is only limited by the main transformer. To get the maximum current on the secondary side of the transformer, we use the following equations

$$\text{full-load current}(I_{fl}) = \frac{(KVA * 1000)}{\text{voltage} * 1.732} \quad (3.8)$$

$$\text{SC current}(I_{sc}) = \frac{I_{fl}}{\%Z} \quad (3.9)$$

where Z is the impedance of the percentage impedance of the transformer (given in the datasheet).

This available SC current is calculated using Equation 3.7 as the current available from the feeder in Equation 3.6 to calculate the feeder impedance.

3.2.4.2 Transformers

The positive sequence impedance ($Z_T = R_T + jX_T$) is the same as the negative sequence impedance and can be calculated by :

$$Z_T = \frac{u_{kr}}{100} \cdot \frac{U_{rT}^2}{S_{rT}} \quad (3.10)$$

The resistance and reactance are calculated by:

$$R_T = \frac{u_{Rr}}{100} \cdot \frac{U_{rT}^2}{S_{rT}} = \frac{P_{krT}}{3 \cdot I_{rT}^2} \quad (3.11)$$

$$X_T = \sqrt{Z_T^2 - R_T^2} \quad (3.12)$$

where,

- U_{rT} is the rated voltage of the transformer on the high-voltage or low-voltage side
- I_{rT} is the rated current of the transformer on the high-voltage or low-voltage side
- S_{rT} is the rated apparent power of the transformer
- P_{krT} is the total loss of the transformer in the windings at the rated current
- u_{kr} is the SC voltage at rated current in percent
- u_{Rr} is the rated resistive component of the SC voltage in percent

Investigation of various network transformers was done in [27] and a correction factor (K_T) is introduced to get more accurate values [24] and the impedance is given by

$$\vec{Z}_{TK} = K_T \vec{Z}_T$$

where,

$$K_T = 0.95 \cdot \frac{c_{max}}{1 + 0.6 \cdot x_T} \quad (3.13)$$

3.2.4.3 Transmission Line

The Impedance per unit length \vec{Z}_L and $Z_{(0)L}$ is taken from the manufacturer datasheet, and it is multiplied by the length of the conductor to get the impedance.

The effective resistance per unit length R'_L of overhead lines at the conductor temperature 20 °C may be calculated from the nominal cross-section q_n and the resistivity ρ according to the equation 3.14 [3]:

$$R'_L = \frac{\rho}{q_n} \quad (3.14)$$

:

$$X'_L = \omega \cdot \frac{\mu_0}{2\pi} \cdot \left(\frac{1}{4n} + \ln \frac{d}{r} \right) \quad (3.15)$$

where,

- d is the geometric mean distance between conductors.
- r is the radius of a single conductor.
- n is the number of bundled conductors, for single conductors $n = 1$

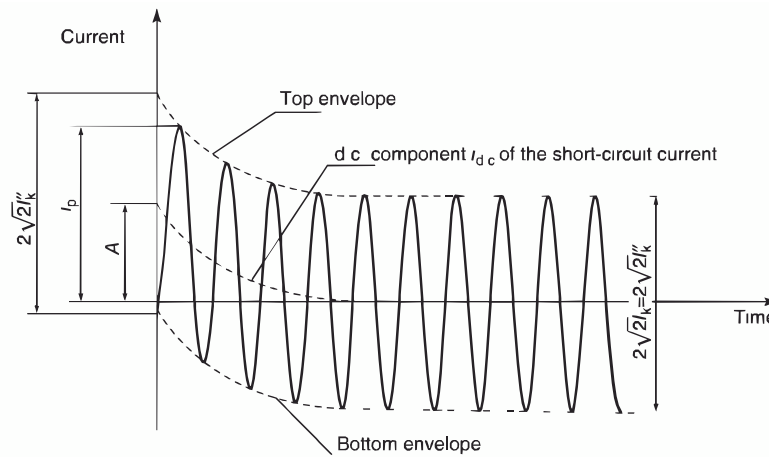


Figure 3.7: AC SC current [3]

- $\mu_0 = 4\pi \cdot 10^{-4} \text{ H/km}$

The SC far from generator¹ according to [3] is given in Figure 3.7. The SC current parameters according to this method are as follows

3.2.4.4 Initial Symmetrical SC Current I_k''

It is the RMS value of the AC component of the SC current at the instant of the SC. While using fuses or current-limiting CBs to protect substations, the initial symmetrical SC current is first calculated as if these devices were unavailable. Maximum initial SC current or peak is generated when the SC occurs at zero voltage, as explained in the previous section. The symmetrical component is calculated by using the equivalent voltage source $\frac{c \cdot U_n}{\sqrt{3}}$ at the SC location and the equivalent SC impedance $Z_k = |R_k + jX_k|$.

For a three-phase SC fault, the initial symmetrical SC current $I_{k3phase}''$ is calculated using equation 3.16

$$I_{k3phase}'' = \frac{c \cdot U_n}{\sqrt{3} \cdot Z_k} \quad (3.16)$$

For a line-to-line fault without a ground connection, the initial symmetrical SC current is calculated by

$$I_{k2}'' = \frac{\sqrt{3}}{|\vec{z}_{(+)} + \vec{z}_{(-)}|} \cdot \frac{c \cdot U_n}{\sqrt{3}} \quad (3.17)$$

If $\vec{z}_{(+)} = \vec{z}_{(-)}$,

$$I_{k2}'' = \frac{\sqrt{3}}{2} \cdot I_k''$$

¹In case of SC faults far from generator, the symmetrical component remains the same. This type of fault applies to the system considered in this thesis.

For a line-to-earth fault, the initial SC current is given by

$$I''_{k1} = \frac{3}{\left| \vec{Z}_{(+)} + \vec{Z}_{(-)} + \vec{Z}_{(0)} \right|} \cdot \frac{cU_n}{\sqrt{3}} \quad (3.18)$$

3.2.4.5 Peak SC Current I_p

It is the maximum instantaneous SC current that depends on the DC component of the SC current. The peak SC current can be calculated for all types of SCs by

$$i_p = \kappa \sqrt{2} I''_k \quad (3.19)$$

The factor κ can be calculated by the expression 3.20, leading to the highest possible instantaneous value of the SC current [24].

$$\kappa = 1.02 + 0.98e^{-\frac{3R}{X}} \quad (3.20)$$

For determination of the ratio $\frac{R}{X}$, three methods have been presented in [3] and the method using equivalent frequency is chosen as the most accurate method [24]. According to this method, an equivalent impedance $Z_c = R_c + jX_c$ of the positive-sequence system as seen from the SC location is calculated assuming a frequency $f_c = 20$ Hz [3][24]. Then, the ratio is calculated using the equation

$$\frac{R}{X} = \frac{R_c}{X_c} \cdot \frac{f_c}{f} \quad (3.21)$$

3.2.4.6 DC Component of SC Current I_{dc}

The maximum DC component i_{dc} of the SC current decays with time as the energy stored in the inductor is released and is calculated by

$$i_{dc} = \sqrt{2} \cdot I''_k \cdot e^{-2\pi \cdot f \cdot t \cdot \frac{R}{X}} \quad (3.22)$$

Where,

- I''_k is the initial symmetrical SC current
- f is the nominal frequency
- t is the time

The ratio $\frac{R}{X}$ or $\frac{X}{R}$ can be determined using the methods in the previously.

3.2.5 Verification

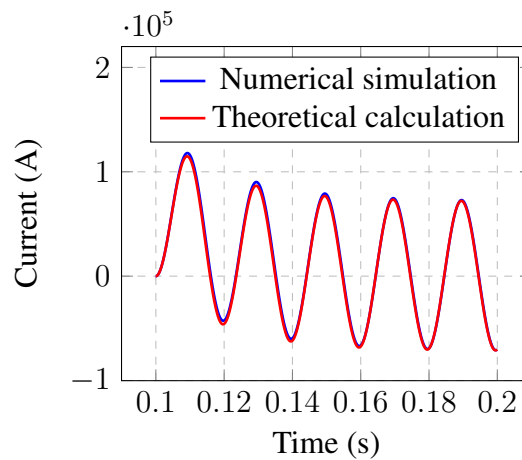


Figure 3.8: Verification of calculation and simulation

Peak SC current	Value (kA)
Simulation	117.2
Calculation	115.8

Table 3.3: Three phase fault results

After doing several simulations, on average, there is a difference of 1.7% when comparing peak SC current simulation with calculation results as seen in Figure 3.8. This is because as the $\frac{X}{R}$ ratio of the transformer is not available from the transformer datasheet, the value of the ratio is approximated to 10 [3]. However, sensitivity analysis is done by varying the $\frac{X}{R}$ to find the ratio so that the simulation and calculation results are the same. From the analysis as shown in Figure 3.9, the value of $\frac{X}{R}$ can be taken as 8.83 to make the results match.

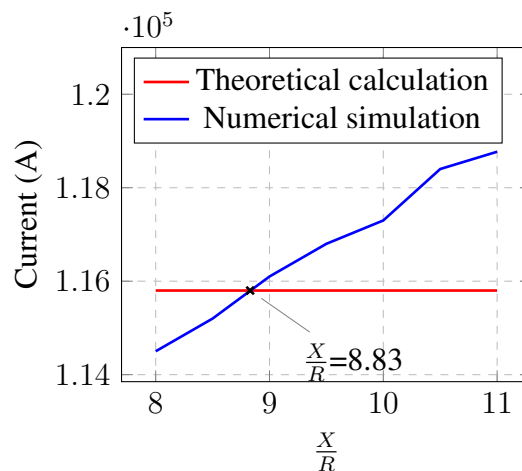


Figure 3.9: Sensitivity analysis to find $\frac{X}{R}$

3.3 Determination of SCCR

SCCR is the maximum current the system can withstand for a specific time until the fault is cleared. To determine the overall SCCR of the system, IEC standards do not specify a method. However, it is mentioned that UL508A can be followed for SCCR calculations. This determination of overall SCCR can be done using the following three steps according to [15]:

1. **Step 1: Establishing the SCCR of individual power circuit components.**

This step involves the identification of the SCCR of all the components present in the system. Usually, the SCCR values are displayed on the datasheet of the components. If the SCCR values are not available, the table given in [15] can be used.

2. **Step 2: Modifying the available SC current within a portion of a circuit in the panel due to the presence of current limiting components.**

Usually, the overall SCCR of the system is the lowest SCCR or interruption rating of components and protective elements considered. However, this SCCR can be increased by using current limiting elements. This is because, now the component sees only the limited current and if this current is lower than its SCCR, it can withstand the high current.

3. **Step 3: Determining the overall panel SCCR.**

This step involves determining the overall SCCR of the system, which is the lowest SCCR, and the interruption rating of all components and protective elements. Step 2 should also be considered in this step.

3.4 Conclusion

In this chapter, a standardized method for determining the AC SC current is presented and the calculation and simulation methods are compared to identify the cause for the difference. A method for the determination of the overall SCCR of the system is also presented. It was explained that the overall SCCR of the system can be increased by limiting the current. This way of increasing the SCCR by improving the protection and limiting the current is explored in the next chapter. However, according to UL 508A [15], a series connection of current limiting CBs is not physically allowed. However, they have also mentioned that the results of the physical test conducted in a laboratory certified by either IEC or Semi S22 can be accepted. Through this chapter, research questions 2 and 4 are answered. The methods explained in this chapter are implemented in the Matlab tool for system assessment.

AC SC PROTECTION

IN the previous chapter, standardized methods to determine the SC current along with the overall SCCR of the system are explained. It was also mentioned that the overall SCCR can be improved by improving the protection of the system so that the SC current can be limited. Therefore, this chapter deals with improving AC system protection focusing on the study of standard and current limiting CBs.

4.1 AC Mechanical CBs

CBs are devices that can open the circuit during abnormal conditions such as a short circuit or overloads, leading to an increase in circuit current and isolating the faulty part of the system. The CB uses a tripping mechanism that opens the contacts when a high current due to any abnormal condition flows through them.

The main aim of the tripping mechanism is to move the contacts so that the circuit is opened and the current is interrupted. However, this interruption process is not simple. When the contact separates, an arc is formed between the contacts. This is because, at the instant of contact separation, the inductance of the system leads to excess electrons near the edge of the contacts leading to high electric fields and the insulating medium between the contacts is subjected to extremely high electric stress leading to breakdown [23]. The breakdown of the insulating medium between the contacts results in the formation of an arc between the contacts and current continues to flow through the arc until it is fully extinguished [7]. To quench the arc, the contacts are placed in a closed chamber containing a fluid-insulating medium that helps recombine with the ions that provide the conducting medium, making them neutral [23]. The CBs can be classified based on the number of phases they need to protect as single, two, three and four poles.

The AC mechanical CBs mostly use thermal-magnetic principles and have two tripping mechanisms for overload and short circuit conditions.

- **Overload protection :** During an overload condition, the thermal protection principle is used to move the contacts. A bimetallic strip is used, which is made up of two metals with different coefficients of thermal expansion, so that when they

experience a high current due to overload they expand differently and bend to move the switch linkage, hence the contacts and break the circuit.

- **Short circuit protection** : During a short circuit, electromagnetic principles are used to trip the circuit. This is done by a copper coil which acts as an electromagnet. When high current flows through the electromagnet, it is magnetized and magnetic flux lines start flowing and it exerts an electromagnetic force which depends on the amount of current. When the current reaches a very high value due to a short circuit, the electromagnet becomes strong enough to move the switch linkage, hence the contacts and breaking of the circuit.

4.1.1 Arc Voltage

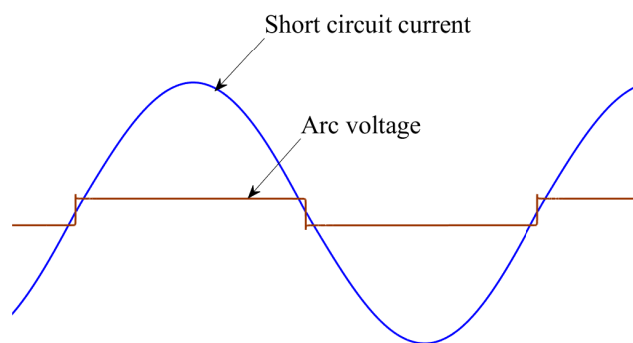


Figure 4.1: Arc voltage

When the mechanical contacts start to separate, the short circuit current flows through the arc that is formed. The voltage drop across the arc is given in Figure 4.1. It can be observed that the arc voltage is lower than the rated voltage as there is current flow and the arc is purely resistive as the voltage is in phase with the current [23].

The arc is interrupted at zero crossing of current and at the instant when the arc is interrupted, there is a voltage difference between the terminals of the breaker, which is known as Transient Recovery voltage (TRV) and is explained in the next section.

4.1.2 TRV

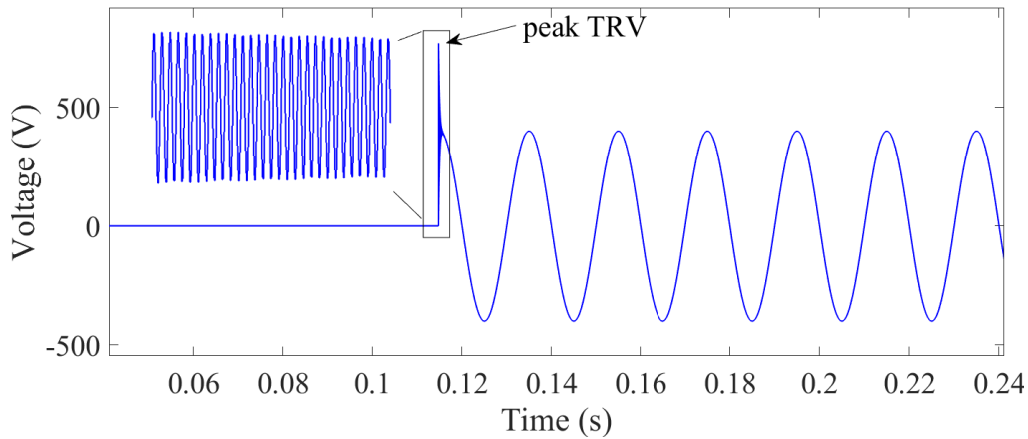


Figure 4.2: TRV

When the arc is extinguished the voltage of the CB is expected to return to the system voltage, but the voltage undergoes a transient and reaches a value with the maximum possible peak of two times the system voltage. However, the peak is lower due to the system losses. The appearance of peak TRV oscillations is due to the stray capacitance due to the transformer windings and the value can be as low as 10pF [23].

The TRV waveform shown in Figure 4.2 has two stages, the transient recovery stage where high-frequency oscillations are observed, and the recovery voltage where the system voltage is reached. The frequency and magnitude of the oscillations observed during the TRV are due to the L and C in the system. The frequency of oscillation is given by

$$f_{trv} = \frac{1}{2\pi\sqrt{LC}} \quad (4.1)$$

4.1.2.1 Reason for TRV

The reason for the cause of TRV is that when the breaker opens and the arc conducts the current does not flow through the capacitor. Right after the arc is extinguished current flows in the capacitor through the inductor due to which the voltage across the breaker is equal to the system voltage plus the voltage due to LC oscillations. The TRV depends on when the fault is interrupted, the type of fault, and L and C in the system. The TRV is maximum when the system is lossless. However, it is reduced due to copper and iron losses in the system.

4.1.2.2 Effect of TRV

If the peak TRV increases beyond the withstand capacity of the CB, there is a problem with arc restrike due to dielectric breakdown. This leads to the formation of an arc again and even can cause damage.

4.1.2.3 Factors Affecting TRV

To understand the factors affecting TRV, an equivalent circuit of the power system with the stray capacitance is shown in Figure 4.3

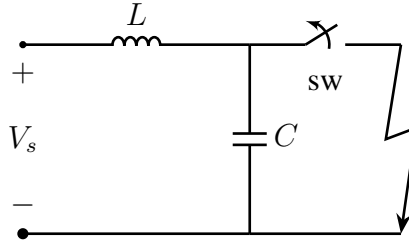


Figure 4.3: Equivalent single phase circuit

After extinguishing the fault, KVL to loop 1 gives

$$V_c = V_s + V_L \quad (4.2)$$

Applying KVL to loop 2 leads to

$$V_c = V_{sw} \quad (4.3)$$

Equations 4.2 and 4.3 can be combined and given as

$$V_{sw} = V_s + V_L \quad (4.4)$$

where

$$V_{sw} = V_c = \frac{1}{C} \int i dt$$

The factors affecting TRV can be defined by considering Equation 4.4 as follows:

- **System Voltage:** As the system voltage increases, the peak TRV increases. This is because, according to Equation 4.4, the TRV voltage is directly proportional to the system voltage and a linear increase in peak TRV voltage is expected with an increase in system voltage. This is confirmed by the simulation results as shown in Figure 4.4.

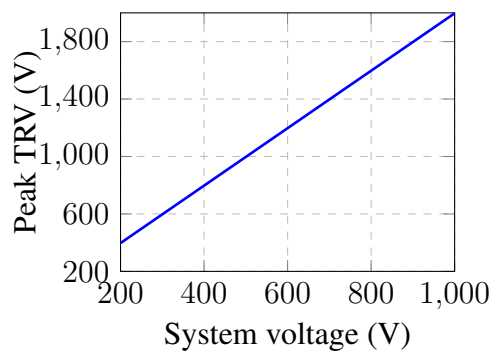


Figure 4.4: Variation of peak TRV with system voltage

- **System Inductance:** According to Equation 4.4, as the system inductance increases, the voltage across the inductor V_L increases, leading to an increase in the peak TRV.
- **Stray Capacitance:** According to Equation 4.4, the capacitance is inversely proportional to the voltage across the switch.

4.2 Current Limiting AC CBs

Current limiting CBs limit the short circuit current passing through their contacts and the limiting capability depends on their limiting mechanism and tripping time. They interrupt the current within the first half cycle of the current before the peak current is reached. The reduction in current is also accompanied by a reduction in the current flow time compared to non-current limiting CBs. The current limiting effect is shown in Figure 4.5.

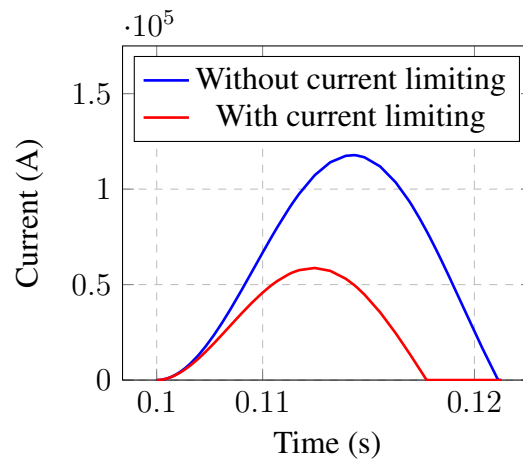


Figure 4.5: AC short circuit current limitation

4.2.1 Need for Limitation

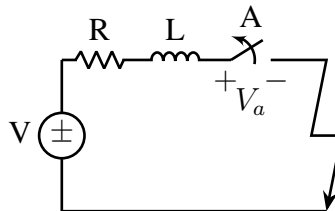


Figure 4.6: Single phase representation of a system

Consider one phase of a 3-phase AC system with Voltage V and delivering a load through a CB as shown in Figure 4.6. R is the equivalent resistance of the system and L is the equivalent inductance. Using KVL the voltage equation can be written as

$$V = iR + L \frac{di}{dt}$$

Since the system inductance is high compared to the resistance, the equation can be written as

$$\frac{di}{dt} = \frac{V}{L}$$

From this equation, it can be seen that the rate of increase in current is dependent on the voltage and inductance. To avoid such high currents developing we need a current-limiting CB that can limit the current by providing a voltage drop that opposes the current increase.

4.2.2 Conditions for Current Limitation

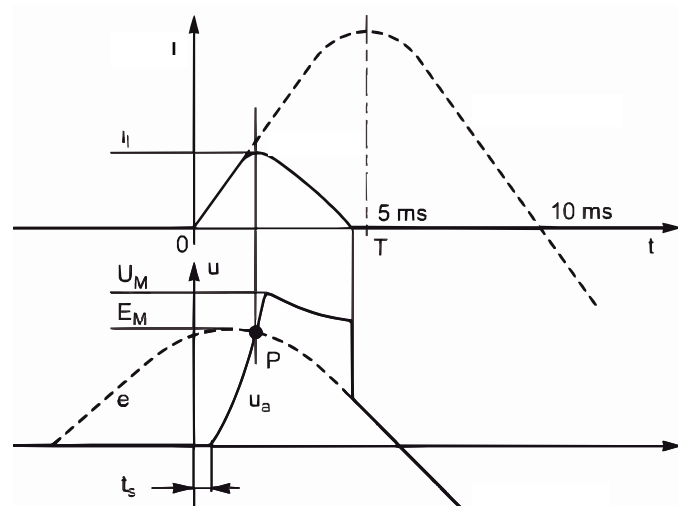


Figure 4.7: Limited short circuit current [28]

Consider the system in Figure 4.6, now the breaker is replaced by a current-limiting CB that provides a reverse voltage of V_a when current is flowing across it. Now KVL equation can be written as

$$V = \frac{di}{dt} + V_a$$

From the equation, the peak current is reached when $V = V_a$. Figure 4.7 shows the system voltage and prospective short circuit current. P is the intersection point of the system voltage curve and the developed voltage curve. For the current to be limited, the P should be before the peak prospective current [28], so it can be concluded that the tripping time should be very low and the separation of contacts should also be fast so that the system voltage V is reached before the peak. Adding to this, the developed voltage should be slightly more than the system voltage so that $\frac{di}{dt}$ becomes negative and the current starts to decrease faster.

To obtain the voltage V_a the resistance of the arc produced between the contacts can be increased by using appropriate cooling methods. The use of sufficient cooling methods can ensure the voltage developed reaches the required value allowing current limitation.

4.2.3 Cascading

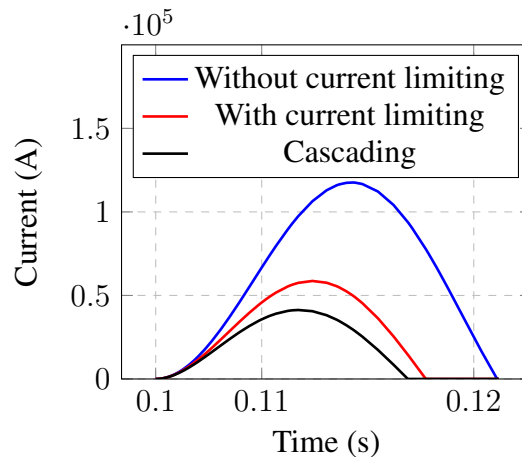


Figure 4.8: Effect of cascading

The Effect of cascading is possible when both upstream and downstream CBs are currently limiting and are connected in series. According to this concept, the upstream main CB which has a higher current rating than the downstream CB trips first in case of a short circuit, limits the short circuit current and protects the components connected downstream by allowing limited current to flow through their contacts. Due to this, the downstream CB sees the limited current and if it is also current limiting, limits the current further. This phenomenon can be explained using Figure 4.8 where an increase in the number of series connected current limiting CBs, decreases the peak.

The Advantages of cascading are as follows:

- Cascading allows the use of CBs in places where the prospective short circuit current level exceeds the standalone breaking capacity of the downstream device
- This allows cheaper CBs with lower ratings to be used downstream.

However, due to their phenomenon, the upstream CB trips first in all cases, which is opposite to the concept of selectivity.

4.3 Comparison

The overview of the comparison between the CBs is shown in Figure 4.9. The following parameters are considered for comparing the standard with current limiting CBs:

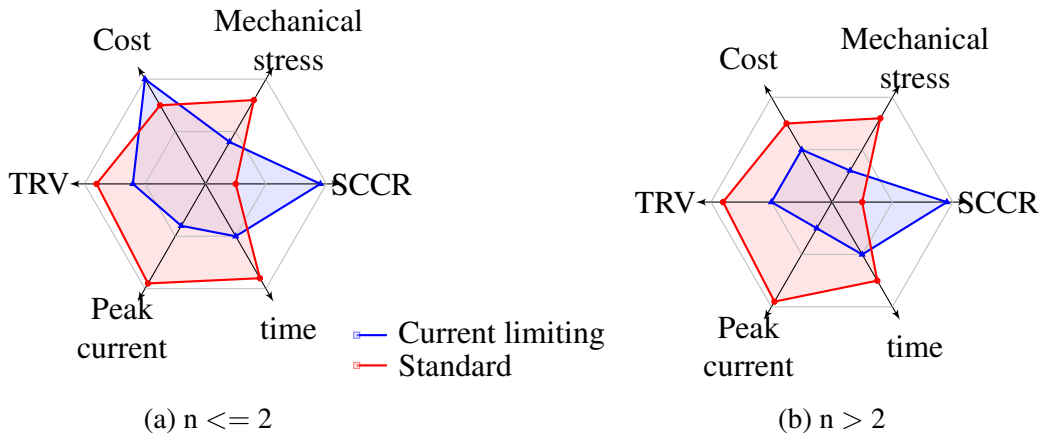


Figure 4.9: Comparison overview of parameters, where n is the number of CBs in series

4.3.1 SCCR

The SCCR of the system can be improved by using a current-limiting CB. This effect was explained in the previous chapter.

4.3.2 Mechanical Stress

Electromagnetic forces are induced in conductors when current flows through them. When these forces interact with a parallel conductor, there will be a force between the conductors [29]. The direction of the force depends on the direction of the current flowing through them. If the current in the two conductors has the same direction, forces are attractive and the forces are repulsive when the current flows in opposite directions. The force between the conductors is uniformly distributed and is given by

$$F = \frac{\mu_0}{2\pi} i_1 i_2 \frac{l}{a} \quad (4.5)$$

where,

- i_1 and i_2 are instantaneous values of currents in the conductors
- l is the center line distance between supports
- a is the distance between conductors

From Equation 4.5, it can be seen that the force depends on the currents flowing through the conductors. When a current-limiting CB is used, as the conductor current is limited, the force between the conductors is reduced.

4.3.3 Effect on TRV

Adding a current limiting CB is equivalent to adding a series resistance in the system. This added resistance leads to a voltage drop [30] and the Equation 4.4 becomes

$$V_{sw} = V_s + V_L - V_R \quad (4.6)$$

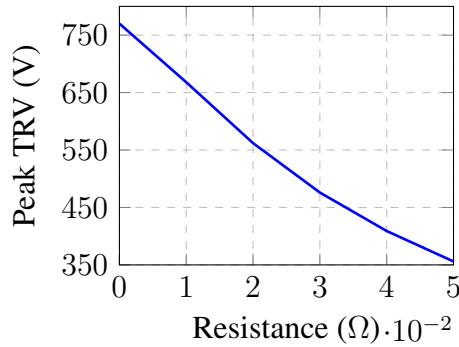


Figure 4.10: Variation of peak TRV with breaker resistance

where,

$$V_R = iR \quad (4.7)$$

The TRV is expected to decrease linearly with resistance as per the equation. This is validated using the simulation in Figure 4.10.

4.3.4 Peak Current and Interruption Time

Use of current limiting CBs limits the peak current based on the peak let-through curve from the datasheet of the CB and also the SC interruption time as seen in Figure 4.5. The peak let-through curve of an Eaton NZMN series current limiting CB is shown in Appendix A.

4.3.5 Cost

To compare the costs, the CBs considered are shown in Table 4.1.

Type	Model	Peak withstand current (kA)
Standard	Eaton 120667MRB6	50 kA
Current limiting	Eaton NZMN series	50 kA, 25 kA

Table 4.1: Cost analysis

The capital cost of a CB depends on its rating and peak withstand capacity. cost of one current limiting CB is higher than the standard CB. As the number of current limiting CBs connected in series increases lower rated CB can be used thus reducing the cost. The cost reduction can be seen in Figure 4.9.

4.4 Conclusion

In this chapter, different CBs such as the standard and current limiting are explained. Their comparison is presented showing the advantages of using the current limiting CB, including the increase in the system SCCR. This chapter answers the research question 4. The next chapter focuses on determining the available short circuit current when a SC fault occurs on the DC side.

DC SC STUDY

THE difference between the SC currents in an AC and a DC system is due to the difference in zero crossing of current leading to different transients. Adding to this, the DC fault current rises faster than an AC fault current [31]. Therefore, it is important to analyze the fault current so that appropriate protection mechanisms can be used.

Authors in [32][33] and [34] analyzed DC side faults based on modeling and simulation without any numerical calculation methods. Whereas, authors in [4] give a numerical calculation method to determine the DC SC current on the DC side of the Voltage source converter (VSC). However, most literature focuses only on DC faults in a high voltage (HVDC) system. The standard IEC 61660 [35] gives theoretical equations to calculate the DC SC current in a low-voltage DC system. However, this standard applies to power plants and substations and not completely to industrial machinery. The idea from the previously mentioned literature is used as the base to derive a numerical equation to calculate the DC SC current in a low-voltage system. The results of the numerical analysis are validated with the simulation output results.

The possible DC SC faults are [36]

- **Pole-to-pole fault:**
This type of fault has a SC between the two DC lines. This fault can be temporary or permanent and is the most severe fault with a high peak SC current.
- **Pole-to-ground fault:**
This type of fault has a SC between one DC line and the ground.

In the scope of this thesis, only pole-pole fault is considered. The DC fault currents due to the above-mentioned faults can be due to a DC voltage source such as a battery or an AC voltage source using AC-DC rectifiers. The calculations of DC fault current arising from the two sources are explored in this chapter.

5.1 Fault Current from DC Voltage Source

DC voltage source can contribute to the DC fault without any restrictions directly or through a DC-DC converter. Figure 5.1 shows a boost converter with a DC pole-to-pole

fault.

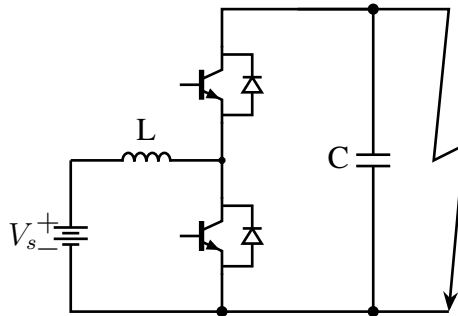


Figure 5.1: Boost converter

The DC fault current due to a DC voltage source is shown in Figure 5.2. The current increases rapidly and reaches a high value within a few milliseconds [31]. This damages the components on the path. Due to the presence of an inductor, the transient state involves current increasing with a rate equal to the inductor time constant τ equal to $\frac{L}{R}$. A steady state is reached where a constant current flows as seen in Figure 5.2. This current is given by

$$i(t) = \frac{V_s}{t} (1 - e^{-\frac{t}{\tau}}) \quad (5.1)$$

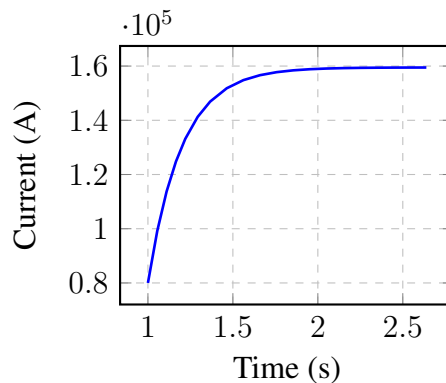


Figure 5.2: DC fault current from a DC voltage source

5.2 Fault Current from AC Voltage Source

AC source must be converted to DC to analyze the faults. Voltage source converters (VSC) are widely employed in low-voltage systems for converting AC to DC. They are based on transistors, which allow independent control of active and reactive power and can control the output voltage freely. The advantages of using VSCs are listed in [37]. The major drawbacks of VSCs are fault ride-through capability during DC SC faults due to low DC side impedance and the absence of zero crossing of fault current [4]. The next section explains the modeling of a two-level VSC.

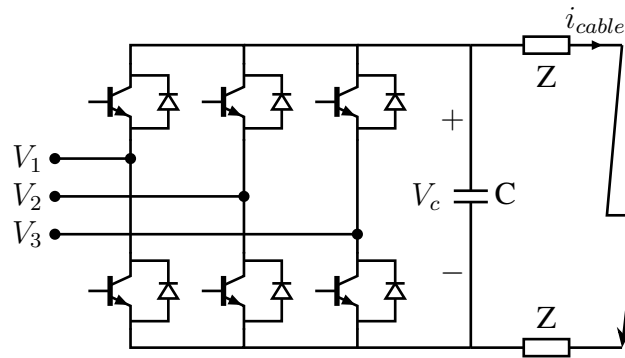


Figure 5.3: Two level VSC

5.2.1 Two-level VSC

The three-phase two-level voltage source converter is shown in the Figure 5.3 [38] [39]. It has six semiconductor switches, two in each arm. Capacitor C is used to make the DC output voltage smooth. An inductor and a resistor are used that will function as an AC filter [40]. Pulse width modulation (PWM) modulation technique can be used to design the pulses to switch the semiconductor switches. PWM involves comparing a repeating waveform with a sinusoidal waveform. This way, we can get the output voltage that we need. The controller for the converter is designed by controlling the current controlled Real/Reactive power and DC voltage as shown in Figure 5.4. The control is done in the dq reference frame. This is because it is always easier to control a DC component, and the AC side sinusoidal varying current quantities can be converted into a rotating frame to make them equivalent to DC quantities. Also, this type of control is called current control because the power P_s and Q_s are controlled by the current i_d and i_q , and the AC side voltage cannot be varied. The voltage and current signals are transformed into the dq frame and then processed to provide the control signals in the dq frame. Finally, the control signals in the dq frame are converted to the abc frame and given to the converter.

To convert signals from the abc frame to the dq reference frame we use park transformation whose equation is shown in Appendix B.

5.2.1.1 Phase Locked Loop (PLL) Controller

For converting components from abc to dq reference frame, the phase angle value is needed, which is generated using the PLL controller. This means the input voltage angle must be synchronized with one of the dq axes. To align the input voltage to the d axis, we set $v_q = 0$. The implementation of the PLL controller is shown in Figure 5.5.

5.2.1.2 Inner Controller

Using KVL across the phase reactor leads to the equation

$$V_f = Ri_c + L_p \frac{di_c}{dt} + v_c \quad (5.2)$$

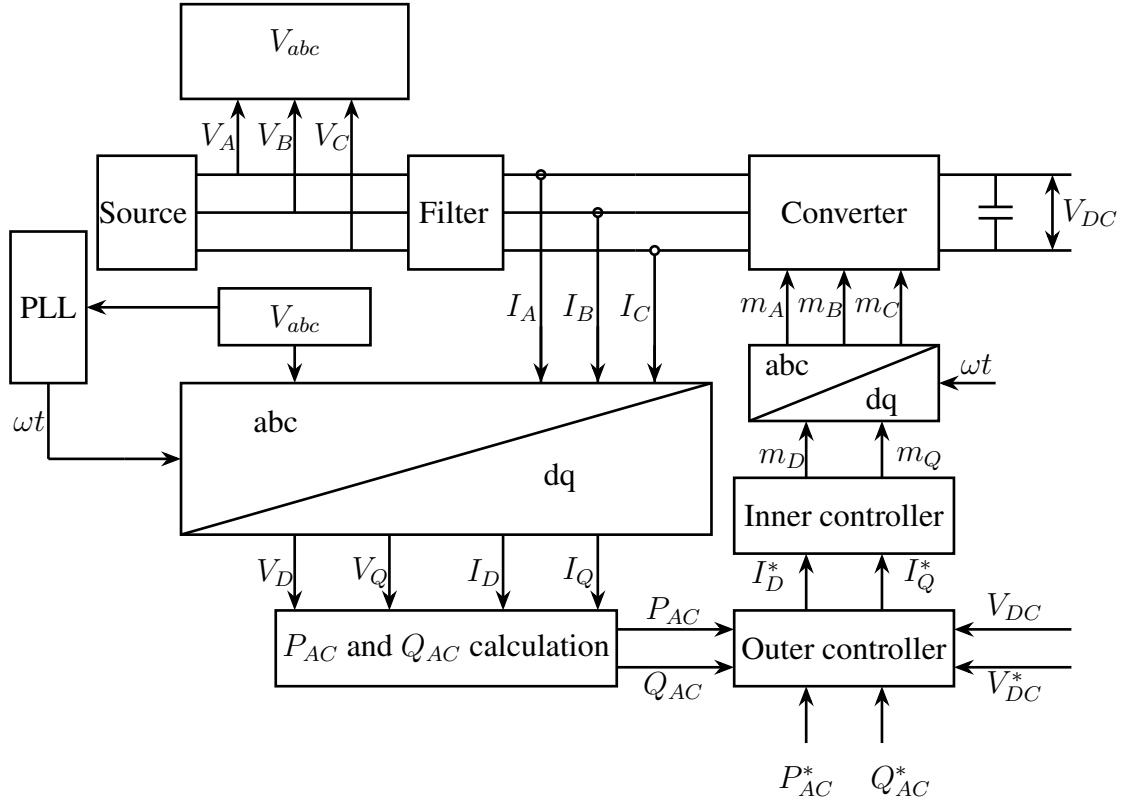


Figure 5.4: Controller in dq frame

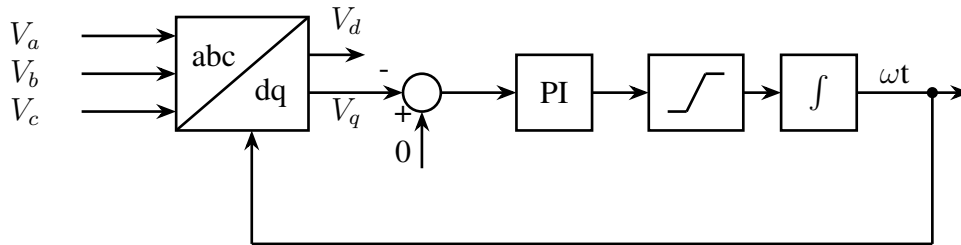


Figure 5.5: PLL controller

Where, V_f is the voltage across the filter, v_c is the converter voltage.

In case of dq transformation Equation 5.2 can be written as

$$V_{fd} = Ri_{cd} + L_p \frac{di_{cd}}{dt} + v_c - \omega L_p i_{cq} \quad (5.3)$$

$$V_{fq} = Ri_{cq} + L_p \frac{di_{cq}}{dt} + v_c + \omega L_p i_{cd} \quad (5.4)$$

In Equations 5.3 and 5.4, the dynamics of i_d and i_q are coupled due to presence of $L\omega$. To decouple this, the equations can be written in terms of modulation indices m_d and m_q as per [41]

$$m_d = \frac{2}{V_{dc}} (u_d - L\omega i_q + u_{cd}) \quad (5.5)$$

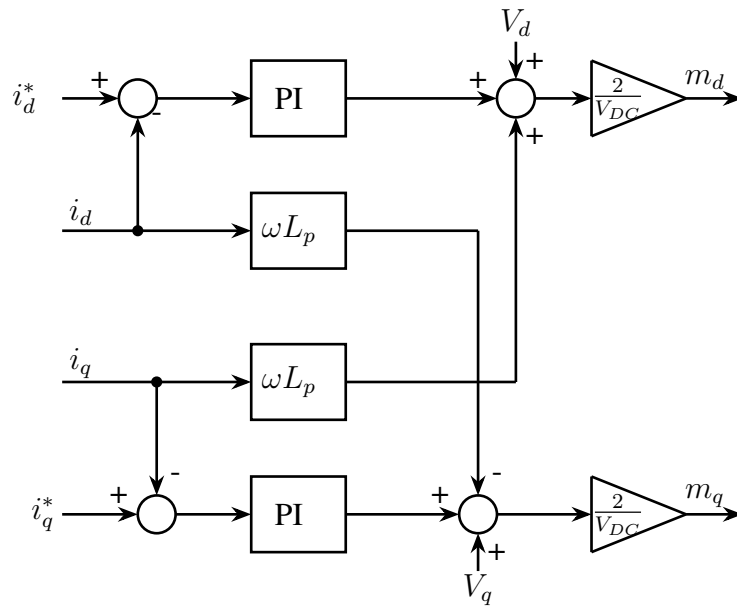


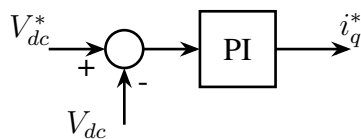
Figure 5.6: Inner controller

$$m_q = \frac{2}{V_{dc}}(u_d + L\omega i_d + u_{cq}) \quad (5.6)$$

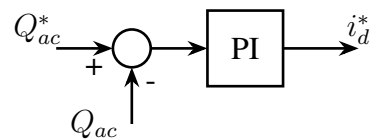
The Equations 5.5 and 5.6 are implemented as control blocks in Matlab as shown in Figure 5.6.

5.2.1.3 Outer Controllers

The DC voltage controller as shown in Figure 5.7a that gives the reference q axis current and reactive power control as shown in Figure 5.7b is part of the outer controllers. These controllers try to keep the DC voltage and reactive power to the required value by correcting the error. PI controllers are used for this purpose.



(a) Voltage controller



(b) Reactive power controller

Figure 5.7: Outer controllers

5.2.2 Current Calculation

The two-level VSC converter with a DC line-to-line fault is shown in Figure 5.3. During a DC fault, the IGBTs of the VSCs are blocked for self-protection, and the reverse diodes are exposed to overcurrent [4]. According to the theoretical analysis of DC side faults in a VSC done in [4], the transient response of the system can split into three stages [42]:

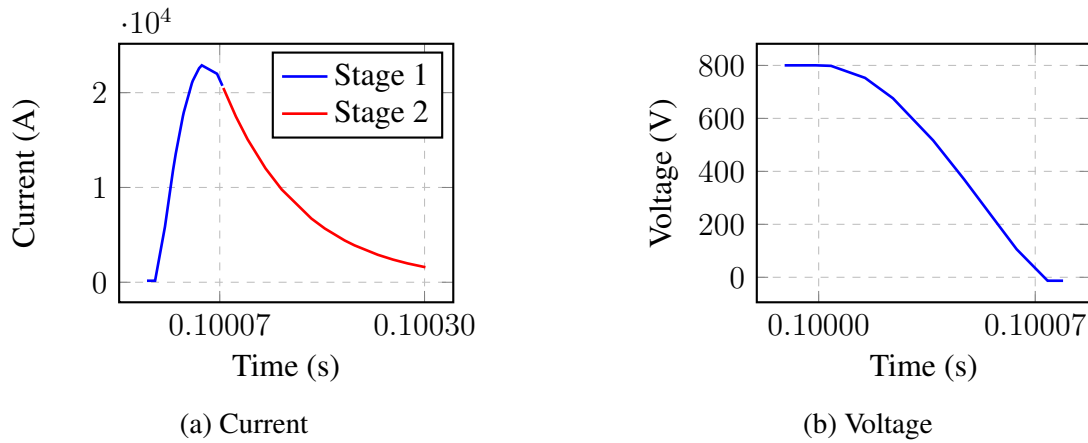


Figure 5.8: DC fault analysis

5.2.2.1 Stage 1: Capacitor Discharge

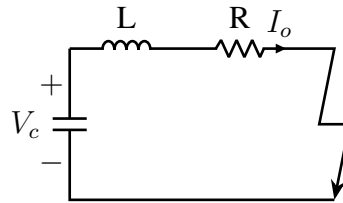


Figure 5.9: Capacitor discharge stage

This is the first stage after the occurrence of a DC SC fault, where the DC side capacitor starts discharging through the fault line, and the voltage across it begins to fall to zero. As a result of the discharge, the cable current starts rising rapidly, as seen in Figure 6.3a. It is noted that there is no current contribution from the AC side during this stage as the DC side voltage is more than the AC side. The equivalent circuit during this stage can be represented by Figure 5.9, and it consists of R , L , and C connected in series leading to oscillations.

Assuming the fault occurs at $t_0 = 0$, KVL leads to the equation

$$V_R + V_L + V_C = 0 \quad (5.7)$$

The current i through the circuit is given by

$$i = i_C = C \frac{dV_C}{dt} \quad (5.8)$$

$$V_R = Ri_C = RC \frac{dV_C}{dt} \quad (5.9)$$

$$V_L = L \frac{di}{dt} = LC \frac{d^2V_C}{dt^2} \quad (5.10)$$

Combining all the valve equations we get

$$\frac{d^2V_C}{dt^2} + \frac{R}{L} \frac{dV_C}{dt} + \frac{1}{LC} V_C = 0 \quad (5.11)$$

Now we define two factors

1. Natural frequency $\omega_0 = \frac{1}{\sqrt{LC}}$
2. Damping factor $\alpha = \frac{R}{2L}$

$$\frac{d^2V_C}{dt^2} + 2\alpha \frac{dV_C}{dt} + \omega_0^2 V_C = 0 \quad (5.12)$$

The solution for the above equation is

$$V_C = -\alpha \pm \omega_d \quad (5.13)$$

Where ω_d is the damped frequency given by

$$\omega_d = \sqrt{\alpha^2 - \omega_0^2}$$

Now assuming that the system is under-damped such that $\alpha < \omega_0$, we get the solution as

$$V_c(t) = e^{-\alpha t} (A_1 \cos \omega t + A_2 \sin \omega t) \quad (5.14)$$

We can use the Equation 5.8 to get the current as

$$I_o(t) = C e^{-\alpha t} ((A_2 \omega - A_1 \alpha) \cos \omega t - (A_1 \omega + A_2 \alpha) \sin \omega t) \quad (5.15)$$

To find the values of A_1 and A_2 , we can consider the initial conditions and we obtain the following:

- $A_1 = -V_0$
- $A_2 = \frac{I_0 + \alpha V_0 C}{C \omega}$

5.2.2.2 Stage 2: Diode Freewheel

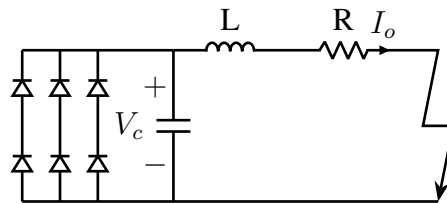


Figure 5.10: Diode freewheel Stage

This stage starts when the DC voltage becomes zero and the current commutates to the VSC freewheeling diodes [43]. The equivalent circuit is shown in Figure 5.10. Considering the initial current value as I_0' , the expression for $I_0(t)$ is given by

$$I_0(t) = I'_0 e^{-\left(\frac{R}{L}\right)t} \quad (5.16)$$

The current through each pair of freewheeling diodes is

$$I_{diode} = I_0/3 \quad (5.17)$$

This is the most challenging phase for the freewheel diodes because high current flows through that can damage them.

5.2.2.3 Stage 3: Grid Feeding

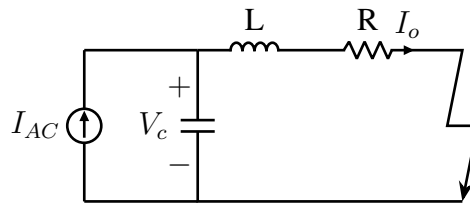


Figure 5.11: Grid feeding stage

During this stage, only the body diodes of the VSC conduct, and the converter acts as an uncontrolled rectifier with a forced response due to the grid side. The equivalent circuit is shown in Figure 5.11. The current value during this stage is the RMS symmetrical AC SC current.

5.2.3 Verification

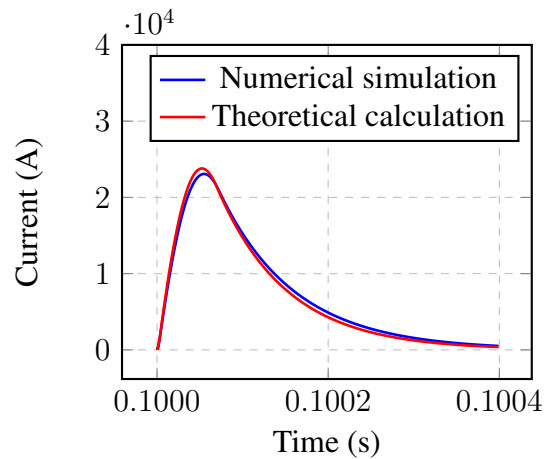


Figure 5.12: Verification of calculation and simulation

Peak SC current	Value (kA)
Numerical simulation	23.990
Theoretical calculation	24.480

Table 5.1: DC fault results

The variation of DC SC fault current obtained from simulation and numerical calculation is shown in Figure 5.12. Several iterations were done, and the variation is close to 2%. This variation is within the accepted range and can be due to the resistance of the free-wheeling diodes and other elements not considered in the calculation, making the value slightly higher.

5.3 Conclusion

This chapter presents a standardized method for determining the DC SC current and compares the calculation and simulation methods to identify the differences. Through this chapter, research question 5 is answered. The methods explained in this chapter are implemented in the Matlab tool for system assessment. The next chapter deals with ways to improve the protection of the DC system that can lead to an increase in the overall SCCR of the system.

DC SC PROTECTION

DC fault protection is important for the reliable operation of the DC power systems and comprises the detection, location, interruption, and isolation of SC faults [31]. Fault interruption is arguably the most important and challenging aspect of DC fault protection. Because of the absence of natural zero current crossings and the low reactance nature of DC grids, it is much more difficult to develop cost-effective and reliable fault interruption solutions for DC systems than traditional AC systems [31].

This chapter focuses on the interruption part of DC SC protection. Figure 6.1 shows the different technologies that are considered for DC SC fault interruption in this thesis. These technologies are compared and determined whether they can be used in the DC system to limit the current and increase the system SCCR.

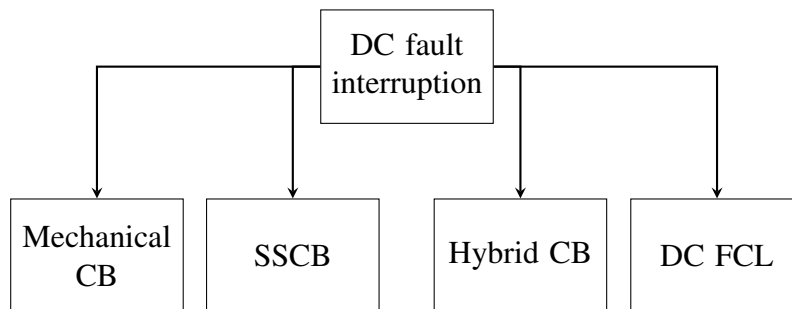


Figure 6.1: DC fault interruption

The main aim of the interruption mechanism is to interrupt the faulty part of the system. The main difference between AC and DC systems is that there is no zero current crossing in a DC system. A high-resistance arc extinguishing method can be employed since the DC system has no zero current crossing. This method increases the arc resistance by increasing the arc length using arc runners and arc chutes. When the current is sufficiently low, the fluid in the medium is used to distinguish the arc by removing the ions in the medium. When the current is interrupted, the stored magnetic energy in elements such as inductors gets converted to electrostatic energy, increasing the voltage across the CB. If the voltage exceeds the CB withstand capacity, the arc will strike again [7].

To solve the problem of over-voltage across the CB, it is important to obtain zero current crossing in a DC system. This can be done by introducing a capacitor in the fault path to convert the unipolar DC to an AC and obtain zero crossing. This AC is due to the interaction of the capacitor inserted and the stray inductance in the circuit, which leads to LC oscillations.

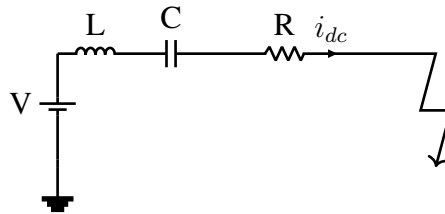


Figure 6.2: LC path

The circuit after the introduction of a capacitor C is shown in Figure 6.2. The voltage and current due to the oscillations are shown in Figure 6.3. This principle is used in the DC mechanical CBs to create an artificial zero crossing of current to interrupt.

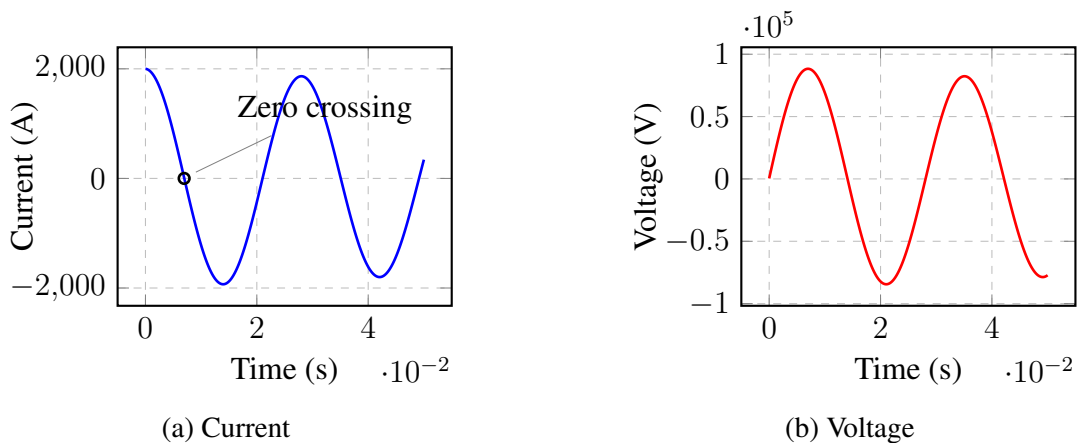


Figure 6.3: LC oscillation response

6.1 DC Mechanical CB

In a DC mechanical CB, an LC circuit along with an energy absorption path is provided in parallel to the CB contacts. The circuit is shown in the Figure 6.4 and the working principle is explained in [9][44] as follows:

1. During normal operation, the switch is closed and current flows through the switch as it offers low on-state resistance.
2. As the contact starts to open due to SC faults, an arc is formed and the arc voltage increases, which is the voltage across the LC path.

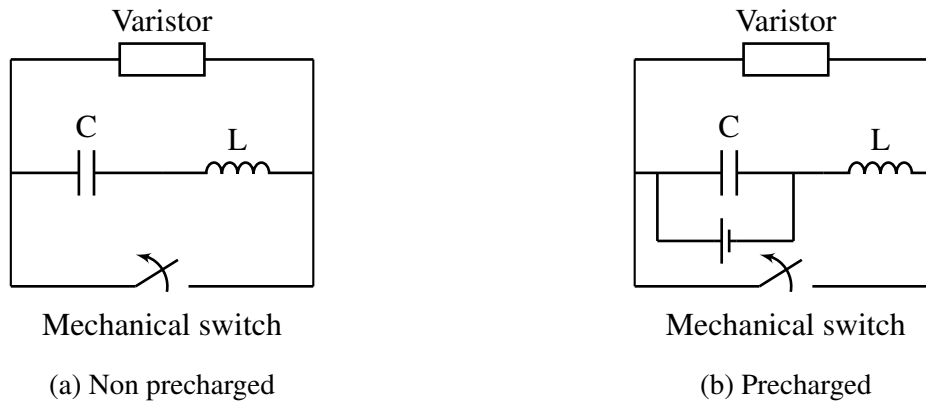


Figure 6.4: DC mechanical CB

3. As the contact starts to open, the voltage across the LC path causes oscillation with natural frequency $\omega = \frac{1}{\sqrt{LC}}$.
4. A zero crossing of current occurs due to this oscillation and the arc is interrupted then.
5. The current quickly charges the C until the threshold voltage level of the energy-absorbing elements. These elements can consist of a switch or a non-linear varistor. The voltage is limited by these elements, current only flows through the energy absorbing path and the current ceases.

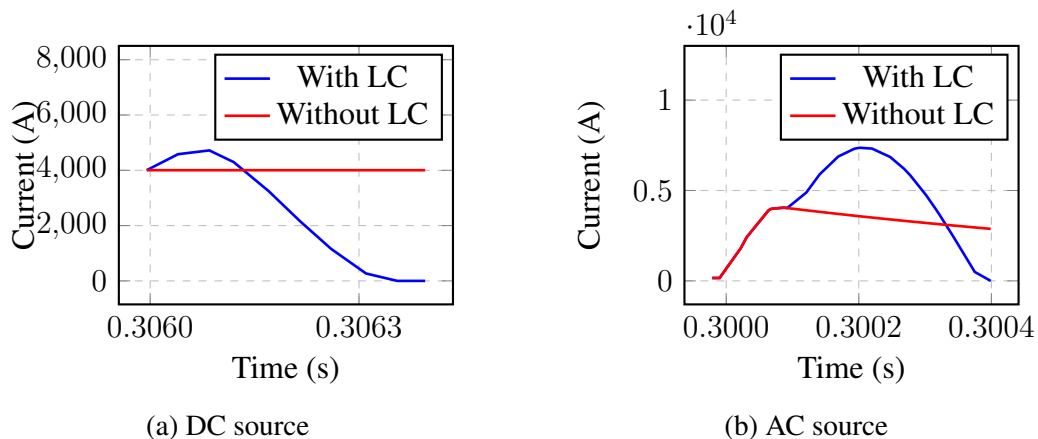


Figure 6.5: Comparison of current in DC mechanical CBs with and without SSCB.

The main problem with the DC mechanical CB is the tripping time which takes around 10 ms to 60 ms [45]. As the DC fault current rises quickly, there is a need for faster action. To reduce the current rise and the peak current till the time the CB trips, there is a need for FCL along with the DC CBs [13].

Latest technologies including SSCB which use semiconductor switches can be used that can significantly reduce the fault interruption time and the peak current. This SSCB technology is explained in the next section.

6.2 SSCB

SSCB uses semiconductor devices to switch and break the circuit in case of faults [46]. Using fast switching devices, without the need for mechanical contacts eliminates the formation of arc and reduces the switching time [47]. Because of fast switching, these CBs can limit the peak let-through energy and current [10].

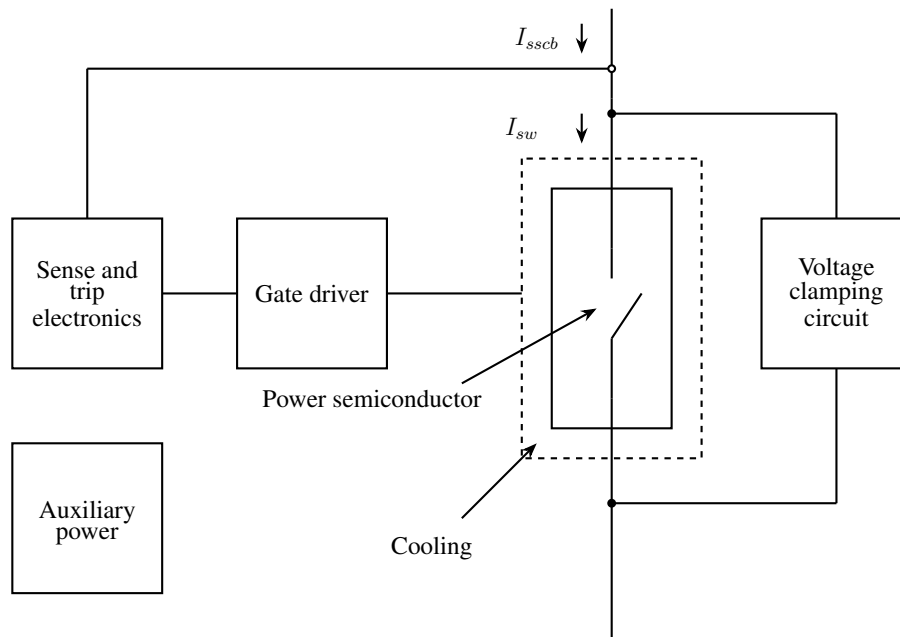


Figure 6.6: Components of SSCB [10]

The components of an SSCB are shown in Figure 6.6. It consists of a power semiconductor for switching, a voltage clamping circuit for absorbing energy, a gate driver to switch the semiconductor, and sense and trip electronics to give a tripping signal to the gate driver.

Figure 6.7 shows the current waveform from a DC and AC source respectively with an SSCB. Different types of components that can be used along with their comparison are presented in the next sections.

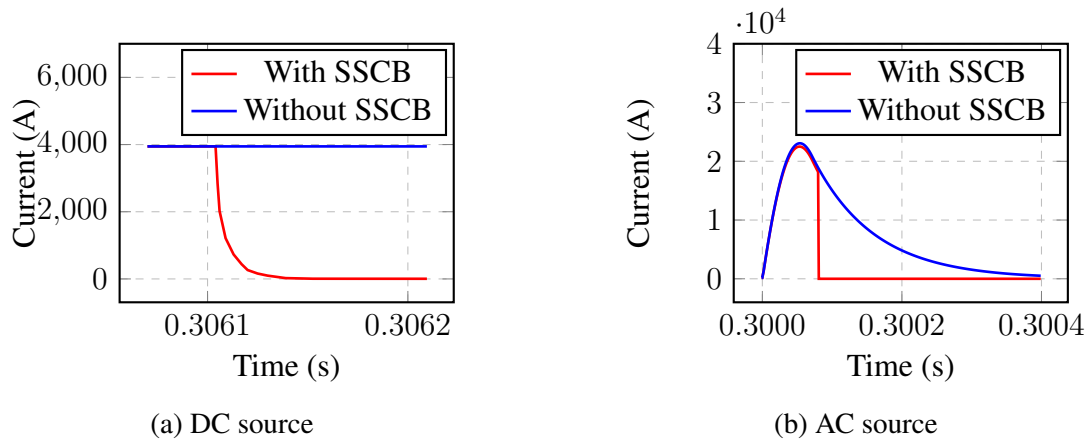


Figure 6.7: Comparison of current in DC SSCBs with and without SSCB.

6.2.1 Power Semiconductor Technology

The power semiconductor switch is the main component of the SSCB. Authors in [10] have done an extensive review of the different power semiconductor technologies focusing on low voltage and medium voltage. The choice of power semiconductor switch can be decided based on their properties such as

- Polarity - Unipolar and bipolar
- Material - Si and Wide bandgap (WBG) materials (SiC and GaN)
- Device topology

These properties have an impact on the voltage and current rating of the switch, cost and performance.

6.2.1.1 Based on Performance

- **Material:** Si-based semiconductor switches are more mature and commercially available for a wide range of voltage and current ratings. However, these devices cannot work above 200°C [48] and require a cooling system.

WBG material-based semiconductor switches show superior properties such as operation at higher temperatures and higher switching speeds leading to lower switching losses and also lower conduction losses compared to Si-based switches [10].

The comparison between Si, SiC and GaN is shown in the table

Semiconductor Material	Si	SiC	GaN
Bandgap (eV)	1.1	3.3	3.4
Breakdown Electric field (MV/cm)	0.3	2.5	3.3
Electron mobility ($cm^2v^{-1}s^{-1}$)	1400	1000	1200

Table 6.1: Comparison of Si, SiC and GaN [49]

- **Device Topology and Polarity:** Fully controlled switches such as MOSFET, IGBT and JFET can be considered. semiconrolled devices such as thyristors, also have low conduction losses, low cost and are suitable for high current applications. However, for such SSCB, an additional circuit to turn off the device has to be introduced which increases the complexity [10]. Switches using IGCT because of high conductivity modulation have very low conduction voltage drops at high current levels [49]. But, they do not fit well for low-level currents.

Normally on devices such as JFET, have low on resistance and are a very good option for SSCB. IGBT-based devices have low switching speeds and hence more switching losses compared to MOSFETs, but since the application does not require fast switching they can also be considered.

6.2.1.2 Based on Cost

Si-based devices are more mature and commercially available and have lower costs as compared to WBG-based devices such as SiC [50].

6.2.2 Voltage Clamping Circuit

Voltage clamping circuits are important in SSCBs and they perform the following two functions [31]:

- To clamp the transient voltage across the power semiconductor devices and avoid over-voltage damage.
- To absorb the residual energy left in the system parasitic inductances after semiconductor switches turn off.

According to Literature, voltage clamping can be achieved by using metal oxide varistors (MOV), transient voltage suppressor diode (TVS) or by using an RC snubber [51][52].

The main problem with SSCB is the cost and conduction loss due to the use of a semiconductor switch [53][54]. The next section explains hybrid CBs that combine the advantage of SSCB with faster switching and mechanical DCCB with lower conduction losses.

6.3 Hybrid CBs

Hybrid CBs use a combination of mechanical switches and a power semiconductor switch to break the circuit [55]. They are designed to make use of the advantages of both solid-state and mechanical CBs. The basic principle behind the working of hybrid CBs can be explained using the conventional hybrid CB as shown in Figure 6.8. The main path consists of a mechanical switch with a low on-state loss and a power semiconductor switch connected parallel to it. It also has a surge arrester connected in parallel that absorbs the excess energy [56].

The operation can be divided into three stages:

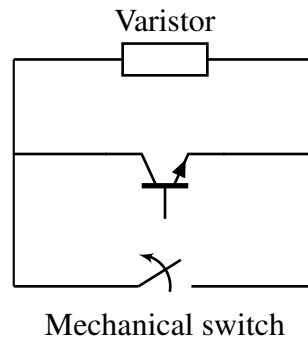


Figure 6.8: Basic hybrid CB

1. **Stage 1:** During normal operation current flows through the mechanical switch.
2. **Stage 2:** When a fault occurs, current is commutated to the semiconductor switch connected in parallel and the mechanical switch is turned off without arc formation.
3. **Stage 3:** Once, the voltage across the contacts is more than the system voltage and less than the withstand voltage of the semiconductor and mechanical switch, the semiconductor switch is turned off and current flows through the surge arrester, where energy is absorbed and voltage reaches system voltage.

There are different ways that the commutation happens from the mechanical switch to the semiconductor switch:

- **Natural Commutation:** In this mode of commutation, when a fault occurs, the voltage across the mechanical switch increases and if this voltage is higher than the forward voltage of the semiconductor switch, the current starts flowing through the semiconductor switch and hence current is commutated to the semiconductor switch. This type of commutation happens in Figure 6.8.
- **Voltage Zero Crossing Commutation:** This mode of commutation is shown in Figure 6.9a. It uses a series LC oscillation circuit that when the fault occurs produces an oscillation and a reverse current. This leads to an artificial zero crossing of current in the main branch and the mechanical switch is opened without the arc formation and the current is transferred to the semiconductor switch. The oscillations depend on the L and C values. The complexity in this method is increased due to the addition of L and C elements.
- **Resistance Zero Crossing Commutation:**

This mode of commutation uses semiconductor switches along with the mechanical switch in the main branch as shown in Figure 6.9b. When a fault occurs, the semiconductor is opened first, commutating the current to the parallel semiconductor branch ensuring arc-free switching of the mechanical switch. The main problem with this method is that during normal operation, current flows through the semiconductor switch in the main branch causing high conduction losses [57].

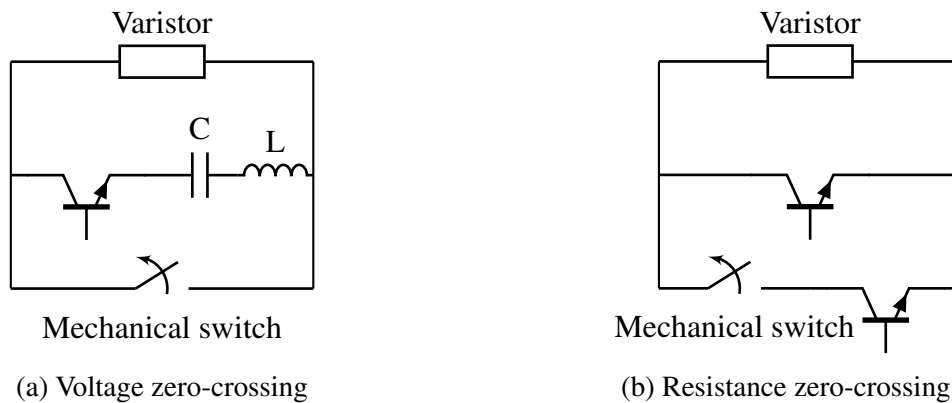


Figure 6.9: Types of hybrid DC CB commutation

6.4 DC FCL

The main problem associated with DC fault is that due to zero crossing of current and low impedance on the DC side, there is a rapid increase in SC current and the value is extremely high [12]. This affects the converter as the high current flows through the freewheeling diode and the power system in general. This raises the need for FCL that can reduce the rate of rise of SC current and decrease the overall current peak. Ideally, FCL are connected in series with the system and when a fault occurs they limit the peak current and reduce the rate of rise of current. The Important requirements of FCLs are as follows:

- Not affecting the normal operation.
- Controlling the SC fault current.

There are two major types of FCLs :

6.4.1 Resistive Type FCL

This type of FCL uses resistance in series with the system and when a fault occurs the peak is reduced [58]. Figure 6.10 shows the effect of resistance FCLs in limiting the current. As seen from the figure, this type of FCL can limit the current but cannot help restrict the rapidly rising fault current. Resistive FCLs are often a superconducting coil that has zero resistance during normal conditions but very high resistance during fault conditions [59].

The main problem with resistive FCLs is since it limits the current and do not affect the rate of rise, the value of resistance needed is quite high. This not only increases the cost but also the losses in the system. Alternative to this is the use of an inductor to limit the current that in addition to limiting the current, limits the rate of increase in current. Therefore a slower CB such as a mechanical or a hybrid can be used in combination with this [12].

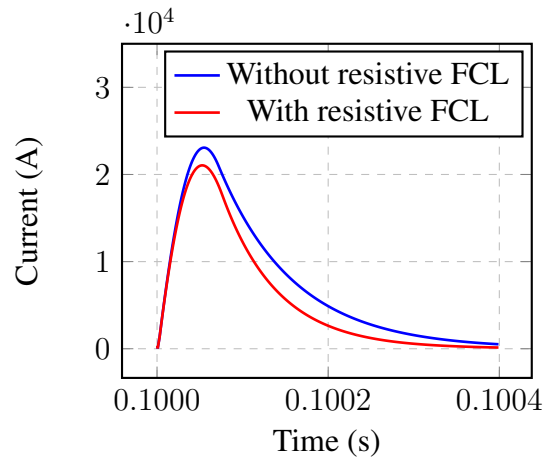


Figure 6.10: Effect of resistive FCL

6.4.2 Inductive Type FCL

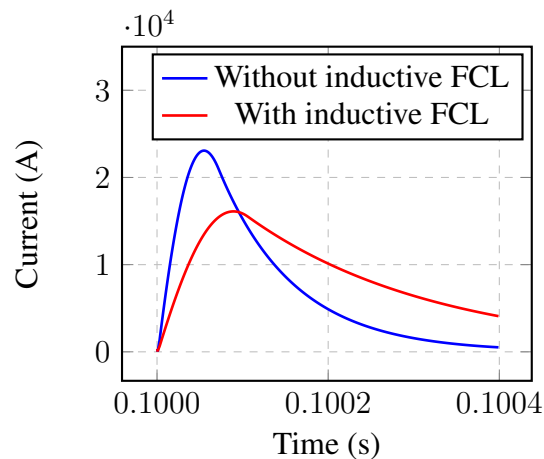


Figure 6.11: Effect of inductive FCL

Inductive type FCLs use DC reactors, which are inductor coils whose values can be calculated by using the equations given in [60], that have resistance due to the conductor material to reduce the peak and can also reduce the rate of rise of current. The DC SC current in the case of using inductive FCL is shown in Figure 6.11. The Authors in [12] have reviewed and compared different types of inductive FCLs such as flux coupling, iron core and solid-state. Considering several factors such as cost, complexity and losses, only solid-state inductive FCL is considered in this thesis.

6.4.2.1 With Bias Source

The Bridge type FCL with bias source is shown in Figure 6.12a and uses a diode bridge configuration, for bidirectional operation, with a DC reactor and a DC bias voltage source. This topology is introduced and explained in [61]. The DC bias voltage is selected such that the bias current I_b is more than the DC cable current I_{dc} .

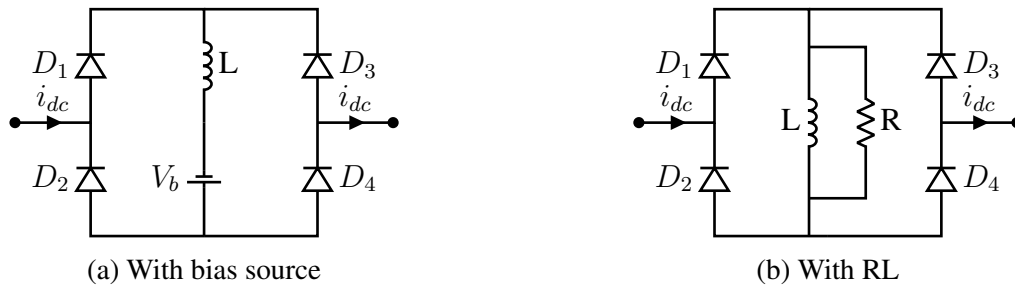


Figure 6.12: Solid state FCL

During normal operation, the current due to the bias voltage source is I_b and applying KCL, the current flows through all four diodes. The current flowing through the reactor is I_b and no DC current flows through the reactor. The current flowing through the diodes is given by

$$I_{D1} = \frac{I_b + I_{dc}}{2} \quad (6.1)$$

$$I_{D2} = \frac{I_b - I_{dc}}{2} \quad (6.2)$$

$$I_{D3} = \frac{I_b - I_{dc}}{2} \quad (6.3)$$

$$I_{D4} = \frac{I_b + I_{dc}}{2} \quad (6.4)$$

When a fault occurs, the DC current I_{dc} increases more than I_b and so $I_b - I_{dc}$ becomes negative leading to D_2 and D_3 becoming reverse biased and not conducting. Now the current flows through the limiting reactor. This type of FCL with a bias source is shown in Figure 6.12a.

6.4.2.2 With RL

The bridge type FCL with a parallel RL is shown in Figure 6.12b. This topology was first introduced in [62] in combination with a hybrid CB. However, this can also be used along with mechanical CBs with an higher value of the reactor. According to the authors in [62], during normal operation the current flows through the RL combination and the stability of the system is minimized. During fault conditions, the reactor and the resistor will function together, providing a reverse voltage and limiting the amplitude respectively. This topology along with the hybrid CB lowers the conduction loss to up to 52% [62]. But, they have not considered the loss due to the inductor. However, they have a significant contribution to the conduction losses [63].

6.5 Comparison

The overview of the comparison between DC protection technologies is shown in Figure 6.13. The following parameters are considered for comparing the technologies:

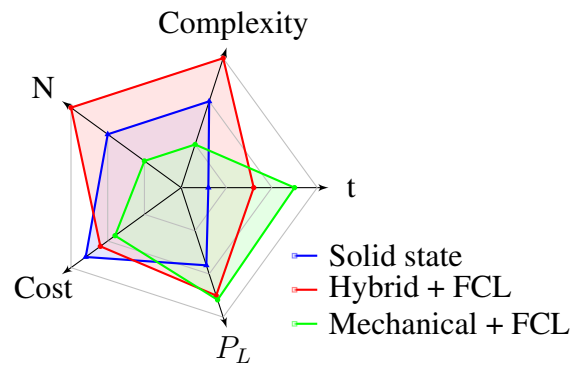


Figure 6.13: Overview of the comparison of DC protection technologies

6.5.1 Complexity

Hybrid CBs are the most complex DCCBs as they use both mechanical and semiconductor switches, followed by SCCBs due to the sensors and gate drivers needed for the semiconductor operation and the least complex DCCB is the mechanical CB [64].

6.5.2 Number of Components (N)

Hybrid CB has a greater number of components with both mechanical and semiconductor switches, followed by SCCB and DCCB has the least number of components.

6.5.3 Fault Interruption Time (t)

The interruption time of a DC mechanical CB is slightly less than 60 ms. Whereas, the interruption time of hybrid DCCB is around 2-30ms and SSCB is less than 1 ms [65].

6.5.4 Cost

The capital cost of different topologies can be compared for a common current and voltage rating of 80A and 400 V respectively. Considering DC mechanical CBs along with FCLs, the total cost is around 209 euros. Hybrid CBs also need FCLs but with a lower reactor value, leading to a total of 250 euros. Finally, SSCB cost goes up to 280 euros.

6.5.5 Conduction Power Loss (P_L)

Mechanical DCCB and hybrid DCCB have negligible conduction losses due to the presence of mechanical switches [66]. However, the combination of FCLs leads to very high losses due to high inductance and resistance values. SSCB on the other hand has high conduction losses due to the on-state resistance of the semiconductor [53].

6.6 Conclusion

In this chapter, different DCCBs such as mechanical, hybrid, solid-state and FCLs are studied and compared so that the DC fault current can be limited either by interrupting

before the peak current or by limiting the peak. From the comparison, it can be concluded that although the interruption time can be improved by using the latest technologies thereby limiting the current and increasing the system SCCR, they are still growing and because of their higher capital cost and losses they are not suitable to be implemented in the ASML system at this time. This chapter answers research question 5 regarding improving the protection of DC systems.

DESIGN OF SC ASSESSMENT TOOL

THE standardized methods proposed in the previous chapters to assess the system are implemented as a program or tool. This tool takes any system as an input and then based on the available SC current and SCCR of components assesses the system and gives the overall SCCR of the system as the output. This output is further used for physically testing the system. Due to time constraints, assessment of the system is only implemented on the AC side and only calculation of available SC current is implemented on the DC side. This chapter explains the design of the assessment tool and how different components are modeled.

7.1 Introduction

Various frameworks such as Matlab, python and javascript were considered to design the tool. Finally, Matlab was selected as the framework. This is because Matlab has libraries for power systems and simulink that make the visualization of waveforms and simulation a bit less complicated. More specifically the Simscape library is used to model the components and the Matlab appdesigner is used to build the Overall user interface for the application.

7.2 Software Architecture

The software architecture of the Matlab tool is designed to ensure modularity, scalability, and ease of maintenance. This tool uses a layered type of architecture and the layers are shown in Figure 7.1.

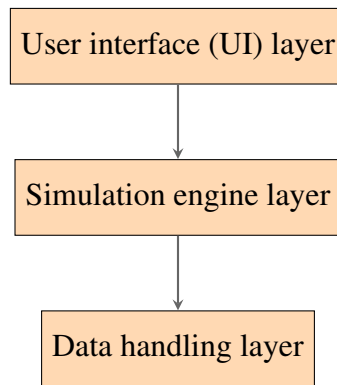


Figure 7.1: Layer based architecture

7.2.1 User Interface (UI) layer

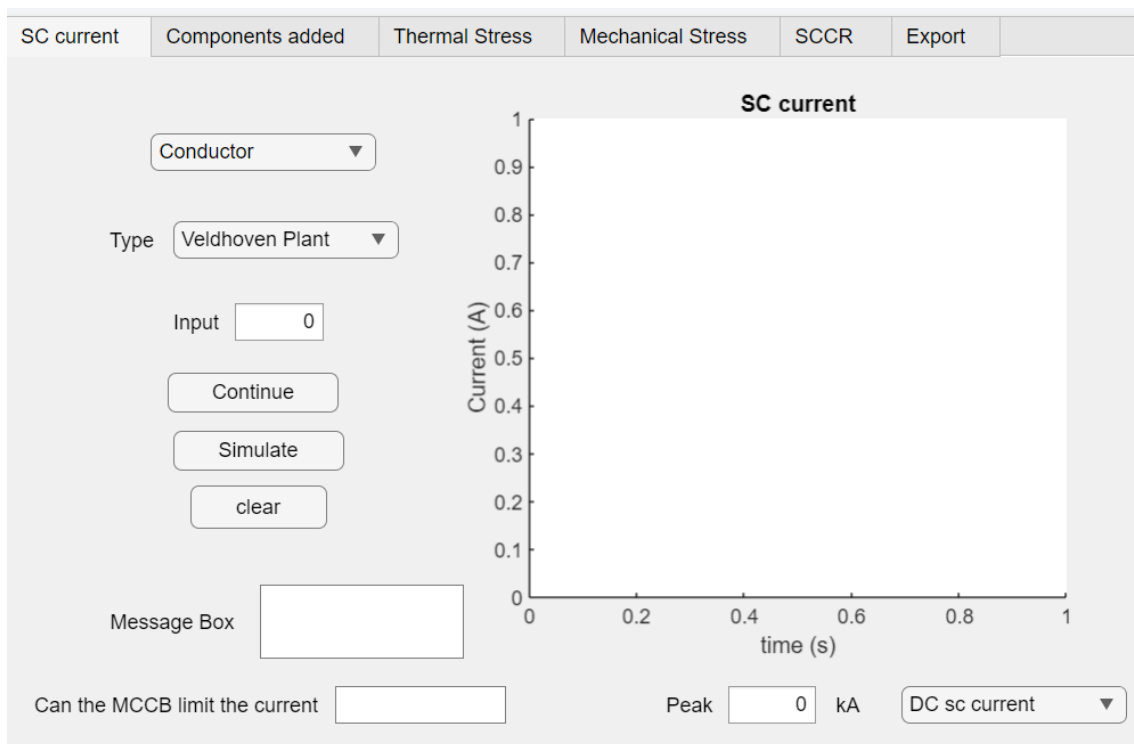


Figure 7.2: Tool UI

The UI layer provides an interface for the users to select the components and specify the designed system. Event-driven programming is used to design this layer. This means different events are triggered based on the input given by the user. The UI of the tool is shown in Figure 7.2 has six panels on the top and the contents of each panel are explained as follows:

7.2.1.1 SC Current

The SC current panel is the starting page of the tool and has two dropdown menus, one for selecting the type of component. The second dropdown menu is for selecting a spe-

cific type of component and its values are automatically updated based on the selected component from the first dropdown menu. There is also an input textbox, where specific inputs such as the length of the conductor can be updated.

The continue button is to select the next component, the Simulate button is to simulate the entire model and the clear button is to start a new design. The message box textbox responds to the selected input. The current waveform along with the peak is shown in the axes. An example system is simulated and the SC current panel is shown in Figure 7.3.

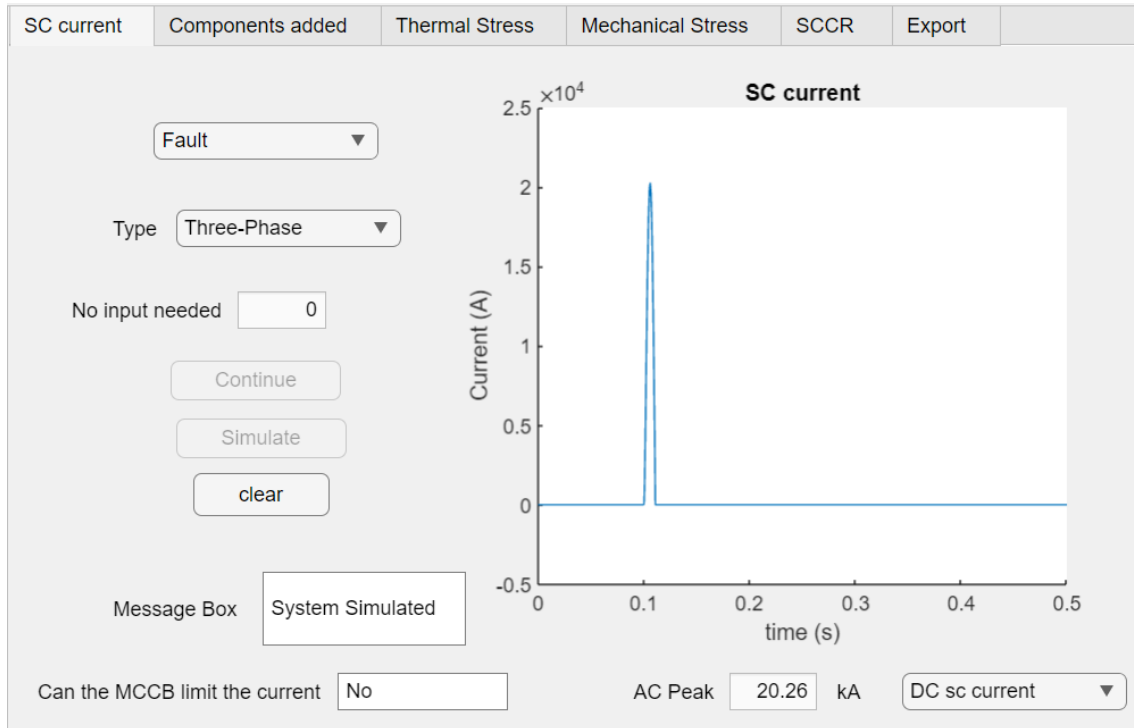


Figure 7.3: SC current panel

7.2.1.2 Components Added

This panel lists the components and their types that are selected and is updated based on each selection.

7.2.1.3 Thermal Stress

This panel based on the available SC current gets the peak let-through energy or joules energy from the CB datasheet and compares it with the Joules energy withstand capacity of the conductor, which is calculated using the Equation 7.1. The result of the comparison is presented in the textbox.

$$I^2t = k^2s^2 \quad (7.1)$$

Where s is the cross-section of the conductor in mm^2 and k is a factor that depends on the material. The value of k can be taken as 226, for a PVC insulation with a copper conductor [67].

7.2.1.4 Mechanical Stress

This panel based on the distance between conductors and support inputs given by the user, determines the force between the conductors based on Equation 4.5.

7.2.1.5 SCCR

This panel gets the peak let-through current from the CB datasheet. Compares this current with the SCCR of individual components and determines if all components can withstand the SC current. If all components can withstand, output is the overall SCCR of the system. Otherwise, design is not valid. The standardized methods described in the previous chapter are used in this panel.

7.2.1.6 Export

The Export panel has a button and when pressed makes a report of the design and exports a text file comparing the simulation results with the numerical calculation results.

The input and output of all the panels are summarized in Table 7.1.

Panel	Input	Output
SC current	1. Component 2. Type of component 3. Specific component input	SC current plot
Components added	No input	Gives the list of components added
Thermal stress	No input	Determine if conductors can withstand thermal stress
Mechanical stress	1. Distance between conductors 2. Distance between supports	Mechanical force between conductors
SCCR	No input	1. Determine if components can withstand the SC current 2. Overall SCCR 3. Check if design id fault tolerant
Export	File name	Exports a text file with all details

Table 7.1: Summary of the tool panels

7.2.2 Simulation Engine Layer

This layer is responsible for running simulations based on user inputs. The simulation utilizes Matlab Simscape and Simulink libraries to model electrical components and simulate their behavior. This layer also manages the creation, configuration, and execution of simulation models dynamically based on user-defined inputs.

In this layer, the modeling of different components is important and is explained in the subsequent sections.

7.2.2.1 Transformer

The maximum current on the secondary side of the transformer is calculated using Equation 3.9 and this is considered as the input current. The data such as transformer rating

and impedance percentage to calculate the maximum current on the secondary side is obtained from the transformer datasheet.

The Three-phase voltage source block from the Matlab Simscape library is used.

7.2.2.2 Conductor

A conductor is modeled by getting the values of the cross-section area and diameter of the wire from the datasheet and using the following equations to calculate the resistance and reactance of the conductor

$$R = \frac{\rho l}{A} \quad (7.2)$$

$$X_L = 2\pi f L \quad (7.3)$$

7.2.2.3 AC CB

The three-phase breaker block from the Simscape library in Matlab Simulink is used to model the AC CB. The type of fault can be selected in the block. Based on the available SC current, the breaker resistance is set to zero for standard CBs and current-limiting CBs. The peak let-through of the CB is determined from the let-through curves in the CB datasheet. The switching time of the CB is also set based on the characteristic curve of the CB from the datasheet.

7.2.2.4 Contactors, Busbars, EMI filters and Connectors

According to [3], components such as contactors, busbars, and connectors do not contribute any impedance to the SC current calculations, and thus, a virtual component in Matlab Simulink is used by considering a subsystem block.

7.2.2.5 AC - DC Converter

A Two-level VSC is considered for converting AC to DC. The modeling of the two-level converter is explained in Chapter 5. A two-level converter block is used, and the controllers are imported to the Simulink model.

7.2.3 Data Handling Layer

This layer is responsible for managing the input data from the user and the data obtained from the datasheet required for simulation based on user input. This layer also manages the export of the system to a text file.

The input data obtained from the user are stored in a global variable and the data from datasheets are stored as tables in the backend. The datasheets and values of all the components used are obtained from the database of ASML.

Component	Matlab block	Input	Values
Transformer	Three-phase source block	Voltage (V)	From datasheet
		Frequency (Hz)	From datasheet
		Available SC current (A)	From Equation
Conductor	Three-phase series RLC	Resistance	From datasheet
		Inductance	From Equation
CB	Three-phase Breaker	Tripping time	From characteristic curve in datasheet
		Resistance	From peak let-through curve in datasheet
Three phase fault	Three-phase fault	Type	User input
		Time	Voltage zero crossing
AC - DC converter	Two level converter	DC link voltage	User input
Contactar	Subsystem	-	-
Connector	Subsystem	-	-
EMI Filter	Subsystem	-	-
Busbar	Subsystem	-	-

Table 7.2: Summary of component modeling

7.3 Conclusion

In this chapter, the standardized method for system assessment is implemented as a Matlab tool. The architecture of the tool including the UI, modeling of components and outputs is elaborated. The result from this tool is validated by comparing it with a physical test result of a branch circuit from the mains distribution system of ASML in the next chapter.

CASE STUDY ASML

THIS chapter deals with validating the assessment methods developed in the earlier sections implemented as a tool with the physically tested results of the ASML machine. As mentioned in the previous chapter, due to time constraints, only the AC side is considered for validation. First, the branch circuit in the ASML mains distribution system taken for validation is explained. Next, the results are compared.

8.1 The System

The ASML machine consists of several cabinets or panels that are connected and perform various functionalities. The mains distribution system is part of the mains cabinet that is connected to the feeder. The considered branch circuit is part of the mains distribution system and is shown in Figure 8.1. The different components used in the circuit along with their model and SCCR values are shown in Table 8.1.

The available current on the secondary side of the transformer is 30 kA. There are two current limiting molded case circuit breaker (MCCB) connected and a standard miniature circuit breaker (MCB) connected before the location of the fault.

Type	Model	SCCR (kA)
Transformer	-	30
MCCB 1	Eaton NZMN 23 AF175-NA	35
Conductor 1	70 mm ²	-
MCCB 2	Eaton NZMB1-3 AF30 NA	35
Conductor 2	6 mm ²	-
Connector	Harting Han HsB	5
Contactors	Eaton DILM 32-10	10
Busbar	-	10
MCB	Eaton FAZ-C13NA	10
Conductor 3	25 mm ²	-

Table 8.1: Components in the circuit

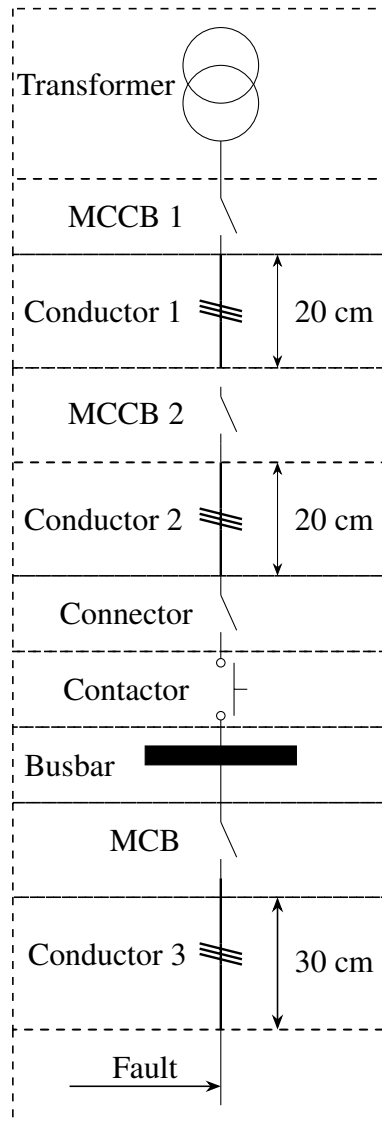


Figure 8.1: Branch circuit of ASML mains distribution system

8.2 Comparison of Results

To compare the results, a three-phase fault scenario is considered at the location as shown in Figure 8.1 at 0.1 sec and the results of available SC current obtained from Matlab tool and physical tests are compared.

The data of each component used is obtained from the database of ASML. The system is given as input to the Matlab tool by selecting the appropriate components along with their types which are already added to the database in the tool. The output screenshots of the tool are shown in the Appendix C. The SC current with and without CBs obtained from the tool are shown in Figure 8.3 and Figure 8.2 respectively.

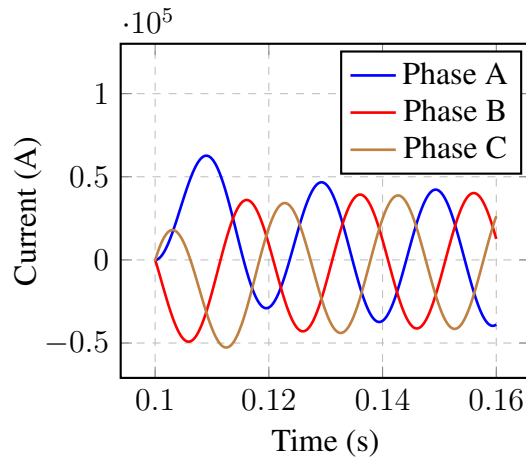


Figure 8.2: SC current without CB

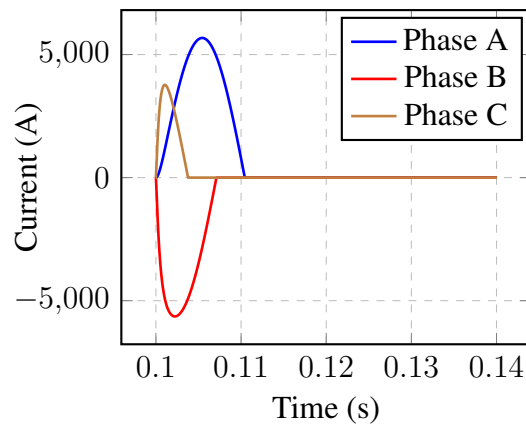


Figure 8.3: SC current with current limiting CB

The physical test results for this system are obtained from ASML and the test is conducted by a testing company according to the methods given in IEC standards. The comparison between the results is shown in Table 8.2.

	Peak SC current (kA)	SCCR (kA)
Matlab tool	5.7	35
Physical test	4.8	35

Table 8.2: Comparison of results

From Table 8.2, it can be seen that there is a difference between the result from the tool and the physically tested result. This is because the IEC 60909-0 standard does not consider the impedance of busbars, connectors, and contactors while calculating the available SC current. However, these elements have some impedance that lowers the available SC current.

The SCCR of the system through the assessment method is 35 kA because of the series connection of current limiting CBs, which is not physically allowed according to UL508A. However, as the test is performed by a certified laboratory and the system can withstand 35 kA, this is considered the SCCR of the system.

8.3 Conclusion

This chapter considers and assesses a branch circuit of the ASML mains distribution system using the Matlab tool. The results from the tool are validated with the results obtained from the physical testing of the circuit, and the reason for the variation in the results was also explained. This chapter answers the research question 7.

CONCLUSION

For assessment of the industrial mains distribution system, available SC current has to be calculated, compared with the component SCCR and the overall SCCR of the system has to be determined. This overall SCCR is then given as the current input during the SC physical tests of the system to verify the results. Since the assessment is implemented as a program, the closeness between the theoretical calculation and numerical simulation methods becomes important. To simulate the system, all components have to be modeled and this was done in Matlab. Moreover, as the assessment has to comply with various international standards, the connection and difference between the standards were studied.

The standardized method to calculate the available SC current on both AC and DC systems was described and the reason for the slight variation of around 1.5% between the simulation and calculation results was due to the $\frac{X}{R}$ factor in the AC side and difference in impedance on the DC side. Sensitivity analysis was done to determine the factor of difference to make the results exactly match. Based on the literature, a standardized method to determine the overall SCCR of the system was elaborated.

It was established that a higher SCCR is better and the SCCR of the system can be increased by improving the system protection so that the SC current is limited. To improve the protection on the AC side, a current limiting CB was examined and they have more advantages compared to traditional CBs considering factors such as reduced thermal and mechanical stress, reduced cost and reduced overall peak. The overall SCCR is increased in this case, which is confirmed by the physical test results. Various DCCB technologies such as hybrid and solid-state including different topologies of FCLs were examined on the DC side. SSCB has the advantage of lower interruption time. However, they have higher conduction losses and increased capital costs. DC mechanical CB on the other hand is cheap but is quite slow and requires the need for an FCL in combination that can limit the current. This increases complexity, cost and losses. Finally, hybrid CB was considered, and although it has advantages such as lower losses and faster interruption, they are more complex and slow as compared to the rise in DC fault current. Thus, an FCL in combination with the CB is needed in this case. Based on the analysis, theoretically, all three can be used but it depends on ASML if they are ready to invest in the new technologies considering the costs and losses as a consequence of increasing the SCCR.

A Matlab assessment tool was developed based on the standardized methods determined. This tool based on the given system input, calculates the available SC current, compares it with the SCCR of individual components and gives out the overall SCCR of the system. However, due to time constraints, assessment can be done only on the AC side and only the SC current can be calculated on the DC side. Finally, the results of the tool are compared with the physically tested result of a branch circuit of the ASML mains distribution system. The comparison led to the conclusion that the components such as busbars, contactors and connectors that were initially thought of as not contributing to the SC current according to IEC [3], indeed contribute and the variation in the SC current value was determined.

In short, the SC assessment method was established in this thesis for the industrial mains distribution system and was implemented as a Matlab tool. The results of the tool were validated with the results from physical tests. Finally, various ways to improve the SCCR were examined answering all the research questions that needed to be answered to achieve the main objective of this master thesis.

CURRENT LIMITING CB

Figure A.1 and Figure A.2 shows the peak let-through current and peak let-through energy curves of the current limiting Eaton NZMN series circuit breaker.

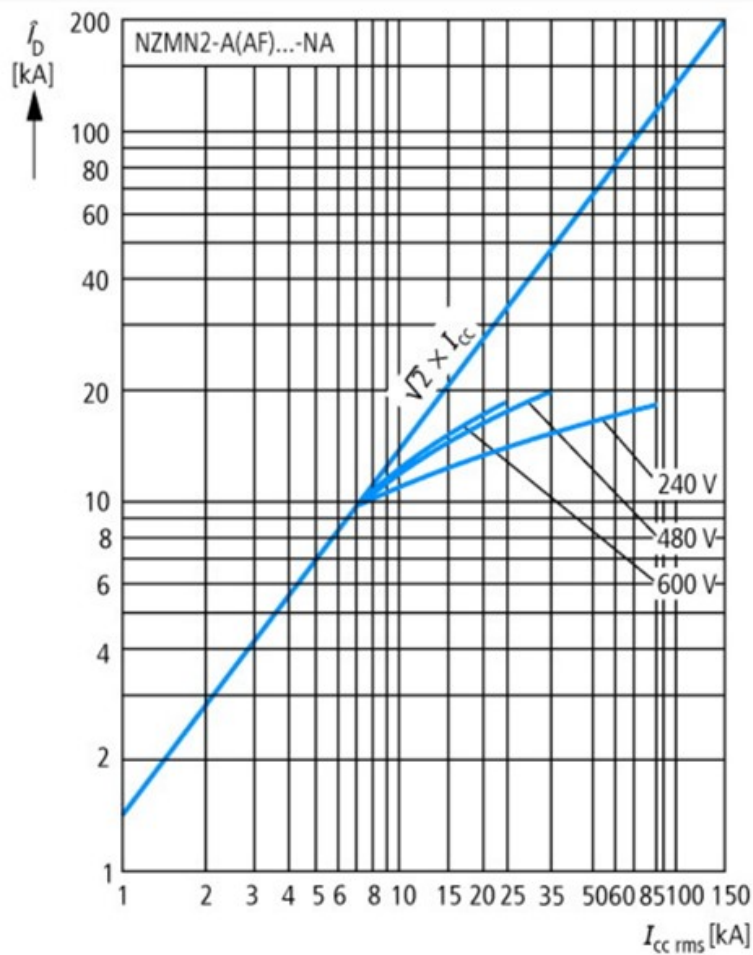


Figure A.1: Peak let-through current of Eaton NZMN series from datasheet

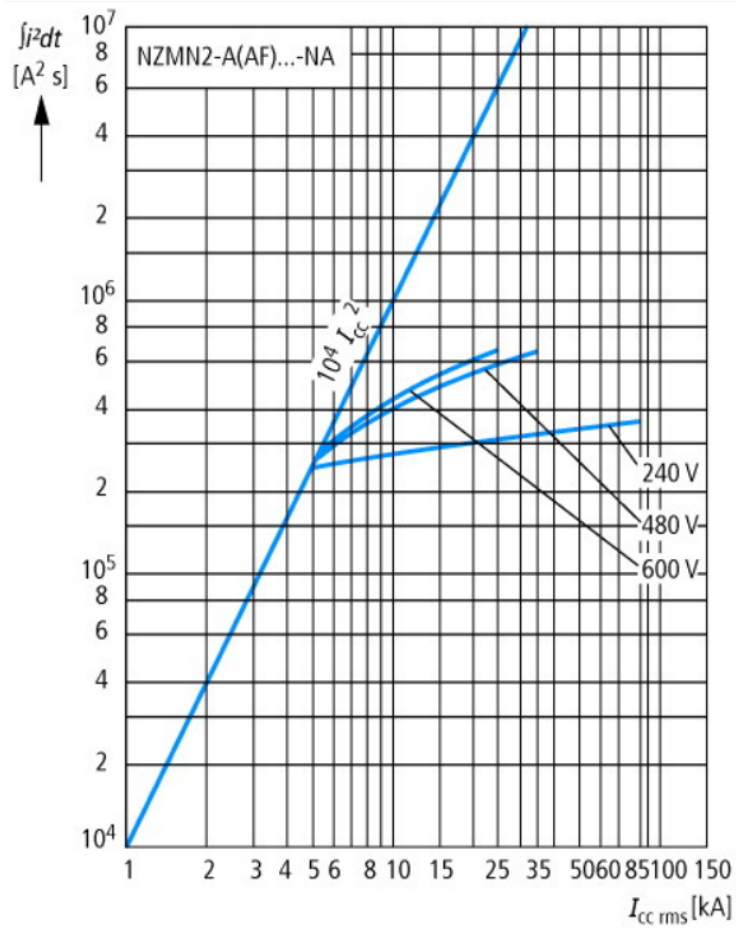


Figure A.2: Peak let through energy of Eaton NZMN series from datasheet



PARK TRANSFORMATION

The equation of park transformation to convert from abc to dq reference frame is given by

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2}{3}) & \cos(\theta + \frac{2}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2}{3}) & -\sin(\theta + \frac{2}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (\text{B.1})$$



TOOL RESULTS

The following figures show the output of the matlab tool for the branch circuit of ASML mains distribution system considered for validation of the results.

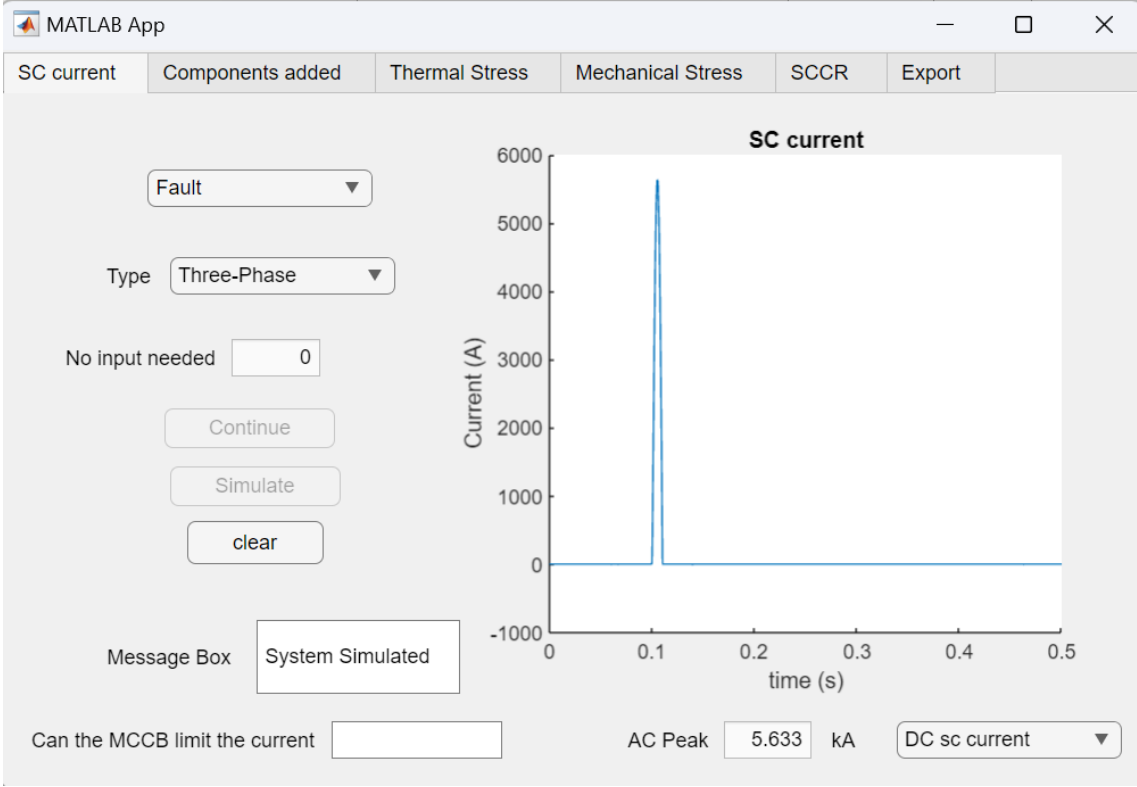


Figure C.1: Result 1

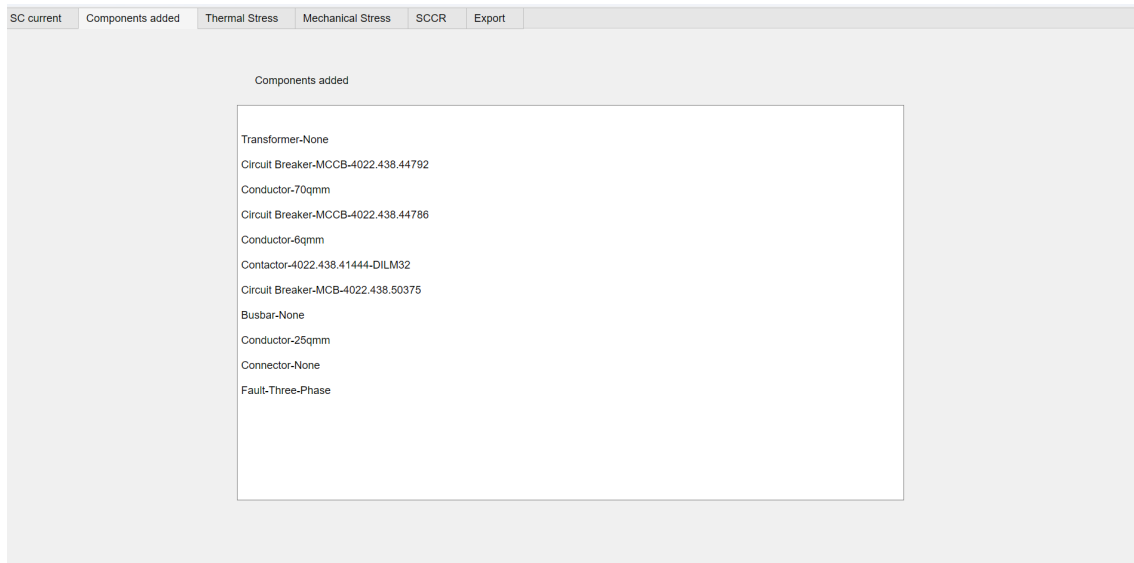


Figure C.2: Result 2

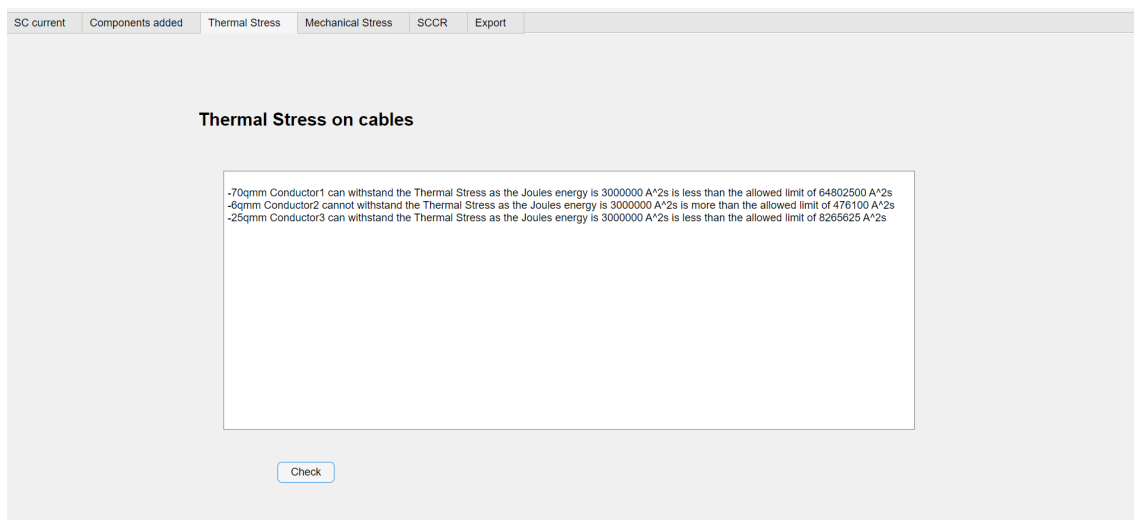


Figure C.3: Result 3

SC current Components added Thermal Stress Mechanical Stress **SCCR** Export

Mechanical Force on Cables

Distance between Supports in m

Distance between Conductors in m

Force N

Short circuit time Sec

Figure C.4: Result 4

SC current Components added Thermal Stress Mechanical Stress **SCCR** Export

-MCCB1 can withstand the SC current as the Interrupting rating is 35000 A and available short-circuit current is 30000 A
-MCCB2 can withstand the SC current as the Interrupting rating is 35000 A and available short-circuit current is 10466.9905 A
-MCB1 can withstand the SC current as the Interrupting rating is 15000 and available short-circuit current is 3982.9673 A
-Contactor1 can withstand the short-circuit as the SCCR is 5000 A and available SC current of 3982.9673 A
-SCCR of Connector1 is 10000 and can withstand the short-circuit as available SC current of 3982.9673A
-SCCR of Busbar 1 is 10000 A and can withstand the short-circuit as available SC current is 3982.9673 A

Overall SCCR (IEC) kA

Overall SCCR (UL) kA

Component(s) that cannot withstand the SC current

IEC - All components can withstand - The design is okay

Figure C.5: Result 5

BIBLIOGRAPHY

- [1] “Moore’s law”. In: (). URL: <https://www.asml.com/en/technology/all-about-microchips/moores-law>.
- [2] “About ASML”. In: (). URL: <https://www.asml.com/en/news/stories/2021/semiconductor-manufacturing-process-steps>.
- [3] “IEC 60909-0:2016, Short circuit currents in three-phase a.c. systems - Part 0: Calculation of currents”. In: *International Electrotechnical Commission* (2016).
- [4] Jin Yang, John E. Fletcher, and John O’Reilly. “Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables”. In: *IEEE Transactions on Industrial Electronics* 59.10 (2012), pp. 3827–3837. DOI: 10.1109/TIE.2011.2162712.
- [5] “IEC 60909-1:2016, Factors for the calculation of short-circuit currents according to IEC 60909-0”. In: *International Electrotechnical Commission* (2016).
- [6] “NFPA 79: 2021, Electrical Standard for Industrial Machinery”. In: (2021).
- [7] Soumya R Mohanty D N. Vishwakarma Badri Ram. *Power System Protection And Switchgear*. Tata McGraw Hill Education Private Limited, 2022.
- [8] Botong Li et al. “A protection scheme for MMC–HVDC grid based on blocking time of converter station”. In: *International Journal of Electrical Power Energy Systems* 152 (2023), p. 109241. ISSN: 0142-0615. DOI: <https://doi.org/10.1016/j.ijepes.2023.109241>. URL: <https://www.sciencedirect.com/science/article/pii/S0142061523002983>.
- [9] Christian M. Franck. “HVDC Circuit Breakers: A Review Identifying Future Research Needs”. In: *IEEE Transactions on Power Delivery* 26.2 (2011), pp. 998–1007. DOI: 10.1109/TPWRD.2010.2095889.
- [10] Rostan Rodrigues et al. “A Review of Solid-State Circuit Breakers”. In: *IEEE Transactions on Power Electronics* 36.1 (2021), pp. 364–377. DOI: 10.1109/TPEL.2020.3003358.

- [11] Ana Rafaela Figueiredo Bento, Fernando Bento, and Antonio J. Marques Cardoso. “A Review on Hybrid Circuit Breakers for DC Applications”. In: *IEEE Open Journal of the Industrial Electronics Society* 4 (2023), pp. 432–450. DOI: 10.1109/OJIES.2023.3320900.
- [12] Hang Zhou et al. “Inductive Fault Current Limiters in VSC-HVDC Systems: A Review”. In: *IEEE Access* 8 (2020), pp. 38185–38197. DOI: 10.1109/ACCESS.2020.2976116.
- [13] M. K. Bucher et al. “Options for ground fault clearance in HVDC offshore networks”. In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2012, pp. 2880–2887. DOI: 10.1109/ECCE.2012.6342371.
- [14] Rockwell Automation. “Global Short-circuit Current Ratings Tool”. In: (). URL: <https://www.rockwellautomation.com/en-us/support/product/product-selection-configuration/global-short-circuit-current-ratings-tool.html>.
- [15] “UL 508A: 2018, Industrial control Panels”. In: (2022).
- [16] “IEC 60909-0:2016, Short circuit currents in three-phase a.c. systems - Part 0: Calculation of currents”. In: *International Electrotechnical Commission* (2016).
- [17] Sander A. Franke. *Fault Current Control in the Transmission Network*. 2012.
- [18] L. van der Sluis. *Transients in Power Systems*. John Wiley and Sons, Inc., 2001.
- [19] Jr W. Stevenson J. Grainger. *Power System Analysis*. McGraw-Hill, Inc., 1994.
- [20] Xiaofeng Zhang et al. “A distribution short circuit analysis approach using hybrid compensation method”. In: *IEEE Transactions on Power Systems* 10.4 (1995), pp. 2053–2059. DOI: 10.1109/59.476075.
- [21] T.-H. Chen et al. “Distribution system short circuit analysis-A rigid approach”. In: *IEEE Transactions on Power Systems* 7.1 (1992), pp. 444–450. DOI: 10.1109/59.141741.
- [22] C. L. Fortescue. “Method of Symmetrical Co-Ordinates Applied to the Solution of Polyphase Networks”. In: *Transactions of the American Institute of Electrical Engineers* XXXVII.2 (1918), pp. 1027–1140. DOI: 10.1109/T-AIEE.1918.4765570.
- [23] Jr William D. Stevenson. *Elements of power system analysis*. McGraw-Hill, Inc., 1955.
- [24] “IEC 60909-1:2016, Factors for the calculation of short-circuit currents according to IEC 60909-0”. In: *International Electrotechnical Commission* (2016).
- [25] Mulukutla S. Sarma J. Duncan Glover Thomas J. Overbye. *Power System Analysis and Design*. Cengage Learning, 2015.
- [26] I. Kasikci. “Definitions: Methods of Calculations. In Short Circuits in Power Systems”. In: *John Wiley Sons, Ltd* (2018). URL: <https://doi.org/10.1002/9783527803378.ch1>.
- [27] Waider. G. *Impedance correction factors during the short-circuit current calculation with the equivalent voltage source at the short-circuit location, TH Darmstradt*. 1992.

- [28] P.Schueller. “Cahier technique.63, LV breaking by current limitation”. In: *Schneider electric* (2005).
- [29] “IEC 60865-1:2016, Short-circuit currents - Calculation of effects - Part 1: Definitions and calculation methods”. In: *International Electrotechnical Commission* (2021).
- [30] Baina He and Yunwei Zhao. “Simulation and Research of Transient Recovery Voltage”. In: *2012 Sixth International Conference on Electromagnetic Field Problems and Applications*. 2012, pp. 1–4. DOI: 10.1109/ICEF.2012.6310413.
- [31] Lisa Qi L. John Shen Z. “Overview of Direct Current Fault Protection Technology”. In: *Power Systems*. Springer, Cham (2023).
- [32] Sul Ademi et al. “Fault current characterisation in VSC-based HVDC systems”. In: *13th International Conference on Development in Power System Protection 2016 (DPSP)*. 2016, pp. 1–7. DOI: 10.1049/cp.2016.0043.
- [33] B. Chang et al. “Point-to-point two-level converter system faults analysis”. In: *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*. 2014, pp. 1–6. DOI: 10.1049/cp.2014.0252.
- [34] Jin Yang, John E. Fletcher, and John O’Reilly. “Multi-terminal DC wind farm collection and transmission system internal fault analysis”. In: *2010 IEEE International Symposium on Industrial Electronics*. 2010, pp. 2437–2442. DOI: 10.1109/ISIE.2010.5637547.
- [35] “Short-circuit currents in d.c. auxiliary installations in power plants and substations - Part 1: Calculation of short-circuit currents”. In: *International Electrotechnical Commission* (1997).
- [36] Jared Candelaria and Jae-Do Park. “VSC-HVDC system protection: A review of current methods”. In: *2011 IEEE/PES Power Systems Conference and Exposition*. 2011, pp. 1–7. DOI: 10.1109/PSCE.2011.5772604.
- [37] Fabricio A. Mourinho et al. “Modeling and analysis of superconducting fault current limiters applied in VSC-HVDC systems”. In: *2015 IEEE Power Energy Society General Meeting*. 2015, pp. 1–5. DOI: 10.1109/PESGM.2015.7286262.
- [38] Miad Ahmadi et al. “Implementation of DC Micro Grid Tied PV-Storage Based EV Fast Charging Station”. In: *2021 IEEE International Conference on Environment and Electrical Engineering and 2021 IEEE Industrial and Commercial Power Systems Europe (EEEIC / ICPS Europe)*. 2021, pp. 1–6. DOI: 10.1109/EEEIC/ICPSEurope51590.2021.9584631.
- [39] Mojtaba Ahmadi and Shahram Karimi. “Voltage unbalance compensation using new structure of decouple double synchronous reference frame in stand-alone microgrids”. In: *IET Generation, Transmission & Distribution* 14.22 (2020), pp. 5093–5103. DOI: <https://doi.org/10.1049/iet-gtd.2020.0209>. eprint: <https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/iet-gtd.2020.0209>. URL: <https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-gtd.2020.0209>.

- [40] Miad Ahmadi et al. “Integration of Distributed Energy Resources and EV Fast-Charging Infrastructure in High-Speed Railway Systems”. In: *Electronics* 10.20 (2021). ISSN: 2079-9292. DOI: 10.3390/electronics10202555. URL: <https://www.mdpi.com/2079-9292/10/20/2555>.
- [41] “Two-Level, Three-Phase Voltage-Sourced Converter”. In: *Voltage-Sourced Converters in Power Systems*. John Wiley Sons, Ltd, 2010. Chap. 5, pp. 115–126. ISBN: 9780470551578. DOI: <https://doi.org/10.1002/9780470551578.ch5>. eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/9780470551578.ch5>. URL: <https://onlinelibrary.wiley.com/doi/abs/10.1002/9780470551578.ch5>.
- [42] Ibrahim Alwazah et al. “Analysis of The Three-Phase AC Short-Circuit And The DC Short-Circuit in a VSC-MTDC System”. In: *2023 5th International Youth Conference on Radio Electronics, Electrical and Power Engineering (REEPE)*. Vol. 5. 2023, pp. 1–6. DOI: 10.1109/REEPE57272.2023.10086911.
- [43] Ranran Xie et al. “Fault Characteristics Study of VSC Converter and Protection Design in DC Microgrids”. In: *2018 IEEE International Conference on Energy Internet (ICEI)*. 2018, pp. 241–246. DOI: 10.1109/ICEI.2018.00051.
- [44] Shining Lu. *DC Cable Short Circuit Fault Protection in VSC-MTDC*. 2021.
- [45] D. Naidoo and N.M. Ijumba. “HVDC line protection for the proposed future HVDC systems”. In: *2004 International Conference on Power System Technology, 2004. PowerCon 2004*. Vol. 2. 2004, 1327–1332 Vol.2. DOI: 10.1109/ICPST.2004.1460207.
- [46] Tanel Jalakas et al. “Design of Solid State Circuit Breaker”. In: *2022 IEEE 63th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*. 2022, pp. 1–5. DOI: 10.1109/RTUCON56726.2022.9978903.
- [47] Yufeng Wang et al. “A Novel Solid-State Circuit Breaker for DC Microgrid System”. In: *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles International Transportation Electrification Conference (ESARS-ITEC)*. 2018, pp. 1–6. DOI: 10.1109/ESARS-ITEC.2018.8607419.
- [48] José Millán et al. “A Survey of Wide Bandgap Power Semiconductor Devices”. In: *IEEE Transactions on Power Electronics* 29.5 (2014), pp. 2155–2163. DOI: 10.1109/TPEL.2013.2268900.
- [49] Jesper Magnusson and David Schaeffer. “ABB’s Recent Advances on Hybrid DC Circuit Breakers”. In: *Direct Current Fault Protection: Basic Concepts and Technology Advances*. Ed. by Isik C. Kizilyalli, Z. John Shen, and Daniel W. Cunningham. Cham: Springer International Publishing, 2023, pp. 225–242. DOI: 10.1007/978-3-031-26572-3_10. URL: https://doi.org/10.1007/978-3-031-26572-3_10.

- [50] Haichen Liu et al. “Si IGBT and SiC MOSFET Hybrid Switch-Based Solid State Circuit Breaker for DC Applications”. In: *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2022, pp. 1–6. DOI: 10.1109/ECCE50734.2022.9948172.
- [51] Ana Rafaela Figueiredo Bento, Fernando Bento, and Antonio J. Marques Cardoso. “A Novel DC Circuit Breaker with an Absorbing Branch Based on TVS Diodes”. In: *2023 IEEE Fifth International Conference on DC Microgrids (ICDCM)*. Vol. Single. 2023, pp. 1–5. DOI: 10.1109/ICDCM54452.2023.10433588.
- [52] Thanh Long Le et al. “Solid-state Circuit Breaker for aircraft high voltage DC network”. In: *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2024, pp. 3100–3107. DOI: 10.1109/APEC48139.2024.10509126.
- [53] A. Yulong Liu et al. “A Review of Research Progress on Low-Voltage DC Solid-State Circuit Breakers”. In: *2024 IEEE 10th International Power Electronics and Motion Control Conference (IPEMC2024-ECCE Asia)*. 2024, pp. 3551–3556. DOI: 10.1109/IPEMC-ECCEAsia60879.2024.10567620.
- [54] Waqas Ali, Ara Bissal, and Martin März. “Modeling and experimental verification of a hybrid DC breaker during fault interruption”. In: *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2023, pp. 1851–1857. DOI: 10.1109/APEC43580.2023.10131382.
- [55] Anshuman Shukla and Georgios D. Demetriades. “A Survey on Hybrid Circuit-Breaker Topologies”. In: *IEEE Transactions on Power Delivery* 30.2 (2015), pp. 627–641. DOI: 10.1109/TPWRD.2014.2331696.
- [56] Francis B. Effah et al. “Hybrid HVDC circuit breaker with self-powered gate drives”. In: *IET Power Electronics* 9.2 (2016), pp. 228–236. DOI: <https://doi.org/10.1049/iet-pel.2015.0531>. eprint: <https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/iet-pel.2015.0531>. URL: <https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-pel.2015.0531>.
- [57] Asif Khan et al. “Performance analysis of DC circuit breakers for future HVDC grids in GB”. In: *17th International Conference on Developments in Power System Protection (DPSP 2024)*. Vol. 2024. 2024, pp. 206–213. DOI: 10.1049/icp.2024.0977.
- [58] Bin Li and Jiawei He. “Studies on the Application of R-SFCL in the VSC-Based DC Distribution System”. In: *IEEE Transactions on Applied Superconductivity* 26.3 (2016), pp. 1–5. DOI: 10.1109/TASC.2016.2537049.
- [59] Jude Inwumoh, Kosala Gunawardane, and Craig Baguley. “Impact of Superconducting Resistive-FCL on MMC-HVDC Fault”. In: *2021 IEEE 12th Energy Conversion Congress Exposition - Asia (ECCE-Asia)*. 2021, pp. 1088–1092. DOI: 10.1109/ECCE-Asia49820.2021.9479158.
- [60] Bin Li and He. “A Novel Solid-State Circuit Breaker With Self-Adapt Fault Current Limiting Capability for LVDC Distribution Network”. In: *IEEE Transactions on Power Electronics* 34.4 (2019), pp. 3516–3529. DOI: 10.1109/TPEL.2018.2850441.

- [61] Jiawei He, Bin Li, and Ye Li. “Analysis of the fault current limiting requirement and design of the bridge-type FCL in the multi-terminal DC grid”. In: *IET Power Electronics* 11.6 (2018), pp. 968–976. DOI: <https://doi.org/10.1049/iet-pel.2017.0493>. eprint: <https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/iet-pel.2017.0493>. URL: <https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-pel.2017.0493>.
- [62] Huijie Lyu et al. “An Improved Hybrid DC Circuit Breaker With Self-Adaptive Fault Current Limiting Capability”. In: *IEEE Transactions on Power Electronics* 37.4 (2022), pp. 4730–4741. DOI: 10.1109/TPEL.2021.3121180.
- [63] T. Shimizu et al. “Loss evaluation of AC filter inductor core on a PWM converter”. In: *8th International Conference on Power Electronics - ECCE Asia*. 2011, pp. 1047–1052. DOI: 10.1109/ICPE.2011.5944704.
- [64] Weijiang Chen et al. “Development and prospect of direct-current circuit breaker in China”. In: *High Voltage* 6.1 (2021), pp. 1–15. DOI: <https://doi.org/10.1049/hve2.12077>. eprint: <https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/hve2.12077>. URL: <https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/hve2.12077>.
- [65] M. Mobarrez et al. “Comparative study of DC circuit breakers using realtime simulations”. In: *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*. 2014, pp. 3736–3742. DOI: 10.1109/IECON.2014.7049056.
- [66] Javadi Taherzadeh Radmanesh. “Circuit breakers in HVDC systems: state-of-the-art review and future trends”. In: *Prot Control Mod Power Syst* 8 (2023).
- [67] “IEC 60364-1:2005, Low-voltage electrical installations – Part 1: Fundamental principles, assessment of general characteristics, definitions”. In: *International Electrotechnical Commission* (2005).