MSc thesis in Electrical Engineering, Mathematics and Computer Science

12-pulse buck rectifier and partial power processing based converter for ultra-high power EV charging

Dun Lan

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12-PULSE BUCK RECTIFIER AND PARTIAL POWER PROCESSING BASED CONVERTER FOR ULTRA-HIGH POWER EV CHARGING

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Dun Lan

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Faculty of Electrical Engineering, Mathematics and Computer Science
Delft University of Technology

Supervisors:	Prof. Dr. ir. Pavol Bauer
	Dr.Zian Qin
committee member:	Prof. Dr. ir. Pavol Bauer
	Dr.Zian Qin
	Dr.ir. Jose Rueda Torres

ABSTRACT

With the rapid development of electrical vehicles (EV) and the trends in transportation electrification, the demand for fast charging facilities for electric vehicles is rising.

In this thesis, a two-stage power electronics converter for DC fast battery charging application is designed and studied. A buck type 12-pulse converter with triangular current shaping method for harmonic reduction and power factor correction is chosen to be the front-end converter. Back-end converter is designed to be a full bridge converter with partial power processing technique.

This thesis innovatively proposed highly efficient ultra-fast charger charger using the multiple pulses rectifier with partial power processing DC-DC converter.

This EV fast charger meets the requirements of isolation, high efficiency, high output voltage and good power quality (low THD and unity power factor). This thesis describes in detail the analytical modeling of the studied circuit, including the loss modeling of the semiconductors and passive components and the design of three phase three winding transformer and phase shift full bridge transformer. Finally, the simulation results and experimental results of the proposed EV fast charging system are presented and analyzed.

ACKNOWLEDGEMENTS

During the thesis project, my theoretical knowledge has been put into practice and my experimental skills have been improved. I would like to express my sincere thanks to the following people who helped me a lot during the thesis.

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ACRONYMS AND SYMBOLS

1 INTRODUCTION

1.1 MOTIVATION

Over the past decades, the importance of reducing greenhouse gas emissions has taken root. Tremendous efforts from both researchers and industry are devoted to reducing carbon emissions. It is worth noting that transportation is responsible for 24% of direct CO_2 emissions from fuel combustion [17]. The electrification of transportation will greatly boost the progress towards zero emissions. A major part of transportation electrification is the replacement of internal combustion engines (ICE) vehicles with Electric vehicles (EV). After a decade of rapid growth, in 2020 the global electric car stock hit the 10 million mark, a 43% increase over 2019, and representing a 1% stock share [16]. China, with 4.5 million electric cars, has the largest fleet, though Europe had the largest annual increase to reach 3.2 million in 2020 [16].

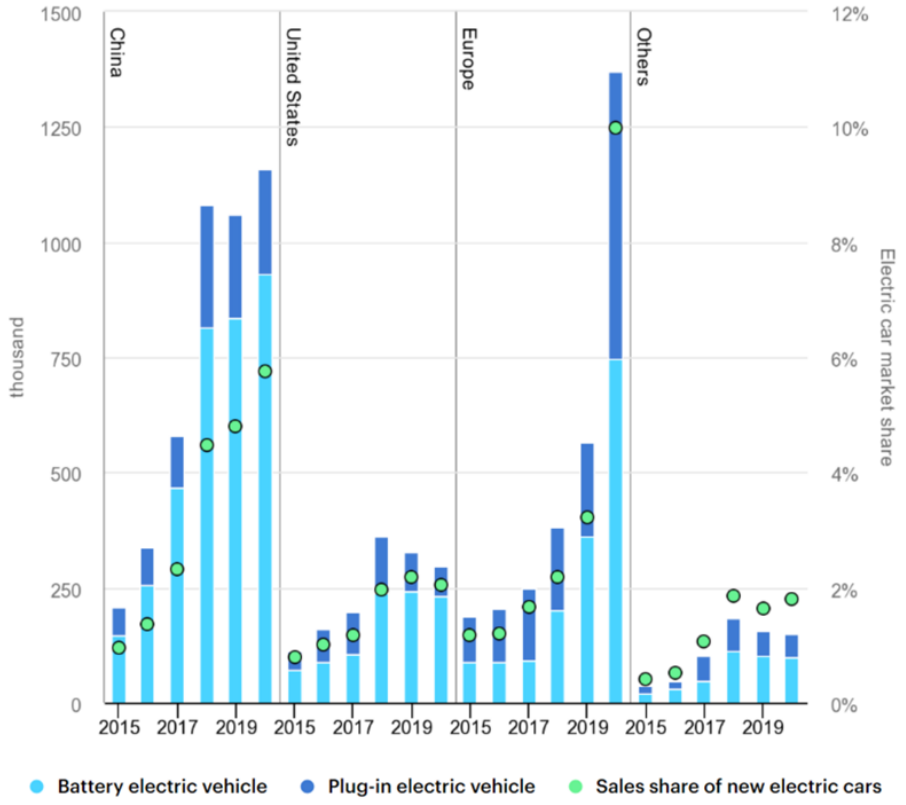


Figure 1.1: Global Electric Car Registrations and Market Share 2015-2020 [16]

To further promote EV, more than 20 countries have electrification targets or ICE bans for cars, and 8 countries plus the European Union have announced net-zero pledges[16]. Under the policy of different countries, the

electric car share will have significant growth in the future. International energy agency predicts that the electric car share will be up to 14% in 2030 [15].

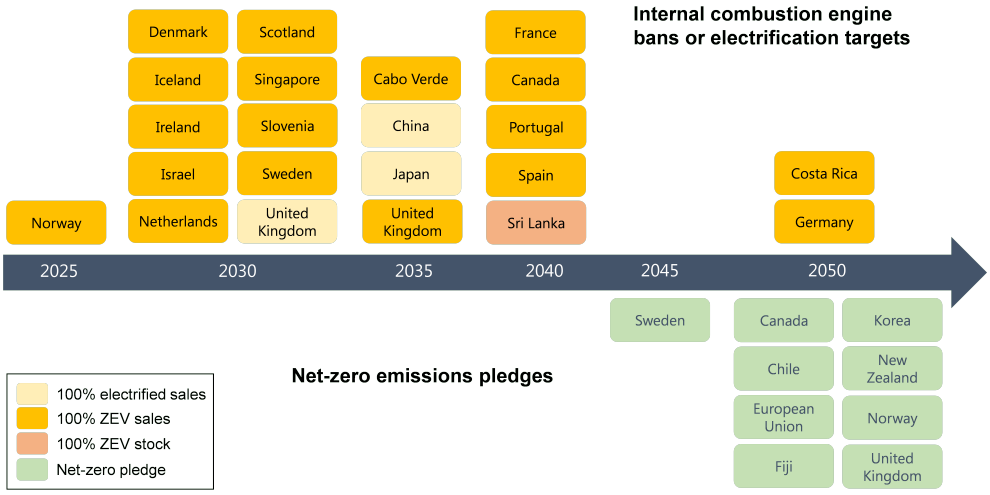


Figure 1.2: Electrification targets, ICE bans and net-zero pledges of different countries[16]

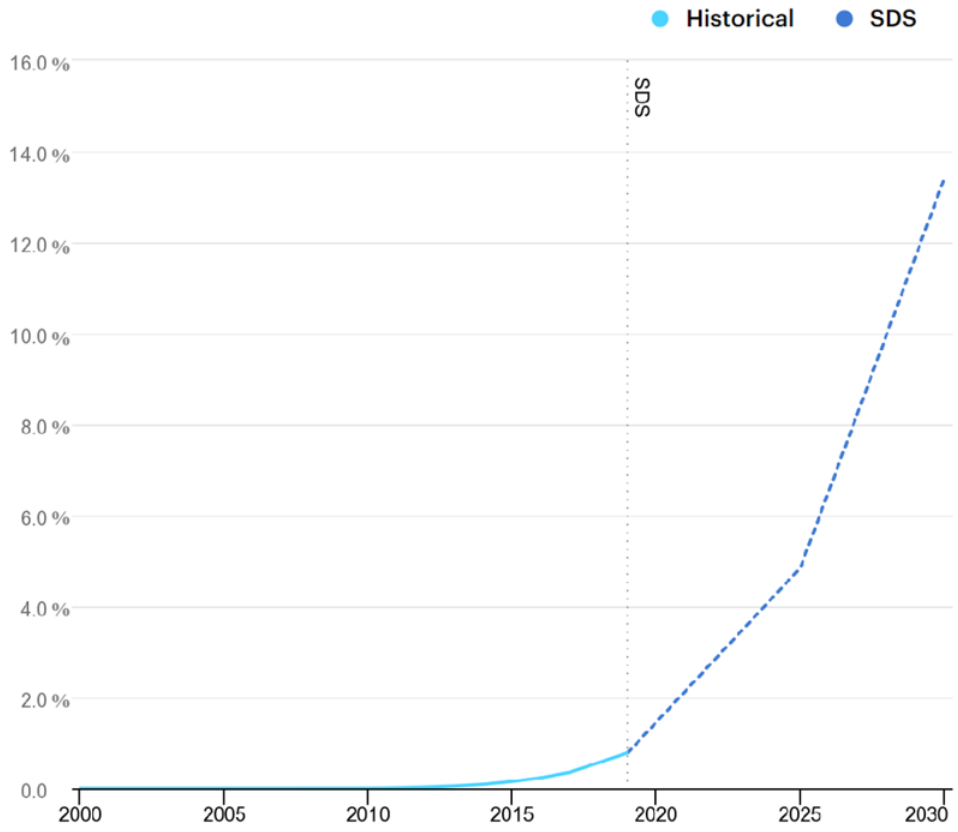


Figure 1.3: Electric car share in the Sustainable Development Scenario(SDS), 2000-2030[15]

Charging problems and range anxiety have always been the main barriers of EV promotion. More and more manufacturers develop their own electric

cars, about 370 electric vehicle models were released globally in 2020[16]. The average range of the new BEV has steadily increased. In 2020, the weighted average range of new battery electric vehicles was about 350 km [16]. Charging problem that a lack of charging infrastructure and slow charging speed is becoming the main concern for EV customers [12].

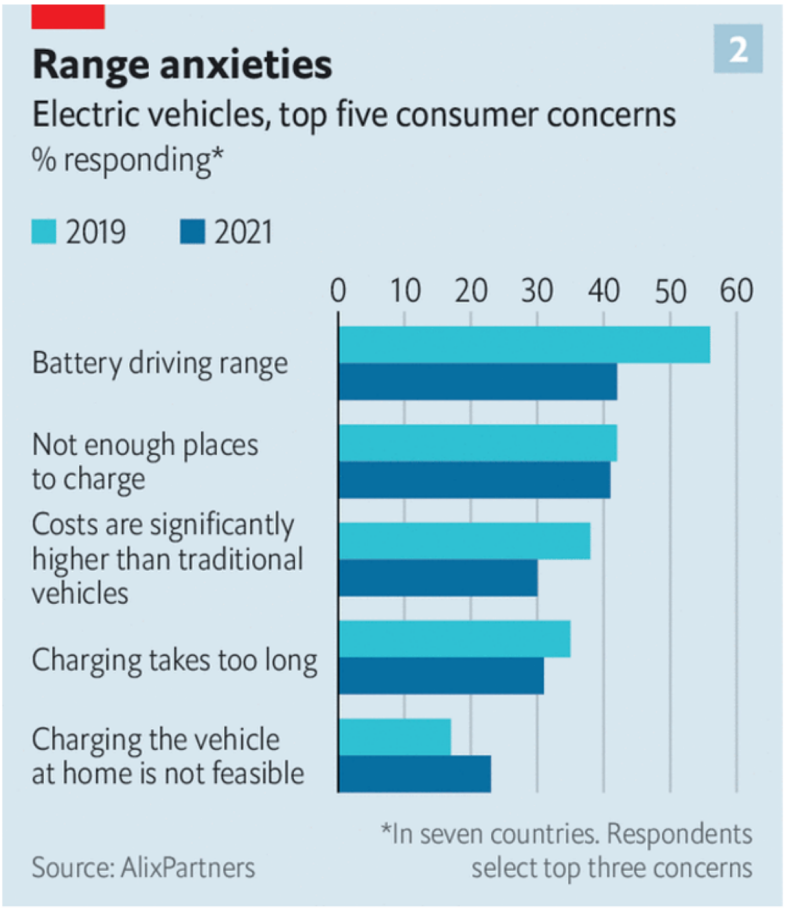


Figure 1.4: Top Five Consumer Concerns [12]

There are three main charging technique, namely battery swapping, conductive charging and inductive charging.

Battery swapping technique can quickly recharge EV by replacing the battery. However, battery swapping technique is not as attractive as the other two techniques because of the problems such as lack of standard technical standards and expensive construction cost. Inductive charging generates AC current in the induction coil in EV by generating a changing magnetic field in the charging station, and convert it into Direct current (DC) by a rectifier to charge the battery.

The conductive charging can be classified into on-board charging and off-board charging. On-board charging is also called AC charging.

Off-board charging is also called fast DC charging, Because bulky converter can be installed in charging station, which allows large charging power.

Conductive charging is the most widely adopted charging solution. AC charging, which provides lower power, is usually installed in private place

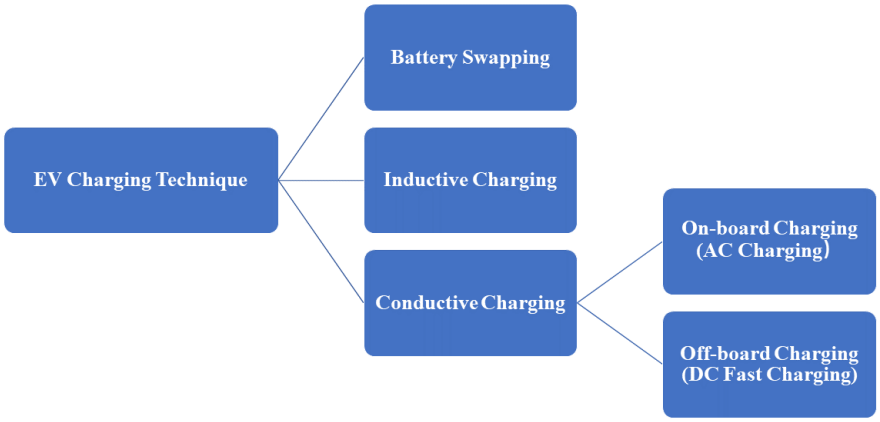


Figure 1.5: Classification of charging techniques

such as home and workplace, because cars can be parked for long periods of time and cost less. On the other hand, DC fast charging can effectively solve range and charging queuing problems, is more suitable for time-constrained situations, such as highways and public quick charging.

In the Sustainable Development Scenario, there are more than 20 million public slow chargers and almost 4 million public fast chargers installed by 2030 corresponding to installed capacities of 150GW and 360 GW respectively[16].

The DC Fast charging technology is believed to address the charging concerns and it is developing towards ultra-fast charging, which is capable of providing 150kW or more, expecting to charge EV battery to 80% within 10 minutes [40] [45]. To charge a mainstream (e.g. Tesla Model S [10]) 103kWh battery capacity to 80% in 10 minutes, the required fast charging power is 494.4 kW. The development of fast charging technology will therefore be of increasing importance to the EV development.

1.2 OBJECTIVE

The project focuses on using triangular current shaping method to reduce THD and realizing power factor correction in first stage AC-DC converter and implementing partial power processing technique in second stage DC-DC converter.

- One of the main challenge of the project is to deal with triangular current shaping method with buck PFC circuit. ;
- Another challenge is to reduce the influence of partial power processing used in DC-DC converter on the operation of AC-DC converter.
- One of innovation of this project is to implement partial power processing technique together with multiple pulse rectifier in EV DC charger .

- Another innovation is that the system is designed to apply in multiple application senarios.

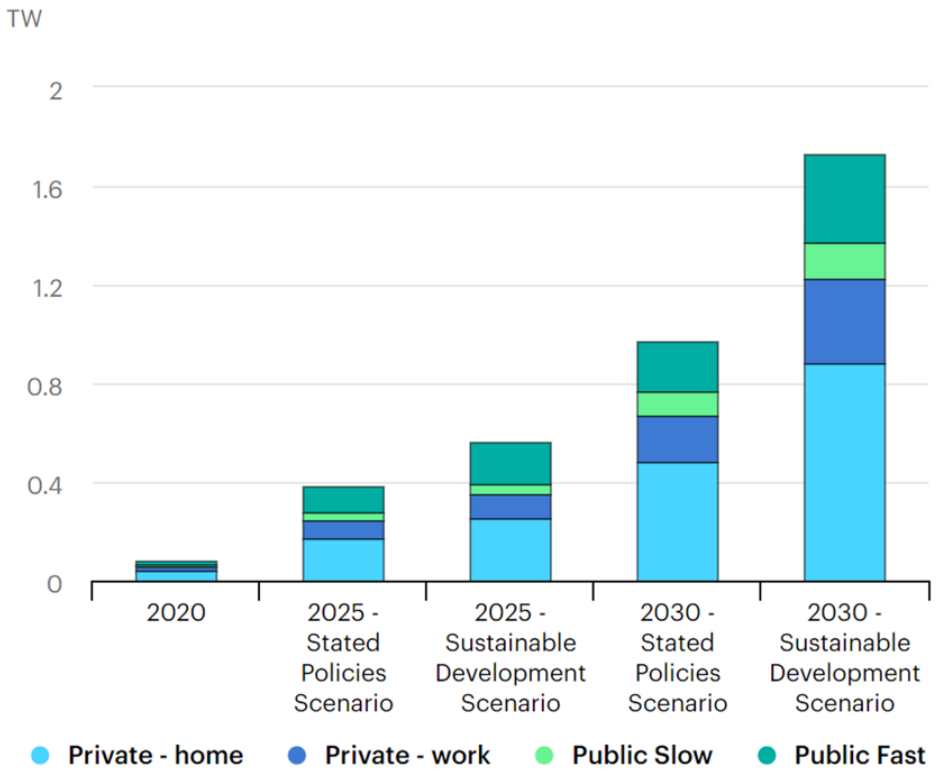


Figure 1.6: Cumulative installed charging power capacity for electric light-duty vehicles chargers by scenario, 2020-2030[16]

The goal of this thesis project is to design a 12-pulse rectifier as front-end stage converter for EV fast charging with triangular current sharping method for harmonic reduction, and apply partial power processing technique in EV fast charging to improve system efficiency, fulfilling low current harmonics, galvanic isolation, large output voltage range and high efficiency. Thus, there are some small objectives needed to complete step by step, which is listed below:

- Introduce EV market and charging technique of EV;
- Determine the specifications of the project converter according to policy and the state of art of technique.
- Design the 12-pulse rectifier with harmonic reduction method to have low current harmonics
- Extend the output range and improve efficiency by implementing partial power processing technique on full bridge DC-DC converter topology.
- Investigate Mathematical model of the converter system and optimize the efficiency with loss modeling.

- Verify the triangular current power factor correction method.
- Using SPICE to simulate the converter system and compare the results of prototype converter with simulation results.
- Doing experiment to verify that the control strategy in buck circuit is able to make inductor current keep track of the triangular current reference and the input filter can filter out the discontinuous current from buck.

1.3 OUTLINE OF THE THESIS

Chapter 1 investigates the motivation and the objectives of this project, including the background of the EV and DC fast charging technique.

Chapter 2 introduces the state-of-art technology of the DC fast charging and two special research topics which are the triangular current sharping method for harmonic reduction and partial power processing technique.

The design of AC-DC stage converter and DC-DC stage converter are described in detail in Chapter 3 and Chapter 4.

The Mathematical loss modeling of the converter system and the loss modeling results of two charging modes are presented in Chapter 5.

Chapter 6 builds up the simulation of the proposed system. Verify the triangular current power factor correction method and study the loss distribution. Simulation and loss modeling are done both in two modes.

Chapter 7 sets up the experiment of AC-DC stage converter. Experimental results are analyzed and further improvement of the experiment are introduced.

Finally, the project and the developing direction of this project are summarized in Chapter 8.

2 LITERATURE REVIEW ON CHARGING TOPOLOGIES, STANDARDS AND TECHNIQUES

2.1 DC FAST CHARGING CONVERTER

DC fast charging systems (DCFCs) convert the AC voltage from the power grid to the DC voltage required for charging the EV batteries. There are several requirements from the application point of view, i.e., galvanic isolation for safety considerations, good power quality for the power grid and wide output voltage range for the flexible EV batteries available on the market. Besides, great efforts have been made to improve the converter efficiency and power density.

DCFCs can be designed as a single or a two-stage converter [41]. The two-stage converter can be classified as low frequency isolation-based and high frequency isolation-based, as shown in Fig. 2.1. For galvanic isolation, isolated transformer is essential, either implemented in AC-DC or DC-DC converter stage.

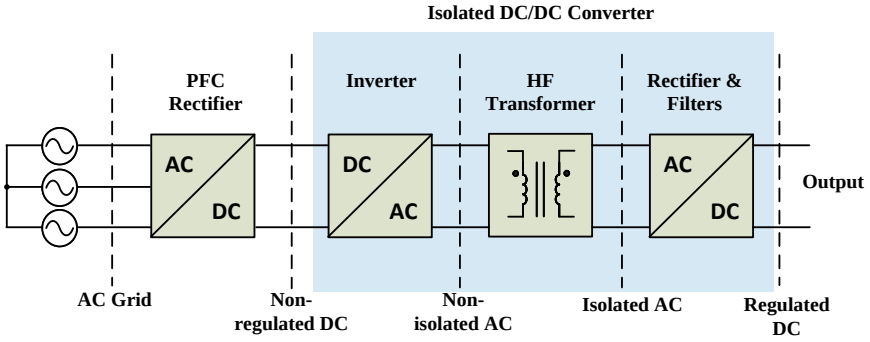
For the two-stage charger, it is an AC-DC PFC converter followed by either a non-isolated or an isolated DC-DC converter. The role of the front-end AC-DC converter is to convert AC mains voltage into DC voltage and also act as input current filter for PFC and harmonic reduction. Power factor and Total harmonic distortion (THD) are the major factors that influence the selection of a particular PFC rectifier topology. Boost type topology and their variants are widely used for PFC rectification purposes[24]. The main function of the second-stage DC-DC converter is to offer regulated voltage and current to better charge the HV battery.

2.1.1 Frond-end AC/DC Converter

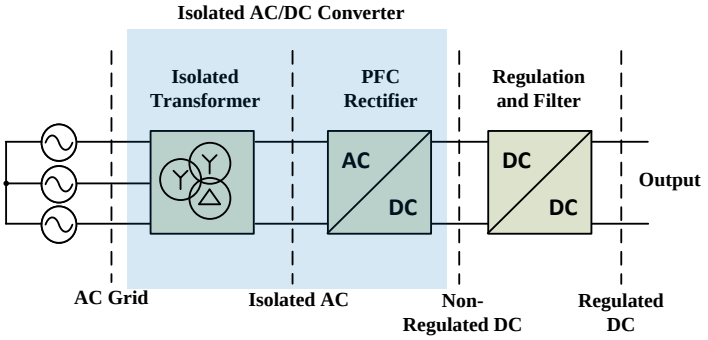
The front-end AC/DC rectifier converter of DCFCs is connected to three-phase AC low-voltage (LV) or medium-voltage (MV) grid depending on the converter topology. The high power AC/DC converters are usually low THD, high Power factor, less numbers of components and high power density. Based on components type, the rectifier is classified into active rectifier and passive rectifier.

The most popular topologies for active rectifiers are two-stage Voltage Source Converters (VSCs, see Fig. 2.2 a) and three-level converters, such as T-type converters (see Fig. 2.2 b) and Neutral Point Clamped Converters (NPCs, see Fig. 2.2 c)[33].

Passive rectifier uses diodes to rectify the AC currents, and a bulky input filter to reduce the THD. For instance A 3-phase system requires six diodes to make up the passive rectifier. This design is commonly referred to as a 6-pulse rectifier because DC side voltage has six pulses. 6-pulse rectifier

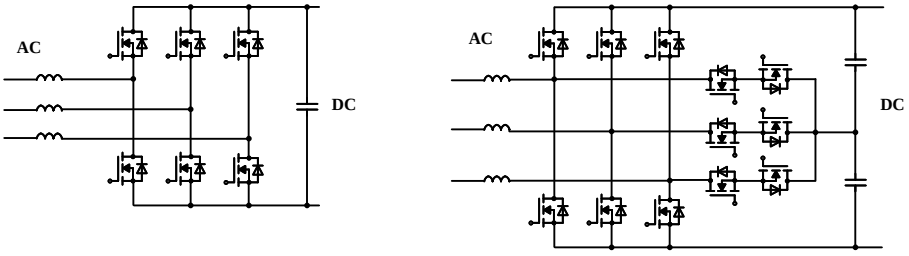


(a) Two-stage High Frequency Isolated Structure



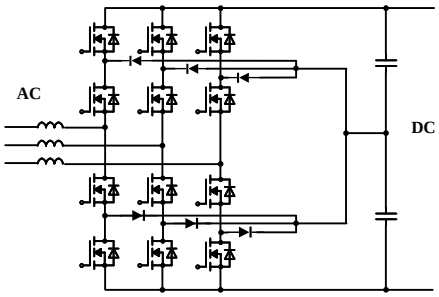
(a) Two-stage Low Frequency Isolated Structure

Figure 2.1: Two-stage Isolation-based Structure [2]

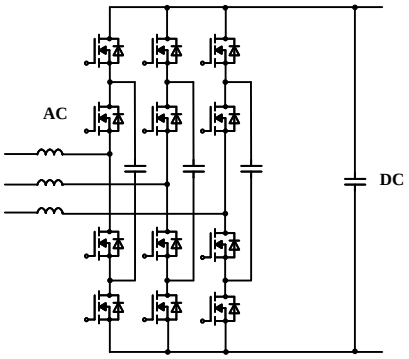


(a) Two-level Voltage Source Converter

(b) Three-level T-type Converter



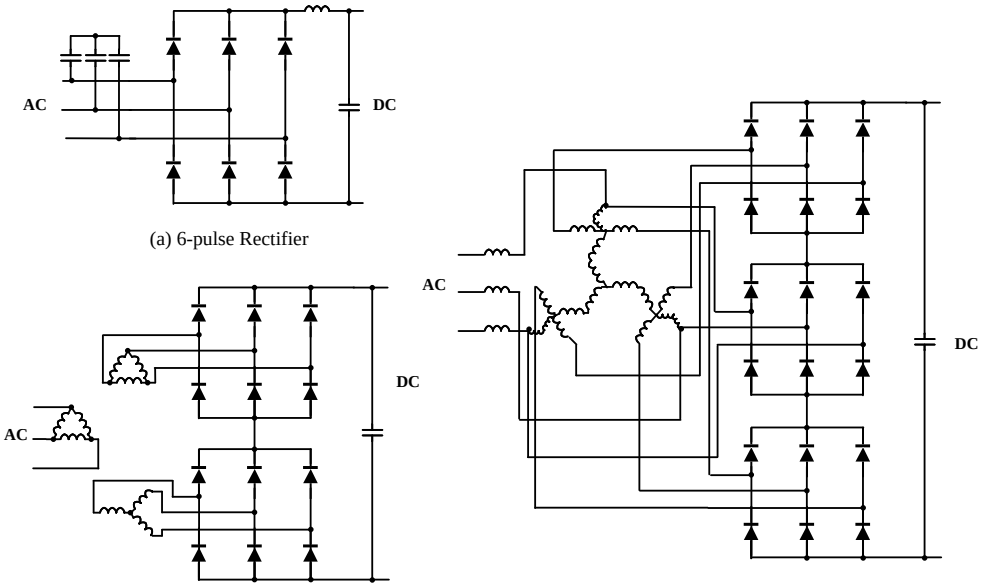
(c) Three-level Neutral Point Clamped Converter



(d) Three-level Floating Capacitor Converter

Figure 2.2: Block schemes of active AC-DC converter topologies: (a) two-stage Voltage Source Converter (VSC); (b) Three-level T-type Converter; (c) Neutral Point Clamped Converter (NPC); (d) Three-level Floating Capacitor Converter [33]

usually needs large input filter to realize low THD. One approach to reduce THD in passive converters is to use 12, 18, or even 24 pulse rectifiers. A 12-pulse rectifier uses two 6-pulse rectifiers (12 diodes) with a phase-shift transformer creating a 30 degree phase shift between the two current waveforms, which eliminates the 5th and 7th harmonics. 6-pulse rectifier, 12-pulse rectifier and 18-pulse rectifier are shown in Fig. 2.3.



(a) 6-pulse Rectifier

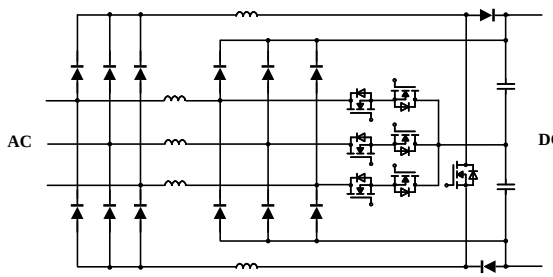
(b) 12-pulse Rectifier

(c) 18-pulse Rectifier

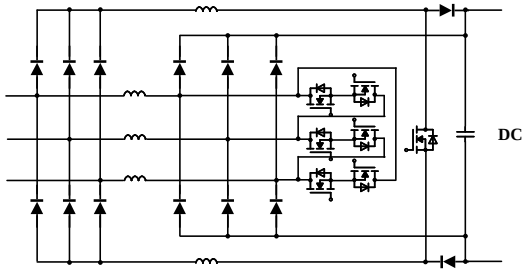
Figure 2.3: Block schemes of passive AC/DC converter topologies: (a) 6-pulse rectifier; (b) 12-pulse rectifier; (c) 18-pulse rectifier

The Multi-pulse rectifier (MPR) technology is widely used in high power application due to its simple structure, high robustness, and relatively low harmonic distortion [28][32]. Compared with the active rectifier, Multi-pulse rectifier is simpler, more reliable but bulkier [11]. However, in high power applications, the connection to the medium voltage (MV) distribution grid becomes important due to the power availability issues in the low voltage (LV) distribution grids. Therefore, a DCFC may naturally require a line frequency transformer to enable this MV grid connection, and the selection of the MPR technology can become a natural choice.

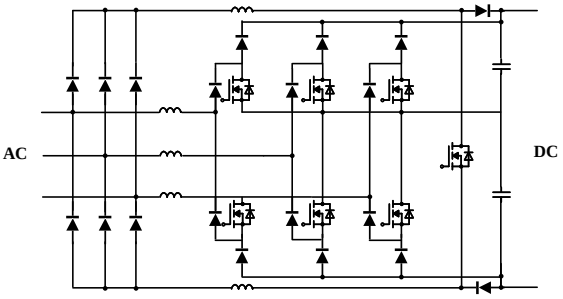
Hybrid rectifiers usually denote the parallel connection of a passive and active rectifier. Hybrid rectifiers take advantage of the benefits of passive rectifiers and active rectifiers. In general, passive rectifiers are more reliable and efficient, which are designed to process more system power. On the other hand, active rectifiers can control the input current to be nearly sinusoidal and are designed to process less system power. Therefore, the hybrid rectifiers are usually cheaper, more robust and efficient while providing low current THD and high power factor. Fig. 2.4 shows three hybrid rectifiers which can adjust line current and control DC bus voltage.



(a) Two-level Delta-switch Rectifier

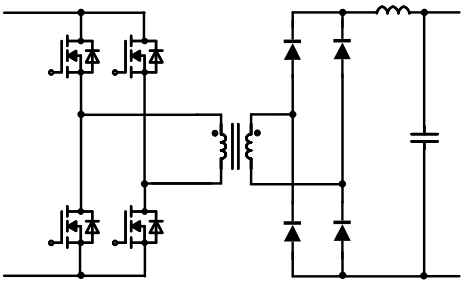


(b) Three-level T-type Rectifier

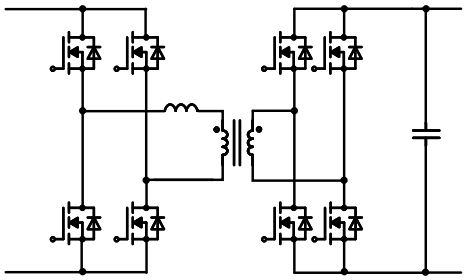


(c) Three-level VIENNA Rectifier

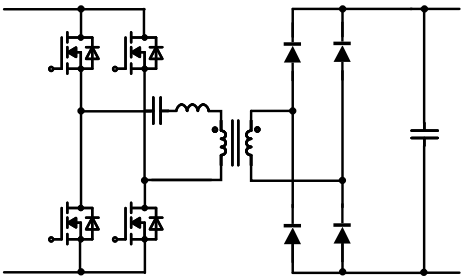
Figure 2.4: Hybrid rectifier systems based on (a) two-stage unidirectional delta-switch rectifier, (b) three-level T-type rectifier, (c) three-level VIENNA six-switch rectifier, [37]



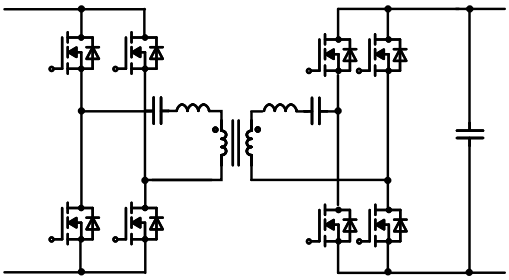
(a) Full Bridge Rectifier



(b) DAB Rectifier

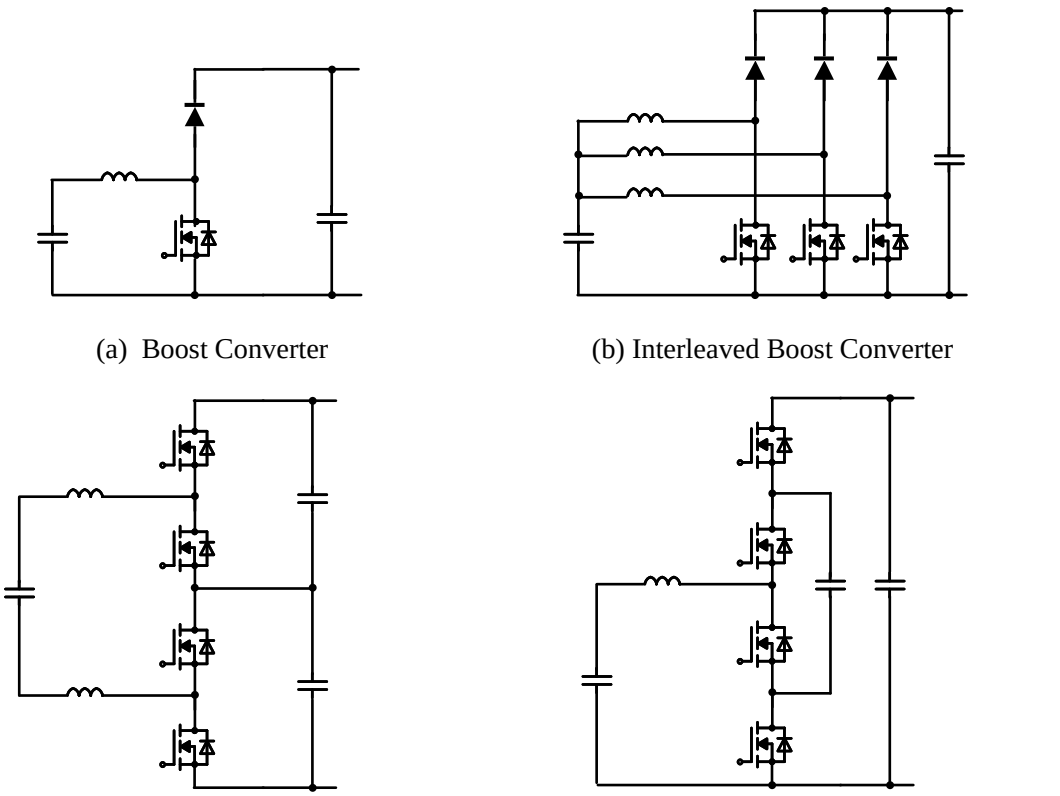


(c) LLC Rectifier



(c) DAB-CLLC Rectifier

Figure 2.5: Isolated DC-DC Converters: (a) Full Bridge Converter, (b) Dual Active Bridge (DAB) Converter, (c) LLC Converter, (d) DAB-CLLC Converter [42]



(a) Boost Converter

(b) Interleaved Boost Converter

(c) Bidirectional Three-level Boost Converter

(d) Three-level Flying Capacitor Converter

Figure 2.6: Non-isolated DC-DC Converters: (a) Boost Converter, (b) Interleaved Boost Converter, (c) Bidirectional Three-level Boost Converter, (d) Three-level Flying Capacitor Converter [42]

Isolated DC-DC Converters				
Property	Full bridge	DAB	LLC	DAB-CLLC
Reliability	H	M	M	L
Complexity	L	L	M	H
Voltage Range	M	H	H	H
Power Flow	uni	bi	uni	bi
Price	L	M	M	H
Non-isolated DC-DC Converters				
Property	Boost	Interleaved	3-level	Flying Capacitor
Complexity	L	M	H	H
Power capability	L	H	M	M
Voltage range	L	L	H	H
Price	L	M	H	H
* H-High; M-Middle; L-Low				

Table 2.1: Comparison of Different Isolated and Non-isolated DC-DC Converter

2.1.2 Back-end DC/DC Converter

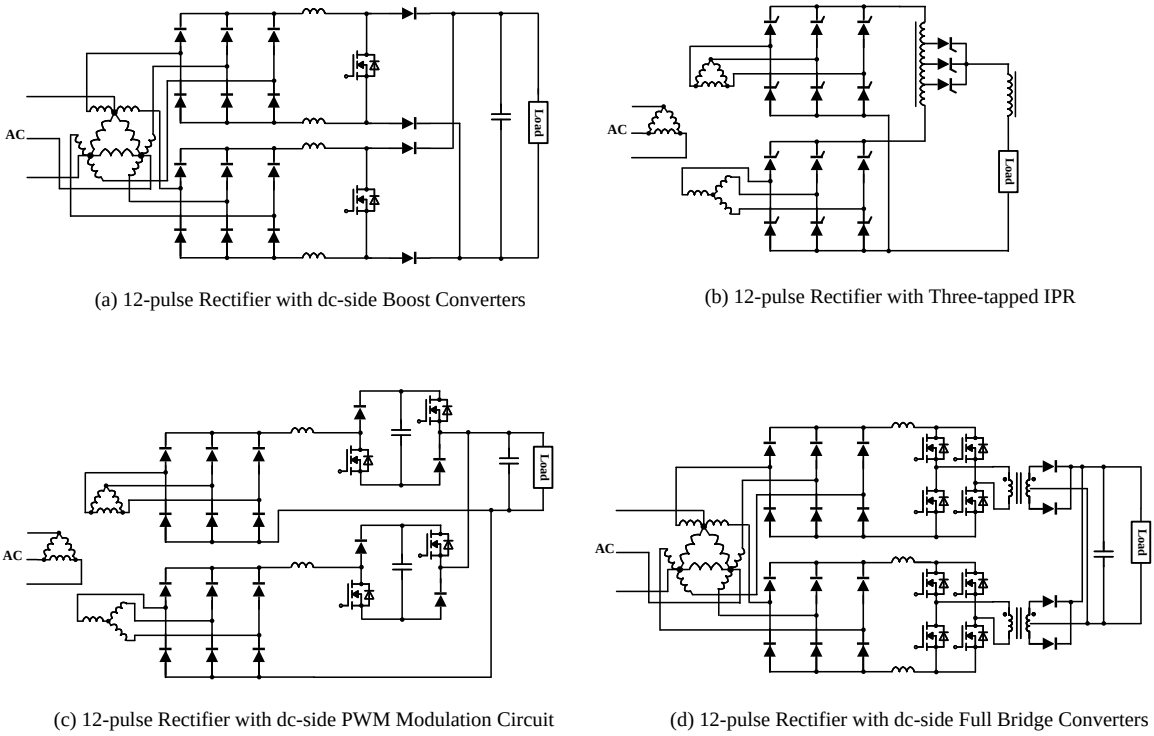
The back-end DC-DC converter provides the regulated voltage for the battery of the EVs and can also provide an isolated interface when there is absent galvanic isolation in the former AC-DC converter. The DC-DC converter can be classified into isolated and non-isolated topologies. Isolated DC-DC converters used in DCFC system are usually full bridge converter, dual active bridge (DAB) converter, LLC converter and DAB-CLLC converter, as shown in Fig. 2.5. Alternatively, Non-isolated DC-DC converter are interleaved boost converter, bidirectional three-level boost converter and flying capacitor converter, as shown in Fig. 2.6

The comparison of different DC-DC converters are shown in Table.2.1. Full bridge converter is usually more reliable than DAB and LLC converter because control and topology of full bridge converter are most simple. Compared to Boost circuits, 3-level converter and flying capacitor converter enhance the power capability and increase the voltage level, while the number of components and cost are increased.

2.2 HARMONIC REDUCTION METHOD FOR 12-PULSE RECTIFIER

Among the known MPRs, 12-pulse rectifier is the most widely used because of its economical and efficiency advantages [29]. 12-pulse rectifier can achieve the harmonic reduction because of its inherent nature, but current harmonics can not meet the harmonic requirements of the design without additional harmonic reduction means. Many harmonic reduction methods for 12-pulse rectifier have been studied, which toplogies are shown in Fig. 2.7 together with their associated topologies.

One of the most effective harmonic reduction methods for the 12-pulse converter is to shape the output current of two diode bridge to be close to a triangular shape by usage of auxiliary non-isolated DC-DC converter, which mostly implements a boost type circuit, as shown in Fig. 2.7 (a). [11]. This kind of auxiliary circuit can be classified as current injection with interphase reactor (IPR), as shown in Fig. 2.7 (b), and separate modulation method [11]. Separate modulation method is simpler than the former one in terms of both the control and circuit realizations. In [7], the boost type separate modulation was implemented in a 12-pulse rectifier with the close to triangular current shaping method. A THDi of 3% was achieved but at the cost of considerable magnetic size. Another boost type 12-pulse rectifier with auto-transformer, as show in Fig. 2.7 (c), minimized the equivalent kVA rating of the transformer and improved the power density, but consequently resulted in a higher THD of 4.45%, which though is still in compliance with the IEEE 519 standard [26]. Instead of the convention boost type circuit used in the literature, [8] proposed a full bridge type topology to meet isolation requirement, as show in Fig. 2.7 (d), while the losses increased significantly due to the larger part count of magnetic and semiconductor components.



(a) 12-pulse Rectifier with dc-side Boost Converters

(b) 12-pulse Rectifier with Three-tapped IPR

(c) 12-pulse Rectifier with dc-side PWM Modulation Circuit

(d) 12-pulse Rectifier with dc-side Full Bridge Converters

Figure 2.7: Harmonic Reduction Circuits in 12-pulse rectifier [11]

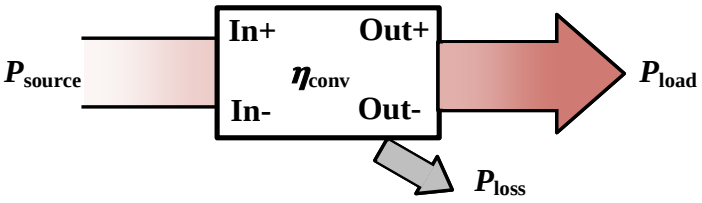
2.3 PARTIAL POWER PROCESSING

Partial power processing technology has recently attracted a lot of attention because of its advantages and is considered as an attractive solution to present and upcoming applications in the future [1]. Majority studies focused on the DC applications, such as, small wind turbine system [3], photovoltaic system [47] [6], energy storage system [19] and EV fast charging [21] [23].

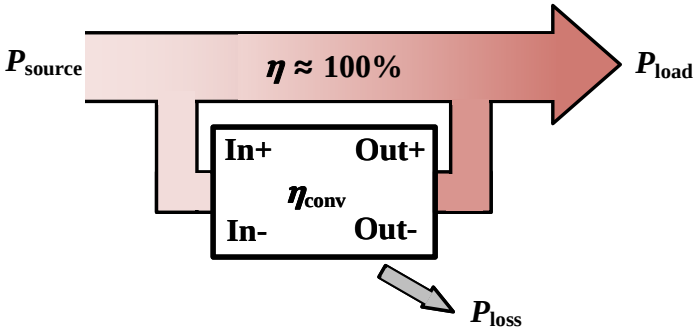
Partial power processing (PPP) technique, as literally, is that a partial power processing converter processes only a portion of the power from the input source to the load, resulting in a reduction in losses and thus an increase in system efficiency. The concept of partial power processing is illustrated in Fig. 2.8. Fig. 2.8 (a) shows the power flow diagram of the full power processing (FPP) converter where total system power is processed by the converter. Fig. 2.8 (b) shows the power flow diagram of PPP converter. By changing the topology of FPP converter, part of the total power is directly output to the load with an efficiency approximate to 100%, and the rest of the power is processed by the converter. The efficiency of the converter itself does not change, but the efficiency of the system as a whole increases because of the reduction in the processed power by the converter. The efficiency of FPP and PPP converter system can be expressed as (2.1) and (2.2).

$$\eta_{\text{system}} = \frac{P_{\text{load}}}{P_{\text{source}}} = \eta_{\text{conv}} = \frac{P_{\text{out}}}{\text{in}} \tag{2.1}$$

$$\eta_{\text{system}} = 1 - K_{\text{pr}} \cdot (1 - \eta_{\text{conv}}) \tag{2.2}$$



(a) Power flow of FPP Converter System



(b) Power flow of PPP Converter System

Figure 2.8: Power flow diagram. (a) FPP converter system; (b) PPP converter system

where K_{pr} is the processed power ratio of the converter, η_{system} and η_{conv} are the efficiency of the whole system and converter, respectively. Processed power ratio K_{pr} is a function of voltage gain ($\frac{V_{load}}{V_{source}}$) and is different from different topologies of partial power processing.

PPP strategies can be classified as three main types [1], as Fig. 2.9:

- Differential Power Converters (DPC).
- Parital Power Converters (PPC).
- Mixed strategies.

DPC is suitable to the applications of multiple elements in series on the bus, aimed at correcting current imbalances. According to power flow direction, DPC can be classified as two groups, Element to Element and Bus to Element. Compared to DPC, PPC is to control the power flow, current and voltage level. Since fast charging system in this thesis is one element to one element, PPC is selected as the PPP strategy of the DCFC system.

According to the galvanic isolation of basic converter topology of PPC, PPC can be classified as isolated converter and non-isolated converter. Different connection methods of isolated PPC are shown in Fig. 2.10. Fig.2.10 (a) presents an Input-parallel-output-series (IPOS) step-up topology, which means the input of converter is parallel connected with input source and output of converter is series connected with load. Polarity of the input and output of converter decide whether the output voltage level is step-up or step-down. Phase shift full bridge converter, for example, is presented in Fig.2.10 (a) as the isolated basic converter of partial power processing topol-

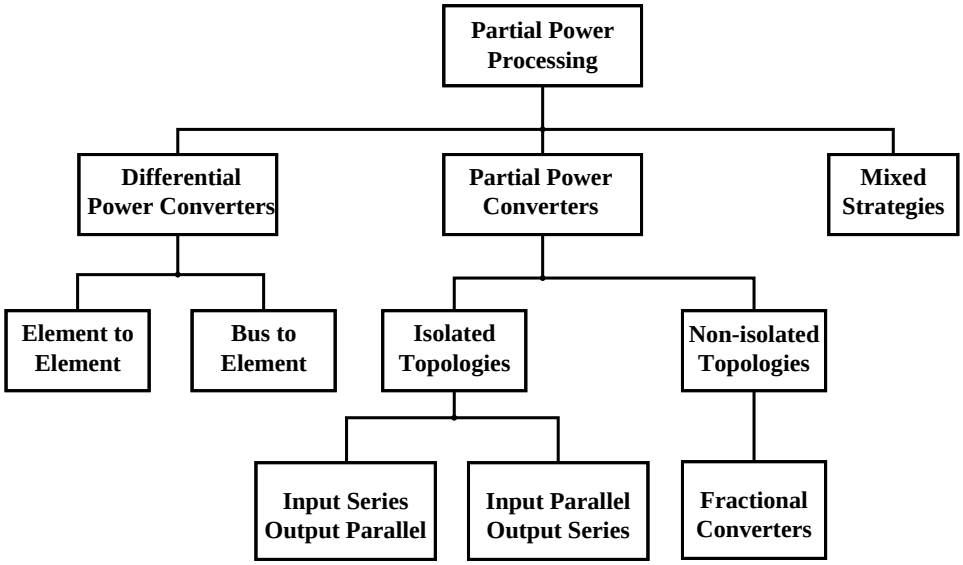


Figure 2.9: PPP classification

ogy. Other common isolated converters of partial power processing are dual active bridge (DAB) and Flyback.

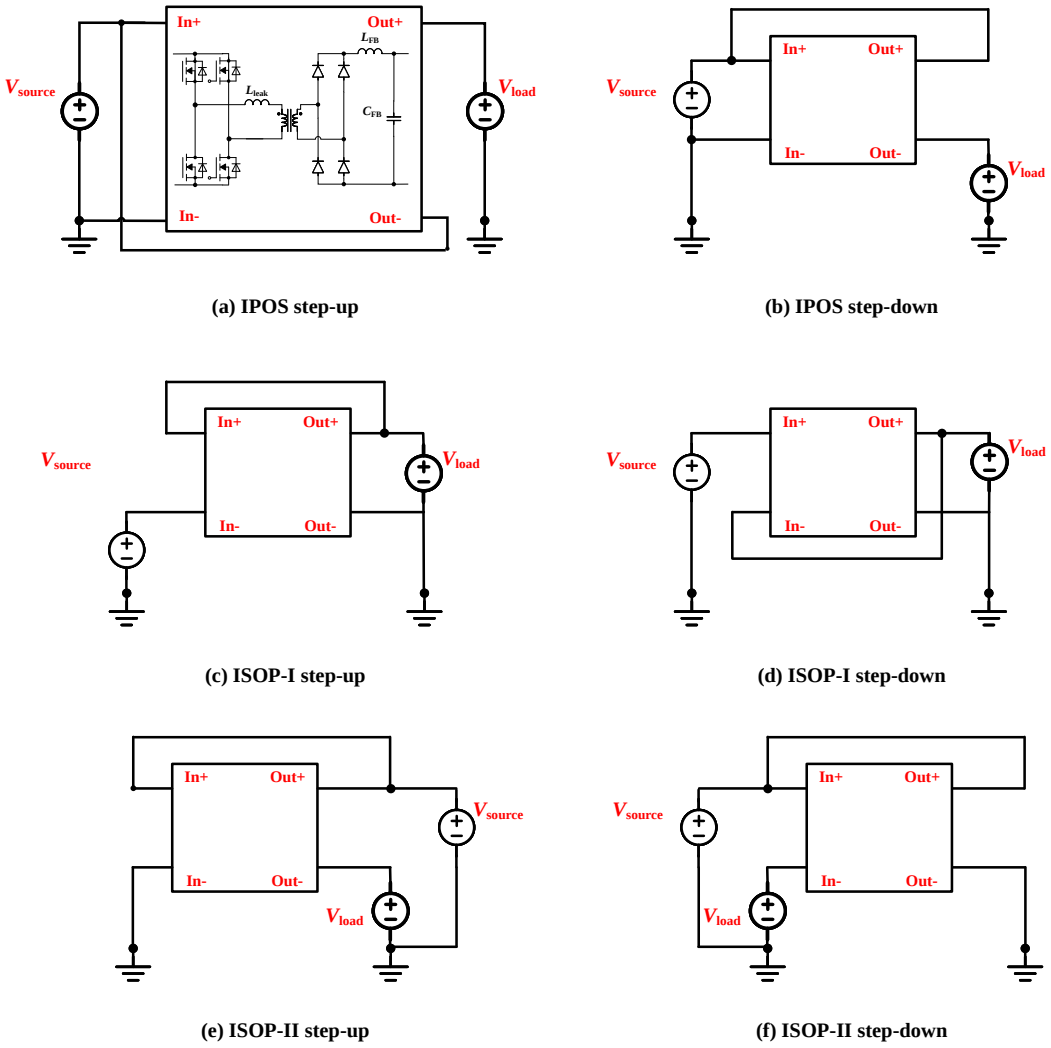
Different connection methods of non-isolated PPC, named fraction converters, are shown in Fig. 2.11. Noted that, with different connection methods, the processed power ratio K_{pr} is a different function of voltage gain and converter efficiency.

For EV fast charging application, many studies implemented PPP in DC-DC stage and shows an increase of the system efficiency, shown in Tabel. 2.2. Isolated full bridge converter as based converter of partial power processing for EV charging more advantageous and studied. Compared with non-isolated based topologies, isolated based topologies have more PPP connection choices, wider voltage range and higher reliability. Another common isolated based topology, flyback, is not suitable for high power application because the transformer need to store energy during the conversion. Therefore, flyback are used in the application of Photovoltaic and Energy storing system.

Considering that the EV fast charging is an high power application and the advantages of isolated based topologies, phase shift full bridge converter is chosen as the based topology of partial power processing technique. Therefore, partial power processing phase shift full bridge is selectedto be the DC/DC converter in the thesis.

PPP connection method	K_{pr}	Eff.η	Based Topology
IPOS-II step-down [21]	33%	-	Full Bridge
IPOS step-up [20]	56.7%	98.55%	Full Bridge
ISOP step-down [35]	35%	98%	Full Bridge
FCC step-down [23]	70%	98%	Full Bridge

Table 2.2: PPP in EV fast charging



(a) IPOS step-up

(b) IPOS step-down

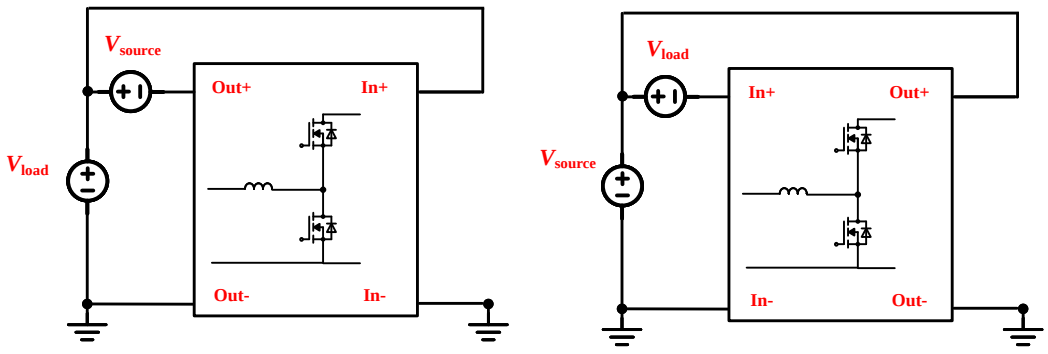
(c) ISOP-I step-up

(d) ISOP-I step-down

(e) ISOP-II step-up

(f) ISOP-II step-down

Figure 2.10: Different PPP connection of isolated PPC



(a) Fractional Converters step-up

(b) Fractional Converters step-down

Figure 2.11: Different PPP connection of Non-isolated PPC (a) FCC step-up, (b) FCC step-down

2.4 DC FAST CHARGING STANDARD

2.4.1 Power level of Fast Charging

The power of DC fast charging has been boosted rapidly. CHAdeMO, GB/T and CCS are the mainstream standard used in the world. China and Japan are developing a new version of GB/T fast charging standard (Being referred to as Chaoji), Aiming at harmonizing all the standards. Table.2.3 shows the maximum power of latest version of charging standard.

Standard	Version	Maximum Output Power(kW)
CHAdeMO[2]	2.0	400
GB/T[2]	27930	185
Chaoji[2]	1&2	900
CCS[2]	HPC350	350
Tesla[39]	V3	250

Table 2.3: Maximum Power of Mainstream DC fast Charging Standard

2.4.2 Voltage Level of Fast Charging

The conventional voltage level is 400 V. However, with the increase need of high power charging, 400 V voltage level structure limits the charging power. Thus, 800 V voltage level structure is proposed and is regarded as next generation high voltage level. To reduce range anxiety, many manufacturers are developing 800 V based commercial passenger cars that support ultra-high power fast charging. With the launch of the Taycan Turbo S, porsche's first passenger EV to support an 800 V voltage platform, many 800 V passenger EV of other company have appeared on the market, as shown in Table.2.4. To have fast charging speed, higher voltage levels such as 1200 V and 1600 V would be proposed in the foreseeable future.

EV model	Battery Capacity (kWh)	Battery voltage (V)	Fast charging power (kW)
Porsche Taycan Turbo S[14]	93.4	800	270
KIA EV6[25]	58	800	220
Cadillac lyriq[5]	100	800	190
BYD Dophin[22]	44.9	800	60

Table 2.4: Different Passenger EV of 800 V Charging Coltage

2.4.3 Power Factor and Harmonics Requirement

For EV charging, current harmonic distortion is a considerable problem due to the the switching actions of the power semiconductors in the AC-DC stage. Current harmonic distortion could bring in extra electricity bills and energy waste. Besides, introduction of severe harmonic distortion into the AC grid causes a negative impact on other electrical equipment, such as leading to

degradation and causing unbalance operation. For the safe operation of the equipment in grid, standards such as IEC 61000-3-12 and IEEE 519-2014 were established to regulate the harmonics introduced into the grid by the electrical equipment. This thesis is designed based on the standard IEEE 519-2014. Current harmonic limitation of Standard IEEE 519-2014 is shown in Fig. 2.12.

Individual harmonic order (odd harmonics)						
I_{SC}/I_L	<11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Figure 2.12: Current harmonic limitation of IEEE Standard 519 – 2014 [18]

where I_L—Max. demand load current and I_{SC}—short circuit current. TDD—total demand distortion, harmonic current distortion in % of maximum demand load current. Even harmonics are limited to 25% of odd harmonic limits above.

Current THD of DC fast charging station product is usually set at no more than 5% THD. The power, THD, power factor (PF) and efficiency of products on the market are shown in Table.2.5.

Brand	Power(kW)	THD(%)	PF	Efficiency(%)
Nici[31]	360	< 5	0.99	95
Blink[4]	175	< 5	0.99	96
SETEC Power[34]	300	< 5	0.99	-

Table 2.5: Power factor and THD of DC fast charging station product and literature

2.5 PROPOSED TOPOLOGY

In this thesis, a two-stage converter for DC fast battery charging application is designed and studied. The front-end converter is a buck type 12-pulse converter with triangular current shaping method for harmonic reduction and power factor correction. The back-end converter is a full bridge converter with partial power processing technique.

Front-end buck type 12-pulse converter takes advantage of the high reliability and simplicity of the MPR, while also achieving low THD_i and high power factor on the AC side. For the application at hand, the selected buck-type PFC auxiliary circuit provides unique advantages over the boost type circuit previously used in the literature [36], namely: the natural current source functionality allows a direct connection to the battery, leading to much less DC filtering requirement; the solution can potentially enable direct start-up, while allowing for dynamic current limitation; and a wider output voltage control range, while maintaining PFC capability at the input.

These advantages bring in the improvement of input power quality and efficiency of the system. Therefore, the buck-type 12-pulse converter featuring triangular current shaping is used for the 100 kW DC fast charger design. Back-end partial power processing phase shift full bridge converter takes advantage of the high power handing capability of full bridge topology and simplicity of phase shift control, while also stepping up the voltage level for batteries rated above 800V. With partial power processing technique, the power processed by the full bridge converter is reduced, thus, reducing the system losses.

Fig. 2.13 shows the proposed topology of two-stage converter for the EV DC fast battery charging. A phase shift transformer with $Y/Y/\Delta$ connection provides galvanic isolation and the necessary 30 degree phase shift between each phase voltages delivered for the upper and lower diode bridges. An AC filter is necessary for grid-compliance, and two buck type DC-DC converter circuits use the current and voltage control to separately control the output current of the two diode bridges to have a close to triangular shape which will provide the desired PFC capability and also to control the battery charging profile, e.g., the constant current (CC) and constant voltage (CV) battery charging. A phase shift full bridge DC/DC convert is connected after 12-pulse AC/DC converter with Input Parallel Output Series (IPOS) partial power processing connection. Phase shift control method can realize Zero Voltage Switch (ZVS) to reduce losses.

This DCFC system is designed for multiple application scenarios. When the two mode switches switch to M1, partial power processing full bridge converter is excluded from the DCFC system. To charge the battery rated at less than 800V, the system is more efficient without the back-end DC/DC converter. When the two switches switch to M2, the DCFC system are 2-stage system, which can provide high charging voltage. In Mode 2, the system is designed for 1200-1600 V battery charging.

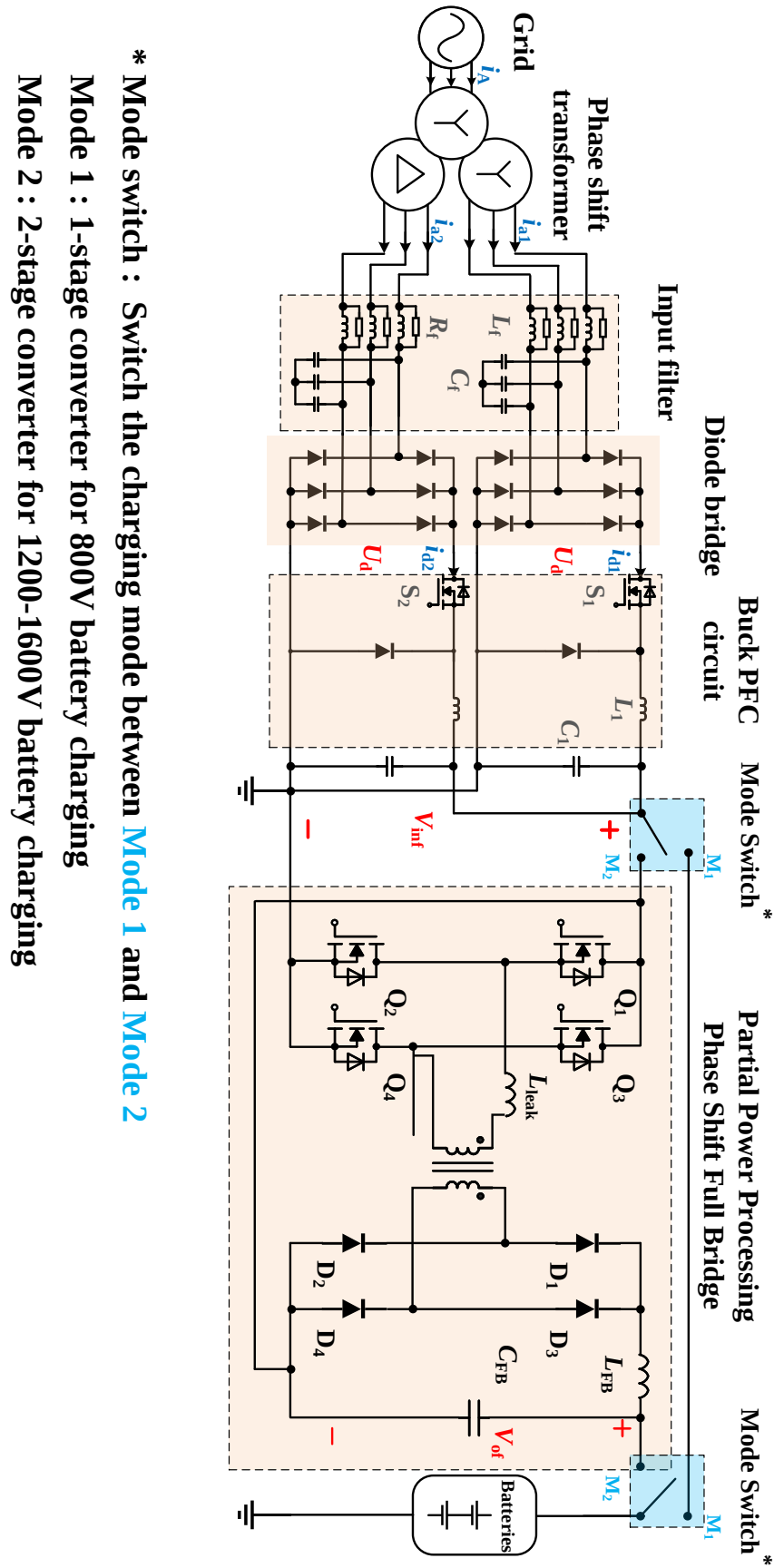


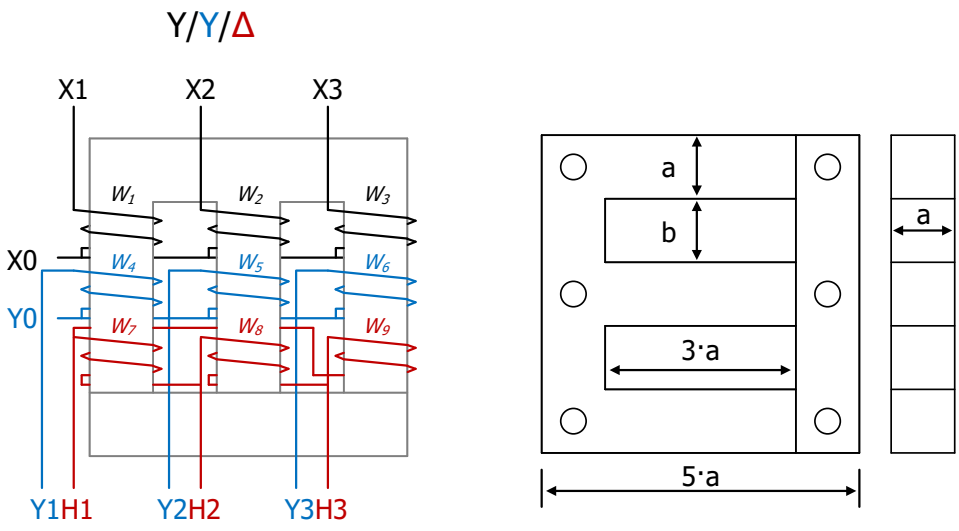
Figure 2.13: Proposed two-stage converter for the EV DC fast battery charging.

3 AC-DC:12-PULSE RECTIFIER DESIGN

3.1 THREE PHASE THREE WINDING Y/Y/Δ TRANSFORMER DESIGN

For galvanic isolation requirement and 30 degree phase-shift of voltage, the transformer connecting grid and AC-DC converter is designed as Y/Y/Δ three winding three phase transformer.

Three Phase Three winding transformer design is shown in Fig. 3.1. Fig. 3.1(a) describes a suitable winding connection of the Y/Y/Δ transformer. 'X0-X3' is the primary side of transformer in Y connection. 'Y0-Y3' is the secondary side of transformer in Y connection. 'H1-H3' is the tertiary side of transformer in Δ connection. In this connection, there will be a 30 degree voltage phase shift between the secondary side voltage and the tertiary side voltage. The EI core shape is selected because it is a common shape for large capacity power transformer. 3% Silicon Steel is chosen as the core material, which is a soft magnetic material that is best used in electrical power transformers under operation frequency of 50-60 Hz with small core loss. Fig. 3.1(b) describes the transformer EI core outline, where the size parameter $a = 200\,\text{mm}$ and $b = 50\,\text{mm}$.



(a) Three Phase Three Winding with Y/Y/Δ Connection

(b) EI Three Phase Laminations Outline

Figure 3.1: Three Phase Three winding connection and outline

3.2 TRIANGULAR CURRENT SHAPING METHOD

$$\begin{cases} u_a = U_1 \sin(\omega t) \\ u_b = U_1 \sin\left(\omega t - \frac{2\pi}{3}\right) \\ u_c = U_1 \sin\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \tag{3.1}$$

The turns ratio between the primary and the secondary windings in the star-star and star-delta transformers(Y/Y/Δ connection)is $1 : k : \sqrt{3}k$. The input filter is a second order low pass filter which could have a small portion of the shunt capacitors, e.g., several 100 nF, moved to the output of the diode bridges in order to minimize the commutation loop of the buck type converter. As the cutoff frequency of the AC filter is tuned for attenuating the high-frequency components generated by the operation of the buck type converter, this does not influence the triangular current shaping method utilized in this work which has a relatively low frequency (e.g., 6x the grid frequency as shown in Fig. 3.3). Therefore, the influence of the AC filter to the low frequency components is omitted in the following analysis.

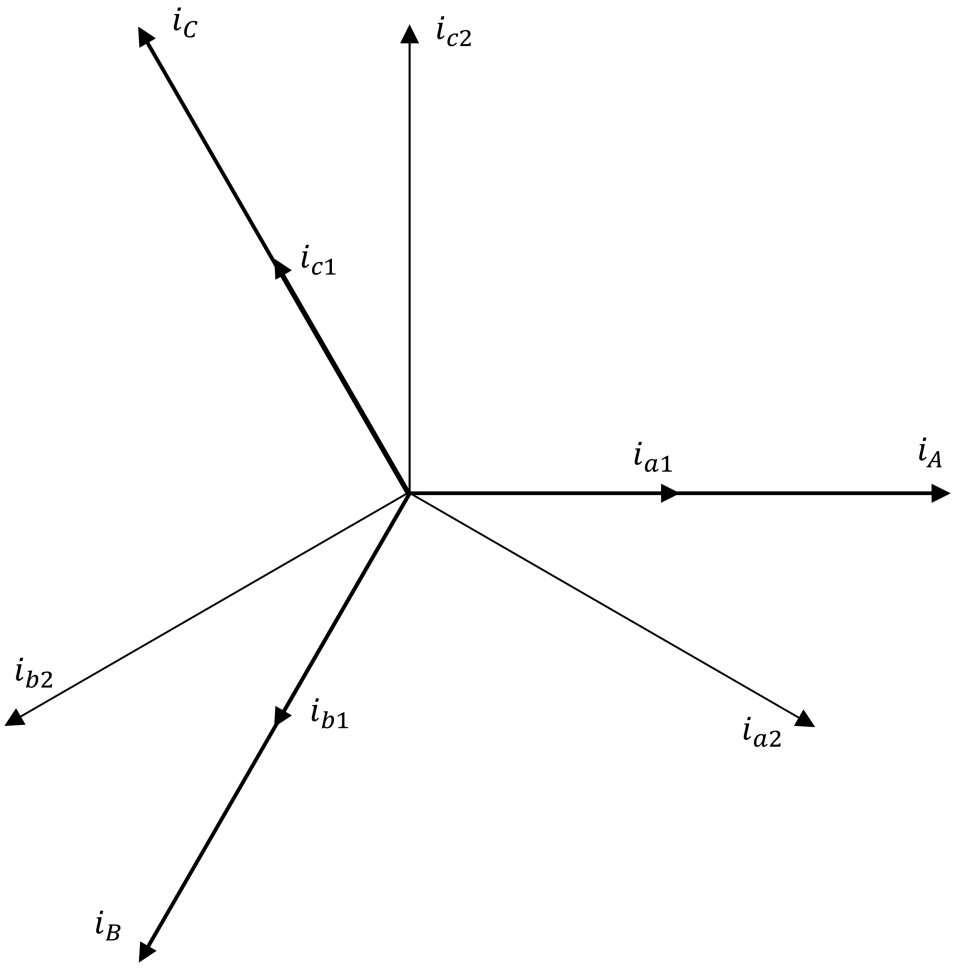


Figure 3.2: Current vector of star-delta and star-star transformer

For the selected configuration of phase-shift transformer, the current relationship between the input phase current and the two diode bridge phase currents is expressed as (3.2), and current vector are shown in Fig. 3.2.

$$\begin{cases} k \cdot i_{\mathrm{A}} = i_{\mathrm{a1}} + (i_{\mathrm{a2}} - i_{\mathrm{b2}}) / \sqrt{3} \\ k \cdot i_{\mathrm{B}} = i_{\mathrm{b1}} + (i_{\mathrm{b2}} - i_{\mathrm{c2}}) / \sqrt{3} \\ k \cdot i_{\mathrm{C}} = i_{\mathrm{c1}} + (i_{\mathrm{c2}} - i_{\mathrm{a2}}) / \sqrt{3} \end{cases} \tag{3.2}$$

$$\begin{cases} i_{\mathrm{a1}} = i_{\mathrm{d1}} S_{\mathrm{a1}}; i_{\mathrm{b1}} = i_{\mathrm{d1}} S_{\mathrm{b1}}; i_{\mathrm{c1}} = i_{\mathrm{d1}} S_{\mathrm{c1}}, \\ i_{\mathrm{a2}} = i_{\mathrm{d2}} S_{\mathrm{a2}}; i_{\mathrm{b2}} = i_{\mathrm{d2}} S_{\mathrm{b2}}; i_{\mathrm{c2}} = i_{\mathrm{d2}} S_{\mathrm{c2}}. \end{cases} \tag{3.3}$$

where $i_{\mathrm{A,B,C}}$ are the grid side phase currents, $i_{\mathrm{a1,b1,c1}}$ are the upper diode bridge phase currents, and $i_{\mathrm{a2,b2,c2}}$ are the lower diode bridge phase currents. i_{d1} and i_{d2} are the averaged output current of the two diode bridges. $S_{\mathrm{a1,b1,c1}}$ and $S_{\mathrm{a2,b2,c2}}$ are the turn-on functions of each phase of the two diode bridge. S_{a1} can be expressed as

$$S_{\mathrm{a1}} = \begin{cases} 0 & \omega t \in \left[0, \frac{\pi}{6}\right] \\ 1 & \omega t \in \left[\frac{\pi}{6}, \frac{5\pi}{6}\right] \\ 0 & \omega t \in \left[\frac{5\pi}{6}, \frac{7\pi}{6}\right] \\ -1 & \omega t \in \left[\frac{7\pi}{6}, \frac{11\pi}{6}\right] \\ 0 & \omega t \in \left[\frac{7\pi}{6}, 2\pi\right] \end{cases} \tag{3.4}$$

Where ω is the angular grid frequency. The turn-on functions of the other phases (i.e. S_{b1},S_{b2} and so on) are of 120 degree phase shift relationship between different phases and 30 degree phase shift between the two diode bridges, which can be easily derived from $S_{a}1$.

The relationship between the input phase currents and the two diode bridge output currents is derived and can be expressed as

$$\begin{cases} k \cdot i_{\mathrm{A}} = A_1 i_{\mathrm{d1}} + A_2 i_{\mathrm{d2}} \\ k \cdot i_{\mathrm{B}} = B_1 i_{\mathrm{d1}} + B_2 i_{\mathrm{d2}} \\ k \cdot i_{\mathrm{C}} = C_1 i_{\mathrm{d1}} + C_2 i_{\mathrm{d2}} \end{cases} \tag{3.5}$$

where the coefficients A, B, and C are expressed as

$$\begin{cases} A_1 = S_{\mathrm{a1}} \\ A_2 = (S_{\mathrm{a2}} - S_{\mathrm{b2}}) / \sqrt{3} \\ B_1 = S_{\mathrm{b1}} \\ B_2 = (S_{\mathrm{b2}} - S_{\mathrm{c2}}) / \sqrt{3} \\ C_1 = S_{\mathrm{c1}} \\ C_2 = (S_{\mathrm{c2}} - S_{\mathrm{a2}}) / \sqrt{3} \end{cases} \tag{3.6}$$

The expected sinusoidal input phase current from the grid side is expressed as,

$$\begin{cases} i_{\mathrm{A}} = I \sin(\omega t) \\ i_{\mathrm{B}} = I \sin\left(\omega t - \frac{2\pi}{3}\right) \\ i_{\mathrm{C}} = I \sin\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \tag{3.7}$$

where I is the amplitude of the AC grid current.

The averaged i_{d1} and i_{d2} from Eq. (3.5), (3.6) and (3.7), are expressed as (3.8) and shown in Fig. 3.3, where the transformer turns ratio k and current I are seen as reference values which depend on the local grid connection and power processed by the system.

$$\begin{cases} i_{d1} = \frac{B_1 \sin(\omega t) - \frac{A_2}{B_2} \sin\left(\omega t - \frac{2\pi}{3}\right)}{A_1 - \frac{B_1}{B_2} A_2} k \cdot I \\ i_{d2} = \frac{B_1 \sin(\omega t) - \frac{A_1}{B_1} \sin\left(\omega t - \frac{2\pi}{3}\right)}{A_2 - \frac{B_2}{B_1} A_1} k \cdot I \end{cases} \tag{3.8}$$

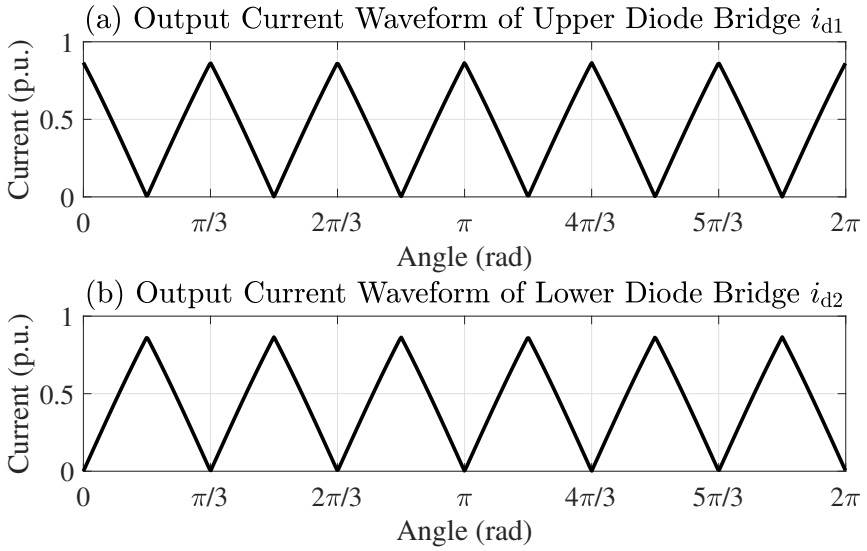


Figure 3.3: Solved output current waveform of diode bridge from Eq. (3.8). Herein, $k = 1$ is considered and values are rated to the AC grid amplitude I.

As shown in Fig. 3.3, i_{d1} and i_{d2} has $\pi/6$ phase shift and the shape of the current waveform is almost a standard triangular waveform. Noted that in reality the current waveform of the diode bridges is discontinuous formed by pieces of the impressed buck's inductor current. The averaged values derived in (3.8) and shown in Fig. 3.3 are the one derived after the AC filter.

The the peak value of i_{d1} and i_{d2} is:

$$\hat{i_{d1}} = \hat{i_{d2}} = \frac{\sqrt{3}}{2} k \cdot I \tag{3.9}$$

Assume i_{d1} and i_{d2} as triangular form. Then i_{d1} and i_{d2} are expressed in a period as:

$$i_{d1} = \begin{cases} \frac{3\sqrt{3}}{\pi} k \cdot I \cdot \omega t + \frac{\sqrt{3}}{2} k \cdot I & \omega t \in \left[-\frac{\pi}{6}, 0\right] \\ -\frac{3\sqrt{3}}{\pi} k \cdot I \cdot \omega t + \frac{\sqrt{3}}{2} k \cdot I & \omega t \in \left[0, \frac{\pi}{6}\right] \end{cases} \tag{3.10}$$

$$i_{d2} = \begin{cases} -\frac{3\sqrt{3}}{\pi} k \cdot I \cdot \omega t & \omega t \in \left[-\frac{\pi}{6}, 0\right] \\ \frac{3\sqrt{3}}{\pi} k \cdot I \cdot \omega t & \omega t \in \left[0, \frac{\pi}{6}\right] \end{cases} \tag{3.11}$$

3.3 BUCK PFC CIRCUIT DESIGN

3.3.1 Control Design

Fig. 3.4 shows the control block of two Buck PFC circuit. There are voltage PI closed-loop control and current PI closed-loop control for each buck circuit. Phase Lock Loop (PLL) generates phase angle of AC voltage from gird side. The current reference varies according to the phase angle. The current references for two buck inductor current control are triangular shape with 180 degree phase-shift for each other, as shown in Fig. 3.3. Voltage PI closed-loop control offers regular output voltage, and current PI closed-loop control realizes PFC and harmonic reduction using triangular current shaping method.

the inductor current, input voltage and duty cycle of the upper buck PFC circuit are shown in Fig. 3.5.

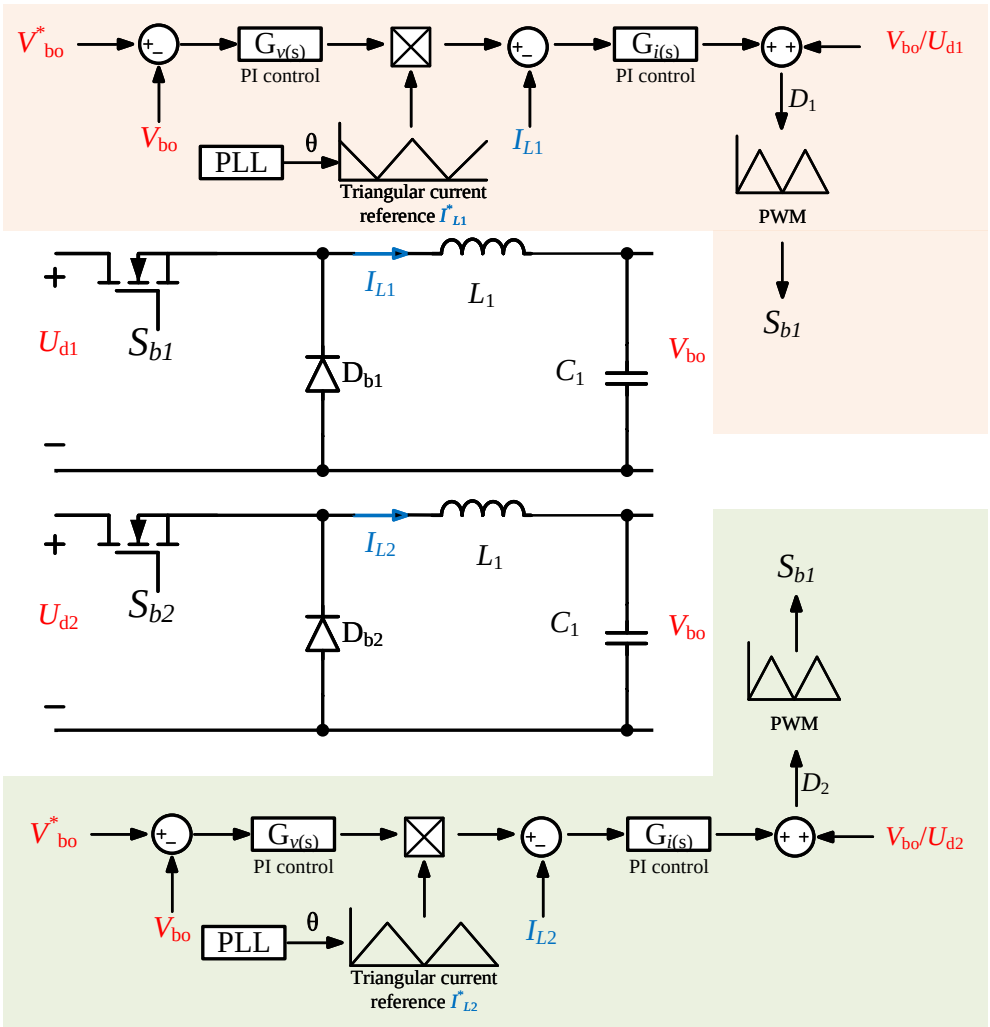


Figure 3.4: Control block of two Buck PFC circuit

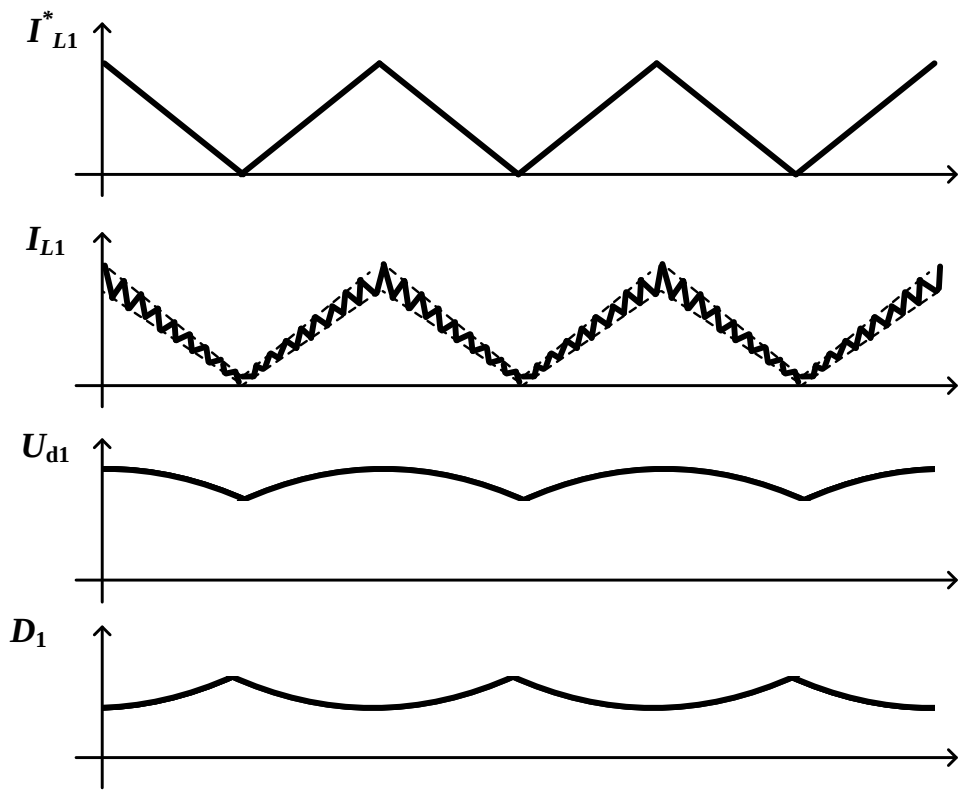


Figure 3.5: Current, voltage and duty cycle of Buck

3.3.2 Phase Lock Loop

To control the power factor, the current reference has to synchronized with the phase angle of ac voltage from grid. PLL is widely used in active inverter to keep track of the grid frequency and phase. In the thesis, the inputs of PLL are the three phase ac voltage and the output is phase angle of three phase ac voltage. Assuming that, the phase angle of ac voltage is θ, the block diagram of PLL technique can be described as Fig. 3.6. Three phase a-b-c voltage can be transformed to d-q voltage by using the Clark and Park transfer function, which is described as,

$$\begin{aligned}
\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} &= \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \\ 0 \end{bmatrix} \\
&= \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t)\cos(\theta) + \sin(\omega t)\sin(\theta) \\ -\sin(\theta)\cos(\omega t) + \cos(\theta)\sin(\omega t) \\ 0 \end{bmatrix} \\
&= \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t - \theta) \\ \sin(\omega t - \theta) \\ 0 \end{bmatrix}
\end{aligned} \tag{3.12}$$

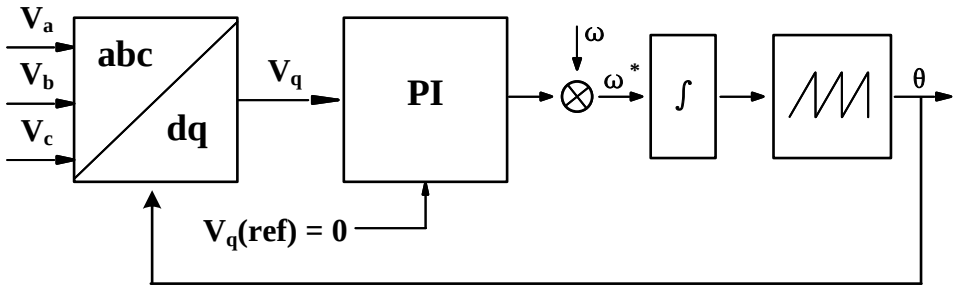


Figure 3.6: Block diagram of PLL [9]

3.3.3 Parameter Design

12-pulse rectifier can reach high output voltage which is available for current battery charging voltage. To reduce system losses, for 800 V charging voltage, 12-pulse rectifier is designed to directly charge battery, and the output voltage of buck circuit is set to 800 V.

The main design constraint for the buck circuit is the maximum allowed current ripple across the inductor (ΔI_{L1}) and maximum output capacitor voltage ripple (ΔV_o), based on which, the buck circuit inductance L_1 and capacitance C_1 can be calculated as [13],

$$L_1 = \frac{D \cdot (1 - D) \cdot U_d}{\Delta I_{L1} \cdot f_s} \tag{3.13}$$

$$C_1 = \frac{D \cdot (1 - D) \cdot U_d}{8 \cdot L_1 \cdot \Delta V_{bo} \cdot f_s^2} \tag{3.14}$$

where D is the duty cycle of the buck circuit. U_d is the maximum output voltage of diode bridge. V_{bo} is the output voltage of buck circuit. f_s is the switching frequency of the PWM modulator of the buck converter.

3.4 INPUT FILTER DESIGN

As previously discussed, the input current of the buck circuit is discontinuous, formed by the inductor current when the active semiconductor is turned on and null when the switch is turned Off. Therefore, the input filter is required to filter out the high frequency current component defined by the PWM operation of this DC-DC converter. The input filter, which in the studied case is a LC filter, can be designed as [13],

$$C_f = \frac{D \cdot (1 - D) \cdot I_o}{\Delta V_{Cf} \cdot f_s} \tag{3.15}$$

$$L_f = \frac{D \cdot (1 - D) \cdot I_o}{8 \cdot \Delta I_{Lf} \cdot C_f \cdot f_s^2} \tag{3.16}$$

Note that the adding of the input filter will influence the stability margins of the feedback control loops of the buck circuit. For stability enhancement purpose, the use of passive or active damping technique at the input filter is advantageous. According to the Extra Element Theorem (EET) [30], adding the filter circuit to the buck converter will bring a correction factor M to the original transfer function. The control-to-output transfer function $G_{vd}(s)$ of the buck converter with input filter can be expressed as

$$G_{vd}(s)_{|Z_o(s)=0} = \frac{V_o(s)}{\hat{d}(s)} \tag{3.17}$$

$$G_{vd}(s) = \left(G_{vd}(s)_{|Z_o(s)=0}\right) \cdot M \tag{3.18}$$

$$M(s) = \frac{1 + \frac{Z_o(s)}{Z_N(s)}}{1 + \frac{Z_o(s)}{Z_D(s)}} \tag{3.19}$$

$$Z_D(s) = \frac{R}{D^2} \frac{1 + \frac{sL_1}{R} + s^2 L_1 C_1}{1 + sRC_1} \tag{3.20}$$

$$Z_N(s) = -\frac{R}{D^2} \tag{3.21}$$

where $G_{vd}(s)_{|Z_o(s)=0}$ is the control-to-output transfer function without input filter. $Z_o(s)$ is the output impedance of the input filter. $Z_D(s)$ is the converter input impedance, with the controller variable $\hat{d}(s)$ set to zero, expressed as (3.20). $Z_N(s)$ is the converter input impedance, with the output nulled to zero, expressed as (3.21). R is the equivalent load impedance modelled as a resistance.

For the stability of the buck control, the coefficient $M(s)$ should be close to 1. In case a passive damping circuit is used, to reduce the loss the damping resistor R_f could be paralleled connected with L_f. In this case the output impedance of the input filter $Z_o(s)$ can be expressed as

$$Z_o(s) = \frac{sR_f L_f}{s^2 R_f L_f C_f + sL_f + R_f} \tag{3.22}$$

The use of active damping or virtual resistance should be sought in the studied application in order to minimize the system losses. The input filter transfer function of the buck side current i_B to the grid side current i_g is expressed as

$$G_i(s) = \frac{i_g}{i_B} = \frac{sL_f + R_f}{s^2 R_f L_f C_f + sL_f + R_f} \tag{3.23}$$

The bode magnitude plot of the correction factor and input filter transfer function is shown in Fig. 3.7. Herein, the parameters of the input filter are set as $L_f = 30\,\mu H$, $C_f = 15\,\mu F$ and $R_f = 5\,\Omega$.

As it can be noted in Fig. 3.7, the utilization of damping provides great attenuation to oscillations at the resonance frequency of the filter, which make the system more robust to stability problems.

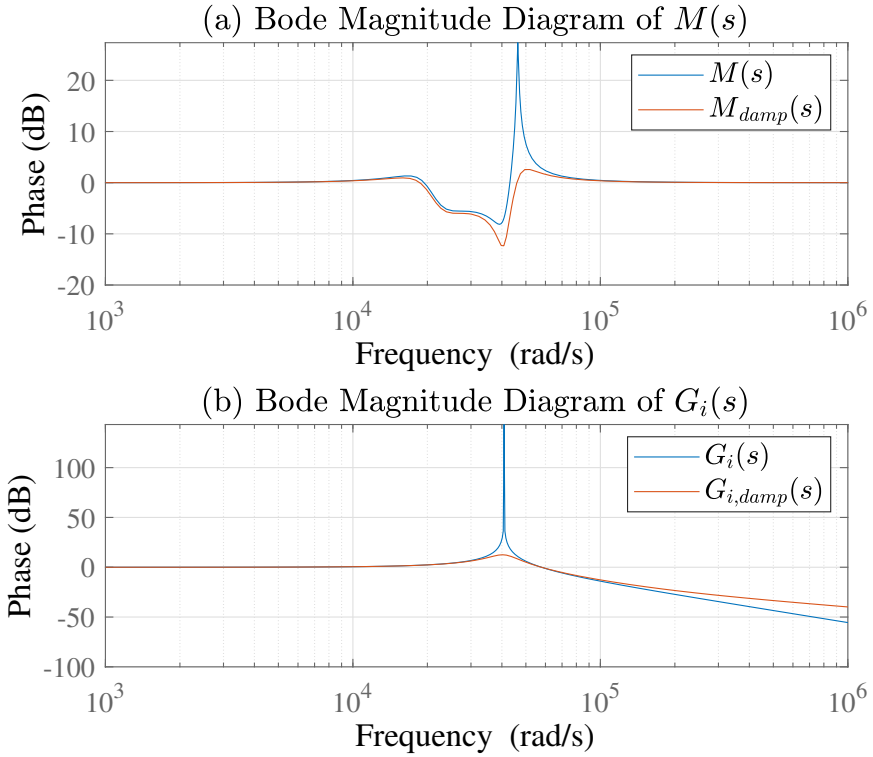


Figure 3.7: Bode Magnitude Plot of $M(s)$ and $G_i(s)$

4 DC-DC:PARTIAL POWER FULL BRIDGE CONVERTER DESIGN

4.1 PARTIAL POWER RATIO

The Input-parallel-output-series (IPOS) connection of partial power structure is shown in Fig. 4.1. The equivalent circuit that presenting the relationship of the output voltage is shown as Fig. 4.2.

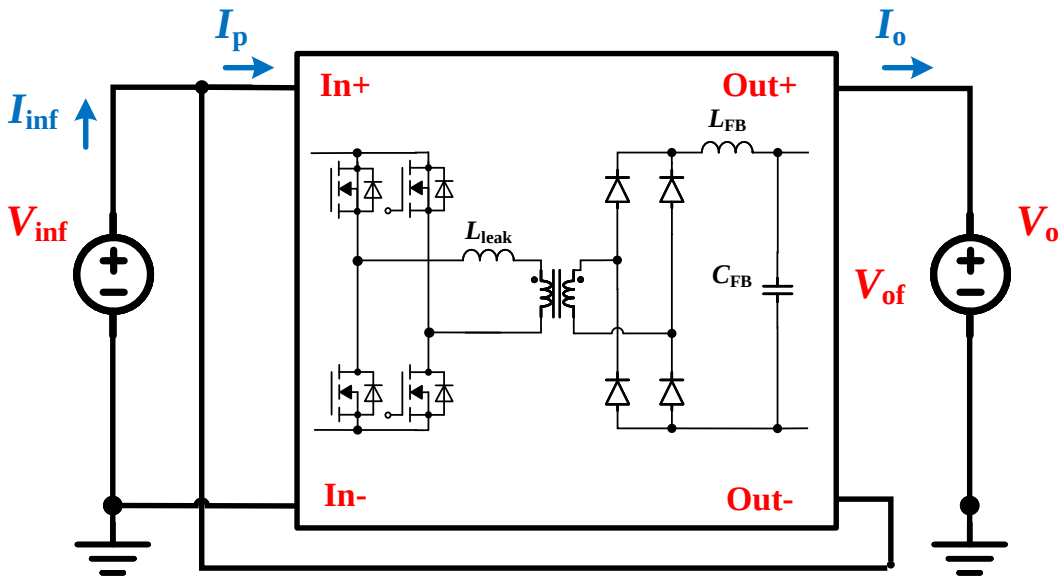


Figure 4.1: IPOS Partial Power Connection

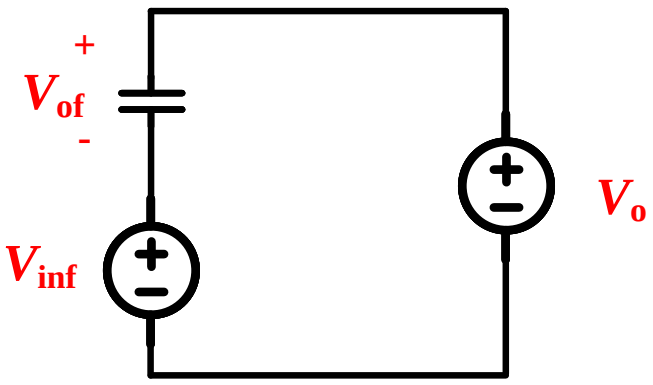


Figure 4.2: Equivalent circuit of output voltage

From the equivalent circuit, the power processed by the phase shift full bridge can be studied. The voltage and current can be expressed as (4.1) and (4.2) according to Kirchhoff's laws.

$$V_{\text{inf}} + V_{\text{of}} = V_{\text{o}} \tag{4.1}$$

$$I_{\text{inf}} = I_{\text{p}} + I_{\text{o}} \tag{4.2}$$

where V_{of} is the output voltage of full bridge and V_{o} is the output voltage of the whole system. I_{inf} is the input current of full bridge. I_{p} is the processed current by the converter. I_{o} is the output current of the whole system.

The efficiency of the system η_{FB} can be calculated as,

$$\eta_{\text{FB}} = \frac{V_{\text{o}} \cdot I_{\text{o}}}{V_{\text{inf}} \cdot I_{\text{inf}}} \tag{4.3}$$

The ratio of processed power by full bridge converter K_{pr} is expressed as

$$K_{\text{pr}} = \frac{P_{\text{conv}}}{P_{\text{inf}}} = \frac{V_{\text{of}} \cdot I_{\text{o}}}{V_{\text{inf}} \cdot I_{\text{inf}}} \tag{4.4}$$

Substitute (4.1), (4.2) and (4.3) into (4.4), processed power can be expressed as the function of voltage gain ($G_V = \frac{V_{\text{o}}}{V_{\text{inf}}}$)

$$K_{\text{pr}} = \eta_{\text{FB}} - \frac{\eta_{\text{FB}}}{G_V} \tag{4.5}$$

4.2 FULL BRIDGE TRANSFORMER DESIGN

Ferrite N87 is choosen as the core material because it is a soft magnetic material which is suitable for high-frequency application. Lize wire [27] is chosen so that the relationship between the ac resistance and the dc resistance is 1. Core geometry K_g approach is used in the design of core shape [27].

$$K_c = 0.145 \left(K_f\right)^2 (f)^2 \left(B_m\right)^2 \left(10^{-4}\right) \tag{4.6}$$

$$K_g = \frac{P_t}{2K_e \cdot \alpha_g} \tag{4.7}$$

where $K_f = 4$ for square wave and K_e is electrical condition. According to K_g C core [27] is selected as the core of high frequency transformer.

Primary turns N_{p} can be calculated as,

$$N_{\text{p}} = \frac{V_{\text{p}} \left(10^4\right)}{K_f \cdot B_{\text{ac}} \cdot f_{\text{sFB}} \cdot A_{\text{c}}} \tag{4.8}$$

where V_{p} is primary side voltage, B_{ac} is flux density, A_{c} is core area and f_{sFB} is the switching frequency of full bridge.

Secondary turns N_{s} is determined by the maximum output voltage of full bridge, expressed as,

$$N_{\mathrm{s}} = \frac{N_p \cdot V_{\mathrm{of,max}}}{V_{\mathrm{inf}}} \tag{4.9}$$

The strands number S_{n} of selected Lize wire is determined by current density J, which can be calculated with (4.10),(4.11) and (4.12).

$$J = \frac{P_t \left(10^4\right)}{K_f \cdot K_u \cdot B_{\mathrm{ac}} \cdot A_{\mathrm{c}} \cdot A_{\mathrm{p}}} \tag{4.10}$$

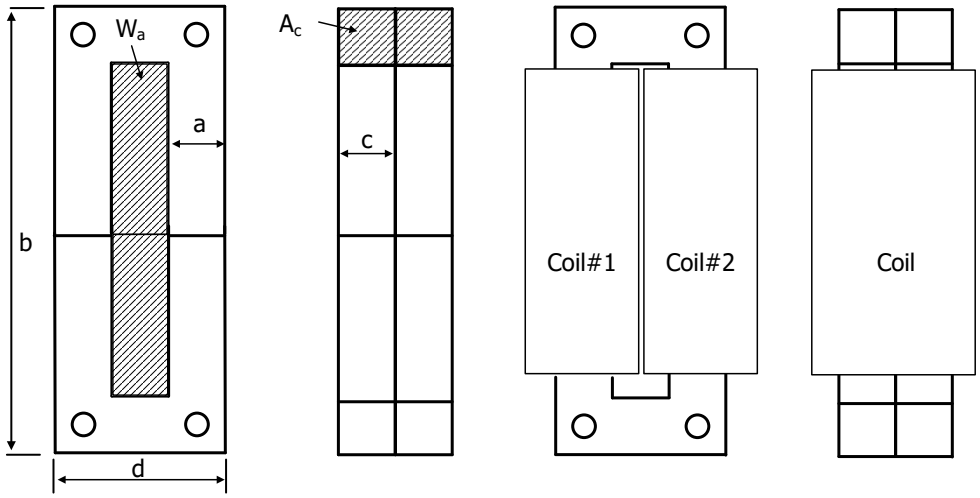
where P_{t} is the power of transformer. A_{p} is the area product, $A_{\mathrm{p}} = W_{\mathrm{a}} A_{\mathrm{c}}$.

$$A_{\mathrm{wa}} = \frac{I_{\mathrm{p,s}} \cdot \sqrt{D_{\mathrm{max}}}}{J} \tag{4.11}$$

$$S_{\mathrm{n}} = \frac{A_{\mathrm{wa}}}{\#20} \tag{4.12}$$

where A_{wa} is the bare wire area, $I_{\mathrm{p,s}}$ is the primary side and secondary side current of transformer.

Core design is shown in Fig. 4.3 and HF transformer design is shown in Table. 4.1.



(a) UU N87 Full bridge transformer core (b) UU N87 Full bridge transformer winding

Figure 4.3: Full Bridge Transformer Core Design

Core material	Ferrite N87
Core shape	UU
Core size	93/152/30
a	28 mm
b	152 mm
c	30 mm
d	93 mm
W_a	32.65 cm^2
A_c	16.8 cm^2
Permeability	1900
Flux density B_m	200 mT
Stack numbers	2
Primary turns	39
Secondary turns	40
Lize wire	AWG#20
Wire strands	14

Table 4.1: Full Bridge Transformer Parameters Design

4.3 PARTIAL POWER FULL BRIDGE

4.3.1 Topology

The conventional full bridge is shown in Fig. 4.4. Partial power processing topology is shown in Fig. 4.5. For unidirectional power transmission, four switches are in the input side and four diodes are in the output side.

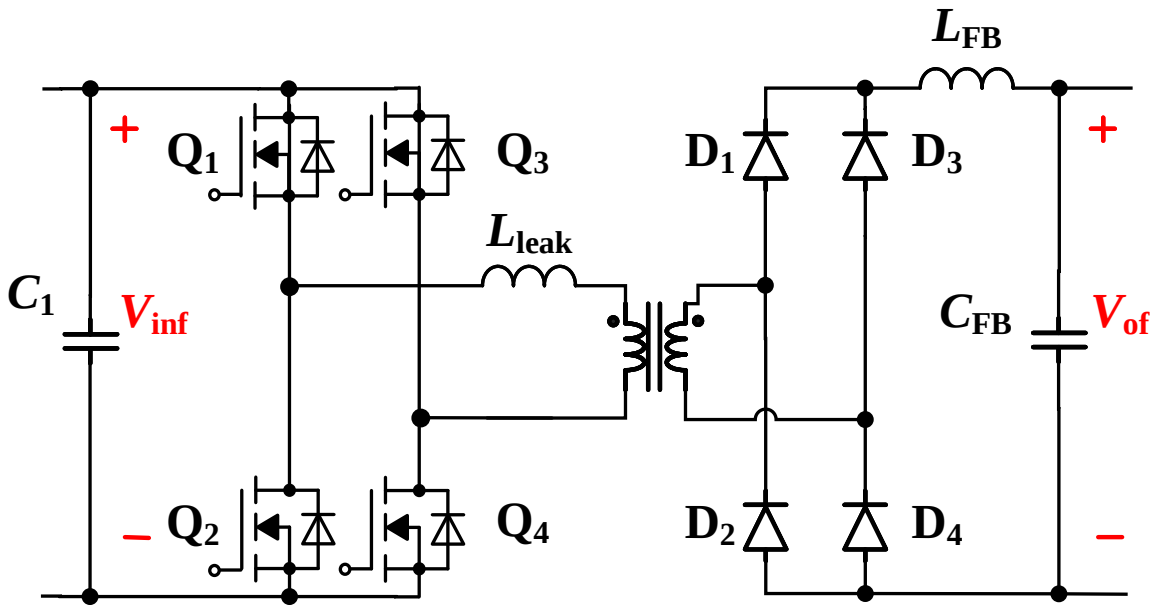


Figure 4.4: Conventional full bridge topology

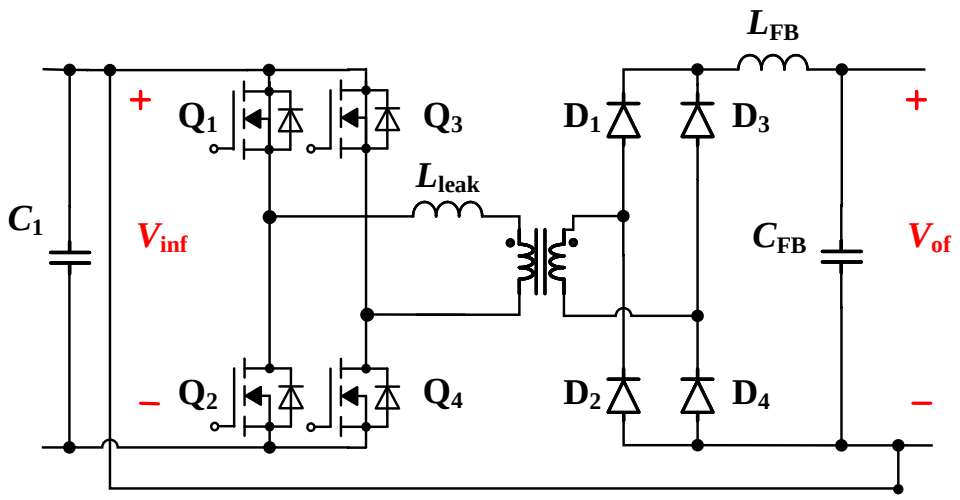


Figure 4.5: Partial Power Processing Full Bridge Topology

4.3.2 Control Design

Fig. 4.6 shows the control block of partial power full bridge circuit. Main controllers are Voltage PI closed-loop control and current PI closed-loop control. Voltage PI closed-loop control offers regular output voltage.

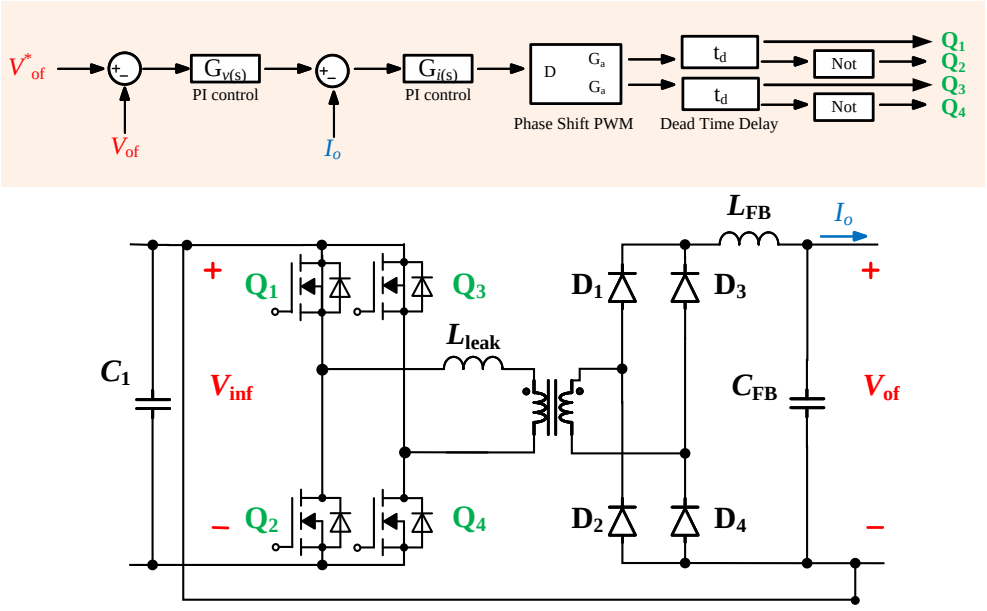


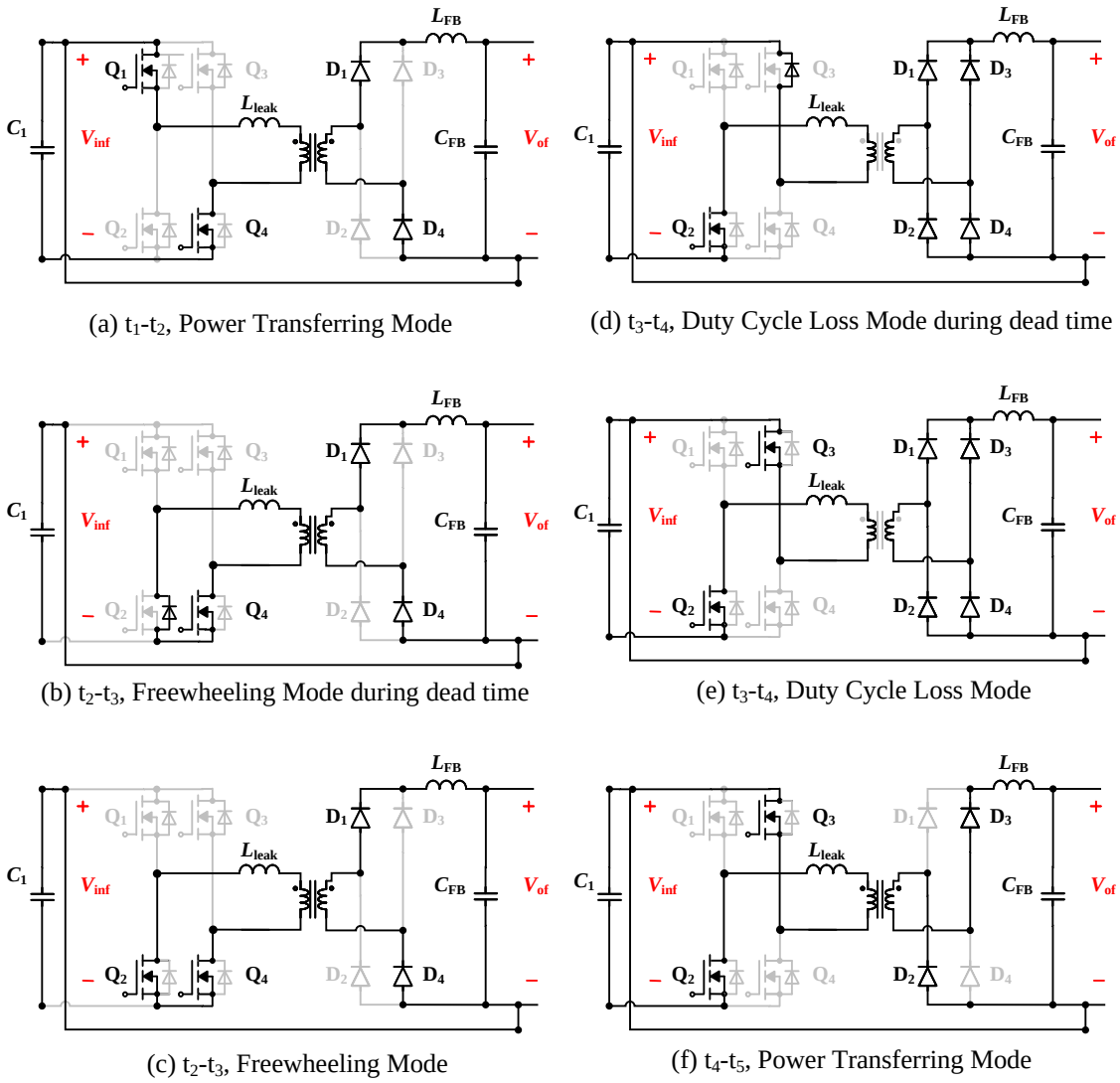
Figure 4.6: Control Block of Partial Power Processing Phase Shift Full Bridge

4.3.3 Opertation

There are three main operation mode of partial power phase shift full bridge converter, which shown as Fig. 4.7.

Power Transferring Mode $t_1 - t_2$: SIC MOSFET Q1 and Q4 are conducting at this stage. With the partial power processing ISOP connecting, input voltage of full bridge is equal to the voltage difference between output volt-

age of buck and output voltage of full bridge. Input voltage of full bridge is shared by the voltage on leakage inductor and magnetic inductor. Primary side current increases from I_{p1} to I_{p2}. Power is transfering to the secondary side and a small part of powre is stored in leakage inductor. On the secondary side, only diode D1 and D4 are conducting. At t_2, SIC MOSFET Q1 is hard turned off and power transfering mode ends.



(a) t_1-t_2, Power Transferring Mode

(d) t_3-t_4, Duty Cycle Loss Mode during dead time

(b) t_2-t_3, Freewheeling Mode during dead time

(e) t_3-t_4, Duty Cycle Loss Mode

(c) t_2-t_3, Freewheeling Mode

(f) t_4-t_5, Power Transferring Mode

Figure 4.7: Partial Power Processing Full Bridge Operation

Freewheeling Mode $t_2 - t_3$: At t_2, body diode of SIC MOSFET Q2 turns on because of continuous current of the leakage inductor. The conduction of primary side body diode of Q2 and MOSFET Q4 forms a freewheeling loop. At this stage, Leakage inductor releases energy. Voltage of leakage inductor is applied on the magnetic inductor. Primary side current decreases from I_{p2} to I_{p3}. After the dead time, SIC MOSFET Q2 are turned on with ZVS because of the conduction of body diode. On the secondary side, only diode D1 and D4 are conducting. Voltage on output inductor is equal to the voltage difference between output voltage of full bridge and the secondary

side voltage of transformer. At t_3, SIC MOSFET Q4 is hard turned off and freewheeling mode ends.

Duty Cycle Loss Mode $t_3 - t_4$: At t_3, body diode of SIC MOSFET Q3 turns on because of continuous current of the leakage inductor. With the conduction of body diode of Q3 and MOSFET Q2, reverse input voltage of full bridge is applied on leakage inductor. Because of the different current changing speed of output inductor and leakage inductor and transformer current relationship, secondary side diode D2 and D3 turns on. With four diode conducting, secondary side voltage of transformer is clamped to zero. No voltage is applied on transformer, which causes the loss of duty cycle. Primary side current decreases from I_{p3} to $-I_{p1}$. Secondary side current of D1 and D4 decreases and current of D2 and D3 increases. After the dead time, SIC MOSFET Q2 are turned on with ZVS because of the conduction of body diode. At t_4, primary side current is equal to the current of output inductor. At this moment, current of diode D1 and D4 decrease to zero and turn off. Voltage of transformer is no longer clamped to zero and duty cycle loss mode ends. After t_4, voltage is applied on transformer with the conduction of MOSFET Q2 and Q3, and a new power transferring mode starts. The operation MOSFET Q1, Q4 and Q2, Q3 of full bridge are symmetric. The operation of the rest half period is the same as $t_1 - t_4$.

These three processes are described by formulas in the following section. Gate signals, current and voltage are shown in Fig. 4.8. Transformer equivalent circuit of different modes are shown in Fig. 4.9.

Power Transferring Mode: Fig. 4.9 (a) shows the equivalent circuit during power transferring mode and (b) shows the transformer equivalent circuit after referring to primary side. Secondary side voltage and inductor L_{FB} are referred to primary side, expressed as,

$$L_{\mathrm{FB}}^{'} = L_{\mathrm{FB}} \cdot n^2; \tag{4.13}$$

$$E_{\mathrm{p}} = E_{\mathrm{s}} \cdot n; \tag{4.14}$$

where $n = \frac{n_{\mathrm{p}}}{n_{\mathrm{s}}}$ is the turn ratio of full bridge transformer and E_{s} is equal to V_{of}. With superposition theorem of voltage, voltage on the magnetic inductor L_m can be expressed as,

$$V_{\mathrm{m}} = V_{\mathrm{m1}} + V_{\mathrm{m2}} \tag{4.15}$$

$$V_{\mathrm{m1}} = \frac{L_{\mathrm{m}} // L_{\mathrm{FB}}^{'}}{L_{\mathrm{leak}} + L_{\mathrm{m}} // L_{\mathrm{FB}}^{'}} \cdot V_{\mathrm{inf}} \tag{4.16}$$

$$V_{\mathrm{m2}} = \frac{L_{\mathrm{m}} // L_{\mathrm{leak}}}{L_{\mathrm{FB}}^{'} + L_{\mathrm{m}} // L_{\mathrm{leak}}} \cdot E_{\mathrm{p}} \tag{4.17}$$

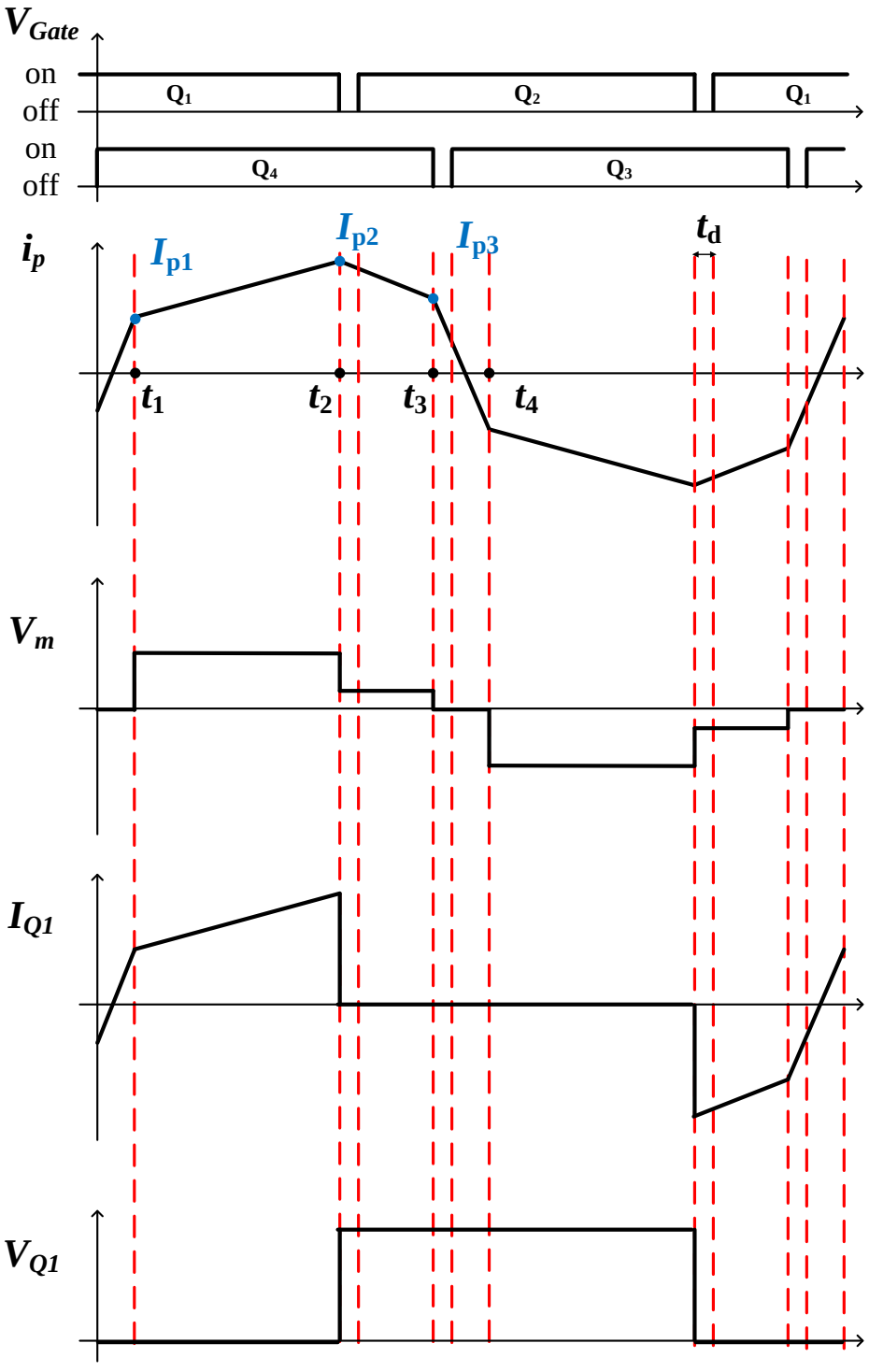
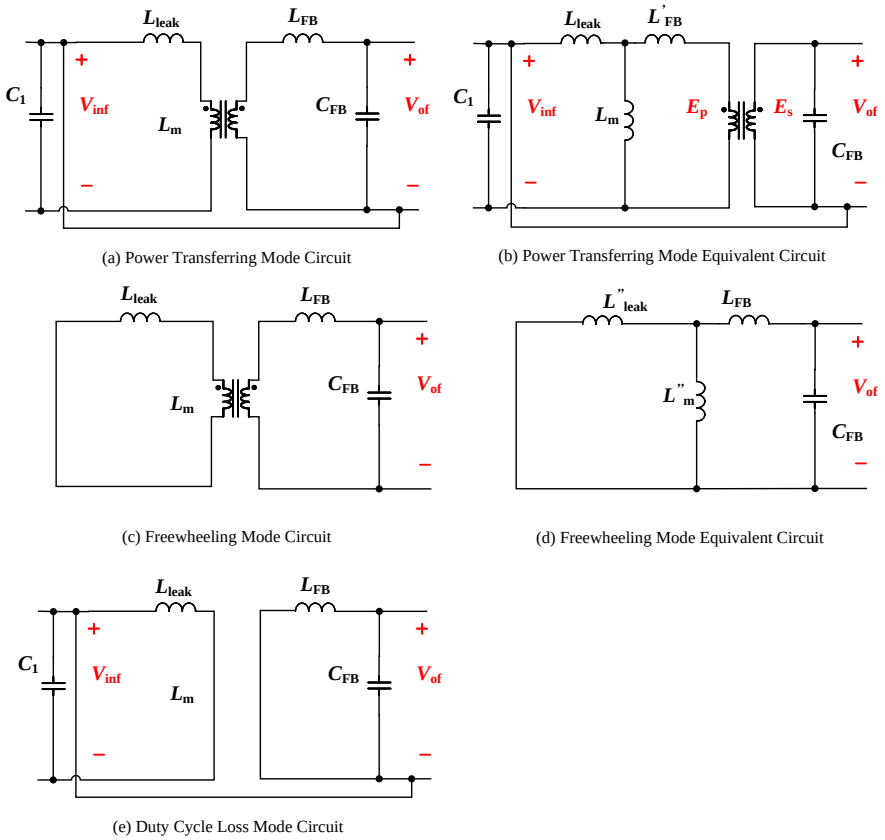


Figure 4.8: Gate signals, current and voltage of operation



(a) Power Transferring Mode Circuit

(b) Power Transferring Mode Equivalent Circuit

(c) Freewheeling Mode Circuit

(d) Freewheeling Mode Equivalent Circuit

(e) Duty Cycle Loss Mode Circuit

Figure 4.9: Power Transferring Mode Transformer Equivalent Circuit

Knowing the voltage on magnetic inductor, voltage of transformer secondary side is expressed as,

$$V''_{\mathrm{m}} = \frac{V_{\mathrm{m}}}{n} \tag{4.18}$$

During power transferring mode, the current change of full bridge inductor is expressed as,

$$\Delta I_{\mathrm{s,pt}} = \frac{\left(V''_{\mathrm{m}} - V_{\mathrm{of}}\right) \cdot D_{\mathrm{eff}}}{L_{\mathrm{FB}} \cdot f_{\mathrm{sFB}}} \tag{4.19}$$

where f_{sFB} is the switching frequency of full bridge converter, D_{eff} is the effective duty cycle and is expressed as

$$D_{\mathrm{eff}} = \frac{V_{\mathrm{of}} \cdot n}{2V_{\mathrm{inf}}} \tag{4.20}$$

Current change and average current of primary side can be expressed as,

$$\Delta I_{\mathrm{p,pt}} = \Delta I_{\mathrm{s,pt}} / n \tag{4.21}$$

$$I_{\mathrm{p,pt,avg}} = \frac{K_{\mathrm{pr}} \cdot P_{\mathrm{o}}}{V_{\mathrm{of}} \cdot n} \tag{4.22}$$

Thus, current I_{p1} and I_{p2} in Fig. 4.8 can be calculated as,

$$I_{p1} = I_{p,pt,avg} - \frac{1}{2} \cdot \Delta I_{p,pt} \tag{4.23}$$

$$I_{p2} = I_{p,pt,avg} + \frac{1}{2} \cdot \Delta I_{p,pt} \tag{4.24}$$

Freewheeling Mode: Fig. 4.9 (c) shows the equivalent circuit during freewheeling mode and (d) shows the transformer equivalent circuit after referring to secondary side. Primary side leakage inductor and magnetic inductor are referred to secondary side, expressed as,

$$L''_{leak} = L_{leak}/n^2 \tag{4.25}$$

$$L''_{m} = L_{m}/n^2 \tag{4.26}$$

During freewheeling mode, voltage on the full bridge inductor and the current change of full bridge inductor are expressed as,

$$V_{FB,fw} = \frac{L_{FB}}{L''_{leak}//L''_{m} + L_{FB}} \cdot V_{of} \tag{4.27}$$

$$\Delta I_{s,fw} = \frac{V_{FB,fw} \cdot (1/2 - D_{eff} - D_{loss})}{L_{FB} \cdot f_{sFB}} \tag{4.28}$$

where D_{loss} is the duty cycle loss. Primary side current change and I_{p3} can be expressed as,

$$\Delta I_{p,fw} = \Delta I_{s,fw}/n \tag{4.29}$$

$$I_{p3} = I_{p2} - \Delta I_{p,fw} \tag{4.30}$$

Duty Cycle Loss Mode: Fig. 4.9 (e) shows the equivalent circuit during freewheeling mode. There is no voltage on the magnetic inductor. The operations of Primary side and secondary side circuit are independent. The current changes in primary side and secondary side are expressed as

$$\Delta I_{p,dl} = \frac{V_{inf} \cdot D_{loss}}{L_{leak} \cdot f_{sFB}} \tag{4.31}$$

$$\Delta I_{p,dl} = I_{p3} + I_{p1} \tag{4.32}$$

$$\Delta I_{p,dl} = \frac{I_{s2} - \Delta I_{s,fw}}{n} \tag{4.33}$$

With (4.31),(4.32) and (4.33), current I_{p3} in Fig. 4.8 and D_{loss} can be derived.

4.3.4 Parameter Design

The output voltage of 12-pulse rectifier (output voltage of buck circuit) is designed to fit the current existing 800 V charging voltage. For higher voltage application, this step-up type PPP full bridge is designed to increase the output voltage of DCFC system to $1200 - 1600$ V. Therefore, the input voltage of full bridge converter is 800 V and the output voltage of full bridge converter is $400 - 800$ V. Voltage gain of PPP full bridge is $1.5 - 2$. According to (4.5), processed power ratio by the converter is around $\frac{1}{3} - \frac{1}{2}$, considering the efficiency of converter η_{FB} is close to 1.

As the output filter design of buck circuit, the output filter design of PPP full bridge is also based on the maximum allowed current ripple across the inductor ($\Delta I_{L\mathrm{FB}}$) and maximum output capacitor voltage ripple (ΔV_{of}).

According to (4.19), the PPP full bridge circuit inductance L_{FB} can be calculated as,

$$L_{\mathrm{FB}} = \frac{\left(V_{\mathrm{m}}'' - V_{\mathrm{of}}\right) \cdot D_{\mathrm{eff}}}{\Delta I_{\mathrm{s,pt}} \cdot f_{\mathrm{sFB}}} \tag{4.34}$$

and capacitance C_{FB} can be calculated as,

$$C_{\mathrm{FB}} = \frac{\Delta I_{\mathrm{s,pt}}}{8 \cdot \Delta V_{\mathrm{of}} \cdot f_{\mathrm{sFB}}} \tag{4.35}$$

4.4 BATTERY MODELING

With higher C-rate charging the battery, the lag between voltage and state of charge (SOC) increases, so the SOC of the battery can only reach till 70%-80%. Therefor, constant current constant voltage (CCCV) mode are usually in battery fast charging. CC mode remains high C-rate charging in order to charge the battery with high power and speed. When the SOC of the battery reach 70%-80%, the charging power is reduced with CV charging. Characteristic curves for CCCV charging is shown in Fig. 4.10.

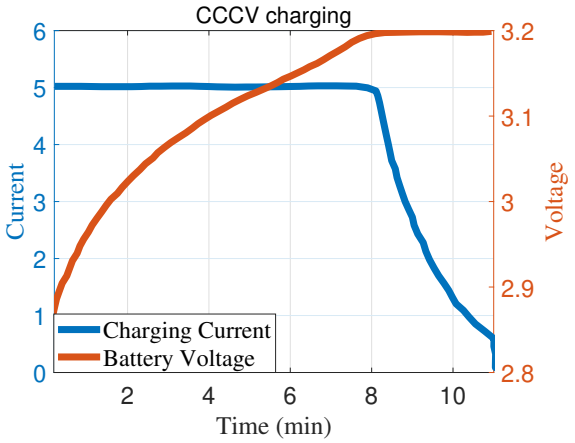


Figure 4.10: Characteristic curves for CCCV charging [35]

5 LOSS MODELING

The dominant system losses can be divided into three parts: The loss of passive components, i.e., inductor and capacitor, the loss of the multi-pulse transformer, and the loss of the semiconductor, i.e diode and SIC MOSFET.

5.1 INDUCTOR LOSS

The loss of the inductor consists of the copper winding and core losses, and it can be expressed as

$$P_L = P_{L,\text{winding}} + P_{L,\text{core}} \tag{5.1}$$

Winding loss of inductor consists of the conduction loss of DC current component and AC current component. Considering both the proximity and skin effects, the equivalent AC resistance of a certain frequency component can be modelled by a factor F_r which multiples the equivalent DC resistance of the inductor winding expressed as [46],

$$\begin{aligned} P_{L,\text{winding}} &= P_\text{DC} + P_\text{AC} \\ &= R_\text{DC} I_\text{DC}^2 + \sum_{n=1}^{\infty} R_\text{ACn} I_\text{n}^2 \end{aligned} \tag{5.2}$$

$$R_\text{AC} = F_\text{r} R_\text{DC} \tag{5.3}$$

where F_r is a function of frequency, which could be derived as following: the skip depth is expressed as,

$$\delta = \frac{1}{\sqrt{\pi f \mu \gamma}} \tag{5.4}$$

where μ is the magnetic permeability of wire material , γ is the conductivity of wire material at a certain temperature.

$$F_R = y \times \left[M(y) + \frac{2}{3} \times \left(m^2 - 1\right) \times D(y) \right] \tag{5.5}$$

where $y = h_\text{c}/\delta$, h_c is the conductor thickness and m is the number of winding layers. function M(y) and D(y) are expressed as,

$$\begin{cases} M(y) = \frac{\sinh(2y)+\sin(2y)}{\cosh(2y)-\cos(2y)} \\ D(y) = \frac{\sinh(y)-\sin(y)}{\cosh(y)+\cos(y)} \end{cases} \tag{5.6}$$

Taking the loss modeling of the buck converter inductor L_1 as an example, the time-varying inductor current consists of several AC components and a DC component. For the triangular periodic current going through the buck converter inductor $i_{L1}(t)$, $i_{L1}(t)$ is the superimposed of the current $i_{\mathrm{n}}(t)$ on the DC component I_{DC}.

$$\begin{aligned} i_L(t) &= I_{\mathrm{DC}} + i_{\mathrm{n}}(t) \\ &= I_{\mathrm{DC}} + \sqrt{2}\sum_{n=0}^{\infty} I_{\mathrm{n}} \sin\left(n\omega t + \phi_{\mathrm{n}}\right) \\ &= I_{L1} + \sqrt{2}\sum_{n=1,3\ldots}^{\infty} \frac{(-1)^{(n-1)/2}}{n^2}\frac{8}{\pi^2}\sin\left(n\omega t - \frac{n\pi}{2}\right) \end{aligned} \tag{5.7}$$

where I_{L1} is the DC current component of inductor current. ω is 6 times of the grid frequency, where $\omega = 2\pi f_{\mathrm{g}}$.

As the inductor current is time-varying and non-sinusoidal, Improved Generalized Steinmetz Equation (IGSE) is used for calculating the core loss [44].

$$P_{L,\mathrm{core}} = P_v \cdot V \tag{5.8}$$

$$P_v = \frac{1}{T}\int_0^T k_{\mathrm{i}} \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{5.9}$$

where ΔB is the peak-to-peak flux density and

$$k_{\mathrm{i}} = \frac{\gamma}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} \mathrm{d}\theta} \tag{5.10}$$

where γ, α and β are the Steinmetz parameters modeling the core losses for sinusoidal excitation. For the inductor design the chosen core material is the MAGNETICS MPP toroid.

The loss of the input filter inductor L_{f} is calculated with the same method, but due to the high-frequency filtering functionality of the input filter the winding losses are mainly dominated by the DC component and the relatively low AC frequency components.

The loss of the output filter inductor L_{FB} of partial power full bridge is calculated with the same method. Unlike the current of input filter inductor $i_{L\mathrm{f}}$ and buck inductor i_{L_1}, the DC current component of full bridge inductor take the majority and a small part of AC current component with the frequency of $2 \cdot f_{\mathrm{s}}$.

The mitigation of the high-frequency AC component will also impact positively the core losses.

5.2 CAPACITOR LOSS

The loss of capacitor C_{f}, C_1 and C_{FB} are relatively smaller, compared with other system loss. The major loss of capacitor is dielectric loss, which can be expressed as

$$P_C = I_{c,\text{rms}}^2 \cdot R_{\text{esr}} \tag{5.11}$$

where R_{esr} is the equivalent series resistance of the capacitor, and $I_{c,\text{rms}}$ is the rms value of the current flowing through the capacitor.

5.3 TRANSFORMER LOSS

5.3.1 Three Phase Transformer

The loss of the three phase three winding transformer $P_{3\text{pT}}$ in the AC side consists of copper winding loss $P_{3\text{pT,winding}}$ and core loss $P_{3\text{pT,core}}$, which can be expressed as

$$P_{3\text{pT}} = P_{3\text{pT,winding}} + P_{3\text{pT,core}} \tag{5.12}$$

$$P_{3\text{pT,winding}} = P_{\text{pri,winding}} + P_{\text{sec,ter,winding}} \tag{5.13}$$

For the winding loss in the primary side, where the conduction current is an sinusoidal waveform, could be expressed as,

$$P_{\text{pri,winding}} = R_{\text{pri,AC}} \cdot I_{\text{pri,rms}}^2 \tag{5.14}$$

where $R_{\text{pri,AC}}$ is the equivalent resistance of the transformer winding considering the proximity and skin effects. $I_{\text{pri,rms}}$ is the rms current flowing through the primary side winding.

The currents at the secondary and tertiary sides is not grid-frequency sinusoidal as the primary side, so winding loss of these two windings are calculated as (5.2).

$$\begin{aligned} P_{\text{sec,ter,winding}} &= P_{\text{DC}} + P_{\text{AC}} \\ &= R_{\text{DC}} I_{\text{DC}}^2 + \sum_{n=1}^{\infty} R_{\text{ACn}} I_{\text{n}}^2 \end{aligned} \tag{5.15}$$

Core loss of three phase three winding transformer is calculated as,

$$P_{3\text{pT,core}} = P_w \cdot W_{\text{core}} \tag{5.16}$$

where W_{core} is the weight of the transformer core and P_w is the power loss of core per kg. As the current waveform of the primary side is close to a sinusoidal, General Steinmetz equation(GSE) (5.17) methods can be used [**transformerloss**], expressed as,

$$P_w = \gamma_{\text{T}} \cdot f^{\alpha_{\text{T}}} \cdot B^{\beta_{\text{T}}} \tag{5.17}$$

where 3% Silicon Steel Core Material is chosen as the core material, the parameter γ_{T}, α_{T} and β_{T} can be derived from the datasheet [43].

5.3.2 Full Bridge Transformer

The loss of the full bridge transformer is calculated as three phase transformer and expressed as,

$$P_{\text{FBT}} = P_{\text{FBT,winding}} + P_{\text{FBT,core}} \tag{5.18}$$

$$P_{\text{FBT,winding}} = P_{\text{pri,winding}} + P_{\text{sec,winding}} \tag{5.19}$$

Conduction current in the primary side winding and secondary side winding is not sinusoidal shape, but trapezium shape, as shown in Fig. 4.8. Trapezium shape can be expressed as the sum of DC component and AC components. The winding loss is expressed the same as (5.15),

$$\begin{aligned} P_{\text{pri,sec,winding}} &= P_{\text{DC}} + P_{\text{AC}} \\ &= R_{\text{DC}} I_{\text{DC}}^2 + \sum_{n=1}^{\infty} R_{\text{ACn}} I_{\text{n}}^2 \end{aligned} \tag{5.20}$$

As the transformer current is non-sinusoidal, Improved Generalized Steinmetz Equation (IGSE) is used for calculating the core loss.

$$P_{\text{FBT,core}} = P_w \cdot W_{\text{core}} \tag{5.21}$$

$$P_w = \frac{1}{T} \int_0^T k_{\text{i}} \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{5.22}$$

where k_{i} is the expressed as (5.10). N87 is selected as the core material and the parameters can be derived from curve fitting.

5.4 SEMICONDUCTOR LOSS

The loss across the diode consists of conduction loss and reverse recovery loss. The high frequency switching power circuit can use Silicon Carbide (SiC) Schottky diodes to avoid reverse recovery loss. Thus, the SiC diode GD25MPS17H is chosen as the buck diodes. The diode bridge VUO52-16NO1 is selected and is operated in low frequency. Compared with conduction loss, reverse recovery loss of the diode bridge is relatively small in lower frequency, which is then neglected. For the output side of the full bridge converter, SIC schotty Diode MSCDC50H1701AG are selected as the diode bridge.

According to the on-state characteristic, the equivalent circuit of the diode can be seen as a series connected V_{f} and R_{d}. Thus, the conduction loss can be expressed as [38]

$$\begin{aligned} P_{\text{d}} &= P_{\text{d,con}} + P_{\text{d,rev}} \approx P_{\text{d,con}} \\ &= V_{\text{f}} \cdot I_{\text{d,avg}} + R_{\text{d}} \cdot I_{\text{d,rms}}^2 \end{aligned} \tag{5.23}$$

where V_f is the forward voltage, R_d is the effective resistance of the diode, $I_{d,avg}$ and $I_{d,rms}$ are the average and rms values of the diode forward current, respectively.

The SIC MOSFET G3R20MT17N is selected as switching semiconductor of the buck converter. The losses in the power semiconductors are mainly two parts: the switching and conduction losses, and it can be expressed as

$$P_s = P_{con} + P_{sw} \tag{5.24}$$

The conduction loss model of the MOSFET is the same as for the diode, which can be expressed as

$$P_{con} = V_s \cdot I_{s,avg} + R_s \cdot I_{s,rms}^2 \tag{5.25}$$

where V_s is the voltage drop across the MOSFET when it is conducting, R_s is the effective resistance of the MOSFET, $I_{s,avg}$ and $I_{s,rms}$ are the average and rms values of the MOSFET current, respectively.

The switching loss is a function of the switching energies $E_{on,off}$ [38] and is scaled with the voltage ratio of the switching voltage V_{sw} and datasheet reference voltage V_{ref}.

$$P_{sw} = \frac{f_s V_{sw}}{2\pi V_{ref}} \int_0^{2\pi} E_{on,off}\, d\omega t \tag{5.26}$$

According to the switching energy loss characteristic of the SIC MOSFET datasheet, the switching energies $E_{on,off}$ can be curved fitting as a quadratic function of the switched current $i_s(t)$, as given by (5.27). $i_s(t)$ is also a triangular current waveform as $i_L(t)$.

$$E_{on,off}(t) = a_{1,2} i_s(t)^2 + b_{1,2} i_s(t) + c_{1,2} \tag{5.27}$$

where a_1, b_1, c_1 are the curve fitting second order coefficients for E_{on} and a_2, b_2, c_2 are the coefficients for E_{off}.

For full bridge converter, The SIC MOSFET IFF6MR12W2M1B11 is selected as the switching semiconductor. There is no turn-on loss of the switching loss, because phase shift operation can realize Zero voltage switching (ZVS).

$$P_{sw} = \frac{f_{sFB} V_{sw}}{2\pi V_{ref}} \int_0^{2\pi} E_{off} d\omega t \tag{5.28}$$

The equation of turn-off switching loss and conduction loss are the same as (5.27) and (5.25).

5.5 LOSS DISTRIBUTION

5.5.1 Mode 1

In Mode 1, the partial power full bridge converter is not included in the system. Fig. 5.1 shows the loss breakdown of the system under Mode 1 with the setting of Table. 5.1.

In this setting, the system efficiency is 98.73%. The losses of the passive components L_1, L_f C_1 and C_f take 9% of the total loss. The losses of the Semiconductors (buck converter (34%) and rectifier diode bridges (24%)) take 58%, while the transformer contributes to 34 % of the total losses.

Table 5.1: System parameters of Mode 1

Parameters (Mode 1)	Value	Unit
Grid Voltage (line-to-neutral)	220	V
Grid Frequency f_g	50	Hz
System output Power	100	kW
Transformer winding ratio k	1.8	
Switching Frequency f_s	24	kHz
Output dc voltage	800	V
Input Filter Inductor L_f	0.03	mH
Input Filter Capacitor C_f	15	µF
Input Filter Damping Resistor R_f	5	Ω
Buck Inductor L_1	0.1	mH
Buck Capacitor C_1	20	µF
Power Factor PF @ Full load	0.999	
THD_i @ Full load	1.36	%
Efficiency η @ Full load	98.73	%

5.5.2 Mode 2

In Mode 2, the partial power full bridge converter is included in the system. Parameters setting of the part of Mode 1 are the same, PPP DC/DC part setting are shown as Table . 5.2. Fig. 5.2 shows loss breakdown of the system under Mode 2.

In this setting, the system efficiency is 98.16%. Compared with Mode 1, efficiency of Mode 2 are decreased because of

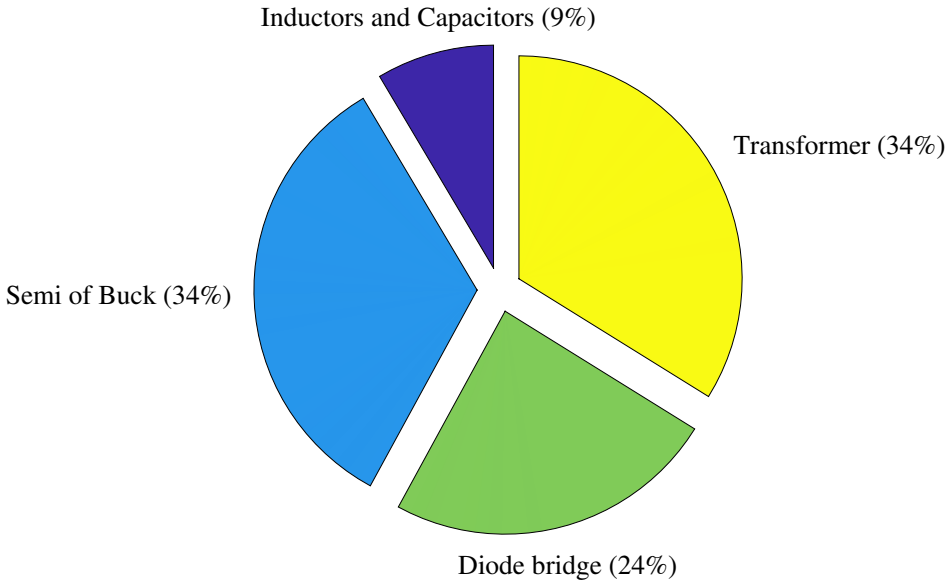


Figure 5.1: The proportion of losses in each part of the system in Mode 1

Table 5.2: System parameters of Mode 2

Parameters (DC/DC Mode 2)	**Value**	**Unit**
FB Transformer winding ratio $N_p : N_s$	39:40	
Output dc voltage	1600	V
Switching Frequency of FB f_{sFB}	16	kHz
FB Inductor L_f	0.03	mH
FB Capacitor C_f	15	µF
Efficiency η @ Full load	98.16	%

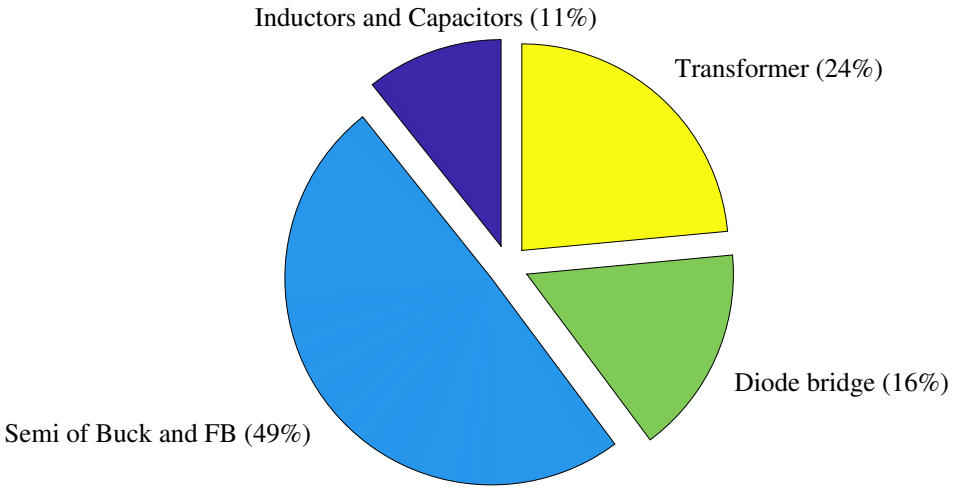


Figure 5.2: The proportion of losses in each part of the system in Mode 2

6 SIMULATION RESULTS

6.1 SIMULATION MODEL

In order to verify theoretical analyses and parameters setting, simulation model of the proposed two-level ev fast charging system was developed in the PLECS environment and tested, as shown in Fig. 6.1. Three subsystems are buck control, mode switch control and phase shift full bridge control.

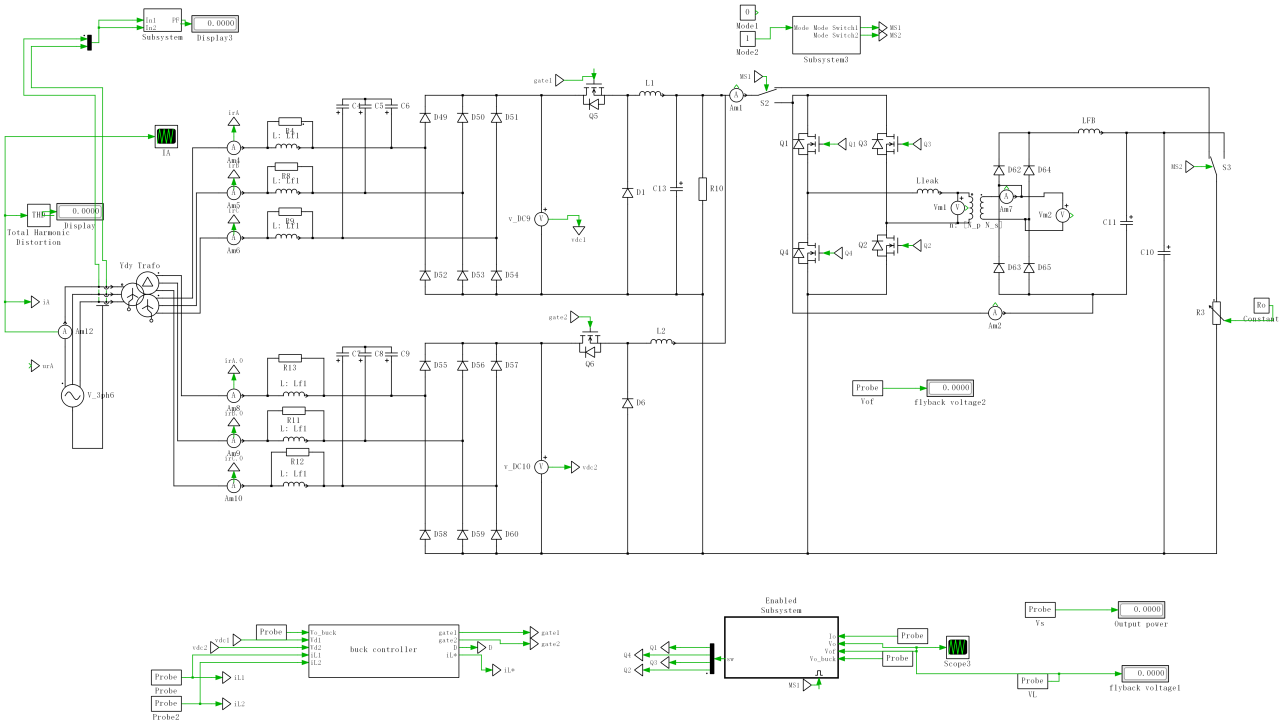


Figure 6.1: Simulation model of proposed EV fast charger

With the control setting as Fig. 3.4, Simulation results of the inductor current, input voltage and duty cycle of the upper buck PFC circuit are shown in Fig. 6.2. Compare with the expected waveform shown in Fig. 3.5, Inductor current can well trace the triangular reference current waveform, while there are some fluctuations showing in the output voltage of the diode bridge. The fluctuations are caused by resonate of inductor and capacitor of input filter when the current change from increase to decrease at the peak. Besides, the turn ratio of three phases three windings transformer is set to have high duty cycle to have less losses.

With the phase shift control setting as Fig. 4.8, the full bridge gate signals of switches, current and voltage waveform are shown as Fig. 6.3, which are expected as Fig. 4.6.

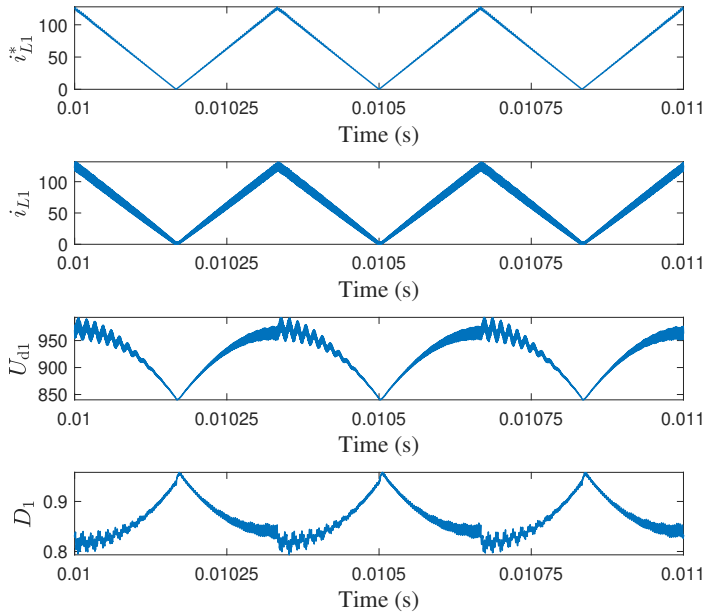


Figure 6.2: Simulation result of current, voltage and duty cycle of buck PFC circuit

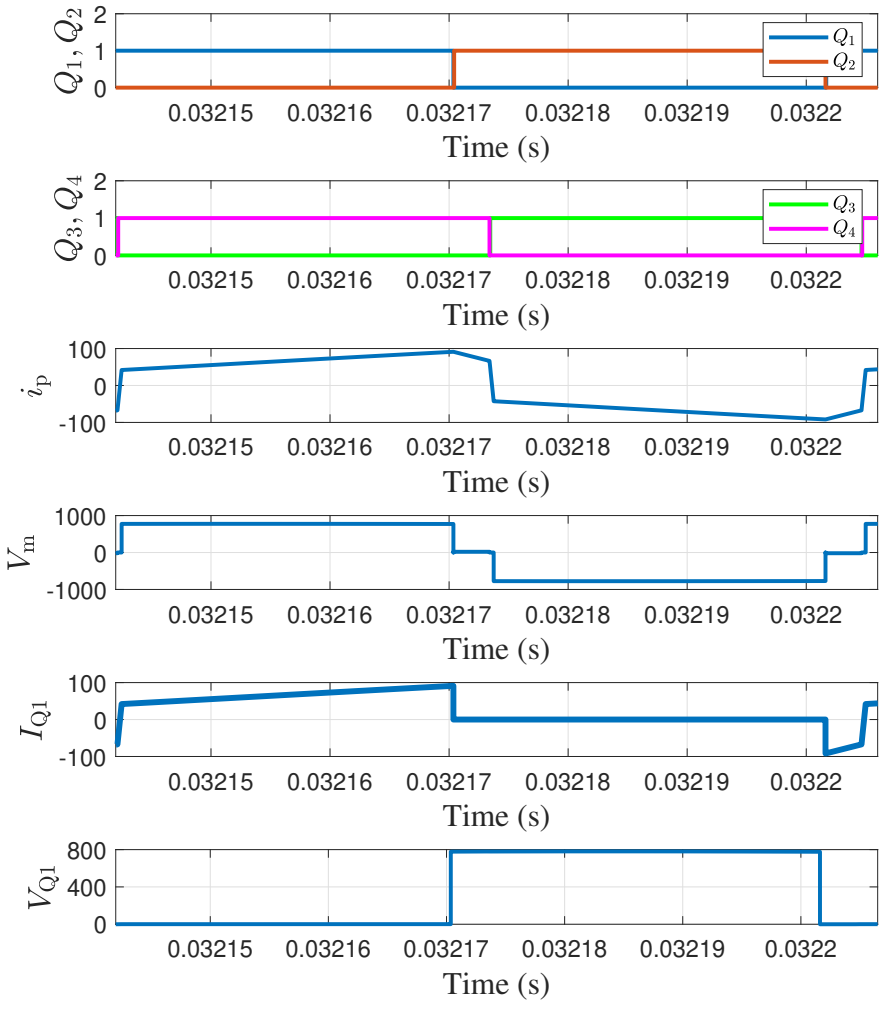


Figure 6.3: Gate Signals, Current and Voltage of Full Bridge

6.2 INPUT CURRENT SHAPE

The current of the MOSFET, which is also the output current of the diode bridge, is controlled to have a triangular shape, shown in Fig. 6.4. In Fig. 6.4(a) shows the current waveform of the upper SIC MOSEFT Q1 and (b) shows the current waveform of the lower SIC MOSEFT Q2. They are discontinuous because of the switching of MOSFET.

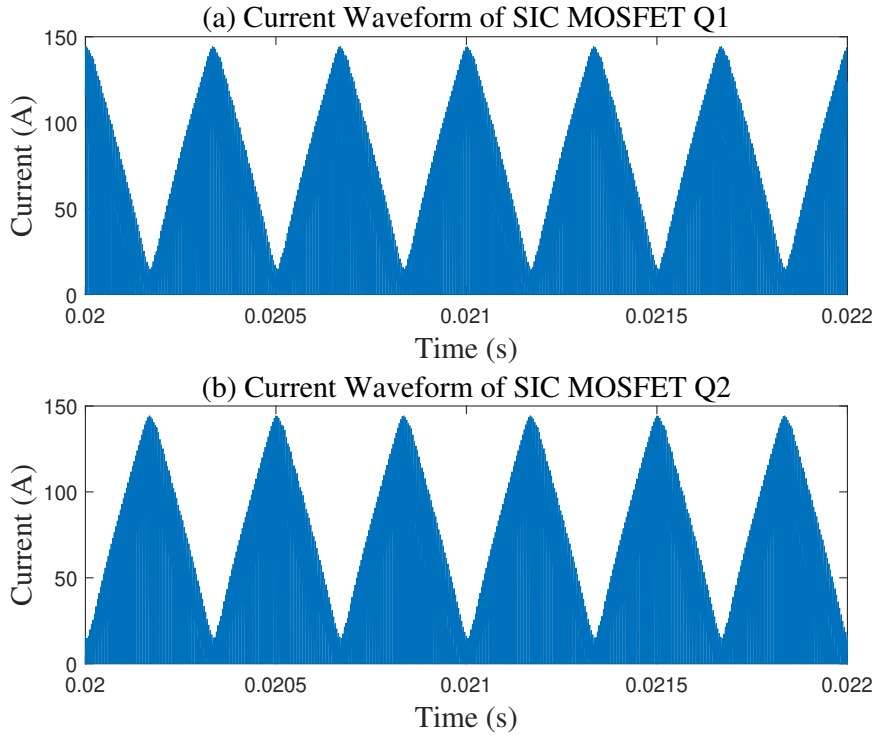


Figure 6.4: Current waveform across the active switches of the Buck converter.

Fig. 6.6 shows the 3 phase ac current in the secondary side and tertiary side of the transformer. We can see that the 3 phase current are periodic triangular.

Fig. 6.6 shows the input current waveform of phase A i_{A}, the secondary side current waveform of phase A i_{a1}, and the tertiary side current waveform of phase A i_{a1} and phase B i_{b2}. The transformer winding turns ratio k here is set to 1. As Fig. 6.6 shown, after the composition of the current component, the input current waveform is closed to sinusoidal. This demonstrates the feasibility of the triangular current shaping method with the buck converter circuit.

The system is designed to meet the current harmonic limits of the IEEE 519-2014 standard. According to this standard [18], the recommended current distortion limits for systems nominally rated from 120 V up to 69 kV is of interest for this paper studied application.

From simulation result at full load (100 kW), the total harmonic distortion (THD) of the system, which is the same as the Total demand distortion (TDD) under full load, is measured as 1.36% and conforms to the standard limits (5%). Power factor is measured as 0.999, which conforms to the standard

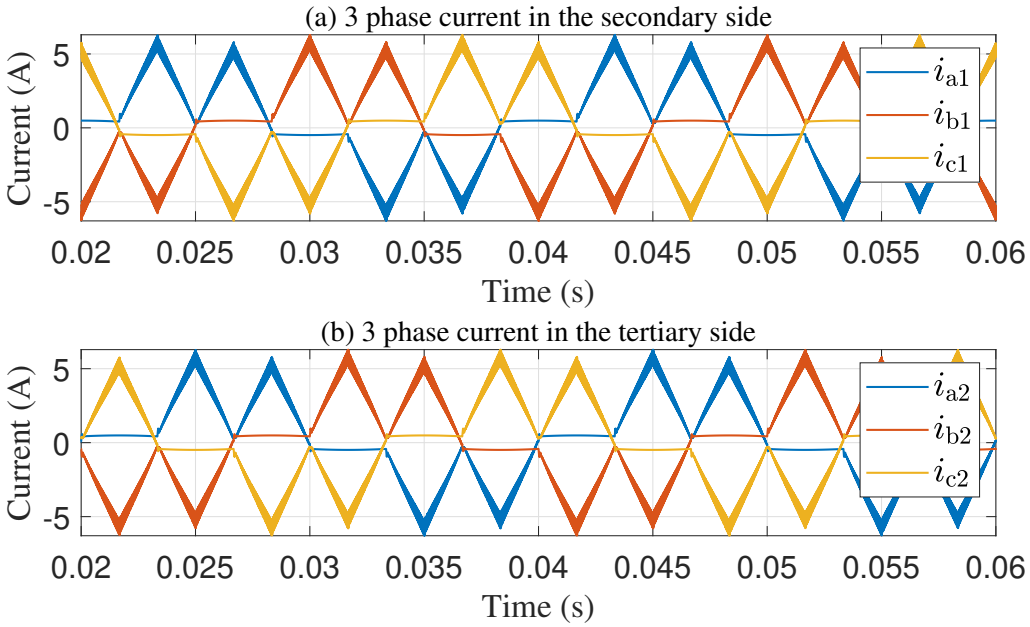


Figure 6.5: 3 phase current in the secondary side and tertiary side

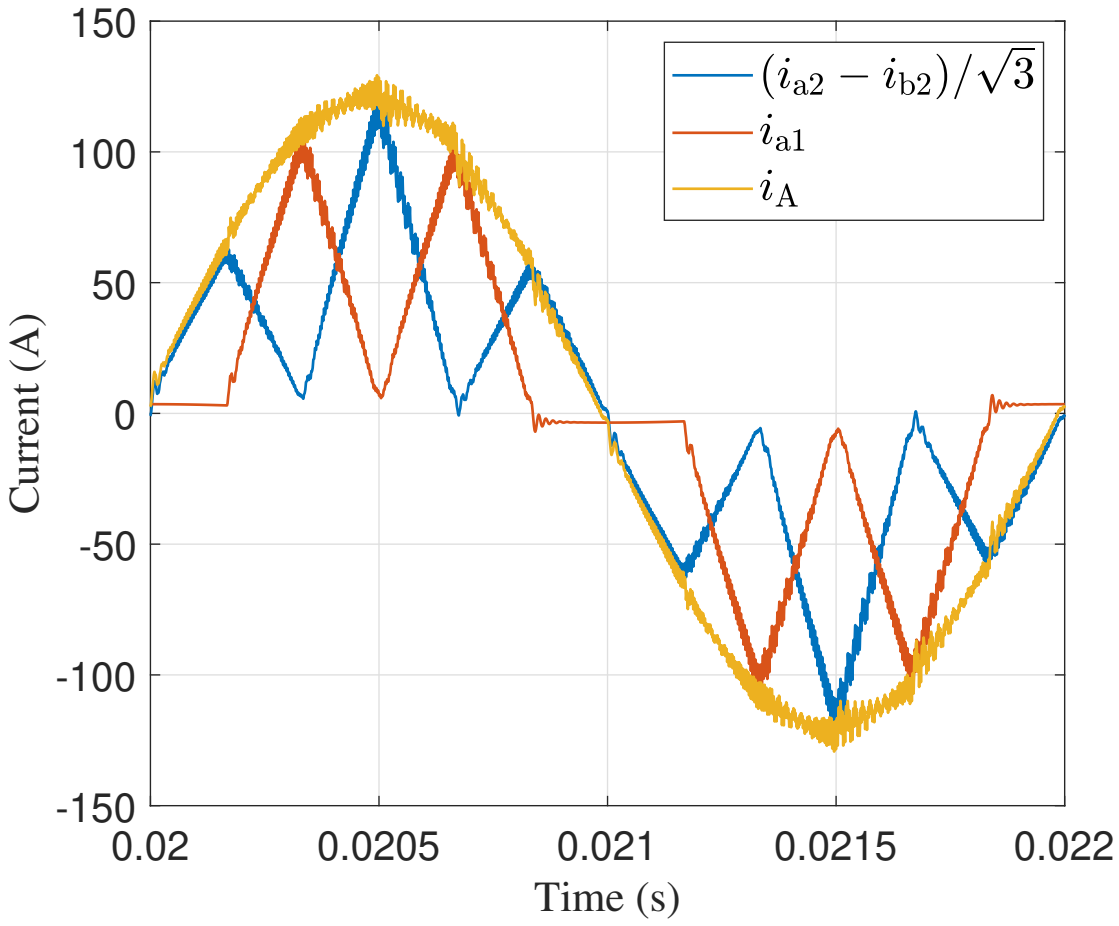


Figure 6.6: Input current waveform.

(> 0.99). The individual harmonic order limits of the strictest standards $\frac{I_{SC}}{I_L} < 20$ and simulation result of the system are presented in Fig. 6.7. As Fig. 6.7 shown, all the simulated current harmonics conforms to the considered standard.

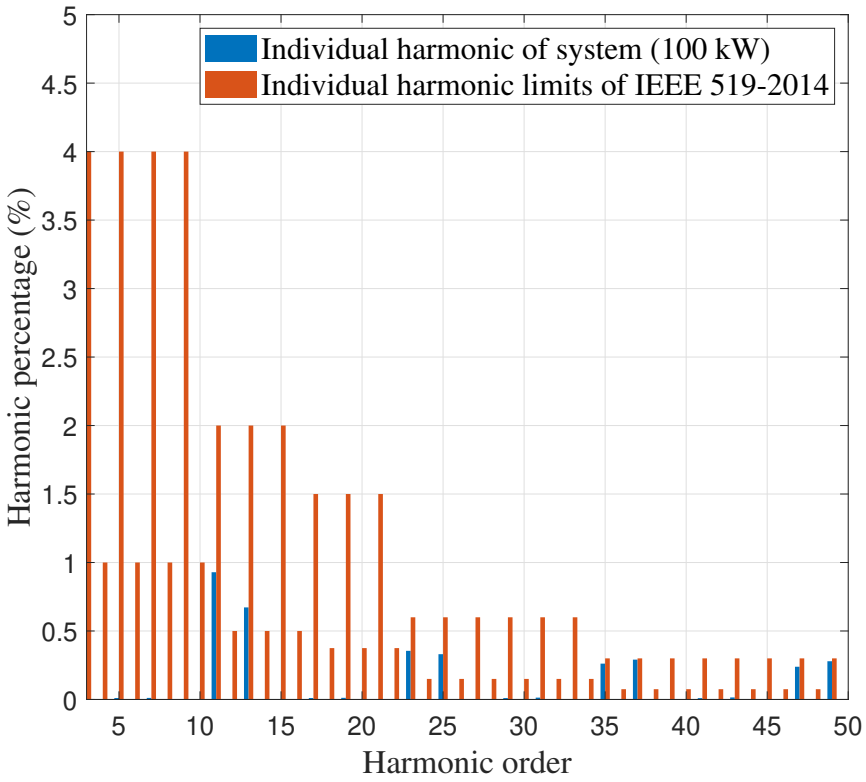


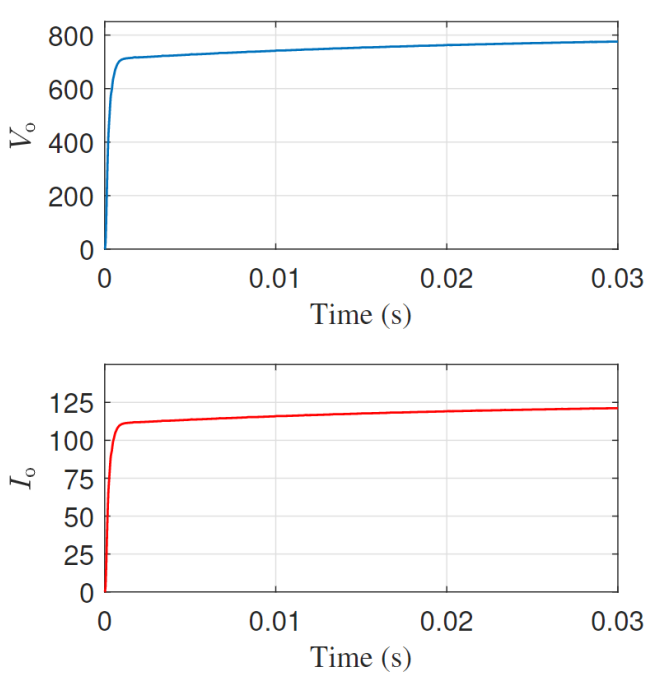
Figure 6.7: Current Individual Harmonic Distortion Limits and System Simulation Result of $3 \leq h \leq 50$.

6.3 OUTPUT VOLTAGE RESPONSE

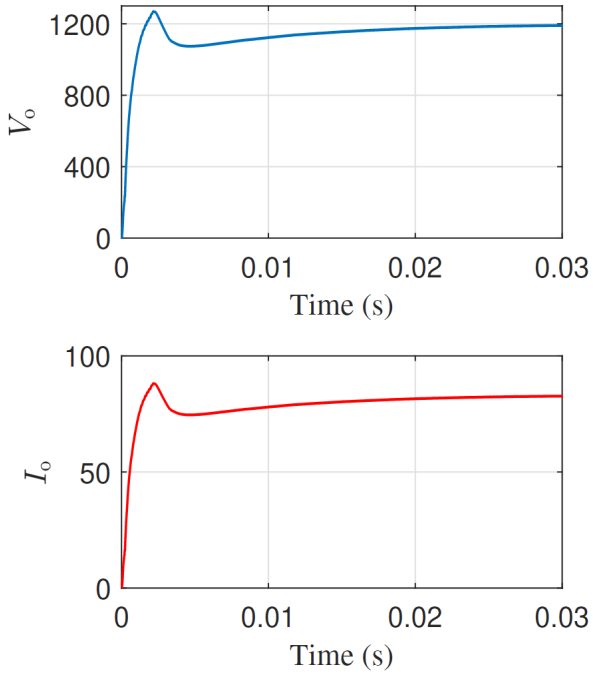
Fig. 6.8 (a) shows the output voltage and current in Mode 1 with 800V voltage setting. In Mode 1, Partial Power Phase shift full bridge is not included in the EV charging system. Fig. 6.8 (b) shows the output voltage and current in Mode 2 with 1200V voltage setting. Fig. 6.8 (c) shows the output voltage and current changed from Mode 1 to Mode 2. The power of the simulation of two mode are 100 kW.

From the simulation results, this EV fast charger can normally run alone and provide expected regulated voltage in Mode 1 and 2. Beside, it can also switch to different mode with the Mode switches and work flexibly for different voltage applications.

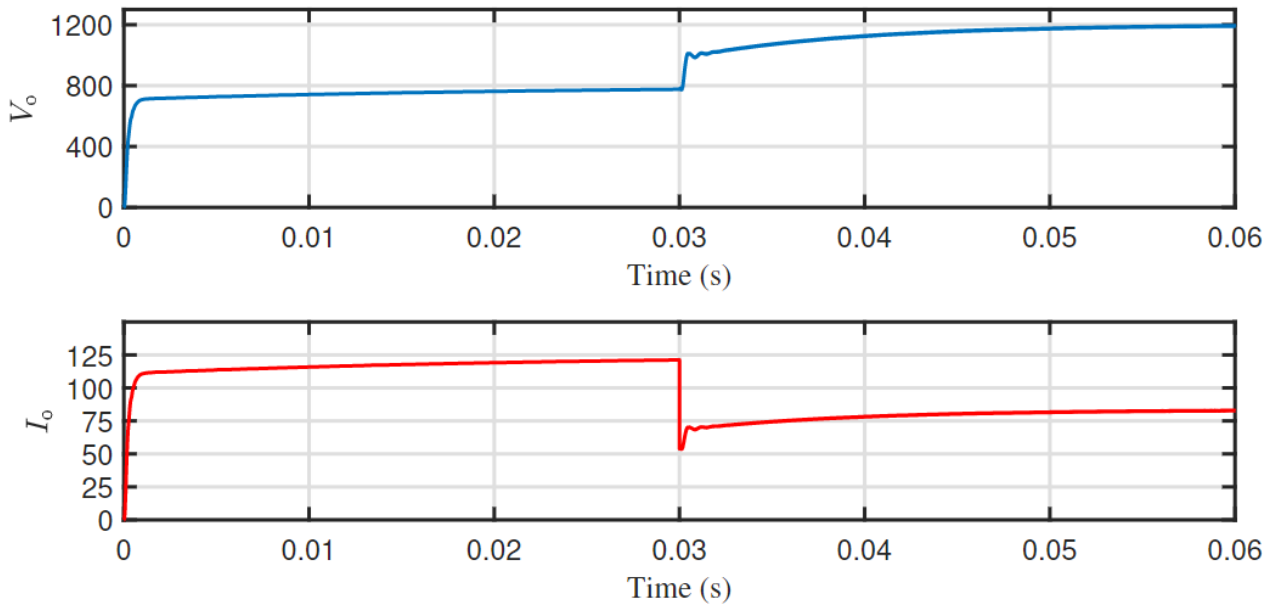
Fig. 6.9 shows the output voltage and current with battery charging modeling in Mode 2. The battery modeling was firstly in CC charging mode and then in CV charging mode.



(a) Mode 1



(b) Mode 2



(c) From Mode 1 to Mode 2

Figure 6.8: Output Voltage and Current of Two Modes

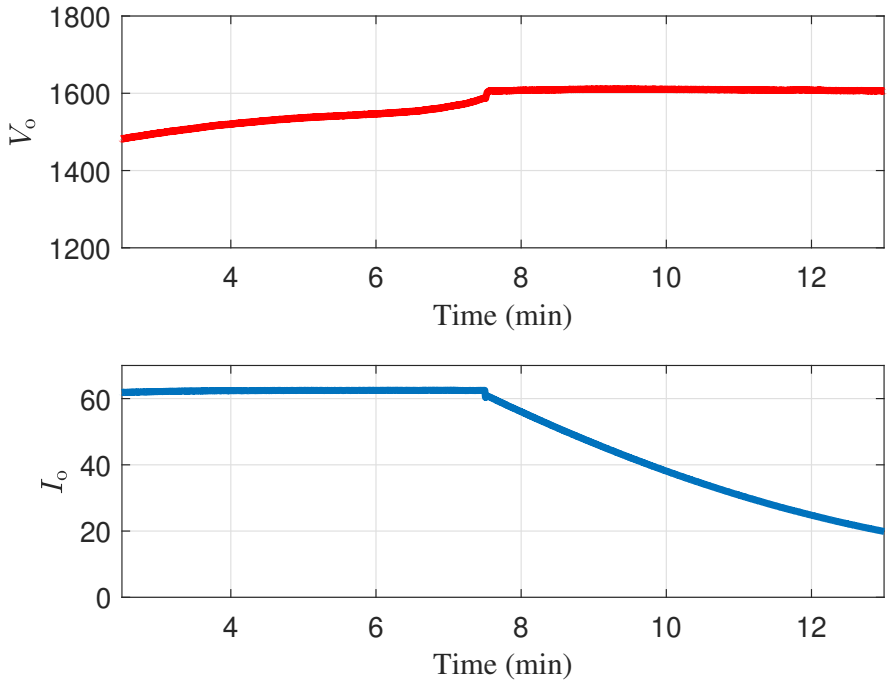


Figure 6.9: Output Voltage and Current of CCCV Charging

Fig. 6.10 shows partial power processed by the full bridge converter and full power with battery charging modeling in Mode 2. Processed power ratio are closed to 0.5 during charging.

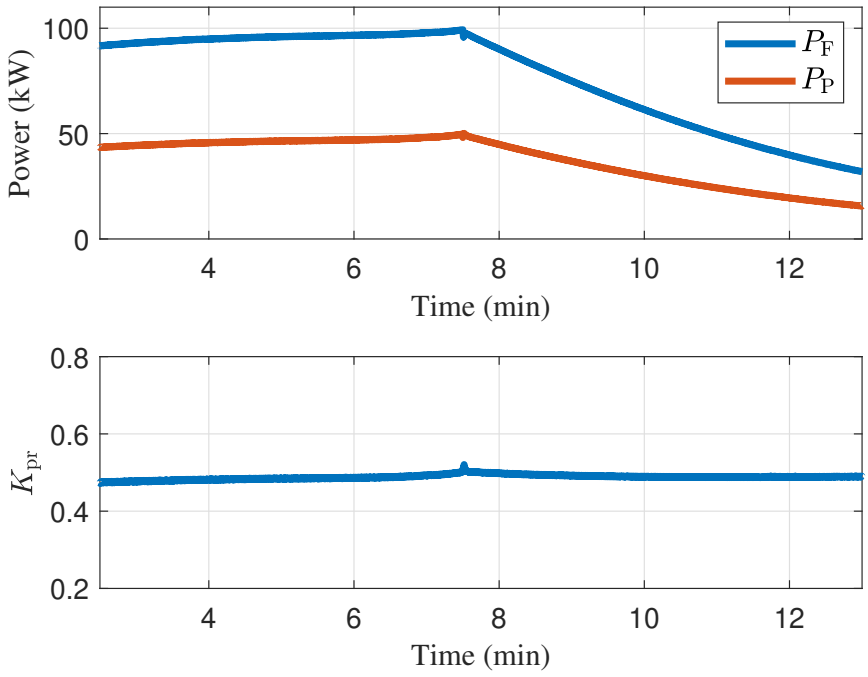


Figure 6.10: Processed Power, Full Power and Processed Power Ratio

7 EXPERIMENTAL REALIZATION

7.1 EQUIPMENT SETUP

In order to varify the triangular current shaping method for harmonic reduction with buck circuit and corroborating the simulation results from PLECS software, a prototype of 1.5 kW was developed and analyzed in the laboratory, as shown in Fig. 7.1 Fig. 7.3, and Fig. 7.2.

Due to the time constraints, the prototype was set up with existing equipment in the laboratory. With only one buck circuit was available, a six-pulse rectifier with buck circuit and input filter was set up. Corresponding experiment set up topology are shown in Fig. 7.4. In Table. 7.1, the specifications of the rectifier prototype are presented.

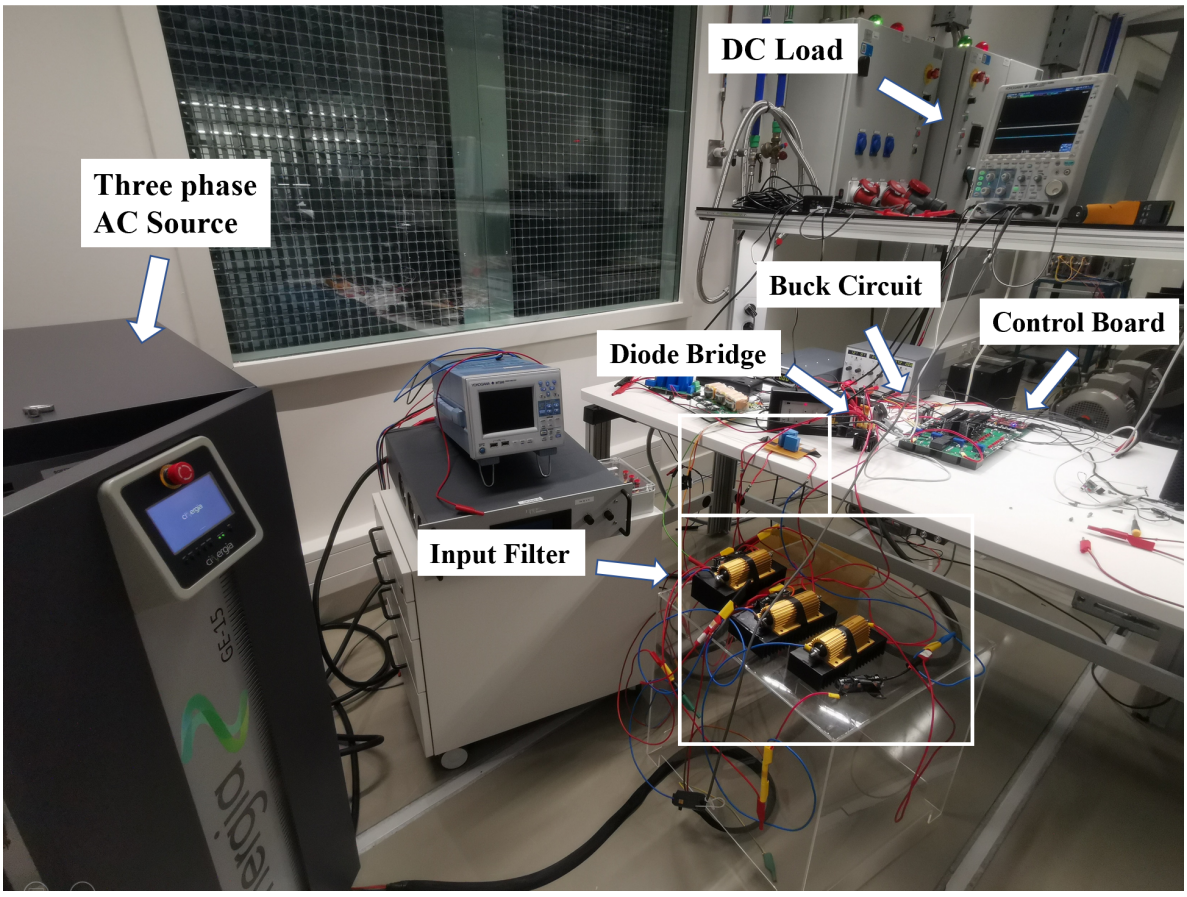


Figure 7.1: Experimental Setup Overview

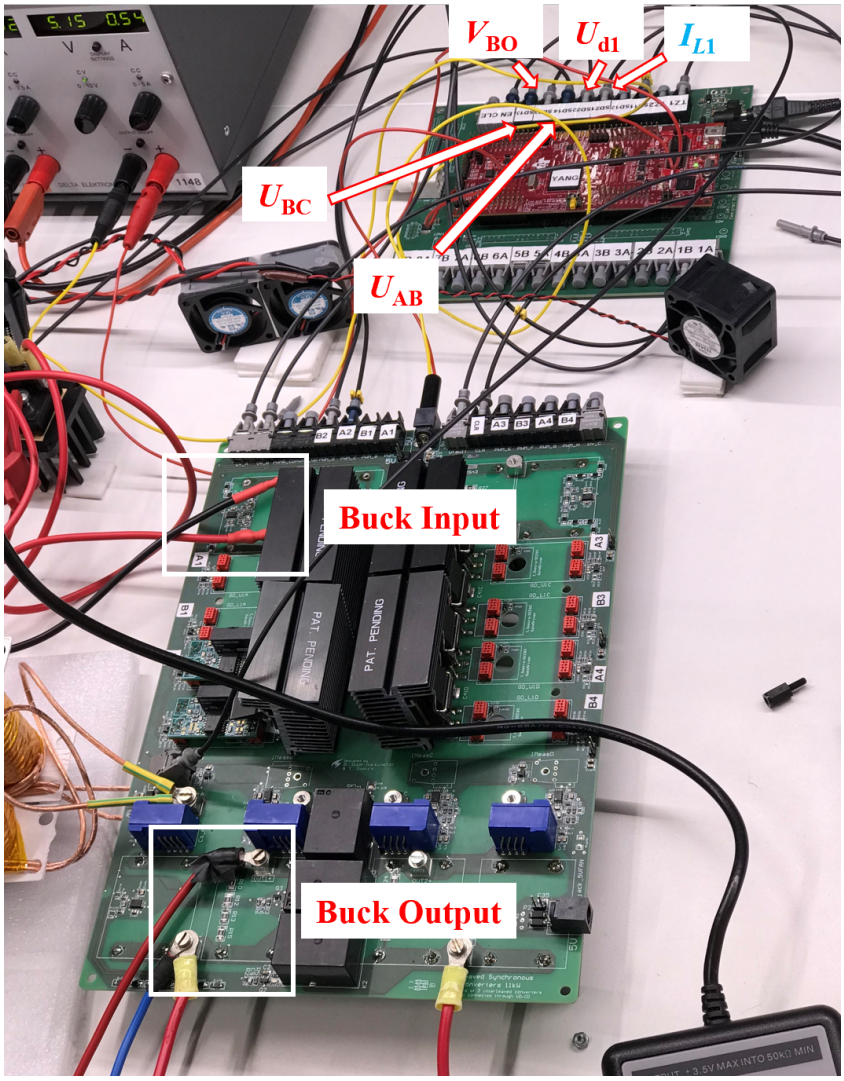


Figure 7.2: Control Board and Buck Circuit

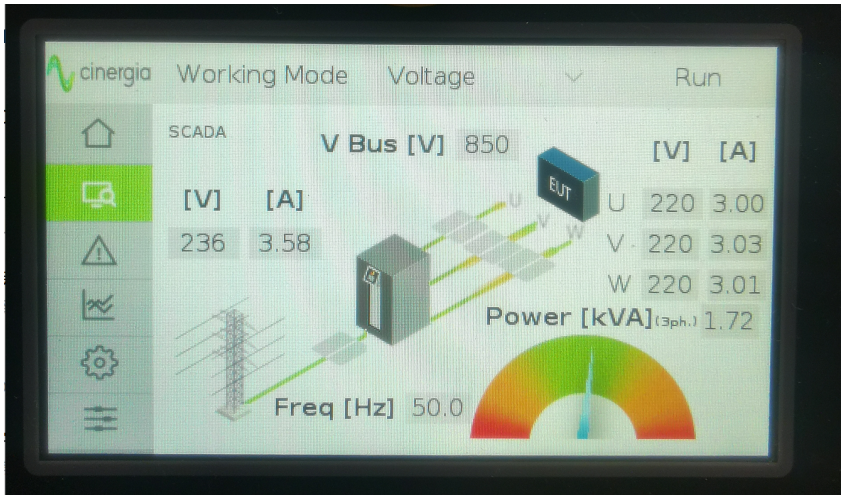


Figure 7.3: Cinergia setting of AC source

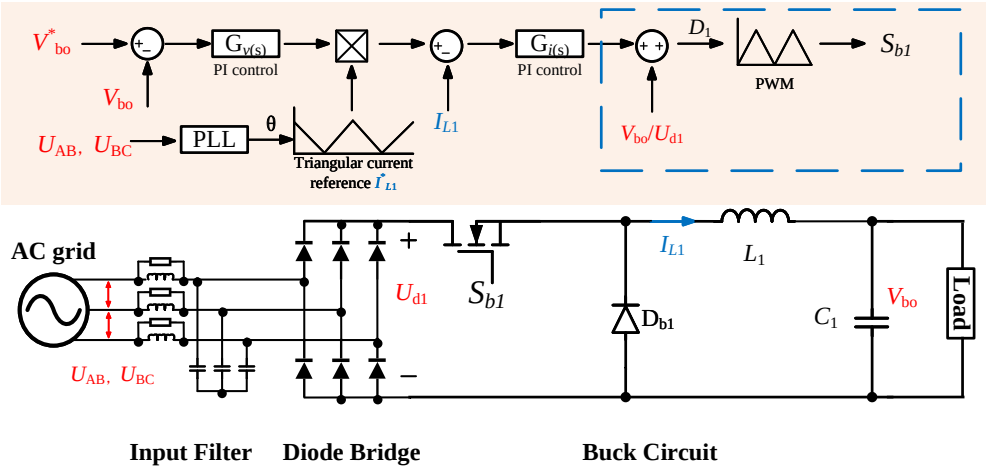


Figure 7.4: Experimental Setup Topology and Control Scheme

Table 7.1: Prototype parameters

Parameters	Value	Unit
Input Line Voltage	220	V_{rms}
DC Load as resistor	60	Ω
System output Power	1.5	kW
Switching Frequency f_s	50	kHz
Output dc voltage	300	V
Input Filter Inductor L_f	0.047	mH
Input Filter Capacitor C_f	4.7	µF
Input Filter Damping Resistor R_f	22	Ω
Buck Inductor L_1	0.1	mH
Buck Capacitor C_1	600	µF
Diode Bridge	VS-36MT160	
SIC MOSFET	IMW120R060M1	

7.2 EXPERIMENTAL RESULTS

Fig. 7.5 shows the signals of the buck output voltage, diode bridge output voltage, Phase A current and buck inductor current under fix duty cycle. In Fig. 7.5, the Phase A current was not discontinuous, demonstrating that the input filter worked well. Under fix duty cycle, inductor current presented an approximate triangular waveform. However, the current shape of inductor current was not standard regular triangle. To achieved this, inner current closed loop control needs to be applied to have inductor current keep track of triangular current reference. The triangular current reference was generated by the PLL successfully, as shown in Fig. 7.6.

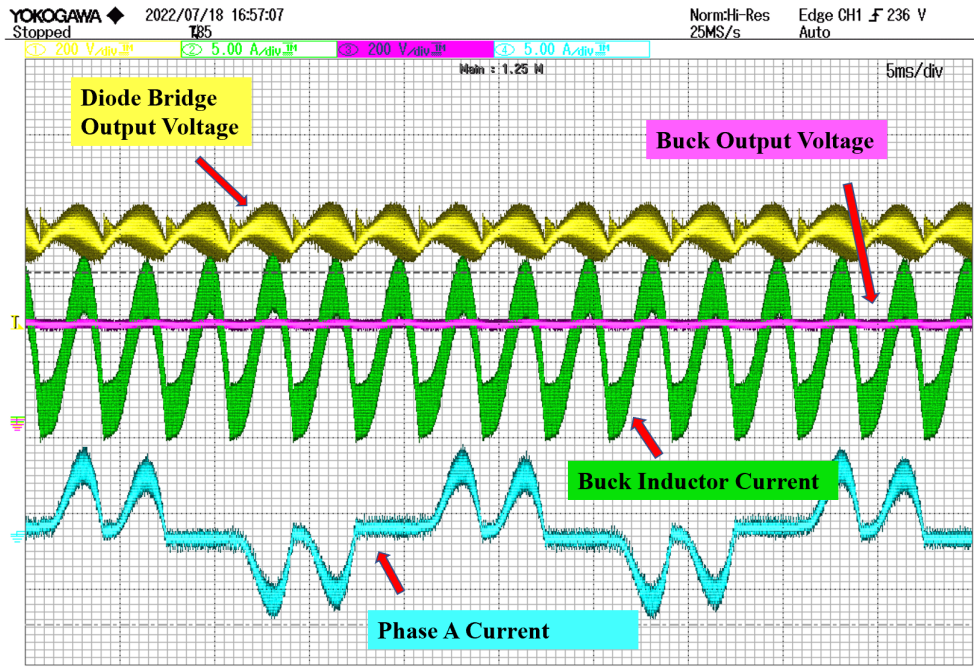


Figure 7.5: Experimental Results of Fix Duty Cycle

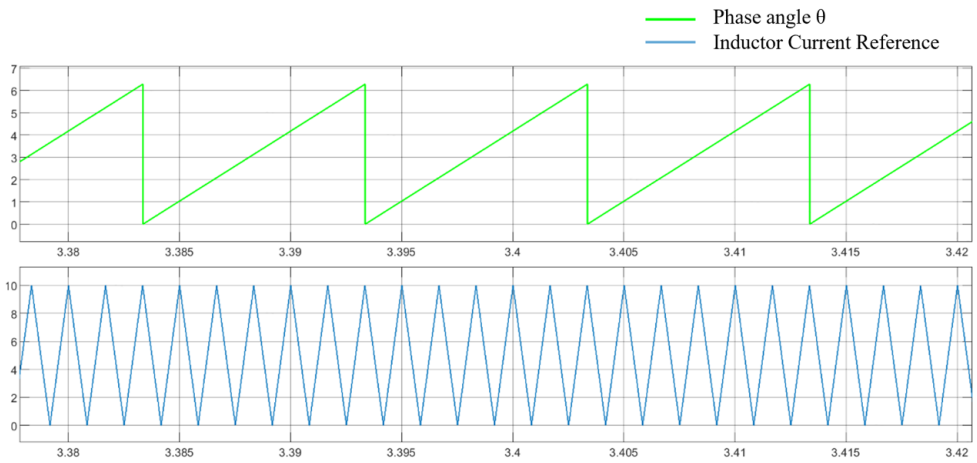


Figure 7.6: Generated Triangular Current Reference

Fig. 7.7 shows the signals of the buck output voltage, diode bridge output voltage, Phase A current and buck inductor current under open loop control. The open loop control refers to the control within the blue border in Fig. 7.4. Duty cycle of open loop was changed with the input voltage of the buck circuit which was the six-pulse output voltage of diode bridge.

Fig. 7.8 shows the signals of the buck output voltage, diode bridge output voltage, Phase A current and buck inductor current under voltage and current closed loop control. The inductor current is almost regular triangular. Noted that the slight difference was cause by the current sensor. The current sensor did not work properly as expected and it needed to be re-calibration often during the experiment. Compared with the open loop control and fix duty control, the inductor current waveform of closed loop control could keep track of the triangular current reference generated by the PLL and the

output voltage could be stable at 300V. This result verified that the voltage and current closed loop control work properly.

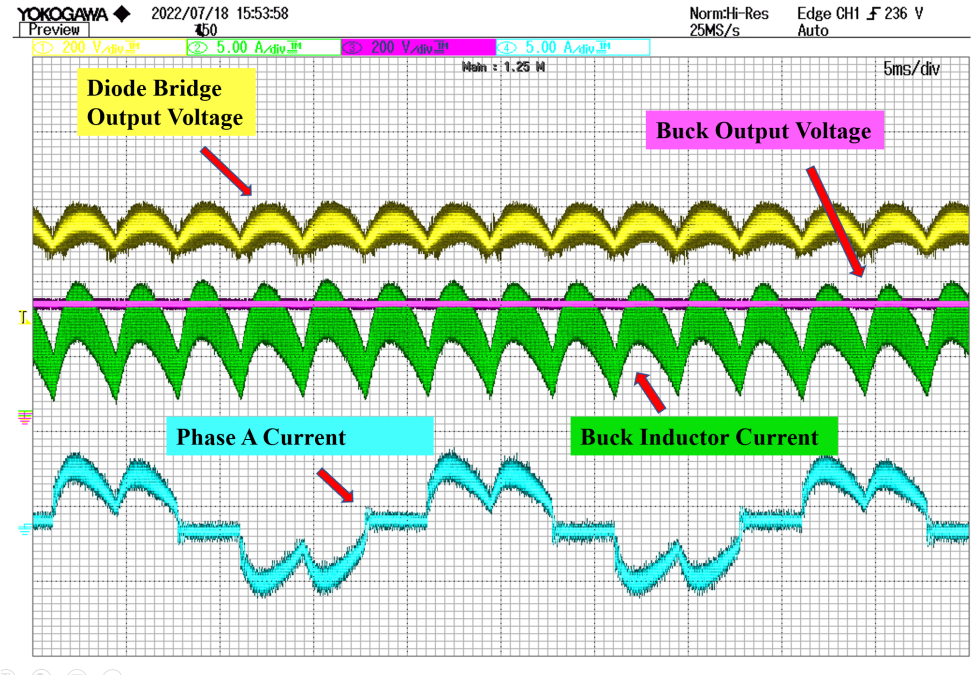


Figure 7.7: Experimental Results of open loop control

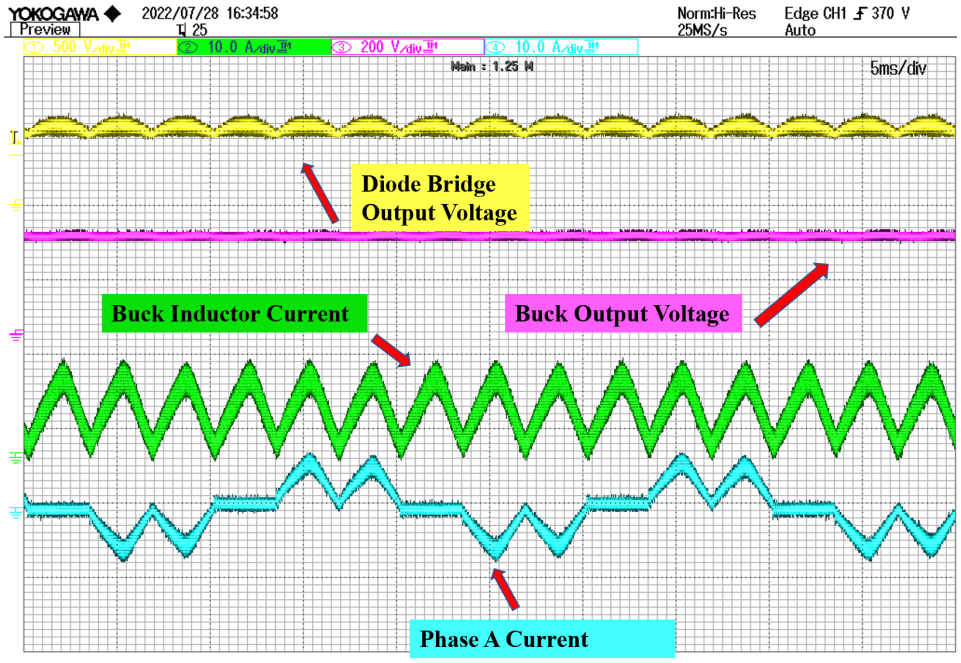


Figure 7.8: Experimental Results of voltage and current closed loop control

8 CONCLUSION

This thesis focused on the ultra-fast DC fast charger for 800 V and 1200-1600 V battery charging. The proposed topology implemented triangular current shaping method with buck circuit in 12-pulse rectifier and partial power processing technique in full bridge DC-DC converter. The main challenge of the project is to implement these two technique together to develop a high efficiency and high power DC fast charging system.

The motivations of this project are introduced in charter 1. DC fast charger is developed towards higher efficiency, output voltage range and power level. In chapter 2, the state-of-art technique are introduced in detailed, especially the AC-DC and DC-DC topology of DC fast charger, and harmonic reduction and partial power processing these two main study topic. Through the literature review, the requirements of the DC fast charger and the main study topic content, 12-pulse AC-DC rectifier and partial power processing phase shift full bridge DC-DC converter are chosen as the two-level converter for the proposed DC fast charger.

The front-end AC-DC converter of the system, including the three phase three winding transformer, input filter, 12-pulse rectifier and control, is designed in detail in chapter 3. The back-end DC-DC converter, including high frequency transformer, partial power connecting, phase shift full bridge converter and control, is designed in detail in chapter 4. Loss modeling of the whole system, such as the inductor losses, transformer losses and semiconductor losses are introduced in chapter 5. These loss modeling are described in equations and modeled in MATLAB. Loss modeling results demonstrated that the system is high efficiency, whose efficiency in two mode are up to 98.16% and 98.73%.

Simulation results in PLECS in Chapter 6 shown that the proposed topology can output expected power (100 kW) and voltage level (800, 1200-1600), reduce the harmonic with triangular current shaping method (THD 1.36% and PF 0.999) and increase the efficiency in DC-DC converter with partial power processing technique. The design and selection of components are verified by simulation and modeling results.

In Chapter 7, experiment setup, results and improvement of the AC-DC converter are introduced. The experiment results verify that the control strategy in buck circuit can make inductor current keep track of the triangular current reference and the input filter can filter out the discontinuous current from buck.

In conclusion, this thesis project develops a high power DC fast charging system for EV that implemented triangular current shaping method and partial power processing technique successfully, which complies with the standards IEEE 519-2014 and requirements of EV fast charger

There are several aspects that this thesis project can be developed in the future.

- The three phase three winding transformer is relatively large and it can be replaced by auto-transformer. this replacement would increase of power density.
- The damping method of the input filter could be change to active damping, this may improve the power quality. Furthermore, the switching frequency can be reduced to reduce switching loss.
- The design of inductor could be optimized with an Matlab script screening in different core materials, winding sizes and air gap lengths.
- For experiment, The current sensor could be replaced with a newer and more accurate one in order to have more regular triangle current waveform.

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