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Wang, Zhongkai; Choi, Minsoo; Kwon, Paul; Lee, Kyoungtae; Yin, Bozhi; Liu, Zhaokai; Park, Kwanseo; Biswas, Ayan; Du, Sijun; More Authors

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A 200Gb/s PAM-4 Transmitter with Hybrid Sub-Sampling PLL in 28nm CMOS Technology

Zhongkai Wang[1], Minsoo Choi[2], Paul Kwon[1], Kyoungtae Lee[3], Bozhi Yin[1], Zhaokai Liu[1], Kwanseo Park[1], Ayan Biswas[1], Jaeduk Han[4], Sijun Du[5], Elad Alon[1]
[1]University of California, Berkeley, CA, [2]Samsung Semiconductor, Inc., San Jose, CA,
[3]University of California, San Francisco, CA, [4]Hanyang University, Seoul, South Korea,
[5]Delft University of Technology, Delft, Netherlands, zhongkai@berkeley.edu

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Abstract

This paper presents a complete 200Gb/s PAM-4 transmitter (TX) in 28nm CMOS technology. The transmitter features a hybrid sub-sampling PLL (SSPLL) with a delta-sigma (ΔΣ) modulator, clock distribution network with flexible timing control, and data path with a hybrid 5-tap Feed-Forward Equalizer (FFE) and T-coil for bandwidth extension. The prototype chip achieves 4.69 pJ/bit efficiency, 54mV eye height, 0.27UI eye width, and 97% RLM under ~6dB channel loss at 50GHz.

Keywords: SerDes, Transmitter, Sub-sampling PLL, 28nm, CMOS.

Introduction

As the data rate of ultra-high-speed wireline IOs doubles every 3-4 years, the transmitters are required to support 200+Gb/s [1-2] data rates, which is extremely challenging for standard planar CMOS technologies and necessitates significant design effort and advanced techniques. Therefore, we present a complete 200Gb/s PAM-4 TX in 28nm CMOS technology to address the stringent bandwidth and jitter requirements by utilizing a low-jitter hybrid sub-sampling PLL with delta-sigma (ΔΣ) modulator, a clock distribution network with flexible timing control, and a high-bandwidth data path with a 5-tap FFE. The design is implemented using a generator-based flow [3] to enhance design productivity.

TX Architecture and Circuit Design

The overall TX architecture is shown in Fig. 1. The SSPLL and quadrature clock generator produce the low-jitter 4-phase 25GHz clocks, while quadrature and the duty cycle errors are corrected by the current-starving variable delays and ac-coupling resonant buffers, respectively. The buffers drive the 4-to-1 multiplexers (MUXs) in the data path and the C^{2}MOS clock dividers in the clock distribution network. The phases of the divided clocks are adjusted by the inverter-based phase interpolator and digital-controlled delay line to maximize the time margin between the retimers, 8-to-4 MUXs, and 4-to-1 MUXs across PVT corners. The data path consists of a pattern generator, 128:8 serializer, thermometer encoder, retimer, and 18 FFE driver segments. To extend the data path bandwidth, T-coils are added at the output node to isolate the MUX/driver cells and ESD diodes (supporting >1-KV HBM and 250-V CDM levels) from the capacitive loading of the resistors, pull-up current sources, and PADs. The flexible 5-tap coarse-fine FFE is adjusted to cancel the pre-and post-inter-symbol interferences (ISIs).

A. Quadrature Clock Generation: One of the main considerations related to clock generation/distribution in planar technologies is the topology of voltage-controlled oscillator (VCO) and quadrature clock generation. A quadrature VCO generating 4-phase clocks directly occupies large layout area with two coupled resonators. On the other hand, quadrature clock phases can be generated by a single VCO and clock divider operating at half rate (50GHz), which significantly increases power and complexity. In this design, a differential LC VCO at quarter-rate and quadrature clock generation circuit is selected to address the aforementioned issues. As shown in Fig. 2, a Class-C VCO with a tail inductor is used to reduce the noise contribution of the current source, which improves the phase noise by ~5dB. The VCO tank includes a 4-bit capacitor DAC, fine-tuning varactor, and proportional varactor. An injection-locked quadrature generator [4] is used to generate the 4-phase clocks.

B. Hybrid SSPLL: In Fig. 2, a hybrid SSPLL is designed based on an analog proportional path and a digital integral path. The VCO generates differential clocks with frequency between 23.6GHz and 28.6GHz and drives an ac-coupled TIA-based buffer. The buffer output is directly sampled by the sub-sampling phase detector (SSPD) and also connected to the divider chain, composed of a C^{2}MOS divider and static flip-flops (FFs) dividers. The divider output and reference clock go into the dead-zone phase detector (DZPD) for frequency locking. For the proportional path, the SSPD and DZPD drive the sub-sampling charge pump (SSCP) and the traditional charge pump (CP), respectively, whose currents are summed into the analog loop filter (LF). In the integral path, the outputs of the SSPD are sampled by a comparator, and the DZPD output is synchronized by a reference clock. These digital outputs are added together and integrated by the digital LF. The hybrid loop reduces the capacitor area of the LF and provides more programmable integral control. A ΔΣ modulator is inserted between the digital filter and the 9-bit DAC to increase the integral control accuracy and reduce ripples on the proportional and integral control signals.

C. Feed-Forward Equalizer: Fig. 3 shows the circuit diagram of the coarse-fine FFE scheme in a FFE driver segment. For coarse coefficient adjustment, the 1-UI delay is implemented in quarter rate by multiplexing proper data (D8<0:7>) and clock (C8<0:3>) into the 8-to-4 MUX, which increases the time margin for the MUX and enables the implementation of the 5-tap FFE at a lower data rate. The fine FFE is adjusted in the 4-to-1 MUX/driver stage by tuning the gate voltage of the cascode transistor (M2) with a 7-bit DAC, which provides a tap weight resolution of 0.6mVppd.

Measurement Results

The proposed TX was designed, generated, and fabricated in a 28nm planar CMOS technology using an open-source circuit generation framework [1] (Fig. 4). Due to the bandwidth of probes, cables, DC blocks and scope headers, the total channel loss at baud-rate frequency is ~6dB. Fig. 5 shows the measurement results of the PLL phase noise and spectrum at the C^{2}MOS divider output. The phase noise of the 12.5GHz clock output at 1MHz offset frequency is -120dBc/Hz. By

integrating the phase noise from 1kHz to 100MHz, the integrated RMS jitter is 62.97 fs, and the spur from the reference coupling is -62.33dBc. The PLL power consumes 17mW, corresponding to -251.7 dB FOM, which is comparable to state-of-the-art customized PLLs. Fig. 6 compares the pulse response without FFE and with FFE. By properly setting the 1-tap and 2-tap post cursor FFE, the ISI is eliminated and the FFE improves the loss by 4.5dB at baud-rate frequency. Fig. 7 shows the measured eye-diagram of PRBS7 NRZ and PAM-4 patterns with FFE. The measured eye-heights and eye-widths of 200Gb/s PAM-4 data are 62/54/60mV and 3.5/2.7/3.3ps, respectively, with 96.7% level mismatches (RLM). The whole TX consumes 937mW (4.69pJ/b, 17mW in SSPLL, 348mW in clock distribution, and 566mW in data path). Table I compares the TX performance with other state-of-the-art designs. This design achieves the highest data-rate with an on-chip PLL in a standard planar CMOS process.

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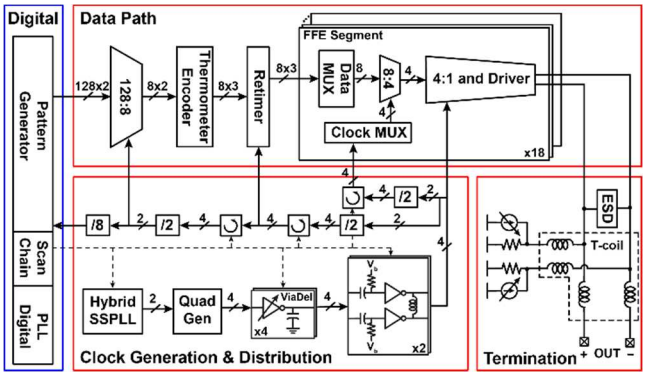


Fig. 1 TX architecture.

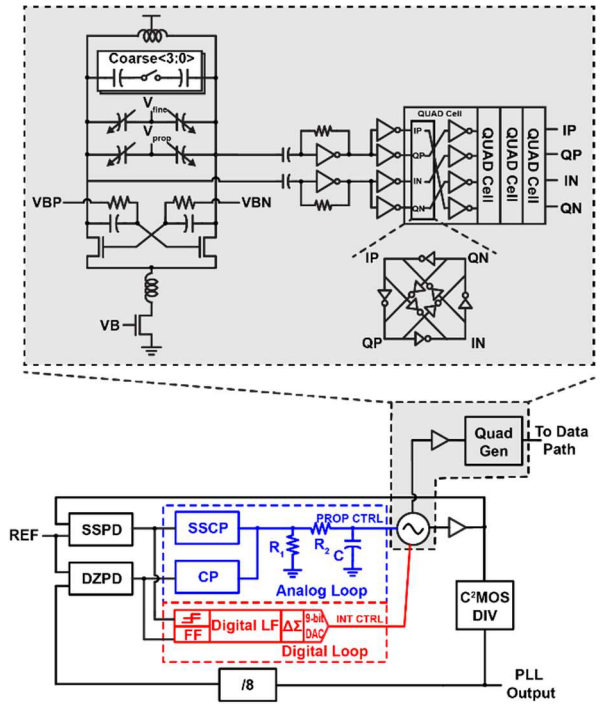


Fig. 2 Structure of hybrid SSPLL and quadrature clock generation.

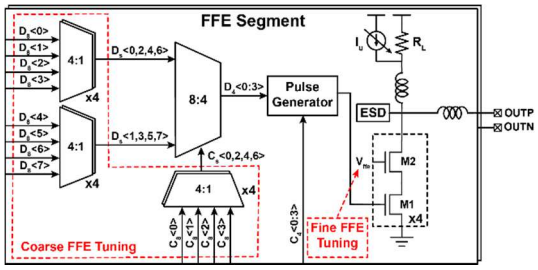
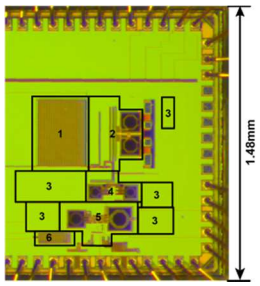


Fig. 3 Coarse and fine FFE scheme in a FFE driver segment.



	Block	Layout	Area (mm²)
1	Patten Gen.	Synthesized	0.1357
2	Data Path	Generated	0.1292
3	Bias Circuit	Generated	0.1646
4	Clock Dis.	Generated	0.0472
5	PLL	Generated	0.0766
6	PLL Digital	Generated	0.0084
	Top	Manual	0.5617

Fig. 4 Die micrograph.

Fig. 5 Phase noise and spectrum of hybrid SSPLL at the divider output.

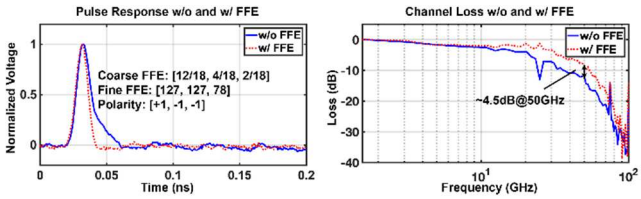


Fig. 6 Pulse response and channel loss w/o and w/ FFE.

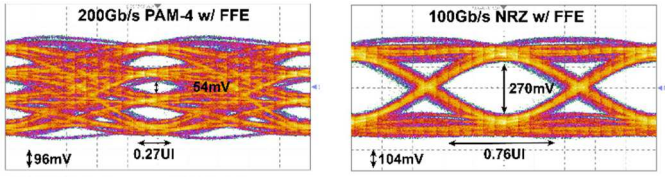


Fig. 7 Eye-diagram of NRZ pattern and PAM-4 pattern

TABLE I: PERFORMANCE SUMMARY AND COMPARISON

	ISSCC'21[1]	ISSCC'21[2]		ISSCC'18[4]		ISSCC'20[5]	ISSCC'21[6]	ISSCC'21[7]	This work	
Technology	10nm FinFET	28nm CMOS		10nm FinFET		40nm CMOS	7nm FinFET	7nm FinFET	**28nm CMOS**	
Architecture	Quarter-rate	Quarter-rate		Quarter-rate		Quarter-rate	Quarter-rate	Quarter-rate	**Quarter-rate**	
Clock Source	On-Chip	External		On-chip		External	External	External	**On-chip**	
Output Swing w/o FFE	1.0V_{ppd}	0.8V_{ppd}		0.75V_{ppd}		0.56V_{ppd}	-	-	**0.75V_{ppd}**	
FFE	8-tap	5-tap		3-tap		8-tap	8-tap	5-tap	**5-tap**	
ESD	Yes	Yes		Yes		No	Yes	Yes	**Yes**	
RJ (fs_rms)	65 (4MHz CDR)	204		150		-	-	-	**134**	
Signaling	PAM-4	PAM-4	NRZ	PAM-4	NRZ	NRZ	PAM-4	PAM-4	**PAM-4**	**NRZ**
Data Rate (Gb/s)	224	180	90	112	56	100	112	112	**200**	**100**
Efficiency (pJ/bit)	2.25	4.59*	9.18*	1.72	3.44	6.19*	1.40*	1.71*	**4.69**	**9.37**
Eye Height (mV)	90	53	234	30	260	73	59	46	**51**	**270**
Active Area (mm²)	0.088	0.432		0.0302		0.504	0.032	0.228	**0.541**	

*Excluding PLL