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Analysis of High Step-Up Quasi-Z-Source-Based Converter With Low Input Current Ripple

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ABSTRACT This article presents a new high step-up quasi-*Z*-source-based dc–dc converter with switched boost techniques and voltage multiplier cells. Compared with the conventional *Z*-source-based converters, this converter not only can achieve high voltage gain but also has good efficiency at high output voltage and higher output power conditions. Most of the *Z*-source-based converters suffer from high current stress across the power MOSFETs and the operation in lower power. However, the other important advantages include very low input current ripple, low voltage and current stress across the power switches, no duty ratio limitation, and leakage current elimination by providing the common grounded feature. So, in this topology, the null of the output is connected to the negative terminal of the input dc source directly. Therefore, the leakage current can be eliminated completely. As a result, the proposed converter is suitable for renewable energy sources (RESs)' applications, such as photovoltaic (PV) systems. The mathematical analysis, operating principle for the proposed converter, and comparison with other converters are evaluated. Finally, in order to verify the accurate performance of the proposed converter and confirm the mentioned features of the proposed converter, a 1-kW laboratory prototype is built and tested.

INDEX TERMS DC–DC converter, high-voltage conversion, low current ripple, voltage multiplier cell, *Z*-source.

I. INTRODUCTION

Recently, high step-up dc–dc converters are the most evaluated topics due to the importance of renewable energy sources (RESs) as clean energy in reducing global oil consumption. The output voltage of photovoltaic (PV) panels in the RES applications is a low-level voltage, so it is necessary to use the high step-up dc–dc converters in PV-based grid-connected or off-grid applications [1], [2], [3]. Some dc–dc converters with different structures have been presented in [4], [5], [6], and [7], which have a large duty ratio.

Accordingly, to prevent high current ripple with low efficiency, the *Z*-source converter and quasi-switched boost converter became effective structures with a small range of duty ratio [8], [9]. Furthermore, the voltage gains of both mentioned converters are the same and they can be used in various power conversions, such as ac–dc, dc–ac, ac–ac, and dc–dc [10], [11], [12], [13]. In [14], a new quasi-*Z*-source converter is presented that solves some drawbacks of the *Z*-source converter, such as discontinuous input current and leakage current, due to the lack of a common grounded connection between the null of output and negative terminal of input. However, these kinds of converters cannot provide voltage boosting feature and the low voltage stress on the semiconductors. Therefore, to provide high step-up voltage gain and decrease the voltage stresses, some *Z*-source-based converters with different structures are presented.

In [15], [16], [17], [18], [19], [20], and [21], various kinds of *Z*-source dc–dc converters with hybridization structures, cascaded structures, and the combination with switched capacitor cell and switched inductor cell have been presented. These converters cannot provide high voltage gain but the main switches in these converters have high voltage stress. In addition, the input current ripple is not low and some of the mentioned topologies are suffered from the lack of a common grounded feature. All the above-mentioned disadvantages cause high costs with low efficiency in a higher power.

In [22] and [23], switched *Z*-source/quasi-*Z*-source dc–dc converters with extra power switches have been proposed that cannot provide the common grounded feature and extended duty ratio. Also, in these converters, the voltage gain, output power, and overall efficiency are low. In [24], [25], [26], and [27], new isolated high step-up *Z*-source converters are presented, which can provide a high voltage gain by applying a higher turn ratio for the transformer. Meanwhile, it leads to lower efficiency at high powers because of high leakage inductance.

In [28] and [29], nonisolated coupled inductor-based *Z*-source and quasi-*Z*-source converters with voltage multiplier cells are presented. In these kinds of topologies, the coupled inductor needs a higher turn ratio than 1 to achieve high step-up voltage gain. A higher turn ratio decreases the normalized voltage stress of the power switch but increases the current stress and the conduction losses. As a consequence, they operate at a high power with low overall efficiency.

In this research article, a new high step-up *Z*-source network with switched boost and voltage multiplier techniques is proposed. In the proposed converter, two inductors of the network are coupled in the same magnetic core. The suggested converter not only decreases the voltage and current stress across the semiconductors but also can provide high voltage gain and desired efficiency at high power conditions compared with recently presented *Z*-source-based structures. Besides, the input current of the proposed converter is continuous with low ripple. Also, in the proposed converter, the null of the output is connected to the negative terminal of the input power supply directly. So, the proposed converter can provide the common grounded feature and leakage current elimination.

In addition, the proposed converter, operating at an input voltage of 60 V, offers versatile applications. It can efficiently harness solar energy through solar panels, converting it into a higher output voltage of 650 V suitable for integration with a three-phase inverter. This configuration enables seamless utilization in various contexts from solar power systems to electric vehicles. In the latter scenario, where 60-V lithium-ion battery cells serve as the input voltage source, the converter facilitates smooth power conversion, enabling connection to a three-phase inverter for driving and controlling the induction machine. This flexibility underscores its potential to drive sustainable energy solutions and advance electric vehicle technology, offering a promising pathway toward cleaner and more efficient power utilization.

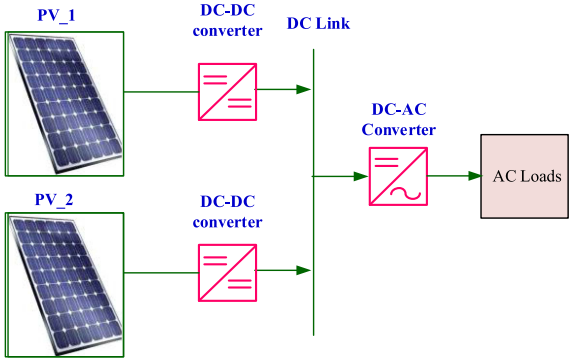


FIGURE 1. PV-based configuration for the proposed dc–dc converter.

The motivation behind this article stems from the need for improved dc–dc converters, especially in the realm of RESs, such as PV systems. The traditional *Z*-source-based converters have limitations, including high current stress on power MOSFETs and inefficiency at high output voltages and power levels. To address these challenges, the article introduces a novel high step-up quasi-*Z*-source-based dc–dc converter with switched boost techniques and voltage multiplier cells.

This innovative converter not only achieves a high voltage gain but also maintains good efficiency even under demanding conditions. By incorporating switched boost techniques and voltage multiplier cells, it mitigates the drawbacks associated with conventional *Z*-source-based converters. Notably, it significantly reduces current stress on power switches, minimizes input current ripple, and eliminates duty ratio limitations. Additionally, the converter features a common grounded topology that directly connects the null of the output to the negative terminal of the input dc source, thereby completely eliminating leakage current.

The advantages of this proposed converter make it particularly well-suited for applications involving RESs, such as PV systems [30]. This issue is shown in Fig. 1. Its ability to operate efficiently, even at high output voltages and power levels, enhances its appeal for integration into such systems. By addressing key drawbacks of existing converter topologies, this new quasi-*Z*-source-based converter offers a promising solution to advance the performance of renewable energy applications, contributing to the ongoing transition toward sustainable energy utilization.

In summary, this article introduces a novel dc–dc converter based on a high step-up quasi-*Z*-source architecture, integrating switched boost techniques and voltage multiplier cells. In comparison with the traditional *Z*-source converters, this design not only achieves a high voltage gain but also demonstrates superior efficiency under high output voltage and increased power output conditions. Unlike many *Z*-source converters, which face challenges, such as excessive current stress on power MOSFETs and limited operation at lower power levels, this converter offers additional benefits, including minimal input current ripple, reduced voltage and current stress on power switches, absence of duty ratio constraints, and elimination of leakage current through a shared ground

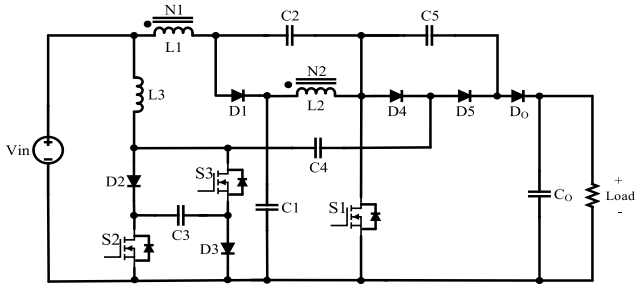


FIGURE 2. Structure of the proposed quasi-z-source (QZS) dc–dc converter.

configuration. Consequently, by directly connecting the null of the output to the negative terminal of the input dc source, the leakage current is effectively eliminated. This feature renders the proposed converter particularly suitable for applications involving RESs, such as PV systems.

The rest of this article can be organized as follows. In Section II, the proposed topology and its operation modes and steady-state analysis are described in detail. In Section III, the design of passive parameters, such as capacitors and inductors, is provided. The small-signal analysis of the proposed converter is considered in Section IV. Section V provides the power losses of the converter and its overall efficiency in detail. Also, the comparison results between the other recent converters are presented in Section VI. Finally, in Section VII, the experimental results of the laboratory prototype at 1 kW are obtained and presented to prove the features of the proposed converter. Finally, Section VIII concludes this article.

II. PROPOSED CONVERTER AND ITS OPERATING PRINCIPLE

In this section, the proposed converter and its operational modes are explained completely. The equivalent circuit of the proposed quasi-impedance source (QIS) converter is depicted in Fig. 2.

The direct connection of the grid null to the negative terminal of the input dc source serves as a fundamental design element in the proposed converter, as depicted in Fig. 2. By establishing this direct link, the converter achieves a common grounded feature, a critical aspect for electrical systems, especially those involving PV applications. This feature is particularly significant because it effectively eliminates leakage current, which is a common issue in PV-based converters.

Leakage current can arise due to various factors, such as insulation breakdown or parasitic capacitances, and it can lead to inefficiencies, safety concerns, and even system failures. However, with the proposed converter's innovative topology, this concern is effectively mitigated, enhancing the overall performance of PV systems.

By eliminating leakage current, the proposed converter not only ensures safer operation but also addresses key limitations associated with traditional PV converters. This breakthrough significantly enhances the efficiency and reliability of PV systems, making them more viable for widespread adoption in renewable energy integration efforts.

In essence, the proposed converter represents a promising solution for renewable energy integration, offering improved performance, reliability, and safety in PV applications. Its ability to overcome leakage current restrictions marks a significant advancement in converter technology, paving the way for more efficient and sustainable energy systems.

In the proposed converter topology, the integration of an inductor and capacitor in series with the switch is aimed at achieving soft switching, which is vital for reducing switching losses and improving the overall efficiency. Soft switching refers to the technique of ensuring that the voltage or current across the switch transitions smoothly between its on and off states, minimizing the occurrence of abrupt changes that can lead to energy losses and electromagnetic interference.

To achieve soft switching, the values of the inductor and capacitor must be carefully chosen to resonate at a specific frequency, known as the resonance frequency. This resonance frequency is typically determined based on the operating conditions of the converter and the desired performance metrics, such as efficiency, voltage ripple, and switching frequency.

When the inductor and capacitor resonate at the desired frequency, the energy stored in the inductor is smoothly transferred to the capacitor and vice-versa, minimizing the voltage and current stress on the switch during the switching transitions. This resonance condition allows the switch to turn on and off under near-zero-voltage or current conditions, hence the term "soft switching."

Overall, the incorporation of an inductor and capacitor in series with the switch enables the proposed converter to operate more efficiently by minimizing switching losses and improving power conversion performance, making it a key aspect of modern power electronics design.

Considering Fig. 2, the QIS network converter with switched boost techniques consists of two winding coupled inductors L_1 and L_2 in one magnetic core, inductor L_3, capacitors C_1, C_2, and C_3, diodes D_1, D_2, and D_3, and switches S_1, S_2, and S_3. The voltage multiplier cell includes capacitors C_4 and C_5, and diodes D_4 and D_5, which provide the connection of this network to the output using the output dc filter (diode D_O and capacitor C_O).

The steady-state operational waveforms of the presented converter are illustrated in Fig. 3. Also, the operational principles of continuous conduction mode in this converter are expressed.

As a result, the inductors L_1, L_2, and L_3 and all of the capacitors are assumed to be large sufficiently and the utilized semiconductors are considered ideal.

Also, the switching gate pulse of switch S_1 is 180° different from switches S_2 and S_3 during a switching period. The steady-state performance of the presented converter can be categorized into four modes. The equivalent circuit of each mode is shown in Fig. 4 and explanations of them are as follows.

Mode 1 [$t_0 < t < t_1$]: The equivalent circuit of this mode is shown in Fig. 4(a). At $t = t_0$, the power switch S_1 is turned on and diodes D_2, D_3, and D_5 are in the conducting state. The

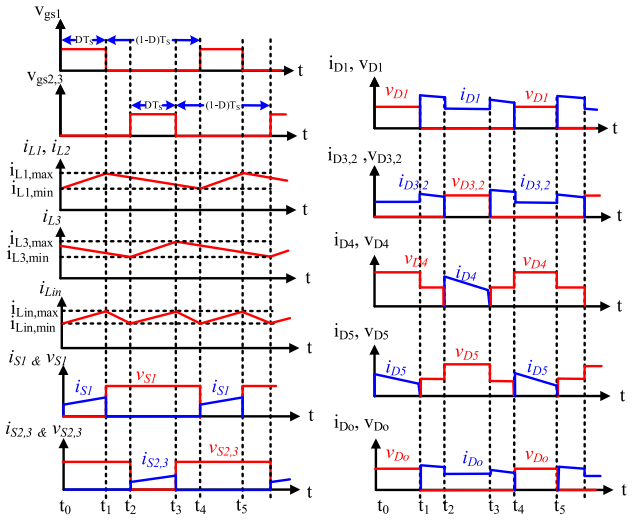


FIGURE 3. Steady-state operational waveforms of the presented converter.

energy from input voltages transferred to L_1 and L_2 and their currents increased linearly. Also, during this mode, the capacitor C_3 is charged through the inductor L_3 and input power supply, so the current of L_3 decreases linearly. In addition, the capacitor C_5 is charged by C_3 and C_4 through the diode D_5 and as well as the output capacitor C_O feeds the load. In this time interval, the following equations are obtained:

$$\frac{dI_{L1}}{dt} = \left((V_{\text{in}} + V_{C2})\,L_2 - V_{C1}M\right)/M^2 - L_1L_2 \tag{1}$$

$$\frac{dI_{L2}}{dt} = \left(V_{C1}L_1 - (V_{\text{in}} + V_{C2})\,M\right)/M^2 - L_1L_2 \tag{2}$$

$$V_{L1} = V_{\text{in}} + V_{C2} \tag{3}$$

$$V_{L2} = V_{C1} \tag{4}$$

$$V_{L3} = V_{\text{in}} - V_{C3} \tag{5}$$

$$V_{C5} = V_{C3} + V_{C4}. \tag{6}$$

In (1) and (2), M is the mutual inductance of the coupled inductor, and $k = M/\sqrt{L_1L_2}$ is the coupling coefficient.

Mode 2 [$t_1 < t < t_2$]: At the beginning of this mode, the switch S_1 is turned off and diode D_5 is reversed bias. Diodes D_2 and D_3 are still conducting and diodes D_1 and D_O start to conduct. Also, in this mode, the power switches S_2 and S_3 are still turned off. In this mode, the inductor L_1 and input energy source charge the capacitor C_1 and, simultaneously, the inductor L_2 transfers the stored energy into capacitor C_2. Therefore, the currents of L_1 and L_2 are decreased. On the other side, the stored energy in inductance L_3 still charges the capacitor C_3. Meanwhile, the stored energy of the capacitor C_5 is injected to the output capacitor and load. The current direction of this mode is shown in Fig. 4(b). In this mode, the following equations can be written:

$$\frac{dI_{L1}}{dt} = \left((V_{\text{in}} - V_{C1})\,L_2 + V_{C2}M\right)/M^2 - L_1L_2 \tag{7}$$

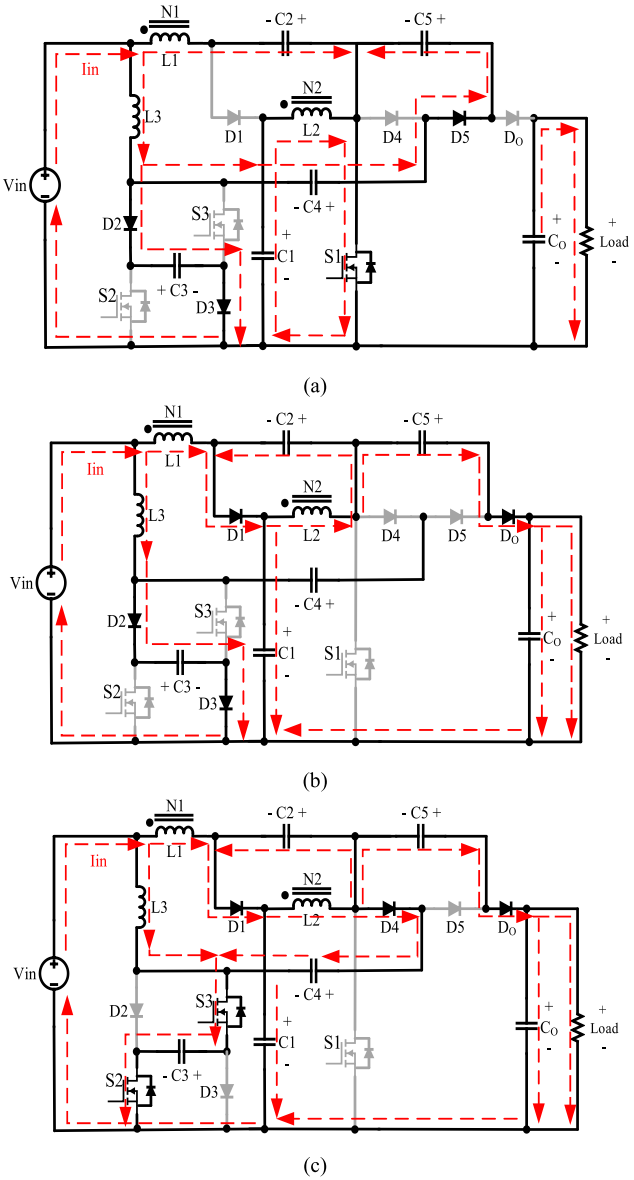


FIGURE 4. Operation modes of the proposed dcdc converter. (a) Mode1 , (b) Mode2, (c) Mode3.

$$\frac{dI_{L2}}{dt} = -\left(V_{C2}L_1 + (V_{\text{in}} - V_{C1})\,M\right)/M^2 - L_1L_2 \tag{8}$$

$$V_{L1} = V_{\text{in}} - V_{C1} \tag{9}$$

$$V_{L2} = -V_{C2} \tag{10}$$

$$V_O = V_{C1} + V_{C2} + V_{C5}. \tag{11}$$

Mode 3 [$t_2 < t < t_3$]: In this mode, the power switches S_2 and S_3 are turned on, diodes D_1 and D_O are still conducting the current, and diode D_4 starts to turn on. The equivalent circuit with the current paths of this mode is shown in Fig. 4(c).

The energy of inductors L_1 and L_2 is still decreasing as same as the previous mode but inductor L_3 is charged by capacitor C_3 and input voltage source. Also, in this time interval, the energy of the coupled inductor (L_1 and L_2) charges the capacitor C_4 by conducting the diode D_4.

By using Kirchhoff's voltage law in this mode, the equations of this mode are achieved as follows:

$$V_{L3} = V_{\text{in}} + V_{C3} \tag{12}$$

$$V_{C4} = V_{C1} + V_{C2} + V_{C3}. \tag{13}$$

Mode 4 [$t_3 < t < t_4$]: At $t = t_3$, all power switches S_1, S_2, and S_3 are turned off again and mode 2 is repeated for the second time in a time period.

Also, the equivalent circuit of this mode is the same as mode 2, and the current values are changed, as it is shown in Fig. 3. After t_4, the power switch S_1 is turned on again and mode 1 is repeated for the next time period.

The number of windings' turns for the secondary and primary sides of the coupled inductor is considered equal ($N_1 = N_2 = N$) due to the same voltage.

By applying the voltage-second principle across L_1, L_2, and L_3 and using (3)–(5), (9), (10), and (12), the voltages of capacitors C_1, C_2, and C_3 can be expressed as follows:

$$V_{C1} = \frac{1-D}{1-2D} V_{\text{in}} \tag{14}$$

$$V_{C2} = \frac{D}{1-2D} V_{\text{in}} \tag{15}$$

$$V_{C3} = \frac{1}{1-2D} V_{\text{in}} \tag{16}$$

where D is the switching duty cycle of the proposed converter during the full switching period. From mode 3 and using (13)–(16), the voltage of capacitor C_4 can be attained as follows:

$$V_{C4} = \frac{2}{1-2D} V_{\text{in}}. \tag{17}$$

By substituting (16) and (17) into (6), the voltage of capacitor C_5 can gained as follows:

$$V_{C5} = \frac{3}{1-2D} V_{\text{in}}. \tag{18}$$

By substitution of (14), (15), and (18) into (11), the output voltage can be attained as follows:

$$V_O = \frac{4}{1-2D} V_{\text{in}}. \tag{19}$$

The voltage gain of the presented converter is determined as follows:

$$G = \frac{V_o}{V_{\text{in}}} = \frac{4}{1-2D}. \tag{20}$$

To facilitate calculation, it is assumed that the power losses are ignorable. Also, it should be assumed that the input and output powers are equal and (21) and (22) are written as follows:

$$V_O I_O = V_{\text{in}} I_{\text{in}} = V_{\text{in}} (I_{L1} + I_{L3}) \tag{21}$$

$$I_{L1} = I_{L3}. \tag{22}$$

Therefore, considering (20), the input current and the average current values of all inductors can be attained as follows:

$$I_{\text{in}} = \frac{4}{1-2D} I_O \tag{23}$$

$$I_{L1} = I_{L2} = I_{L3} = \frac{2}{1-2D} I_O. \tag{24}$$

By using Kirchhoff's current law and ampere-second balance principle, all the capacitors' average currents in a time period can be obtained when they are in charging or discharging modes

$$\begin{cases} I_{C1-\text{charge}} = \frac{2D}{(1-D)(1-2D)} I_O \\ I_{C1-\text{discharge}} = -\frac{2}{(1-2D)} I_O \end{cases} \tag{25}$$

$$\begin{cases} I_{C2-\text{charge}} = \frac{2D}{(1-D)(1-2D)} I_O \\ I_{C2-\text{discharge}} = -\frac{2}{(1-2D)} I_O \end{cases} \tag{26}$$

$$\begin{cases} I_{C3-\text{charge}} = \frac{1}{(1-D)(1-2D)} I_O \\ I_{C3-\text{discharge}} = -\frac{1}{D(1-2D)} I_O \end{cases} \tag{27}$$

$$\begin{cases} I_{C4-\text{charge}} = \frac{1}{D} I_O \\ I_{C4-\text{discharge}} = -\frac{1}{D} I_O \end{cases} \tag{28}$$

$$\begin{cases} I_{C5-\text{charge}} = \frac{1}{D} I_O \\ I_{C5-\text{discharge}} = -\frac{1}{1-D} I_O \end{cases} \tag{29}$$

$$\begin{cases} I_{CO-\text{charge}} = \frac{D}{1-D} I_O \\ I_{CO-\text{discharge}} = I_O. \end{cases} \tag{30}$$

The normalized voltage stresses across power switches (S_1–S_3) are founded as follows:

$$V_{S1} = V_{S2} = V_{S3} = \frac{1}{1-2D} V_{\text{in}} = \frac{V_O}{4}. \tag{31}$$

The maximum normalized voltage stresses across power diodes D_1, D_2, D_3, and D_O are expressed as follows, when they are reversed biased:

$$V_{D1} = V_{D2} = V_{D3} = V_{DO} = \frac{1}{1-2D} V_{\text{in}} = \frac{V_O}{4}. \tag{32}$$

Also, the maximum normalized voltage stresses across power diodes D_4 and D_5 during mode 1 and mode 3 are obtained as follows, respectively:

$$V_{D4} = V_{D5} = \frac{3}{1-2D} V_{\text{in}} = \frac{3V_O}{4}. \tag{33}$$

The current stresses of semiconductors can be expressed as follows:

$$I_{S1} = I_{L1} + I_{L2} + I_{C5-\text{charge}} = \frac{1+2D}{D(1-2D)} I_O \tag{34}$$

$$I_{S2,S3} = I_{C3-\text{Discharge}} = \frac{1}{D(1-2D)} I_O \tag{35}$$

$$I_{D1} = I_{L1} + I_{C2-\text{charge}} = \frac{2}{(1-D)(1-2D)} I_O \tag{36}$$

$$I_{D2,D3} = I_{C3-\text{charge}} = \frac{1}{(1-D)(1-2D)} I_O \tag{37}$$

$$I_{D4} = I_{D5} = \frac{1}{D} I_O \tag{38}$$

$$I_{DO} = I_{C5-\text{discharge}} = \frac{1}{1-D} I_O. \tag{39}$$

III. PARAMETER DESIGN OF THE PRESENTED CONVERTER

In this section, the desired values of passive elements (inductors and capacitors) are calculated.

A. CALCULATION OF THE INDUCTANCE VALUES OF INDUCTORS

To calculate the inductance values of used inductors, assuming that the current ripple of inductors is ΔI_L and the inductor voltage during the on-state can be defined as follows:

$$V_L = L \frac{\Delta I_L}{D T_S}. \tag{40}$$

By substituting (14) into (3) and (15) into (10), the voltage of both L_1 and L_2 is equal when switch S_1 is on and off

$$V_{L_1} = V_{L_2} = \frac{(1-D) V_{\text{in}}}{(1-2D)} \tag{41}$$

$$V_{L_1} = V_{L_2} = \frac{-D V_{\text{in}}}{(1-2D)}. \tag{42}$$

Considering (41) and (42), it is assumed that the number of turns in the primary and secondary sides of the coupled inductor is equal ($N_1 = N_2$). This means that the average values of the two inductive currents are the same. Therefore, by using (40) and (41), the two inductors can be designed as follows:

$$L_1 = L_2 = \frac{(1-D) D V_{\text{in}}}{(1-2D) f_s \Delta I_{L1}}. \tag{43}$$

As well as, by using (12), (16), and (40) during the on-state, the inductor L_3 can be designed as follows:

$$L_3 = \frac{(2-2D) D V_{\text{in}}}{(1-2D) f_S \Delta I_{L3}} \tag{44}$$

where f_S is the switching frequency.

B. CALCULATION OF THE CAPACITANCE VALUES OF CAPACITORS

To calculate the capacitance values of the used capacitors, assuming that the voltage ripple of capacitors is ΔV_C and the passing current of the capacitor during the on-state can be defined as follows:

$$I_C = C \frac{\Delta V_L}{D T_S}. \tag{45}$$

Substituting (14)–(18) and (25)–(30) into (45), the minimum value of each capacitor can be designed as follows:

$$C_1 \geq \frac{8D}{(1-D)(1-2D) R_L f_S r_C\%} \tag{46}$$

$$C_2 \geq \frac{8}{(1-2D) R_L f_S r_C\%} \tag{47}$$

$$C_3 \geq \frac{4}{(1-2D) R_L f_S r_C\%} \tag{48}$$

$$C_4 \geq \frac{2}{R_L f_S r_C\%} \tag{49}$$

$$C_5 \geq \frac{4}{3 R_L f_S r_C\%} \tag{50}$$

$$C_O \geq \frac{D}{R_L f_S r_C\%}. \tag{51}$$

where f_S is the switching frequency and $r_C\%$ is the voltage ripple percentage.

IV. SMALL-SIGNAL ANALYSIS AND CLOSED-LOOP CONTROL SYSTEM

For small-signal analysis, the state variables are defined in the proposed converter using passive elements, which include capacitors and magnetizing inductance of the coupled inductor and simple inductor. Based on the main time intervals of switching on and off in the power switch, the average state space of the whole system can be defined, and using the method of small-signal modeling and linearization of converter-mode variables, the open-loop system conversion function from output voltage to duty cycle is obtained. Finally, to stabilize the output voltage, by defining a closed-loop system and adjusting the controller, the stability of the whole system will be checked.

First, in the proposed converter, the inductor current (i_{L1}), the inductor current (i_{L3}), and the voltage of capacitors (V_{C1}-V_{CO}) are selected as state variables. Therefore, the vector of state variables (x), the input voltage vector (u), and the output voltage vector (y) are considered as follows:

$$\begin{cases} x^T = [i_{L1} \quad i_{L3} \quad V_{C1} \quad V_{C2} \quad V_{C3} \quad V_{C4} \quad V_{C5} \quad V_{CO}] \\ u^T = [d] \\ y^T = [V_{\text{out}}]. \end{cases} \tag{52}$$

Based on the main time intervals of the proposed converter operation and considering the series resistance r_L with inductors and series resistance r_C in capacitors circuit loops, valid state-space variables can be obtained. Equivalent circuits for the three modes of converter operation are shown in Fig. 4.

The matrix of system state-space variables for the circuit of Fig. 4(a) in the first operation mode is obtained as (53) and (54) shown at the bottom of the next page. The matrix of system state-space variables of the desired system for the circuit of Fig. 4(b) in the second and fourth operating modes is obtained as (55) shown at the bottom of the next page. The matrix of system state-space variables for the circuit of Fig. 4(c) in the third operation mode is obtained as (56) shown at the bottom of the next page.

By using the main modes for the presented converter, the average state space of the system can be considered as (57) shown at the bottom of the next page. Based on (57), the total average state space, the time interval of the first-mode matrix will be $d(t)$, the time interval of the third-mode matrix will be $d(t)$, and the time interval of the second- and fourth-mode matrices will be $\frac{1-d(t)}{2}$, in which the coefficients A, B, C, and D are constant matrices and they can be obtained

as (58)–(60) shown at the bottom of the next page, respectively. Based on the method of small-signal modeling, the state variables, output, input voltages, and duty cycles containing two parts of dc ($\bar{X}$, $\bar{Y}$, $\bar{U}$, $\bar{D}$) and ac ($\tilde{x}$, $\tilde{y}$, $\tilde{u}$, $\tilde{d}$) can be written as (61) shown at the bottom of the next page.

It is supposed that the ac values are small and do not change considerably during one period. Therefore, the small-signal model can be displayed as (62) shown at the bottom of the next page. Thus, matrices A', B', C', and D' have constant values and can be obtained as relations (63)–(65) shown at the bottom of the next page.

The values for all the elements used in the third proposed converter, which have also been used in the practical results, are summarized in Table 1. Given these values, the matrices A', B', C', and D' are computed. Therefore, the open-loop transfer function of the proposed converter from the output voltage to the duty cycle can be calculated as (66) shown at the bottom of the next page, using MATLAB software. According to (66), it can be seen that all the poles of the open-loop system are located on the left side of the $j\omega$-axis. This concept means that the open-loop system is stable but does not have the desired stability and may be out of stability with minimal changes. The block diagram of the closed-loop voltage control system for the first proposed converter is shown in Fig. 5.

The transfer function $G_C(S)$ is a proportional–integral (PI) controller in which the control coefficients K_i and K_P are set to 0.00005 and 0.000001, respectively.

To ensure stability in controlling the converter, it is essential to adjust the coefficients of the PI controller. These coefficients determine the response of the controller and are typically determined using MATLAB software, where they are programmed based on predefined relationships. Alternatively, trial-and-error methods can be employed to find suitable values for these coefficients.

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \\ \frac{du_{C3}}{dt} \\ \frac{du_{C4}}{dt} \\ \frac{du_{C5}}{dt} \\ \frac{du_{Co}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_L}{L_1} & 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{-r_L}{L_3} & 0 & 0 & -\frac{1}{L_3} & 0 & 0 & 0 \\ -\frac{1}{nC_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & -\frac{1}{2C_3r_C} & -\frac{1}{2C_3r_C} & \frac{1}{2C_3r_C} & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{2C_4r_C} & -\frac{1}{2C_4r_C} & \frac{1}{2C_4r_C} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2C_5r_C} & \frac{1}{2C_5r_C} & -\frac{1}{2C_5r_C} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_OR_L} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L1}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \\ u_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_3} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} U_{\text{in}}(t) \tag{53}$$

$$y = U_O(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L3}(t) & u_{C1}(t) & u_{C2}(t) & u_{C3}(t) & u_{C4}(t) & u_{C5}(t) & u_{CO}(t) \end{bmatrix}^T \tag{54}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \\ \frac{du_{C3}}{dt} \\ \frac{du_{C4}}{dt} \\ \frac{du_{C5}}{dt} \\ \frac{du_{Co}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_L}{L_1} & 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-r_L}{L_3} & 0 & 0 & -\frac{1}{L_3} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & -\frac{1}{C_1r_C} & -\frac{1}{C_1r_C} & 0 & 0 & -\frac{1}{C_1r_C} & \frac{1}{C_1r_C} \\ \frac{1}{nC_2} & 0 & -\frac{1}{C_2r_C} & -\frac{1}{C_2r_C} & 0 & 0 & -\frac{1}{C_2r_C} & \frac{1}{C_2r_C} \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_5r_C} & -\frac{1}{C_5r_C} & 0 & 0 & -\frac{1}{C_5r_C} & \frac{1}{C_5r_C} \\ 0 & 0 & \frac{1}{C_Or_C} & \frac{1}{C_Or_C} & 0 & 0 & \frac{1}{C_Or_C} & -\frac{R_L+r_C}{C_Or_CR_L} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L1}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \\ u_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_3} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} U_{\text{in}}(t) \tag{55}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \\ \frac{du_{C3}}{dt} \\ \frac{du_{C4}}{dt} \\ \frac{du_{C5}}{dt} \\ \frac{du_{Co}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_L}{L_1} & 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-r_L}{L_3} & 0 & 0 & \frac{1}{L_3} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & -\frac{2}{C_1r_C} & -\frac{2}{C_1r_C} & -\frac{1}{C_1r_C} & \frac{1}{C_1r_C} & -\frac{1}{C_1r_C} & \frac{1}{C_1r_C} \\ \frac{1}{nC_2} & 0 & -\frac{2}{C_2r_C} & -\frac{2}{C_2r_C} & -\frac{1}{C_2r_C} & \frac{1}{C_2r_C} & -\frac{1}{C_2r_C} & \frac{1}{C_2r_C} \\ 0 & -\frac{1}{C_3} & \frac{1}{C_3r_C} & \frac{1}{C_3r_C} & \frac{1}{C_3r_C} & -\frac{1}{C_3r_C} & 0 & 0 \\ 0 & 0 & \frac{1}{C_4r_C} & \frac{1}{C_4r_C} & \frac{1}{C_4r_C} & -\frac{1}{C_4r_C} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_5r_C} & -\frac{1}{C_5r_C} & 0 & 0 & -\frac{1}{C_5r_C} & \frac{1}{C_5r_C} \\ 0 & 0 & \frac{1}{C_Or_C} & \frac{1}{C_Or_C} & 0 & 0 & \frac{1}{C_Or_C} & -\frac{R_L+r_C}{C_Or_CR_L} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L1}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \\ u_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_3} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} U_{\text{in}}(t) \tag{56}$$

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \tag{57}$$

In more detail, the PI controller operates by comparing the desired output of the system (reference signal) with the actual output and generating an error signal. The proportional term of the controller responds to the current error signal, while the integral term integrates past errors over time. Adjusting the PI controller coefficients allows for fine-tuning the controller's response to achieve stable and optimal performance of the converter. By programming these coefficients in MATLAB or through iterative trial-and-error, engineers can effectively adjust the controller to meet the desired control objectives and ensure stability in the system.

$$A=\begin{bmatrix} \frac{-r_L}{L_1} & 0 & \frac{d(t)-1}{L_1} & \frac{d(t)}{L_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{-r_L}{L_3} & 0 & 0 & \frac{2d(t)-1}{L_3} & 0 & 0 & 0 \\ \frac{n-(n+1)d(t)}{nC_1} & 0 & -\frac{1}{C_1r_C} & -\frac{1}{C_1r_C} & -\frac{d(t)}{C_1r_C} & \frac{d(t)}{C_1r_C} & \frac{d(t)-1}{C_1r_C} & \frac{1-d(t)}{C_1r_C} \\ \frac{n-(n+1)d(t)}{nC_2} & 0 & -\frac{1}{C_2r_C} & -\frac{1}{C_2r_C} & -\frac{d(t)}{C_2r_C} & \frac{d(t)}{C_2r_C} & \frac{d(t)-1}{C_2r_C} & \frac{1-d(t)}{C_2r_C} \\ 0 & \frac{1-2d(t)}{C_3} & \frac{d(t)}{C_3r_C} & \frac{d(t)}{C_3r_C} & \frac{d(t)}{2C_3r_C} & -\frac{3d(t)}{2C_3r_C} & \frac{d(t)}{2C_3r_C} & 0 \\ 0 & 0 & \frac{d(t)}{C_4r_C} & \frac{d(t)}{C_4r_C} & \frac{d(t)}{2C_4r_C} & -\frac{3d(t)}{2C_4r_C} & \frac{d(t)}{2C_4r_C} & 0 \\ 0 & 0 & \frac{d(t)-1}{C_5r_C} & \frac{d(t)-1}{C_5r_C} & \frac{d(t)}{2C_5r_C} & \frac{d(t)}{2C_5r_C} & \frac{d(t)-2}{2C_5r_C} & \frac{1-d(t)}{C_5r_C} \\ 0 & 0 & \frac{1-d(t)}{C_Or_C} & \frac{1-d(t)}{C_Or_C} & 0 & 0 & \frac{1-d(t)}{C_Or_C} & \frac{R_Ld(t)-R_L-r_C}{C_Or_CR_L} \end{bmatrix} \tag{58}$$

$$B=\begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_3} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{59}$$

$$C=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix},\quad D=[0] \tag{60}$$

$$\begin{cases} x=\bar{X}+\tilde{x} \\ y=\bar{Y}+\tilde{y} \\ u=\bar{U}+\tilde{u} \\ d=\bar{D}+\tilde{d} \end{cases} \tag{61}$$

$$\begin{cases} \dot{\tilde{x}}=A'\tilde{x}+B'\tilde{u} \\ \tilde{y}=C'\tilde{x}+D'\tilde{u} \end{cases} \tag{62}$$

$$A'=\begin{bmatrix} \frac{-r_L}{L_1} & 0 & \frac{D-1}{L_1} & \frac{D}{L_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{-r_L}{L_3} & 0 & 0 & \frac{2D-1}{L_3} & 0 & 0 & 0 \\ \frac{n-(n+1)D}{nC_1} & 0 & -\frac{1}{C_1r_C} & -\frac{1}{C_1r_C} & -\frac{D}{C_1r_C} & \frac{D}{C_1r_C} & \frac{D-1}{C_1r_C} & \frac{1-D}{C_1r_C} \\ \frac{n-(n+1)D}{nC_2} & 0 & -\frac{1}{C_2r_C} & -\frac{1}{C_2r_C} & -\frac{D}{C_2r_C} & \frac{D}{C_2r_C} & \frac{D-1}{C_2r_C} & \frac{1-D}{C_2r_C} \\ 0 & \frac{1-2D}{C_3} & \frac{D}{C_3r_C} & \frac{D}{C_3r_C} & \frac{D}{2C_3r_C} & -\frac{3D}{2C_3r_C} & \frac{D}{2C_3r_C} & 0 \\ 0 & 0 & \frac{D}{C_4r_C} & \frac{D}{C_4r_C} & \frac{D}{2C_4r_C} & -\frac{3D}{2C_4r_C} & \frac{D}{2C_4r_C} & 0 \\ 0 & 0 & \frac{D-1}{C_5r_C} & \frac{D-1}{C_5r_C} & \frac{D}{2C_5r_C} & \frac{D}{2C_5r_C} & \frac{D-2}{2C_5r_C} & \frac{1-D}{C_5r_C} \\ 0 & 0 & \frac{1-D}{C_Or_C} & \frac{1-D}{C_Or_C} & 0 & 0 & \frac{1-D}{C_Or_C} & \frac{R_LD-R_L-r_C}{C_Or_CR_L} \end{bmatrix} \tag{63}$$

$$B'=\begin{bmatrix} 0 & 0 & \frac{1}{L_1} & \frac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{2}{L_3} & 0 & 0 & 0 \\ \frac{-(n+1)}{nC_1} & 0 & 0 & 0 & -\frac{1}{C_1r_C} & \frac{1}{C_1r_C} & \frac{1}{C_1r_C} & \frac{-1}{C_1r_C} \\ \frac{-(n+1)}{nC_2} & 0 & 0 & 0 & -\frac{1}{C_2r_C} & \frac{1}{C_2r_C} & \frac{1}{C_2r_C} & \frac{-1}{C_2r_C} \\ 0 & -\frac{2}{C_3} & \frac{1}{C_3r_C} & \frac{1}{C_3r_C} & \frac{1}{2C_3r_C} & -\frac{3}{2C_3r_C} & \frac{1}{2C_3r_C} & 0 \\ 0 & 0 & \frac{1}{C_4r_C} & \frac{1}{C_4r_C} & \frac{1}{2C_4r_C} & -\frac{3}{2C_4r_C} & \frac{1}{2C_4r_C} & 0 \\ 0 & 0 & \frac{1}{C_5r_C} & \frac{1}{C_5r_C} & \frac{1}{2C_5r_C} & \frac{1}{2C_5r_C} & \frac{1}{2C_5r_C} & \frac{-1}{C_5r_C} \\ 0 & 0 & \frac{-1}{C_Or_C} & \frac{-1}{C_Or_C} & 0 & 0 & \frac{-1}{C_Or_C} & \frac{R_L}{C_Or_CR_L} \end{bmatrix} \tag{64}$$

$$C'=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, D'=[0] \tag{65}$$

$$G(s)\big|_{U\text{in}(t)=0}=\frac{Uo(t)}{d(t)}. \tag{66}$$

TABLE 1. Specifications of the Proposed Converter to Find the Dynamic Response of the System

Parameters	Specifications
Vin	60 V
V_o	655 V
P_o	1000 W
Duty cycle	0.325
Inductor L_3	700 μH
Primary of coupled inductor L_1 n_1:n_2	350 μH n_1:n_2=1:1
r_C	0.02 Ω
r_L	0.02 Ω
C_3 ,C_1, C_2	220 μF
C_4	22 μF
C_5	100 μF
C_O	100 μF

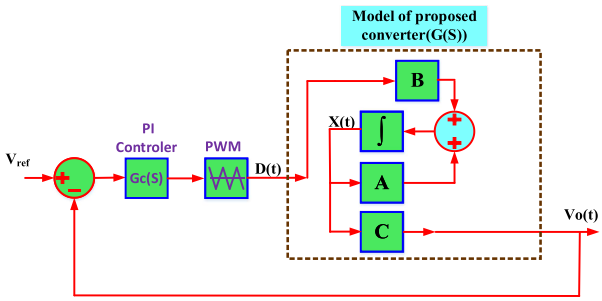


FIGURE 5. Block diagram of the closed-loop control system of the proposed converter.

Therefore, the corresponding transmission function of the closed-loop voltage control system can be expressed as follows:

$$G_{CV}(s) = G_C(s)G(s). \tag{67}$$

The bode diagram of the open-loop system $G(S)$ and the transfer function of the closed-loop control system $G_C(S)$ are shown in Fig. 6. The gain margin (GM) and phase margin (PM) for the open-loop system are 4.35 dB and −88.82°, respectively, indicating that the open-loop system is unstable.

The GM and PM should be positive ranges (GM > 0 dB) and (PM > 0°), which are 29 dB and 90.2° for the closed-loop system, respectively. These values prove that the closed-loop system is stable with the PI controller and that any change in the output load or input voltage will not impede the stability of the system.

V. POWER LOSS AND EFFICIENCY ANALYSIS

In this section, using the values of voltages, average and effective values of currents of all elements, internal resistance, and some characteristics of semiconductors, the losses of the

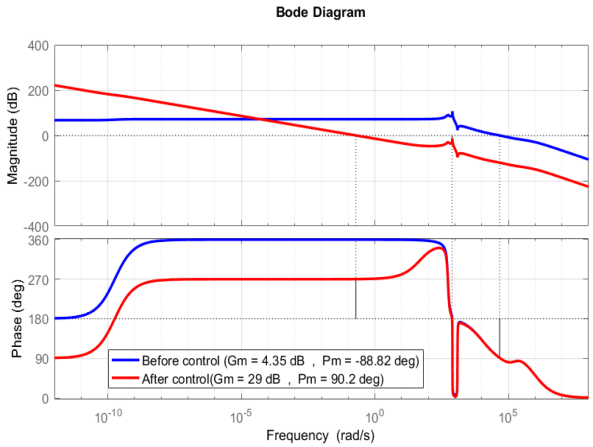


FIGURE 6. Bode diagram of the control system for the proposed converter.

proposed converter are calculated and finally, using the input, output power, and wasted power of the converter, the efficiency value can be obtained. The effective current (rms) values of all the elements used in the proposed converter are given in Table 2. Specifications related to loss calculations for all elements are also collected in Table 3.

By using Table 3, at first, the losses of power switches can be calculated as follows, which are obtained from the sum of conduction losses P_{Con} and switching losses P_{Sw}

$$P_S = P_{\text{Sw}} + P_{\text{Con}} = R_{DS-\text{on}} i^2_{S,\text{RMS}} + 0.5 f_s \left(t_r + t_f\right) i_{S,\text{av}} V_s. \tag{68}$$

In this equation, $R_{DS-\text{on}}$ is the MOSFET internal resistance, $i_{S,\text{RMS}}$ is the rms current of the switch, f_s is the switching frequency, t_r and t_f are the on- and off-times of the switch, and V_S and $i_{S,\text{av}}$ are the voltage stress and average current of the switch, respectively.

As observed, the individual losses of the switches were calculated and from the sum of conduction losses P_{Con} and switching losses P_{Sw}, their total losses are obtained as follows:

$$P_{S-\text{tot}} = P_{\text{Sw}} + P_{\text{Con}} = 6.33 + 11.1 = 17.4\,\text{W}. \tag{69}$$

The total losses of power diodes can be defined as follows, which are obtained from the sum of the individual losses of the diodes:

$$P_D = \sum_{1}^{n} \left(V_{FD} i_{Dn,\text{av}} + r_d i^2_{Dn,\text{RMS}}\right)$$
$$= P_{D1} + P_{D2} + P_{D3} + P_{D4} + P_{D5} + P_{DO} = 22.65\,\text{W}. \tag{70}$$

In this regard, r_d is the internal resistance of the diode, $i_{D,\text{RMS}}$ is the rms current of the diode, $i_{D-\text{av}}$ is the average current passing through the diode, and V_{FD} is the voltage drop of the diode. The total losses of the converter capacitors can be obtained from the sum of the individual losses of the

TABLE 2. Effective Current Relations (RMS) of All Elements Used in the Proposed Converter

Component	RMS Current Values
S_1	$i_{S1,RMS} = \frac{1+2D}{D(1-2D)}\sqrt{D}I_O$
S_2 and S_3	$i_{S1,RMS} = \frac{1}{D(1-2D)}\sqrt{D}I_O$
D_1	$i_{D1-RMS} = \frac{2}{(1-D)(1-2D)}\sqrt{1-D}I_O$
D_2 and D_3	$i_{D2,3-RMS} = \frac{1}{(1-D)(1-2D)}\sqrt{1-D}I_O$
D_4 and D_5	$i_{D4,5-RMS} = \frac{\sqrt{D}}{D}I_O$
D_O	$i_{DO-RMS} = \frac{\sqrt{1-D}}{1-D}I_O$
L_1, L_2, L_3	$i_{L-RMS} = \sqrt{[(I_{L-avg})^2 + \frac{1}{12}\Delta I_L{}^2]}$
C_1	$i_{C1,RMS} = \left(\frac{2}{(1-2D)}\right)\sqrt{\frac{D}{(1-D)}}I_O$
C_2	$i_{C2,RMS} = \left(\frac{2}{(1-2D)}\right)\sqrt{\frac{D}{(1-D)}}I_O$
C_3	$i_{C3,RMS} = \frac{1}{(1-2D)\sqrt{D(1-D)}}I_O$
C_4	$i_{C4,RMS} = \sqrt{\frac{2}{D}}I_O$
C_5	$i_{C5,RMS} = \frac{1}{\sqrt{D(1-D)}}I_O$
C_O	$i_{CO,RMS} = \sqrt{\frac{D}{(1-D)}}I_O$

TABLE 3. Specifications of the Proposed Converter Elements for Calculating Losses

Component	Specifications
Power MOSFETs $S1$, $S2$, and $S3$	R_{DS} = 0.04 Ω, tf = 23 ns, tr = 94 ns
Diodes $D1$, $D4$, and $D5$	R_{D1} = 0.0047 Ω, V_{FD1} = 1.1 V
Diodes $D2$, $D3$, and D_O	R_D = 0.015 Ω, V_{FD1} = 0.75 V
Capacitors	r_C = 0.02 Ω
Inductor $L3$	r_{L3} = 0.015 Ω
Coupled windings $L1$ and $L2$	r_{L1} = r_{L2} = 0.023 Ω

capacitors

$$P_C = \sum_{1}^{n} r_C i_{Cn,\mathrm{RMS}}^2 = P_{C1} + P_{C2} + P_{C3} + P_{C4} + P_{C5} + P_{CO} = 3.91\,\mathrm{W}. \quad (71)$$

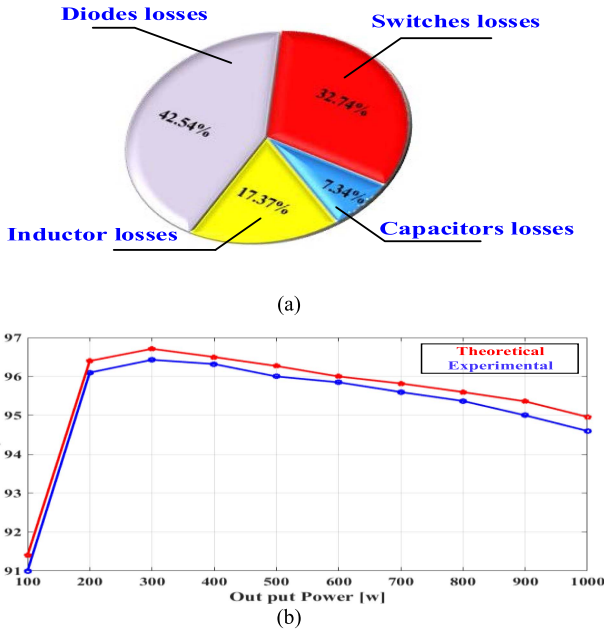


FIGURE 7. Loss analysis. (a) Power loss distribution of various components for the presented converter. (b) Efficiency of the converter for various output powers.

In this regard, r_C is the internal resistance of the capacitor, and $i_{C,\mathrm{RMS}}$ is the rms current of the capacitor. In this section, the total losses of the third proposed converter inductors can be obtained from the sum of the individual losses of copper loss and core loss. Converter copper losses are obtained from the following equation:

$$P_{\mathrm{cu}-L} = r_{L1} i_{L1,\mathrm{RMS}}^2 + r_{L2} i_{L2,\mathrm{RMS}}^2 + r_{L3} i_{L3,\mathrm{RMS}}^2 = 7.07\,\mathrm{W}. \quad (72)$$

In this regard, r_L is the series resistance of the winding and $i_{L,\mathrm{RMS}}$ is the rms current of the inductor windings. Cores' losses of the converter are defined using [31] as follows:

$$P_{\mathrm{Core}} = K_C f_S^{\alpha} \Delta B^{\beta} \alpha. \quad (73)$$

In this regard, the coefficient K_C depends on the weight and volume of the core and the coefficients α and β according to the switching frequency are obtained from the datasheet of the desired core. The change in core flux density in the proposed converter is defined as the following relation using the number of windings turns:

$$\Delta B_{-L1} = \frac{(N_{L1}\Delta I_{L1} + N_{L2}\Delta I_{L2})\,\mu_0}{l_{g-L1}} = \frac{2 \times 22 \times 0.31 \times 8.74 \times 4\pi \times 10^{-7}}{1.28 \times 10^{-3}} = 0.116\,\mathrm{T} \quad (74)$$

$$\Delta B_{-L3} = \frac{N\Delta I_{L3}\mu_0}{l_{g-L3}} = \frac{44 \times 0.31 \times 8.74 \times 4\pi \times 10^{-7}}{2.56 \times 10^{-3}} = 0.058\,\mathrm{T} \quad (75)$$

TABLE 4. Comparison Results of the Presented Converter and Other *Z*-Source DC–DC Converters

Ref	Number of				Voltage gain (M)	Switch Maximum Normalized		f_S [kHz]	Vin-Vo	P_{out} [kW]	Eff [%]	Common ground	Input Current ripple
	S	D	C	M.C		Voltage stress	Current stress						
QZS [14]	1	2	3	2	$\frac{1}{1-2D}$	MV_{in}	$2I_{in}$	50	24–120	0.04	94.5	Yes	High
[19]	1	5	7	3	$\frac{2+D}{1-2D}$	$\frac{(2M+1)}{5}V_{in}$	$\frac{(M-1)(1+2M)}{M(M-2)}I_{in}$	40	24–365	0.2	90.3	No	High
[21]	2	5	7	4	$\frac{3+2D}{1-2D}$	$\frac{(M+1)}{4}V_{in}$	$\frac{(M-1)(1+M)}{M(M-3)}I_{in}$	50	20–300	0.2	78	No	High
[23]	2	5	5	2	$\frac{3-3D}{(1-3D)}$	$\frac{(M-1)V_{in}}{2}$	$\frac{4M^2-9M+3}{M(M-3)}I_{in}$	100	40–240	0.14	98	No	High
[26]	4	4	3	2	$\frac{2n}{1-2D}$	$\frac{MV_{in}}{2n}$	$\frac{2M}{M-2n}I_{in}$	10	80–400	0.45	93.7	No	High
[27]	4	4	10	4	$\frac{2n}{1-2D}$	$\frac{MV_{in}}{2n}$	$\frac{M}{M-2n}I_{in}$	50	60–400	0.3	94.7	No	Low
[28]	1	5	7	3	$\frac{2n+1-D}{1-2D}$	$\frac{(2M-1)}{4n+1}V_{in}$	$\frac{(2M-1)^2}{M(M-2n-1)}I_{in}$	100	24–300	0.1	89	No	High
[29]	1	4	5	2	$\frac{2+n}{1-2D}$	$\frac{MV_{in}}{2+n}$	$\frac{(4+2n)M-2n^2-6n-4}{(M-n-2)(2+n)}I_{in}$	50	60–580	0.5	95.5	Yes	High
prop	3	6	6	2	$\frac{4}{1-2D}$	$\frac{MV_{in}}{4}$	$\frac{M-2}{M-4}I_{in}$	40	60–650	1	94.6	Yes	Low

S: Switch, D: Diode, C: Capacitor, and M.C: Magnetic core.

TABLE 5. Comparison Results of the Presented Converter and Other Topologies Based on Voltage and Current Stress, and Power Density

Ref	Voltage gain (M)	Switch Maximum Normalized		Inductor's total current stress	Diode's total current stress	P_{out} [kW]	Total Volume (mm^3)	Power Density (W/mm^3) ($*10^{-4}$)
		Voltage stress	Current stress					
QZS [14]	$\frac{1}{1-2D}$	MV_{in}	$\frac{4M}{M-1}I_{in}$	$2GI_O$	$(G+1)I_O$	0.04	-	-
[19]	$\frac{2+D}{1-2D}$	$\frac{(2M+1)}{5}V_{in}$	$\frac{(M-1)(1+2M)}{M(M-2)}I_{in}$	$(2G+1)I_O$	$(G+4)I_O$	0.2	363249.68	4.12
[21]	$\frac{3+2D}{1-2D}$	$\frac{(M+1)}{4}V_{in}$	$\frac{(M-1)(1+M)}{M(M-3)}I_{in}$	$2GI_O$	$(G+3)I_O$	0.2	546481.66	3.65
[23]	$\frac{3-3D}{(1-3D)}$	$\frac{(M-1)V_{in}}{2}$	$\frac{4M^2-9M+3}{M(M-3)}I_{in}$	$2(G-1)I_O$	$(2G+1)I_O$	0.14	173740	8.11
[26]	$\frac{2n}{1-2D}$	$\frac{MV_{in}}{2n}$	$\frac{2M}{M-2n}I_{in}$	$(2n+G)I_O$	$(G+2)I_O$	0.45	320996.71	14.01
[27]	$\frac{2n}{1-2D}$	$\frac{MV_{in}}{2n}$	$\frac{M}{M-2n}I_{in}$	$(2G+3)I_O$	$(G+4)I_O$	0.3	263805.3	11.37
[28]	$\frac{2n+1-D}{1-2D}$	$\frac{(2M-1)}{4n+1}V_{in}$	$\frac{(2M-1)^2}{M(M-2n-1)}I_{in}$	$(2G+n)I_O$	$(G+4)I_O$	0.1	247203.13	4.04
[29]	$\frac{2+n}{1-2D}$	$\frac{MV_{in}}{2+n}$	$\frac{(4+2n)M-2n^2-6n-4}{(M-n-2)(2+n)}$ in	$(2G+n)I_O$	$(G+3)I_O$	0.5	247165.39	20.22
prop	$\frac{4}{1-2D}$	$\frac{MV_{in}}{4}$	$\frac{M}{2(M-4)}I_{in}$ $\frac{M-2}{M-4}I_{in}$	$\frac{3}{2}GI_O$	$(G+3)I_O$	1	260984.7	3.83

S: Switch, D: Diode, C: Capacitor, and M.C: Magnetic core.

where parameters $l_{g\text{-}L1}$ and $l_{g\text{-}L3}$ represent the air gap within the EE cores, a crucial factor in determining the number of winding turns for the inductors' design. The air gap is deliberately introduced to mitigate core saturation in these types of inductors. Core saturation occurs when the magnetic flux within the core reaches a maximum level, limiting the inductor's ability to store energy efficiently and leading to performance degradation.

To prevent core saturation and ensure optimal performance, designers carefully calculate the required air gap based on factors, such as the material properties of the core and the expected operating conditions of the inductor. By introducing an air gap, the magnetic flux is dispersed more evenly throughout the core, allowing for increased energy storage capacity and preventing magnetic saturation.

Using (71)–(73), the values of the flux density changes of each core were obtained. Therefore, the losses of each core are calculated separately as follows:

$$P_{\text{Core\_}L1} = 0.41 \times 5.59 \times 10^{-4} \times (40k)^{1.43} \times (0.116)^{2.85} = 1.92\,\text{W} \tag{76}$$

TABLE 6. Comparison of Total Stresses Between the Presented Converter and Other *Z*-Source-Based DC–DC Converters

Ref	Voltage gain (M)	Total current stress on switches	Total voltage stress on switches	Total voltage stress on diodes	Total voltage stress on capacitors	TCSF	TSDP	Inductor ripple at the same condition
QZS [14]	$\frac{1}{1-2D}$	$\frac{4M}{M-1}I_{in}$	MV_{in}	$2MV_{in}$	$2MV_{in}$	$5MV_{in}$	$\frac{4M^2}{M-1}P_O$	30%
[19]	$\frac{2+D}{1-2D}$	$\frac{(M-1)(1+2M)}{M(M-2)}I_{in}$	$\frac{(2M+1)}{5}V_{in}$	$(2M+1)V_{in}$	$\frac{13M-6}{5}V_{in}$	$5MV_{in}$	$\frac{(M-1)(1+2M)^2}{5M(M-2)}P_O$	30%
[21]	$\frac{3+2D}{1-2D}$	$\frac{2(M-1)(1+M)}{M(M-3)}I_{in}$	$\frac{(M+1)}{2}V_{in}$	$2(M+1)V_{in}$	$\frac{5M+3}{2}V_{in}$	$(5M+6)V_{in}$	$\frac{(M-1)(1+M)^2}{2M(M-3)}P_O$	15%
[23]	$\frac{3-3D}{(1-3D)}$	$\frac{5M^2-12M+3}{M(M-3)}I_{in}$	$(M-1)V_{in}$	$3MV_{in}$	$\frac{7M-6}{3}V_{in}$	$\frac{19M-9}{3}V_{in}$	$\frac{(5M^2-12M+3)(M-1)}{2M(M-3)}P_O$	30%
[26]	$\frac{2n}{1-2D}$	$\frac{4M}{M-2n}I_{in}$	$\frac{4MV_{in}}{n}$	$\frac{(2n+1)M}{n}V_{in}$	$\frac{(2n+1)M}{2n}V_{in}$	$\frac{(6n+11)M}{2n}V_{in}$	$\frac{4M^2}{n(M-2n)}P_O$	30%
[27]	$\frac{2n}{1-2D}$	$\frac{2M}{M-2n}I_{in}$	$\frac{MV_{in}}{2n}$	$3MV_{in}$	$\frac{(2n+1)M}{n}V_{in}$	$\frac{(10n+3)M}{2n}V_{in}$	$\frac{M^2}{n(M-2n)}P_O$	15%
[28]	$\frac{2n+1-D}{1-2D}$	$\frac{(2M-1)^2}{M(M-2n-1)}I_{in}$	$\frac{(2M-1)}{4n+1}V_{in}$	$\frac{5(2M-1)}{4n+1}V_{in}$	$\frac{(4n+(3+4n)M)V_{in}}{4n+1}$	$\frac{(4n-6+(15+4n)M)V_{in}}{4n+1}$	$\frac{(2M-1)^3}{M(4n+1)(M-2n-1)}P_O$	30%
[29]	$\frac{2+n}{1-2D}$	$\frac{(4+2n)M-2n^2-6n-4}{(M-n-2)(2+n)}I_{in}$	$\frac{MV_{in}}{2+n}$	$\frac{(2n+4M)V_{in}}{2+n}$	$\frac{((5+2n)M-2-n)V_{in}}{4n+2}$	$\frac{((15+2n)M-2+3n)V_{in}}{4n+2}$	$\frac{M((4+2n)M-2n^2-6n-4)}{(M-n-2)(2+n)^2}P_O$	30%
prop	$\frac{4}{1-2D}$	$\frac{2M-2}{M-4}I_{in}$	$\frac{3MV_{in}}{4}$	$\frac{5MV_{in}}{2}$	$\frac{11MV_{in}}{4}$	$\frac{25MV_{in}}{4}$	$\frac{M(M-1)}{2(M-4)}P_O$	15%

S: Switch, D: Diode, C: Capacitor, and M.C: Magnetic core.

TABLE 7. Comparison of the Cost and Output Power of the Proposed Converter and Compared References

Ref.		[14]	[19]	[21]	[23]	[26]	[27]	[28]	[29]	Prop.
P_{out}(W)		40	200	200	141	450	300	100	500	1000
Price of ($)	S	-	5	28.03	-	55.56	13.8	5	5.5	15
	D	-	5	19.4	-	19.28	7.5	32.05	24.25	27.21
	M.C	-	59.98	32	-	45	63.44	16	32	16
	C	-	37.5	30.85	-	32.19	43.18	29.74	32.52	30.9
	Total	-	107.48	110.28	-	152.03	127.92	82.79	93.27	89.11

$$P_{\text{Core\_}L3} = 0.41 \times 5.59 \times 10^{-4} \times (40k)^{1.43} \times (0.058)^{2.85} = 0.26\,\text{W}. \quad (77)$$

The total losses of the inductors are obtained from the sum of the individual losses of copper and core as follows:

$$P_{L-\text{Total}} = P_{\text{Core}} + P_{\text{Cu}} = 7.07 + 2.18 = 9.25\,\text{W}. \quad (78)$$

Finally, the total losses of the converter can be calculated from the sum of the individual losses obtained

$$P_{\text{Loss-Total}} = P_S + P_D + P_C + P_L = 17.43 + 22.65 + 3.91 + 9.25 = 53.24\,\text{W}. \quad (79)$$

Therefore, the converter efficiency is obtained from the following equation using the calculated losses:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{Loss-Total}_L}} = \frac{1000\,\text{W}}{1053.24\,\text{W}} = 94.94\%. \quad (80)$$

The power loss distribution of various components under $V_{\text{in}} = 60$ V, $V_O = 650$ V, and $P_{\text{out}} = 1$ kW is evaluated in Fig. 7(a). The calculated total loss of the presented converter

is about 53.24 W. The losses of all power switches are obtained about 17.43 W, which is 32.74% of the total losses. The calculated losses of all diodes are about 22.65 W, which is obtained 42.54% of the total losses. Furthermore, the total losses of the inductors L_1, L_2, and L_3 are calculated at about 9.25 W, which is 17.37% of the total losses. The obtained losses of all capacitors are about 3.91 W, which is 7.34% of the total losses. By considering total losses, the calculated efficiency of the converter is attained at about 94.94%. The measured efficiency of the proposed laboratory prototype with calculated efficiency for various output power is shown in Fig. 7(b). As it can be observed, the measured efficiency of the presented converter in output power of 1 kW is 94.7 % approximately, which is close to the calculated efficiency.

By decreasing the output power, the efficiency of the converter is increased and the maximum efficiency of the presented converter is about 96.41 % at the output power of 300 W.

VI. COMPARISON STUDY

In this section, in order to show the difference of the proposed converter and its advantages compared with some other recently presented Z-source converter, a comprehensive comparison is done.

This comparison is done based on some items, such as the number of elements, voltage gain, maximum normalized voltage and current stress of power switches, efficiency with output power, input current ripple, and the common grounded feature. The comparison results have been provided in Table 4. Regarding Table 4, compared with most of the presented converters, as the same as other converters, the proposed topology uses the same number of magnetic cores. Meanwhile, some converters use a greater number of cores than the presented converter.

Also, for the presented converter, the number of diodes, capacitors, and switches in comparison with some converters is more, the voltage gain of the presented converter is higher, and the maximum voltage and current stress of the power switches are low. In addition, from the point of current stress of the semiconductors, compared with the other converters, the proposed structure has the lowest value of current stress. These features lead to choosing the semiconductors with a low range of voltage and current in the same condition for all compared topologies.

In addition, the proposed converter has been compared with references, as presented in Table 4, based on the voltage gain (M), switch maximum normalized (voltage stress and current stress), inductors' total current stress, diodes' total current stress, P_{out} (kW), total volume (mm^3), and power density [(W/mm^3) ($*10^{-4}$)].

The results of this comparison are provided in Table 5. In (81), the power density of the modified topology and other compared topologies is determined by the ratio of the output power (P_{out}) to the total volume of each topology. The calculation of the total volume involves summing the volumes of various components, such as energy storage elements, such as capacitors and inductors (including their cores), as well as the volume occupied by the power switches and diodes. This information is sourced from the datasheets of these components and aggregated numerically to ascertain the overall volume of each topology.

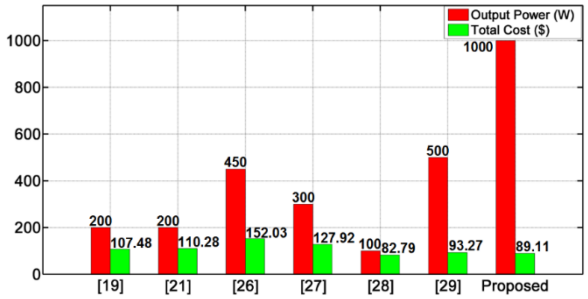


FIGURE 8. Bar graph of the cost and output power of the proposed converter and compared references.

This comprehensive approach ensures the accurate assessment of power density, considering the physical space occupied by essential elements within the power system

$$\text{Power density } (\text{W/mm}^3) = \frac{P_{\text{out}}\,(\text{W})}{\text{Total volume } (\text{mm}^3)}. \quad (81)$$

Another comparison of the proposed converter with other structures is performed based on some items, such as voltage gain (M), total current stress on switches, total voltage stress on switches, total voltage stress on diodes, total voltage stress on capacitors, total component stress factor (CSF), total switching device power (SDP), and percentage value of inductor ripple at the same condition. The results of this comparison are provided in Table 6.

Furthermore, in order to showcase the superiority of the proposed converter in terms of cost, the cost calculation for the proposed converter and the compared structures in Table 1 has been conducted and presented in Table 7. The bar graph of the cost and output power of the proposed converter and other compared topologies is shown in Fig. 8. Based on the data, as presented in Fig. 8, it is evident that the construction cost of the proposed converter for generating an output power of 1 kW is lower compared with the costs associated with the other converters analyzed for the same output power level. This cost advantage observed with the proposed converter is deemed beneficial, further highlighting its attractiveness and competitiveness relative to the alternatives under consideration.

The comparison of voltage gains, maximum normalized voltage, and current stress of switches for all converters is depicted in Fig. 9. Under the same condition for all converters, the turn ratio of the coupled inductor (n) for all converters is considered as 1.

Considering Fig. 9(a), the voltage gain of the presented converter is higher than the other Z-source converters. However, from Fig. 9(b), at constant input voltage condition for all converters, the maximum normalized voltage stress on power

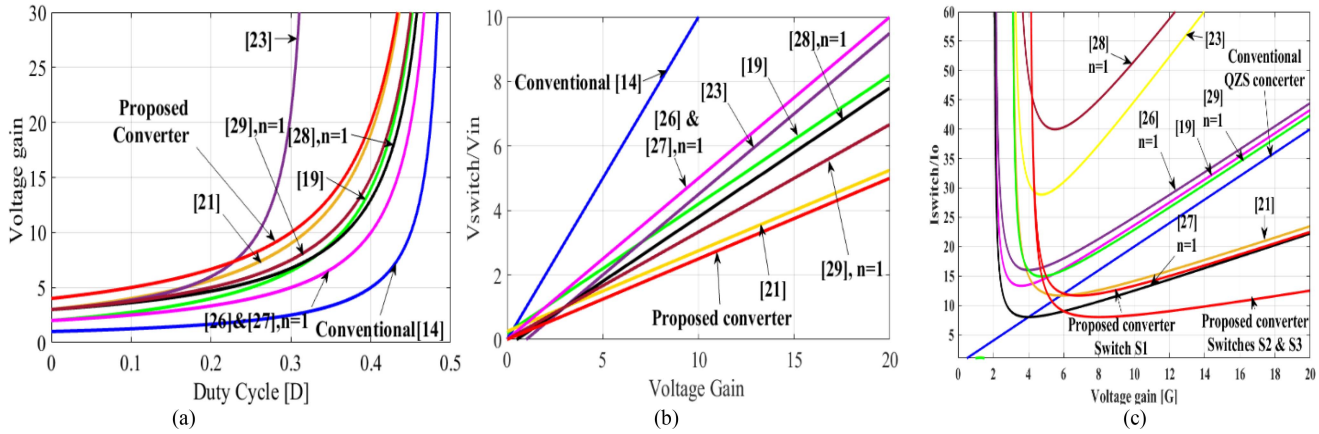


FIGURE 9. Comparison results. (a) Voltage gain. (b) Maximum normalized voltage stress on power switch. (c) Maximum normalized current stress across power switch.

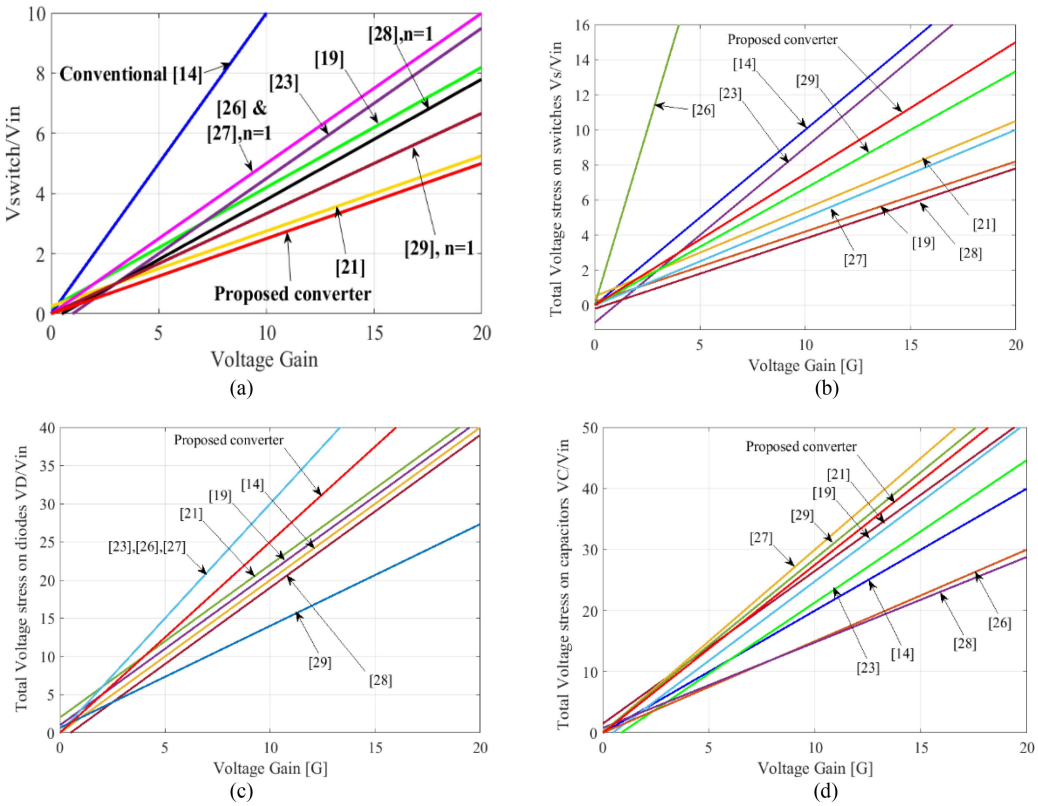


FIGURE 10. Comparison results of normalized voltage stresses. (a) Maximum normalized voltage stress on power switch. (b) Total voltage stress on power switches. (c) Total voltage stress on power diodes. (d) Total voltage stress on capacitors.

switch in terms of voltage gain for the proposed converter is low.

Also, considering Fig. 9(c), the maximum normalized current stress across the power switches of the presented converter is less than most of the other topologies at the same input current condition.

Even though, the current stress of power switch in [27] is less than the switch S_1, the current stresses across the power switches S_2 and S_3 are very lower, and the number of elements in [27] is more, which leads to higher cost and losses. Furthermore, the suggested converter is a common grounded topology and the ripple of input current is low. As a result, by consideration of the mentioned advantages, the presented converter can be operated at higher power than the other *Z*-source converters with appropriate efficiency, volume, and total cost.

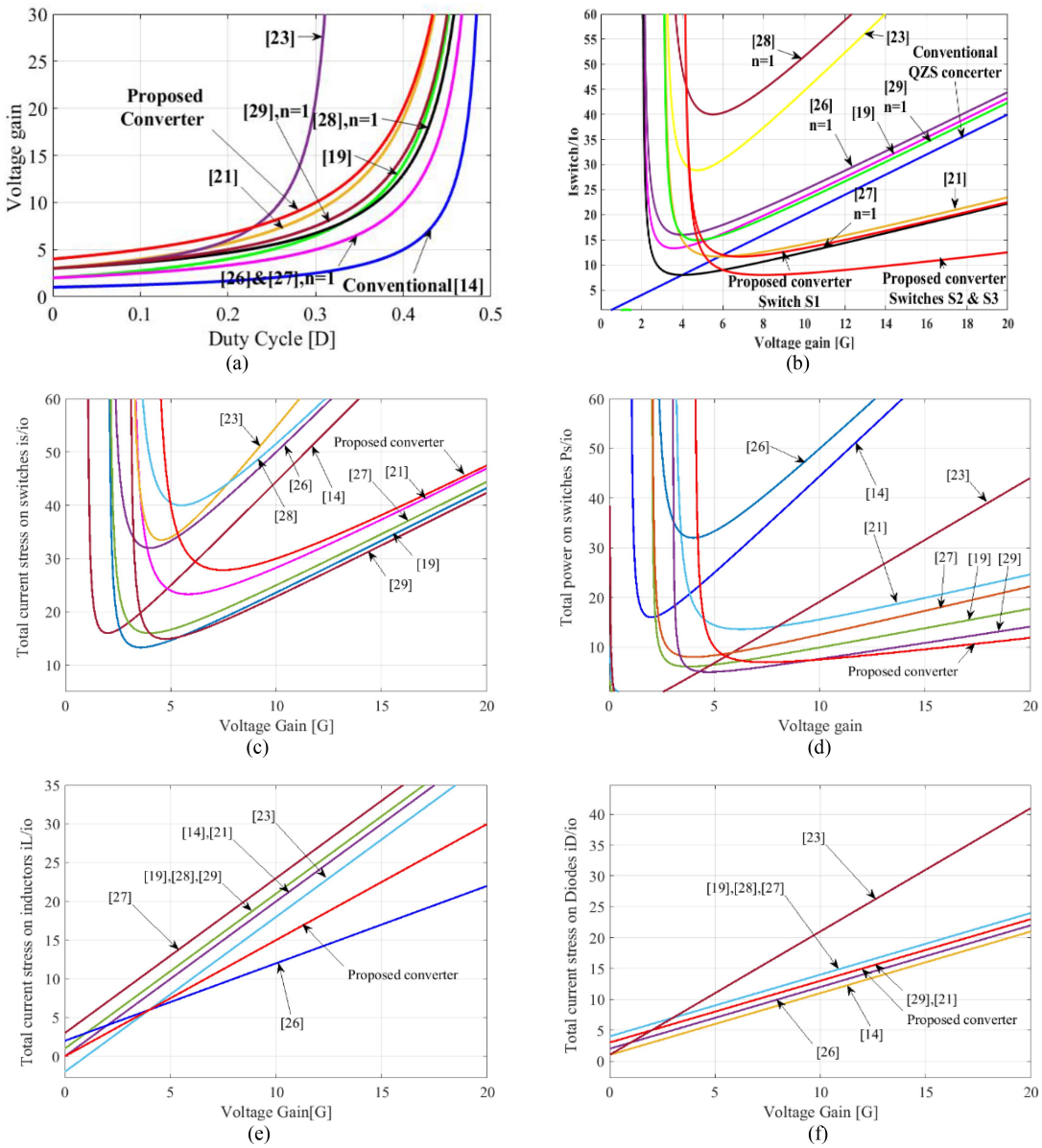
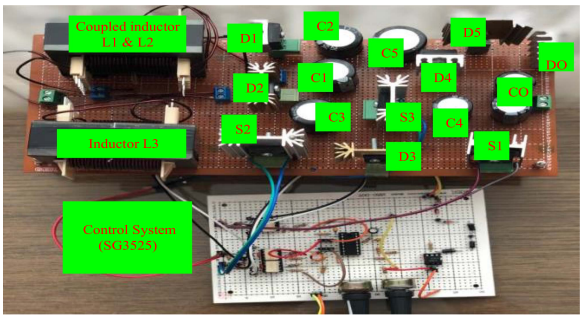


FIGURE 11. Comparison results of the presented converter. (a) Voltage gain. (b) Maximum normalized current stress across power switches. (c) Total normalized current stress across power switches. (d) Total normalized power of switches. (e) Total normalized current stress across inductors. (f) Total normalized current stress across power diodes.

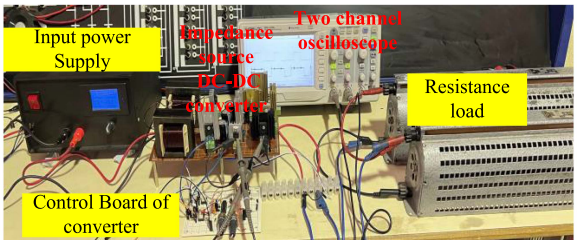
In addition, the comparison of the proposed converter with other similar converters based on the maximum normalized voltage stress on power switch, total voltage stress on power switches, total voltage stress on power diodes, and total voltage stress on capacitors is shown in Fig. 10(a)–(d), respectively. Also, Fig. 11(a)–(g) illustrates the comparison results of the presented converter based on voltage gain, maximum normalized current stress across power switches, total normalized current stress across power switches, total normalized power of switches, total normalized current stress across inductors, and total normalized current stress across power diodes. According to Fig. 11(a), the voltage gain of the proposed converter is higher than the rest of the structures, and the voltage and current stresses on the switches of the proposed converter are lower than the rest of the structures. Although the total voltage stress of the switches, diodes, and capacitors of the proposed converter is slightly higher than some of the structures, the current stress of the inductors, and most importantly from Fig. 11(d), the total power of the switches in the proposed structure is lower than other structures. All of these features show that the proposed converter can operate at a higher power than the other converters.

VII. EXPERIMENTAL RESULTS

In this section, in order to confirm the theoretical analysis, the experimental test results of a 1-kW prototype are evaluated,



(a)



(b)

FIGURE 12. (a) Photograph of the laboratory prototype, (b) Control system.

TABLE 8. Experimental Prototype Specification of the Presented Converter

Component	Description
Input voltage	60 V
Maximum Output dc voltage	650 V
Maximum Output power	1 kW
Switching Frequency	40 kHz
Coupled Inductor L_1 and L_2	350 µH EE65 ferrite core
Inductor L_3	700 µH EE65 ferrite core
Capacitor C_1, C_2, and C_3	220 µF 200 V
Capacitor C_4	68 µF 450 V
Capacitor C_5	100 µF 500 V
Capacitor C_O	220 µF 2*450 V
Diode D_2, D_3, and Do	SFAF2004G 200 V–20 A
Diode D_1, D_4, and D_5	IXYS DSEI30-06 600 V–37 A
MOSFET S_1, S_2, and S_3	IRFP260N 200 V–50 A

which has been built in the laboratory. The laboratory prototype with the control system is shown in Fig. 12(a) and (b), respectively.

The values of used components in the experimental prototype are gathered in Table 8. Based on Fig. 12, in the control system, an industrial IC SG3525 has been utilized to obtain simple drive and control of the power MOSFETs. Although the number of the power MOSFETs is three, this IC produces two output pulses with 180 phase-shift degrees. These gate pulses are applied to power switches with three TLP260 drivers. Regarding Table 2, the input voltage is 60 V and the switching frequency is set to 40 kHz with the approximated duty ratio of 32.5% in the control system.

By considering the mentioned information, the experimental results of output and capacitor voltages are demonstrated in Fig. 13. From Fig. 13(a), the output voltage is about 650 V and the voltage of capacitor C_1 is about 109 V. The experimental voltage gain is about 10.83 and the theoretical voltage gain is about 11.42, which confirm each other. The voltages of capacitor C_2 and C_5 are about 51 V and 489 V, respectively, which are shown in Fig. 13(b). Fig. 13(c) and (d) shows the voltages of capacitors C_3 and C_4, which are about 163 V and 328 V, respectively.

By consideration of the total losses of the presented converter, mentioned input voltage, and duty ratio, all these voltage values confirm the theoretical analysis. In Fig. 14, the experimental waveforms of the semiconductors are illustrated.

From Fig. 14(a) and (b), the voltage stresses across the power MOSFET S_1, diode D_3, power MOSFET S_2, and diode D_2 are about 160 V, respectively. As well as, 180° phase shift between V_{DS1} and V_{DS1} can be observed.

In Fig. 14(c), the maximum voltage stresses on diodes D_5 and D_O are shown, which are 489 and 160 V approximately.

In addition to the voltage stresses, the current waveforms of diodes D_1 and D_4 are displayed in Fig. 14(d) and (e) to confirm the accuracy of theoretical analysis. As it can be seen, the maximum voltage stresses on D_1 and D_4 are 160 V and 489 V, respectively.

All the above-mentioned values prove that all experimental results follow the theoretical equations. The current waveforms of inductor L_3 and coupled inductors L_1 and L_2 are displayed in Fig. 15(a).

As it can be observed from this figure, the ripple and average currents of coupled inductor L_1 and inductor L_3 are equal. Also, there is a 180° phase shift between these currents, which is the only difference between them. The average value of these currents is about 8.79 A, which follows the theoretical currents' equations. The input current of the presented converter is evaluated in Fig. 15(b). As it can be seen, due to the sum of currents of the inductors L_1 and L_3, the ripple of input current is low and the average value of this current is about 17.58 A.

The dynamic response of the presented converter is displayed in Fig. 16. The dynamic response of the open-loop control system is shown in Fig. 16(a). At first, the input voltage is 60 V and the output voltage is about 650 V, then the input voltage decreases to 34 V in 350 ms. In this time interval, the output voltage decreases to 365 approximately, which shows that the presented converter follows the theoretical analysis with an appropriate dynamic response. Also, the dynamic response of the proposed converter with input voltage variation in a closed-loop system is illustrated in Fig. 16(b). In this part, the input voltage is variated but the output voltage is not affected by input voltage changing. All these results show that the proposed converter has better dynamic responses. As well as in Fig. 16(c), the dynamic response of the closed-loop system with load variation is illustrated.

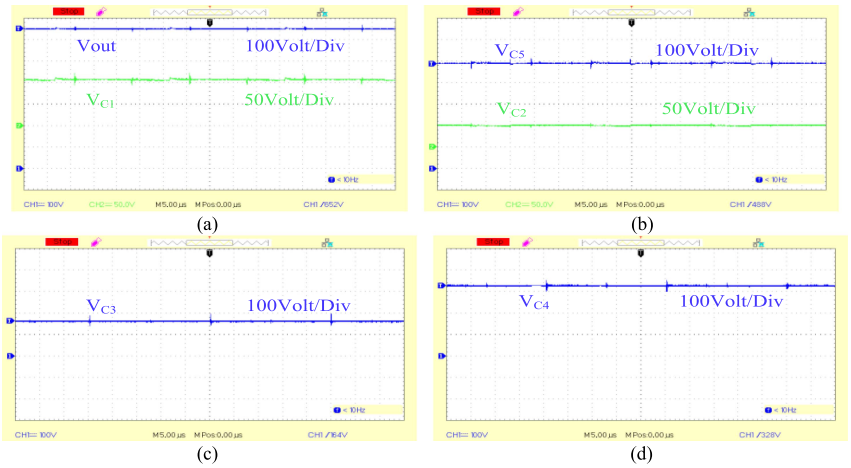


FIGURE 13. Voltages of output and capacitors. (a) Output voltage and voltage of capacitor C_1. (b) Voltage of capacitors C_2 and C_5. (c) Voltage of capacitor C_3. (d) Voltage of capacitor C_4.

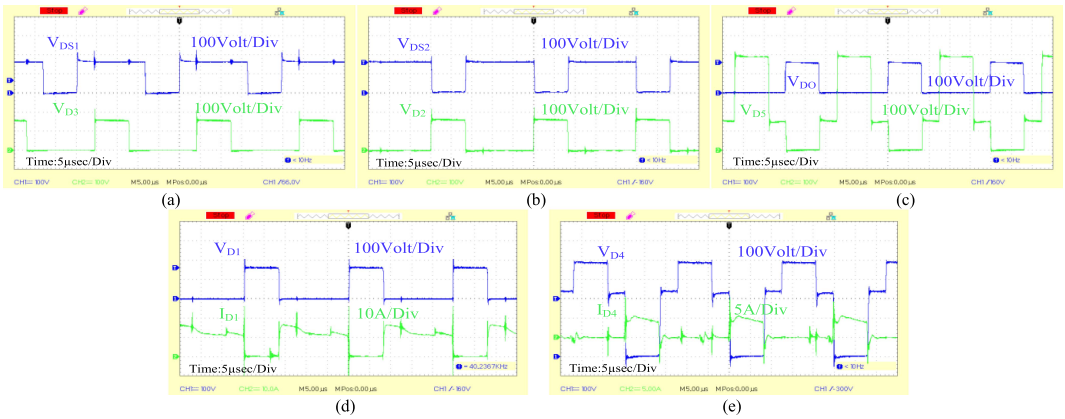


FIGURE 14. Experimental waveforms of semiconductors. (a) Voltage stress on power switch S_1 and diode D_3. (b) Voltage stress on power switch S_2 and diode D_2. (c) Voltage stress on diodes D_5 and D_O. (d) Voltage and current of diode D_1. (e) Voltage and current of diode D_4.

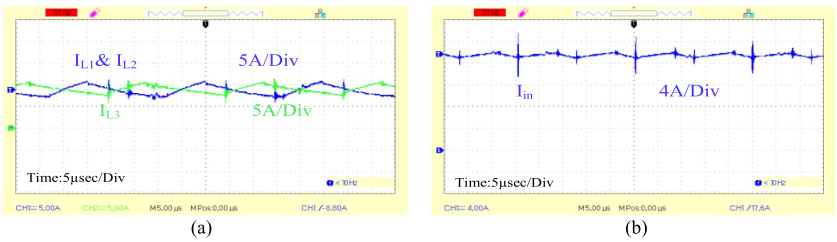


FIGURE 15. Current waveforms. (a) Current of inductors L_1, L_2, and L_3. (b) Input current.

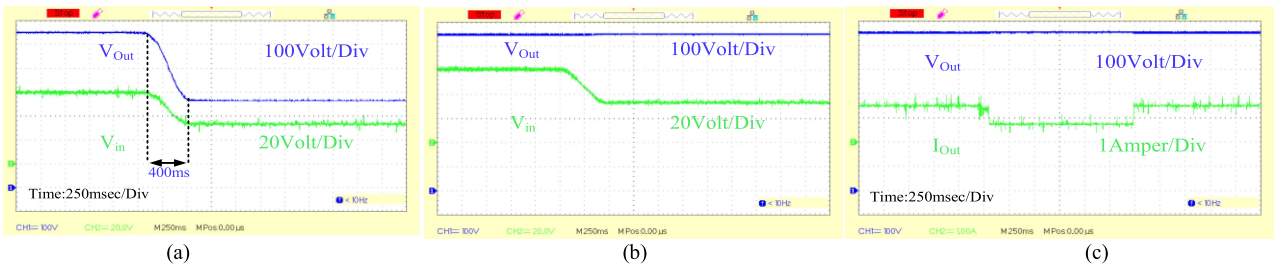


FIGURE 16. Dynamic response of the presented converter. (a) Open-loop system with input voltage variation. (b) Closed-loop system with input voltage variation. (c) Closed-loop system with load variation.

As it can be observed, at first, the output current is 1.53 A (full load) and the output voltage is about 650 V.

Then, by the sudden change in load, the current decreases to half the amount of full-load current and, after a while, increases to the full-load current. However, the output voltage of the converter is fixed to 650 V, which proves that the closed-loop control system has a good dynamic response.

VIII. CONCLUSION

In this study, a new high step-up dc–dc converter based on the quasi-*Z*-source network with low input current ripple and using a voltage multiplier cell is proposed. The important advantages that distinguish the presented converter from other *Z*-source converters are included as follows: High voltage gain, common grounded feature, leakage current elimination in the PV-based applications, low current and voltage stress across the power switches, extended duty ratio, good efficiency at high output voltage, and high power with small duty ratio in comparison with the conventional *Z*-source-based converters.

All above-mentioned characteristics are compared with other *Z*-source converters and the mathematical analysis with the operating principle has been examined. Finally, a 1-kW experimental laboratory prototype of the proposed converter has been built to prove all the mathematical analyses and above-mentioned advantages. In addition, the measured efficiency of the presented converter at 1 kW is about 94.6%, which shows that the efficiency of this converter is higher than the other *Z*-source-based converter at high power conditions. Therefore, this *Z*-source-based converter can achieve suitable efficiency at high power conditions than the other *Z*-source converters, which is appropriate for RES applications, such as PV systems.

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