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Modeling and Understanding the Compact Performance of h-BN Dual-gated ReS₂ Transistor

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In this study, high-performance few-layered ReS₂ field-effect transistors (FETs), fabricated with hexagonal boron nitride (h-BN) as top/bottom dual gate dielectrics, are presented. The performance of h-BN dual gated ReS₂ FET having a trade-off of performance parameters is optimized using a compact model from analytical choice map, which is consisted of three regions with different electrical characteristics. The bottom h-BN dielectric has almost no defects and provides a physical distance between the traps in the SiO₂ and the carriers in the ReS₂ channel. Using a compact analyzing model and structural advantages, we introduce an excellent and optimized performance of h-BN dual-gated ReS₂ having a high mobility of 46.1 cm²V⁻¹s⁻¹, a high current on/off ratio of ~10⁶, a subthreshold swing of 2.7 Vdec⁻¹, and a low effective interface trap density ($N_{t,eff}$) of 7.85×10^{10} cm⁻²eV⁻¹ at a small operating voltage (< 3 V). We demonstrate these phenomena through not only a fundamental current-voltage analysis, but also technology computer aided design (TCAD) simulations, time-dependent current, and low-frequency (LF) noise analysis. In addition, we introduce a simple method to extract the interlayer resistance of ReS₂ channel through Y-function method as a function of constant top gate bias.

1. Introduction

Si technology faces fundamental limitations due to ever-reducing gate lengths and the consequent decreased gate controllability.^[1] Transition-metal dichalcogenide (TMD) materials are promising candidates to replace the Si channel because of their high carrier mobility, excellent applicability, mechanical, optical, and electrical properties.^[2-10] Among these numerous TMD materials, rhenium disulfide (ReS₂) has a distorted 1T structure^[11] with higher interlayer resistance (R_{int}) compared to other TMD materials,^[12,13] and anisotropic electrical and optical properties.^[13,14] Recently, in comparison with the well-known molybdenum disulfide (MoS₂), which has the 2H phase, ReS₂ has attracted significant attention because of its direct

bandgap from single layer to bulk since each layer is decoupled from the other.^[15] Although field-effect transistors (FETs) using ReS₂ as a channel have been widely reported, their performance is inferior to those of MoS₂, because ReS₂ FETs have low mobility, low current on/off ratio, and large subthreshold swing.^[16] To overcome this low performance, h-BN was used as a gate dielectric, graphene contact or suspended structure were designed for next-generation devices.^[17,18] However, the mobility, threshold voltage, subthreshold swing, and current on/off ratio of ReS₂ FETs have a trade-off relationship at typically only improved separately, at the cost of degrading another.^[16-18] Consequently, further research to correctly understand its electrical characteristics and optimize the performance is required. Since TMD materials like ReS₂ have a large surface/volume ratio, the interface between the TMD channel and the gate dielectrics affects the performance of the devices significantly.^[19-21] Therefore, usage of a h-BN gate dielectric,^[22] which has almost no dangling bonds acting as charge carrier traps, or a dual-/tri- gated structure^[23] to increase gate controllability, can lead to an improvement in the performance of FETs.

In this work, by understanding the electrical characteristics of top/bottom h-BN dual-gated ReS₂ FETs, optimized performance parameters are presented. In particular, when the bottom gate voltage is swept, while keeping the top gate bias constant, two transconductance (g_m) peaks are observed in a specific region, being an indication of two separate conduction paths. Therefore, we present an analytic choice map that enables compact modeling depending on the top/bottom gate voltage conditions. Variations in the fixed top gate bias on the other hand, cause a band bending of channel and a change in its conduction path, resulting in trapping at interface traps and variations of the mobility and subthreshold swing. In addition to analysis of fundamental current-voltage characteristics (I_D - $V_{BG(TG)}$, I_D - V_D), technology computer aided design (TCAD) simulations, time-dependent current fluctuations, and low-frequency (LF) noise spectra analysis are also performed. Time-dependent current fluctuations and LF noise analysis in the

frequency domain obtained through Fourier transform provide strong support for the analytic choice map. In addition, we introduce a simple Y- function method^[24,25] for extracting the approximate interlayer resistance by separated conduction path according to the top gate bias without any simulations or fabrications of device by channel thickness.^[12,26,27]

2. Results and Discussion

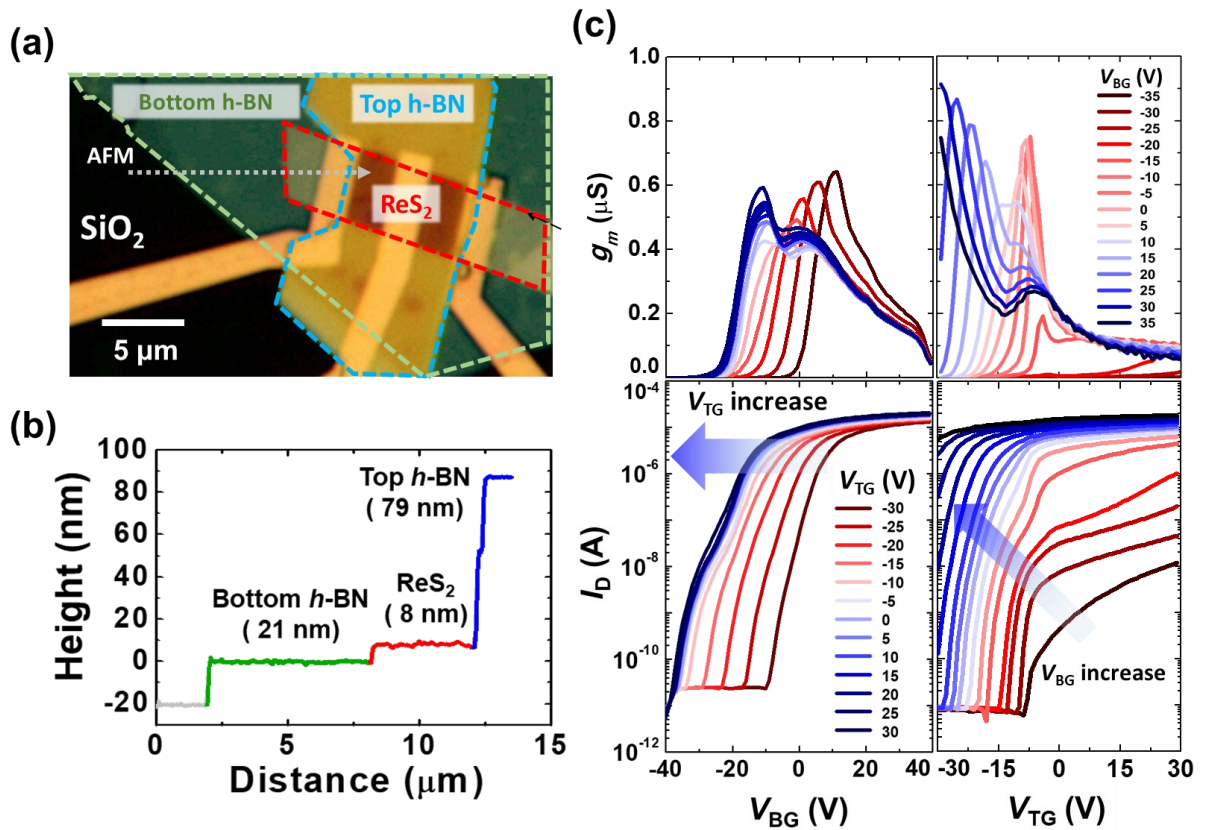


Figure 1. (a) Optical microscopy image of h-BN dual gated few-layer ReS₂ FET. (b) Height profile of the top/bottom h-BN dielectrics and few-layer ReS₂ channel. (c) Transconductance (g_m - $V_{BG(TG)}$) and transfer characteristics (I_D - $V_{BG(TG)}$) of dual gated ReS₂ FET applying different top (bottom) gate voltages ($V_{TG(BG)}$).

2.1. Optical image and electrical characteristics with different voltages

We fabricated h-BN dual-gated ReS₂ field-effect transistor (FET) on a Si/SiO₂ substrate by micro contact transfer method (See **Figure S1**). The optical microscope image of the fabricated h-BN dual-gated ReS₂ FET with source/drain electrode and top gate electrode is shown in

Figure 1a. The length and width of the ReS₂ channel are 6.2 and 4.8 μm, respectively, and above the top h-BN dielectric layer, the gate electrode with a length of 2 μm is located centrally with respect to the source and the drain. **Figure 1b** shows the thickness profile of the bottom/top h-BN layers and ReS₂ channel measured using atomic force microscope (AFM). The thickness of the bottom h-BN layer is 21 nm, which allows to generate a large enough physical distance between the SiO₂ interface traps and the ReS₂ channel, therefore reducing the influence of the traps on the carriers.^[28] The thickness of ReS₂ channel between the top and the bottom h-BN layers is 8 nm (≈ 10 layers). The thickness of the top layer h-BN layer is 79 nm and used as a top gate dielectric. In addition, the optical Raman spectra of ReS₂ and h-BN were measured with a laser wavelength of 532 nm. The typical Raman peaks at 160 cm⁻¹ (E_g) and 217 cm⁻¹ (A_g -like) were observed in the ReS₂ channel and a main peak of 1366 cm⁻¹ was observed in h-BN layers (see **Figure S2a** and b).^[30,31]

Figure 1c shows the measured transfer characteristics (I_D - $V_{BG(TG)}$) and transconductance curves (g_m - $V_{BG(TG)}$) at different applied top (V_{TG}) or bottom gate biases (V_{BG}). I_D - V_{BG} are measured by sweeping the V_{BG} , with $V_D = 1$ V and for various V_{TG} biases and is showing n-type characteristics with a current on/off ratio of 10⁶. On the other hand, when the V_{TG} is swept with fixed V_{BG} , I_D - V_{TG} shows n-type characteristics where the on-current is changing significantly according to the applied V_{BG} bias. The reason for this phenomenon is that the entire length of the ReS₂ channel is not fully covered with the top gate electrode, and therefore an according minimum V_{BG} is required to turn on the device. In both the top and the bottom gate voltage sweeps, the transconductance curves (g_m - $V_{BG(TG)}$) show two separate g_m peaks when the top (bottom) gate bias ($V_{TG(BG)}$) exceeds a certain threshold. These two separate g_m peaks indicate that two separate conduction paths being formed due to weak interlayer coupling of ReS₂.^[15] Since high gate leakage current causes errors in g_m peak extraction, small gate currents are essential. Our devices show very low values $I_G < 100$ pA in all measurements (see **Figure S3a** and b). In addition, as the thickness of the ReS₂ channel becomes thinner, only one g_m peak is

observed as the vertical electric field exerts an effect on the entire layer (see **Figure S4**). The output characteristics (I_D - V_D) show linear behavior regardless of the V_{TG} or V_{BG} , resulting in an Ohmic contact at source/drain (see **Figure S5a** and **b**).

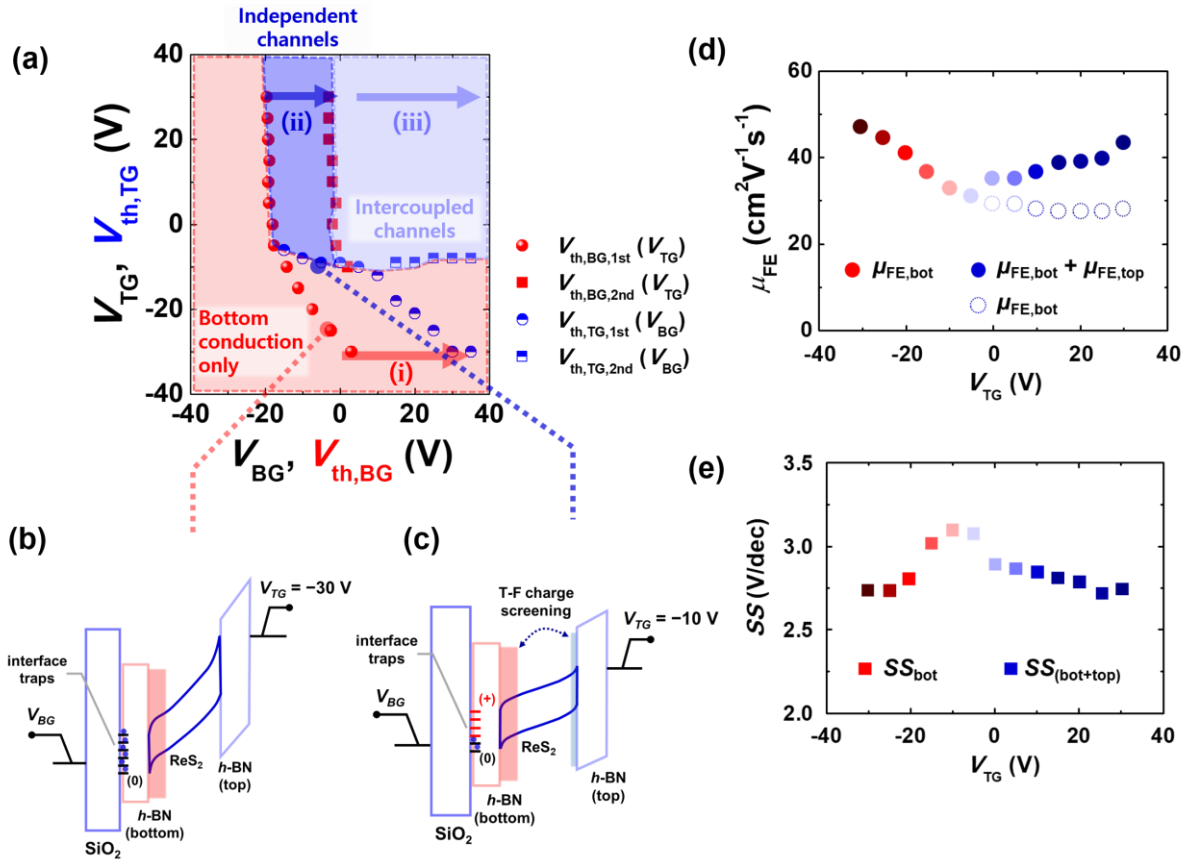


Figure 2. (a) Analytical choice map for the threshold voltage (V_{th}) distributions of h-BN dual-gated ReS₂ FET with three different regions (bottom conduction only, independent channels, and intercoupled channels). Symbols show the variation of the bottom-gate-sweep threshold ($V_{th,BG}$) as a function of constant top-gate bias and the top-gate-sweep threshold ($V_{th,TG}$) as a function of constant bottom-gate bias, respectively (Symbols are extracted from the first and second transconductance peaks). Band diagrams with interface traps and a channel, when V_{TG} being (b) -30 V and (c) -10 V. (d) Field-effect mobility (μ_{FE}) and (e) subthreshold swing (SS) variations according to different V_{TG} .

2.2. The interrelationship of the two conduction paths

Through the second derivative method, threshold voltages ($V_{th, TG(BG)}$) extracted from g_m - $V_{TG(BG)}$ curves are shown in **Figure 2a**. These threshold voltage variations are obtained from the first and the second g_m peaks as a function of the constant applied top or bottom gate bias. The threshold voltage dependencies also called as analytical choice map can be divided into three regions by the interrelationship of the top and the bottom conduction paths.

In the first region, as shown in **Figure 2b**, only the bottom conduction path is mainly formed when $V_{TG} < -10$ V is applied, and $V_{th, BG, 1st}(V_{TG})$ is negatively shifted as the applied V_{TG} increases. When $V_{BG} < -20$ V and $V_{TG} > 0$ V are applied, only a small amount of bottom conduction path is formed because the top gate electrode covers only part of the channel length. The shift of $V_{th, BG, 1st}(V_{TG})$ in the bottom conduction path is explained by band bending according to the applied V_{TG} and electron carrier trapping/detrapping at the interface traps between the SiO₂ and h-BN. When $V_{TG} = -30$ V is applied, the band on the top h-BN side rises as shown in **Figure 2b**, confining the carriers in the ReS₂ channel into the bottom conduction path, as well as increasing the average Fermi level of ReS₂ channel. The donor-like interface traps at the interface between SiO₂ and h-BN are mostly trapped and turned into neutral state by electrons, showing a threshold voltage ($V_{th, BG, 1st}$) of 2.7 V when sweeping V_{BG} . When the more positive V_{TG} is applied, however, the band on the top h-BN side and average Fermi level of ReS₂ channel are lowered, resulting in detrapping of electrons from the interface traps. Therefore, some of interface traps turn into positive charges and $V_{th, BG, 1st}$ moves in a negative direction. As a result, the band bending by V_{TG} bias and the electrostatic impact of the interface charge are the main factors of the variations in the current density distribution, and interface charges have great influences on carrier mobility via coulomb scattering and on hysteresis.

When a $V_{TG} > -10$ V is applied, however, $V_{th, BG, 1st}$ no longer shifts and $V_{th, BG, 2nd}$ begins to occur as the top conduction path is starting to be formed. This phenomenon in the second region occurs because the top conduction path formed as shown in **Figure 2c** induces the Thomas-

Fermi (T-F) charge screening effect.^[32] The T-F charge screening effect is more pronounced in ReS₂, which has weak interlayer coupling characteristics, and the top gate bias no longer affects the bottom conduction path, resulting in forming independent top and bottom conduction paths.

Finally, in the third region ($V_{TG} > -10$ V and $V_{BG} > 10$ V), a sufficiently large back gate bias affects the overall ReS₂ channel vertically, forming intercoupled channels in which the top/bottom conduction paths are mutually affected. As shown in **Figure S6c**, two main paths according to the applied V_{TG} is observed through SILVACO TCAD simulation using the material parameters of h-BN and ReS₂ as shown in **Table S2**.^[33–37]

Figure 2d and **e** show the field-effect mobility (μ_{FE}) and the subthreshold swing (SS) variations as a function of the constantly applied V_{TG} , extracted from I_D - V_{BG} , respectively. The μ_{FE} variation according to V_{TG} extracted by the maximum values of g_m - V_{BG} (see **Figure 2d**) shows an excellent carrier mobility of $46.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ when $V_{TG} = -30$ V is applied, compared to those of previous studies (see **Table S1**).^[34,38–41] As the applied V_{TG} increases, the positively charged interface traps through band bending also increase, the carrier mobility decreases continuously until $V_{TG} = -5$ V, after which it is no longer reduced due to the T-F charge screening effects by top conduction path. Rather, since the mobilities of the top conduction path are included after -10 V of V_{TG} , the mobilities ($\mu_{FE,bot} + \mu_{FE,top}$) slightly increase, but when $\mu_{FE,top}$ extracted from g_m - V_{BG} are removed, $\mu_{FE,bot}$ remain almost constant. The tendency of the subthreshold swing variation as a function of V_{TG} is similar to that of the carrier mobility. When $V_{TG} = -30$ V, the subthreshold swing shows the best performance of 2.7 V/dec. In addition, as the carrier concentration of the top conduction path is included, the subthreshold swing is rather slightly reduced after -10 V of V_{TG} .

2.3. Time-dependent current and low-frequency noise analysis

Time-dependent current measurement and low-frequency (LF) noise measurement are nondestructive and efficient analysis techniques to identify trapping/detrapping phenomena of carriers.^[28,42–49] The measurements for time-dependent current and LF noise were performed to further understand the phenomena of interaction of top and bottom conduction paths in the h-BN dual-gated ReS₂ channel. Specific V_{BG} and V_{TG} voltages were applied to the device with $V_D = 1$ V, and the current fluctuations (ΔI_D) as a function of time, which were amplified by a current amplifier, were measured for 1 s with a sampling rate of 30 μ s. Then, power spectral densities (S_{I_D}), time-dependent current fluctuations, and probability density as a function of current values were analyzed through Python.

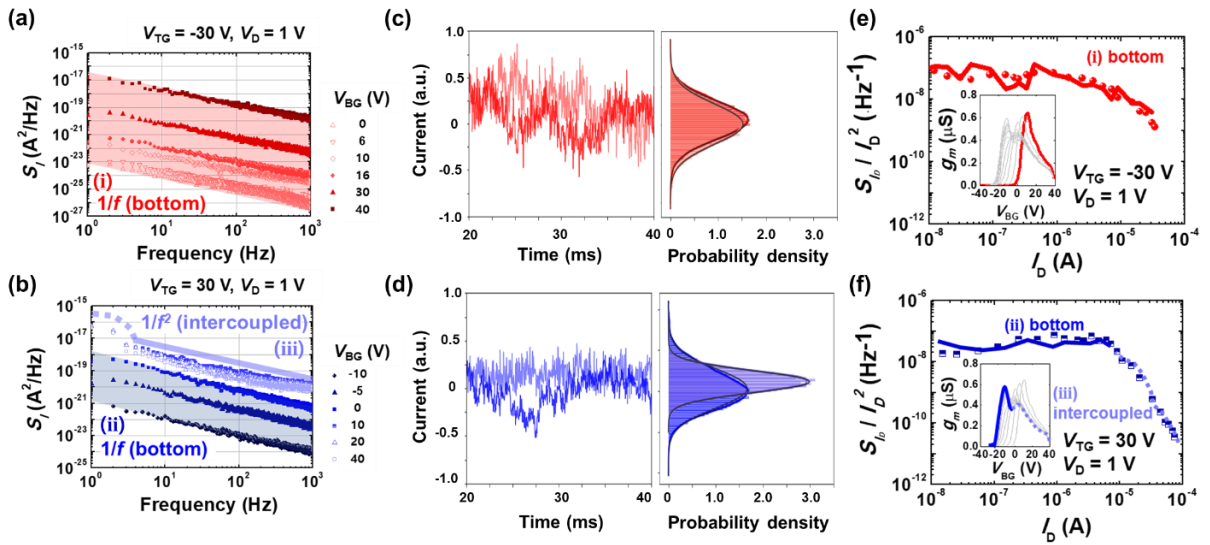


Figure 3. The variations of power spectral densities (S_{I_D}) at $V_D = 1$ V, when V_{TG} of (a) -30 V and (b) 30 V. Normalized current fluctuations (ΔI_D) and probability densities of ΔI_D , measured at V_{TG} of (c) -30 V and (d) 30 V. The variations in the measured S_{I_D}/I_D^2 as a function of V_{BG} at $f = 15$ Hz and $V_D = 1$ V, when the V_{TG} of (e) -30 V and (f) 30 V (The insets show g_m - V_{BG} curves).

Figure 3a shows the variation of S_{I_D} at $V_{TG} = -30$ V and $V_D = 1$ V with increasing V_{BG} , indicating $1/f$ behavior at all V_{BG} regions (see the region (i) in **Figure 2a**). The S_{I_D} increases with increasing V_{BG} and shows a $1/f$ trend for all V_{BG} , which represents the noise spectra between the bottom conduction path and the interface trap as $V_{TG} = -30$ V is applied. As shown in the region (ii) of **Figure 2a**, the S_{I_D} , measured at $V_{TG} = 30$ V shows $1/f$ behavior for the independent bottom conduction path when $V_{BG} < 0$ V in **Figure 3b**. However, they start to behave as the summation of $1/f$ and $1/f^2$ (Lorentzian shape) when $V_{BG} > 10$ V (see the region (iii) in **Figure 2a**), given by **Equation 1**:^[48,50–52]

$$S_{I_D} = \frac{K_f}{f} + \frac{A}{1 + (\frac{f}{f_o})^2} \quad \text{(Equation 1)}$$

where K_f is a coefficient indicating the amplitude of the $1/f$ behavior, the second term is the sum of $1/f^2$ component with the plateau value A , f_o is the frequency of the generation-recombination (G-R) noise component associated with the time constant ($\tau = 1/2\pi f_o$) of the interface traps located at the interface between the SiO_2 and the bottom h-BN.

The sum of $1/f$ and $1/f^2$ shows that mutually intercoupled top/bottom conduction paths are generated, and the intercoupled top conduction path represents a Lorentzian shape ($1/f^2$, G-R) due to these two factors. (1) larger physical distance between the interface traps and the carriers in top conduction path than that of bottom conduction path and (2) T-F charge screening effect by the intercoupled bottom conduction path.

Interestingly, as shown in **Figure 3c**, the normalized current fluctuations (ΔI_D) are slightly different depending on the V_{BG} , but the probability densities at all V_{BG} have the same Gaussian distributions with the mean value of ≈ 0 and the standard deviation of ≈ 0.25 (see **Figure 3c**). Gaussian distribution of the normalized current fluctuations in h-BN dual gated ReS_2 FET is given by **Equation 2**.^[47,48,50]

$$f(\Delta I_D | \mu_i, \sigma_i^2) = \frac{1}{\sqrt{2\pi\sigma_i^2}} e^{-\frac{(\Delta I_D - \mu_i)^2}{2\sigma_i^2}} \quad (\text{Equation 2})$$

where i depends on the trapping/detrapping phenomena and the type of traps, μ_i is the mean, and σ_i^2 is the variance.

As such, the fact that probability densities of all V_{BG} follow the same Gaussian distribution means that only the bottom conduction path causes trapping/detrapping of carriers at $V_{TG} = -30$ V.

In addition as shown in **Figure 3d**, the effect of two conduction paths is also shown in the probability densities of the ΔI_D measured at $V_{TG} = 30$ V. The probability densities at $V_{BG} < 10$ V show Gaussian distributions, which are associated with independent bottom conduction path, exactly the same as those of $V_{TG} = -30$ V with the same mean value (μ_1) of ≈ 0 and the same standard deviation (σ_1) of ≈ 0.25 . At $V_{BG} > 10$ V. However, the different Gaussian distributions with μ_2 of ≈ 0.11 and σ_2 of ≈ 0.13 are observed by the intercoupled top/bottom conduction paths.

Corresponding to the above phenomena, the normalized drain current spectral densities (S_{I_D}/I_D^2) as a function of drain current at various V_{BG} as measured at $V_{TG} = -30$ V and 30 V are shown in **Figure 3e** and **f**, respectively.

The measured S_{I_D}/I_D^2 at $V_{TG} = -30$ V in **Figure 3e** are fitted to the carrier number fluctuation, correlated with the mobility fluctuation (CNF-CMF) model, which can be expressed as:^[47,50]

$$\left. \frac{S_{I_D}}{I_D^2} \right|_{V_{TG}=-30V} = \frac{q^2 k T \lambda N_{t,eff}}{f W L C^2} \left(1 + \frac{\alpha_{SC} \mu_{eff,bot} C I_D}{g_m} \right)^2 \left(\frac{g_m}{I_D} \right)^2 \quad (\text{Equation 3})$$

where q is the charge of electron, k is the Boltzmann constant, T is the 300 K, λ is the tunneling attenuation length, $N_{t,eff}$ is the effective interface trap density, f is the frequency, C is the dielectric capacitance per unit area calculated by the bottom h-BN with SiO₂, g_m is the

transconductance ($= \partial I_D / \partial V_{BG}$) at $V_{TG} = -30$ V, α_{SC} is the scattering parameter, $\mu_{eff,bot}$ is the effective mobility.

Based on the measured S_{I_D}/I_D^2 at $V_{TG} = -30$ V fitted into the CNF-CMF model, $N_{t,eff}$ of 7.85×10^{10} $\text{cm}^{-2}\text{eV}^{-1}$ and α_{SC} of 1.3×10^5 VsC^{-1} , which are calculated through the bottom conduction path of ReS₂ channel, are further improved compare to those of previous studies.^[40,53,54]

At $V_{TG} = 30$ V, however, the measured S_{I_D}/I_D^2 are not fitted by only one CNF-CMF model, but perfectly fitted by two different CNF-CMF models as shown in **Figure 3f**. The measured S_{I_D}/I_D^2 are divided into two regions by the point at $I_D \approx 10$ μA ($V_{BG} = 5$ V), and before this point, S_{I_D}/I_D^2 are influenced by the independent bottom conduction path and afterwards by the mutually intercoupled top/bottom conduction paths.

The effective interface trap densities and scattering parameters affected by the top/bottom conduction path are well fitted to two kinds of CNF-CMF models, respectively, which can be expressed as:

$$\begin{aligned} \left. \frac{S_{I_D}}{I_D^2} \right|_{V_{TG}=30V} = & \left[S_{Vfb,bottom} (1 + \alpha_{SC,bottom} \Omega_{bottom})^2 \right]_{I_D < 10 \mu A} \\ & + S_{Vfb,intercoupled} (1 + \alpha_{SC,intercoupled} \Omega_{intercoupled})^2 \Big|_{I_D > 10 \mu A} \left(\frac{g_m}{I_D} \right)^2 \end{aligned}$$

(Equation 4)

where $\Omega_{bottom(intercoupled)} = \mu_{eff,bottom(intercoupled)} C I_D g_m^{-1}$, and $S_{Vfb,bottom(intercoupled)} = N_{t,eff,bottom(intercoupled)} q^2 k T \lambda_f^{-1} W^{-1} L^{-1} C^{-2}$ are power spectral densities obtained from the bottom (and intercoupled) conduction paths, respectively.

Based on the measured S_{I_D}/I_D^2 at $V_{TG} = 30$ V fitted into the different CNF-CMF models, $N_{T,eff,bottom}$ of 1.02×10^{11} $\text{cm}^{-2}\text{eV}^{-1}$ and $\alpha_{SC,bottom}$ of 1.0×10^5 VsC^{-1} , which are calculated

through the independent bottom conduction path of ReS₂ channel, are slightly degraded than those of $V_{TG} = -30$ V. On the other hand, $N_{T,eff,intercoupled}$ of $8.02 \times 10^8 \text{ cm}^{-2}\text{eV}^{-1}$ and $\alpha_{SC,intercoupled}$ of $1.0 \times 10^2 \text{ VsC}^{-1}$ at $V_{TG} = 30$ V calculated through fitting by the intercoupled top conduction path are substantially less affected due to the two reasons described above and show extremely low values.

2.4. Simple method to extract interlayer resistance of few-layer ReS₂ using the Y-function method

The Y-function method, which is also called drain current ratio method, is designed to avoid the dependence of the obtained V_T on R_{SD} and reduction of mobility.^[24,55,56]

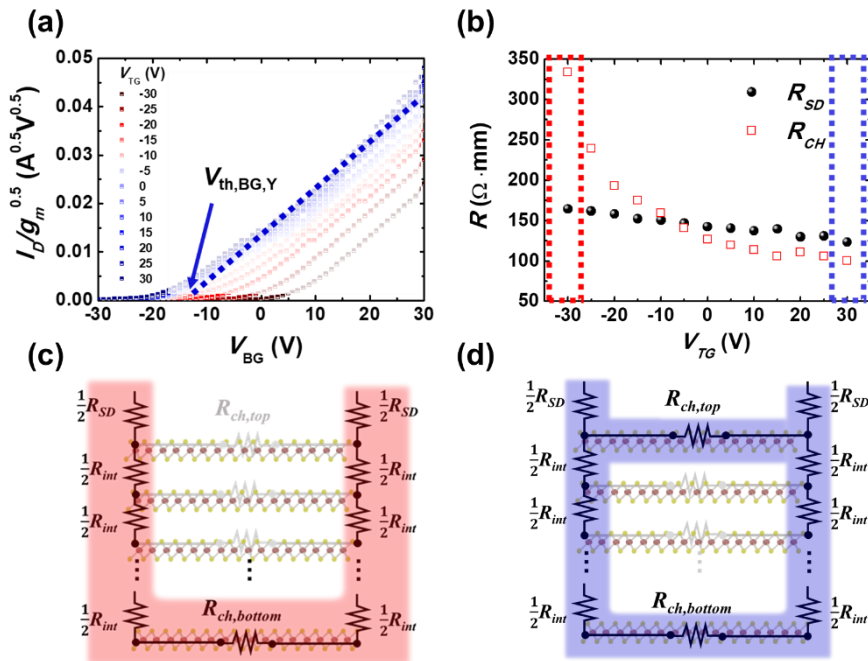


Figure 4. (a) Y-function ($I_D/g_m^{0.5}-V_{BG}$) with the linear fitting in the strong inversion, when different V_{TG} is applied. (b) The R_{SD} and R_{CH} as function of V_{TG} , extracted by Y-function method. Illustrations of current path in dual-gated few-layer ReS₂ FET when (c) -30 V and (d) 30 V of V_{TG} is applied, respectively.

Figure 4a shows Y-function ($I_D/g_m^{0.5}-V_{BG}$) with various V_{TG} applied, given **Equation 5**, and by performing a linear fit at the constant Y, the point where $I_D/g_m^{0.5} = 0.015 \text{ A}^{0.5}\text{V}^{0.5}$, the new threshold voltages ($V_{th,BG,Y}$) are extracted. In **Equation 6**, the variations in R_{SD} and R_{CH} according to different V_{TG} extracted by ignoring the change in an intrinsic attenuation factor (θ_{10}) at constant Y are shown in **Figure 4b**. ($I_D = I_{D,bot} + I_{D,top}$)

$$Y = \frac{I_D}{\sqrt{\frac{\partial(I_{D,bot}+I_{D,top})}{\partial V_{BG}}}} = \left(\frac{W}{L} C \mu_0 V_D\right)^{\frac{1}{2}} (V_{BG} - V_{th,BG,Y}) + \frac{I_{D,top}}{\sqrt{g_{m,bot}}} \quad \text{(Equation 5)}$$

$$I_D = \frac{W}{L} C \left[\frac{\mu_0}{1+(\theta_{10}+R_{SD}C\mu_0\frac{W}{L})(V_{BG}-V_{th,BG,Y})} \right] (V_{BG} - V_{th,BG,Y}) V_D \quad \text{(Equation 6)}$$

Here, $I_D/g_m^{0.5} = 0.015 \text{ A}^{0.5}\text{V}^{0.5}$ corresponds to regions (i) and (ii) in **Figure 2a**, and $I_{D,top} \ll I_{D,bot}$ can be assumed, as a result, the second term ($I_{D,top}/g_{m,bot}^{0.5}$) of **Equation 5** is ignored.^[57]

The extracted R_{SD} has a nearly constant value between 140 and 150 Ωmm regardless of the applied V_{TG} , but the R_{CH} has a high value of 340 Ωmm at $V_{TG} = -30 \text{ V}$, and decreases rapidly in inverse proportion until $V_{TG} = -10 \text{ V}$. The R_{CH} maintains the value of $\approx 100 \Omega\text{mm}$ when $V_{TG} > 15 \text{ V}$. From the values obtained through **Figure 4b**, three simple assumptions are needed to extract the interlayer resistance (R_{int}) of the ReS_2 channel. Firstly, the current when $V_{TG} = -30$ and 30 V are applied flows through the bottom/top channel as shown in **Figure 4c** and **d**, respectively. Secondly, ReS_2 channel consists of 10 layers with $9 \times R_{int}$. Finally, the resistance of the channel where the carriers hardly flow should also be connected in parallel through using the continued fraction equation (see **Equation S1**), but it is negligible because the resistance of the depleted channel is very large. At $V_{TG} = -30 \text{ V}$, the first equation is obtained by the sum of the bottom ReS_2 and interlayer resistances, and at $V_{TG} = 30 \text{ V}$, the second equation is obtained by the parallel combination of the top and bottom ReS_2 and interlayer resistances. (see **Equation S2**). Therefore, R_{int} extracted through the above assumptions and the system of linear

equations with two unknown values (R_{int} , $R_{\text{CH,on}}$) is found to be 21.2 Ωmm , which is larger than those of other 2D materials (see **Equation S2**).^[26,58]

3. Conclusion

We presented an in-depth analysis for h-BN dual-gated ReS₂ FETs showing an optimized performance and understanding its electrical properties at various top gate biases. Optimization and interpretation were conducted in parallel with secondary g_m peak, threshold voltage, subthreshold swing, mobility through fundamental current-voltage analysis, time-dependent current, LF noise, and TCAD simulation analysis. Structurally, the bottom h-BN layer introduces almost no traps and provides an enough physical distance between the interface traps of SiO₂ and the carriers in the channel. Consequently, we demonstrated an excellent optimized performance of h-BN dual-gated ReS₂ having a high μ_{FE} of 46.1 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, a high current on/off ratio of $\sim 10^6$, a low subthreshold swing of 2.7 Vdec^{-1} , and a low $N_{\text{t,eff}}$ of $7.85 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ at a small operating voltage ($< 3 \text{ V}$) through understanding unique characteristics of h-BN dual-gated ReS₂ FET with various analysis. Additionally, we presented a simple method for extracting the approximate R_{int} using constant Y-function method. We anticipate this study to be applicable not only to ReS₂ but also to other 2D layered materials, resulting in implementing a compact modeling through analytical choice maps and extracting approximate their interlayer resistances. Further performance improvements of devices are expected when the top gate electrode covering the entire channel length is fabricated and considering the anisotropic properties of ReS₂ channel.

4. Experimental Methods

Few layered ReS₂ and h-BN flakes were mechanically exfoliated *via* the Scotch tape technique and then transferred onto a clean SiO₂/Si substrate. The SiO₂/Si substrate consists of a heavily p-doped Si wafer with thermally grown 90 nm thick SiO₂ layers. A h-BN flake used as top gate

dielectric was prepared by mechanical exfoliation and then transferred on top of stacked ReS₂ flake. The position of h-BN flake was accurately controlled by using home-made micro-manipulation system. (See **Figure S1**) Source, drain, and top gate electrodes were patterned by a conventional e-beam lithography after poly-methyl methacrylate (PMMA) e-beam resist was spin-coated. The 100 nm of Au was deposited by e-beam evaporation in order to form source, drain, and top gate electrodes. After lift-off process, the device was annealed at 200°C for ~2 h in vacuum condition.

Atomic force microscopy (AFM) was performed using Park System XE-100 to estimate the thickness of ReS₂ and h-BN flakes. Electrical properties measurements were performed at room temperature (300 K) through a Keithley 4200 parameter analyzer. Raman FT-IR spectrometer (LabRam ARAMIS IR, Horiba Jobin Yvon, $\lambda_{\text{exc}} = 532$ nm) was used to confirm the peak of ReS₂ and h-BN sheets. Time-dependent current and LF noise characteristics were measured by a home-made measurement system, consisting of a home-made battery box, a low noise current-to-voltage pre-amplifier (SR570, Stanford Research Systems), and a data acquisition system (DAQ-4431, National Instruments).^[4,46] We used some Python libraries for analyzing current fluctuation data (<https://docs.python.org/3/library/statistics>, <https://scikit-learn.org/stable/modules/density.html>) and power spectral densities (https://scipy-lectures.org/intro/scipy/auto_examples).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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References

- [1] M. M. Waldrop, *Nature* **2016**, *530*, 144
- [2] A. Allain, A. Kis, *ACS Nano* **2014**, *8*, 7180.
- [3] C. Ataca, H. Şahin, E. Aktuörk, S. Ciraci, *J. Phys. Chem. C* **2011**, *115*, 3934.
- [4] K. Lee, H. Lee, Y. Kim, J. Choi, J. Ahn, D. H. Shin, Y. Cho, H. Jang, S. W. Lee, J. Shin, H. Ji, G. T. Kim, *Nanotechnology* **2020**, *31*, 455202
- [5] S. Jo, N. Ubrig, H. Berger, A. B. Kuzmenko, A. F. Morpurgo, *Nano Lett.* **2014**, *14*, 2019.
- [6] D. Ovchinnikov, A. Allain, Y. S. Huang, D. Dumcenco, A. Kis, *ACS Nano* **2014**, *8*, 8174.
- [7] H. Lee, K. Lee, Y. Kim, H. Ji, J. Choi, M. Kim, J. P. Ahn, G. T. Kim, *Nanoscale* **2019**, *11*, 22118.
- [8] W. Zhang, M. H. Chiu, C. H. Chen, W. Chen, L. J. Li, A. T. S. Wee, *ACS Nano* **2014**, *8*, 8653.
- [9] Y. Moon, J. H. Shon, D. Kim, K. Lee, M. Joo, G. Kim, **2020**, *116*, 183102.
- [10] K. Lee, Y. Kim, D. Kim, J. Lee, H. Lee, M. Joo, Y. H. Cho, J. Shin, H. Ji, G. T. Kim, *ACS Appl. Mater. Interfaces* **2021**, *13*, 2829.

- [11] X. Li, C. Chen, Y. Yang, Z. Lei, H. Xu, *Adv. Sci.* **2020**, *7*, 2002320.
- [12] A. Castellanos-Gomez, E. Cappelluti, R. Roldán, N. Agraït, F. Guinea, G. Rubio-Bollinger, *Adv. Mater.* **2013**, *25*, 899.
- [13] C. H. Ho, Y. S. Huang, K. K. Tiong, *J. Alloys Compd.* **2001**, *317–318*, 222.
- [14] Q. Cui, J. He, M. Z. Bellus, M. Mirzokarimov, T. Hofmann, H. Y. Chiu, M. Antonik, D. He, Y. Wang, H. Zhao, *Small* **2015**, *11*, 5565.
- [15] S. Tongay, H. Sahin, C. Ko, A. Luce, W. Fan, K. Liu, J. Zhou, Y. S. Huang, C. H. Ho, J. Yan, D. F. Ogletree, S. Aloni, J. Ji, S. Li, J. Li, F. M. Peeters, J. Wu, *Nat. Commun.* **2014**, *5*, 1.
- [16] Y. Xiong, H. W. Chen, D. W. Zhang, P. Zhou, *Phys. Status Solidi - Rapid Res. Lett.* **2019**, *13*, 1800658.
- [17] K. C. Lee, S. H. Yang, Y. S. Sung, Y. M. Chang, C. Y. Lin, F. S. Yang, M. Li, K. Watanabe, T. Taniguchi, C. H. Ho, C. H. Lien, Y. F. Lin, *Adv. Funct. Mater.* **2019**, *29*, 1809011.
- [18] K. Thakar, B. Mukherjee, S. Grover, N. Kaushik, M. Deshmukh, S. Lodha, *ACS Appl. Mater. Interfaces* **2018**, *10*, 36512.
- [19] J. K. Huang, J. Pu, C. L. Hsu, M. H. Chiu, Z. Y. Juang, Y. H. Chang, W. H. Chang, Y. Iwasa, T. Takenobu, L. J. Li, *ACS Nano* **2014**, *8*, 923.
- [20] S. McDonnell, B. Brennan, A. Azcatl, N. Lu, H. Dong, C. Buie, J. Kim, C. L. Hinkle, M. J. Kim, R. M. Wallace, *ACS Nano* **2013**, *7*, 10354.
- [21] D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, M. C. Hersam, *ACS Nano* **2014**, *8*, 1102.
- [22] Q. A. Vu, S. Fan, S. H. Lee, M. Joo, W. J. Yu, Y. H. Lee, *2D Mater.* **2018**, *5*, 031001.
- [23] M.-L. Chen, X. Sun, H. Liu, H. Wang, Q. Zhu, S. Wang, H. Du, B. Dong, J. Zhang, Y. Sun, S. Qiu, T. Alava, S. Liu, D.-M. Sun, Z. Han, *Nat. Commun.* **2020**, *11*, 1205.
- [24] G. Ghibaudo, *Electron. Lett.* **1988**, *24*, 543.

- [25] H. Chang, W. Zhu, D. Akinwande, *Appl. Phys. Lett.* **2014**, *104*, 113504.
- [26] J. Na, M. Shin, M. K. Joo, J. Huh, Y. Jeong Kim, H. Jong Choi, J. Hyung Shim, G. T. Kim, *Appl. Phys. Lett.* **2014**, *104*, 233502.
- [27] S. Das, J. Appenzeller, *Phys. Status Solidi - Rapid Res. Lett.* **2013**, *7*, 268.
- [28] B. Kaczer, J. Franco, P. Weckx, P. J. Roussel, V. Putcha, E. Bury, M. Simicic, A. Chasin, D. Linten, B. Parvais, F. Catthoor, G. Rzepa, M. Walzl, T. Grasser, *Microelectron. Reliab.* **2018**, *81*, 186.
- [29] Y. Liu, J. Guo, E. Zhu, L. Liao, S. Lee, M. Ding, I. Shakir, V. Gambin, Y. Huang, X. Duan, *Nature* **2018**, *557*, 696.
- [30] T. Fujita, Y. Ito, Y. Tan, H. Yamaguchi, D. Hojo, A. Hirata, D. Voiry, M. Chhowalla, M. Chen, *Nanoscale* **2014**, *6*, 12458.
- [31] X. Ling, W. Fang, Y. Lee, P. T. Araujo, X. Zhang, J. F. Rodriguez-nieva, Y. Lin, J. Zhang, J. Kong, M. S. Dresselhaus, *Nano Lett.* **2014**, *14*, 3033.
- [32] R. Resta, *Phys. Rev. B* **1977**, *16*, 2717.
- [33] A. Laturia, M. L. Van De Put, *npj 2D Mater. Appl.* **2018**, *2*, 6.
- [34] J. Y. Park, H. Joe, H. S. Yoon, S. Yoo, T. Kim, K. Kang, B. Min, S. C. Jun, *ACS Appl. Mater. Interfaces* **2017**, *9*, 26325.
- [35] D. Ovchinnikov, F. Gargiulo, A. Allain, D. J. Pasquier, D. Dumcenco, C. H. Ho, O. V. Yazyev, A. Kis, *Nat. Commun.* **2016**, *7*, 12391.
- [36] N. A. Pike, A. Dewandre, B. Van Troeye, X. Gonze, M. J. Verstraete, *Phys. Rev. Mater.* **2018**, *2*, 063608.
- [37] A. A. Shubnic, R. G. Polozkov, I. A. Shelykh, I. V Iorsh, *Nanophotonics* **2020**, *9*, 4737.
- [38] F. Liu, S. Zheng, X. He, A. Chaturvedi, J. He, W. L. Chow, T. R. Mion, X. Wang, J. Zhou, Q. Fu, H. J. Fan, K. Tay, L. Song, R. He, C. Kloc, P. M. Ajayan, Z. Liu, *Adv. Funct. Mater.* **2016**, *26*, 1169.

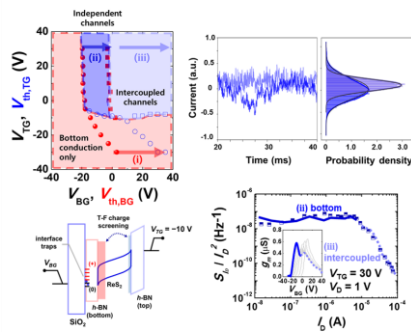
- [39] J. Xu, L. Chen, Y. Dai, Q. Cao, Q. Sun, S. Ding, *Sci. Adv.* **2017**, *3*, e1602246.
- [40] S. Y. Kim, D. Jeong, H. Lee, I. Na, S. Kim, D. Kim, S. Lim, B. C. Lee, S. Lee, S. M. Yang, G. Kim, M. Joo, *2D Mater.* **2020**, *7*, 031004.
- [41] K. Keyshar, Y. Gong, G. Ye, G. Brunetto, W. Zhou, D. P. Cole, K. Hackenberg, Y. He, L. Machado, M. Kabbani, A. H. C. Hart, B. Li, D. S. Galvao, A. George, R. Vajtai, C. S. Tiwary, P. M. Ajayan, *Adv. Mater.* **2015**, *27*, 4640.
- [42] D. K. Schroder, *Microelectron. Reliab.* **2007**, *47*, 841.
- [43] C. T. Rogers, R. A. Buhrman, *Phys. Rev. Lett.* **1985**, *55*, 859.
- [44] K. Lee, J. Yun, S. Lee, J. Song, Y. Kim, J. Kwak, G. T. Kim, *Nanoscale* **2020**, *12*, 15888.
- [45] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed., John Wiley & Sons, New York, Vol. 44 **2006**.
- [46] K. Lee, S. Nam, H. Ji, J. Choi, J. Jin, Y. Kim, J. Na, M. Ryu, Y. Cho, H. Lee, J. Lee, M. Joo, G. T. Kim, *npj 2D Mater. Appl.* **2021**, *5*, 4.
- [47] M. von Haartman, M. Ostling, *Low-Frequency Noise In Advanced Mos Devices*, Springer, Berlin **2007**.
- [48] K. Lee, Y. Kim, H. Lee, S. Park, Y. Lee, M. Joo, H. Ji, J. Lee, J. Chun, M. Sung, Y. H. Cho, D. Kim, J. Choi, J. W. Lee, D. Y. Jeon, S. J. Choi, G. T. Kim, *Nanotechnology* **2021**, *32*, 165202.
- [49] K. Lee, S. Nam, H. Kim, D. Y. Jeon, D. Shin, H. G. Lim, C. Kim, D. Kim, Y. Kim, S. H. Byeon, G. T. Kim, *Adv. Theory Simulations* **2020**, *3*, 2000012.
- [50] T. Grasser, *Noise in Nanoscale Semiconductor Devices*, Springer, Cham **2020**.
- [51] H. Wong, Y. C. Cheng, *IEEE Trans. Electron Devices* **1990**, *37*, 1743.
- [52] S. H. Song, M. K. Joo, M. Neumann, H. Kim, Y. H. Lee, *Nat. Commun.* **2017**, *8*, 1.
- [53] J. Na, Y. T. Lee, J. A. Lim, D. K. Hwang, G. T. Kim, W. K. Choi, Y. W. Song, *ACS Nano* **2014**, *8*, 11753.

- [54] W. Liao, W. Wei, Y. Tong, W. K. Chim, C. Zhu, *ACS Appl. Mater. Interfaces* **2018**, *10*, 7248.
- [55] N. Subramanian, G. Ghibaudo, M. Mouis, *2010 Proc. Eur. Solid State Device Res. Conf. ESSDERC 2010* **2010**, 309.
- [56] H. Y. Chang, W. Zhu, D. Akinwande, *Appl. Phys. Lett.* **2014**, *104*.
- [57] N. Rodriguez, S. Cristoloveanu, F. Gámiz, *J. Appl. Phys.* **2007**, *102*, 083712.
- [58] S. Das, J. Appenzeller, *Nano Lett.* **2013**, *13*, 3396.

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Modeling and Understanding the Compact Performance of h-BN Dual-gated ReS₂ Transistor

Implementing a compact modeling through analytical choice maps and extracting approximate their interlayer resistances in h-BN dual-gated ReS₂. Optimization and interpretation of performances in ReS₂ FETs were conducted in parallel with secondary g_m peaks, threshold voltages, subthreshold swing, mobility through DC analysis, time-dependent current, LF noise, and TCAD simulation analysis.



Supporting Information

Modeling and Understanding the Compact Performance of h-BN Dual-gated ReS₂ Transistor

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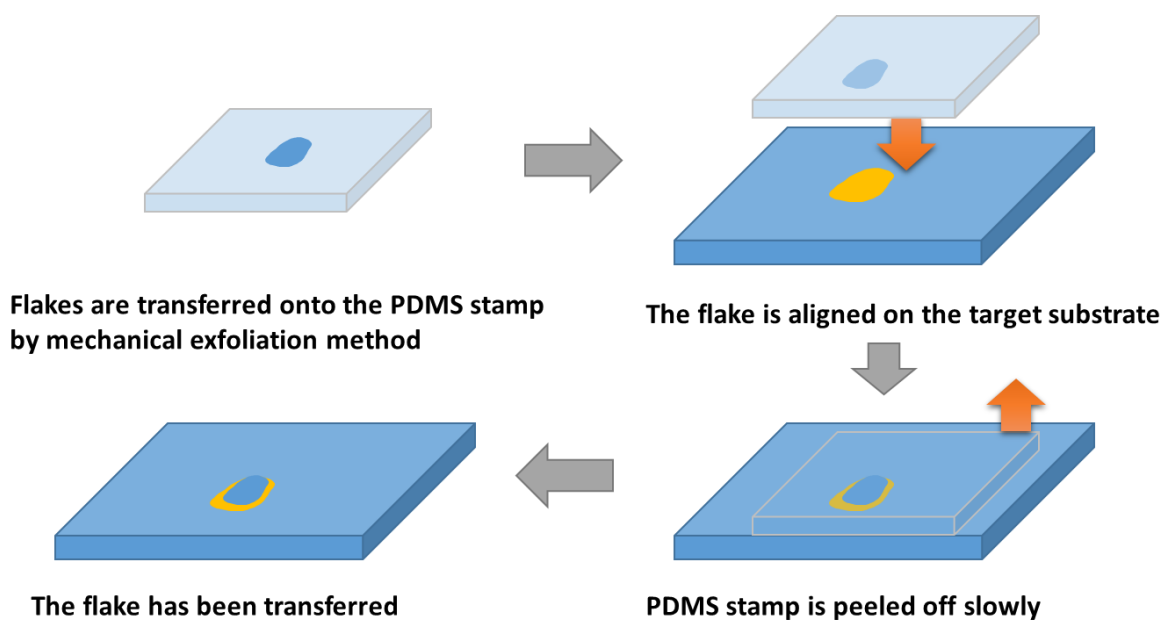


Figure S1. Dry transfer method schematic

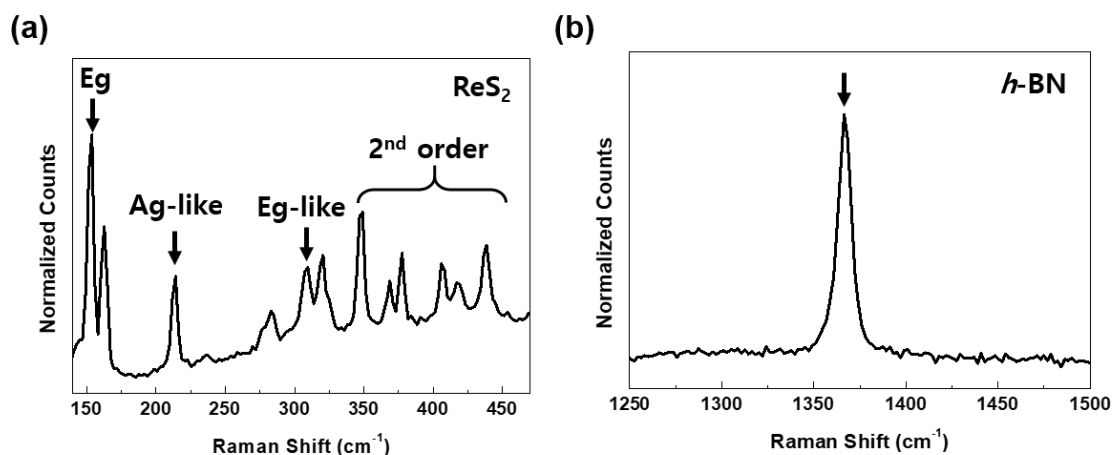


Figure S2. Representative Raman spectroscopy of (a) ReS₂ channel and (b) h-BN

Figure S2a and **b** show Raman spectra of ReS₂ and h-BN were measured with a laser wavelength of 532 nm, respectively. The typical Raman peaks at 160 cm⁻¹ (E_g) and 217 cm⁻¹ (A_g -like) were observed in the ReS₂ channel and a main peak of 1366 cm⁻¹ was observed in h-BN layers

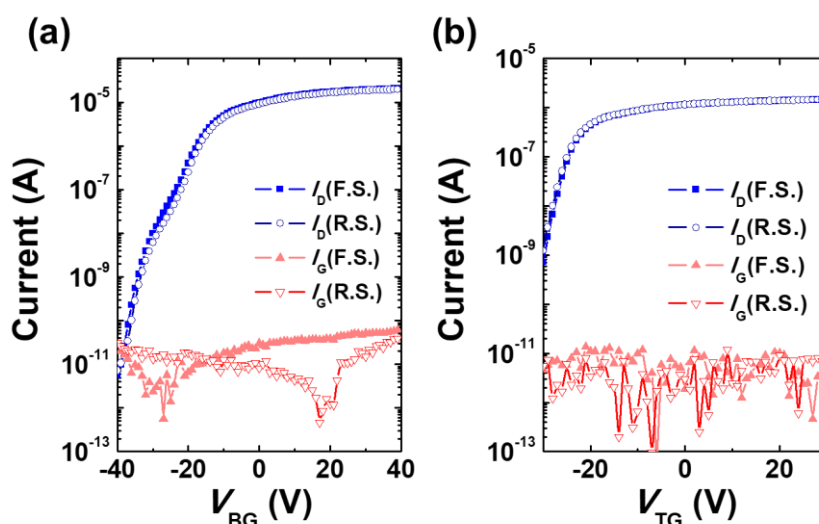


Figure S3. Transfer characteristics (I_D - $V_{BG(TG)}$) and gate currents (I_G - $V_{BG(TG)}$) of h-BN dual gated ReS₂ FET while (a) V_{BG} sweep at $V_{TG} = 30$ V and (b) V_{TG} sweep at $V_{BG} = 20$ V (F.S. and R.S. indicate forward and reverse sweeps, respectively).

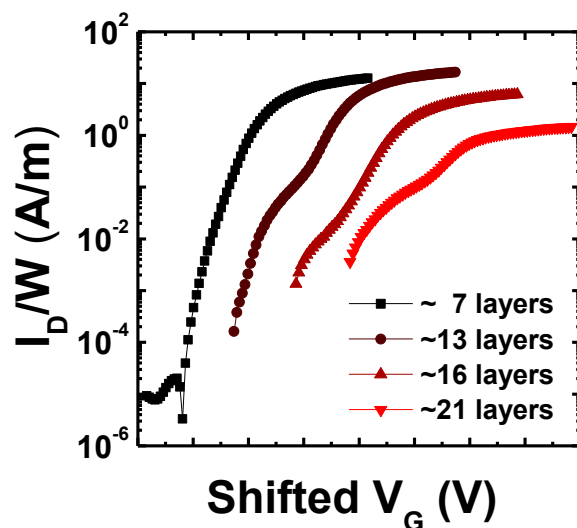


Figure S4. Transfer characteristics (I_D - V_G) of bottom gated ReS₂ FETs with different layers of ReS₂ channel

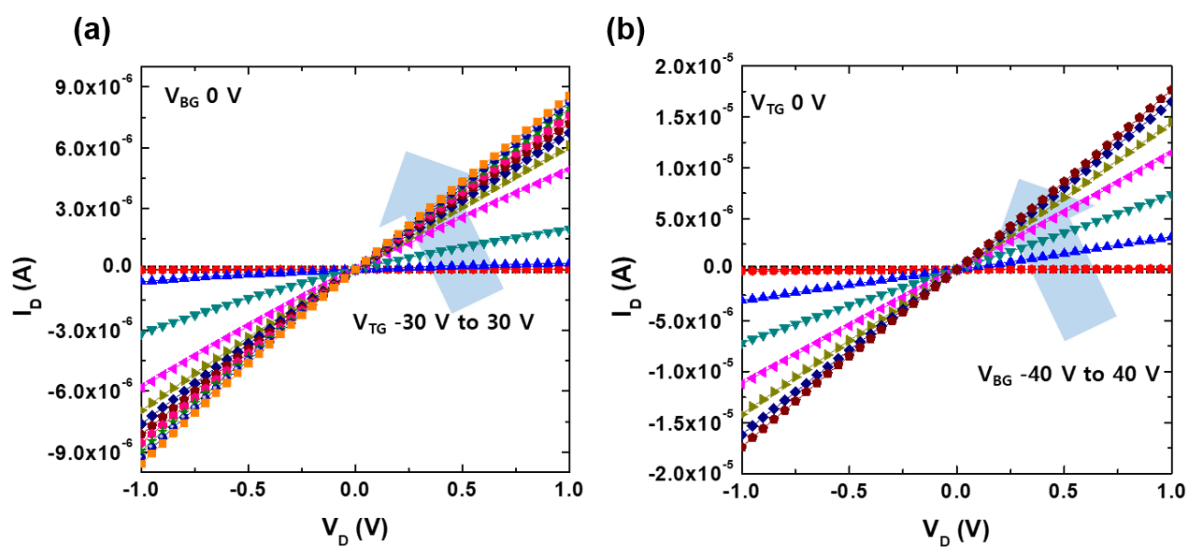


Figure S5. Output characteristics (I_D - V_D) of ReS₂ with different (a) V_{TG} and (b) V_{BG} .

Figure S5a and **b** show the I_D - V_D , with different V_{TG} and V_{BG} is applied at $V_{BG} = 0$ V and $V_{BG} = 0$ V, respectively, shows linear characteristics, obtaining Ohmic contacts.

Table S1. Comparison table with previous studies of ReS₂ FETs

Study	Method	Channel	Structure	Mobility [cm ² V ⁻¹ s ⁻¹]	Current on/off ratio
[17] K.-C. Lee et al.	Mechanical exfoliation	multilayer	graphene contact h-BN/ReS ₂ /h-BN	< 3.05	10 ⁵
[18] K. Thakar et al.	Mechanical exfoliation	multilayer	suspended ReS ₂	< 8	10
[34] J. Y. Park et al.	Mechanical exfoliation	multilayer	graphene contact	< 10.11	< 10 ⁵
[39] J. Xu et al.	Mechanical exfoliation	multilayer	Al ₂ O ₃ /ITO back gate	7.32	< 10 ⁶
[38] F. Liu et al.	Mechanical exfoliation	multilayer	SiO ₂ back gate	18	10 ⁵
[40] S. Y. Kim et al.	Mechanical exfoliation	multilayer	SiO ₂ back gate	< 15	< 10 ³
[41] K. Keyshar et al.	CVD grown	monolayer	SiO ₂ back gate	0.072	10 ³

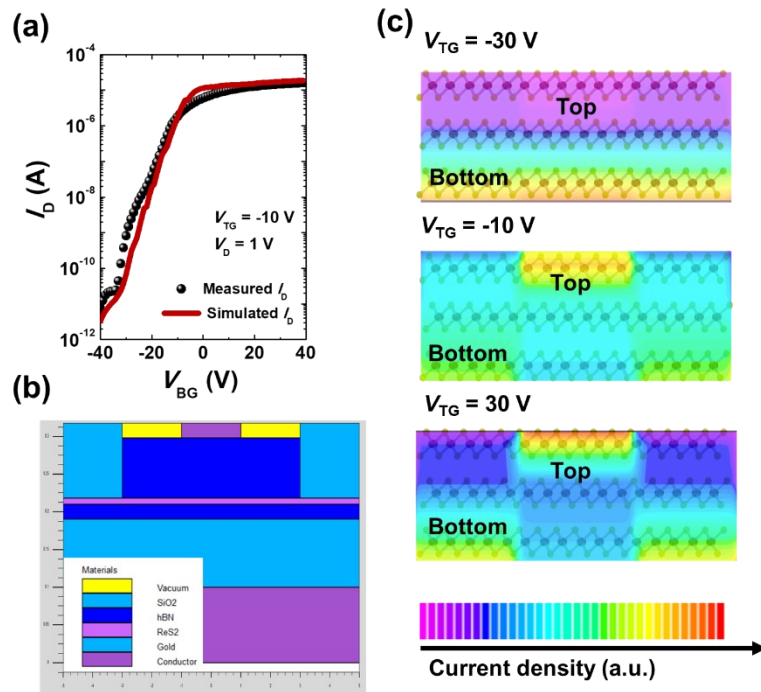


Figure S6. (a) Transfer characteristics (I_D - V_{BG}) at $V_{TG} = -10$ V and $V_D = 1$ V. (b) Designed structure in SILVACO TCAD. (c) Simulated current densities when the V_{TG} is applied as -30, -10, and 30 V, respectively.

Figure S6a shows transfer characteristics (I_D - V_{BG}) at $V_{TG} = -10$ V and $V_D = 1$ V, and simulated transfer curves are calculated from the structure of **Figure S6b** and the parameters in **Table S2**. **Figure S6b** is a device simulation structure designed to perform SILVACO TCAD simulations. As shown in **Figure S6c**, the separated conduction path according to the applied V_{TG} is described through SILVACO TCAD simulation using the material parameters of h-BN and ReS₂ as shown in **Table S2**. However, 10 layers are simulated as one semiconductor three-dimensional bulk and artificially n-doped according to **Table S2**. Without applying the weak interlayer coupling effect to the TCAD simulation, the approximate current density change is observed at constant $V_{BG} = -5$ V. At $V_{TG} = -30$ V, only the bottom conduction path is mainly observed, but at $V_{TG} = -10$ V, the top conduction path starts to be observed by a 2 μm of top gate electrode, and a separate conduction path is observed at $V_{TG} = 30$ V. Therefore, the obviously separated conduction path can be described as the result of **Figure 2a**, if applying strong interlayer resistance (R_{int}) due to weak interlayer coupling effect is applied to calculation of TCAD simulations.

Table S2. Parameters of h-BN and ReS₂ for TCAD simulation

Materials	h-BN	ReS ₂
Bandgap Energy (eV)	3.9	1.3
Electron affinity (eV)	1.11	4.30
Permittivity	4.2	15
Effective mass of electrons (m_e)	0.26	0.5
Effective mass of holes (m_h)	0.47	0.3

Interface trap density (cm ⁻² eV ⁻¹)	1 × 10 ¹¹
Trap depth (μm)	0.004

$$R_{CH} = \frac{1}{\frac{1}{R_{top,0}} + \frac{1}{R_{int} + \frac{1}{\frac{1}{R_{top,1}} + \frac{1}{R_{int} + \frac{1}{\frac{1}{R_{top,2}} + \dots + \frac{1}{R_{int} + \frac{1}{\frac{1}{R_{top,8}} + \frac{1}{R_{int} + R_{top,9}}}}}}}}$$

(Equation S1)

$$9R_{int} + R_{CH,on} = 340 \text{ } \Omega\text{mm}, \quad R_{CH,on} \parallel (9R_{int} + R_{CH,on}) = 100 \text{ } \Omega\text{mm} \text{ (Equation S2)}$$