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Design Trade-Offs of Modular Multilevel Converter-Based Arbitrary Wave Shape Generator for Conventional and Unconventional High Voltage Testing

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ABSTRACT This paper comprehensively investigates the design trade-offs of a Modular Multilevel Converter (MMC) operations as an Arbitrary Wave shapes Generator (AWG) to perform High Voltage (HV) dielectric testing of different grid assets. HV AWG applications pose unique operating conditions to the MMC, which influences the selection of the various system parameters. This influence of the MMC system parameters is studied analytically, with MATLAB-Simulink simulations and a down-scaled MMC prototype. It is found that the Phase-Shift Carrier (PSC) modulation technique proves to be a superior modulation technique over Nearest Level Control (NLC). The correct choice of arm inductance and series damping resistance improves the harmonic performance of the output voltage waveform. The fast switching SiC MOSFETs are well suited to generate complex waveforms with high bandwidth. The adapted control system with the proportional controller can accurately generate the different waveforms with Total Harmonic Distortion (THD) less than 5%. The circulating current in the MMC is negligible for the HV AWG application, which explains why the submodule capacitor voltages are balanced even when asymmetric complex wave shapes are generated from the MMC. Additionally, the submodule capacitor ripple expression is derived for this unique application, and it matches well with the simulation and experimental results. For this application, submodule capacitance in the μF range is sufficient to keep the ripple within 1% of its average value. Moreover, the challenges of realizing the full-scale MMC setup are discussed. The discussed design guidelines are applied to simulate the full-scale prototype with 67 submodules per arm.

INDEX TERMS MMC, AWG, conventional and unconventional dielectric testing, complex waveforms, modulation techniques, down-scaled prototype, capacitor voltage ripple.

I. INTRODUCTION

High Voltage (HV) equipment in the electrical power system such as switchgear, cables, and transformers are experiencing new electrical stresses due to the rise of Distribution Generation (DG) systems and large renewable energy integration by power electronic converters [1], [2]. For this reason, HV equipment must more often endure higher dV/dt stress due to solid-state switching and circulating high-frequency current harmonics, which can degrade the reliability of the grid by weakening the dielectric material of the grid asset. Conventional HV dielectric test sources i.e., transformers (cascaded and resonant), impulse generators, and rectifier circuits, face many limitations in terms of flexibility to generate different wave shapes, current rating, as well as time-consuming to build a customized test setup. Since these new electrical stresses are mainly generated by the switching mechanisms

of the Semiconductor (SM) devices, the same ingredient is chosen to develop a programmable HV test source for future and advanced dielectric tests of various grid assets.

SM devices can work either in the linear region with varied impedance or switching region, leading to two altogether different solution directions for Arbitrary Wave shape Generation (AWG). Based on the linear operation of SM devices, HV amplifiers are designed, and they are used with a function generator as an AWG. In the linear region of operation, SM devices exhibit relatively high losses [3], restricting the current flowing due to the heat generated in the HV amplifier. With an equivalent capacitive load, the bandwidth of the voltage waveform obtained from such an amplifier is limited [4] since the current flowing through the capacitive load is directly proportional to the frequency of the voltage waveform applied to it. Hence, this paper investigates other solution directions of switching converters, such as multilevel converters topologies for AWG.

In the literature, there are few attempts to use multilevel converters topologies for arbitrary wave shape generations in applications like dielectric barrier discharge plasma actuator [5], [6], HVDC valve testing [7], and HV testing [8]. Among most common multilevel topologies, i.e., Cascaded H bridge (CHB) and Modular Multilevel Converter (MMC), mostly, CHB topology or its variants with different DC source implementation are chosen to implement an AWG over MMC. Technically, MMC and CHB have similar working principles since MMC is evolved from the CHB [9]. A CHB converter has one converter arm where each H-bridge submodule has a dedicated DC source. An MMC can be seen as two series-connected CHBs, without the distributed DC sources, and interconnected by a single DC voltage source [10]. For the AWG application, the MMC can be implemented using half-bridge submodules, unlike the intrinsic H-bridge circuit of the CHB. The primary difference lies with the DC source requirement in both solutions. For generating positive and negative waveforms, the MMC needs two isolated DC voltage sources or a single source with at least two split capacitors, each rated for the maximum generated voltage. In comparison, the many distributed DC sources in the CHB are rated for submodule voltage level and have a floating potential requiring insulation for the maximum generated voltage. This isolation for the maximum generated voltage will be necessary because each DC source is typically fed by a DC-DC isolated converter connected to the same low voltage battery [5], or medium voltage grid [11]. Therefore, the design scalability of the CHB becomes more challenging [5]. For the application at hand, this design feature is crucial for customized tests at different voltage levels. Hence, the MMC is chosen as an advantageous solution for an AWG.

With various benefits of MMC, it is being adapted for different applications in power engineering. The most dominant use of MMC is for HVDC transmission [10]. Even before the MMC was invented, CHB was used as a STATCOM, and MMC is being adapted for STATCOM application to fully compensate the unbalanced and distorted nonlinear load [12]. With low harmonic output voltage, MMC can reduce filtering requirements for Medium Voltage (MV) drive applications [13], [14]. For the ever-growing wind industry, MMC can be used as storage for Fault Ride Through capability as discussed in [15]. Moreover, the use of MMC is being evaluated for electric vehicle, and battery storage applications [16], [17]. HV Testing application requires single-phase MMC to generate arbitrary voltage waveforms across the HV insulation present in various grid assets without transferring the active power. All applications, as mentioned earlier, are using MMC for active power transfer ranging up to MW, leading to currents up to kA. HV testing application draws much less current up to a level of few A. However, there is a possibility that the test object breaks down with a flashover, and the test source should supply enough energy for that. Additionally, the performance of MMC-based HV AWG is not evaluated for its power efficiency but based on the output voltage waveforms' voltage efficiency. Hence, the main contribution of this paper is as follows:

- A detailed understanding of the HV AWG requirement
- Comprehensive analysis of different design trade-offs present in the MMC-based AWG
- Proof of discussed trade-offs with the MATLAB-Simulink simulations and with the down-scaled prototype of a MMC
- Discussion on realizing the full-scale prototype of a MMC-based HV AWG and its controller

The literature mentioned above about AWG, particularly [8], does not discuss the design trade-offs or explain the design guidelines of realizing such a HV AWG. Hence, this paper offers a unique discussion about the design of the main operating parameters of a MMC, i.e., modulation technique, arm inductance, series resistance, number of submodules, SM devices, submodule capacitance, and control aspects. Before going into detail about the design, Section II goes into detail about the HV AWG application and identifies the differences between the HV AWG application and the existing application of MMC. Section III presents the selected MMC topology and governing dynamic equations. Next, Section IV dives deeper into different design trade-offs present in the MMC-based AWG. Section V describes the chosen parameters for the MATLAB-Simulink simulations and experimental setup and presents the performance of the MMC-based AWG. Section VI discusses different challenges and characteristics of full-scale HV AWG and its controller. Finally, Section VII concludes the work done and gives future research recommendations.

II. HV AWG APPLICATION

Before integrating the power grid equipment into the grid, they are tested to determine the mechanical, thermal, and dielectric properties for reliable operation. HV tests are used to determine the dielectric properties such as the dielectric strength, partial discharges, and dielectric losses of MV and HV insulation materials [18]. During these dielectric tests,

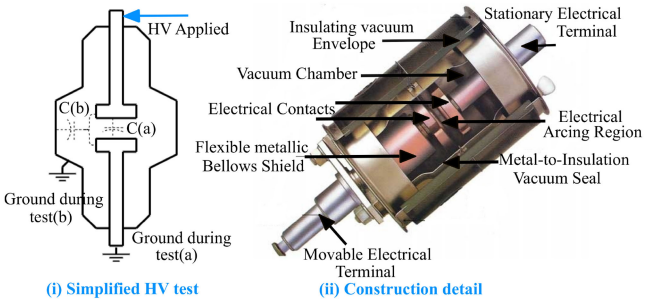


FIGURE 1. **MV Vacuum circuit breaker [34].**

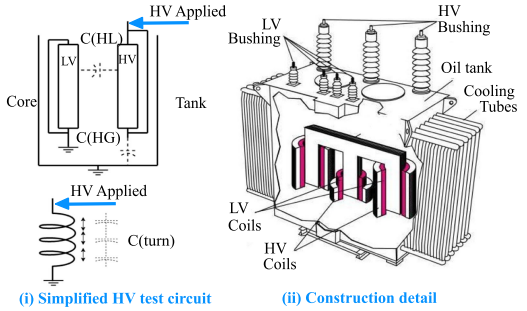


FIGURE 2. **MV Distribution Transformer [35].**

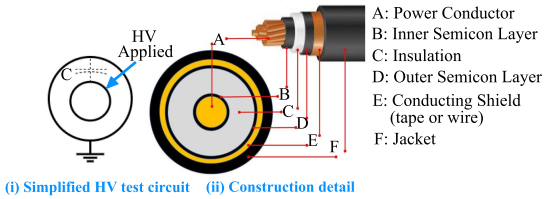


FIGURE 3. **MV AC Cable [36].**

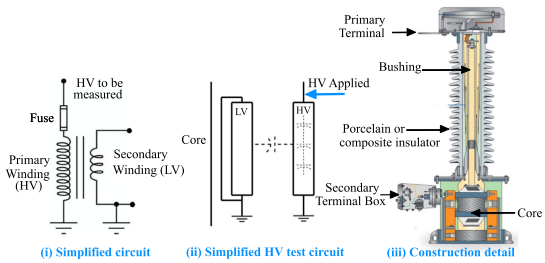


FIGURE 4. **MV Potential Transformer [37].**

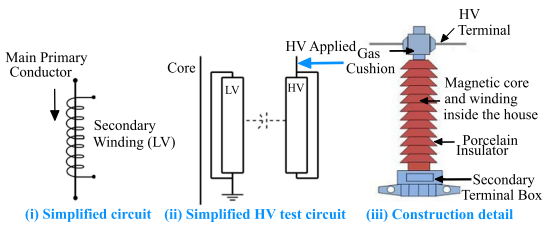


FIGURE 5. **MV Current Transformer [23].**

the equipment insulation behaves electrically as a capacitance [19].

Power grid equipment and their testing have a long history of more than one century [20]. These test procedures are standardized for a particular voltage class by different standards organizations such as IEC, IEEE, and called conventional HV tests for now on in this paper. In the following subsection, the conventional HV tests of MV equipment are summarized, where the rating of the equipment ranges between 1 kV and 36 kV [21]. Note that MV class grid equipment is prone to many critical operating conditions and thus must withstand voltages above its rated values that reach HV levels (36 kV to 150 kV [21]). Therefore, the certifications of MV equipment are naturally the first target application for a complex and challenging application of MMC-based HV AWG. Power grid HV equipment needs to be tested at extra-high voltage levels (much more than 150 kV) which demands a highly complex MMC-based HV AWG.

Additionally, unconventional HV tests may be employed in both MV and HV class equipment, particularly during the product development stage. Novel diagnostic methodologies where non-sinusoidal waveforms (or other customized voltage shapes) are used to determine different dielectric properties of the insulation materials. In the following sections, several points are discussed related to the application of MMC-based HV AWG. Additionally, the differences between HV testing and energy transmission applications of an MMC are investigated.

A. CONVENTIONAL HV TESTS

Fig. 1, Fig. 2, Fig. 3, Fig. 4, and Fig. 5, show pictures of circuit breaker, distribution transformer, AC cable, Potential Transformer (PT), and Current Transformer (CT) respectively. CT and PT are types of instrument transformer. In Fig. 1, to Fig. 5,, construction details of the equipment mentioned above are shown with their simplified diagrams of how HV tests are performed in relation to the applied HV potential and grounding parts. Note that therein the equivalent dielectric capacitances that will affect the tests are shown additionally. There is a significant difference between a distribution transformer and the instrument transformer (PT and CT both) in terms of its construction and operation [22]. Hence, the dielectric tests performed on the distribution transformer and PT are different in their test circuit, as shown in Figs. 2 and 4. Though the test connections are the same for distribution transformer and CT, there is only a single turn in the primary winding of a CT with a toroidal core [23] instead of standard E core in the distribution transformer [24]. The range of the mentioned dielectric capacitance is found and presented in Table 1. In the EU, these equipment are tested according to the IEC standards [25]–[28], mainly it includes sinusoidal and lightning impulse test waveforms [29]. Here, the sinusoidal is the power frequency waveform, and the lightning impulse is a steep impulse with 1.2 μs rise time and 50 μs tail time. The power frequency tests of MV class equipment are conducted at a higher voltage than the rated voltage of the equipment

TABLE 1 Typical Range of the Equivalent Capacitance of Dielectric Insulation Materials

Vacuum Circuit Breaker [31]	Distribution Transformer [31]	AC Cable [32]	Instrument Transformer [33]
C(a)=50 pF C(b)=50 pF	C(HG)=12-16 nF C(LG)=19-26 nF	C=1-10 nF	C(PT)=1 nF C(CT)=0.25 nF

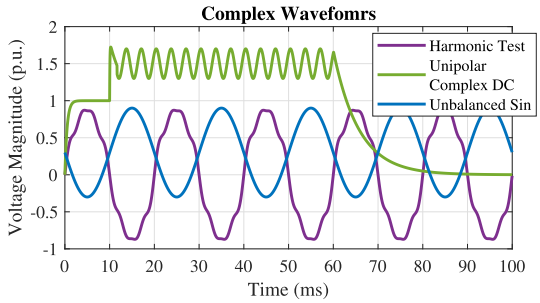


FIGURE 6. Complex waveforms demonstrated in this paper.

due to the different switching transients [18]. For example, a 3 kV equipment will be tested with 10 kV, and a 36 kV rated equipment is tested at 70 kV to 80 kV [27]. In some cases, the manufacturer or owner of the Device Under Test (DUT) can customize a test that demands a higher voltage than the standardized value to test the limits of their equipment. Similarly, the lightning impulse is tested at 6 to 7 times higher voltage than the rated voltage of the equipment depending on the voltage class of the equipment. For example, 36 kV transformer will be tested with 170 kV to 220 kV lightning impulse [27]. Apart from these standard dielectric tests, PTs need to be evaluated for their accuracy to measure higher-order voltage harmonics. Hence, the AWG should generate higher-order harmonics, e.g., up to 50^{th} harmonics [30]. An example of complex waveform generation of up to 7^{th} harmonics is shown in Fig. 6.

B. UNCONVENTIONAL HV TESTS

Unconventional HV tests include material tests where non-sinusoidal waveforms are used to correlate the dielectric property to the condition of the MV or HV insulation, e.g., location of the defect, type of defect, lifetime, etc., [38], [39]. Furthermore, these tests include future and advanced waveforms required to test MV/HV equipment with real electric stress generated due to a power electronics-rich power grid. One such complex waveform is the unipolar DC waveform generated specifically in the symmetric monopole HVDC transmission system [2], as shown in Fig. 6. The mentioned complex waveform consists of switching impulse and superposition of a 6^{th} harmonic component of the fundamental grid frequency of 50 Hz and a DC component value. With the conventional (mostly passive-based) HV test sources, three different voltage sources need to be coupled together to generate such a waveform that is cumbersome and difficult to realize. The specific waveform is generated when the cable experiences a pole to ground fault. In this case, the voltage on another cable can become two times higher than the rated values. This is usually restricted to 1.5 times the rated value by installing surge arresters. When the surge arrester reacts toward the fault, the control of the HVDC MMC protects the solid-state switches, e.g., IGBTs, by going into a blocked state, and the converter acts as a diode rectifier [40]. The AC side circuit breaker identifies this fault and disconnects the converter from the grid after a few 10 s of ms. Even the testing of these surge arresters needs a controllable waveform as discussed in [41]. The harmonic test waveform and the unipolar complex waveform depicted are chosen to demonstrate the design trade-offs for the MMC-based AWG discussed in this paper. In addition, an unbalanced sinusoidal waveform is added to the above list which is not completely bipolar or unipolar waveform, hence it is called as a mixed polar waveform. All three waveforms are depicted in Fig. 6.

C. DIFFERENCE BETWEEN HV AWG AND ENERGY TRANSMISSION APPLICATION

- *The magnitude of power transfer:* For the AWG, the mentioned capacitive load will require a relatively low output current requirement of up to a few A. This small current constitutes the reactive power transfer to the equivalent capacitive load for building up the voltage stresses. Hence the active power requirement is low and represents only the losses within the converter and test object, which significantly contradicts the HVDC transmission application, where active power flows is in the MW range [42].
- *Test object behaviour:* During an HV test, the breakdown of the test object or flashover is a likely phenomenon. Hence, the test source should supply sufficient energy for the breakdown and protect itself rapidly (in several μs or few ms). In power applications like renewable energy generation and battery energy systems, it could be necessary that the power electronics supply energy for a fault in a coordinated matter that can last a relatively long time (several ms) without disconnection, e.g. Low Voltage Ride Through [43].
- *Frequency of use:* Generally, a power electronic converter integrated into the grid is used for continuous operation. A test source is used only for a fixed amount of time during working hours. For dielectric tests, the typical test duration varies from 1 minute to 4 hours.
- *Performance parameter:* Power efficiency of the converter is of utmost importance in energy transmission, but voltage accuracy is highly important in HV testing. Since there is no intentional active power transfer, specifications will be voltage and current capability, slew rate, small- and large-signal bandwidth.

D. SUMMARY OF HV TEST REQUIREMENT ON MMC-BASED AWG

Apart from the discussed differences between the two applications of MMC in II-C, Fig. 7 summarizes the HV test requirements, which shows variable voltage and frequency

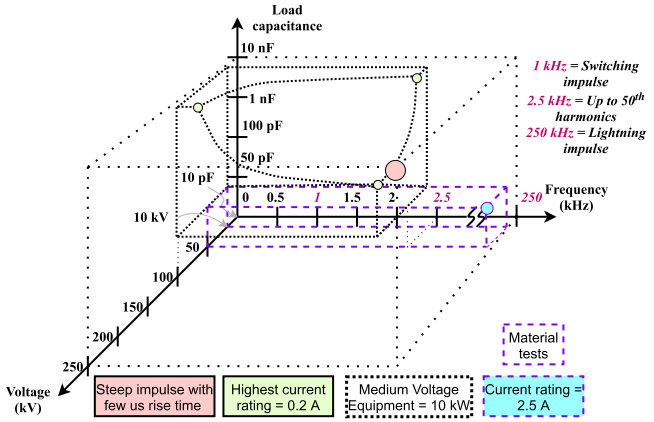


FIGURE 7. **Summary of HV test requirements for the MMC-based AWG.**

operation along with a typical value of equivalent load capacitance. Generally, the MMC is designed for fixed output voltage and frequency. In this figure, three boxes are visible, showing different HV test requirements. The outer box with a lighter dotted line is for the lightning impulse with 1.2 μs rise time across 10 nF load capacitance with the peak of 250 kV. These requirements are too extreme for an MMC with respect to the fact that there will be too many submodules that must switch with only small jittering (maximum of few 100 ns) to satisfy the operation time within 1 μs and SM devices in the submodule need to be able to carry pulse currents in the range of kA to charge the load capacitance with 250 kV in few μss. On the contrary to this, much less current such as 0.2 A, is sufficient for other test requirements, as shown in the dark-dotted box. The dark-dotted box has its one corner missing to keep the power rating of the DC source to be within 10 kW. Because of these challenges, lightning impulse requirements will cause a prohibitively high cost of the MMC-based AWG, and it will not be considered further in this research work. The third box with purple color dotted line is for material tests that require comparatively less voltage (10 kV to 50 kV) and low load capacitance (10 pF to 50 pF). For the reminder of this paper the key specifications considered for the design of the MMC AWG will be: 10 kV to 100 kV output voltage range; DC to 2.5 kHz bandwidth; 50 pF to 10 nF load capacitance range; and 10 kW power rating.

III. CONVERTER TOPOLOGY AND SCHEMATIC

Fig. 8(a) shows the schematic of the MMC-based HV test source, which has been adapted from the original MMC topology for power transmission application [44], [45]. It has a single phase of an MMC, a split DC source, the AC filter comprising the upper and lower arm inductance (L_a), and a capacitive load (C_{load}) representing the equivalent electrical model of the HV equipment. In the schematic, there is a series resistance (R_a) along with the arm inductance. This resistance helps to damp the oscillations generated due to the resonance between the arm inductance and the load capacitance. As discussed earlier in Section II-C, the converter's power efficiency

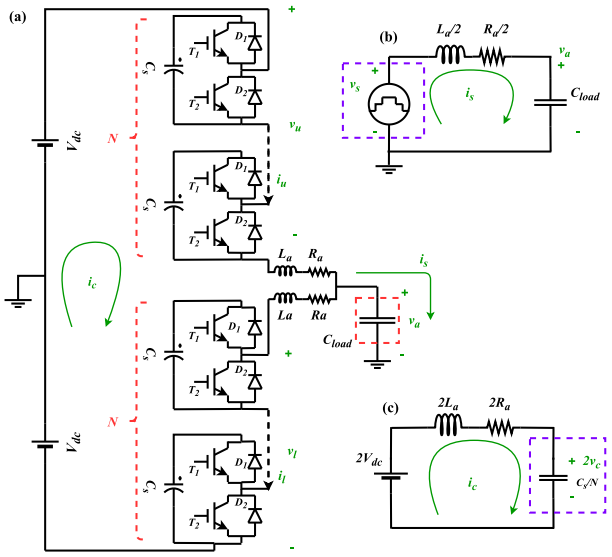


FIGURE 8. **(a) MMC Schematic for HV AWG application. (b) Output current circuit. (c) Circulating current circuit.**

is not an important performance parameter. Hence, the passive damping methodology is chosen to control the MMC-based AWG. However, the losses in the arm resistors are closely monitored during the design process to ensure its practicability. Please note that this methodology of using resistive-based damping is a common practice in conducting HV tests [29].

By applying Kirchhoff's Voltage Law (KVL) in the upper and lower arm, dynamic equations of the MMC can be obtained, as shown in (1) and (2). Note that (3) can be obtained by subtracting (2) from (1), whereas (4) is derived by adding (1) and (2). (3) and (4) are coupled equations with four variables v_u, v_l, i_u, and i_l, where $v_{u,l}$ is the sum of all submodule capacitor voltages in the upper and lower arm respectively, $i_{u,l}$ is the current flowing through the upper and lower arm respectively. By using the linear transformation shown in (5) and (6), (3) and (4) can be simplified [10]. In (5) and (6), i_s represents the output current, v_s can be understood as the inner electromotive force (emf) generated due to the switching of the submodule capacitors, i_c represents the circulating current, which is driven by the circulating voltage (v_c). After substituting (5) and (6) into (3) and (4), partially decoupled differential equations can be obtained, as shown in (7) and (8):

$$V_{dc} - v_u - R_a i_u - L_a \frac{\mathrm{d}i_u}{\mathrm{d}t} - v_a = 0 \tag{1}$$

$$V_{dc} - v_l - R_a i_l - L_a \frac{\mathrm{d}i_l}{\mathrm{d}t} + v_a = 0 \tag{2}$$

$$v_l - v_u + R_a(i_l - i_u) + L_a\left(\frac{\mathrm{d}i_l}{\mathrm{d}t} - \frac{\mathrm{d}i_u}{\mathrm{d}t}\right) - 2v_a = 0 \tag{3}$$

$$2V_{dc} - v_l - v_u - R_a(i_l + i_u) - L_a\left(\frac{\mathrm{d}i_l}{\mathrm{d}t} + \frac{\mathrm{d}i_u}{\mathrm{d}t}\right) = 0 \tag{4}$$

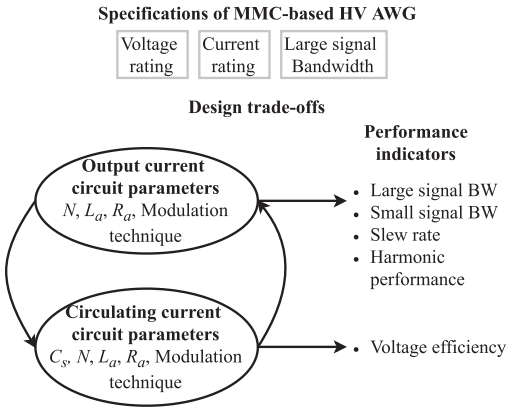


FIGURE 9. Specifications and Design trade-offs of MMC-based AWG.

$$i_s = i_u - i_l \quad v_s = \frac{(v_l - v_u)}{2} \tag{5}$$

$$i_c = \frac{(i_u + i_l)}{2} \quad v_c = v_u + v_l \tag{6}$$

$$v_s - \frac{R_a}{2} i_s - \frac{L_a}{2} \frac{\mathrm{d}i_s}{\mathrm{d}t} - v_a = 0 \tag{7}$$

$$V_{dc} - v_c - R_a i_c - L_a \frac{\mathrm{d}i_c}{\mathrm{d}t} = 0 \tag{8}$$

Equation (7) is a differential equation in terms of output current and inner emf. It can be represented with the RLC circuit, as shown in Fig. 8(b). Similarly, (8) is a differential equation in terms of circulating current and circulating voltage. If (8) is multiplied by two and the circulating voltage is represented by the voltage across the inserted submodule capacitance ($C_{eqv} = C_s/N$), it is possible to represent (8) with the RLC circuit, as shown in Fig. 8(c). In the output current of the circuit, the passive network (L_a, R_a, C_{load}) acts as a filter to v_s and attenuates the harmonics across the load capacitance. The observation above is important with respect to defining design constraints on the arm inductance and series resistance. The output current flowing through the arm inductance and resistances is responsible for building the desired voltage stress across the load capacitance. The upper and lower arm current charge or discharge the inserted submodule capacitors over their average value. The change in the submodule capacitor voltage will change the inner emf (v_s) and, in turn, the output voltage. This is how the output current circuit and the circulating current circuit are coupled with the submodule capacitor voltage feedback, and this partial coupling is shown with purple boxes in Fig 8. Nevertheless, it is important to simplify the complex MMC structure into these simple circuits to understand the design trade-offs and to provide an optimal design of the test source, which is covered in the next section.

IV. DESIGN TRADE-OFFS

Based on two simplified circuits, design trade-offs of the MMC-based AWG are summarized in Fig. 9, along with the specifications and the performance indicators. As discussed in the previous section, the output current circuit dictates the harmonic performance of the output voltage waveforms. Hence, the small- and large-signal bandwidth and slew rate will be determined by the component of the output current circuit, i.e., the number of submodules (N), L_a, R_a, and the modulation techniques. Moreover, the submodule capacitor voltages are balanced by the circulating current circuit, which is essential for the voltage magnitude accuracy. This paper will analyze different design trade-offs present with the choice of modulation technique, L_a, R_a, N, switches, submodule capacitance, control system, control hardware, and overall control architecture.

A. MODULATION TECHNIQUES

There are a wide variety of modulation techniques available for the MMC in literature. They can be broadly classified based on the switching frequency generated in v_s as high-frequency or low-frequency modulation techniques. High-frequency modulation techniques generate Pulse Width Modulation (PWM) waveform, with the switching frequency typically in kHz range. In contrast, low-frequency modulation techniques generate a staircase signal with a switching frequency comparable to the fundamental frequency.

High-frequency modulation techniques can be further divided into carrier-based and space vector modulation techniques. As the name suggests, carrier-based modulation compares carrier waveforms with the reference waveform to control the switches. For each submodule, carrier waveforms can be either phase-shifted in time or level-shifted in amplitude. The phase-shifted carrier makes Phase Shift Carrier (PSC) modulation [46], and it naturally utilizes all submodules evenly. The Level Shifted Carrier (LSC) modulation can be divided into three different types such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) [47]. LSC modulation has one remarkable disadvantage that it uses the submodule unevenly. To reduce the computational efforts for the controller, [48] discusses the implementation of PD LSC PWM using single carrier waveform. The effect of variable modulation index can be solved by adapting dynamic carrier overlapping modulation techniques as implemented in [49]. In space vector modulation (SVM), gate pulses for switches are calculated by representing the desired output voltage vector in a multiple layered hexagon structure, as discussed in [45], [50]. The computation efforts in SVM modulation are simplified in [51] to make it suitable for MMC. There are multiple publications available discussing novel updates to the above-mentioned techniques [52], [53]. Among the various high-frequency modulation techniques, PSC is chosen to evaluate for application of AWG due to its characteristics of even use of submodules. This special characteristic can naturally balance the submodule capacitor voltage facilitating on improving the active control for the HV AWG application [54]. For other techniques, an external controller or sorting algorithms

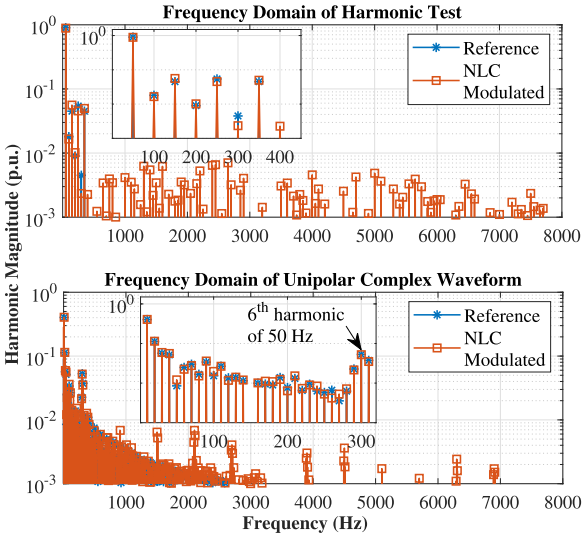


FIGURE 10. Frequency spectrum of NLC modulated waveforms which were shown in Fig. 6.

are required to balance the submodule capacitor voltages [55], [56].

Low-frequency modulation techniques includes Selective Harmonic Elimination (SHE) and Nearest Level Control (NLC). In SHE, the gate pulses are pre-programmed to obtain the desired harmonic performance without comparing the carrier waveforms to the reference waveform [57]. NLC calculates the gate pulse by rounding off the reference waveform to the desired number of submodules [58]. This gives an easy and simple solution for gate pulse calculations in the HV MMC applications where large number of submodules are implemented. Hence, this is chosen in this paper among the low-frequency modulation techniques to verify the features of this technique for the HV AWG application. It is important to note that NLC, similarly to LSC, requires either a controller or sorting algorithm to balance the capacitor voltage.

1) NEAREST LEVEL CONTROL (NLC)

NLC calculates the number of submodules to be inserted using either equation (9) or (10) and assign gate pulses accordingly. (9) results in $(N + 1)$ number of output voltage levels [58], whereas equation (10) generates $(2N + 1)$ number of output voltage levels [59].

$$n_{u,l} = round_{0.5}\left(\frac{N(V_{dc} \mp V_{ref})}{2V_{dc}}\right) \tag{9}$$

$$n_{u,l} = round_{0.25}\left(\frac{N(V_{dc} \mp V_{ref})}{2V_{dc}}\right) \tag{10}$$

Fig. 10 show the frequency domain analysis of the complex waveforms depicted in Fig. 6. Since the unbalanced sinusoidal waveform does not have a complex frequency spectrum, its frequency domain analysis is not elaborated here. They are generated with $N = 12$, and $(2N + 1)$ NLC modulation technique. In Fig. 10, it can be observed that the frequency domain waveform of reference and that of NLC modulated does not match for both harmonic test and unipolar waveforms. The mismatch is more prominently visible in the zoomed picture of the harmonic test waveform. Please note that the y axis scale used in Fig. 10 is logarithmic, and the small visible difference in this scale will already give an error in the range of 10%. For the harmonic test, the error for up to the third harmonics needs to be limited to 1%. Additionally, the harmonic test waveform contains harmonics up to the 7^{th} order, and the variable frequency operation nature of NLC inserts relatively high magnitude of harmonics close to the reference value, e.g., the 8^{th} harmonic, which makes the filtering requirement significantly high. For the unipolar complex waveform, the NLC modulated waveform has higher switching harmonics present in the large baseband harmonics of the reference waveform. This makes it extremely difficult to remove the switching harmonics introduced by the NLC operation. Harmonics introduced by NLC will reduce in magnitude as the number of submodules is increased. Unfortunately, they are not considerably shifted too far on the right side of the highest order of the reference harmonic, and hence they still can interfere with the baseband harmonics. The switching harmonics present due to NLC is difficult to remove for waveforms with a complex frequency spectrum, and one example is shown in [60]. The Total Harmonic Distortion (THD) of these NLC modulated waveforms are within 5%, but it might affect the type of electric stress applied to the insulation under stress [61].

2) PHASE SHIFT CARRIER (PSC)

In PSC, a traditional sine-triangle double edge modulation technique is used where each submodule is assigned with a different carrier signal. They are phase-shifted between them by $2\pi/N$. These phase-shifted carrier signals move the carrier harmonics to the N^{th} carrier frequency. The upper arm and lower arm can use the same carrier signals, or they can be phase-shifted by π/N. With π/N phase difference in the case of N is even, and 0 phase difference in the case of N is odd, generates $(2N + 1)$ number of levels in the output voltage of the converter [46]. This further improves the harmonic spectrum of the output voltage, moving the first carrier frequency to $2N^{th}$ of the fundamental carrier frequency. This specific phase difference between the upper and the lower arms ensures that the upper and lower arm submodules switch at different time instant, generating a higher number of levels and cancelling out more harmonics.

Fig. 11 shows the frequency domain analysis of the complex waveforms depicted in Fig. 6. Since the unbalanced sinusoidal waveform does not have a complex frequency spectrum, its frequency domain analysis is not elaborated here. They are generated with $N = 12$, PWM carrier frequency of 252 Hz, and $(2N + 1)$ PSC modulation technique. In Fig. 11, it can be observed that the frequency domain waveform of the reference and that of the PSC modulated match significantly for both harmonic test and unipolar complex waveform. This means that the switching harmonics

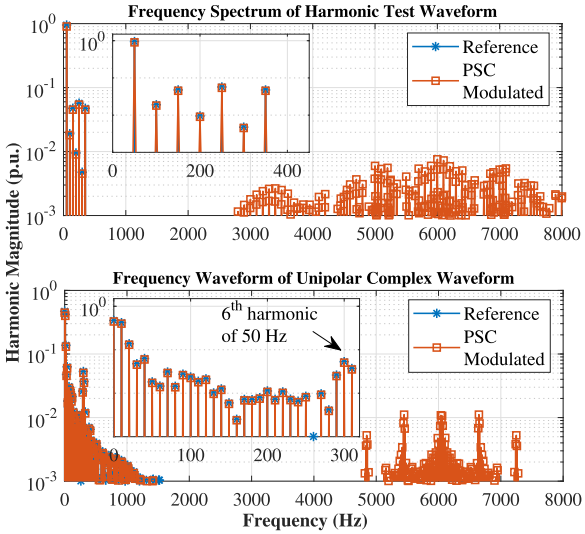


FIGURE 11. Frequency spectrum of PSC modulated waveforms which were shown in Fig. 6.

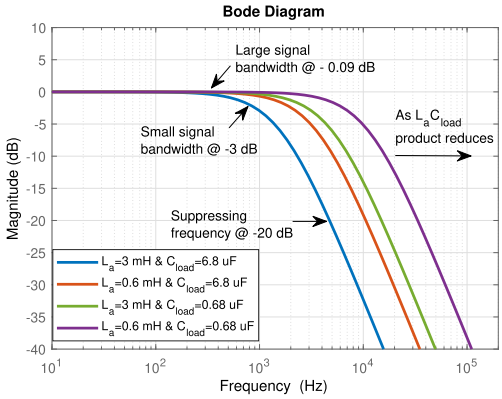


FIGURE 12. Effect of L_a and C_{load} variation on the filter profile.

produced due to PSC do not interfere with the baseband harmonics of the complex waveforms. The separation of switching harmonics from baseband harmonics is crucial for AWG application to generate accurate output wave shapes. Hence, this modulation technique is more beneficial than NLC, and it is chosen for the HV AWG studied in this paper.

B. ARM INDUCTANCE AND SERIES RESISTANCE

Since the equivalent passive network load acts as a series RCL filter, it is possible to choose the correct values of L_a and R_a to attenuate the unwanted high-frequency harmonics from the output voltage waveform. This is important for the HV AWG application because the waveform determines the electric stress applied to the DUT, and these voltage harmonics may cause unwanted additional dielectric stress in the test subject [1], [61]. More sophisticated AC filter topologies commonly used in renewable energy generation such as the third-order LCL filter [62], [63] add too many fully-rated components, particularly the full-rated voltage filtering capacitors, leading to increased the system's complexity and cost. Hence, the transfer function of the selected equivalent second-order RLC low-pass AC filter as necessary for the system design is shown in (11). The condition to remove the unwanted voltage harmonics is shown in (13), and the suppressing frequency ($f_{suppres}$) depends on the implemented modulation technique. For example, in Fig. 11, the undesirable voltage harmonics starts in the frequency of about 3 kHz to 4 kHz, and this frequency can be used as $f_{suppres}$. Additionally, L_a and R_a influence the small-signal bandwidth ($f_{3\,dB}$), large-signal bandwidth ($f_{1\%err}$), and slew rate for the given load capacitance C_{load}. In an open loop operation of the MMC-based AWG, both small- and large-signal bandwidths can be quantified, as shown in (12) and (15) from (11). Additionally, (14) defines damping requirement [64] for the second-order systems, which is important for the stable operation of the MMC with capacitive load. The damping requirement is derived based on the critical damping condition on the second-order control system. From the four established requirements in (12)-(15), large-signal bandwidth (12) and suppressing frequency (13) can be used to choose L_a and R_a. If the chosen resistance satisfies (14), then the choice of L_a and R_a can be used. If these equations are analyzed, it can be understood that the magnitude of the arm inductance and load capacitance should be lower to obtain larger signal bandwidths and a higher slew rate. The value of the series resistor changes as the value of arm inductance and load capacitance change as per (14). With lower values of arm inductance and load capacitance, the suppressing frequency is increased. High suppressing frequency requires higher equivalent switching frequency and higher accuracy on the controller. These trade-offs on the filter design and definition of the above-mentioned terminologies are summarized in Fig. 12, where the series damping resistance for all 4 combinations of L_a and C_{load} is chosen as per (14).

$$\frac{V_a[s]}{V_s[s]} = \frac{1}{s^2\frac{L_a}{2}C_{load} + s\frac{R_a}{2}C_{load} + 1} \tag{11}$$

$$abs\left(\frac{V_a[s]}{V_s[s]}\right)_{@f=f_{1\%err}} = 0.99 \tag{12}$$

$$abs\left(\frac{V_a[s]}{V_s[s]}\right)_{@f=f_{suppres}} = 0.1 \tag{13}$$

$$R_a \geq \sqrt{\left(\frac{8L_a}{C_{load}}\right)} \tag{14}$$

$$abs\left(\frac{V_a[s]}{V_s[s]}\right)_{@f=f_{3\,dB}} = 0.708 \tag{15}$$

C. NUMBER OF SUBMODULES AND SWITCHES

The influence of the number of submodules on the modulation technique and filtering requirement is discussed in the Section IV-A. However, the number of submodules is designed based on the DC link voltage and blocking capability of the commercially available switches. Table 2 shows the

TABLE 2 Number of Submodule and Voltage Rating Per Submodule

Number of submodules	Voltage rating per submodule (kV)
12	16.7
33	6
50	4
67	3
100	2
200	1

required blocking voltage capability for the given number of submodules for the 200 kV DC link. The DC link voltage is chosen so that 100 kV output voltage is produced. For the MMC with the half-bridge submodule implementation and the mid-point connection, as shown in Fig. 8, the DC link voltage must be twice the output voltage rating. In the Table 2, it is visible that the blocking voltage capability needs to be higher. This requirement resembles that of the HVDC energy transmission application [65]. However, the power modules designed for the HVDC application are rated for a very high current (kA range). Since the maximum current rating requirement for this new application is 0.2 A, discrete switches are preferred. Apart from the high blocking capability, the switches should have high switching frequency capability to get higher large-signal bandwidth. For 2.5 kHz large-signal bandwidth, the switching frequency should be much higher than 2.5 kHz. Available discrete MV IGBTs (2.5 kV, 3.3 kV, 4 kV, 4.5 kV) can operate efficiently less than 5 kHz switching frequency [66]. With the given constraints of voltage rating, switching frequency, and current requirement, the choice of Silicon Carbide (SiC) MOSFETs is advantageous. These devices are readily commercially available in TO-package for up to 3.3 kV rating, e.g., G2R120MT33 J from GeneSiC Semiconductor. Though MV SiC MOSFETs (10 kV, 15 kV) are pre-released by CREE-WOLFSPEED [67], they are not yet ready commercially.

D. SUBMODULE CAPACITANCE AND ITS VOLTAGE BALANCING

Next to the switches, the choice of submodule capacitance is crucial in determining voltage efficiency, size, and cost of the MMC-based AWG. Since the converter is not designed for active power transfer, the traditional condition of the total energy stored in all submodule capacitance per MVA rating of the converter [68] might not be valid. Another important usage of submodule capacitance is to keep its voltage ripple within a limit such as 10% of the average submodule capacitor voltage [69], [70]. Many researchers have worked on deriving the submodule capacitor voltage for MMC with HVDC power transmission application [10], [54], [71]. However, the same ripple expression can not be directly used for HV AWG application since hardly any active power is being transferred to the the equivalent capacitive load. Hence, the voltage ripple expressions are derived in the following section for the equivalent capacitive load and non-sinusoidal wave shape.

The partially coupled and complex dynamic model of MMC is simplified by averaging principle [10]. With this principle, it is possible to simplify the product of two continuous varying variables ($n^i_{u,l}$ and $v^i_{u,l}$) using (16) into (17). In these equations, $n^i_{u,l}$ is the modulation index of i^{th} submodule from the upper and lower arm. The averaging principle is used to calculate continuous modulation indices for the upper and lower arm, which is defined as $n_{u,l}$. Additionally, $v^i_{u,l}$ is the individual submodule capacitor voltage of i^{th} submodule from the upper and lower arm. $v^{avg}_{u,l}$ is the average total submodule capacitor voltage in the upper and lower arm. The same principle can be used to derive the capacitor voltage dynamic equations, as shown in (18). (19) is derived for the upper and lower arm capacitor voltage ripple by substituting the upper and lower arm current expressions from (5) and (6) in (18). Generally, in the HVDC transmission application, the average circulating current magnitude I_c is determined by the input and output power balance equation. If it is applied for HV testing application with capacitive load $2V_{DC}I_c = V_aI_s\cos(\phi)$, the average circulating current is found to be zero since $\cos(\phi)$ is zero. Please note that the losses occurring in the arm resistors are neglected in this mathematical derivation considering its small magnitude.

$$n_{u,l} = \frac{1}{N}\sum_{h=1}^{N} n^i_{u,l} \qquad v^i_{u,l} = \frac{v^{avg}_{u,l}}{N} \tag{16}$$

$$v_{u,l} = \sum_{h=1}^{N} n^i_{u,l} v^i_{u,l} = n_{u,l} v^{avg}_{u,l} \tag{17}$$

$$C_s \frac{\mathrm{d}v^i_{u,l}}{\mathrm{d}t} = n^i_{u,l} i^i_{u,l} \qquad \frac{C_s}{N}\frac{\mathrm{d}v_{u,l}}{\mathrm{d}t} = n_{u,l} i_{u,l} \tag{18}$$

$$\frac{C_s}{N}\frac{\mathrm{d}v_{u,l}}{\mathrm{d}t} = n_{u,l}\left(\pm\frac{i_s}{2} + i_c\right) \tag{19}$$

Zero average circulating current can be interpreted as this current is present only to charge or discharge the inserted submodule capacitor voltage without having a large DC component, unlike the traditional application of MMC. As per the circulating current circuit in Fig. 8(c), this circulating current balances the voltage between the DC link and inserted submodules. Hence, it is possible to neglect the circulating current from the ripple expression in (19). Assuming the output voltage is an arbitrary voltage waveform, it is represented as Fourier series, as shown in (21) and (22), where the modulation index is represented as m_a. Additionally, the output current and insertion indices are derived from (21) and (22) in (23) and (24), respectively. When equation (23) and (24) are substituted in (20), the time derivative of capacitor voltage is derived and simplified in (25). For a sinusoidal waveform, it is possible to derive the analytical equation of the total capacitor voltage, as shown in (26). For non-sinusoidal waveforms, MATLAB or Maple software can solve the integration

numerically.

$$\frac{C_s}{N}\frac{\mathrm{d}v_{u,l}}{\mathrm{d}t} = n_{u,l}(\pm\frac{i_s}{2}) \tag{20}$$

$$f(t) = \frac{a_0}{2} + \sum_{h=1}^{\infty}(a_h cos(hwt) + b_h sin(hwt)) \tag{21}$$

$$v_a = m_a V_{dc} f(t) \tag{22}$$

$$i_s = m_a V_{dc} w C_{load} \times \sum_{h=1}^{\infty}(-a_h h sin(hwt) + b_h h cos(hwt)) \tag{23}$$

$$n_{u,l} = \pm\frac{m_a f(t)}{2} + \frac{1}{2} \tag{24}$$

$$\frac{C_s}{N}\frac{\mathrm{d}v_{u,l}}{\mathrm{d}t} = \left[\pm\frac{m_a V_{dc} w C_{load}}{2} \times \sum_{h=1}^{\infty} h(b_h cos(hwt) - a_h sin(hwt))\right] \times \left[\frac{m_a\left(\frac{a_0}{2} + \sum_{h=1}^{\infty}(a_h cos(hwt) + b_h sin(hwt))\right) \pm 1}{2}\right] \tag{25}$$

$$v_u(t) - 2V_{DC} = \frac{m_a^2 V_{dc} C_{load} N}{16 C_s}(1 - cos(2wt)) + \frac{m_{req} V_{dc} C_{load} N}{4 C_s} sin(wt) \tag{26}$$

$$v_u^i(t) - v_u^{avg} = \frac{m_a^2 V_{dc} C_{load}}{16 C_s}(1 - cos(2wt)) + \frac{m_{req} V_{dc} C_{load}}{4 C_s} sin(wt) \tag{27}$$

From voltage ripple expression per submodule in (27), it is clear that the ripple magnitude is independent of the frequency since the charge time product remains the same for different frequencies. However, it is mainly dependant on the ratio of the load capacitance and submodule capacitance and the DC link voltage. The derived expression of the ripple is verified in Sections V and VI with the down-scaled prototype and the full-scale simulation results. It is important to note that the capacitor voltage ripple is kept within 1% of the average capacitor voltage for more accurate output voltage waveforms. This strict ripple restriction does not require a large value of submodule capacitance since the HV AWG needs a low current magnitude. Hence, the full-scale prototype will have submodule capacitance in μF range, which is proved to be feasible later in Section VI. With negligible circulating current, the submodule capacitor voltages are naturally balanced within MMC without the strict requirement of an arm energy controller [56] or sorting algorithm [55], [72]. Because, the PSC modulation technique naturally distributes submodule insertion and bypassing evenly [54]. Additionally, if the switching frequency is chosen to be a non-integer multiple

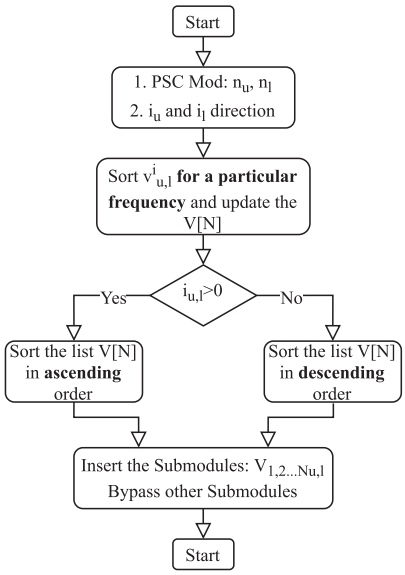


FIGURE 13. Flowchart of the implemented sorting algorithm.

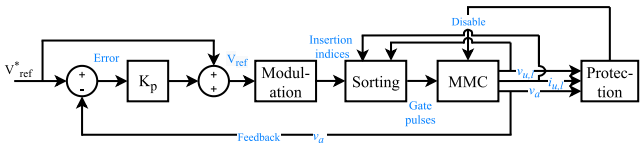


FIGURE 14. Control system of the MMC-based AWG.

of the fundamental frequency [46] with proper selection of the submodule capacitance, it is possible to have improved balanced capacitor voltages. However, the open-loop control of submodule capacitor voltage can lead to slightly different average capacitor voltage values due to small variations in each submodule hardware such as different delay in gate driver, tolerances in the submodule capacitance value, etc. Hence, a combination of both techniques is recommended here to improve the reliability of the HV AWG test source. In this paper, a simple sorting is implemented, where upper and lower arm capacitor voltages are sorted for desired frequency, and the gate pulses are assigned based on the direction of arm current and sorted capacitor voltages. The flowchart of the implemented sorting algorithm is illustrated in Fig. 13.

E. CONTROL SYSTEM

Since the HV AWG application does not need to control the power transfer, the control system block for MMC is adapted for accurate voltage waveform generation, as shown in Fig. 14. The feedback control of the voltage across the load ensures an acceptable steady-state error, and the measurement of the output current can provide fast protection in case of faults, e.g., flashover. Fig. 14 presents a simplified control system implemented and tested in the down-scaled prototype of the MMC-based AWG that will be discussed in Section V. The accuracy of the output voltage waveforms is improved with the reference voltage feedforward loop. This particular

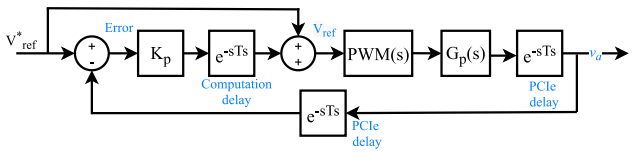


FIGURE 15. Block diagram of the control system of the MMC-based AWG.

controller is chosen for its simplicity and stable operation, and as it will be shown in the next session, it gives good results. Additionally, the submodule capacitor voltages are balanced using a simple selective sorting mechanism as discussed in Section IV-D.

Apart from the parameters discussed in IV-B, the available bandwidth for the generated voltage waveform gets affected by the closed-loop control. Its effect can be studied using the closed-loop block diagram of the MMC-based AWG in the continuous time domain, as shown in Fig. 15. This block diagram consists of the computation and communication delays named Peripheral Component Interconnect Express (PCIe). These delays are represented as exponential functions, and they depend upon the sampling period (T_s) implemented in the controller. (11) represents the plant's transfer function ($G_p[s]$). The generation of PWM in the continuous time domain can be represented as shown in (28) [73]. The modulation index (m_a) and the sampling period determine the magnitude of this transfer function. Additionally, the pulse width modulator samples the data with Zero-Order Hold (ZOH) function. Hence, it is fully represented in (28). The closed-loop transfer function of MMC is derived as shown in (29). This transfer function gives the small- and large-signal bandwidth, including the controller. It is visible that the sampling period plays an important role in determining the final bandwidth of the test source and its effect on the down-scaled prototype, and the full-scale prototype is studied in Sections V and VI, respectively.

$$G_{PWM}[s] = \frac{m_a G_{zoh}[s]}{T_s} = \frac{m_a(1 - e^{-sT_s})}{sT_s} \tag{28}$$

$$\frac{V_a[s]}{V_s[s]} = \frac{G_{sys}[s]}{1 + G_{sys}[s]}$$

$$G_{sys}[s] = (1 + G_{cd}[s])\frac{G_{pFB}[s]}{1 + G_{pFB}[s]}$$

$$G_{cd}[s] = K_p e^{-sT_s}$$

$$G_{pFB}[s] = G_{PWM}[s]G_p[s]e^{-2sT_s} \tag{29}$$

F. CONTROL HARDWARE AND OVERALL CONTROL ARCHITECTURE

Though the modular structure of the MMC offers scalability with respect to its hardware submodule, the controller hardware can create challenges for the scalability of the MMC with a large number of submodules. For the HVDC transmission application, the number of submodules per arm is in the range of 300 to 400, which makes a total of 1800 to 2400 submodules for 3-phase operation [74]–[76]. Such a structure requires a smaller sampling period, higher computing power, and bigger communication burden for the centralized controller implementation [77]. The MMC-based AWG with a submodule voltage rating above 3 kV will have 67 submodules or less, as shown in Table 2. It is important to note that the MMC-based AWG is a single phase implementation. Hence, the total number of submodules are 134 or less, which is roughly 5% of the total submodules required for a HVDC application. Hence, it is possible to have the centralized controller implemented in the FPGA in a single master control strategy [78]. The second reason for choosing the centralized controller is robustness. If the test object experiences a flashover and partial discharges, it can affect the distributed controller present on each submodule [79]. Considering the centralized controller and PSC modulation technique, the MMC-based AWG will need several FPGAs to implement the control. A commercially available real-time simulator with multiple FPGAs included can provide such a solution [80], [81]. The computation burden for the centralized control system can be optimized by adapting the tolerance band method for the submodule capacitor voltage balancing [72] over the simple sorting mentioned earlier. It is important to point out that the HV AWG application of MMC does not have significant circulating current present. Hence, it will reduce the number of switching operations required to balance the submodule capacitor voltages, resulting in the reduction of the computation burden.

V. SIMULATION AND EXPERIMENTAL RESULTS

The above-discussed design trade-offs of the MMC-based AWG are verified with the MATLAB-Simulink simulation and the existing down-scaled MMC prototype. This down-scaled MMC has 12 submodules where a half-bridge topology is implemented using the IGBTs PS219B4-S/-AS/-CS. It is tested with 300 V DC link voltage which can generate peak output voltage of 150 V. The load capacitance is chosen to be 6.8 μF to keep the same current rating as that of the full-scale prototype where the output voltage is 100 kV, and the load capacitance is 10 nF. This hardware setup is controlled using the OPAL-RT simulator (OP5600). Each submodule receives an enable and gate pulse signal and sends back the measurements of the submodule capacitor voltage via a digital voltage oscillator and fiber optics. The measurements of the output voltage across the load capacitance, the DC link voltage, and the arm currents are fed back to the OP5600. With the existing down-scaled prototype of MMC, the design trade-offs of the MMC-based AWG are demonstrated with 150 V output voltage rating, 6.8 μF load capacitance, and 200 Hz large-signal bandwidth. For these specifications, the value of L_a and R_a can be calculated to be 3 mH and 60 Ω, respectively, from equations (12) and (13). The above-mentioned system description is summarized in Table 3. Fig. 16 presents the experimental hardware of the down-scaled MMC prototype.

TABLE 3 System Parameters of Down-Scaled MMC Setup

No.	Description	Symbol	Values
1.	DC-link voltage	$2V_{dc}$	300 V
2.	Maximum output voltage	V_a	150 V
3.	Modulation index	m_a	0.9
4.	Number of submodules	N	12
5.	Switching frequency	F_s	1002 Hz
6.	Large-signal bandwidth (Open loop)	$f_{1\%err}$	200 Hz
7.	Submodule capacitance	C_s	4 mF
8.	Arm inductance	L_a	3 mH
9.	Arm resistance	R_a	60 Ω
10	Load capacitance	C_{load}	6.8 μF

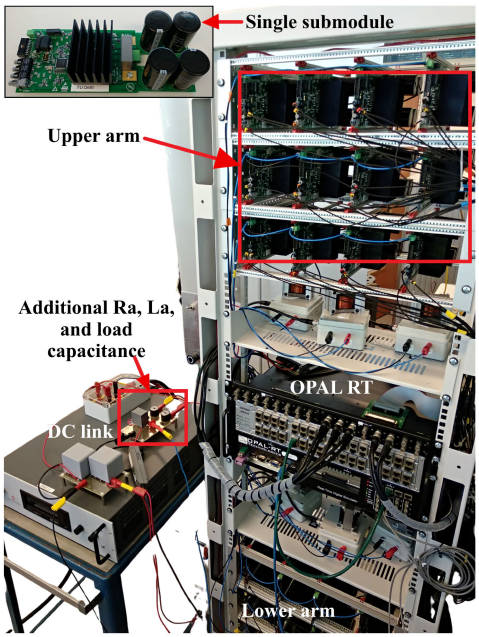


FIGURE 16. Experimental hardware setup.

The controller and various delays do impact the small- and large-signal bandwidth depending upon the sampling period, as discussed in (29). For the down-scaled prototype operated by OPAL-RT, the minimum obtained sampling period is 20 μs. Additionally, the parameter variations on the controller stability are studied using gain and phase margins, as shown in Fig. 17. From this figure, it is clear that the maximum proportional gain possible is five, after which the control system is unstable with negative gain and phase margin [82]. Hence, the small- and large-signal bandwidths are calculated for the same gain and 4.04 kHz, and 4.49 kHz are the obtained values for both bandwidths. These bandwidths are higher than the large-signal bandwidth calculated for the open-loop. Hence, the closed-loop is not affecting the bandwidth for generating accurate waveforms up to 200 Hz.

The performance of the down-scaled MMC-based AWG is demonstrated with three waveforms, i.e., harmonic test waveform, unipolar DC waveform, and unbalanced sinusoidal waveform, as discussed in Section II-C. Other periodic and complex waveforms are shown in the appendix A. First, the

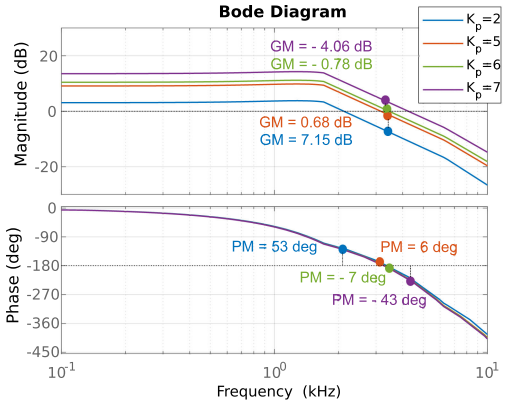


FIGURE 17. Variations of the proportional gain on controller/system stability.

simulation results are compared with the down-scaled prototype for the harmonic waveform in Fig. 18 for output voltage, output current, and submodule capacitor voltages. For clarity in the waveforms, only 4 submodule capacitor voltages are plotted i.e., Upper Arm 1 (UA_1), Upper Arm 12 (UA_{12}), Lower Arm 1 (LA_1), Lower Arm 12 (LA_{12}). It is clear from Fig. 18 that the MATLAB-Simulink simulations with ideal switches match well the experimental results. Small variations in the average submodule capacitor voltages in both arms can be attributed to the small tolerances present in the different submodules in terms of PWM delays in gate driver, submodule capacitance values, etc. Please note that the difference in average value of UA_1 and UA_{12} is only 0.33%. These non-idealities present in different submodules can be eliminated by implementing a sorting algorithm as discussed in IV-D, and its performance is shown in Fig. 18(c). From this figure, it can be concluded that the sorting algorithm removes the non-idealities present in each submodule and brings the average values of all submodules together. Furthermore, Fig. 19(b) shows the sorting algorithm working and how it brings the submodule capacitor voltage together dynamically. For simplicity, the submodule capacitor voltages are sorted continuously equivalent to a simulation step of 20 μs. Additionally, Fig. 19(a) illustrates the performance of the proposed proportional controller. In this figure, the closed-loop control is enabled at 40 ms. The error signal is normalized to 1 with a factor of 150 V. When the control is enabled, the error is reduced significantly, correcting the output voltage waveform. Moreover, the performance of this waveform is verified with the reference waveform in the frequency domain in Fig. 20. With correct values of filter and closed-loop control, it is possible to keep the error in the inserted harmonic magnitude around 1% for up to third harmonics and within 4% for higher harmonics. As per the design condition applied by (12), the error in the first three inserted harmonics remains around 1%. Though the condition of 1% error was applied till 4^{th} harmonic, the slightly higher error of 1.73% is obtained in the 4^{th} harmonic due to its small magnitude (0.5% of fundamental magnitude).

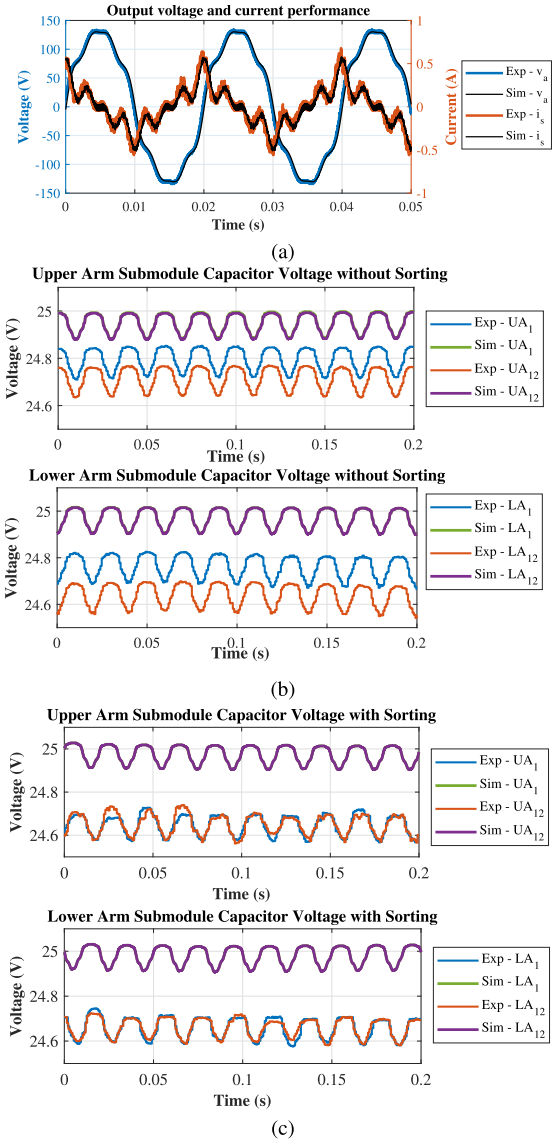


FIGURE 18. **Comparison of simulation results with experimental results for Harmonic test waveform in time domain (a) Output voltage and current, Submodule capacitor voltage, (b) without sorting, and (c) with sorting.**

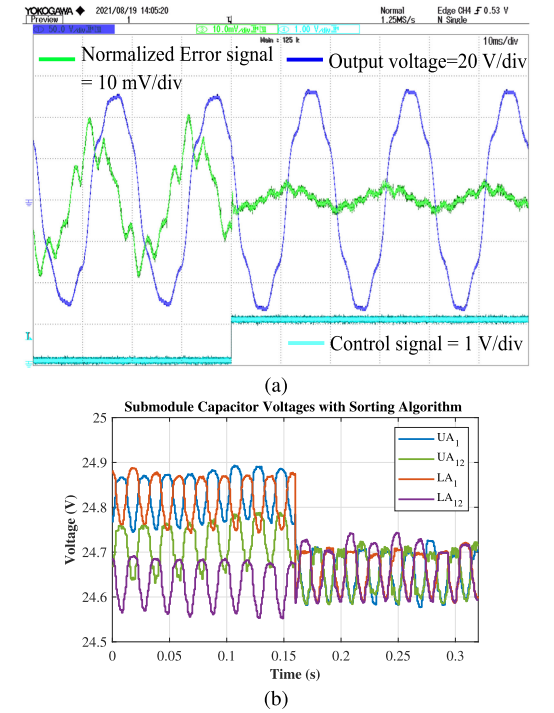


FIGURE 19. **Performance of (a) Proportional controller, (b) Sorting algorithm implementation for Harmonic test waveform.**

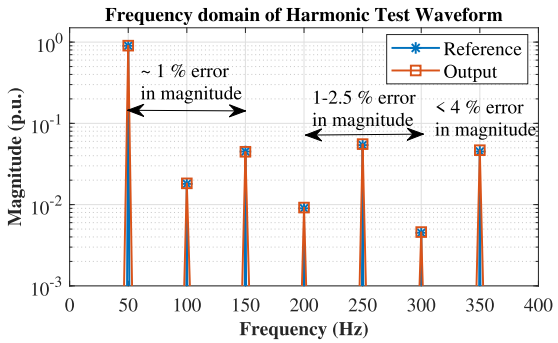


FIGURE 20. **Harmonic test waveform in frequency domain.**

Second, Fig. 21 presents an oscilloscope screenshot of the unipolar complex waveform generated from the down-scaled prototype. The output current and voltage are measured from external voltage and current probes. The pre-selected submodule capacitor voltages (UA_1, UA_{12}, LA_1, LA_{12}) are acquired in real time from the OPAL-RT measurements. Hence, these waveforms are scaled down to stay within the limits of the analog output ports of the OPAL-RT. The submodule capacitor voltages are normalized to 10 with a factor of 2.5. The bottom waveforms are submodule capacitor voltages from 1st submodule from the upper arm and the 12th submodule from the lower arm. From this screenshot, it is visible that the ripple of the upper and lower arm submodules are different. It is because of the unipolar waveform. When an unipolar

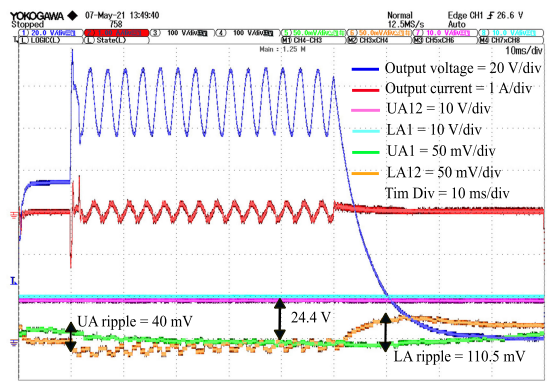


FIGURE 21. **Unipolar complex waveform in time domain.**

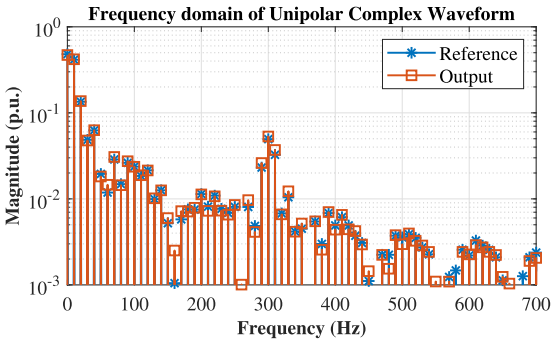


FIGURE 22. Unipolar complex waveform in frequency domain.

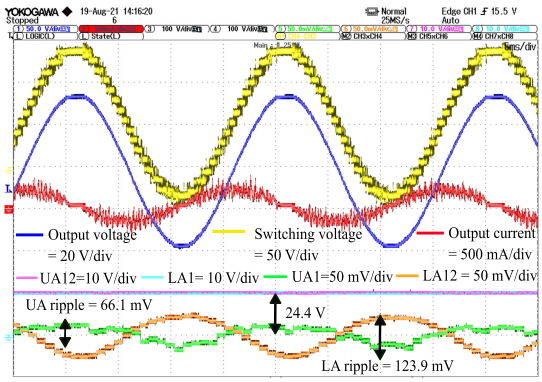


FIGURE 23. Unbalanced sinusoidal waveform in time domain.

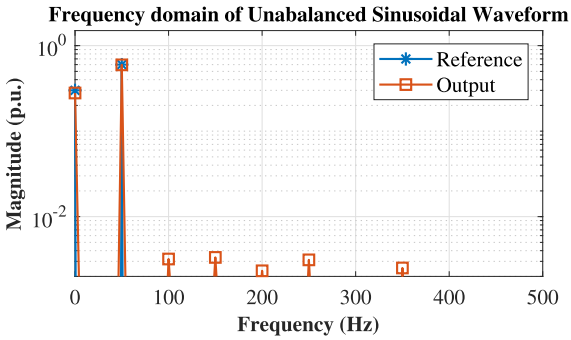


FIGURE 24. Unbalanced sinusoidal waveform in frequency domain.

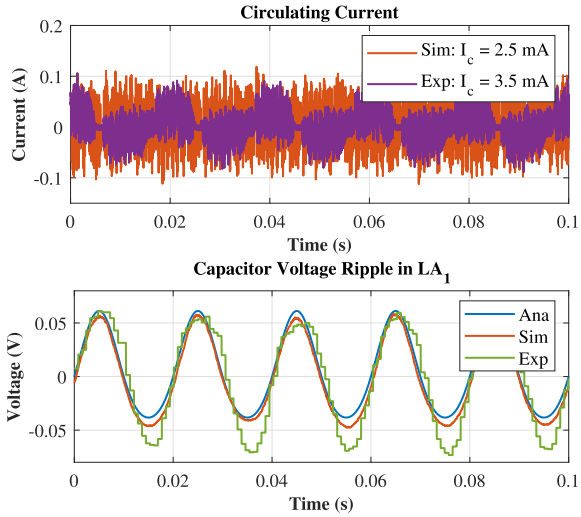


FIGURE 25. Comparison of capacitor voltage ripple analytically, using simulations, and experimentally.

waveform is generated from the MMC, one of the arms (in this case: UA) is not get fully utilized, and only a maximum of half of its number of submodules are inserted. However, this does not affect the capacitor voltage balancing. Additionally, this waveform is not repetitive, and voltage balancing is not at the most priority. After the first test is finished with this waveform, the MMC will need to restart with all capacitor voltages charged to the average values for the next test. Additionally, the full-scale simulation results show the capacitor voltage ripple in detail. This complex waveform consists of a switching impulse that has a rise time of 250 μs which constitutes the peak magnitude of the waveform. The error in this peak magnitude is kept to be 0.1%, which is well within limits given in the IEC standard [29]. Moreover, the performance of this waveform is verified with the reference waveform in the frequency domain in Fig. 22.

Similar to the unipolar complex waveform, Fig. 23 shows the performance of unbalanced sinusoidal waveform in the time domain. For even mixed polarity waveform, the upper and lower arm voltage ripple has different values, as shown in Fig. 23. However, this does not affect the capacitor voltage balancing. The quality of the generated waveform is illustrated in the frequency domain in Fig. 24, and they match well for the DC component and 50 Hz component. With this waveform, mathematical ripple expression derived in Section IV-D is compared analytically, with simulations, and with experiments. First, the ripple expression is plotted together with simulation and experimental results in Fig. 25. Additionally, the circulating current obtained from simulation and experimental results is plotted together with the ripple expression. The simulation results match well with the analytical results for capacitor voltage ripple. Even the experimental results match well in the positive cycle of ripple. However, the experimental ripple is slightly higher on negative peaks compared to analytical and simulation results. It could be because of the low magnitude (110 mV) measured from a digital voltage oscillator designed to measure relatively high voltage (200 V). Furthermore, the average circulating current with a simulation model and experimental setup is relatively low, verifying the assumption of zero average circulating current. Please note that the circulating current is switching positive or negative depending upon the balance between the DC link and the total voltage of the inserted submodule capacitors. If the total voltage of the inserted submodule capacitors is higher than the DC link, the circulating current will be negative and vice versa. The average capacitor voltage ripple is compared for the harmonic test waveform and unbalanced sinusoidal waveform in Table 4. Since the unipolar complex waveform has a complex Fourier spectrum, it becomes computationally challenging to

TABLE 4 Capacitor Ripple Calculations for Waveforms Which Were Shown in Fig. 6

	Analytically calculated (mV)	Simulation results (mV)	Downscaled prototype (mV)
1. Harmonic test waveform	110.2	111.3	131.8
2. Unbalanced sin waveform	UA = 53.5 LA = 99.4	UA = 43.3 LA = 111.5	UA = 40 LA = 110.5

TABLE 5 Performance of Down-Scaled MMC Setup for Waveforms Which Were Shown in Fig. 6

	Magnitude error (%)	THD (%)	Losses (W)
1. Harmonic test waveform (K_p=5)	1 % till 3rd harmonic up to 4 % in higher harmonic	0.34	0.89
2. Unipolar complex waveform (K_p=1)	0.1 % error in the peak of switching impulse	3.30	0.3
3. Unbalanced Sine waveform (K_p=3)	2.9 % error in the positive peak	3.66	0.3

derive the analytical expression even numerically. For the two waveforms, the analytically calculated voltage ripple matches the simulation results. However, a slightly higher value is obtained experimentally due to measurement inaccuracies. With the load capacitance of 6.8 μF and submodule capacitance of 4 mF, the ripple is kept within 1% of the average capacitor voltage, which satisfies the earlier condition decided in Section IV-D.

To analyse the quality of the obtained waveforms furthermore, the definition of THD is adapted for non-sinusoidal voltage waveforms, as shown in (30), to quantify the harmonic performance of the MMC-based AWG. The obtained THD for the harmonic test waveform, unipolar complex waveform, and unbalanced sinusoidal waveform is 0.34%, 3.30%, and 3.66% respectively. These THD values are well below 5% which is within the industrial standard of the allowed distortion in the grid [83]. Apart from the quality of the obtained voltage wave shape and balancing of the submodule capacitor voltages, the losses in the added series resistance are less than 1 W for the shown wave shapes, which justify the usage of the passive damping technique. The overall performance of the AWG is summarised in Table 5.

$$THD_{nonsin} = \frac{\sqrt{\sum_{h=0}^{\infty}(V_{h,ref} - V_{h,out})^2}}{V_{1,out}} \tag{30}$$

VI. DISCUSSION ON REALIZING THE FULL-SCALE PROTOTYPE

This section addresses challenges concerning realizing the full-scale prototype able to deliver a peak voltage of 100 kV. As discussed in Section IV-C, switches are the centrepiece in determining the voltage rating of the submodule. With the suggested solution of selecting SiC MOSFETs, the protection design becomes more challenging [84]. Apart from that, the

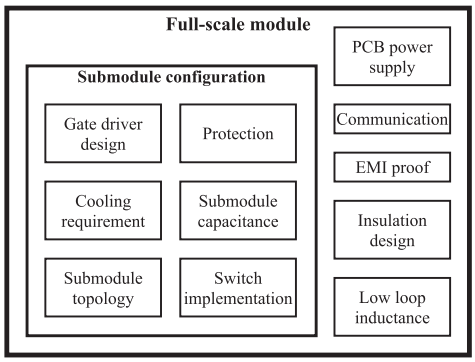


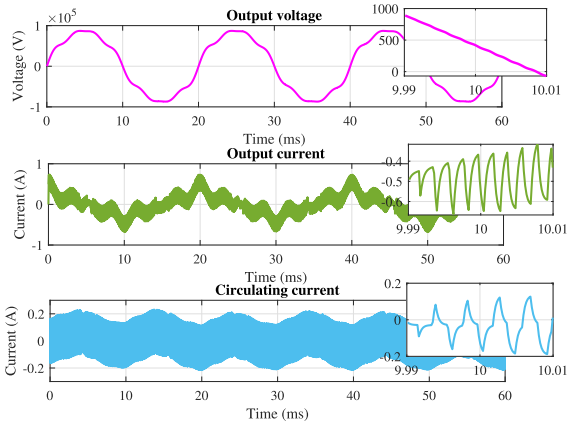
FIGURE 26. Challenging elements in the full-scale module.

TABLE 6 System Parameters of Full-Scale HV MMC Setup

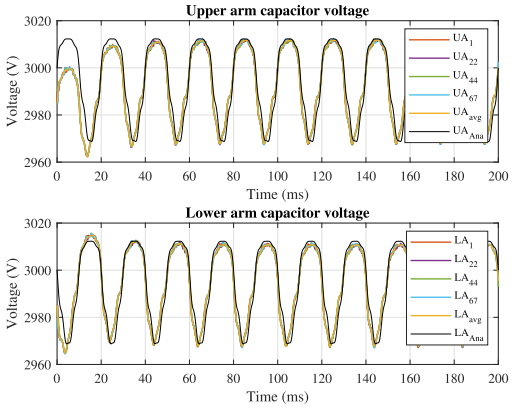
No.	Description	Symbol	Values
1.	DC-link voltage	$2V_{dc}$	200 kV
2.	Output voltage	V_a	100 kV
3.	Modulation index	m_a	0.9
4.	Number of submodules	N	67
5.	Large-signal bandwidth (Open loop)	$f_{1\%err}$	500 Hz
6.	Submodule capacitance	C_s	10 µF
7.	Arm inductance	L_a	3.2 mH
8.	Arm resistance	R_a	9.1 kΩ
9.	Load capacitance	C_{load}	10 nF

auxiliary power supply design is critical. Generally, this auxiliary power supply is obtained from the submodule capacitance [85]. However, the large range of output voltage ratings of the MMC requires a variable DC link voltage. It is more advantageous to change the DC link voltage instead of reducing the number of levels, affecting the harmonic performance. Additionally, the PCB design for the submodule has other challenges of insulation design, cooling system design, and low loop and stray inductance [86]. The mentioned challenges are illustrated in the Fig. 26.

After resolving these hardware challenges, the realized full-scale prototype of the MMC-based AWG will be smaller and cheaper than the MMC for HVDC application for various reasons. First, two obvious reasons are the requirement of the single-phase for the MMC-based AWG over to the three-phase for the HVDC application and the 100 kV output voltage rating, which is lower than the output voltage ratings at the HVDC converter stations (more than 100 kV [42]). MMC is a scalable technology, and the submodules are the elementary building blocks of the system which mainly determines the size and cost of the entire converter. Among the many components present on the submodule, as shown in Fig. 26, the submodule capacitance occupies half of the volume of each submodule [87]. Hence, the size of the converter is largely affected by the choice of submodule capacitance. As discussed in Section IV-D, the submodule capacitance will lie in the μF range for the MMC-based AWG. Hence, the size of each submodule can be much smaller if they are compared at the same voltage rating with the MMC for traditional applications. Additionally, the discrete TO-247

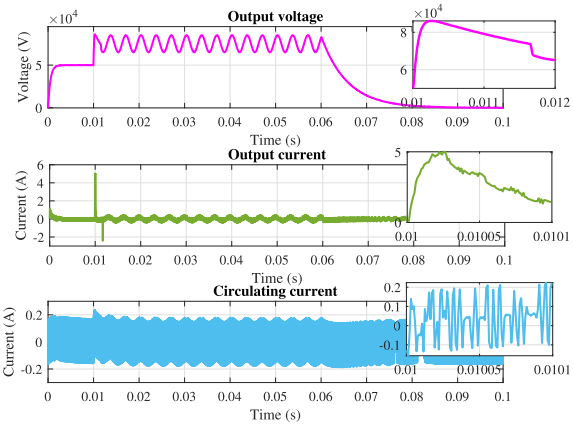


(a) Output performance

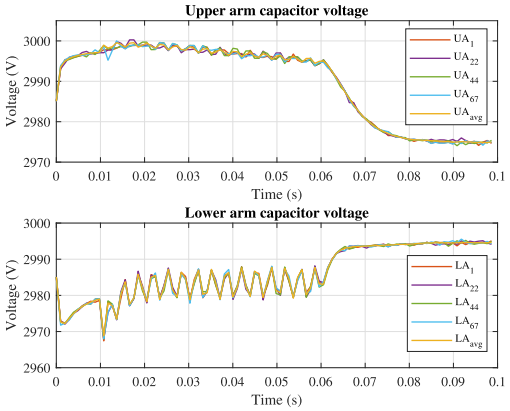


(b) Submodule capacitor voltage

FIGURE 27. **Performance of harmonic test waveform.**



(a) Output performance



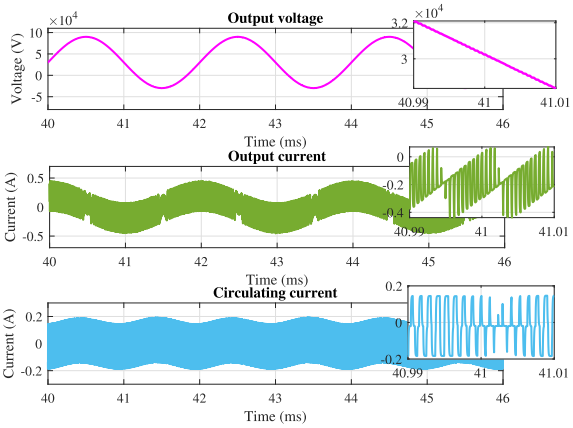
(b) Submodule capacitor voltage

FIGURE 28. **Performance of unipolar complex waveform.**

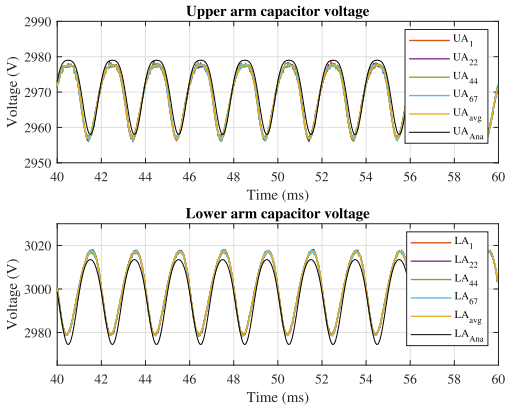
packaged switches specifically designed for HV application (IXYX40N450HV, 4.5 kV and 40 A: 23 mm × 16.2 mm × 5.1 mm) occupies less space over to the power modules (FZ1200R45KL3B5, 4.5 kV and 1.2 kA: 190 mm × 140 mm × 38.5 mm) the same voltage rating. Considering significantly smaller current rating, the conduction losses will be relatively easy to manage, simplifying the cooling requirement. This will reduce the cost and weight of the system and simplify the mechanical structure of the MMC-based AWG over existing solutions of MMC. The MMC-based AWG can provide a higher current rating at a higher voltage level with higher bandwidth than the existing solution of AWG as HV amplifier. Hence, comparing the cost and size of two HV AWG solutions is unfair since the MMC-based AWG can offer many more capabilities than the HV amplifier system.

Furthermore, the performance of the full-scale HV MMC-based AWG is verified with MATLAB-Simulink simulations with 67 submodules per arm and the system parameters are summerized in Table 6. The system can generate 100 kV with 10 nF load capacitance. The values of L_a and R_a are designed as per the guideline discussed in Section IV-B. Additionally, the closed-loop system discussed in Section IV-E is designed for the full-scale prototype with a proportional gain of 5 and a simple sorting algorithm with a sorting frequency of 5 kHz. From the transfer function derived in (29), small- and large-signal controller bandwidth is calculated as 31.2 kHz and 35.3 kHz respectively with 200 ns sampling period. These controller bandwidths show that they do not interfere with the designed open-loop bandwidth of the voltage waveform. Additionally, 200 ns sampling period allows to generate accurate gate pulses up to 37 kHz for 67 submodules per arm ($(1/T_s) = 2NF_{smax}$). Hence, the commercially available devices discussed in Section IV-F can be a possible solution since they can provide a sampling period as small as 200 ns.

Similar to the down-scaled prototype, the performance of the full-scale AWG is showcased with three wave shapes in Fig. 27, Fig. 28, and Fig. 29. These figures show the performance of HV AWG in terms of output voltage, output current, and circulating current with their zoomed pictures. Here, the dynamics of switching circulating current is visible with the zoomed pictures for all three waveforms. This proves the assumption of negligible circulating current with the simulations of the full-scale prototype. Especially for the unipolar complex waveform in Fig. 28(a), the zoomed picture



(a) Output performance



(b) Submodule capacitor voltage

FIGURE 29. Performance of 50 Hz unbalanced sinusoidal.

TABLE 7 Performance of Full-Scale HV MMC Setup for Waveforms Which Were Shown in Fig. 6

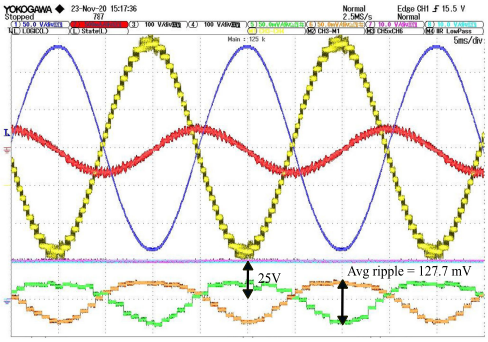
	Magnitude error (%)	THD (%)	Losses (W)
1. Harmonic test waveform (K_p=5)	Less than 1 % for all harmonics	0.01	223.52
2. Unipolar complex waveform (K_p=5)	Approx. 0 % error in the peak of switching impulse	0.2	163.53
3. Unbalanced Sine waveform (K_p=5)	Approx. 0 % error in the positive peak	0.15	238.65

of a switching impulse is shown. With the proper design of the MMC system parameters, the switching impulse shows an expected rise time of 250 μs. Hence, the obtained THD of the waveform is less than 1%. Similarly, the harmonic test waveform can generate much more accurate harmonics. All these results are summarized in Table 7, along with losses that occurred in the arm resistors. These losses are reasonable for the 10 kW full-scale system, where these losses constitute only 2% of the total power delivered from the input side. Furthermore, these figures show the selected (1^{st}, 27^{th}, 44^{th}, 67^{th}) submodule capacitor voltages from upper and lower arms along with their average values. For harmonic test and unbalanced sinusoidal waveform, the analytically derived submodule capacitor voltage is plotted along with the simulation results. The derived analytical expression matches well with the simulation results of the full-scale prototype. Please note that the chosen submodule capacitance of 10 μF is sufficient for the load capacitance of 10 nF, keeping the ripple 1.5% of the average capacitor voltage. For unipolar complex waveform, only one cycle is needed, and it is seen clearly that the upper and lower arm have a different ripple.

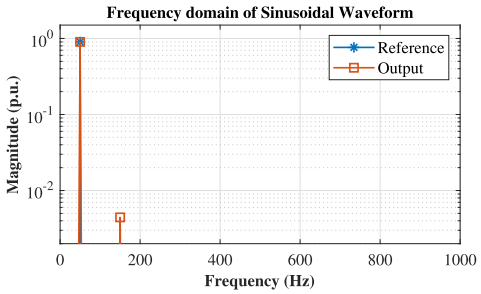
VII. CONCLUSION

This paper introduces the huge potential of MMC to generate complex arbitrary waveforms with good accuracy for HV AWG application. At the beginning of the article, specific characteristics of the HV AWG application are highlighted namely, no intentional active power transfer, low current rating, arbitrary wave shapes, and equivalent capacitive load. Additionally, the performance parameter for the HV AWG application is not the power efficiency of the converter but the voltage efficiency of the generated waveform. These differences give essential HV design requirements for the MMC in terms of output voltage, output current, and the large-signal bandwidth. Based on the new specifications for MMC, the design trade-offs are analyzed by simplifying the complex structure of the MMC into two partially coupled circuits, i.e., output current and circulating current circuit. The output current circuit determines the harmonic performance of the AWG. Its parameters, i.e., modulation technique, L_a, R_a, N, SM devices, submodule capacitance, control system, control hardware, and overall control architecture are studied in detail to obtain the accurate voltage waveforms as per HV testing standards. The circulating current circuit balances the inserted submodule capacitor voltages and the submodule capacitance plays an important role here.

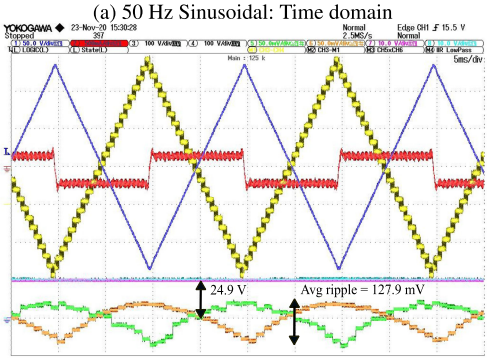
It is found that the PSC modulation technique provides additional advantages over NLC by shifting the carrier harmonics to N^{th} of the switching frequency without changing any baseband harmonics present due to non-sinusoidal wave shape. The arm inductance and series resistance filter the undesirable voltage harmonics and determine the available small- and large-signal bandwidth and slew rate. To obtain higher bandwidths and slew rate, lower values of arm inductance should be used. However, it demands a higher switching frequency to attenuate the carrier harmonics, and a higher switching frequency needs higher accuracy from the controller hardware. Hence, SiC MOSFETs seems to be the most suitable solution with the possibility of higher switching frequency to be controlled using an FPGA-based controller. Apart from this, the analytical expression of submodule capacitor voltage ripple is derived from selecting the value of submodule capacitance using the averaging principle. This derivation is based on the fact that the HV AWG application does not need a large circulating current. This is the reason why submodule capacitor voltages are well balanced even when complex wave shapes are generated.



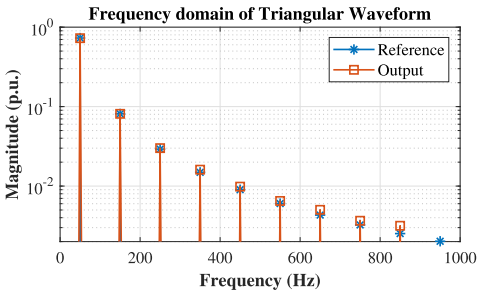
(a) 50 Hz Sinusoidal: Time domain



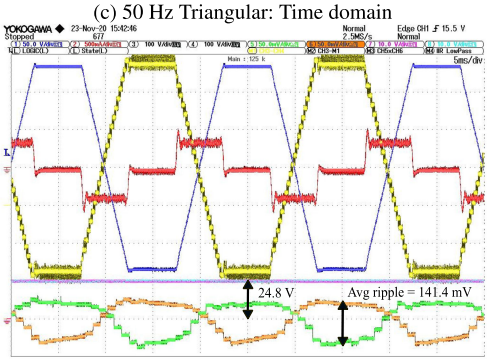
(b) 50 Hz Sinusoidal: Frequency domain



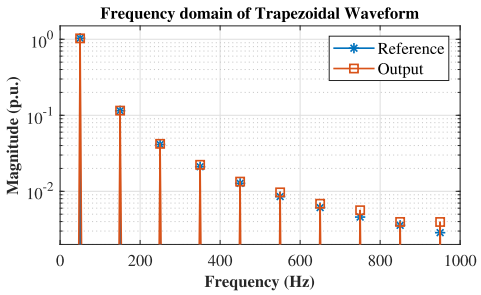
(c) 50 Hz Triangular: Time domain



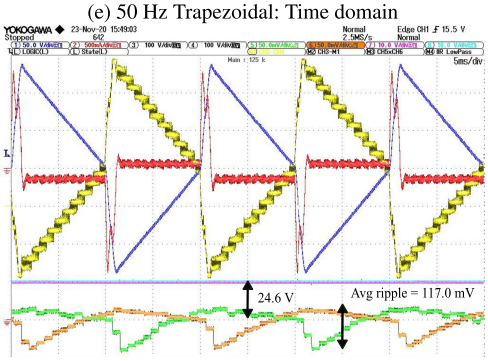
(d) 50 Hz Triangular: Frequency domain



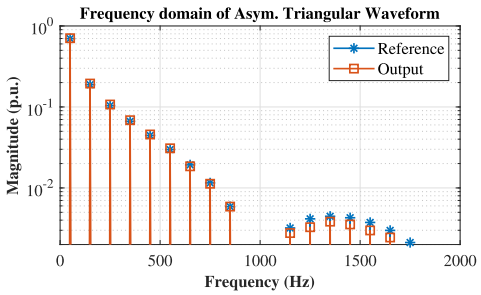
(e) 50 Hz Trapezoidal: Time domain



(f)50 Hz Trapezoidal: Frequency domain



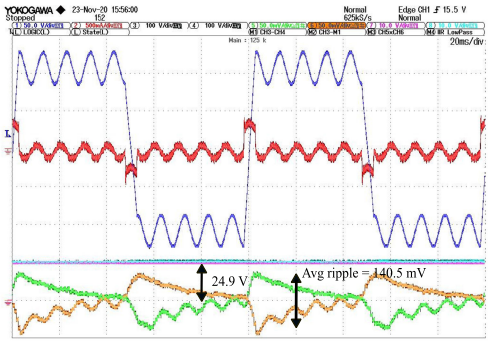
(g) 50 Hz Asymm. Triangular: Time domain



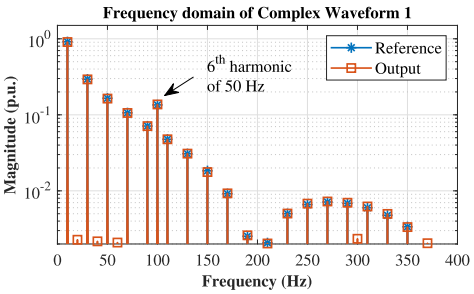
(h) 50 Hz Asymm. Triangular: Frequency domain

FIGURE 30. Periodic waveforms generated from the small prototype of the MMC-based AWG. [Blue: v_a = 50 V/div, red: i_s = 0.5 A/div, Yellow: v_s = 50 V/div, Pink & sky blue: UA_{12} & LA_1 = 10 V/div, Orange & Green: UA_1 & LA_{12} = 50 mV/div, Time Div=5 ms/div]

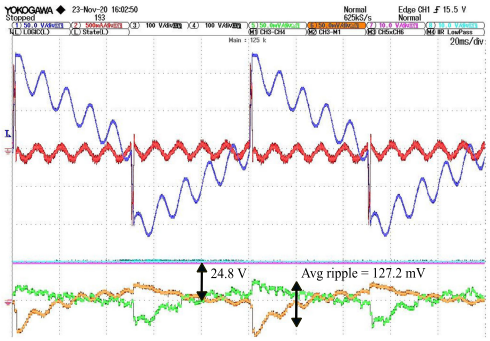
The discussed design trade-offs are demonstrated using MATLAB-Simulink simulations and a down-scaled prototype of a MMC with 12 submodules. Firstly, an important observation is that the obtained simulations with MATLAB-Simulink match well with the experimental results. Secondly, the down-scaled prototype can already provide voltage waveforms with reasonable accuracy for the design value of voltage, current, bandwidth, and the control system. These waveforms include bipolar, unipolar, and mixed polar waveforms to show the performance of MMC-based AWG. The THD of most waveforms is less than or around 1% except for unipolar complex waveform and unbalanced sinusoidal waveform where it is around



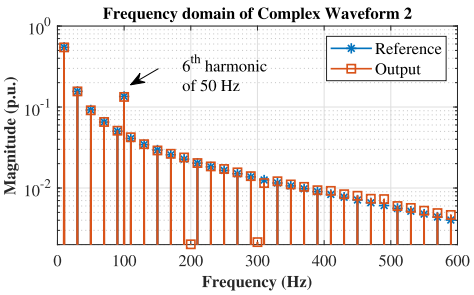
(a) 10 Hz Complex waveform 1: Time domain



(b) 10 Hz Complex waveform 1: Frequency domain



(c) 10 Hz Complex waveform 2: Time domain



(d) 10 Hz Complex waveform 2: Frequency domain

FIGURE 31. Complex waveforms generated from the small prototype of the MMC-based AWG. [Blue: v_a = 50 V/div, red: i_s = 0.5 A/div, Yellow: v_s = 50 V/div, Pink & sky blue: UA_{12} & LA_1 = 10 V/div, Orange & Green: UA_1 & LA_{12} = 50 mV/div, Time Div=20 ms/div]

3%. Thirdly, the theoretical assumption of negligible circulating current and the derived submodule capacitor voltage expression are proved with MATLAB-Simulink simulations and experimentally with the down-scaled prototype. Additionally, the sorting algorithm is implemented to improve the submodule capacitor voltage balancing by removing non-idealities in different submodules. On the same topic, the ripple in the submodule capacitor voltages suggests that the submodule capacitance requirement for HV AWG application is much smaller than that for the traditional energy transmission application of MMC.

Though MMC is scalable for its hardware, it is not translated to its controller. However, HV AWG is a single-phase MMC with a significantly lower number of submodules compared to that of the HVDC transmission. Hence, it is expected to be possible to implement the control system in a centralized controller with a commercially available real-time simulator where multiple FPGAs are available. Overall, the HV AWG will be cheaper and smaller in size compared to existing MMC solutions for grid applications. The performance of the full-scale HV AWG is verified in MATLAB-Simulink with 67 submodules, especially for the circulating current dynamics, submodule capacitance choice, and harmonic performance of the output voltage. In summary, this paper provides a complete analysis of design guidelines for realizing an MMC-based HV AWG for performing dielectric testing on grid assets.

TABLE 8 Performance of MMC-Based AWG for Periodic and More Complex Waveforms

	Magnitude error (%)	THD (%)	Losses (W)
1. Sinusoidal (K_p=3)	0.67	0.47	0.76
2. Triangular (K_p=2)	0.67	0.59	0.53
3. Trapezoidal (K_p=2)	2.22	0.38	1.07
4. Asymm. Triangular (K_p=2)	2.22	1.07	1.45
5. Complex waveform 1 (K_p=2)	1.36	0.72	0.19
6. Complex waveform 2 (K_p=2)	3.79	1.10	0.17

APPENDIX A
OTHER WAVEFORMS OBTAINED FROM THE DOWN-SCALED PROTOTYPE OF THE MMC-BASED AWG

This appendix presents more waveforms obtained from the down-scaled prototype. These waveforms include both periodic and complex waveforms. They are illustrated in Fig. 30 and Fig. 31 with both the obtained time and frequency domain performance. Additionally, all the performance parameters are summarized in Table 8. The derived capacitor voltage expression is compared with the simulation and experimental results in Table 9. As observed earlier, the experimentally obtained voltage ripple is slightly higher, especially for trapezoidal based waveform due to measurement inaccuracies at low voltage. The negligible circulating current answers why the submodule capacitor voltages get balanced even when higher harmonics are generated.

TABLE 9 Capacitor Ripple Calculations for Periodic and Complex Waveforms

	Analytically calculated (mV)	Simulation results (mV)	Downscaled prototype (mV)
1. Sinusoidal	114.7	115.6	127.7
2. Triangular	114.3	116.4	127.9
3. Trapezoidal	114.7	119.6	141.4

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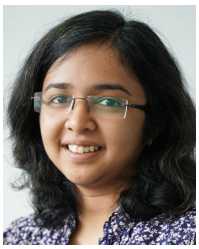

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