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***Abstract*—Accurately sensing the temperature in silicon carbide (power) devices is of great importance to their reliable operation. Here, temperature sensors by resistive and CMOS structures are fabricated and characterized in an open silicon carbide CMOS technology. Over a range of 25-200°C, doped design layers have negative temperature coefficients of resistance, with a maximum change of 79%. Secondly, CMOS devices are used to implement a CTAT, which achieves a maximum sensitivity of 7.5mV/K in a temperature range of 25-165°C. The integration of readout electronics and sensors that are capable of operation in higher temperature than silicon, opens application in harsher environments.**

Keywords—4H-SiC; SiC CMOS; silicon carbide; temperature sensor; wide bandgap semiconductors

I. INTRODUCTION

The field of wide bandgap semiconductors has gained increased research interest over the past decades. Applications in power electronics [1,2] are promising and expected to have substantial future markets [3], with silicon carbide (SiC) and gallium nitride (GaN) as the main materials of choice. Due to the large demand of SiC and GaN based power devices, material costs are steadily decreasing. This development is expected to enable other cost-effective future application of these materials, like integrated systems in harsh environment sensing [4-9].

Silicon carbide is known for its polytypism, which is the phenomena of having multiple crystal structures without changing the chemical composition. At present, the most mature technology uses the 4H-SiC polytype, which has a bandgap of 3.2eV. This bandgap enables application in higher operation temperatures than silicon-based technology as the intrinsic carrier concentration is lower. It is desirable to integrate temperature sensors in systems that need to endure elevated temperatures for monitoring and conditioning of the integrated systems. As such, implementation of SiC temperature sensors in integrated circuit technologies is required.

Over the last twenty years, different technologies for integrated circuit design in SiC were reported, all of which focused on the high temperature application of such circuits. These technologies include CMOS [10-13], BJT [14,15], JFET [16,17] and MESFET [18,19], but access to these mostly proprietary technologies is limited. Fortunately, the SiC CMOS technology developed by Fraunhofer IISB is addressing this need. A vertical p-i-n diode temperature sensor is already reported in this technology [21] and has a sensitivity of 2.3-3.4mV/K for a wide operating range and shows excellent linearity.

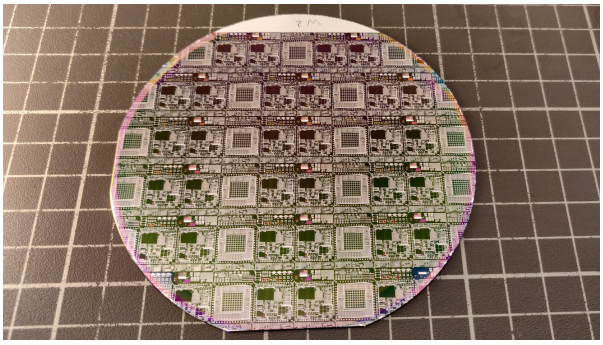

Fig. 1 Photograph of the multi-project four inch silicon carbide device wafer, fabricated in the Fraunhofer IISB SiC CMOS technology [20].

This work reports on temperature sensing in the state-of-the art 6 µm 4H-SiC CMOS technology [20], developed by Fraunhofer IISB. The temperature coefficient of resistance of highly doped layers is characterized up to 200 °C and compared to a circuit-based temperature sensor in a similar range. By implementing temperature sensing capability in an integrated circuit technology in silicon carbide, future work can incorporate temperature sensors in systems that operate in temperatures that exceed the capabilities of silicon, like power devices or harsh environment sensors.

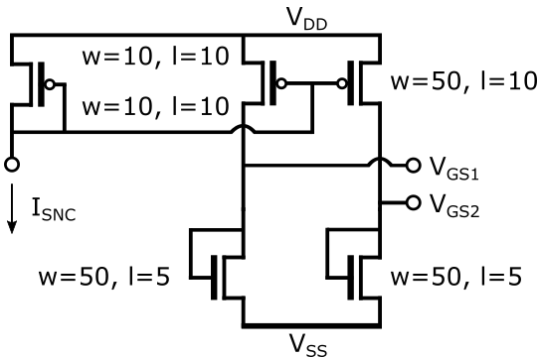

Fig. 2 CMOS circuit of the five transistor diode-based CTAT. The transistor channel width and length is annotated for each device. The circuit requires an external current bias source I_{SNC}, which corresponds to a bias voltage V_{SNC} at that node.

II. Technology Overview

The reported 4H-SiC CMOS technology is used for the fabrication of 100mm multi-project wafers (Fig. 1). The front-end-of-line is a double well process in an n-type epitaxial layer, providing the n-well, p-well, n++ and p++ design layers for device design. The back-end-of-line employs silicides by an RTA process to form ohmic contacts to the n++ and p++ layers. The MOSFET gate material is polysilicon, which offers local interconnect possibilities. A single metallization layer is included for all other interconnections. The CTAT CMOS circuit (Fig. 2) is integrated alongside the monolithic resistors.

III. Results and Discussion

A. Resistance Characterization

Resistive test structures are characterized on wafer-level by means of 4-point measurement on 30 dies. A semi-automatic MicroTech Cascade probe station is used in combination with an Agilant 4156C Precision Semiconductor Parameter Analyzer and the setup is controlled through IC-CAP measurement software. The chuck in the probe station is temperature controlled and measurements are performed at stable temperature.

The normalized sheet resistance of the doped n++ SiC and polysilicon layers is extracted for different temperatures in the range of 25-200°C by measuring Van der Pauw Greek cross structures (Fig. 3). The other doped layers could not be measured in this way, as they are not isolated from the substrate. The polysilicon layer has a positive temperature coefficient of resistance (TCR) that is linear in the measured range, with a maximum change of 15%. This corresponds to previously reported values in literature [22,23]. In contrast, the doped n++ layer has a negative TCR and is not linear in the measured range, with a maximum change of 19%. Dopant atoms in hexagonal silicon carbide have higher ionization energies compared to the cubic silicon crystal structure. Therefore, the dopant atoms are not fully ionized at room temperature [24], explaining the negative TCR and non-linear behavior. Though the doped n++ layer has a larger variation, the non-linear TCR is a drawback.

Next, resistors are integrated and measured over the 20V operating range of the SiC CMOS (Fig. 4a), in which the resistors show linear behavior. There is a small deviation between the results found from the sheet resistance measurement and the integrated resistors, which is likely due to very different bias conditions (-0.1-0.1V for the Van der Pauw structures). The maximum deviation in resistance of the monolithic resistors is 20%. Furthermore, the n++ integrated resistor is measured and compared with its p++ counterpart (Fig. 4b). This reveals that the p++ layer has a significantly higher sensitivity to temperature increase, reaching a change in resistance up to 79%. The difference is again attributed to the ionization energy, as the aluminum

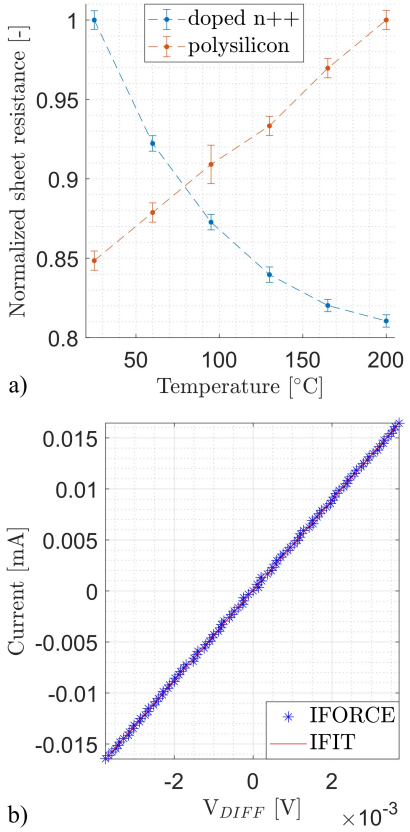

Fig. 3 Normalized resistance (R/R_{max}) of the doped n++ SiC and polysilicon layers for different temperatures in a), exhibiting a negative and positive TCR respectively. The resistance is extracted from IV curves in b) biased in the linear region (-0.1V to 0.1V) through a linear fit on 101 data points in Matlab, of which the inverse slope gives the resistance. The errorbars correspond to the standard deviation.

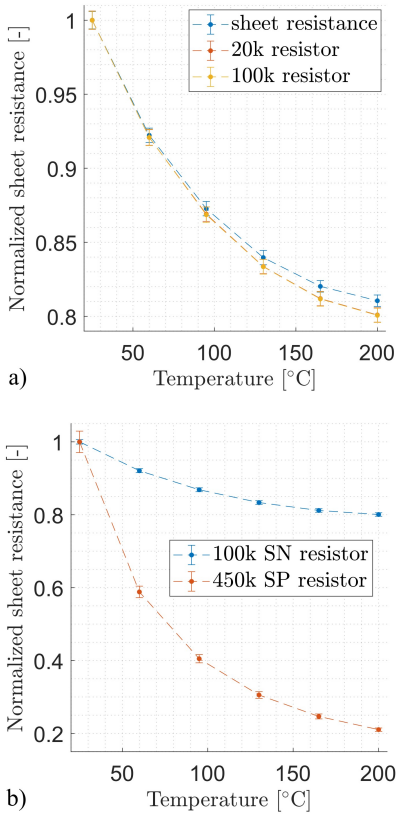

Fig. 4 Comparison of the normalized resistance (R/R_{max}) for different temperatures of doped n++ SiC in a), showing a small deviation between the sheet resistance and specific value resistors. The doped n++ and p++ SiC layers are compared in b), revealing a much higher TCR for the doped p++ SiC layer. The errorbars correspond to the standard deviation.

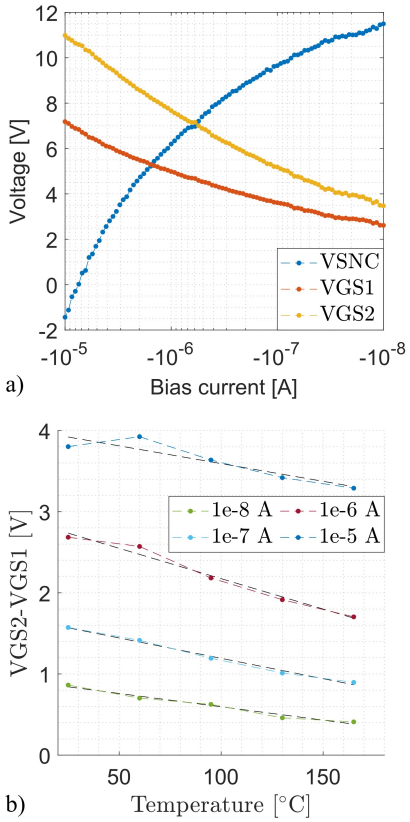

Fig. 5 Response of the CTAT in a) for different current biasing and a temperature of 25°C, listing the bias voltage V_{SNC} and differential outputs V_{GS1} and V_{GS2}. For a selection of current bias conditions, the differential output is plotted in b) for different temperatures. Linear fits are added to each respective curve, of which the slope gives the sensitivity in V/K.

p-type dopant shows a larger variation in the fraction of ionized dopants compared to phosphorus or nitrogen over this temperature range [24].

B. CTAT

The five-transistor diode-based CTAT (Fig. 2) is characterized by a logarithmic sweep of its current biasing I_{SNC} in the range of 10^{-8}-10^{-5}A. The corresponding voltage bias V_{SNC} and differential outputs V_{GS1} and V_{GS2} are measured (Fig. 5a). The magnitude of the differential output (V_{GS2}-V_{GS1}) depends on the current bias but is also sensitive to temperature. To visualize this, four bias levels are selected, and the corresponding differential output is plotted and fitted to a linear curve for different temperature points (Fig. 5b). The resulting sensor sensitivities are in the range of -3.3mV/K to -7.5mV/K, of which the highest sensitivity corresponds to a current bias of 10^{-6}A. This sensitivity is two times higher than the previously reported temperature sensor in this technology [21], within this temperature range.

C. Outlook

The DC response of a small and large inverter [20] is characterized for 25°C and 200°C (Fig. 6). The difference in response is negligible, except for a lower output voltage for the large inverter. This suggests that one can expect similar behavior of digital circuits at 200°C, operated at low frequencies. This prospect would allow sensor integration

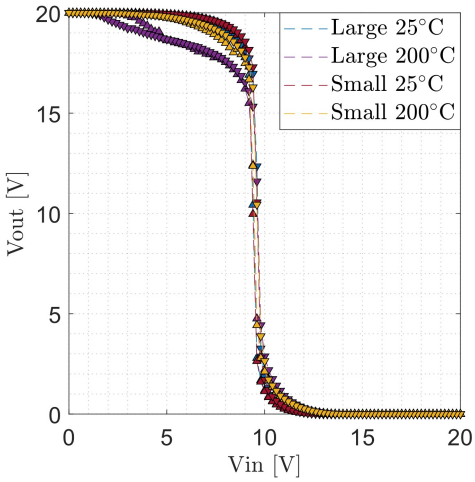

Fig. 6 DC response of a large (40x6 µm NMOS and 160x6µm PMOS) and small (20x6 µm NMOS and 80x6µm PMOS) inverter at 25°C and 200°C. Both an increasing sweep '^' and decreasing sweep 'v' are performed for each case. The switching voltage is close to 10V and no difference is observed for the different geometry or temperatures.

with readout electronics and potentially even larger systems, that can have application in these harsher environments. Future work on analog circuits and integrated systems will further reveal the capabilities and limitations of integrated SiC sensors and electronics.

IV. Conclusions

We presented resistive and CMOS temperature sensors in a 4H-SiC 6µm CMOS technology. The resistive sensors consist of polysilicon, n++ doped and p++ doped design layers, of which the p++ doped layer showed the largest change in resistance of 79% over a range of 25-200°C. Due to higher ionization energies in hexagonal crystal structures with respect to cubic ones such as silicon, the resistive sensors have negative TCR and non-linear responses.

Furthermore, a five-transistor CTAT was implemented in CMOS and characterized for different external bias currents. The device showed a maximum sensitivity of -7.5mV/K for a bias current of 1µA and linear behavior over a temperature range of 25-165°C, which is an improvement by a factor two with respect to previous results in this technology.

Finally, the response of two different sized inverters is reported as preliminary investigation of the effect of temperature on readout electronics. No effect in the DC analysis was observed, which indicates negligible change of behavior of low frequency digital electronics. Future work on the effect of temperature on the readout electronics will further reveal the capability of integrated SiC systems for application in high temperature environments.

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