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Wafer Level Through Polymer Optical Vias (TPOV) Enabling High Throughput of Optical Windows Manufacturing

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Abstract—This article shows the fabrication process and packaging of through polymer optical vias (TPOV). The TPOV enables encapsulation and packaging of silicon photonic systems using film assisted molding (FAM) and the creation of micron-sized through polymer optical vias. The optical vias are lithographically defined in thick film photo-resist ($\sim 300 \mu\text{m}$) and parallel processed on substrate level. Placing and connecting optical windows on individual chips using pick & place is a difficult and time-consuming process because of the stringent requirements on alignment accuracy, cost and throughput. In this work we provide a solution to this problem by combining microfabrication technology with back-end film assisted molding technology for a new packaging approach for the integration of optical windows. As feasibility study we show through polymer optical windows on optical encoder Si photodiode arrays. The resulting microstructures are transparent in the spectrum of interest and hence serve as optical windows towards the substrate. Furthermore, our results show that the high aspect ratio (5:1) micro structure windows can be achieved and protected using FAM-technology. The optical through package windows are accurately defined ($\pm 5 \mu\text{m}$ accuracy due to mask limitations) and can significantly improve the throughput. The total process time of a single wafer with up to 1260 chips and 20160 windows, including lamination, exposure and development, would approximately take 1-1.5 hours.

Keywords—*wafer level packaging, through polymer optical vias(TPOV), micro optical windows*

I. INTRODUCTION

Optoelectronic devices have attracted extensive attention thanks to the spectrum distinguishability, photoelectric conversion feasibility and high transferring speed of photons which enable important applications such as light-emitting diodes, organic electroluminescent diodes and optical detectors

[1-3]. Integrated circuits with optoelectronics require light signals to reach the chip through the package. However, the conventional way of placing and connecting optical windows on individual chips using pick & place is a difficult and time-consuming process. It hampers and limits the maximum throughput of sequential assembly systems using visual alignment technology [4-5]. Additionally, the packaging process of optoelectronics devices requires high accuracy placement of the optical pathways ($\pm 5 \mu\text{m}$), high throughput and low cost. Henceforth, massive parallel process technologies for creating optical windows on chip level is important for the advancement of optical functional device fabrication.

A technology suitable for large-areas fabrication of miniaturized windows in customized shapes and formats at low cost is preferred in industrial chip manufacturing processes. Materials which can be defined by standard lithographic processes and which can create high-aspect ratio optically transparent structures are extremely suitable for massive parallel fabrication of windows. Moreover, it gives the possibility of changing the physical and chemical properties by material modifications to the polymers such as SU8 and SU8-based materials such as SU8 TDFS [6-7].

In this paper, we have successfully fabricated thick optical windows on wafer level using through polymer optical vias (TPOV) which are lithographically defined in optically transparent thick-film photo-resist (SU8/SU8) with thickness/heights of about $300 \mu\text{m}$, and aspect ratios of 5:1. iC-Haus optical Encoder ICs were used as the photodiode array substrate to demonstrate the technology on commercially available devices. In addition, measurements of the transmittance of SU8 ($160 \mu\text{m}$ thick) on quartz ($550 \mu\text{m}$ thick) is characterized in the wavelength range of $\lambda = 700 \rightarrow 1200 \text{ nm}$, as function of temperature. The objective was to study the

effects of soldering reflow at 260°C which can cause yellowing of the window material.

The remainder of the paper is organized in six sections as follows. In section II, we describe the silicon/MEMS microfabrication technology combined with back-end film assisted molding technology. In section III, the fabrication flowchart is discussed. Section IV, discusses the measurement and characterization of the SU8 optical properties. The results and discussion will be given at section V. The conclusions are provided in section VI.

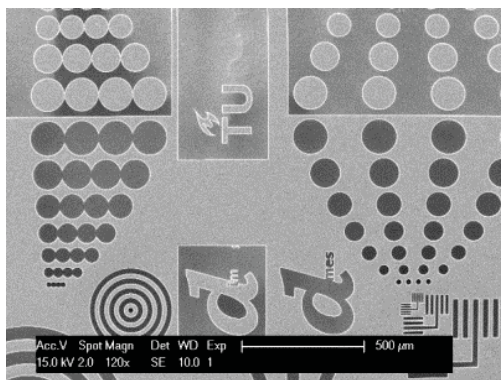
II. APPROACH AND PRELIMINARY RESULTS

A. MEMS Microfabrication Technology

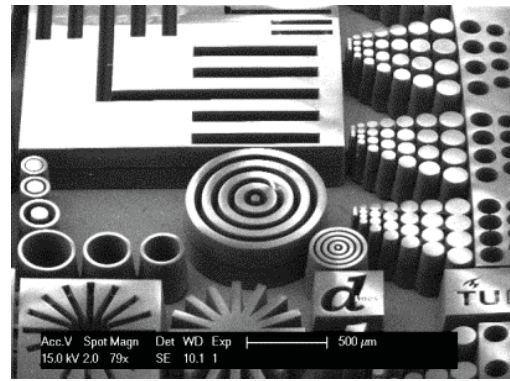
Silicon/MEMS microfabrication technology such as front-end lithography allows for accurate and precise patterning of micro and nanostructures on substrates such as silicon wafers. Combining both front-end microfabrication technology with back-end film assisted molding technology allows for a new packaging approach for integration of optical windows.

- The first step consists of applying a thick layer (in the range of 300 μm) of negative photo-sensitive film on a substrate.
- In the second step we perform lithographic exposure of the negative photoresist using an industry standard MA6 contact aligner with an overlay alignment accuracy of $< 5 \mu\text{m}$.
- Then we perform a development step which removes the unexposed photoresist.
- The final step is the encapsulation using film assisted molding (FAM) and clamping on the high-aspect ratio microstructures.

The fabrication is a parallel process and all microstructures are realized in the same step, this in contrast with pick and place methods. The microstructures can be designed as high-aspect-ratio window-like structures, which can be placed directly on the photodiode arrays in any shape or format. Fig. 1 shows an example SEM image of patterned microstructures.



(a)



(b)

Fig. 1. (a) Top-view of the microstructures defined on a substrate. The microstructures consist of holes and pillars of different diameters and pitch. (b) Tilted side-view showing the high aspect ratio of the microstructures.

After fabrication of the microstructures we encapsulate and package the photonic substrate using film assisted molding (FAM) [8-10]. Using FAM, we clamp and press the microstructures partly into the film. Fig. 2, illustrates the encapsulation process of the through polymer optical vias.

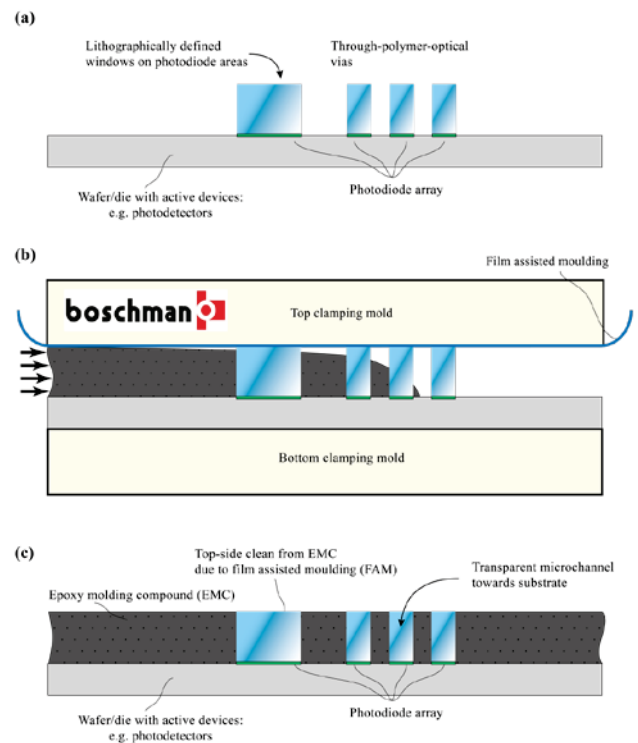


Fig. 2. (a) Cross-sectional view of the substrate and the through polymer-optical-via (TPOV) microstructures. (b) Encapsulation process showing the clamping of the vias during molding. (c) Unloading of the sample, showing the top of the via is clean from Epoxy Molding Compounds (EMC).

B. Proposed Process Flow

We show the concept-art of through polymer optical vias for the iC-Haus device in Fig. 3.

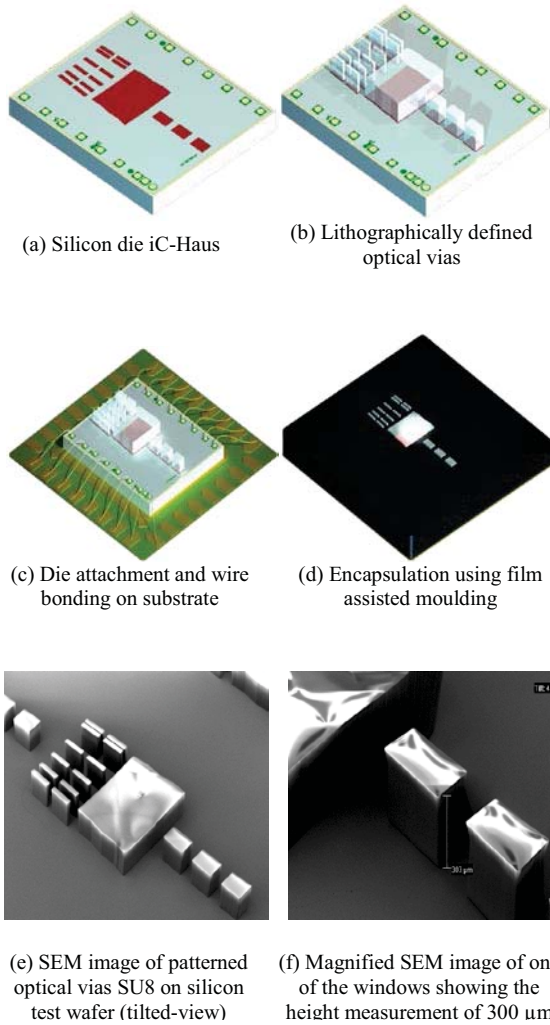


Fig. 3. Process flow and preliminary results for the fabrication and packaging of a photonic substrate with through polymer optical vias. In the SEM images some charging effects of the polymer are visible.

III. FABRICATION OF TEST SAMPLES

The fabrication of through polymer optical vias was accomplished by a lithographic process on laminated SUEX epoxy thick film sheets (TDFS). In order to keep the backside of chip tiles clean and not contaminate the hotplate surface with melted polymer, a clean 6 inches Si substrate wafer was used on the hotplate as a carrier holder. iC-Haus wafers containing chips with optical encoders were diced into multiple 20.16 mm × 20.22 mm tiles, this allows us to run several process variations. We used 48 mm × 48 mm × 350 μm SEUX TDFS as dry film photo resist laminate material for creating the optical opening windows.

The SUEX dry film was laminated on the tiles on a hotplate set at 75°C by rolling. To minimize bubble formation, we increased the temperature of the hotplate up to 85°C. This was

followed by a pre-exposure soft baking for 3 mins at 85°C to improve adhesion. Slow cooling is required to prevent thermal shock. After pre-exposure bake, exposure was performed on a MA6 Contact Aligner for 400 s (10mWatt/cm) in hard contact mode. Post exposure bake is performed for 5 mins at 65°C and 10 mins at 95°C to make negative photo resist crosslink. At last, MicroChen's PGMEA (propylene glycol methyl ether acetate) are used at room temperature to develop in about 15 mins. Acetone is used to clean residual unexposed resist and developer. Exposure to acetone should be minimized to prevent attack of the optical film. Rinse wafers in IPA and dry in air.

In order to improve adhesion between the polymer vias and photodiodes surface, there are three methods. At first, pre-exposure soft baking is recommended for at least 2 mins to let the dry film resist have enough time to reflow and laminated on substrate. Secondly, the key point is to dramatically increase exposure energy to at least 400 s (power density for MA6 we used is 10 mWatt/cm² in the middle and 10 ± 0.5 mWatt/cm² in the outer area) for 300 μm thickness polymer vias. Light is absorbed when it is trying to pass through thick layers of resist which can result in the lack of exposure at the bottom layer of negative photoresist. If the bottom/adhesion layer of the photoresist is not exposed completely it will be easily removed in developing solution. At last, development time should be carefully monitored to prevent under-etch at the bottom. Fig. 4 shows the cross-section of a process flowchart.

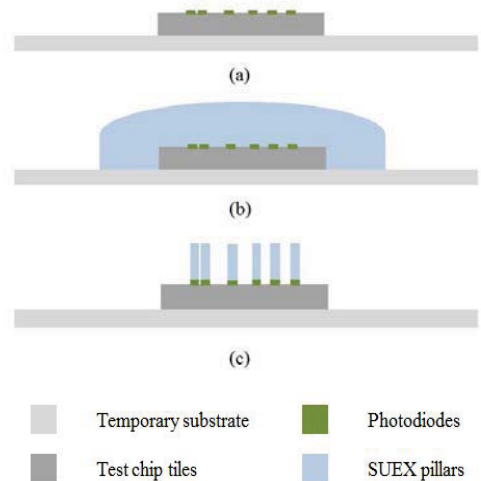


Fig. 4. process flow of fabricating optical opening windows by SUEX. (a) Chip tiles on clean DSP(double side polished) Si wafer. (b) Laminate SUEX on single chip tile. (c) Through polymer optical vias built on photodiodes after standard lithographic process.

The optical windows are accurately aligned with respect to the die, as can be seen in Fig. 5. Even the smallest window features are covering the photodiodes. Moreover, the high-aspect ratio structures allow for close proximity to each other. The minimal space between two microstructures in our test is approximately 50 μm. Fig. 6 shows that patterned microstructures on an iC-Haus tile survived after molding.

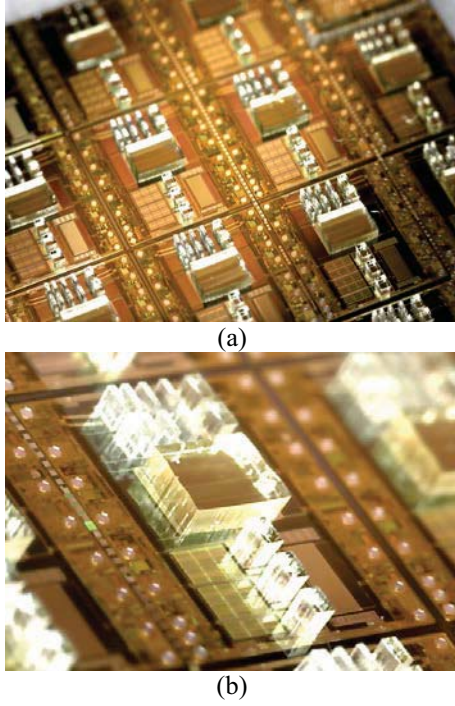


Fig. 5. Optical image (tilted-view) of the patterned microstructures on an iC-Haus tile showing the optical clarity. (a) Chip arrays on tile. (b) Single chip with patterned microstructures.

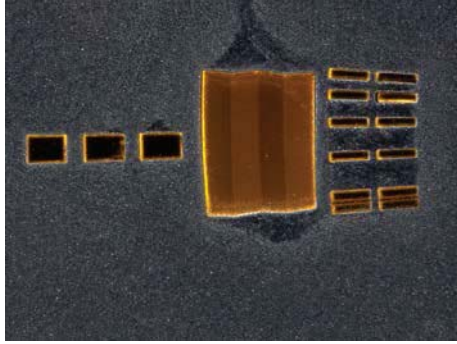


Fig. 6. Optical image of the patterned microstructures on an iC-Haus tile after molding.

IV. EXPERIMENTAL SETUP

The iC-Haus sensor package requires high temperature stability during 3 consecutive solder reflow steps of 260°C for 3 mins each, as can be seen in Fig. 7. The TPOV is patterned onto the photodiode array and is based on a negative thick film photoresist. During the reflow step yellowing of the TPOV can occur.

To characterize the influence of temperature and the yellowing of the photoresist we measure the optical performance in terms of transmission for different wavelengths and for different baking times. The transmission is measured using a Perkin Elmer Lambda 950 UV-Visible spectrophotometer. The spectrum is scanned with 5 nm

increments from $\lambda = 320 \text{ nm} \rightarrow 1500 \text{ nm}$. The spectrophotometer needs a relatively large sample for measurement. Therefore, we coated a 710 μm thick quartz wafer with 160 μm thick SU8. The wafer was diced in 4 tiles of 20 \times 20 mm and labelled with A, B, C and D.

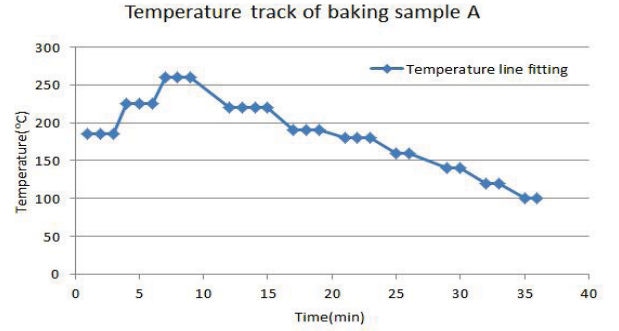


Fig. 7. Hotplate temperature profile used for baking the thick film photoresist Sample A. Samples B, C and D were exposed for 9 mins at 260°C. The total time above 180°C is more than 15 mins.

V. RESULTS AND DISCUSSION

The results in Fig. 8 show the transmission measurements of the 710 μm thick quartz wafer with 160 μm thick SU8. Samples were baked at 260°C for more than 9 mins. We set the hotplate temperature at 15°C above 260°C to correct for the contact resistance and the temperature gradient through the wafer. The first observation is that large un-patterned films of SU8 delaminate from the quartz wafer due to thermal shock. However, this allowed us to test SU8 films without substrate. Below $\lambda = 600 \text{ nm}$, we observe strong adsorption of the incident light after baking.

The transmission measurements are summarized in Table 1 for comparison. The results show that the average transmittance of SU8 films after baking at 260°C remains stable at about 91% in the wavelengths ranging from $\lambda = 700 \text{ nm} \rightarrow 1200 \text{ nm}$. This indicates that roughly 9% of the incoming light is reflected or absorbed at these wavelengths.

The visual inspection of the samples after baking shows that yellowing is present.

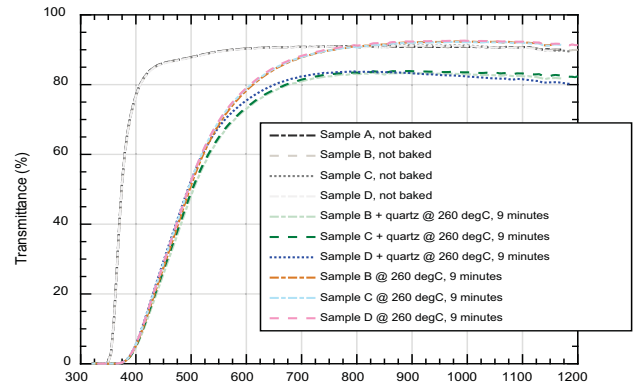


Fig. 8. Transmission measurement of the thick film photo resist (SU8) on a quartz substrate.

TABLE I. AVERAGE SU8 (ON QUARTZ) TRANSMITTANCE MEASUREMENT BETWEEN $\lambda = 740 \text{ nm} \rightarrow 980 \text{ nm}$.

	Sample A	Sample B	Sample C	Sample D
SU8 thickness (μm)	172	164	163	164
Quartz thickness (μm)	710	710	710	710
Reference transmittance ^a	90.9%	90.9%	91.1%	90.9%
Baking time (min)	3+	9++	9++	9++
Post-bake transmittance	83.2%	83.1%	83.6%	83.3%
SU8 only ^b	92.0%	91.5%	91.4%	91.8%

^a Reference transmittance is the SU8 on quartz transmission before the baking step.
^b The transmittance of SU8 after peeling off from the quartz substrate.

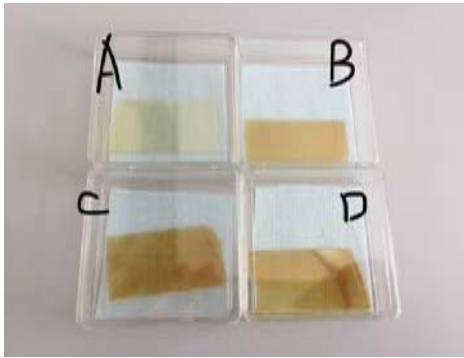


Fig. 9. Optical photograph of the different samples (A, B, C and D) after baking at 260°C .

VI. CONCLUSION

In conclusion, we have successfully fabricated through polymer optical vias (TPOV) in aspect ratio of 5:1. Patterned optical windows were fabricated within $5 \mu\text{m}$ micron alignment accuracy covering and protecting the photodiode arrays while allowing the light in wavelength range of $\lambda = 740 \rightarrow 980 \text{ nm}$ to pass through it. The average SU8 (on quartz) transmittance has been measured at the same wavelength range after extra baking on a hotplate to simulate the soldering step at 260°C which can cause yellowing of the material. The results show that the average transmittance of SU8 films after baking at 260°C remains stable at about 91% in the wavelength ranging from $\lambda = 700 \rightarrow 1200 \text{ nm}$.

Combining both microfabrication technology with back-end film assisted molding technology allows for a new packaging approach for integration of optical windows. The method is suitable for high-throughput manufacturing because it is a parallel process and all microstructures are realized in the same step.

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REFERENCES

- [1] E. F. Schubert, *Light-Emitting Diodes*, 3rd ed., Cambridge, U.K.: Cambridge Univ. Press, 2018.
- [2] C. W. Tang and S. A. Vanslyke, *Organic Electroluminescent Diodes*, *Applied physics letters*, 1987, pp.51-913.
- [3] K. J. Baeg, M. Binda, D. Natali, M. Caironi, Y. Y. Noh, *Organic Light Detectors: Photodiodes and Phototransistors*, *Advanced Materials*, 2013, pp. 4267–4295.
- [4] A. Mahapatra and R. Mansfield. *Optoelectronic Packaging Using Passive Optical Coupling*, in *Optoelectronics Packaging and MOEMS Topical Workshop, IMAPS, Bethlehem, PA, 2002*.
- [5] G. Lecarpentier, J. Mottet, J. Dumas, "High accuracy machine automated assembly for opto electronics," *IEEE 50th Electronic Components and Technology Conference, Las Vegas, NV, USA, May 2000*.
- [6] R. Walczak, P. Sniadek and J. A. Dziuban, SU-8 photoresist as material of optical passive components integrated with analytical microsystems for real-time polymerase chain reaction, *Optica Applicata* 2011, 41 (4), pp. 873–884.
- [7] D. Johnson et al.; SUEX Process Optimization for Ultra Thick High Aspect Ratio LIGA Imaging; *Proc. SPIE*, Vol. 7872(2011), 79722U.
- [8] D. W. Johnson, G. Ahrens and A. Vogt, KM661 Thick Epoxy Sheets for MEMS and Packaging Applications, *Commercialization of Micro and Nano Systems 2009, Copenhagen, Sept 2, 2009*.
- [9] W. Lingen, A. Bos, T. van Weelden, and F. Boschman. The next generation advanced MEMS and sensor packaging. in *Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on. 2010*. J. Clerk Maxwell, *A Treatise on Electricity and Magnetism*, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.
- [10] R. H. Poelma, H. W. Van Zeijl, and G. Q. Zhang, Through-polymer via (TPV) and method to manufacture such a via, in WO 2014107108 (A1), U.D. TECH[NL], Editor. 2014: Netherlands. p. 16.
- [11] M. Kengen, R. H. Poelma, H. W. van Zeijl, A. van Weelden, E. Boschman. Through-polymer-via for 3D heterogeneous integration and packaging. in *Minapad Forum, Grenoble, France, 2015*.