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A Low Power Continuous-Time Zoom ADC for Audio Applications

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Abstract

This paper presents a continuous-time (CT) zoom ADC for use in audio applications. Compared to previous zoom ADCs, its input impedance is mainly resistive, making it much easier to drive while still maintaining high energy efficiency. The prototype is fabricated in a 0.16 µm CMOS process, occupies 0.27 mm^2 and achieves 108.5 dB DR, 108.1 dB SNR, 106.4 dB SNDR in a 20 kHz BW, while consuming 618 µW. This results in a state-of-the-art Schreier FoM of 183.6 dB.

Introduction

ADCs intended for use in audio CODECs of battery powered devices must achieve high resolution and energy efficiency. These requirements can be met by discrete-time zoom ADCs [1,2]. However, their switched-capacitor input circuits draw high peak currents, which must be supplied by their input and reference drivers. Although CT ADCs do not have this problem, their SNR is typically limited to less than 100 dB in audio applications [3-5]. This paper describes an easy-to-drive CT zoom ADC with 108.1 dB SNR.

Continuous-Time Zoom ADC

The proposed CT zoom ADC is shown in Fig. 1. It consists of an N-bit coarse asynchronous SAR ADC and a 1-bit fine CTDSM, which operate concurrently. The coarse ADC's output (k) satisfies $k \cdot V_{LSB,C} < V_{in} < (k+1) \cdot V_{LSB,C}$ where $V_{LSB,C}$ is the coarse quantization step, or least-significant bit (LSB). The references of the 1-bit CTDSM are then adjusted such that $V_{ref+} = (k+1+M) \cdot V_{LSB,C}$ and $V_{ref-} = (k-M) \cdot V_{LSB,C}$ where M is an over-ranging factor that ensures robustness to SAR ADC errors and delay. In this design, the speed of an asynchronous SAR ADC is optimally leveraged to allow M=1, compared to M=2 in [1]. This reduces the peak output current of OTA_1 by ~2×, dramatically relaxing its linearity requirements.

Fig. 2 shows a simplified schematic of the ADC, which is sampled at F_S=5.12MHz. For improved phase margin at F_S, active-RC integrators with resistors (R_{z1-3}) are employed. The input resistors (R_i=10kΩ) define the ADC's thermal noise, and are sized to ensure that self-heating-induced distortion is below -120 dB. A series resistor (R_{ser}=20kΩ) and a small sampling capacitance (55fF), ensure that the SAR ADC's dynamic input impedance is comparatively high. Capacitors C_{ff1-3} implement a feed-forward compensation scheme. A 31-level NRZ R-DAC with DWA is used for low 1/f noise, low power and high linearity. Relatively large resistors (R_{i2-3} =3.45MΩ) and small capacitors (C_{int2}=220fF, C_{int3}=150fF) minimize both the loading of OTA_{2-3}, and their area. A fixed loop delay of $1/8F_S$ accommodates the delay of both the comparator and the DWA logic. For robustness to process variations, the loop filter capacitors are tunable (±15%).

In terms of noise and linearity, OTA_1 (Fig. 3) is the most critical active circuit block. It employs a pseudo-differential topology, whose linearity and swing is improved by the absence of tail current sources [6]. To mitigate its 1/f noise, it is chopped at F_S. Via C_C (=2pF), the chopped input signal is AC coupled to the gates of the N/PMOS input pairs. These are biased at constant gm via large resistors (R_b=3MΩ), thus ensuring that the coupling network's cut-off frequency is well below F_S. The amplified output is then down-modulated at the sources of the output cascodes. Since the bandwidth at these nodes is much greater than F_S, the gain reduction due to chopping is negligible. CMFB regulation is achieved via an auxiliary NMOS input pair. The DC gain of OTA_1 is 60 dB, and due to the use of chopping, its 50Hz CMRR and PSRR exceed 70 dB and 100 dB, respectively. OTA_{2-3} are current-starved inverters as in [1], and consume 12 times less power than OTA_1.

Dynamic errors related to the transitions of an NRZ DAC, e.g. the mismatched rise/fall times of its unit currents, will cause inter-symbol interference (ISI). This, in turn, causes even-order distortion and quantization noise fold-back. DWA increases the unit transition rate, and actually worsens ISI by more than an order of magnitude, according to simulations.

In this work, a differential R-DAC is proposed to reduce the even-order distortion caused by ISI. As shown in Fig. 4, each differential unit can have four different rise/fall times: t_{rp}, t_{rn}, t_{fp}, and t_{fn}. The key observation is that ISI can be cancelled by matching the rising and falling edges of the positive and negative DAC units, i.e. by ensuring that $t_{rp} = t_{rn}$, and $t_{fp} = t_{fn}$. This is mainly determined by the mismatch of the DAC unit resistors R_{up} and R_{un}, and is designed to be quite low (< 1%) in order to meet the target SNDR. Since the on-resistance of the driving inverters is much less than R_u, their mismatch can be neglected. Two flip-flops are used for the positive and the negative halves of each DAC unit. These halves, including the driving inverters and flip-flops, are placed next to each other to improve their matching. The mismatch between the ISI error of different DAC units is shaped by DWA.

Measurement Results

The prototype CT zoom ADC, shown in Fig. 5, has been realized in a 0.16µm CMOS technology. It occupies an area of 0.27 mm^2. The ADC consumes 618 µW from a 1.8 V supply; the analog, DAC, clock and digital circuits consume 45%, 28%, 13% and 14%, respectively.

The measured peak SNR, SNDR and DR are 108.1 dB, 106.5 dB and 108.5 dB, respectively (Fig. 6). The measured output spectrum of the ADC is shown in Fig. 7. Peak SNDR is achieved with a -0.15 dBFS input signal, with HD_3 being the dominant distortion component at -113 dB, whereas the other harmonic components are below -120 dB. Fig. 8 shows HD_2 and HD_3 performance as the input frequency is swept from 10Hz to 20kHz. As expected, the shaped quantization noise becomes dominant outside this band. The coarse SAR ADC still requires an anti-aliasing filter. With an external RC low-pass filter (R_{ser}=20kΩ, C_{filt}=5pF), the measured alias rejection of the overall ADC around F_S is greater than -72 dB for -6 dBFS signals (Fig. 9). In Table I, the ADC's performance is summarized and compared to the state-of-the-art. Despite being implemented in a relatively mature process, it achieves a $FoM_{S,DR}$ of 183.6 dB and $FoM_{S,SNDR}$ of 181.5 dB, which both correspond to state of the art energy efficiency.

References

[1] B. Gönen, *et al.*, *JSSC*, Jun. 2017 [2] S. Karmakar, *et al.*, *ISSCC*, 2017 [3] C. Lee, *et al.*, *VLSI*, 2018 [4] S. Billa, *et al.*, *ISSCC*, 2017 [5] C. Berti, *et al.*, *JSSC*, Jul. 2016 [6] M. S. Akter, *et al.*, *JSSC*, Oct. 2018. [7] B. Wang, *et al.*, *VLSI*, 2018

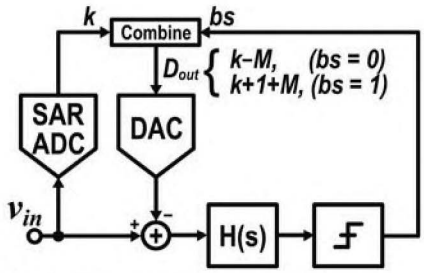

Fig. 1. Proposed CT zoom ADC.

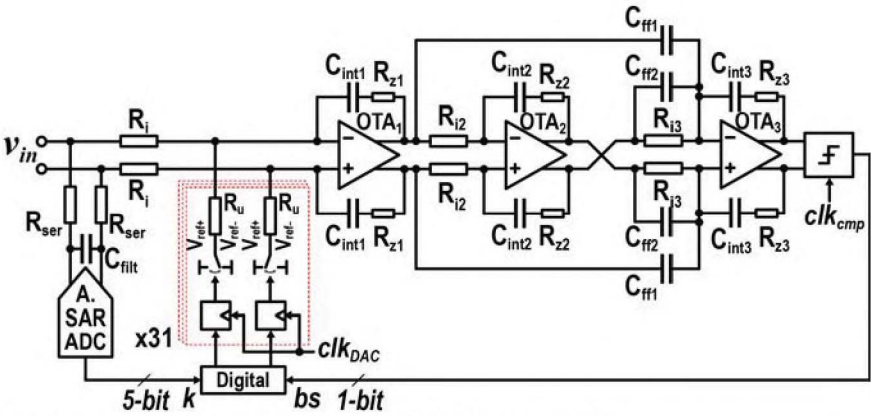

Fig. 2. Simplified schematic of the proposed CT zoom ADC.

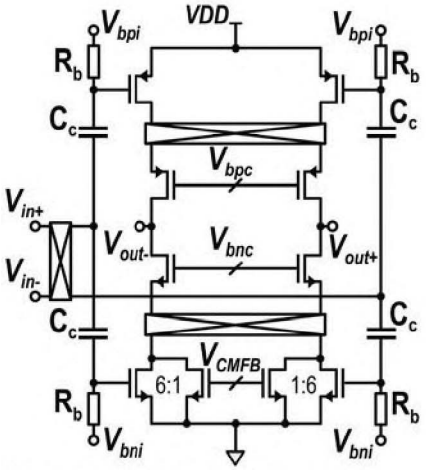

Fig. 3. Simplified schematic of OTA_1.

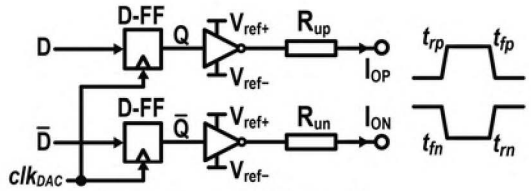

Fig. 4. Schematic of a R-DAC cell.

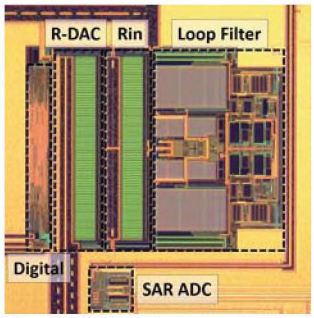

Fig. 5. Chip micrograph.

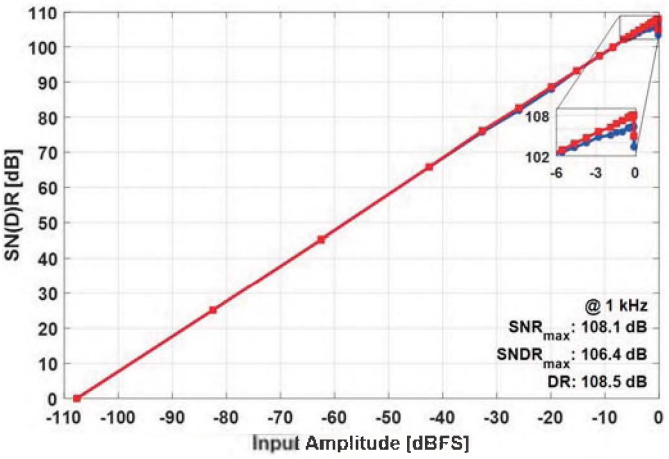

Fig. 6. Measured SNR and SNDR across input amplitude.

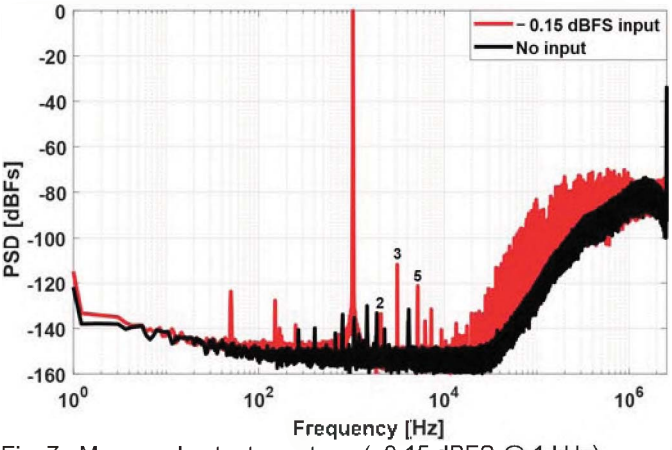

Fig. 7. Measured output spectrum (−0.15 dBFS @ 1 kHz)

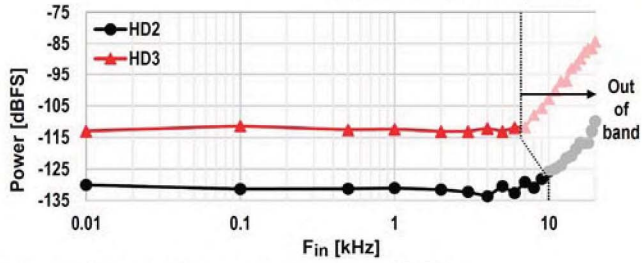

Fig. 8. HD_2 and HD_3 vs F_{in} (Input: -1 dBFS)

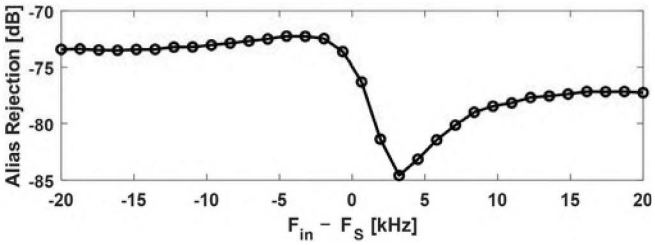

Fig. 9. Alias rejection of the CT zoom ADC (Input: -6 dBFS)

Table I. Performance summary and comparison

	This work	Lee *VLSI'18* [3]	Wang *VLSI'18* [7]	Karmakar *ISSCC'18* [2]	Gönen *JSSC'17* [1]	Billa *ISSCC'17* [4]	Berti *JSSC'16* [5]
Architecture	**CT Zoom**	CT 3-Level	DT Incremental	DT Zoom	DT Zoom	CT FIRDAC	CT Multi-Bit
Tech (nm)	**160**	65	65	160	160	180	160
Area (mm^2)	**0.27**	0.14	0.134	0.25	0.16	1	0.21
Supply (V)	**1.8**	1.2	1.2	1.8	1.8	1.8	1.6
Power (μW)	**618**	68	550	280	1120	280	390
F_S (MHz)	**5.12**	6.144	10.24	2	11.3	6.144	3
BW (kHz)	**20**	24	20	1	20	24	20
SNR (dB)	**108.1**	94.8	N/A	119.1	106	99.3	93.4
SNDR (dB)	**106.4**	94.1	100.8	118.1	103	98.5	91.3
DR (dB)	**108.5**	98.2	101.8	120.3	109	103.6	103.1
$FoM_{S,SNDR}$[+] (dB)	**181.5**	179.5	176.4	183.6	175.5	177.8	170.5
$FoM_{S,DR}$[++] (dB)	**183.6**	183.6	177.4	185.8	181.5	182.9	180.2

[+] $FoM_{S,SNDR}$ = SNDR + 10log(BW/Power) [++] $FoM_{S,DR}$ = DR + 10log(BW/Power)