TOTAL HARMONICS DISTORTION (THD) REDUCTION TECHNIQUES IN CLASS D AMPLIFIERS

by

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ABSTRACT

Class D amplifiers find widespread application in audio devices for driving load speakers, primarily due to their remarkable efficiency. Nonetheless, this enhanced efficiency often comes at the expense of reduced linearity. Hence, techniques for reducing Total Harmonic Distortion (THD) are important in the context of class D amplifiers.

The analysis of the distortion mechanisms is first presented. Specifically, emphasis is placed on the distortion generated within the power stage, encompassing aspects such as deadtime distortion and rising and falling time distortion. Both of them are found to be related to the input signal. Subsequently, the compensation technique is applied to the conventional class D amplifier to reproduce and cancel the error. The idea of the compensation approach involves modifying the amplitude of the triangular waveform based on the input signal. A 12 dB THD improvement is achieved in the concept verification section, which is conducted in LTspice.

The negative feedback serves as another technique to achieve THD reduction. A straightforward two-step design methodology is presented to avoid design iterations in the concept design phase. The phantom zero technique is applied when doing the frequency compensation of the feedback loop. The validation of the concept is performed through the use of SLICAP, while the circuit implementation and simulations are carried out within Cadence. Remarkably, this technique results in an impressive $-111.8\ dB$ THD reduction, achieved when the output power equals $1\ W$.

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INTRODUCTION

A class D amplifier is a switching amplifier that operates by modulating the high-frequency carrier signal with the input signal to generate a pulse width modulated (PWM) signal, which is then amplified using a power stage consisting of a series of MOSFETs [1–8]. The output signal is reconstructed from the amplified PWM signal by passing it through a low-pass filter that removes the high-frequency carrier signal and leaves behind the amplified input signal.

A conventional PWM-based class D amplifier is shown in Figure 1.1.

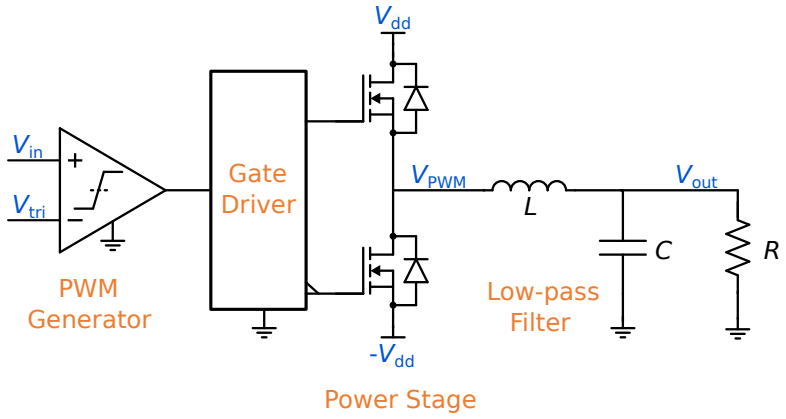

Figure 1.1: Conventional PWM-based class D amplifier.

The PWM signal is generated by comparing the input signal with a high-frequency triangular waveform. The duty cycle of the PWM signal is proportional to the amplitude of the input signal. For example, if the input signal is a sine wave, the PWM signal will have a duty cycle that varies sinusoidally.

The gate drivers are responsible for controlling the switching behavior of the power switches. Without gate drivers, the PWM signal from the previous stage may not be sufficient to properly drive the power MOSFETs which have high input capacitance, leading to slow switching speeds, increased power losses, and reduced efficiency. In addition,

gate drivers also include level shifters to convert the PWM signal levels to the appropriate gate voltage levels required by the power MOSFETs.

Ideally, the PWM waveform at the output of the power stage would be a square-like waveform. After the low-pass filter, the amplified signal is extracted at the output. However, in practice, there are several non-idealities that affect the performance of class D amplifiers, which will be explained in detail in the following chapter.

1.1. PROBLEM STATEMENT

Class D amplifiers find widespread application in audio devices for driving load speakers, primarily due to their remarkable efficiency. Nonetheless, this enhanced efficiency often comes at the expense of reduced linearity. Hence, techniques for reducing Total Harmonic Distortion (THD) are important in the context of class D amplifiers.

The genesis of distortion can be attributed to various sections of the class D amplifier, spanning from the PWM generator and power stage to even the LC filter. Discerning the dominant contributors as well as identifying elements with a comparatively minor impact is indispensable for effective pre-design considerations.

1.2. OBJECTIVES

SystematIC B.V. has established specific target specifications, which are itemized in Table 1.1.

Table 1.1: Target specifications

Specification	**Target**
Switching frequency	1.2MHz
Supply voltage	24V
Load	BTL 8Ω
THD (1kHz, 1W)	<-90dB
Max output power (1kHz, 10%THD)	30W

1.3. THESIS ORGANIZATION

This thesis includes totally five chapters.

In Chapter 2, the distortion mechanisms mainly in the power stage of the class D amplifier are discussed. Both the deadtime distortion and rising and falling time distortion are proven to be related to the input signal.

In Chapter 3, the compensation technique is applied to reduce THD. The theoretical calculation of the reproduced error builds upon the analysis in Chapter 2 and the idea of the compensation approach revolves around reproducing the identified error through the utilization of the modified triangular waveform.

In Chapter 4, the feedback technique is implemented to achieve THD reduction. The conceptual design phase employs a straightforward two-step methodology derived from Structure Electronic Design [9], avoiding design iterations. An essential element is the incorporation of the phantom zero technique, serving to stabilize the feedback loop and yield a more linear transfer function response. The circuit implementation and simulation results are also included in this chapter.

This thesis integrates simulations conducted in Cadence with the utilization of SLICAP (Symbolic Linear Circuit Analysis Program). SLICAP primarily serves as a tool for conceptual design, offering capabilities to analyze Laplace transfer functions and frequency response of the circuit [10]. The design of the circuit and verification is finished with Cadence.

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2

DISTORTION MECHANISMS

2.1. INTRODUCTION

The ideal PWM waveform after the power stage should be a square-like waveform. In reality, the waveform is subject to non-idealities that cause distortion in the output signal.

One of the non-idealities that affects the performance of Class-D amplifiers is the "deadtime" [1–4], which is the interval between turning off one power switch and turning on the next switch. The deadtime is necessary to prevent shoot-through current, which occurs when both switches are turned on simultaneously, causing a short circuit across the power supply. However, the deadtime can also lead to additional distortion.

Another source of non-idealities in Class-D amplifiers is the finite switching time of the power switches. During the switching transition, the switches have a limited time to turn on and off, which results in switching losses and distortion in the output signal. The literature on this specific topic is currently limited, as it is not considered a significant contributor to THD. However, in this chapter, the author discovers that the rising and falling time distortion is dependent on the input value, the results of which can be used for the error analysis in Chapter 3.

The impact of the on-resistance of the power MOSFETs can be also noticed from the actual waveform at V_{PWM} node. The V_{PWM} signal will exhibit characteristics similar to amplitude modulation, where variations in the high and low voltage levels at the V_{PWM} node are determined by the product of the current and on-resistance. Despite this effect, prior research [5] has shown that the on-resistance of the power MOSFETs has minimal impact on the total harmonic distortion.

Other non-idealities that affect the performance of Class-D amplifiers include nonlinearity in the triangular waveform signal [2, 5, 6] and delay in the comparator. However, these factors cannot be easily observed in the waveform of the power stage but rather exist in other circuit modules. Quantifying the impact of these non-idealities on the THD at the output node requires a comprehensive and rigorous analysis. Therefore, this chapter focuses primarily on analyzing deadtime distortion and rising and falling time distortion.

2.2. DEADTIME DISTORTION

To ensure that only one transistor is turned on at the same time in the power stage, a small period of "deadtime" needs to be added, as shown in Figure 2.1. The rising edges of the gate driving voltage are subjected to a time delay T_D while the falling edges remain unchanged.

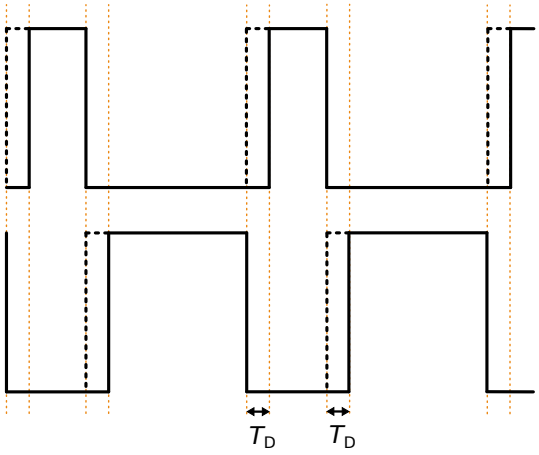
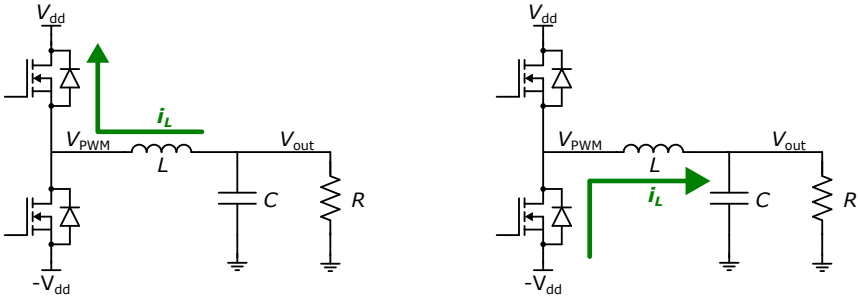


Figure 2.1: Deadtime in PWM signal.

During the deadtime, two transistors in the power stage are both turned off. However, the inductor in the low-pass filter is inclined to maintain its last state, which means there is still current flowing in the inductor.

Typically, n-type power MOSFET is applied in the power stage, with bulk and source connected with each other. The body diode from bulk to the source is then shorted while the bulk-to-drain body diode becomes the source-to-drain diode. The current in the inductor will flow through the body diode during deadtime, as shown in Figure 2.2.



(a) current flows through high-side body diode (b) current flows through low-side body diode

Figure 2.2: Current direction during deadtime.

The voltage of V_{PWM} during deadtime will depend on the direction of the current in the inductor. When the current flows from right to left, as shown in Figure 2.2a, the upper body diode is on, making V_{PWM} higher than the supply voltage by a diode forward voltage V_F; When the current flows from left to right, as shown in Figure 2.2b, the lower body diode is on, making V_{PWM} lower than the ground by a diode forward voltage V_F.

The inductor current consists of the ripple current flowing through the capacitor and the output current flowing to the load. To simplify the analysis, the ripple current is first neglected. In this case, the inductor current is equal to the output current, which represents the amplified input signal.

Hence, the exact voltage value during the deadtime can be determined by utilizing the input signal as depicted in Figure 2.3, where the gain of the amplifier from input to output is assumed to be negative. The positive current represents the current flowing into the load and the negative current flows out.

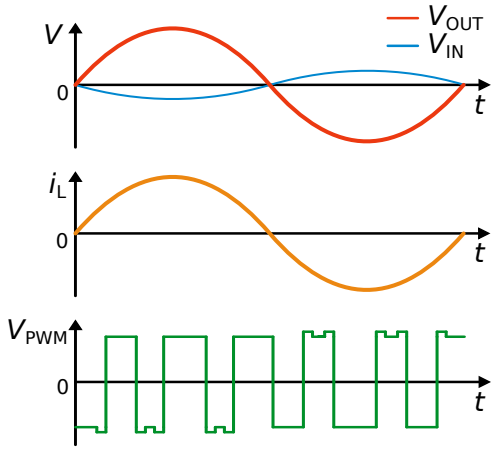


Figure 2.3: The relationship between V_{PWM} and input signal during the deadtime.

The waveform of V_{PWM} is notably distinct from a purely square waveform owing to the presence of deadtime. This divergence leads to the emergence of deadtime distortion in the output signal after the LC filter.

2.3. RISING AND FALLING TIME DISTORTION

The rising and falling of V_{PWM} can be attributed to the charging and discharging of the parasitic capacitors of power MOSFETs. To simplify the analysis, the power MOSFET is modeled with an ideal switch and capacitors, while the gate driver is modeled with an ideal source and a conducting resistor. The model is shown in Figure 2.4.

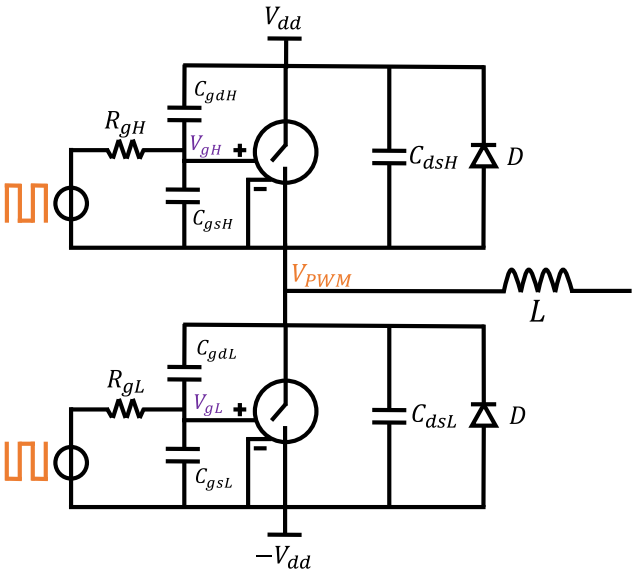


Figure 2.4: Power stage model.

The observation from Figure 2.3 reveals that when the input signal is a sinusoidal waveform, the voltage signal across each terminal and the current signal flowing through the components in the first half cycle of the class D amplifier's input exhibit symmetry with respect to the second half cycle. As a consequence, based on the magnitude relationship between the input signal and the ground signal, the working of the power state can be classified into two distinct situations:

1. $V_{in} < 0$, so that $V_{out} > 0$ and $i_L > 0$ by assuming gain is negative. The duty cycle of V_{PWM} is larger than 50% and current flows through the low-side body diode when during the deadtime;
2. $V_{in} > 0$, so that $V_{out} < 0$ and $i_L < 0$ by assuming gain is negative. The duty cycle of V_{PWM} is smaller than 50% and current flows through the high-side body diode when during the deadtime.

Figure 2.5 illustrates the variation of current in the power stage in the second situation and the subsequent analysis is based on this condition. Figure 2.6 shows the corresponding variation of V_{PWM}. The subfigures (1)-(6) in Figure 2.5 correspond to the voltage stages (1)-(6) in Figure 2.6.

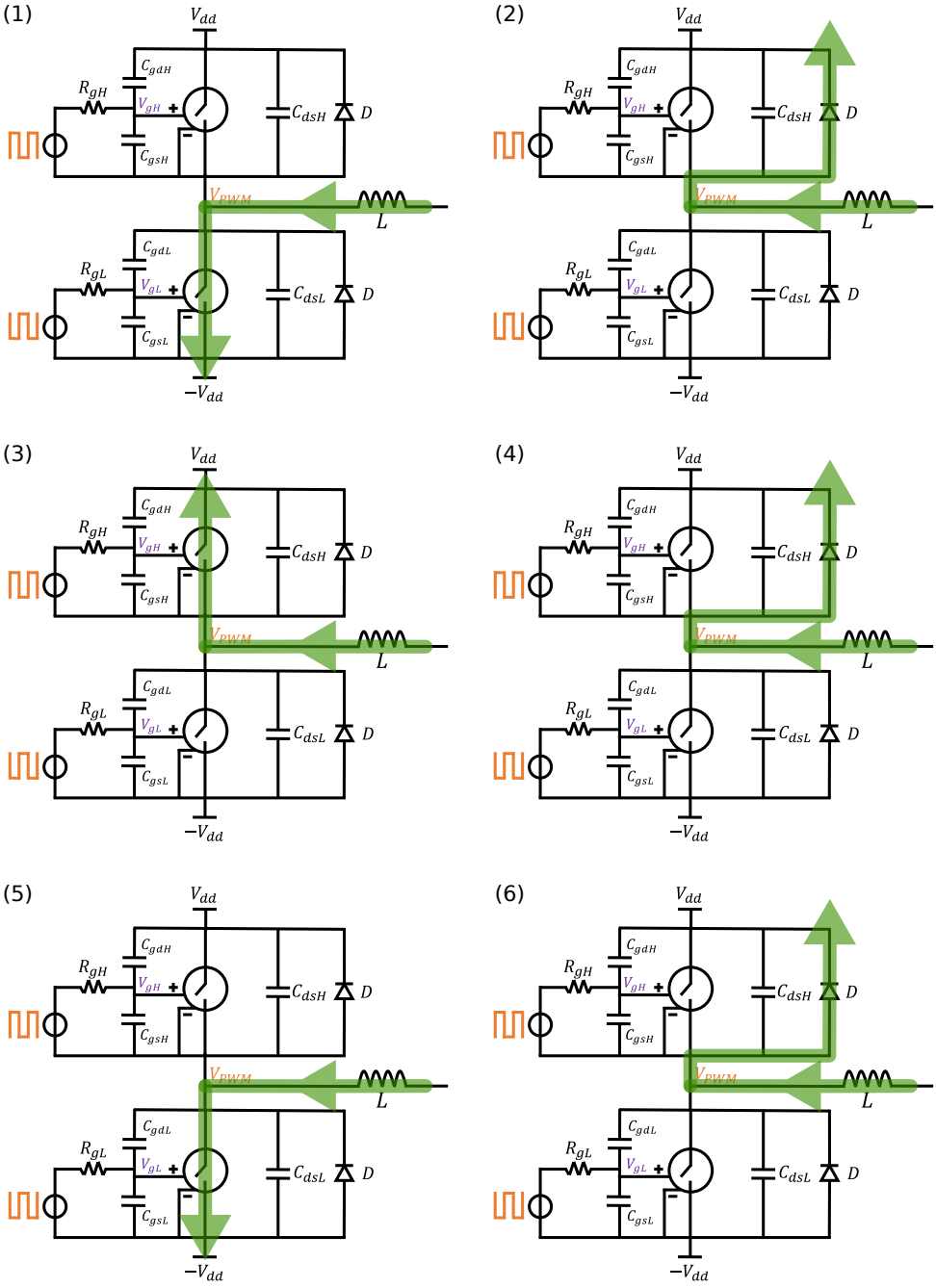


Figure 2.5: Current variation in the power stage.

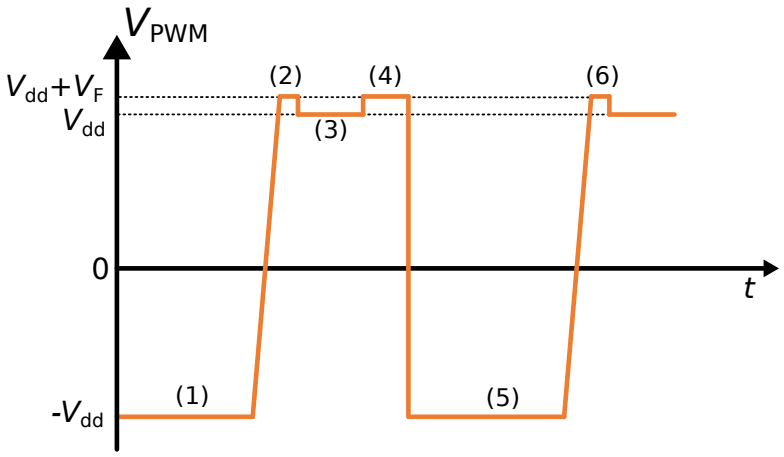


Figure 2.6: Voltage variation at V_{PWM} node during one period.

Here are the detailed explanations for each transition:

- (1)→(2). The low-side power switch is turned off, while the high-side power switch is also off due to the deadtime. Therefore, the inductor current flows through the high-side body diode, making V_{PWM} a diode forward voltage V_F higher than the positive power supply voltage V_{dd}. The PWM voltage rising happens during this transition.
- (2)→(3). The high-side power switch is turned on. The current flows through the channel of the high-side power switch and V_{PWM} equals the positive power supply voltage V_{dd} by neglecting the on-resistance.
- (3)→(4). The high-side power switch is turned off. The circuit goes into the dead-time period again. Therefore, the inductor current flows through the high-side body diode, and V_{PWM} equals $V_{dd}+V_F$.
- (4)→(5). The low-side power switch is turned on. The current flows through the channel of the low-side power switch and V_{PWM} equals the negative power supply voltage $-V_{dd}$ by neglecting the on-resistance. The PWM voltage falling happens during this transition.
- (5)→(6). The transition is the same as (1)→(2).

From stage (1) to stage (2), the voltage V_{PWM} goes up due to the parasitic capacitors of the power switches being charged, as shown in Figure 2.7.

By applying Kirchhoff's current law (KCL), ones can get

$$i_L = I_{dL} + i_{dsL} + i_{gsL} + i_{dsH} + i_{gsH} \tag{2.1}$$

where I_d represents the channel current, and the other terms correspond to the charging currents for each parasitic capacitor.

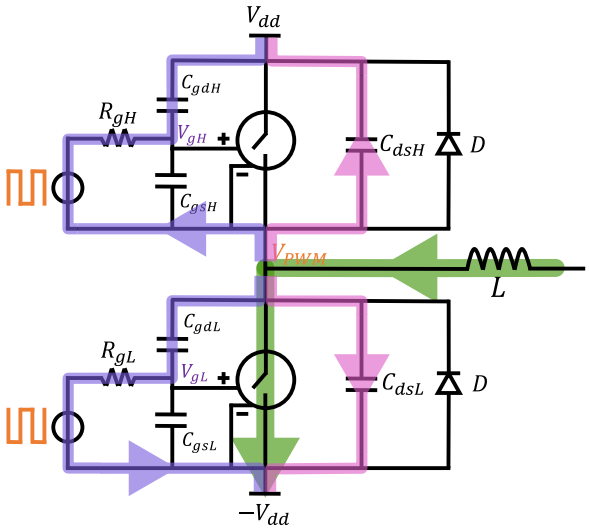


Figure 2.7: Charging and discharging of the capacitors when V_{PWM} goes up.

From stage (4) to stage (5), the voltage V_{PWM} goes down because the low-side power switch is turned on and the parasitic capacitors of the power switches are discharged, as shown in Figure 2.8.

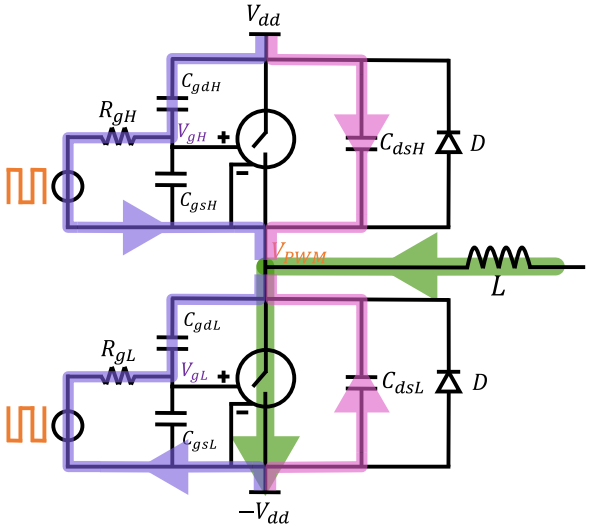


Figure 2.8: Charging and discharging of the capacitors when V_{PWM} goes down.

By applying Kirchhoff's current law (KCL), ones can get

$$i_L = I_{dL} - i_{dsL} - i_{gsL} - i_{dsH} - i_{gsH} \tag{2.2}$$

where I_d represents the channel current, and the other terms correspond to the discharging currents for each parasitic capacitor.

The transition from stage (1) to stage (2) is referred to as "soft switching" due to the switching process occurring as a result of charging the parasitic capacitors with a limited inductor current. As a consequence, the switching time in this case is relatively long.

On the other hand, the transition from stage (4) to stage (5) is termed "hard switching" because it takes place when the low-side power switch is turned on, allowing the parasitic capacitors to discharge rapidly through the low-resistance channel of the MOSFET. As a result, the switching time in this scenario is notably short. Therefore, the distortion caused by hard switching, specifically falling time distortion in this situation, is considered to be zero.

The soft switching from stage (1) to stage (2) causes the rising time distortion at the output, while the rising time is the same as the charging time of the parasitic capacitors with the inductor current. The inductor current comprises both the load current and the ripple current, which is shown in Figure 2.9. T represents the period of the ripple component and D represents the duty cycle of the PWM waveform before the LC filter.

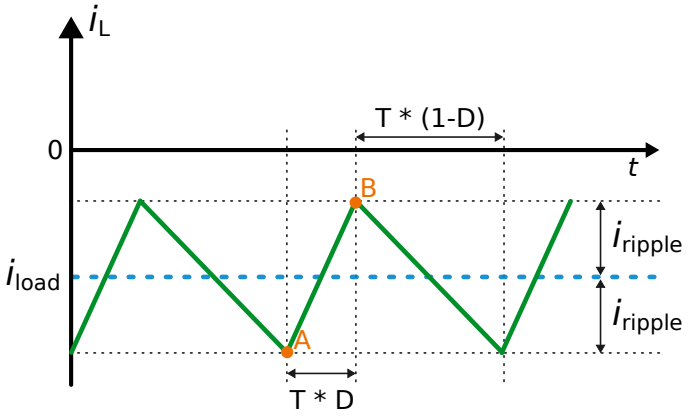


Figure 2.9: The inductor current.

$$i_L = i_{load} + i_{ripple} \tag{2.3}$$

The load current can be calculated using the expression

$$i_{load} = \frac{V_{out}}{R} = \frac{V_{dd} * (2D-1)}{R} \tag{2.4}$$

For the ripple current, it can be calculated as

$$\begin{aligned} i_{ripple} &= \frac{1}{2} * \int_0^{T*D} \frac{V_{dd} - V_{out}}{L} dt \\ &= \frac{V_{dd}}{L} TD(1-D) \end{aligned} \tag{2.5}$$

The soft switching happens when V_{PWM} increases, which results in an increase of inductor current i_L. Therefore, the soft switching is at point A in Figure 2.9. The inductor current at this point is

$$i_L = \frac{V_{dd} * (2D-1)}{R} - \frac{V_{dd}}{L} TD(1-D) \tag{2.6}$$

The current flowing into C_{ds} and C_{gd} are both related to the change of V_{PWM}.

$$i_{ds} = C_{ds} \frac{dV_{PWM}}{dt} \tag{2.7}$$

$$i_{gd} = C_{gd} \frac{dV_{PWM}}{dt} \tag{2.8}$$

Given that the power MOSFET is modeled as an ideal switch and capacitors, the switch can only be in either the on or off state. V_{PWM} will go up only when the ideal switch is off. Therefore, I_{dL} in Equation 2.1 and 2.2 is actually zero when there is current flowing into the capacitors.

Assuming the high-side and low-side power MOSFET are symmetrical, Equ 2.1 becomes

$$\begin{aligned} i_L &= I_{dL} + i_{dsL} + i_{gsL} + i_{dsH} + i_{gsH} \\ &= 2 * i_{ds} + 2 * i_{gd} \\ &= 2 * (1 + \frac{C_{gd}}{C_{ds}}) * i_{ds} \end{aligned} \tag{2.9}$$

Combining Equation 2.9 with Equation 2.6 yields the following expression

$$i_{ds} = \frac{C_{ds}}{2(C_{ds} + C_{gd})} * \left(\frac{V_{dd} * (2D-1)}{R} - \frac{V_{dd}}{L} TD(1-D) \right) \tag{2.10}$$

Finally, the soft switching speed, denoted as $\frac{dV_{PWM}}{dt}$, can be acquired as

$$\frac{dV_{PWM}}{dt} = \frac{i_{ds}}{C_{ds}} = \frac{1}{2(C_{ds} + C_{gd})} * \left(\frac{V_{dd} * (2D-1)}{R} - \frac{V_{dd}}{L} TD(1-D) \right) \tag{2.11}$$

where

$$D = \frac{1}{2} * (\frac{V_{in}}{V_{tri}} + 1) \tag{2.12}$$

Here, V_{in} represents the amplitude of the input signal, and V_{tri} denotes the amplitude of the triangular signal.

Therefore, the soft switching speed is related to the input signal.

The reason for rising and falling time distortion can be attributed to soft switching or hard switching respectively. As hard switching is typically much faster than soft switching, hard switching time is neglected in subsequent calculations, while soft switching time can be determined by the input signal.

2.4. CONCLUSION

In this chapter, the distortion mechanisms in the power stage of class D amplifiers are explained in detail. Deadtime distortion is due to the current flowing through the body diode of the power MOSFETs, causing the change of the duty cycle of the PWM waveform at the output of the power stage. Rising and falling time distortion is due to the charging of the parasitic capacitors of the power MOSFETs. Both of these two kinds of distortion are related to the inductor current, thus the input signal.

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3

DISTORTION REDUCTION BY COMPENSATION

3.1. INTRODUCTION

The compensation technique acts as a feedforward mechanism aimed at improving circuit performance by reducing the error within the circuit. This error usually stems from the inherent characteristics of the original circuit, which enables the prediction of the error before the signal enters the circuit. By incorporating an additional feedforward path that includes the compensation signal, the compensation technique anticipates and cancels out the error, leading to enhanced overall circuit performance.

In addition, it is important to note that the compensation technique does not introduce any additional signal loops within the circuit. As a result, the stability of the circuit is effectively maintained, ensuring that no adverse effects or instability are introduced as a consequence of employing the compensation technique.

Nevertheless, it is worth noting that the compensation technique has certain limitations in terms of enhancing circuit performance. Its effectiveness heavily relies on the reproducibility of the error, which may be challenging due to the omission of various non-linear effects and parasitic parameters during the calculation for the sake of simplicity. The drawback inherently restricts the extent of improvement that can be achieved through the compensation technique.

3.2. THEORETICAL CALCULATION FOR THE ERROR

As described in Chapter 2, the PWM waveform at the output of the power stage will deviate from an ideal square-like waveform due to the presence of deadtime distortion and rising and falling time distortion. Figure 3.1 displays the actual PWM waveform observed at the output of the power stage. The following analysis will still base on the second situation discussed in Section 2.3 due to the symmetry of the sinusoidal input signal.

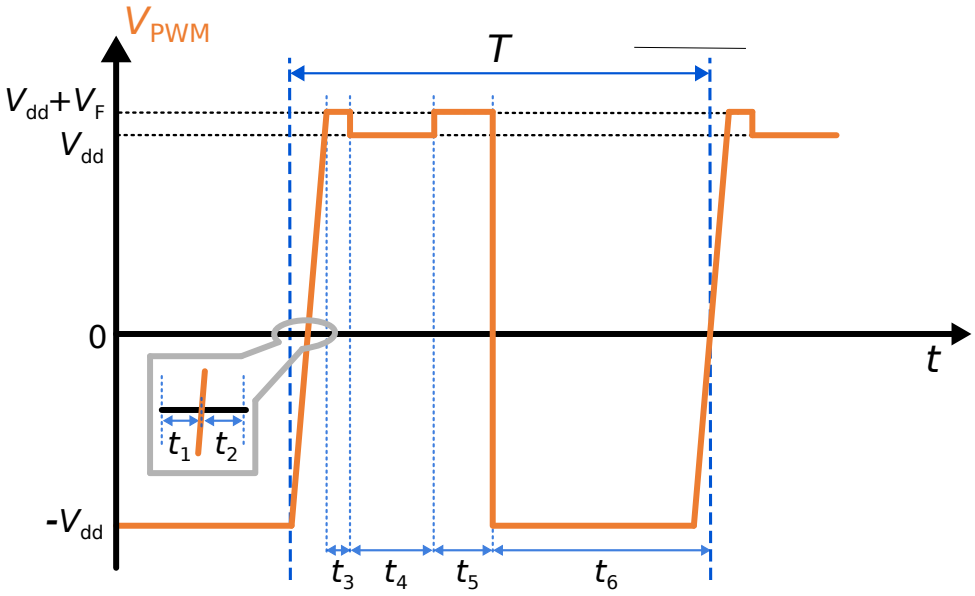


Figure 3.1: Actual PWM waveform at the output of the power stage.

A complete period T of the PWM waveform is divided into several time zones for calculation.

- t_1: the time for the voltage of V_{PWM} to rise from $-V_{dd}$ to 0;
- t_2: the time for the voltage of V_{PWM} to rise from 0 to V_{dd}, $t_1 + t_2$ equals the soft switching time, or the rising time in this situation;
- t_3: the time when the voltage of V_{PWM} is higher than the positive power suply, which means the current flows through the high-side body diode. $t_1 + t_2 + t_3$ equals the deadtime period t_d;
- t_4: the time when the high-side power switch is turned on;
- t_5: the deadtime period t_d;
- t_6: the time when the low-side power switch is turned on.

There is the possibility that t_3 equals 0 if the soft switching time is larger than the deadtime. However, this only happens when the input signal is very small so that the ripple signal cannot be ignored when doing the analysis. Consequently, the compensation method does not encompass situations where the input signal is approximately zero.

Since the switching frequency is much higher than the signal frequency, it is reasonable to approximate the output signal within one switching period as constant. Consequently, the output signal can be effectively extracted by taking the average of the PWM waveform in Figure 3.1. This averaging process aligns with the function of a low-pass filter, which aims to extract the desired signal component while attenuating the high-frequency switching signal.

The actual output voltage can be calculated as

$$V_{out,act} = \frac{1}{T} * \Big(\frac{1}{2} * (-V_{dd}) * t_1 + \frac{1}{2} * (V_{dd} + V_F) * t_2 + (V_{dd} + V_F) * t_3 + V_{dd} * t_4 + (V_{dd} + V_F) * t_5 + (-V_{dd}) * t_6 \Big) \tag{3.1}$$

where

$$t_1 = \left| \frac{2(C_{ds} + C_{gd}) * V_{dd}}{\left(\frac{V_{out,act}}{R} - \frac{V_{dd}}{L} TD(1-D) \right)} \right| \tag{3.2}$$

$$t_2 = \left| \frac{2(C_{ds} + C_{gd}) * (V_{dd} + V_{th})}{\left(\frac{V_{out,act}}{R} - \frac{V_{dd}}{L} TD(1-D) \right)} \right| \tag{3.3}$$

$$t_3 = t_d - t_1 - t_2 \tag{3.4}$$

$$t_4 = T * D - t_d \tag{3.5}$$

$$t_5 = t_d \tag{3.6}$$

$$t_6 = T * (1-D) - t_d \tag{3.7}$$

Finally,

$$V_{out,act} = \frac{1}{T} * \Big(V_{dd} * T * (2D-1) + 2 * (V_{dd} + V_F) * t_d - \frac{2(C_{ds} + C_{gd})}{\left| \left(\frac{V_{out,act}}{R} - \frac{V_{dd}}{L} TD(1-D) \right) \right|} \Big(\frac{1}{2} V_{dd}^2 + \frac{1}{2} (V_{dd} + V_F)^2 + (V_{dd} + V_F) * V_{dd} \Big) \Big) \tag{3.8}$$

$$D = \frac{1}{2} * \Big(\frac{V_{in}}{V_{tri}} + 1 \Big) \tag{3.9}$$

With the same input voltage V_{in}, the ideal output would be

$$V_{out,ideal} = V_{in} * \frac{V_{dd}}{V_{tri}} \tag{3.10}$$

where V_{tri} is the amplitude of the triangular waveform.

Therefore, the error between the ideal output and the actual output can be acquired with other circuit parameters by giving the input signal.

3.3. CONCEPT DESIGN OF COMPENSATION CIRCUIT

Equation 3.11 shows an alternative form of the ideal transfer function in class D amplifiers.

$$\frac{V_{in}}{V_{tri}} = \frac{V_{out,ideal}}{V_{dd}} \tag{3.11}$$

Hence, it can be inferred that in a conventional class D amplifier, the proportion of V_{in} in relation to V_{tri} should be equal to the proportion of $V_{out,ideal}$ in relation to V_{dd}, as depicted in Figure 3.2.

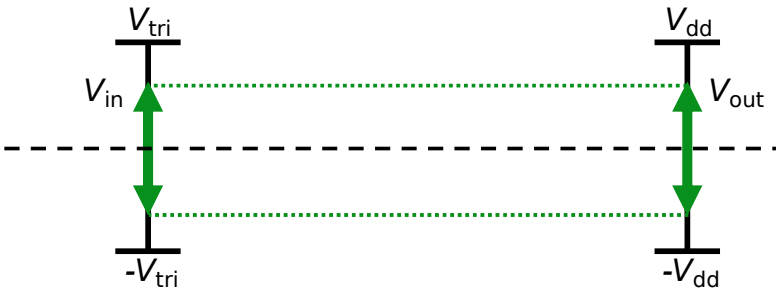


Figure 3.2: Ideal transfer without distortion.

This duty cycle of the PWM waveform before the power stage (referred to as the input duty cycle) will ideally equal the duty cycle after the power stage (referred to as the output duty cycle) so that the input and output can share the same proportion with respect to V_{tri} and V_{dd} relatively.

However, as indicated in the analysis presented in Section 3.4, an error arises between the ideal output and the actual output due to distortion within the power stage, as illustrated in Figure 3.3. This distortion includes effects such as deadtime distortion and rising and falling time distortion, which impacts the output duty cycle and subsequently influences the output after the low-pass filter.

Mathematically, this can be expressed as:

$$|V_{out,act}| < |V_{out,ideal}| \tag{3.12}$$

The concept of compensation is based on the understanding that distortion within the power stage is inevitable and leads to a reduction in output. The idea behind compensation is to incorporate a reproduced error prior to the power stage. By doing so, the output after the power stage can be precisely adjusted to the desired value, effectively compensating for the distortion-induced reduction. This compensation approach aims to counterbalance the distortion effects, ensuring that the output aligns with the desired

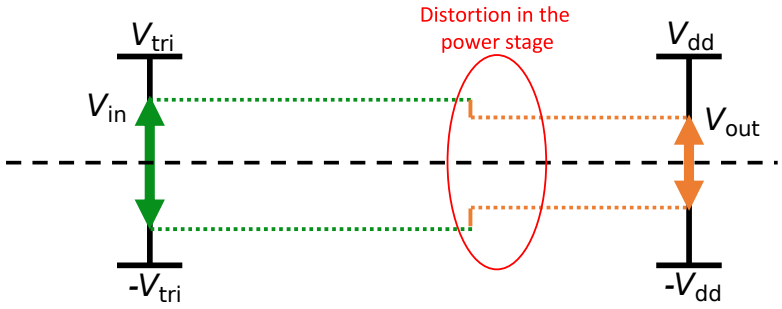


Figure 3.3: Transfer with the distortion from the power stage.

target value despite the inherent distortion present in the power stage.

The compensation idea is achieved by modifying the amplitude of the triangular wave, as shown in Figure 3.4. For a given input V_{in}, by decreasing the amplitude of the triangular wave, the proportion of V_{in} in relation to $V_{modi-tri}$ increases. Following this, if the influence of distortion within the power stage is taken into account, the desired output is achieved.

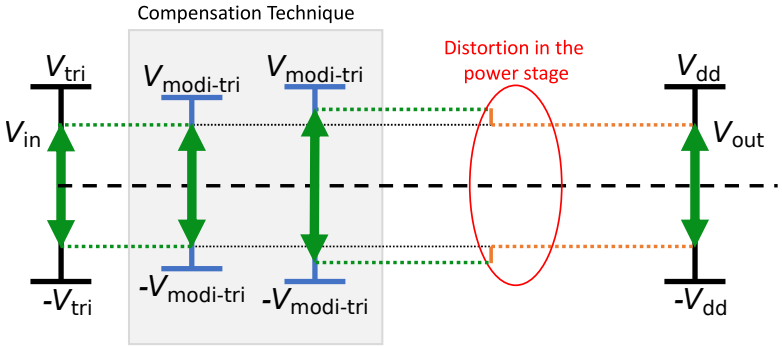


Figure 3.4: Compensation idea for suppressing the distortion.

The following equations illustrate the calculation of the amplitude of the modified triangular wave.

Given an input V_{in}, the ideal output would be

$$V_{out,ideal} = V_{in} * \frac{V_{dd}}{V_{tri}} \tag{3.13}$$

By doing the substitution of $V_{out,ideal}$ for $V_{out,act}$ in Equation 3.8, the actual input duty cycle to achieve the ideal output is obtained.

$$V_{out,ideal} = \frac{1}{T} * \Big(V_{dd} * T * (2D_{act} - 1) + 2 * (V_{dd} + V_F) * t_d - \frac{2(C_{ds} + C_{gd})}{\left(\frac{V_{out,ideal}}{R} - \frac{V_{dd}}{L} T D_{act} (1 - D_{act}) \right)} * \left(\frac{1}{2} * V_{dd}^2 + \frac{1}{2} * (V_{dd} + V_F)^2 + (V_{dd} + V_F) * V_{dd} \right) \Big) \tag{3.14}$$

The relationship between the actual input duty cycle and the modified triangular wave is shown as

$$\frac{V_{in}}{V_{tri,modi}} = 2 * D_{act} - 1 \tag{3.15}$$

By considering Equation 3.13, 3.14 and 3.15 together, the amplitude of the modified triangular wave $V_{modi-tri}$ corresponding to the input signal V_{in} can be obtained. The complex calculation will be done in MATLAB.

3.4. CONCEPT VERIFICATION

The concept verification was conducted using LTSpice, and the testbench setup is depicted in Figure 3.5.

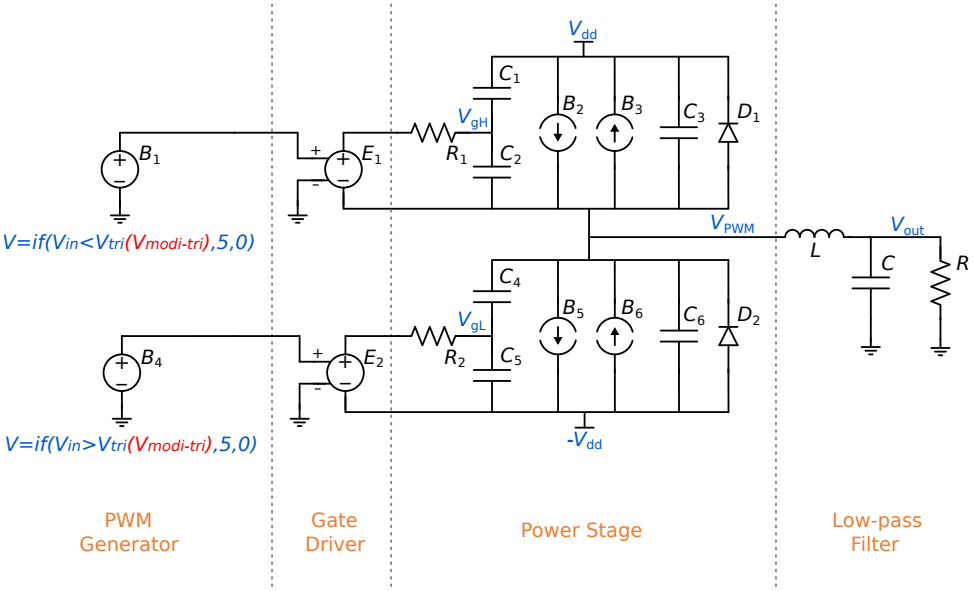


Figure 3.5: Testbench for the concept verification.

In the testbench, the behavior voltage sources are utilized to serve as the PWM generator, while the voltage-control-voltage sources are employed as the level shifter and gate

drive. The EKV MOSFET model is selected to accurately represent the characteristics of the power MOSFETs, considering the presence of parasitic capacitors, bode diodes, and gate resistors. Within the EKV model, two behavior current sources are incorporated to capture the behavior of the channel current in the MOSFET from weak inversion to strong inversion.

$$I_{F,R} = 2n\beta_{sq}U_T^2\frac{W}{L}IC_{F,R} \tag{3.16}$$

where n, β_{sq}, U_T are technology parameters, $IC_{F,R}$ is the forward and reverse inversion coefficient [1].

$$IC_{F,R} = F\left(\frac{V_G - V_{T0} - nV_{S,D}}{nU_T}\right) \tag{3.17}$$

$$\begin{aligned} F(x) &= \left(ln\left(1 + exp(\frac{x}{2})\right)\right)^2 \\ &= \begin{cases} exp(x) & if\, x << 0, \\ (\frac{x}{2})^2 & if\, x >> 0. \end{cases} \end{aligned} \tag{3.18}$$

The simulation was conducted under specific conditions, including the following parameters:

- Amplitude of the input sinusoidal wave: 2V
- Frequency of the input sinusoidal wave: 1kHz
- Amplitude of the carrier triangular wave: 3V
- Frequency of the carrier triangular wave: 1MHz
- Deadtime: 10ns

Moreover, the parameters of the EKV model used in the simulation were set based on the technology library specific to the power MOSFET being employed.

Figure 3.6 displays the modified triangular waveform alongside the input waveform. The modified triangular waveform is determined based on the calculation in Section and . It can be noticed that the amplitude of the modified triangular waveform changes with the input signal. There is no compensation applied when the input signal is around zero since the ripple current cannot be ignored with the small input signal.

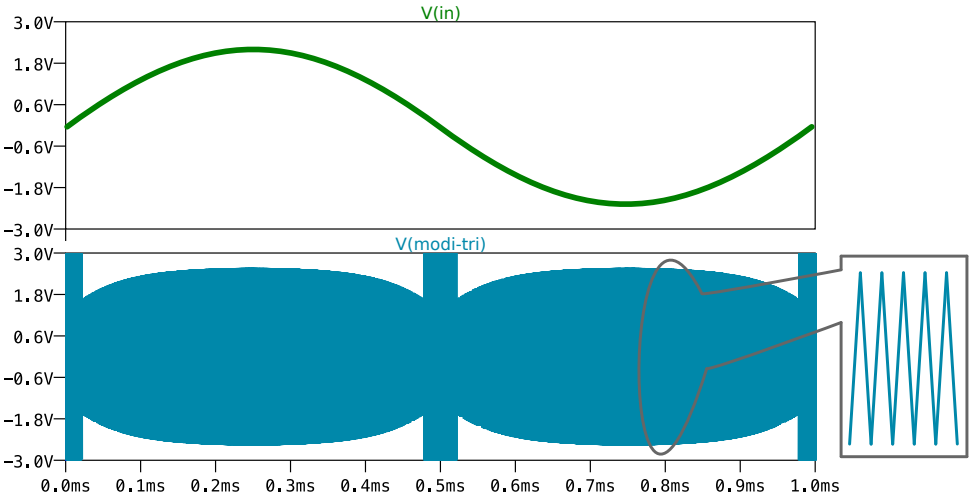


Figure 3.6: Modified amplitude of the triangular wave.

The simulation results for THD versus output power with the modified triangular wave enabled and disabled are shown in Figure 3.7. For the calculation of THD, it takes 20 harmonics into consideration while the harmonics out of the audio band are ignored.

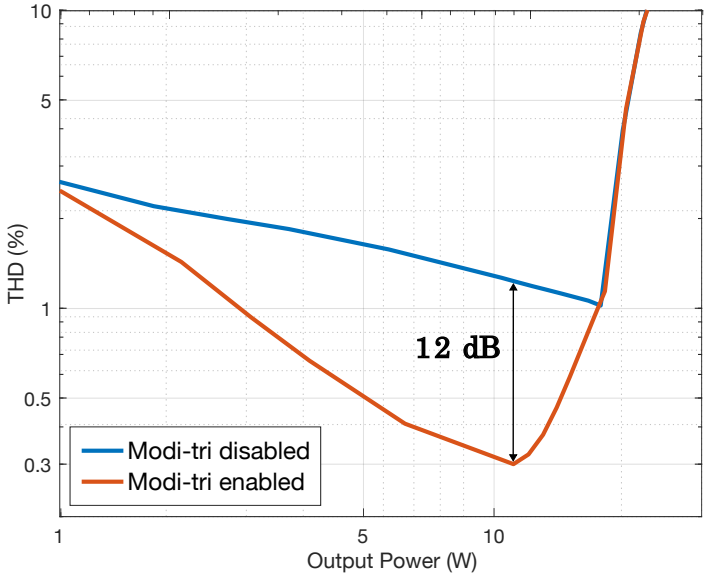


Figure 3.7: THD versus output power with a $1k\ Hz$ input.

The results indicate that the utilization of the modified triangular waveform leads to an effective suppression in total harmonic distortion (THD) when the output power surpasses 1 W. The most notable enhancement, reaching up to 12 dB, is realized at an output power level of approximately 10 W.

3.5. CONCLUSION

In this chapter, a novel compensation technique aimed at reducing distortion is introduced. The theoretical calculation of the reproduced error builds upon the analysis in Chapter 2. The idea of the compensation approach revolves around reproducing the identified error through the utilization of the modified triangular waveform and the validation of this compensation technique is undertaken via simulations conducted in LTspice. The results of these simulations affirm the effectiveness of the proposed compensation method in reducing distortion, leading to a maximum improvement of 12 dB.

However, the application of this compensation technique in an actual transistor-level circuit, especially when factoring in temperature variations and technology corners, may potentially yield an even smaller degree of enhancement in performance. In addition, the equations in this compensation technique are non-linear, making their implementation within transistor-level circuits a challenging and complex task.

Consequently, the compensation technique introduced in this chapter will remain confined to the conceptual design phase and will not progress to the implementation stage with the transistor-level circuit.

REFERENCES

[1] A. Montagne. *Structured Electronic Design*. Delft Academic Press, 2019.

4

DISTORTION REDUCTION BY FEEDBACK

4.1. INTRODUCTION

Negative feedback has been widely recognized as an effective technique for enhancing the linearity of circuits [1–3]. Through the incorporation of a negative feedback loop, the circuit gains the capability to compare the actual output waveform with the desired ideal waveform, thereby enabling the correction of the output and reducing the distortion. The primary consideration during the design of the feedback loop is ensuring stability. Therefore, to attain stable behavior and achieve the desired frequency response, it's typically essential to employ frequency compensation techniques.

Section 4.2 describes the concept design of the negative feedback loop, including the choice of the feedback node and a straightforward two-step approach that avoids iterative loops [4]. The phantom zero technique is applied when doing the frequency response design of the feedback loop. The concept verification presented in Section 4.3 is conducted using SLICAP (Symbolic Linear Circuit Analysis Program, an open-source symbolic simulator package developed in Python for the analysis of circuit transfer functions and frequency responses [5]. Section 4.4 describes the circuit implementation of the feedback path and the controller, together with the simulation results.

4.2. CONCEPT DESIGN OF NEGATIVE FEEDBACK LOOP

4.2.1. FEEDBACK NODE

Figure 4.1 illustrates the conventional class D amplifier configuration. Due to the switching characteristics of class-D amplifiers, an LC low-pass filter is employed after the power stage to extract the low-frequency output signal. However, integrating the large and bulky inductor and capacitor of the LC filter into the chip poses challenges in terms of chip area constraints, making it impractical [6].

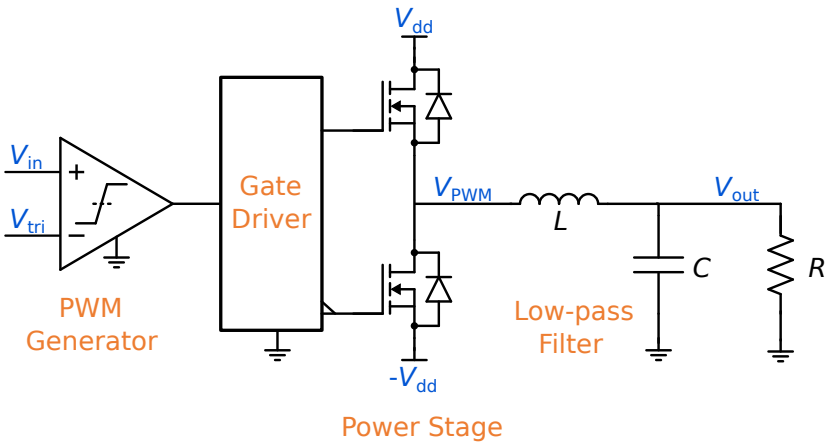


Figure 4.1: Conventional class D amplifier.

As discussed by Marco [7], the inductor and capacitor used in the low-pass filter can introduce distortion due to their inherent nonlinearity. This nonlinearity can be expressed mathematically as follows:

For the capacitor, its voltage dependence can be characterized by the equation:

$$C(V) = C_{nom} \frac{1}{1 + \left(\frac{V}{V_{SAT}}\right)^2} \tag{4.1}$$

where C_{nom} represents the nominal capacitance value and V_{SAT} is the voltage at which the capacitance is reduced by 50% compared to its nominal value.

For the inductor, its current dependence can be described by the equation:

$$L(I) = L_{nom} \frac{1}{1 + \frac{1}{3}\left(\frac{I}{I_{SAT}}\right)^2} \tag{4.2}$$

where L_{nom} represents the nominal inductance value and I_{SAT} is the current at which the inductance is reduced by 25% compared to its nominal value.

With Equation 4.1 and 4.2, the total harmonic distortion (THD) caused by nonlinearity in inductance (THD_L) or capacitance (THD_C) can be approximated as:

$$THD_L = \frac{\omega}{\omega_0 Q} \cdot \frac{P_{out}}{6R_{load} \cdot I_{SAT}^2} \tag{4.3}$$

$$THD_C = \frac{\omega^2}{\omega_0^2} \cdot \frac{P_{out} \cdot R_{load}}{2 \cdot V_{SAT}^2} \tag{4.4}$$

where ω represents the signal angular frequency, ω_0 represents the angular resonance frequency of the LC filter and Q is the quality factor of the LC filter.

To make the distortion caused by the LC filter be suppressed by the loop gain, the LC filter needs to be included in the feedback loop. Therefore, to achieve the best THD performance, feedback after the low-pass filter is chosen. This arrangement has the added advantage of reducing the incorporation of higher-frequency components into the feedback loop.

4.2.2. TWO-STEP DESIGN

FIRST-STEP DESIGN

In the first step, the ideal gain of the amplifier is determined. This gain is primarily determined by the feedback network when the controller is considered a nullor, an ideal controller, and the direct transfer is assumed to be negligible. This step ensures that the desired gain is achieved in the amplifier design.

Figure 4.2 shows the block diagram of negative feedback Class-D amplifier with a nullor.

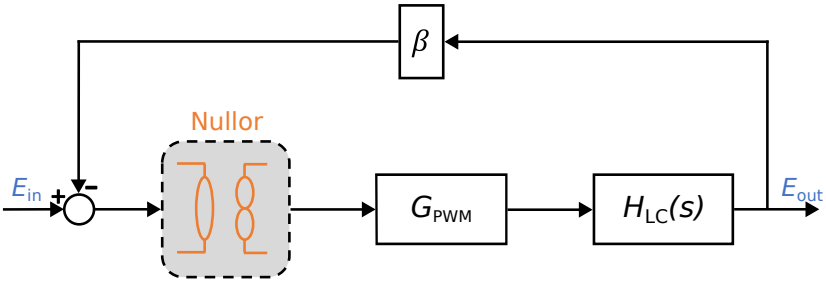


Figure 4.2: Block diagram of negative feedback Class D amplifier with an ideal controller.

The ideal gain can be expressed as

$$A_i = -\frac{1}{\beta} \tag{4.5}$$

In order to achieve the customer's requirement of an output power of $30W$ without clipping, the ideal gain of the amplifier is set to 8. By considering an 8 Ω resistive load and a full-bridge power stage, the amplifier can attain the desired output power under specific conditions. For instance, when the amplitude of the sinusoidal input signal is $V_{in} = 1.37\ V$, the amplifier will produce an output power of $30W$. This can be calculated

using the formula:

$$P_{out}(V_{in} = 1.37\ V) = \frac{\left(2 * \frac{V_{in}}{\sqrt{2}} * A_i\right)^2}{R_{load}} = \frac{\left(2 * \frac{1.37\ V}{\sqrt{2}} * 8\right)^2}{8\ \Omega} = 30\ W \tag{4.6}$$

The circuit will experience clipping when the input voltage reaches $V_{in} = 1.5\ V$ with a supply voltage of $V_{SUP} = 24\ V$.

SECOND-STEP DESIGN

The second step of the design process focuses on designing the controller for the negative feedback amplifier. This involves replacing the nullor in Figure 4.2 with a practical circuit implementation. The transfer function of the controller is denoted as $H(s)$ and the new block diagram is shown in Figure 4.3.

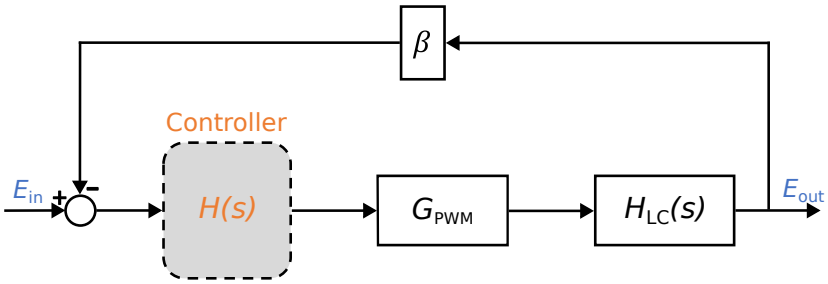


Figure 4.3: Block diagram of negative feedback Class D amplifier with a non-ideal controller.

There are two essential requirements to consider during this design phase:

- Firstly, the controller should be designed to ensure that the loop gain within the audio frequency range of $20-20,000\ Hz$ is as high as possible. This helps in reducing distortion originating from the power stage, enhancing the overall performance of the amplifier.
- Secondly, the controller should be designed in a manner that the unity-gain frequency of the loop f_{UG} is limited by the switching frequency f_{SW} to stabilize the whole loop [8]. This restriction is expressed by the inequality:

$$f_{UG} < \frac{1}{\pi} * f_{SW} \tag{4.7}$$

In Figure 4.4, the x-axis of the loop gain bode plot for the block diagram in Figure 4.3 is annotated with significant frequency points.

- Orange diamond: switching frequency in the class D amplifier;
- Green Triangle: requirement for the unity-gain frequency of the feedback loop;
- Blue circle: cut-off frequency of the LC filter;

- Red bold line: the extent of the audio bandwidth.

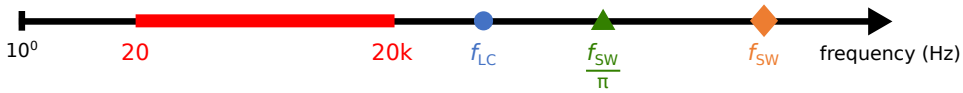
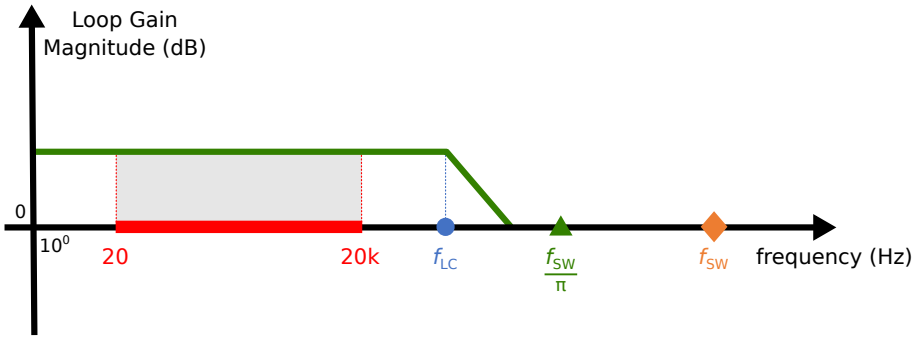


Figure 4.4: Significant frequency points on the x-axis of the loop gain bode plot.

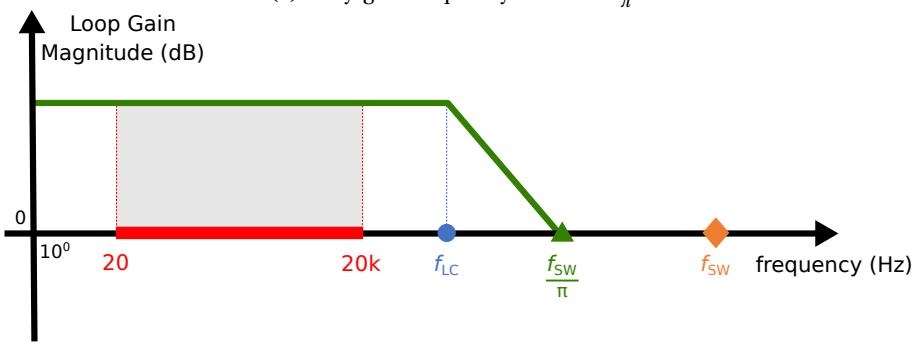
The design starts by assuming a flat transfer function of the controller,

$$H(s) = K \tag{4.8}$$

where K is a constant. Figure 4.5 shows the magnitude plot of the loop gain with $H(s) = K$, among which Figure 4.5a illustrates the situation when the unity-gain frequency is less than $\frac{f_{sw}}{\pi}$ and Figure 4.5b for the unity-gain frequency equaling $\frac{f_{sw}}{\pi}$. The shaded regions denote the loop gain within the audio bandwidth.



(a) unity-gain frequency less than $\frac{f_{sw}}{\pi}$



(b) unity-gain frequency equaling $\frac{f_{sw}}{\pi}$

Figure 4.5: Loop gain magnitude plot with $H(s) = K$.

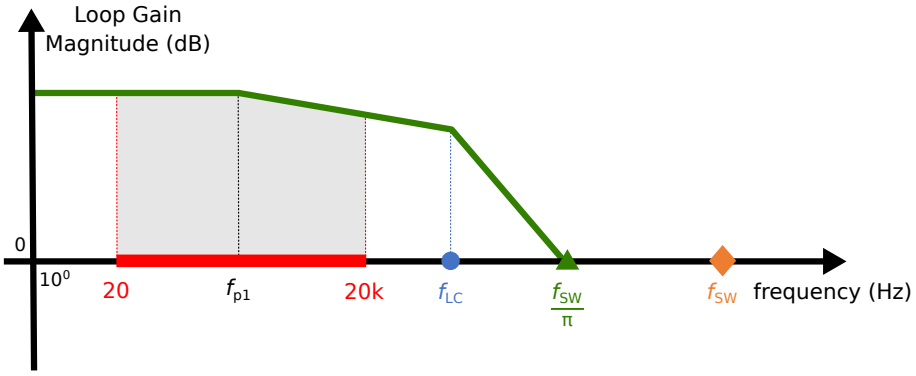
By comparing Figure 4.5a and 4.5b, a conclusion can be made that the unity-gain frequency of the loop gain should just equal the requirement $\frac{f_{sw}}{\pi}$, thus ensuring the maximum loop gain within the audio bandwidth.

If the unity-gain frequency is held constant while aiming to amplify the loop gain, achieving a faster decline in loop gain magnitude becomes necessary. Given that each pole in the transfer function results in a descent of -20dB per decade in the magnitude plot, the solution can be introducing additional poles to the transfer function of the controller.

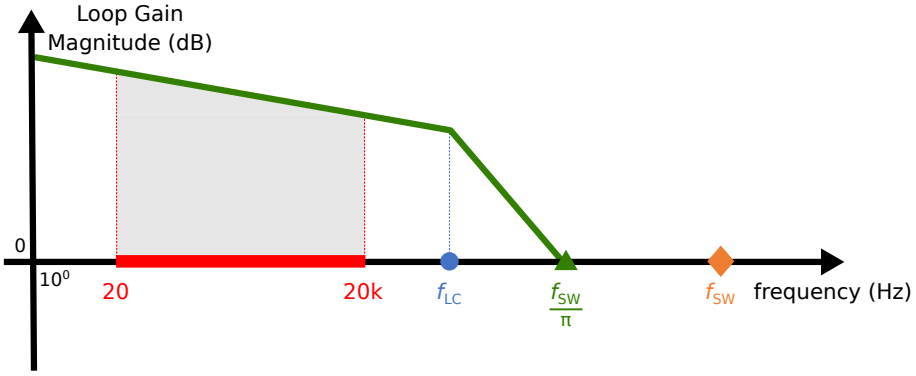
Suppose there is one pole in the transfer function of the controller,

$$H(s) = K \cdot \frac{1}{s + \omega_{p1}} \tag{4.9}$$

Figure 4.5 shows the magnitude plot of the loop gain with $H(s) = K \cdot \frac{1}{s+\omega_{p1}}$, among which Figure 4.6a illustrates the situation when this pole is not at the origin and Figure 4.6b for the pole at the origin.



(a) pole not at the origin



(b) pole at the origin

Figure 4.6: Loop gain magnitude plot with $H(s) = K \cdot \frac{1}{s+\omega_{p1}}$.

From the comparison of Figure 4.6a and Figure 4.6b, a clear observation emerges: when the pole of the controller's transfer function is located at the origin, the resultant loop gain surpasses the scenario where the pole is situated at alternative positions. This conclusion extends to instances where multiple poles are present in the controller's transfer function as well.

Given that the circuit depicted in Figure 4.3 constitutes a multi-pole system, the introduction of zeros becomes imperative to achieve loop stability. However, it's important to notice that zeros have the potential to attenuate the magnitude of the loop gain with the unity-gain frequency fixed. To ensure both the stabilization of the loop and minimal alteration of the magnitude plot, a strategic approach involves situating the zeros in close proximity to the unity-gain frequency.

Figure 4.7 shows the Bode plot of the loop gain, with n poles at the origin and $n+1$ zeros at the unity-gain frequency. This strategic configuration serves the dual purpose of maximizing the loop gain within the audio bandwidth and maintaining stability within the negative feedback loop.

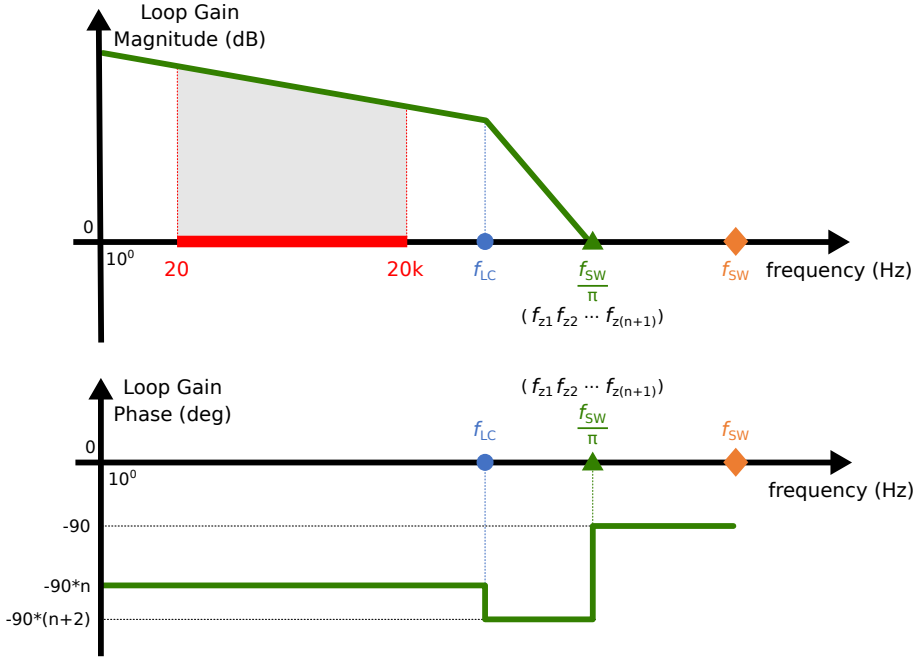


Figure 4.7: Bode plot of the loop gain of the feedback loop.

In conclusion, considering the frequency response characteristics of the controller, it is necessary to incorporate poles in order to boost the loop gain within the audio frequency range, while zeros are required to achieve loop stabilization. The guidelines include positioning the poles in close proximity to the origin and the zeros in close proximity to the unity-gain frequency.

Complex zeros demonstrate greater effectiveness in elevating the phase within the

Bode plot compared to real zeros. The presence of a pair of complex zeros indicates the existence of at least two accompanying poles. Upon incorporating the two complex poles originating from the LC low-pass filter, the circuit encompasses a total of four poles and two zeros within the unity-gain frequency range. Consequently, an additional zero is required to ensure loop stabilization. Importantly, the pole associated with this supplementary zero should be positioned outside of the bandwidth.

Thus, in this particular design, there are a total of four poles and three zeros within the bandwidth. This comprises two poles located at the origin, two poles determined by the LC low-pass filter, and three zeros in close proximity to the unity-gain frequency.

Equation 4.10 shows the transfer function of the negative feedback class D amplifier in Figure 4.3.

$$H_f(s) = \frac{H(s) \cdot G_{PWM} \cdot H_{LC}(s)}{1 + H(s) \cdot G_{PWM} \cdot H_{LC}(s) \cdot \beta} \tag{4.10}$$

It's worth noting that the zeros present in the transfer function $H(s)$ of the controller will also appear in the transfer function of the class D amplifier. However, in many cases, the preferred configuration is an all-pole system. This choice aims to eliminate noise and interference beyond the desired bandwidth, aligning with the goal of achieving optimal signal quality.

According to the theory of phantom zeros, when applied in the feedback factor (β), the zero only appears in the expression for loop gain, contributing to loop stabilization, but does not manifest in the transfer function from the input to the output [4].

However, incorporating all three zeros and their accompanying poles in the feedback path can complicate the design and potentially impact the desired gain established during the first-step design. To maintain simplicity and straightforwardness, this design opts to place two complex zeros and two poles in the controller within the forward signal path. Simultaneously, a single real phantom zero and its corresponding pole (out of the bandwidth) are placed in the feedback signal path. Figure 4.8 shows the block diagram of the negative feedback amplifier with the arrangement of poles and zeros.

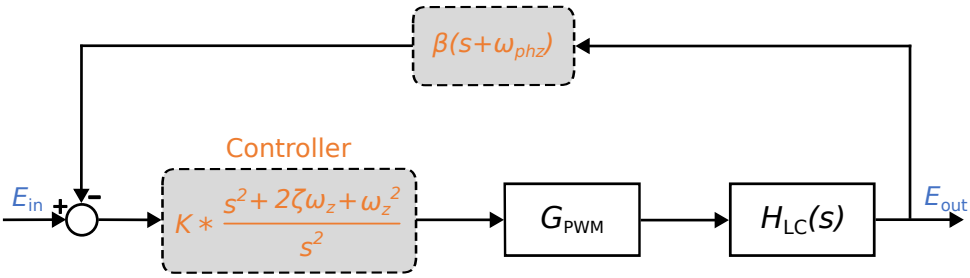


Figure 4.8: Block diagram with the arrangement of poles and zeros.

The loop gain can be expressed as

$$L = K \cdot G_{PWM} \cdot \beta \cdot \frac{(s^2 + 2\zeta\omega_z s + \omega_z^2)(s + \omega_{phz})}{s^2(1 + s^2 LC)} \tag{4.11}$$

where ω_{phz} is the angular frequency of the phantom zero, ω_z represents the angular frequency of the zero in the controller and ζ represents the damping ratio of the two complex zeros.

The transfer function of this designed negative feedback class D amplifier can be expressed as

$$H_f(s) = \frac{K \cdot G_{PWM} \cdot (s^2 + 2\zeta\omega_z s + \omega_z^2)}{s^2(1 + s^2 LC) + K \cdot G_{PWM} \cdot \beta \cdot (s^2 + 2\zeta\omega_z s + \omega_z^2)(s + \omega_{phz})} \tag{4.12}$$

It can be seen that this phantom zero does not appear in the transfer function.

4.3. CONCEPT VERIFICATION

The concept verification phase is conducted using SLICAP and based on the block diagram in Figure 4.8. The loop gain can be written in an alternative form as

$$L = K_{DC} \cdot \frac{(\frac{1}{\omega_z^2} s^2 + \frac{2\zeta}{\omega_z} s + 1)(\frac{1}{\omega_{phz}} s + 1)}{s^2(\frac{1}{LC} + s^2)} \tag{4.13}$$

where

$$K_{DC} = \frac{K \cdot G_{PWM} \cdot \beta \cdot \omega_z^2 \cdot \omega_{phz}}{LC} \tag{4.14}$$

To identify the optimal combination of parameters (K_{DC}, ω_z, ω_{phz} and ζ) for the system, a parameter sweep in SLICAP can be performed. This involves systematically varying these parameters within a defined range and evaluating the performance of the system for each combination.

The following criteria are applied when doing the parameter sweep:

1. The unity-gain frequency of the loop gain should be below $\frac{f_s w}{\pi}$;
2. All the zeros should be in close proximity to the unity-gain frequency of the loop gain;
3. All of the poles of the transfer function should be at the left-half plane in the s domain for stability concern.

The best combination that meets all the design criteria is determined as

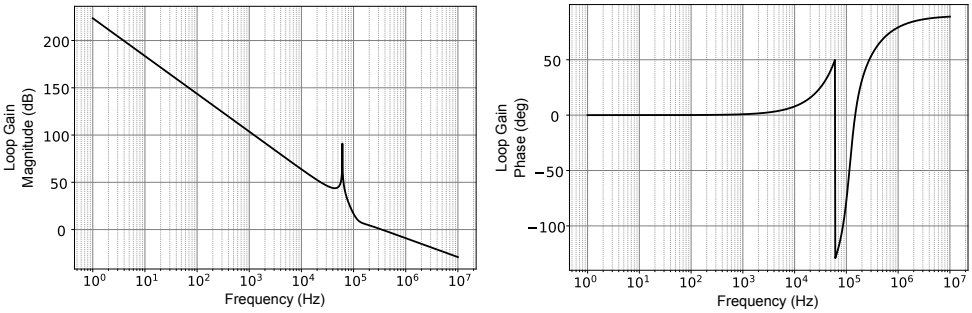
$$K_{DC} = 5.5 * 10^{11}$$

$$\omega_z = \omega_{phz} = 735.1k\ rad/s$$

$$\zeta = 0.3$$

Figure 4.9 presents the bode plot illustrating the frequency response of the loop gain.

The designed negative feedback loop shows a unity-gain frequency of $348.8k\ Hz$. At the frequency of $1k\ Hz$, the loop gain reaches $103.6\ dB$. The phase margin is around 57 degree.



(a) magnitude characteristic (b) phase characteristic

Figure 4.9: Bode plot of the loop gain in SLICAP.

4

Table 4.1 and Table 4.2 show the positions of the poles and zeros of the loop gain. Two poles are at the origin and another two complex poles are introduced by the LC low-pass filter. For the zeros, two complex zeros are implemented in the controller, and another real zero is created in the feedback path by using the phantom zero technique.

Table 4.1: Pole positions of the loop gain

	Real part $[Hz]$	Imag part $[Hz]$	Frequency $[Hz]$
p_1	0.00e+00	0.00e+00	0.00e+00
p_2	0.00e+00	0.00e+00	0.00e+00
p_3	0.00e+00	+6.10e+04	6.10e+04
p_4	0.00e+00	-6.10e+04	6.10e+04

Table 4.2: Zero positions of the loop gain

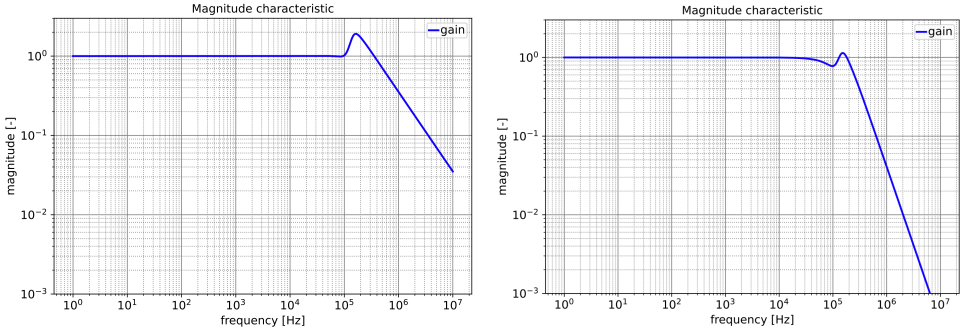
	Real part $[Hz]$	Imag part $[Hz]$	Frequency $[Hz]$
z_1	-3.51e+04	+1.12e+05	1.17e+05
z_2	-3.51e+04	-1.12e+05	1.17e+05
z_3	-1.12e+05	0.00e+00	1.17e+05

Table 4.3 shows the pole positions of the transfer function. All the poles are located at the left-half plane in the s domain, thus proving the negative feedback amplifier is stable.

Figure 4.10 shows the transfer function plots without the phantom zero technique and with the phantom zero technique. By examining the comparison between Figure 4.10a and Figure 4.10b, it can be inferred that the implementation of the phantom zero technique results in several advantageous characteristics in the transfer from input to output. Specifically, this technique leads to reduced peak levels and enhanced roll-off characteristics, thereby enabling faster attenuation. Importantly, these improvements are achieved while ensuring the maintenance of flatness within the audio band.

Table 4.3: Pole positions of the transfer function

	Real part [Hz]	Imag part [Hz]	Frequency [Hz]
p_1	-4.29e+04	+1.33e+05	1.40e+05
p_2	-4.29e+04	-1.33e+05	1.40e+05
p_3	-1.68e+05	+1.03e+05	1.97e+05
p_4	-1.68e+05	-1.03e+05	1.97e+05



(a) transfer without phantom zero

(b) transfer with phantom zero

Figure 4.10: Transfer function plot in SLICAP.

4.4. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

The network depicted in Figure 4.11 utilizes a g_m-stage configuration within the controller to precisely position the desired zeros and poles. This network comprises five g_m stages, represented by ideal voltage-control-current sources, along with two capacitors and one resistor. The symbolic and numeric values associated with the g_m-stage network can be observed in Table 4.4.

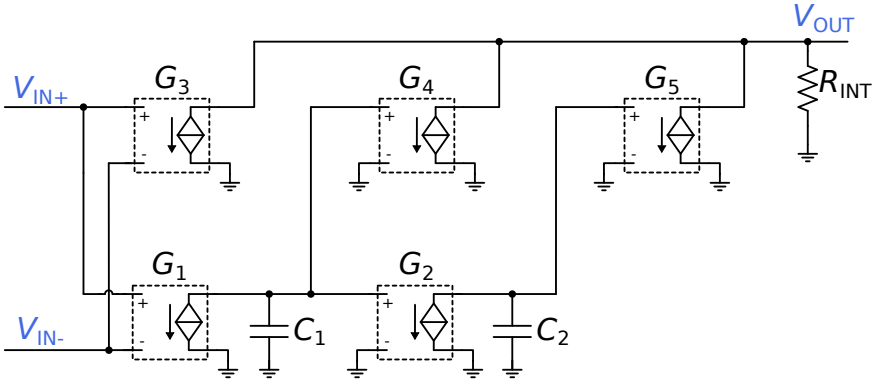


Figure 4.11: G_m-stage network in the controller.

Table 4.4: Symbolic values and numeric values for each component

	G_1	G_2	G_3	G_4	G_5
Symbolic value	g	g	b_2	b_1	b_0
Numeric value	$-8\mu\ S$	$-8\mu\ S$	$100\mu\ S$	$22\mu\ S$	$13.5\mu\ S$

The transfer function of the controller can be expressed as

$$\frac{V_{OUT}}{V_{IN+}-V_{IN-}} = \frac{R_{INT}\left(b_2 s^2 + b_1 \cdot \frac{g}{C} s + b_0 \cdot \frac{g^2}{C^2}\right)}{s^2} \tag{4.15}$$

The poles and zeros of the controller are shown in Table 4.5 and Table 4.6 respectively, which match the designed positions well.

Table 4.5: Poles of the controller

	Real part $[Hz]$	Imag part $[Hz]$	Frequency $[Hz]$
p_1	0.00e+00	0.00e+00	0.00e+00
p_2	0.00e+00	0.00e+00	0.00e+00

Table 4.6: Zeros of the controller

	Real part $[Hz]$	Imag part $[Hz]$	Frequency $[Hz]$
z_1	-3.50e+04	+1.12e+05	1.17e+05
z_2	-3.50e+04	-1.12e+05	1.17e+05

Figure 4.12 presents the testbench for the negative feedback amplifier, which incorporates the ideal power stage and the designed g_m-stage network. It is a non-inverting amplifier with a voltage feedback configuration.

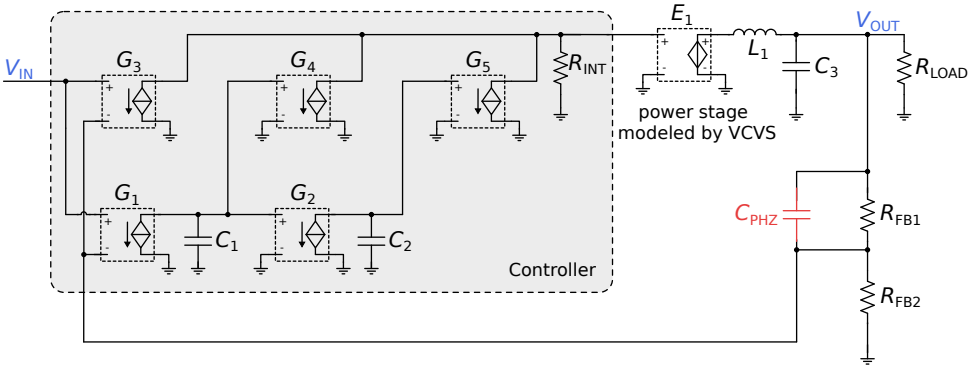


Figure 4.12: Negative feedback class D amplifier with ideal power stage.

The ideal gain is determined by R_{FB1} and R_{FB2}, as described in Equation 4.16.

$$A_i = 1 + \frac{R_{FB1}}{R_{FB2}} \tag{4.16}$$

Additionally, a parallel capacitor is employed to implement the phantom zero along the feedback resistor.

$$\omega_{phz} = \frac{1}{R_{FB1} \cdot C_{PHZ}} \tag{4.17}$$

Figure 4.13 shows the simulation results of the bode plot in Cadence. It achieves a loop gain of 103.7 dB at 1k Hz and a unity-gain frequency of 346.2k Hz. The phase margin is around 58 degree.

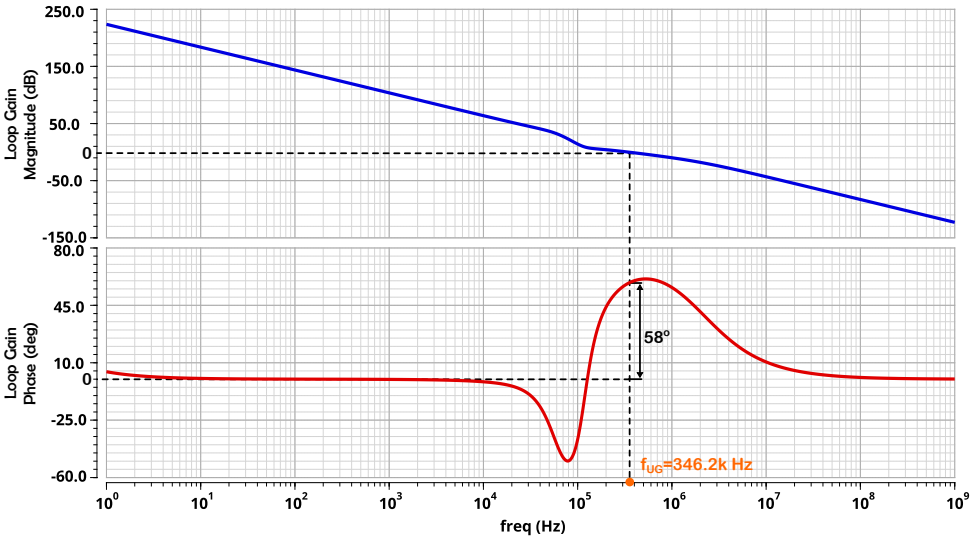


Figure 4.13: Bode plot of loop gain in Cadence.

Prior to designing the transistor-level g_m stages, it is crucial to establish appropriate biasing for the amplifier. The bias design for the amplifier is illustrated in Figure 4.14.

Considering a 24 V power supply for the power stage, the amplifier's output is biased to the midpoint of the supply voltage 12 V. However, for the g_m stages, a 24 V supply is unnecessary. Instead, they are designed to operate under a 5 V supply voltage and are biased at 3 V. To achieve this bias level transition from 12 V to 3 V, a DC current source denoted as I_b is employed.

The voltage at the output node of the controller, denoted as V_{INT}, will be compared with the triangular wave generated by a PWM generator, which has a voltage range from 0.5 V to 3.0 V. Consequently, V_{INT} is designed to be biased at the midpoint of the triangular wave 1.75 V. To ensure no DC current flows through R_{INT}, its other terminal is connected to 1.75 V.

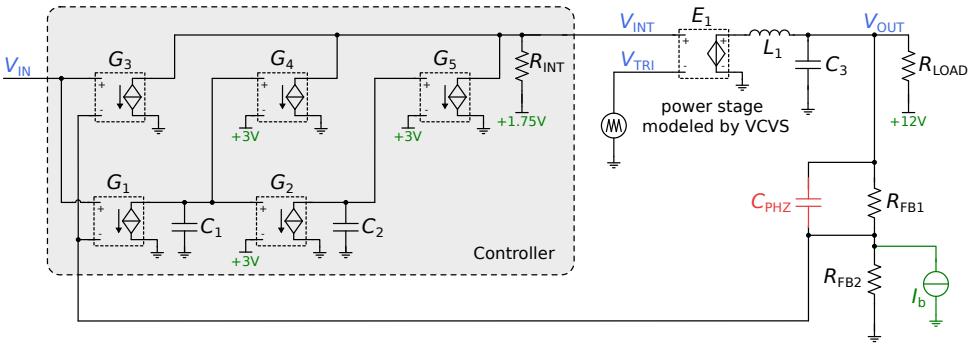


Figure 4.14: Bias design for the negative feedback class D amplifier.

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The next design step is to replace the voltage-control-current sources in the controller with the transistor-level circuit.

From Equation 4.15, it can be noticed that the positions of the two complex zeros are related to the ratio between the values of the g_m stages for the reason that

$$\omega_{z1} + \omega_{z2} = -\frac{b_1 \cdot g}{b_2 \cdot C} \tag{4.18}$$

$$\omega_{z1} \cdot \omega_{z2} = \frac{b_0 \cdot g^2}{b_2 \cdot C^2} \tag{4.19}$$

The positions of the complex zeros are anticipated to remain constant across various simulation conditions. However, the device values tend to vary when subjected to different simulation corners. Consequently, it is essential to design the g_m stages in such a manner that both the numerator and denominator in Equation 4.18 and Equation 4.19 exhibit consistent spreading behavior at different simulation corners.

Table 4.7 provides insights into the impact of temperature and different technology corners on various devices.

Table 4.7: Temperature and corner influence on different devices

		Resistance	Capacitance	g_m of NMOS	g_m of PMOS
Temperature	$25°C$	-	-	-	-
	$-40°C$	Higher	Lower	Higher	Lower
	$85°C$	Lower	Higher	Lower	Higher
Corner	Typical	-	-	-	-
	Slow	Higher	Higher	Lower	Lower
	Fast	Lower	Lower	Higher	Higher

Through simulation, it has been observed that the influence of different technology corners on device values is more significant compared to temperature variations. Based on the analysis of Equation 4.18, Equation 4.19, and Table 4.7, it can be concluded that in order to minimize variations in the positions of the complex zeros, the value of the g_m stages should be determined by using resistors, specifically by employing source degeneration techniques.

Figure 4.15 illustrates the circuit schematic of G_1 and G_2 stage, which incorporates a bias circuit and a folded cascode opamp. As both G_1 and G_2 are connected to a capacitor load, it necessitates a high output impedance to position the poles at the origin. Therefore, a cascode configuration is implemented.

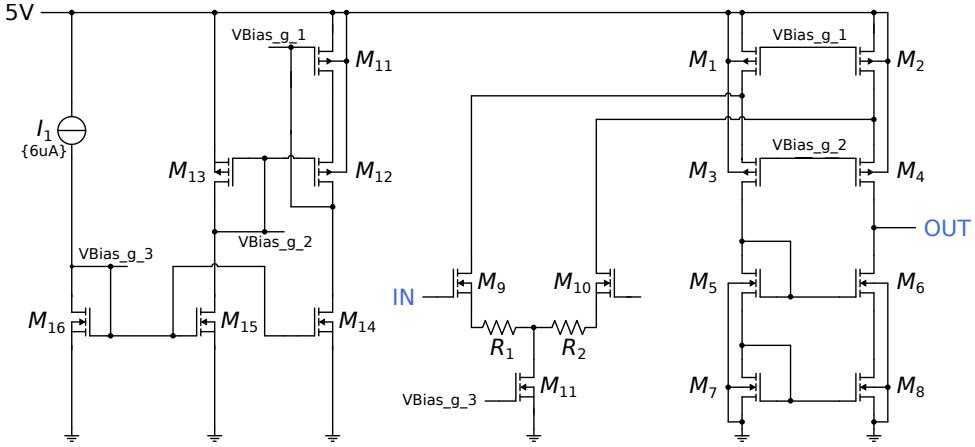


Figure 4.15: Circuit schematic of G_1 and G_2.

The challenge arises from the requirement to simultaneously achieve a lower current noise floor and a higher output swing. A low g_m/i_d value is preferred for minimizing the current noise floor. Conversely, a higher g_m/i_d value is desirable for attaining a larger output swing. Consequently, the design process necessitates a careful balance between these two requirements.

Figure 4.16 depicts the circuit diagram of the transconductance stages, namely G_3, G_4, and G_5. These three stages serve as adders for the error signal, the output following the first integrator, and the output subsequent to the second integrator, respectively. Moreover, they share comparable prerequisites in terms of input swing, output swing, and output impedance. Consequently, they are implemented using the same configuration. However, each stage possesses distinct transconductances, with variations in transistor sizes and resistor values to accommodate these differences.

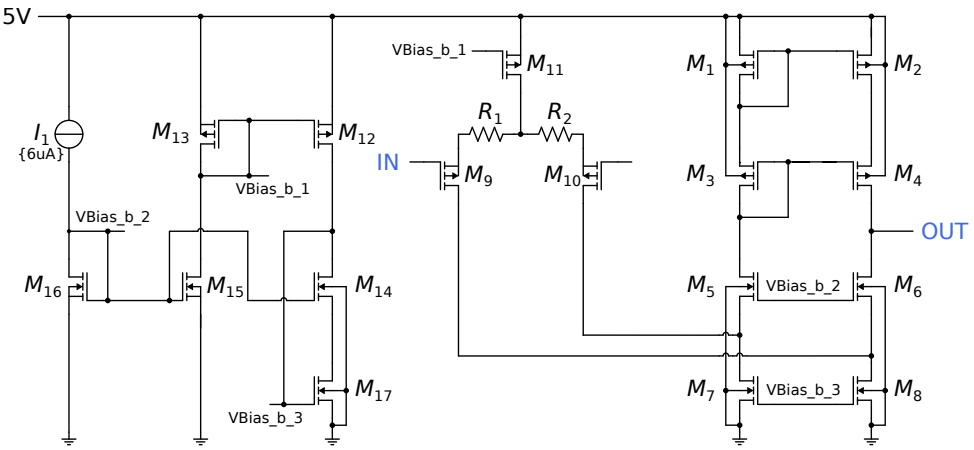


Figure 4.16: Circuit schematic of G_3, G_4, and G_5.

The challenge posed by G_3, G_4, and G_5 arises from their output biasing at 1.75 V, which is the midpoint of the triangular waveform. To achieve an output swing of $V_{pp} = 2.5$ V, the cascode NMOS of the folded cascode operational amplifier in Figure 4.16 needs to be biased in weak inversion, ensuring a saturation current below $100m$ V. This requirement necessitates a high g_m/i_d value and a larger transistor size, which, in turn, makes it challenging to concurrently achieve a high output impedance.

Figure 4.17 shows the simulation results of the output waveform in the time domain under different temperature conditions and technology corners.

The negative feedback class D amplifier ensures stability across various technology corners, thereby validating the effectiveness of both the negative feedback loop design and the employed g_m stages.

Finally, the negative feedback loop is applied on a conventional PWM-based class D amplifier, as shown in Figure 4.18. The power stage of the class D amplifier is powered by a $24V$ supply while the other parts are powered by a $5V$ supply. For purposes of comparison, the left channel of the chip is integrated with the designed negative feedback loop, whereas the right channel is not.

Figure 4.19 shows the THD results versus the output power of the complete negative feedback class D amplifier. The blue line denotes the right channel of the amplifier which is without feedback loop while the orange line denotes the left channel which is with the designed feedback loop. This design achieves a -111.8 dB THD when the output power is 1 W and around 40 W output power when THD is 10%.

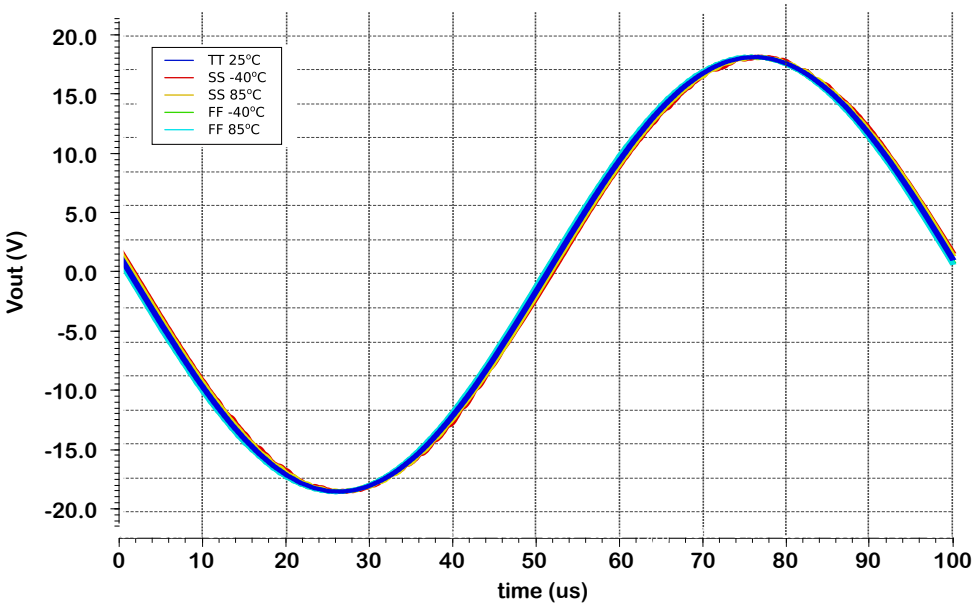


Figure 4.17: Corner simulation results of the output waveform.

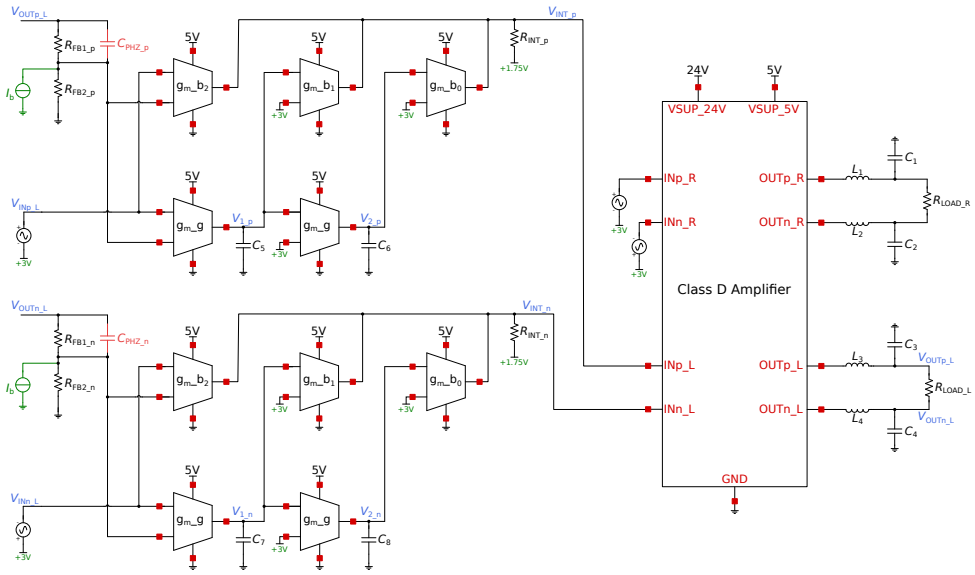


Figure 4.18: Top view schematic of negative feedback class D amplifier.

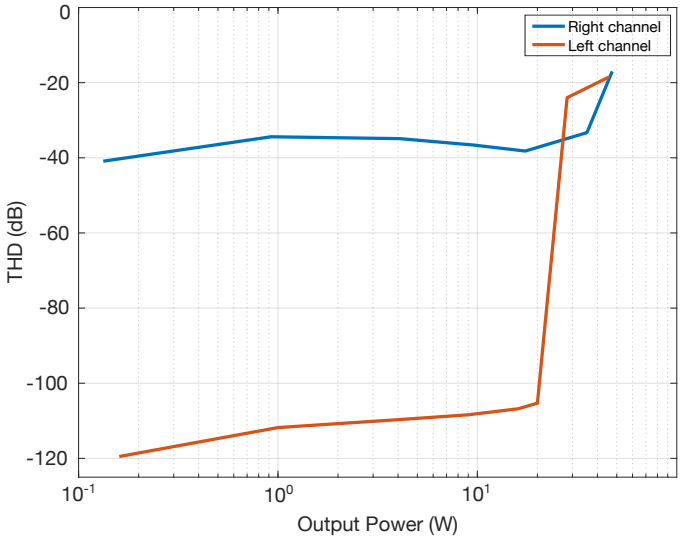


Figure 4.19: THD vs output power with $1k\ Hz$ input.

The voltage limiter, illustrated in Figure 4.20, engages in action when the amplifier experiences overdrive conditions. This limiter comprises two divergent pathways, each featuring a series of NMOS transistors with connected source and gate terminals. Consequently, the NMOS transistors remain in the off state, leaving only the body diodes to operate.

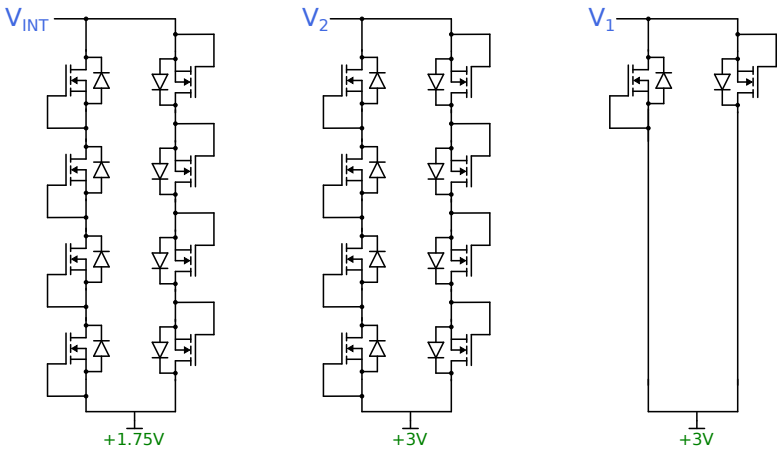


Figure 4.20: Voltage limiter.

When the amplifier is overdriven, the output signal undergoes clipping, leading to

an incremental buildup of voltage across the capacitor. As this voltage surpasses the threshold voltage of the body diode, current flows through the voltage limiter, preventing any internal voltage nodes from reaching infinity.

Figure 4.21 depicts the clipping performance of the amplifier. Notably, it illustrates a smooth recovery from the overdriven state back to the normal operating condition.

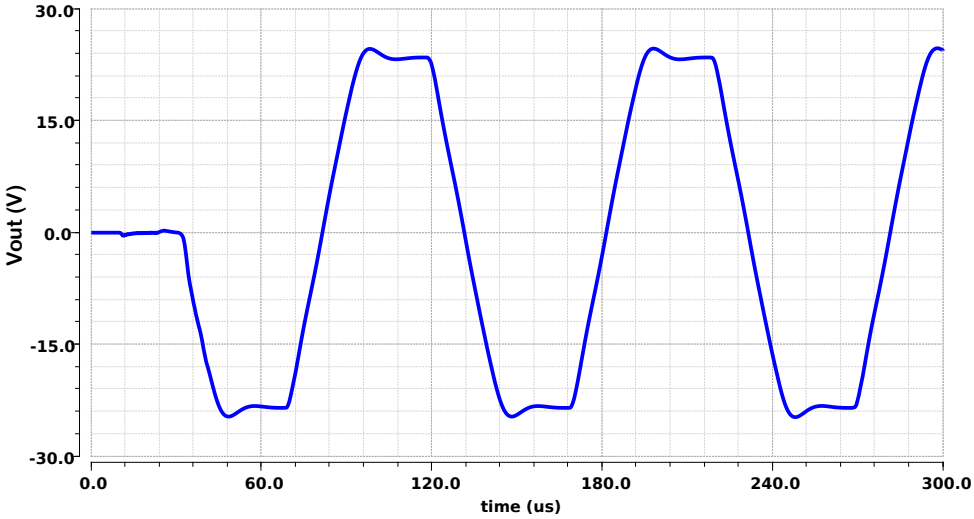


Figure 4.21: Transient simulation results when the amplifier is overdriven.

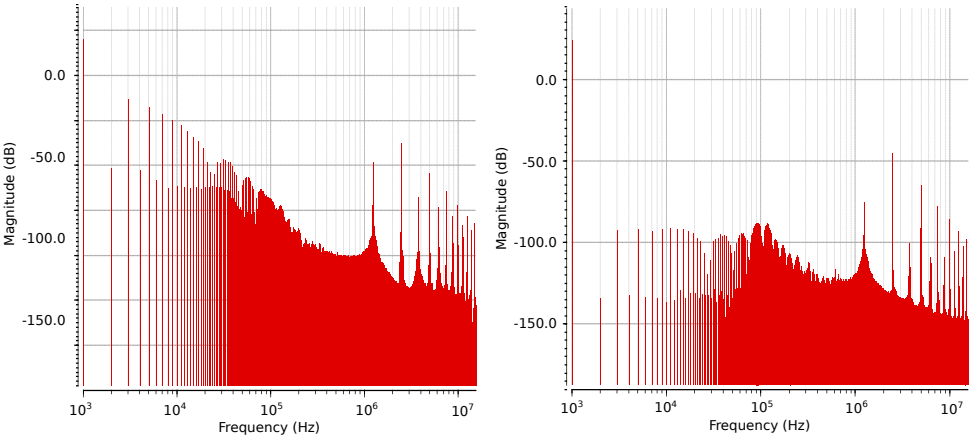
DISCUSSION

In the negative feedback amplifier, the distortion in the loop is expected to be reduced by the amount of loop gain, as expressed by Equation 4.20,

$$V_{out,d} = \frac{V_d}{1+L} \tag{4.20}$$

where $V_{out,d}$ represents the distortion observed at the output, V_d represents the distortion generated in the loop and L is the loop gain.

Therefore, the difference in the magnitude of the harmonics between the open-loop FFT plot, as shown in Figure 4.22a, and the closed-loop FFT plot, as shown in Figure 4.22b should equal the corresponding loop gain magnitude. The input is a $1k\ Hz$ sinusoidal signal.



(a) open-loop (b) closed-loop

Figure 4.22: FFT plot of the output waveform.

However, the observed reduction in distortion for each harmonic is notably less than expected, as evidenced by the data presented in Figure 4.23.

Two potential explanations for the less reduction in distortion are as follows:

1. Given that class D amplifiers operate on a switching principle, it is possible that Equation 4.20 does not hold true in the context of switching-based amplifiers like class D amplifiers.
2. Another possible explanation could be that new forms of distortion are introduced into the system following the implementation of a negative feedback loop.

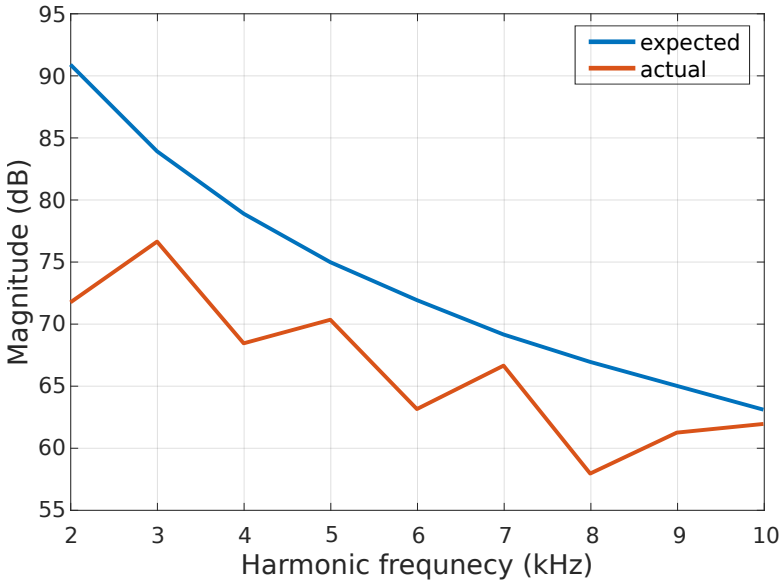


Figure 4.23: Expected distortion reduction and actual distortion reduction.

Paper [9] and [10] offer insights from the frequency domain perspective. In the closed-loop class D amplifiers, the negative feedback loop introduces an additional form of distortion termed "PWM-residual-aliasing distortion" or "PWM-intermodulated distortion." Those PWM residuals will be feedbacked to the input and be modulated by the triangular waveform. Consequently, these modulated PWM residuals can lead to aliasing distortion within the audio bandwidth.

Therefore, due to the switching characteristics of Class D amplifiers, the negative feedback loop introduces new kinds of distortion while reducing THD, causing the inapplicability of Equation 4.20 and the difference between the expected and actual performance in Figure 4.23.

Potential resolutions involve increasing the switching frequency or extra filtering of the ripple component. Employing compensation techniques to cancel the PWM-residual-aliasing distortion also helps. However, these strategies introduce complexities to the overall circuit design and elevate power consumption. The selection of design priorities should be a result of conscientious consideration of practical necessities and associated trade-offs.

4.5. CONCLUSION

This chapter introduces a systematic approach to designing a negative feedback loop with the objective of reducing distortion. The design process employs a straightforward two-step methodology without design iterations during the conceptual design phase. The utilization of the phantom zero technique, functioning both as a means of loop stabilization and achieving a more flat transfer function response, is a notable aspect. The simulation results validate the functionality of the entire circuit across diverse temperature conditions and technology corners. The outcome of these simulations yields a THD value of $-111.8\ dB$ when the output power is $1\ W$.

Nonetheless, it's important to acknowledge that the negative feedback loop, even with an infinitely high loop gain, cannot eliminate all forms of distortion within class D amplifiers. This limitation stems from the inherent switching attributes of Class D amplifiers. The introduction of a negative feedback loop in such amplifiers can simultaneously give rise to novel distortion components, thus adding complexity to the distortion.

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5

CONCLUSION

In this thesis, two THD reduction techniques are presented. The project began with the analysis of the distortion mechanisms in class D amplifiers. The distortion generated in the power stage was mainly focused on, such as deadtime distortion and rising and falling time distortion. The compensation technique in Chapter 3 was based on the analysis of the distortion mechanisms and involves the modified triangular waveform to reduce THD. The compensation concept was proven to be effective with a 12 dB THD improvement compared with the conventional class D amplifier in the concept verification section.

Chapter 4 described the feedback technique. The negative feedback loop included a second-order controller and an LC filter, together with the conventional class D amplifier. A phantom zero was created in the feedback path to stabilize the whole loop while making the transfer function more flat. The achieved results are shown in Table 5.1.

Table 5.1: Achieved results

Specification	**Target**	**Achieved**
Switching frequency	1.2MHz	1.2MHz
Supply voltage	24V	24V
Load	BTL 8Ω	BTL 8Ω
THD (1kHz, 1W)	<-90dB	-111.8dB
Max output power (1kHz, 10%THD)	30W	40W

FUTURE WORK

- For the compensation chapter, the results can be better if the small input situation is also considered, where the ripple current cannot be ignored.
- For the feedback chapter, since the negative feedback loop also introduces new kinds of distortion, it may be possible to incorporate the modified triangular waveform in Chapter 3 as a feedforward path with the feedback loop.