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Extending the Open-Short de-embedding frequency via metal-1 on-wafer calibration approaches

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***Abstract* — In this contribution, we analyze the bandwidth versus accuracy trade-offs of conventional two-step de-embedding approaches, often employed to extract the device model parameters. The accuracy limitation of incorporating the pad/line section of classical DUT test-fixtures into shunt-series complex and frequency-dependent elements is analyzed by means of linear circuit simulations and EM parametric analysis. The de-embedding accuracy is then evaluated by employing 3D surfaces to include both the frequency and the geometrical dependency. To validate the presented analysis, classical device monitoring parameters are extracted versus frequency for the same nMOS device embedded in two different fixtures. One topology only supports pad level calibration, thus including the fixture pad/line section in the de-embedding process. The second topology allows a direct on-wafer calibration (reference plane set on metal-1 in close proximity to the DUT) thus minimizing the residual parasitics to be removed by the de-embedding step. Experimental data are then presented and compared to simulation test benches to highlight the improved consistency of the extracted model parameters of the metal-1 calibration approach up to 220GHz.**

***Index Terms* — [Calibration, De-embedding, mm-wave, Open-Short].**

I. Introduction

Silicon-based technologies (i.e., SiGe HBTs and CMOS SOI) are being proposed as high-performance and complete technology platforms (from the device offering standpoint) to address the needs of upcoming (sub)mm-wave applications, such as beyond 5G and next-generation automotive radar systems.

Nevertheless, the device parameters representing the technology performance metrics, which are being advertised to promote the usage of these technologies, are determined from measurements performed typically (well) below 100 GHz.

Therefore, the technology metrics and device models need to be validated at the frequencies targeted by future applications. To achieve this goal, the semiconductor industry has employed the following approach for extracting the device parameters: embed the device in a (preferably) low-parasitics test fixture, realize a set of dummy fixtures to extract a lumped model of them (i.e., short, open), and then remove the effect of the fixture from the measured data to achieve the device response [1]. While this approach has been, and continues to be, the standard for device (model) parameter extraction, it provides significant limitations when the characterization goal shifts to model validation in the (sub)mm-wave frequency range. The reason for this is to be found in the trade-off between fixture model complexity (i.e., number of fixture elements and required dummy structures) and its frequency validity. As an example, when frequencies approach 200 GHz, the time delay across the pad-line section of the test fixture becomes comparable (i.e., same order of magnitude) to the rise-time of the signal. This is often considered the limit of lumped model representation. When examining this limit from the fixture design perspective, the required pad dimension (i.e., fixed by today's RF probe technologies) and the line section length to the input/output of the DUT (i.e., required to adapt the same RF fixture size to different device sizes), are the most significant contributors for the frequency limitation of the conventional two-step de-embedding approach [1].

In order to expand the frequency validity of lumped-based fixture de-embedding, several techniques with an increased number of elements have been presented in the literature [2][3][4]. Nevertheless, the real-estate penalties required from the increased number of dummies and the limitation arising from the calibration transfer errors at (sub)mm-wave frequencies [5][6] make these approaches sub-optimal.

In this contribution, we analyse the frequency limitation of the two-step de-embedding approach first employing a parameterized fixture model in a circuit simulator and then validating the trend using a 2.5D EM parametric simulation. Then, we compare the modelling accuracy achieved by a conventional fixture-based de-embedding approach, where the primary calibration reference plane is set at the pad levels, with the case of a Metal-1 (M1) calibration approach where the primary calibration is set in close proximity to the DUT interface [7]. The latter approach minimizes the residual parasitics to be removed with the open-short de-embedding, thus expanding the frequency range validity of the de-embedding technique. Finally, the experimental results of the two approaches are compared up to 220GHz using the same device embedded in the two different fixture topologies.

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II. Lumped Fixture Modelling

The classical test-fixture topology to interface the device with the measurement environment (i.e., RF probes), for the extraction of device model parameters, can be generalized as shown in the sketch in Fig. 1 a). For this test-fixture topology the reference plane of the first-tier calibration (red line) is located at the ground-signal-ground pad interface, while the device (terminal) plane is located at the DUT interface (black line).

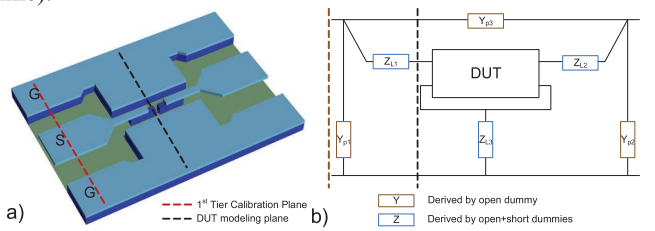


Fig. 1: (a) Simplified sketch of a test fixture for DUT characterization, (b) lumped model of the test fixture based on the open-short de-embedding technique.

In the conventional open-short technique, shown in Fig. 1 b), the open and a combination of the open and the short dummies are used to extract the shunt element of the fixture (brown) and the series one (blue), respectively. The size of the pad with the line length will determine the (frequency-dependent) parameters that will compose the lumped test fixture model.

In order to study the impact of the fixture parasitics on the accuracy of its lumped model frequency response, a simulation environment in Keysight ADS was created, shown in Fig. 2.

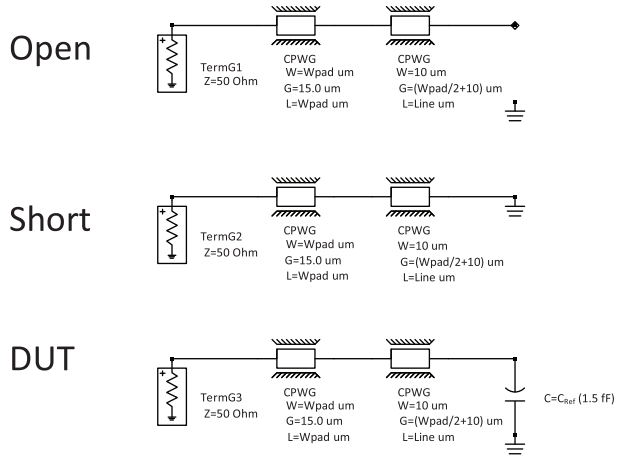


Fig. 2: ADS circuit simulation schematic, representing the open and short (dummies) structures and the intrinsic DUT (C_{Ref} of 1.5fF) embedded in the pad/line fixture for a single port.

By using the CPWG component (i.e., grounded CPW) from the ADS library, the pad-line topology of the conventional fixture (see Fig. 1 a) can be easily recreated, as shown in Fig. 3, for different pad (Wpad) and line-section (Line) sizes.

Employing the simulation approach described in Fig. 2 and the classical approach of the open-short de-embedding formulation [1], we can quantify the error in the extraction of the reference Capacitance (C_{Ref}) versus frequency and the dimension parameter. It is important to note that the derived error will only relate to the frequency limitation of the lumped model approximation, since the open and short conditions used in the simulation dummies are ideal terminations.

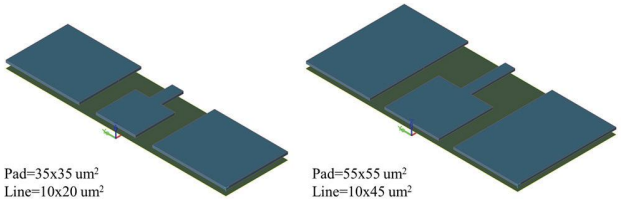


Fig. 3: Layout view of the two sections of CPWG from Fig. 2, with different sizes of the pads and lines.

The relative error in the computed C_{Ref} versus Wpad and frequency is plotted as a 3D surface in Fig. 4 a.

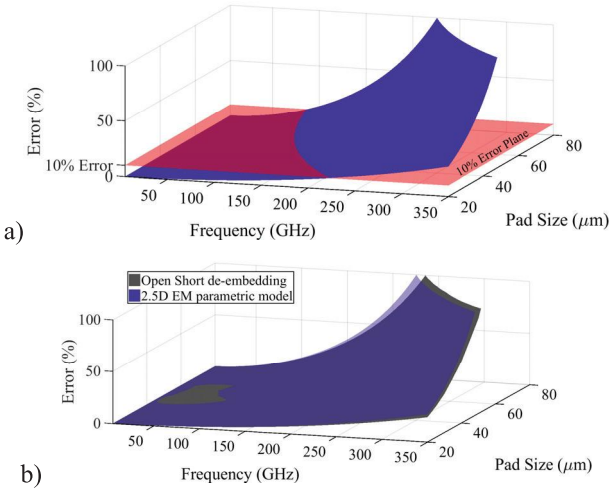


Fig. 4: Surfaces representing the CRef error using the CPWG circuit model for open-short de-embedding versus frequency and the varying (square) size of the pad (a) and a comparison to the deembedding error applying open-short elements extracted from 2.5D EM simulated pad/line fixture instead (b).

Since the simple CPWG model does not account for the pad line discontinuity, a 2.5D EM simulation, employing the same parametric sweep (Wpad), was performed on the layout shown in Fig. 3, and the 3D results are presented in Fig. 4 b).

Overlaying on the 3D surface a constant (error) plane at a given percentage error (i.e., 10% in Fig. 4a)), we can easily identify the limit frequency for a given dimension of the pad/line of the fixture. Moreover, observing the agreement between the two simulation approaches (CPWG model and 2.5D EM, Fig. 4b)), we can conclude that the error due to the lumped two elements approximation is the dominant error in the open-short de-embedding approach.

To further prove that the main limitation of the two-element model arises from the frequency limitation versus the parasitic element value of the fixture, the circuit schematic, shown in Fig. 5, is created in ADS. Here the shunt/series elements

provide the frequency-dependent complex values as extracted by the open-short de-embedding algorithm.

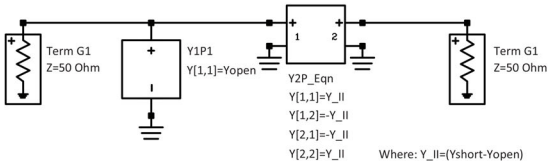
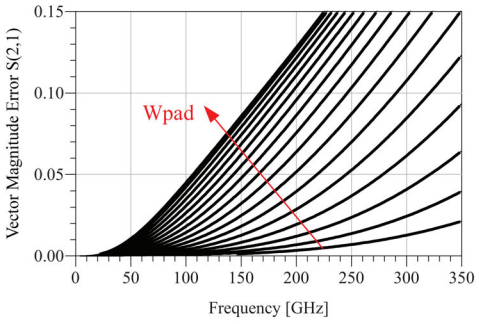
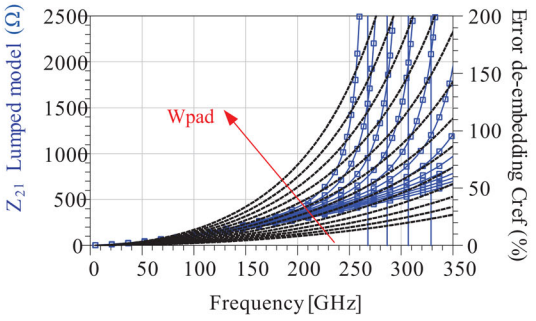


Fig. 5: Two-port circuit model composed of frequency-dependent admittances of the one-port fixture shown in Fig. 2.

The error in the transmission of the lumped model of Fig. 5 can be evaluated using an error vector magnitude metric of the S_{21} parameter compared to the true response of the pad line CPWG section and is visualized in Fig. 6 a).



a)



b)

Fig. 6: a) Vector magnitude error of the lumped model versus CPWG representation of Fig. 2 with Wpad variation between 20 and 80 μm^2. b) Magnitude of the Z_{21} parameter (blue) of the lumped fixture overlayed with the error of the extracted de-embedded Cref (black).

In Fig. 6 b), the error in the de-embedded C_{Ref} is shown versus frequency for the various Wpad dimensions. Moreover, the graph indicates how the peak error in the de-embedded C_{Ref} can be correlated to the resonance, induced by the model, of the transmission parameter.

III. M1 On-Wafer Calibration Fixture

From Fig. 4 a), it can be seen that in order to obtain accurate device-level data at frequencies up to 300 GHz (i.e., error of a few %), while employing simple open-short de-embedding, requires the parasitic of the pad-line section to be absorbed in the calibration path. To achieve this, a device fixture as shown in Fig. 7 should be employed. The design and concept of such a fixture were extensively described in [7]. The reference plane of the calibration then is placed in closed proximity to the device (thus the M1 name), substantially reducing the remaining test fixture parasitics to be removed.

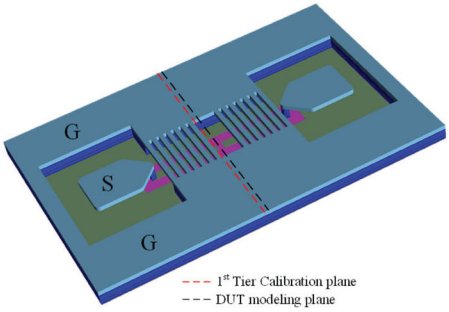


Fig. 7: Example of a device test fixture supporting M1 on-wafer calibration.

The large reduction in lumped element values from the classical Fig. 1 a) versus the M1 fixture Fig. 7 are experimentally quantified in the WR5 band, and the results are shown in Fig. 8.

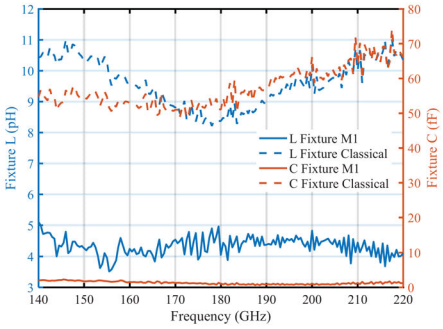


Fig. 8: Measured lumped (frequency-dependent) capacitance and inductance for the classical fixture (dashed lines) and for the M1 fixture (solid lines).

IV. Experimental Results

The presented analysis was applied to a state-of-the-art CMOS FDSOI technology. Two different fixtures, i.e., a classical fixture (as depicted in Fig. 1) and an M1 calibration fixture (as depicted in Fig. 7) were implemented.

Three device-level RF performance metrics were analyzed to compare the results of the two test fixtures with the intrinsic device model (from foundry PDK). Moreover, the frequency error arising from the usage of the classical fixture on the three RF FoMs was evaluated using a simulation test-bench as the one presented by the authors in [8]. The results of this comparison are shown in Fig. 9.

For all the three RF FoMs the frequency expansion of the metrics evaluated from the test bench simulation (red curve) is experimentally supported by a distinct expansion in the frequency signature of the WR5 measured data employing the classical test fixture approach. When using the M1 calibration test fixture to extract the RF FoMs, for the same device

topology, a frequency behavior in line with the foundry PDK model is then found.

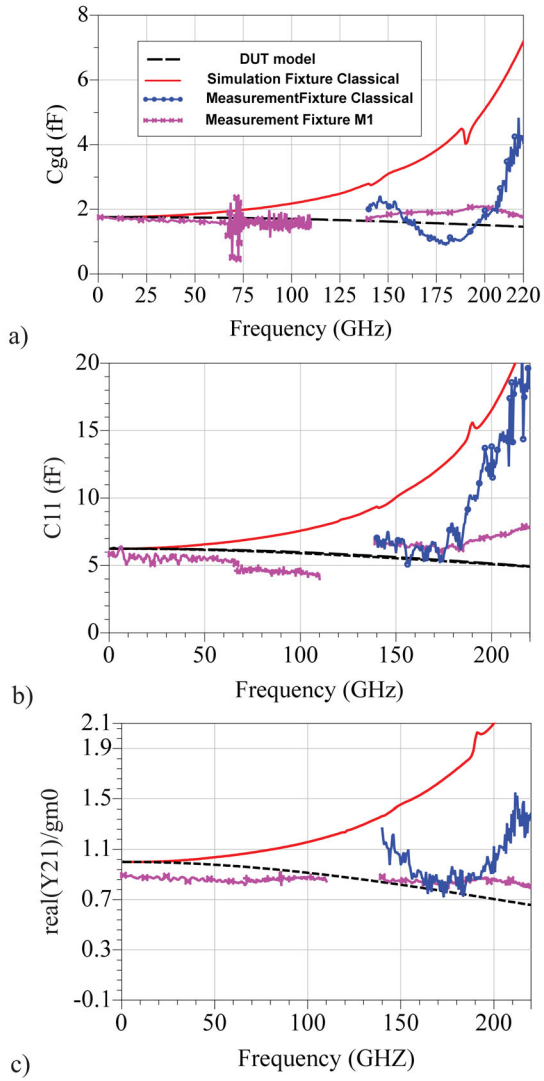


Fig. 9: Technology performance metrics evaluated from transistor model (black dashed lines), simulated classical fixture (red lines), experimental for classical fixture (blue lines) and for experimental from M1 fixture (violet lines): a)gate-drain capacitance C_{gd}, b)input capacitance C_{11}, c) real part of Y_{21} normalized to the low frequency current gain.

It is worth noting that the experimental data of the RF FoMs contain various sources of error, and the de-embedding is only one of such sources. For this reason, no claim is made on the absolute accuracy of the values. Nevertheless, the frequency signature of the various traces and their comparison with the predicted test-bench behavior and the model provides strong evidence to support the presented analysis of the frequency-related error of the classical open-short de-embedding approach based on a lumped fixture model.

Note, that only the WR5 band data is presented for the classical fixture due to an extremely small probe pitch (i.e., 50um) which was available in the laboratories of the authors only in that frequency range.

V. Conclusion

In this paper, we presented a circuit level and a 2.5D EM simulation analysis to describe the frequency limitation of conventional open-short de-embedding approaches. The impact of the fixture size on the accuracy of the de-embedded device level parameter is presented. The usage of a test fixture to support direct on-wafer calibration approaches down to M1 is proposed to absorb the pad level parasitic in the first-tier calibration. The comparison of the RF performance metrics of the same device embedded in the two described test fixtures provided experimental validation of the limitation of the open-short de-embedding approach when applied using conventional pad level (first-tier) calibration test fixtures. The simple open-short de-embedding can provide accurate extracted parameters when coupled with a low-parasitic fixture, i.e., employing an M1 test fixture.

Acknowledgment

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